MOP-AV204A

Parallel Display Specifications

Revision 1.0

Revision History

Revision	Description	Author
1.0	Initial Release	Clark

Contents

Features

The Matrix Orbital Parallel display series offers a low cost display solution utilizing an industry standard communication interface for simple integration into a wide variety of new and existing applications. The luminous text with configurable brightness and a variety of filter options allow the MOP Vacuum Florescent Display line to offer a robust yet stylish display solution for any project. The standard alphanumeric font set also allows up to eight custom characters to be saved in display Random Access Memory for a custom design touch.

Hardware

Drawing

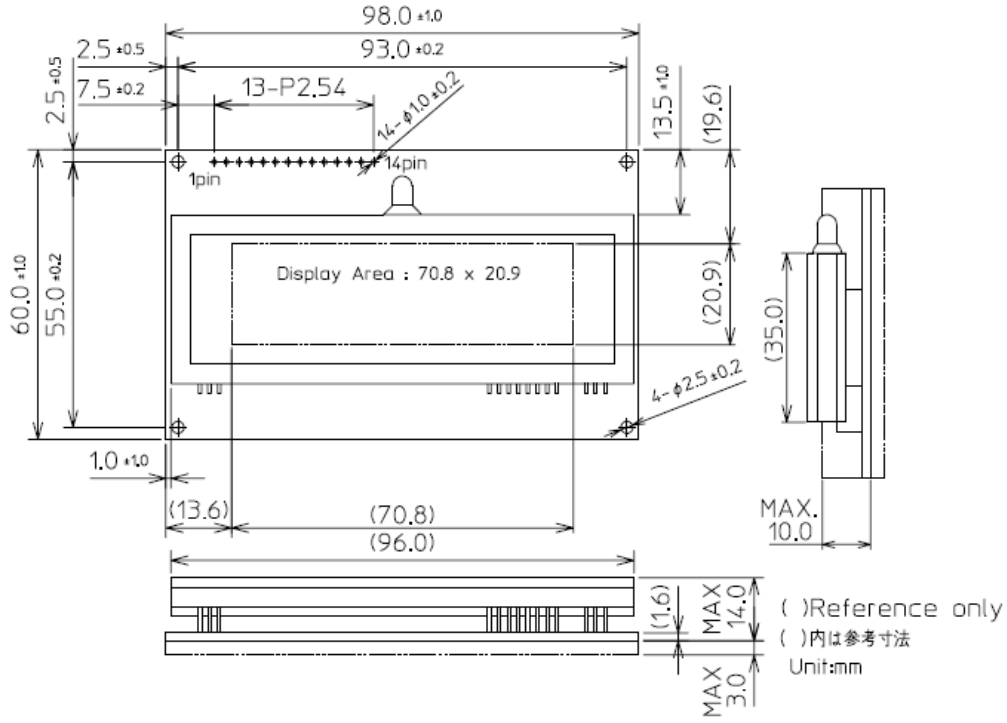

Figure 1: MOP-AV204A Mechanical Drawing

Interface

Table 1: Display Control

Pin	Symbol	Description
1	V_{SS}	Ground
2	V_{CC}	Supply Voltage
3	NC	No Connect
4	RS	Register Select
5	R/W	Read/Write
6	E	Enable

Table 2: Parallel Data

Pin	Symbol	Description
7	DB0	*Data bit 0
8	DB1	*Data bit 1
9	DB2	*Data bit 2
10	DB3	*Data bit 3
11	DB4	Data bit 4
12	DB5	Data bit 5
13	DB6	Data bit 6
14	DB7	Data bit 7

***Note:** Not used in 4-bit mode

Instructions

Outline

The MOP line is controlled using a standard HD44780 compliant controller. The display is enabled by pulling the Chip Enable (E) pin high, communication to and from the device is controlled using the Read/Write (R/W) input, and one of two available 8-bit registers are selected via the Register Select (RS) line. Using Register Select, either the Instruction Register (IR) or Data Register (DR) is selected by toggling RS low or high respectively.

While executing from the IR, the display will pull the Most Significant Bit of the data bus, DB7, high. While this Busy Flag (BF) is set, any instructions sent to the unit will be ignored. The status of this flag and the current position of the Address Counter (AC) can be obtained by performing a read operation on the instruction register at any time.

Table 3: Register Selection

RS	R/W	Operation
0	0	IR write as an internal operation (display clear, etc.)
0	1	Read busy flag (DB7) and address counter (DB0 to DB6)
1	0	Write data to DDRAM or CGRAM (DR to DDRAM or CGRAM)
1	1	Read data from DDRAM or CGRAM (DDRAM or CGRAM to DR)

When writing for the DR, one of two locations can be chosen using the AC. The value provided to the AC when executing a set address command differentiates these locations. The AC is automatically decremented or incremented after a read or a write.

DDRAM provides eighty bytes of display memory to all displays. Memory outside the bounds of the display area can be used as general RAM. DDRAM addressing begins at the top left of the display with a value of 0, addresses then increment from left to right then down once a row is filled.

Table 4: Two Line Addressing

Position	1	2	...	40
DDRAM Address	00	01	...	27
	40	41	...	67

Table 5: Four Line Addressing

Position	1	2	...	20
DDRAM Address	00	01	...	13
	40	41	...	53
	14	15	...	27
	54	55	...	67

CGRAM provides eight custom characters that can be created by writing to CGRAM locations then displayed using the first eight CGROM character codes, as seen in the character ROM table below.

Characters are sent to the display by performing a write operation on the DR using the correct character address within CGROM. Instructions are issued by writing to the IR; a complete list is available below.

Instruction Table

Table 6: Parallel Instruction Table

Instruction	Instruction Code										Description
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Clear Display	0	0	0	0	0	0	0	0	0	1	Write “20H” to all DDRAM locations, set DDRAM address to “00H”, return cursor to its original position, and set I/D to “1”.
Return Home	0	0	0	0	0	0	0	0	1	—	Set DDRAM address to “00H” and return cursor to its original position if shifted. The contents of DDRAM are not changed.
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	SH	Assign cursor moving direction and enable the shift of entire display. DDRAM and CRAM addresses are incremented and cursor moves right when I/D is set to “1”, the opposite is true when reset to “0”. Setting SH to “1” causes the entire display to shift affecting only DDRAM.
Display ON/OFF Control	0	0	0	0	0	0	1	D	—	B	Set display (D), and blinking of cursor (B) on/off control bit. Setting D or B to “1” will cause the display or blinking cursor to turn on; the opposite is true for reset.
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	—	—	Set cursor moving and display shift control bit, and the direction, without changing of DDRAM data. Setting S/L to “1” will shift the screen horizontally while the opposite will move the cursor through all screen positions. Setting R/L to “1” will shift right immediately. AC and DDRAM are not altered.
Function Set	0	0	0	0	1	DL	—	—	—	—	Set interface data length. Setting DL to “1” specifies 8-bit mode, “0” 4-bit.
Set Brightness	1	0	—	—	—	—	—	—	BR1	BR0	<table><tr><th>BR1</th><th>BR0</th><th>Brightness</th></tr><tr><td>0</td><td>0</td><td>100% (Default)</td></tr><tr><td>0</td><td>1</td><td>75%</td></tr><tr><td>1</td><td>0</td><td>50%</td></tr><tr><td>1</td><td>1</td><td>25%</td></tr></table>
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter.
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter.
Read Busy Flag and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Read the status of the display controller through the BF Bit. The contents of address counter can also be read.
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM), location is determined by the AC. AC and display shift are adjusted as specified.
Read Data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM), location is determined by the AC, set command is recommended previous to this. Only AC is adjusted.

Character ROM

The character generator ROM stores up to two hundred fifty-six 5×7 dot character patterns from 8-bit character codes. The first sixteen characters are reserved for custom characters saved in CGRAM.

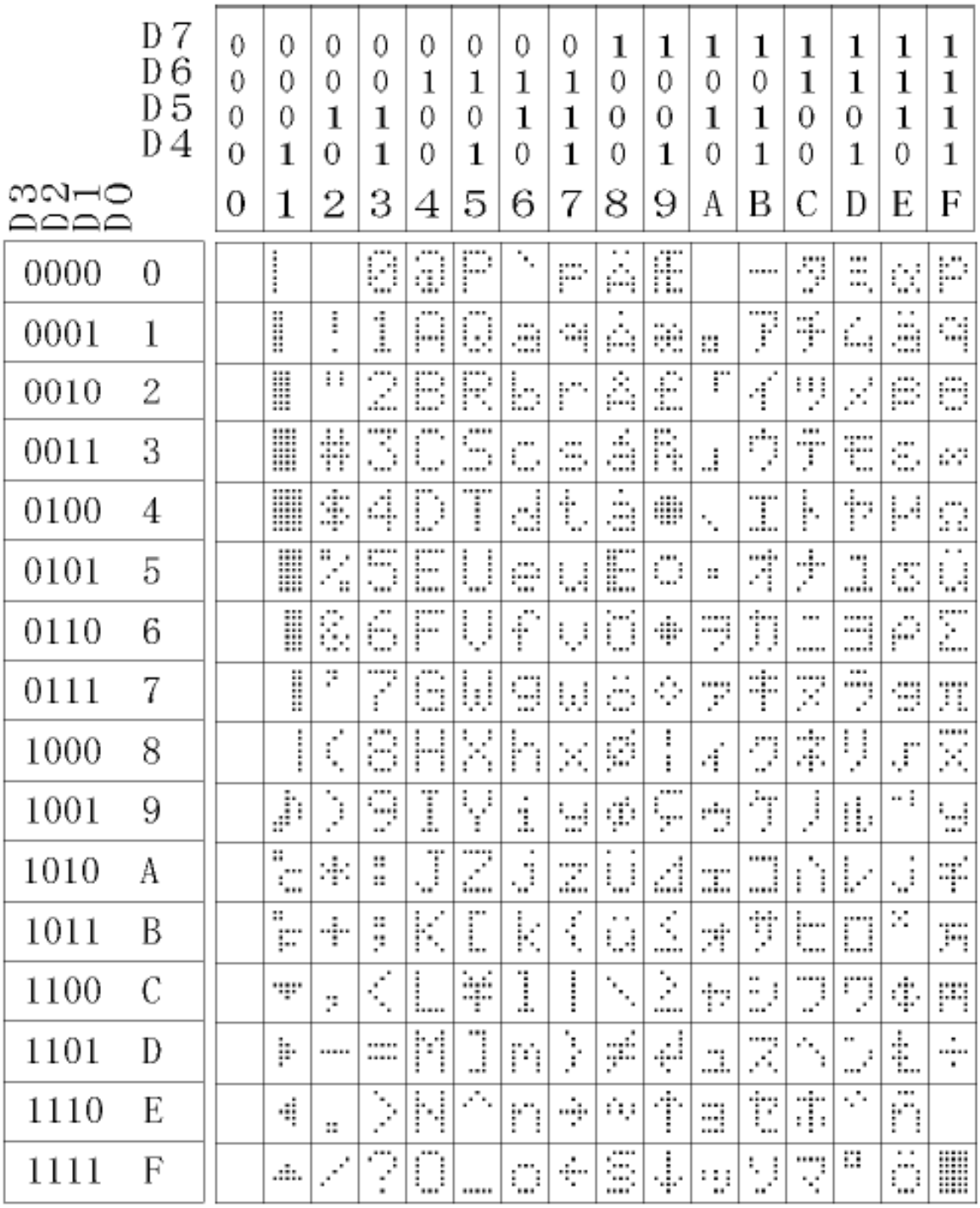

Figure 2: Japanese Character Set

Character RAM

CGRAM allows the creation of up to eight 5x7 character patterns. Eight bytes are assigned to each character address, the least significant five bits of which represent the five pixel columns. Pixels are activated by setting the bit in their position in CGRAM to "1".

Each character has eight addresses in CGRAM corresponding to each of its eight pixel rows. The highest three bits represent the character address in DDRAM. The lowest three bits of this address represent the row positions beginning with 0 at the top.

Finally, each character can be referenced in DDRAM and written to the screen using its eight bit character code. Note that each character is addressable by two codes.

Table 7: Relationship between CGRAM Addresses, Character Codes (DDRAM Data) and Character Patterns (CGRAM Data)

Character code	CG RAM address						CG RAM data (character pattern)							
	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
00H or (08H)	0	0	0	0	0	0	*	*	*	1	2	3	4	5
	0	0	0	0	0	1	*	*	*	6	7	8	9	10
	0	0	0	0	1	0	*	*	*	11	12	13	14	15
	0	0	0	0	1	1	*	*	*	16	17	18	19	20
	0	0	0	1	0	0	*	*	*	21	22	23	24	25
	0	0	0	1	0	1	*	*	*	26	27	28	29	30
	0	0	0	1	1	0	*	*	*	31	32	33	34	35
	0	0	0	1	1	1	*	*	*	0	0	0	0	0
01H or (09H)	0	0	1	0	0	0	*	*	*	1	2	3	4	5
	0	0	1	0	0	1	*	*	*	6	7	8	9	10
	0	0	1	0	1	0	*	*	*	11	12	13	14	15
	0	0	1	0	1	1	*	*	*	16	17	18	19	20
	0	0	1	1	0	0	*	*	*	21	22	23	24	25
	0	0	1	1	0	1	*	*	*	26	27	28	29	30
	0	0	1	1	1	0	*	*	*	31	32	33	34	35
	0	0	1	1	1	1	*	*	*	0	0	0	0	0

Note: * Indicates no effect.

Timing Characteristics

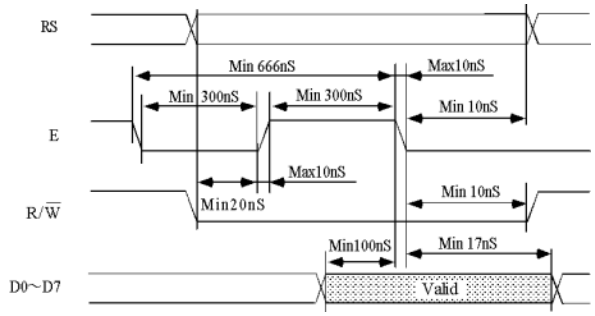

Figure 3: Write Timing Waveform

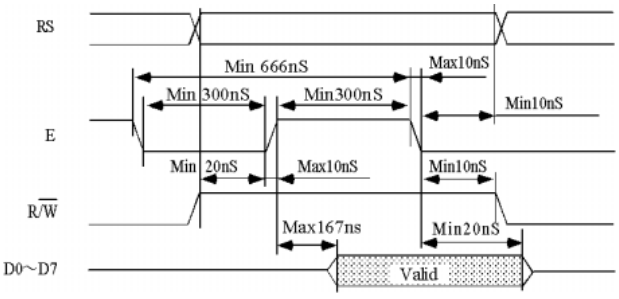

Figure 4: Read Timing Waveform

Initialization

Before beginning any application, it is recommended that all display settings be initialized. Below are algorithms for initializing the display in both 8-bit and 4-bit communication modes.

Before the first wait condition, please allow Vcc to rise to 2.7V then wait 40ms. During the three function set commands that follow, note that the busy flag cannot be checked; it becomes available in the last block. The unit will always expect a total of 8 bits to be sent, so note the structure used in four bit mode. The last initialization block will set the number of lines and character font as specified, turn the display off, issue the display clear command, and finally set the entry mode as desired.

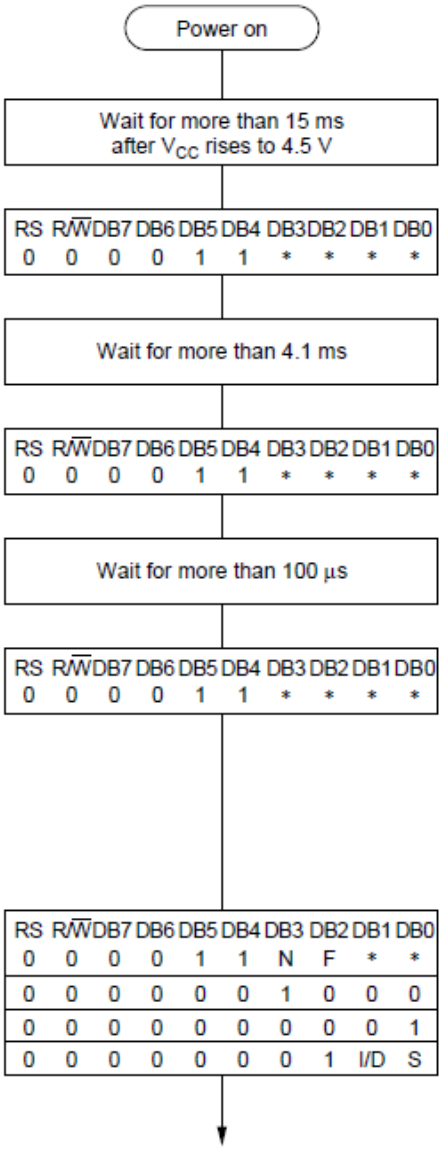

Figure 5: 8-bit Initialization

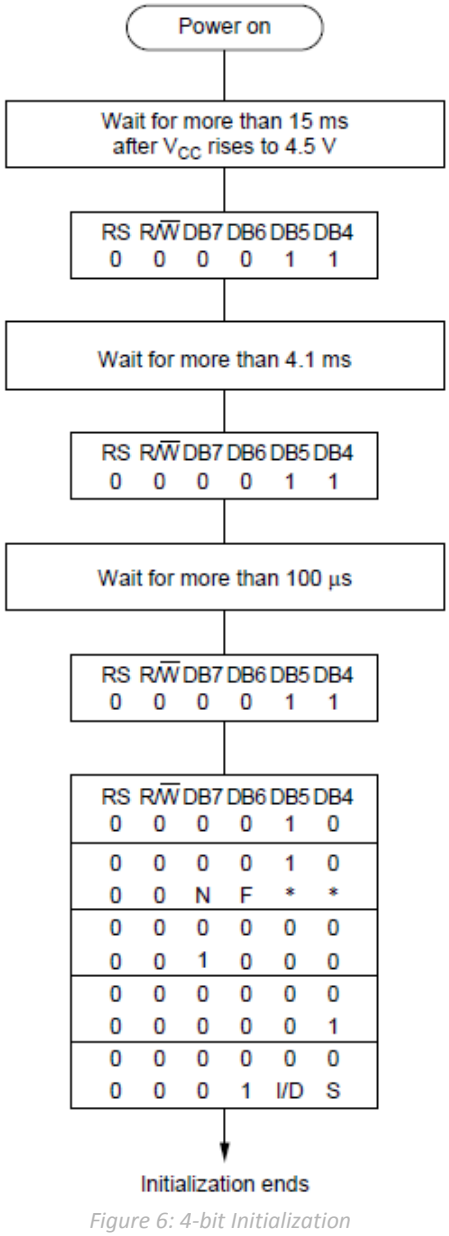

Figure 6: 4-bit Initialization

Note: * Indicates do not care condition.

Specifications

Electrical

Table 8: Electrical Characteristics

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage For Logic	V_{CC}	4.75	5.0	5.25	V
Input Data High Voltage (DB0-DB7)	V_{IH}	V_{SS}+2.2	—	V_{CC}	V
Input Data Low Voltage (DB0-DB7)	V_{IL}	V_{SS}	—	V_{SS}+0.6	V
Input Control High Voltage (RS,W/R,E)	V_{IH}	0.7V_{CC}	—	V_{CC}	V
Input Control Low Voltage (RS,W/R,E)	V_{IL}	V_{SS}	—	0.3V_{CC}	V
Supply Current (Display OFF)	I_{CC}	—	8.0	15	mA
Supply Current (Display ON)	I_{CC}	—	275	350	mA
Supply Current (Initial Inrush)	I_{CC}	—	550	700	mA

Optical

Table 9: Display Characteristics

Item	Dimension	Unit
Number of Characters	20 Characters x 4 Lines	—
Module dimension	98.0 x 60.5 x 17.0	mm
Active area	70.8 x 20.9	mm
Character size	2.40 x 4.70	mm
Character pitch	3.60 x 5.40	mm
Dot size	0.40 x 0.50	mm
Dot pitch	0.50 x 0.70	mm
Luminance	350	cd/m^2
Colour of Illumination	Green (Blue-Green)	

Environmental

Table 10: Environmental Specifications

Item	Symbol	Min	Max	Unit
Operating Temp.	Top	-40	85	℃
Storage Temp.	Tstr	-50	85	℃

Note: Maximum 80% non-condensing humidity.

Troubleshooting

Power

For your MOP Display to function correctly, appropriate power must be applied, often as indicated by the cursor or text illuminating. Please reference all voltages to the Initialization

Before beginning any application, it is recommended that all display settings be initialized. Below are algorithms for initializing the display in both 8-bit and 4-bit communication modes.

Before the first wait condition, please allow Vcc to rise to 2.7V then wait 40ms. During the three function set commands that follow, note that the busy flag cannot be checked; it becomes available in the last block. The unit will always expect a total of 8 bits to be sent, so note the structure used in four bit mode. The last initialization block will set the number of lines and character font as specified, turn the display off, issue the display clear command, and finally set the entry mode as desired.

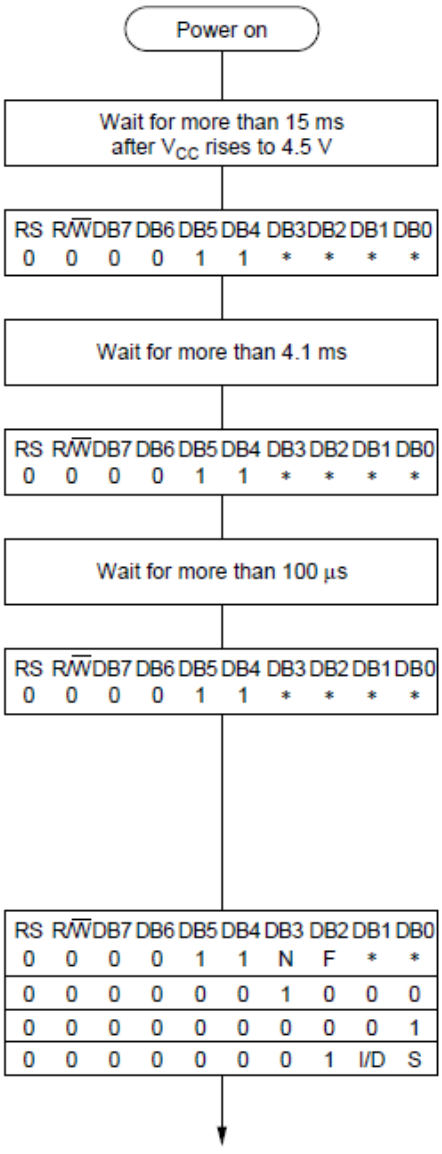

Figure 5: 8-bit Initialization

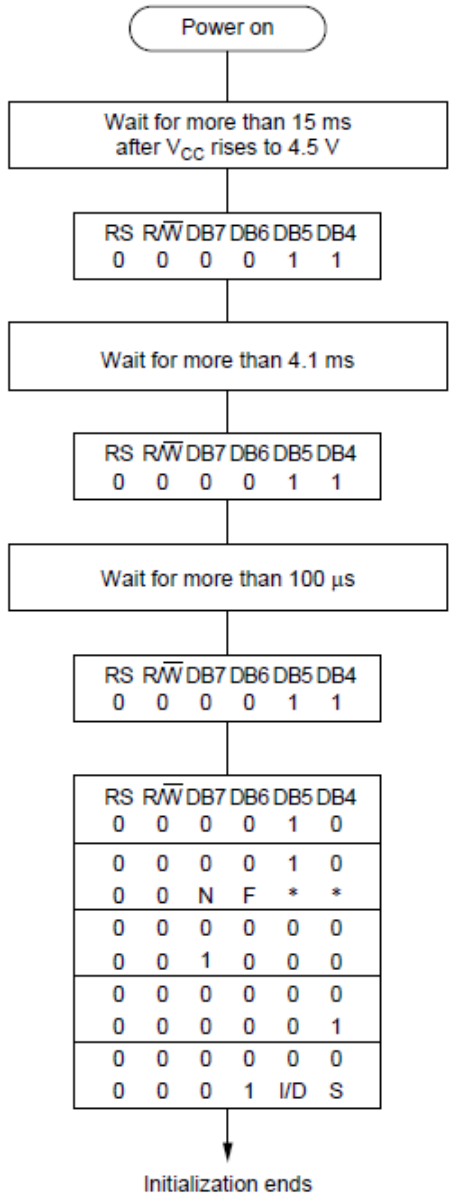

Figure 6: 4-bit Initialization

Note: * Indicates do not care condition.

Specifications provided.

Display

If your display is powered successfully, the text or cursor may be evident. Ensure the correct power is applied and the expected DDRAM addresses are shown by moving the display to the home position.

Communication

When communication of either text or commands is interrupted, check all data and control pins for continuity. Ensure the display has been initialized correctly before sending information using the

appropriate initialization algorithm. For 4-bit mode ensure D4-D7 are used. Finally, slow down communication and refer to Timing Characteristics for proper control flow.

Test Mode

Test mode is initiated by connecting 2 and 3 pin of the 3pin connector CN2 before applying power. In the test mode, a checker pattern is displayed across all characters of the screen. Please note that CN2 may be removed in the future.

Precautions

- Operation outside absolute maximum ratings may cause permanent damage.
- Ensure Anti-Static handling procedures are followed. Store in an anti-static container within a clean environment.
- Do not make extra holes on the display, modify its shape, or change the components. Do not drop, bend, twist, or disassemble the display.
- Physical shock greater than 100G, thermal shock in excess of 10°C/minute, or a direct hit to the glass display surface may crack the glass.
- Do not PUSH the display strongly. At mounting to the system frame, slight gap between display glass face and front panel is necessary to avoid a contact failure of lead pins of display. Twist or warp mounting will make a glass CRACK around the lead pin of display.
- Neither data nor power connectors should be connected or disconnected while power is applied. Removal of primary power with logic signals applied may damage input circuitry.
- Power must be regulated completely since all control logic depends on this line. Do not apply slow-start power. Provide sufficient power to supply inrush current at startup.
- Data cable length between module and host system is recommended within 300 mm to be free from a miss-operation caused by noise.
- Running in test mode for 2 hours may help the stability of the brightness of them VFD when power has not applied more than 2 months.
- Displaying a fixed (static) message longer than 5 hours in a day may cause the phosphor to burn-out. An automatic shut down in programming, scrolling message, or test mode operation during idling of the host is recommended.

Ordering

Part Numbering Scheme

Table 11: Parallel Part Numbering Scheme

MOP	-	A	V	20	4	A	-	B	N	N	N	-	0	1	J	-	3	I	N
1		2	3	4	5	6		7	8	9	10		11	12	13		14	15	16

Options

Table 12: Parallel Part Options

#	Designator	Options
1	Product Line	MOP: Matrix Orbital Parallel Display
2	Display Type	A: Alphanumeric
3	Screen Type	V: Vacuum Florescent Display
4	Display Columns	16: Sixteen Character Columns 20: Twenty Character Columns
5	Display Rows	2: Two Character Rows 4: Four Character Rows
6	Display Form Factor	A: A Form Factor C: C Form Factor
7	IC Package	B: Chip on Board
8	LCD Glass Type	N: Not Applicable
9	Polarizer Style	N: Not Applicable
10	Backlight Colour	N: Not Applicable
11	Viewing Angle	0: Not Applicable
12	Controller	1: HD44870 Compatible
13	Character Set	J: Japanese
14	Input Voltage	3: 5.0V
15	Temperature Range	I: Industrial
16	Negative Voltage Generation	N: None Provided

Contact

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