Application Note 137

32-Bit Non-PCI Interface for Embedded System Design with Ethernet Solution

KSZ8842-32MQL/MVL

General Description

Embedded system design with Ethernet connectivity to a network application is growing very fast and has created tremendous opportunities in consumer products such as Analog Telephone Adapters, Voice over IP, IP Video Phones, Set Top Boxes, IPTVs, Digital Video Recorders and Digital Media Adapters. Micrel provides a broad selection of Ethernet connectivity solutions with switch features for embedded 8-, 16- or 32-bit applications in consumer electronics, industrial and enterprise hardware design. The typical throughput requirement on Non-PCI host interfaces for each application is as shown below:

- VoIP or ATA – 256 Kbps (bi-directional)
- Industrial Control – 3 Mbps (bi-directional)
- IP Video Phone – 3.5 Mbps (bi-directional)
- Digital Video Recorder – 6 Mbps (down stream)
- IPTV (Standard Definition) – 4~8 Mbps (down stream)
- STB or HDTV (High Definition) – 20 Mbps (down stream)

This application note shows how to connect the KSZ8842-32MQL/MVL to various 32-bit microprocessors, microcontrollers or FPGAs.

32-Bit Non-PCI Bus Interface with KSZ8842-32MQL/MVL

The KSZ8842-32MQL/MVL is 2-Port Ethernet Switch with non-PCI interface. The host port is designed for 32-bit bus interface. This application note provides a basic overview of system level signal connections based upon 32-bit bus interfaces to different embedded CPU, such as Freescale (I.MX21/31), Renesas (SR7751) and STMicroelectronics (STx7100).

The KSZ8842-32MQL/MVL supports two transfer modes in the BIU (Bus Interface Unit):

- Asynchronous mode
- Synchronous mode

Both asynchronous and synchronous signals are independent of each other as long as they are not active simultaneously. For the KSZ8842-32MQL/MVL device, synchronous burst transfer and asynchronous transfer can be mixed or interleaved but cannot be overlapped due to sharing of common signals when VLBUSN pin is pulled up to High.

In order to ‘handshake’ with the different bus interfaces (ISA-like or VLBus-like), the following subsections will describe all bus interface signal connections using these two transfer modes. This will assist system design engineers to connect the KSZ8842-32MQL/MVL device to a microprocessor, microcontroller or FPGA of their choice.

32-Bit Asynchronous Bus Interface Mode

The industry standard ISA bus is an example of a typical asynchronous bus. In asynchronous bus interface mode, the host bus read and write operations in the KSZ8842-32MQL/MVL are controlled by the edges of RDN and WRN. ARDY is used to notify the CPU that it should extend the read or write access cycle. All signals, as shown in Table 1 are used for asynchronous bus interfaces with embedded microprocessor host such as the I.MX21, I.MX31 or STx7100. Hardware signal connections SR7751R for example are shown in Figures 1 (without using DATACSN) and 2 (using DATACSN). The format and map for external EEPROM are shown in Table 2.

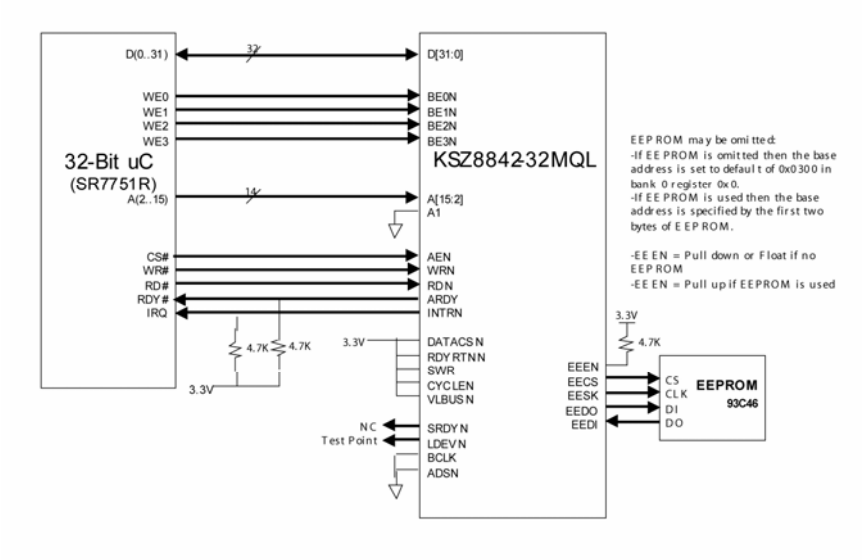

Figure 1. 32-Bit Asynchronous Bus Interface to SR7751R Example

I.MX21 Host Signals	STx7100 Host Signals	KSZ8842M Signals	Type	Asynchronous	
				ADSN = 0 (ISA-like)	Using DATACSN
A[15:1]	EMI_Addr[15:1]	A[15:1]	I	Address bus	N/A (leave open)
D[31:0]	EMI_Data[15:0]	D[31:0]	I/O	Data bus (8-, 16- or 32-bit)	Data (32-bit only)
/CS1	EMI_notCSC	AEN	I	Address Enable (active low)	N/A (leave open)
/EB[3:0]	EMI_BE[1:0]	BE3N,BE2N BE1N,BE0N	I	Byte Enable (active low)	N/A (leave open)
		ADSN	I	Always enabled Address Strobe (Pull down with 4.7K)	Pull down with 4.7K
		LDEVN	O	Local Device (asserted low when right address decoded)	N/A (leave open)
/CSx	/CSx	DATACSN	I	Not used (Tied high)	Data Chip Select is used for direct access QMU data register. When the DATACSN is asserted, it only allows access to the Data Register in 32-bit and BE[3:0]N are ignored
USBG_SCL (GPIO)	EMI_IRQ0	INTRN	O	Interrupt (asserted low when interrupt status bit set)	Interrupt (asserted low when interrupt status bit set)
/OE	EMI_notOE	RDN	I	Asynchronous Read (active low)	Asynchronous Read (active low)
/RW	EMI_RDnotWR	WRN	I	Asynchronous Write (active low)	Asynchronous Write (active low)
/DTACK	EMI_WAIT	ARDY	O	Asynchronous Ready (active high)	Asynchronous Ready (active high)
Unused Pins (only used for Synchronous mode)					
		VLBUSN	I	Pull up with 4.7K	Pull up with 4.7K
		CYCLEN	I	Pull up with 4.7K	Pull up with 4.7K
		SWR	I	Pull up with 4.7K	Pull up with 4.7K
		RDYRTNN	I	Pull up with 4.7K	Pull up with 4.7K
		BCLK	I	Pull down with 4.7K	Pull down with 4.7K
		SRDYN	O	Leave open	Leave open

Note: External Memory Interface (EMI) in STx7100 is 16 bit interface to KSZ8842-16MQL/MVL device only.

Table 1. KSZ8842-32MQL/MVL Bus Interface Signals for 32-Bit Asynchronous Mode.

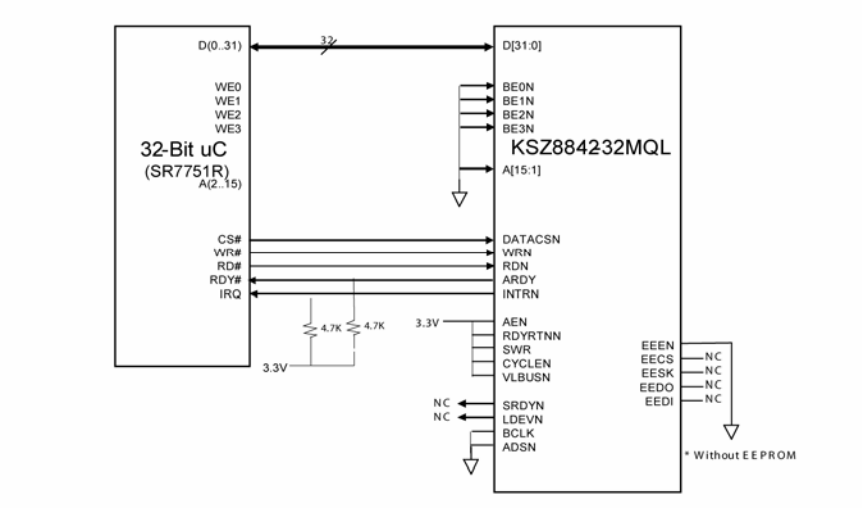

Figure 2. 32-Bit Asynchronous Bus Connections Using DATACSN

EEPROM Word Location	Bit Position [15:8]	Bit Position [7:0]	KSZ8842M Register Location
0x0	Base Address	Base Address	Bank 0 Register 0x0
0x1	MAC Address Byte 2	MAC Address Byte 1	Bank 2 Register 0x0
0x2	MAC Address Byte 4	MAC Address Byte 3	Bank 2 Register 0x2
0x3	MAC Address Byte 6	MAC Address Byte 5	Bank 2 Register 0x4
0x4	Reserved		NA
0x5	Reserved		NA
0x6	Reserved	Bit[1] = Clock_Rate (0: 125 MHz, 1: 25 MHz)	Bank 3 Register 0x0 (Default is 0x0 to select 125 MHz)
0x7 – 0x3F	Not used for KSZ8842M (available for user to define)		NA

Table 2. External EEPROM Map and Format.

32-Bit Synchronous Bus Interface Mode

The synchronous mode supports two different data transfer modes, as shown in Table 3:

1. Single data mode operation occurs when the VLBUSN pin is pulled low. This is the synchronous VL Bus type mode and supports only single-data transfer. The CYCLEN and BCLK are used to indicate either read or write commands to the KSZ8842-32MQL, completion of the read or write cycle can be determined by the SRDYN output signal from KSZ8842-32MQL. SRDYN is controlled by BCLK and is synchronous to the bus. All registers can be accessed using byte, word or double word instructions.
2. Burst data mode operation occurs when the VLBUSN pin is pulled high. This mode directly supports 32-bit access to the data path by using the DATACSN input. Whenever DATACSN is asserted, the address decoder is then disabled and a 32-bit transfer to Data Register is assumed (BE3N – BE0N are ignored).

KSZ8842M Signals	Type	Synchronous	
		Burst Data Mode Operation as shown in Figure 3 (Burst length is set 1, 4, 8 or 16 in BBLR register)	**Single Data Mode Operation as shown in Figure 4 (VLBUSN = 0, VLbus-like)**
A[15:1]	I	Don't care (leave open)	Address bus is used to select bank and register, it is latched by ADSN rising edge
D[31:0]	I/O	Data (32-bit only)	Data bus valid either 8-, 16- or 32-bit according to byte enable control signals BE3N~BE0N
AEN	I	Don't care (leave open)	Address Enable (active low) qualifies valid address bus, this signal is latched by ADSN rising edge
BE3N,BE2N BE1N,BE0N	I	Don't care (leave open)	Byte Enable (active low) for read or write valid data bus, these signals are latched by ADSN rising edge
ADSN	I	Don't care (leave open)	Address Strobe is used to latch A[15:1], AEN and BE3N~BE0N on rising edge
LDEVN	O	Don't care (leave open)	Local Device is asserted low when valid decodes of A[15:1] and AEN = 0
DATACSN	I	Data Chip Select is used to select QMU data register. When the DATACSN is asserted, it only allows access to the Data Register in 32-bit and BE[3:0]N are ignored	Not used (Tied high)
INTRN	O	Interrupt is asserted low when interrupt status bit set	Interrupt is asserted low when interrupt status bit set
VLBUSN	I	Tied high for non-VLBus cycle (burst data transfer)	Tied low for VLBus cycle (single data transfer)
CYCLEN	I	This input stays high for read cycles and low for write cycles during burst data transfer (DATACSN = 0)	This input follows the addressing cycle to signal the command cycle. CYCLEN is created typically by using ADSN delayed by one LCLK and used to sample SWR when it is asserted
SWR	I	Synchronous Read or Write input. Write cycles when high and read cycles when low	Synchronous Read or Write input. It is sampled by the KSZ8842M on first rising edge clock during the CYCLEN is active. Write cycles when high and read cycles when low
RDYRTNN	I	CPU drives this pin low to indicate that the cycle is not completed and the next cycle needs to be delayed. A wait state will be inserted if RDYRTNN is asserted; the RDYRTNN is sampled on the falling edge of BCLK and will insert a wait state on each subsequent falling edge of BCLK when the RDYRTNN is held.	Ready Return is asserted by the CPU to indicate the end of Read or Write in VLBus-like cycle
BCLK	I	Bus Clock is used for synchronous data transfer. Maximum frequency is 50 MHz	Bus Clock is used for synchronous data transfer. Maximum frequency is 50 MHz
SRDYN	O	The KSZ8842M drives this pin low to indicate wait state	Synchronous Ready is used to inform the CPU that it has completed the data transfer and the CPU can terminate the current active bus cycle, CPU can assert RDYRTNN on the next BCLK cycle. The SRDYN is asserted low for one BCLK period.
Unused Pins (only used for Asynchronous mode)			
RDN	I	Pull up with 4.7K	Pull up with 4.7K
WRN	I	Pull up with 4.7K	Pull up with 4.7K
ARDY	O	Leave open	Leave open

Table 3: KSZ8842-32MQL/MVL Bus Interface Signals for 32-Bit Synchronous Mode

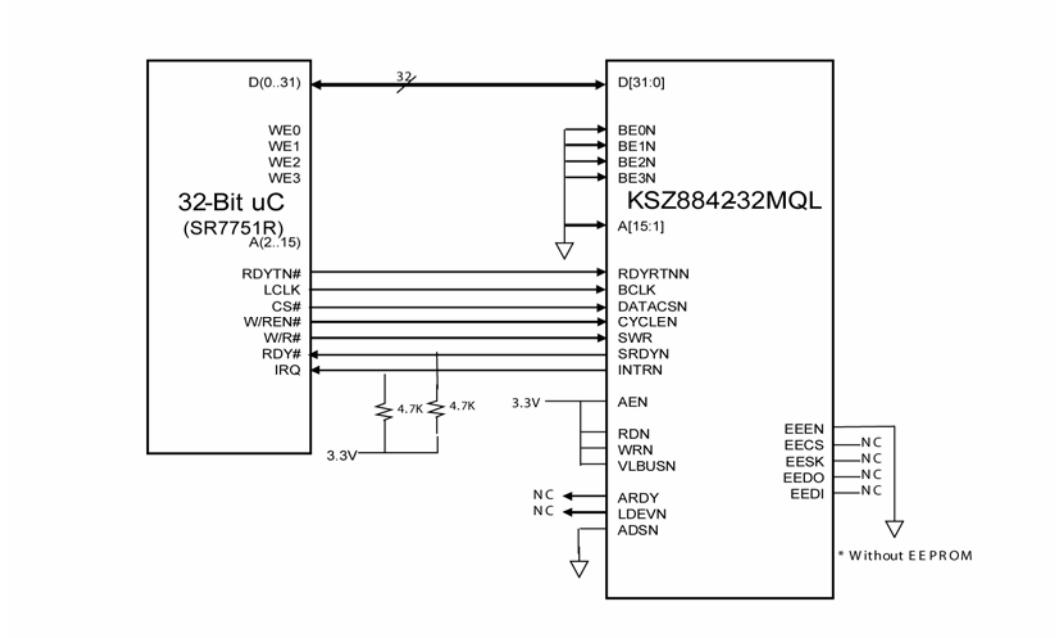

Figure 3. 32-Bit Synchronous Connections Using DATACSN

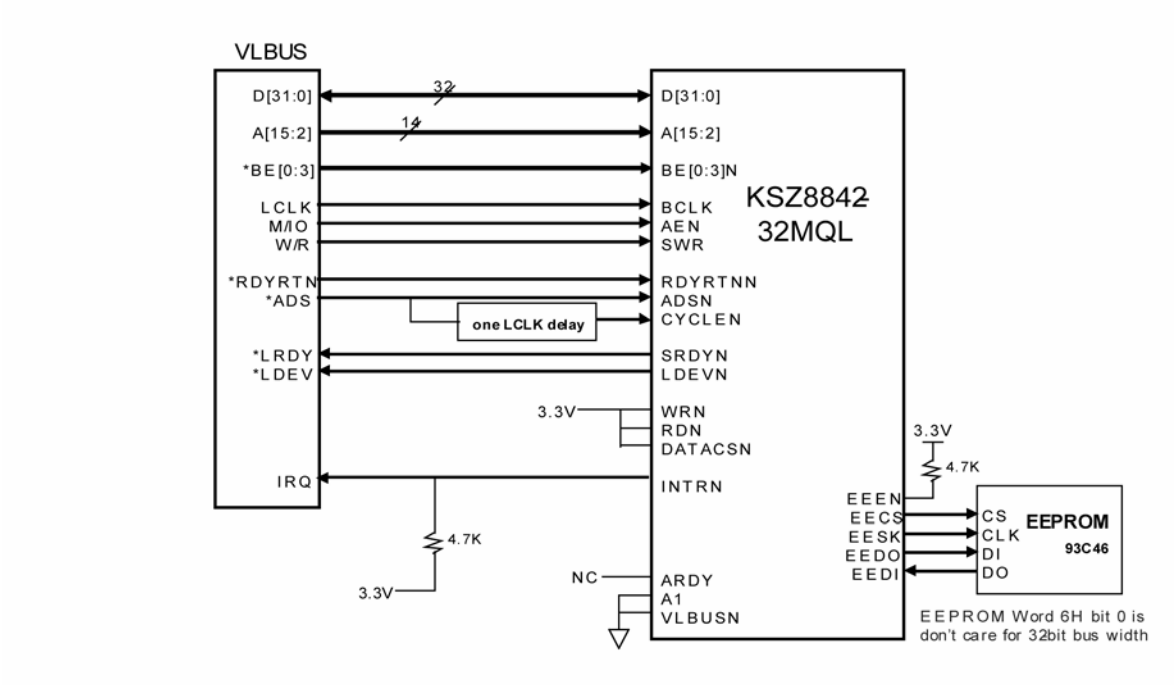

Figure 4. 32-Bit Synchronous VLBUS-like Bus Connections with EEPROM

Supporting Software

In order to meet the needs of diversified embedded system design, Micrel provides the following software drivers to support the following popular OS platforms:

- Windows 2000
- Windows XP
- Windows XP Embedded
- Windows CE 5.0
- Linux 2.4
- Linux 2.6
- VxWorks 5.5.1 (For Renesas SH7551R)

In addition, sample code for two popular 8-bit microcontrollers (8051 and Z80) is also provided. All software can be downloaded from: **www.micrel.com** in the Ethernet products web page. The software is contained in the software design package.

Conclusion

Micrel offers the largest family of embedded controllers in the industry as shown in Table 4 overleaf.

Micrel is therefore a one-stop-shop for:

– Single Port Controllers

– Dual Port Switches, Repeaters and Media Converters

– Footprint compatible devices for easy upgrade

– Copper and Fiber Interfaces

– Pb-Free (RoHS Compliant) products

– Industrial Temp Grade

– Software Driver source code to ease customer development

In addition, Micrel provides the flexibility of offering a single port KSZ8841-32MQL/MVL MAC/PHY plus generic bus interface device that is 100% footprint-compatible for single port applications. This provides engineers with the flexibility to design two products using a single print circuit board and software driver, thereby saving time, money and efforts in the development cycle.

All of the development collateral including the data sheet, schematics, gerber file, IBIS module and software driver can be downloaded from Micrel website. Evaluation boards and user's guide are also available.

Part Number	Bus Type & Width	10/100 Phy/Mac Port	Package	Temp. Range	EEPROM Interface	Wake-on-LAN/ Magic Package	Fiber Port Support	Auto MDIX	LinkMD™ Cable Diagnostics
KSZ8841-16 MQL/MVL/MVLI	Non-PCI 8/16-bit	One-port	128-pin PQFP/ LQFP	0°C to 70°C -40°C to 85°C (MVLI)	Yes	Yes	No	Yes	Yes
KSZ8841-32 MQL/MVL	Non-PCI 32-bit	One-port	128-pin PQFP/ LQFP	0°C to 70°C	Yes	Yes	No	Yes	Yes
KSZ8842-16 MQL/MVL/MVLI	Non-PCI 8/16-bit	Two-ports with Switch	128-pin PQFP/ LQFP	0°C to 70°C -40°C to 85°C (MVLI)	Yes	No	No	Yes	Yes
KSZ8842-32 MQL/MVL	Non-PCI 32-bit	Two-ports with Switch	128-pin PQFP/ LQFP	0°C to 70°C	Yes	No	No	Yes	Yes
KSZ8861-16 MQL	Non-PCI 8/16-bit	One-port	128-pin PQFP	0°C to 70°C	Yes	Yes	Yes 100B-FX or 100B-SX/10B-FL	Yes	Yes
KSZ8861-32 MQL	Non-PCI 32-bit	One-port	128-pin PQFP	0°C to 70°C	Yes	Yes	Yes 100B-FX or 100B-SX/10B-FL	Yes	Yes
KSZ8862-16 MQL	Non-PCI 8/16-bit	Two-ports with Switch	128-pin PQFP	0°C to 70°C	Yes	No	Yes 100B-FX or 100B-SX/10B-FL	Yes	Yes
KSZ8862-32 MQL	Non-PCI 32-bit	Two-ports with Switch	128-pin PQFP	0°C to 70°C	Yes	No	Yes 100B-FX or 100B-SX/10B-FL	Yes	Yes
KSZ8841 PMQL/PMQLI	PCI 32-bit	One-port	128-pin PQFP	0°C to 70°C -40°C to 85°C (PMQLI)	Yes	Yes	No	Yes	Yes
KSZ8842 PMQL/PMQLI	PCI 32-bit	Two-ports with Switch	128-pin PQFP	0°C to 70°C -40°C to 85°C (PMQLI)	Yes	No	No	Yes	Yes

Notes

1. All parts are operating at single power supply (3.3V) with 5V tolerant I/O buffers.
2. All parts support Flow Control.
3. All parts support Auto-negotiation except the fiber port.
4. All parts have 8K Bytes internal memory for RX / TX FIFO buffers
5. All packages are lead-free.

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Table 4. Product Selection Guide for Embedded Ethernet Family.

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