

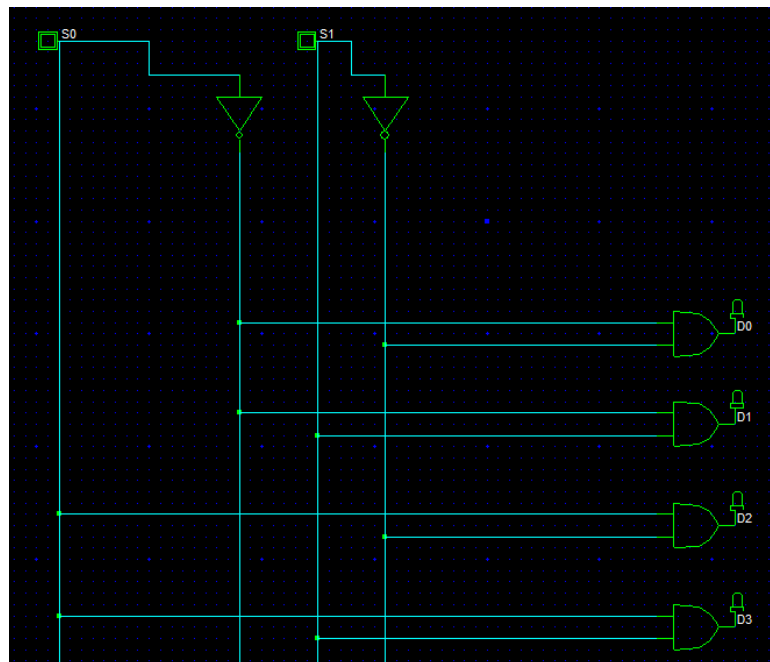
Digital Schematics

Decoder

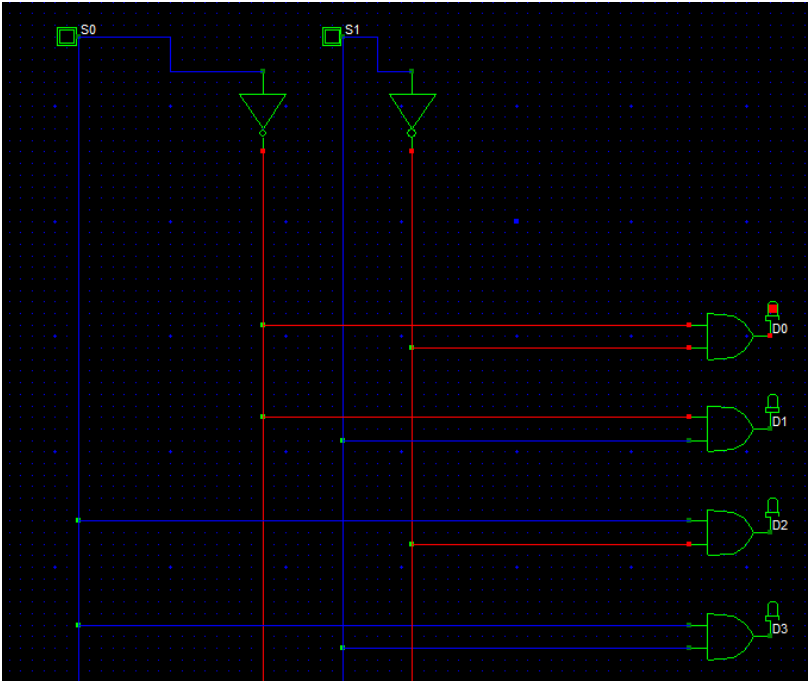
Decoder is a combinational circuit that converts binary information from n input lines to 2^n unique output lines.

We design a simple 2 to 4 Decoder

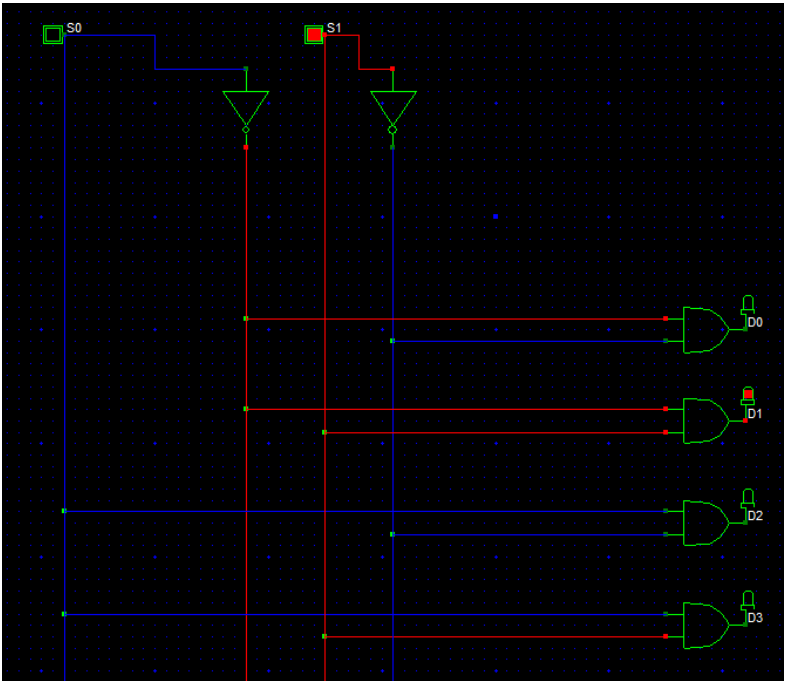
2×1 Decoder



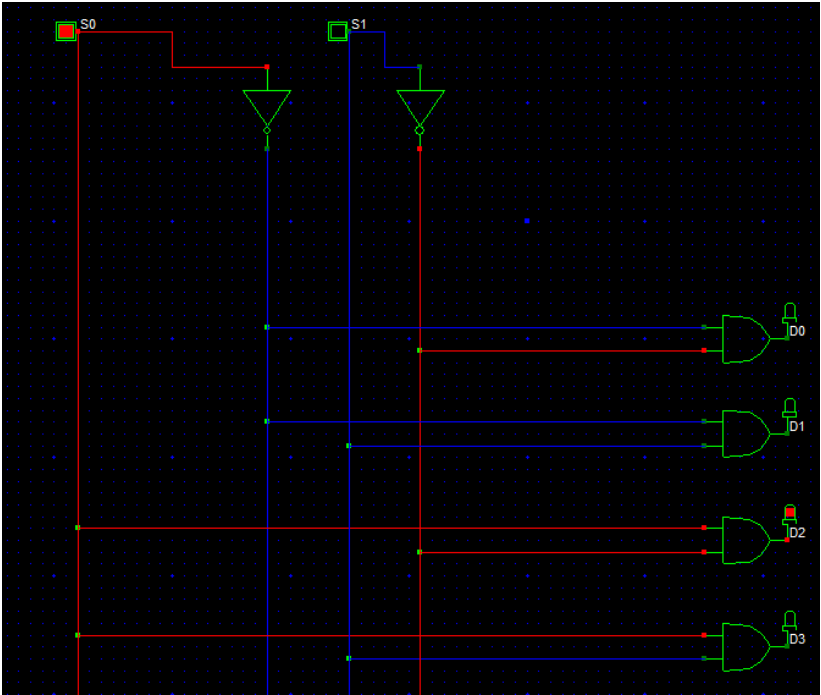
S_0	S_1
0	0



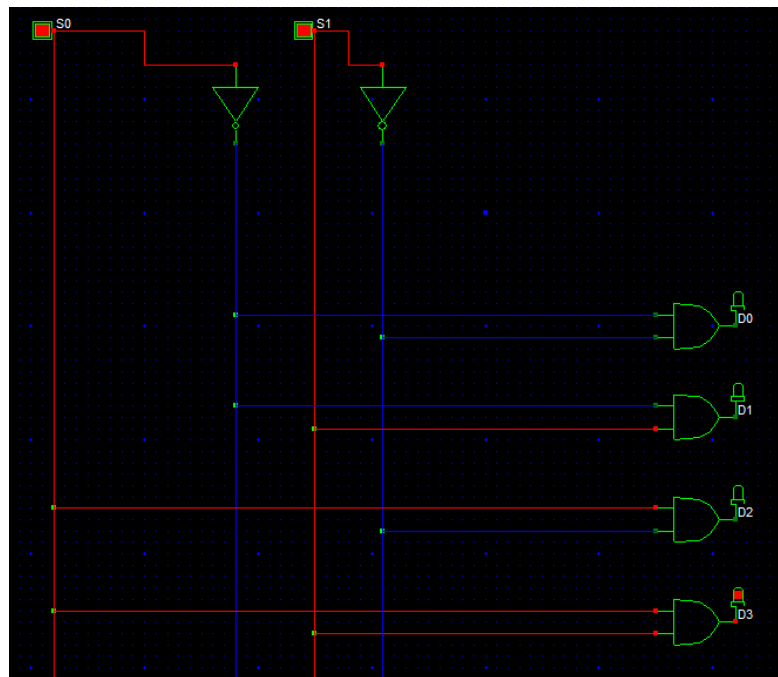
S_0	S_1
0	1



S_0	S_1
1	0



S_0	S_1
1	1

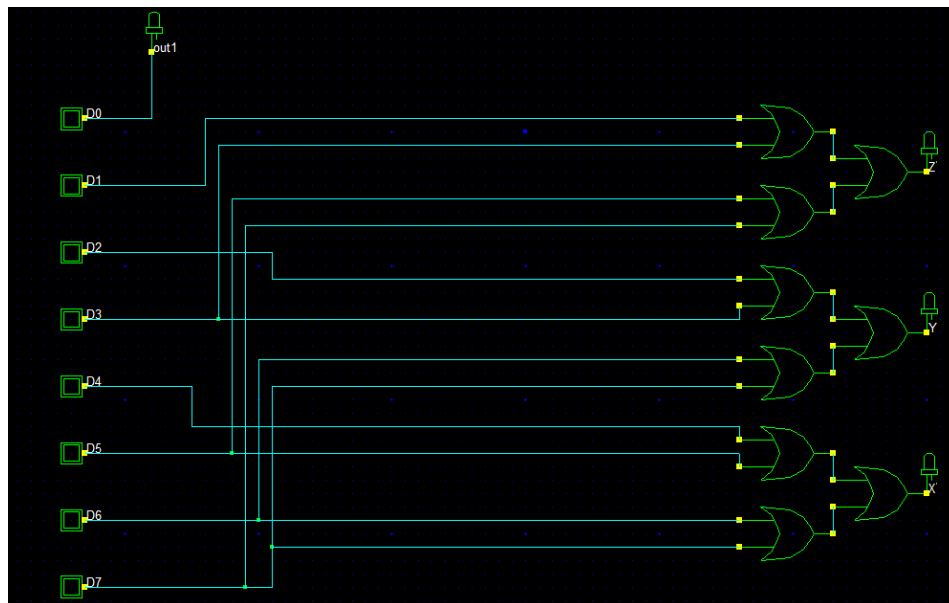


Encoder

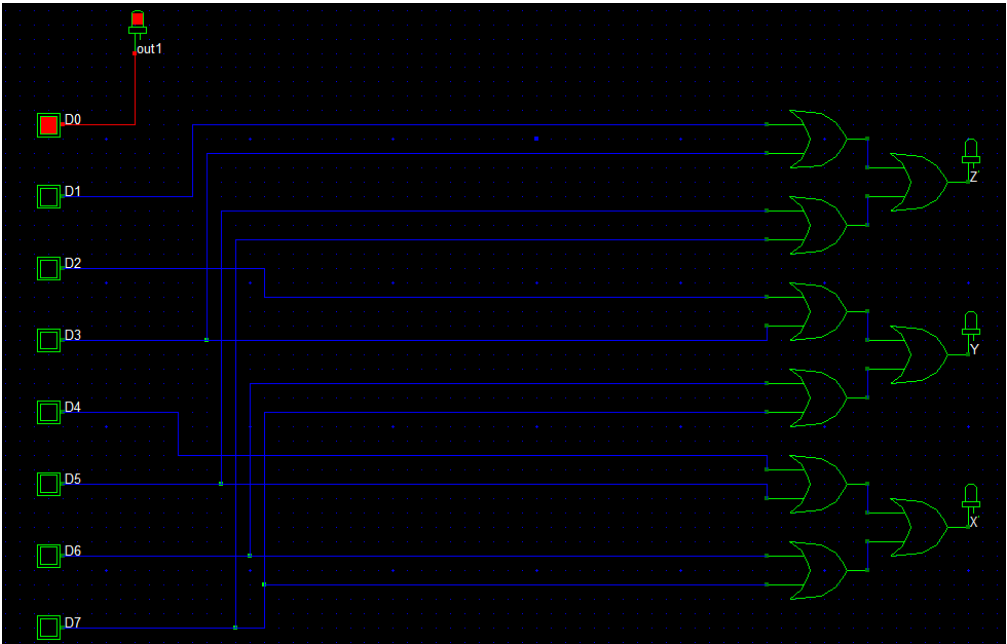
Digital function produces the reverse operation of decoder.

8 to 3 Encoder

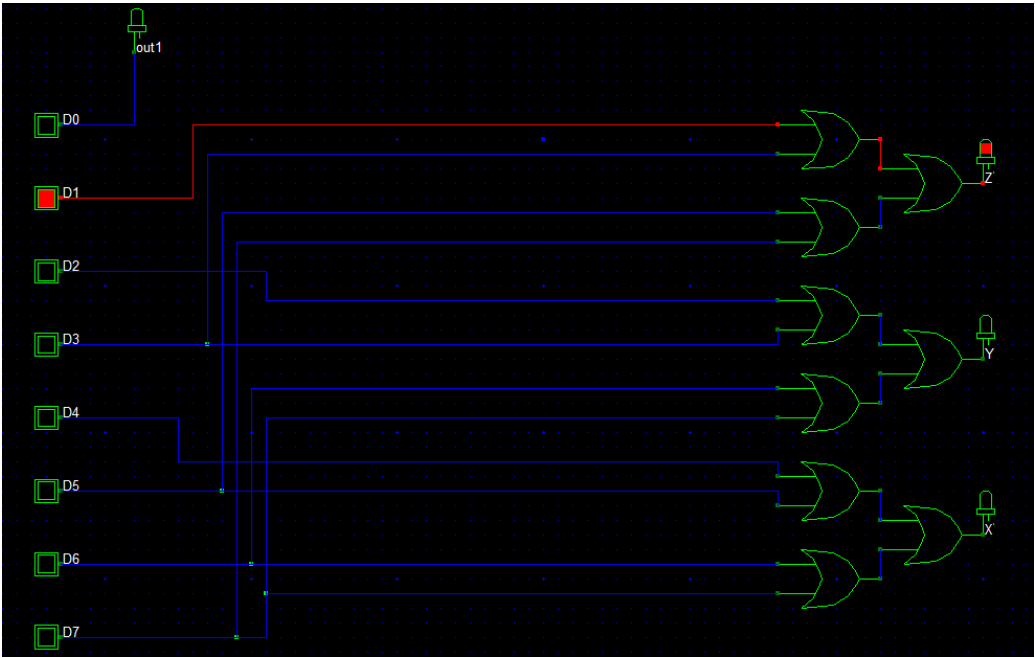
8×3 Encoder



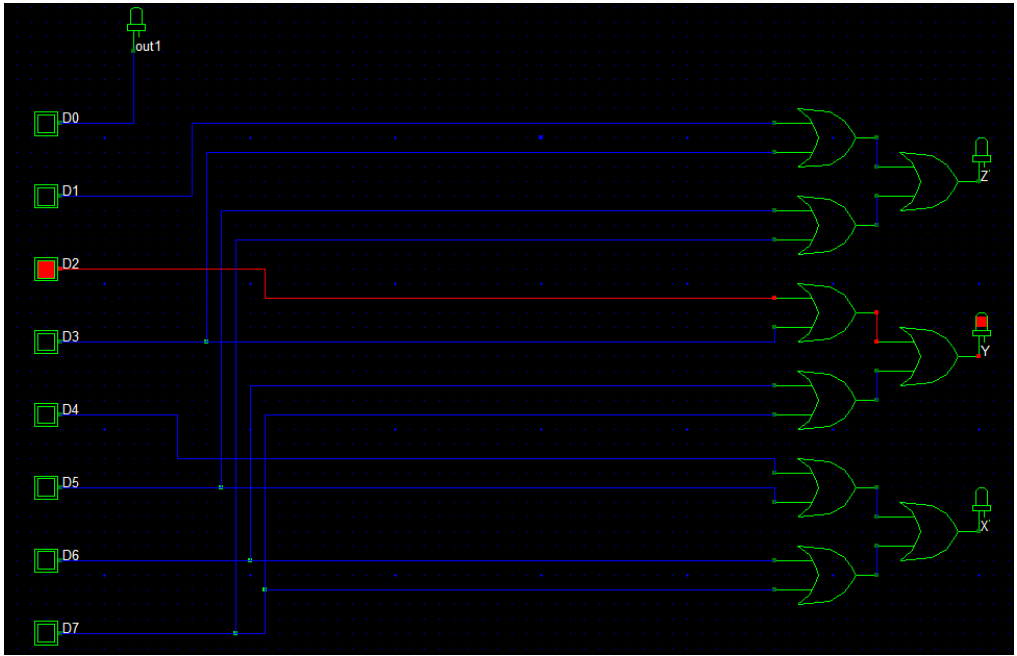
D₀	D₁	D₂	D₃	D₄	D₅	D₆	D₇
1	0	0	0	0	0	0	0



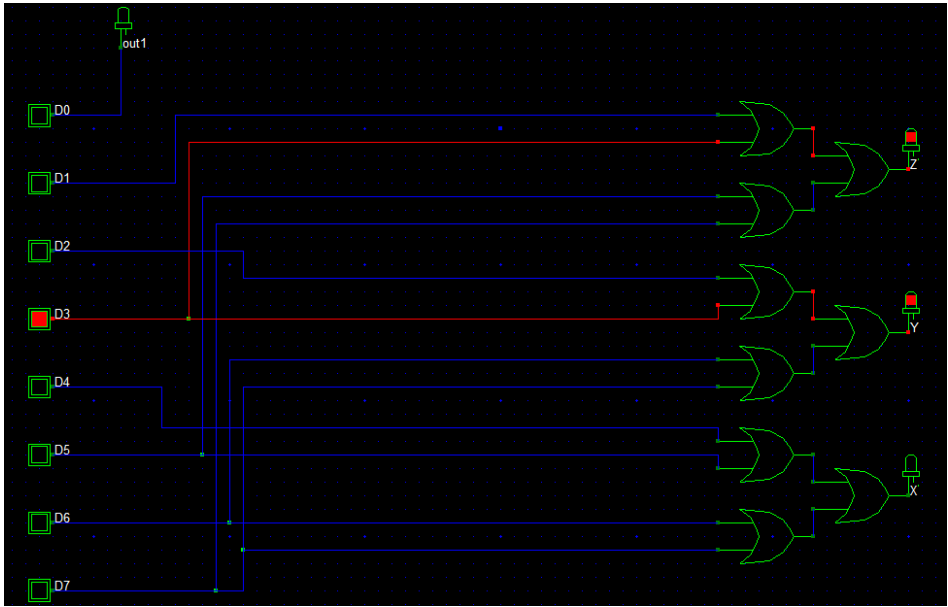
D₀	D₁	D₂	D₃	D₄	D₅	D₆	D₇
0	1	0	0	0	0	0	0



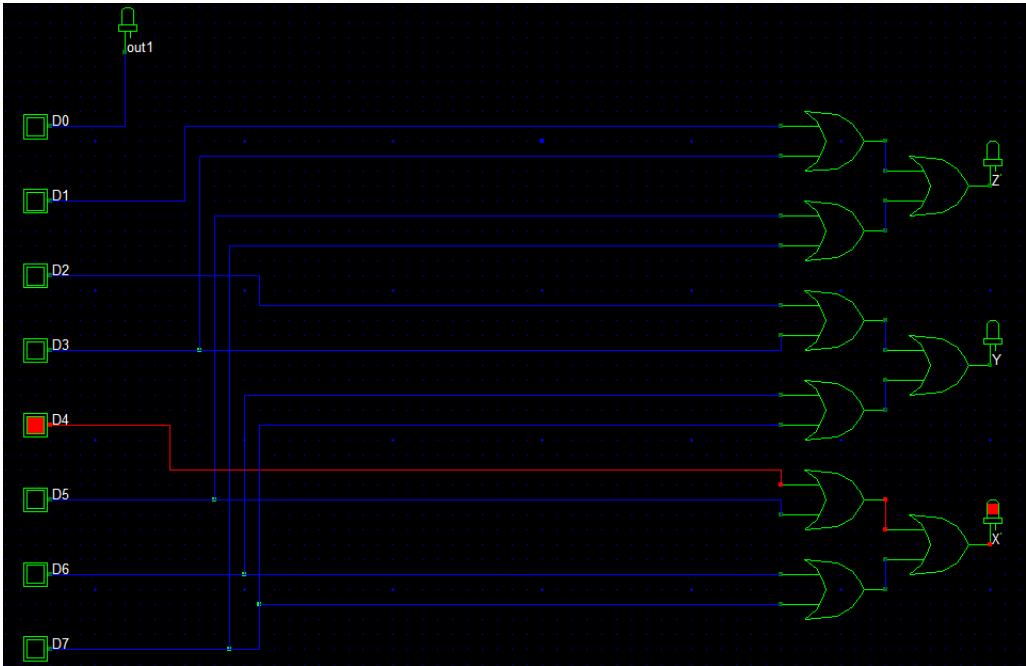
D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0	0	1	0	0	0	0	0



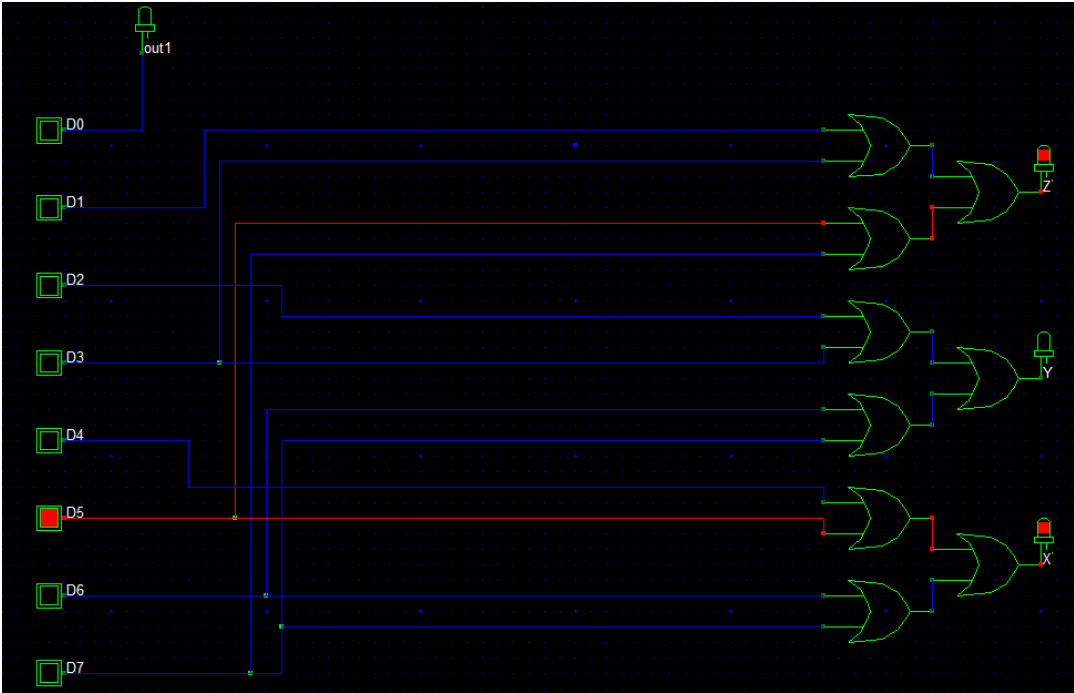
D₀	D₁	D₂	D₃	D₄	D₅	D₆	D₇
0	0	0	1	0	0	0	0



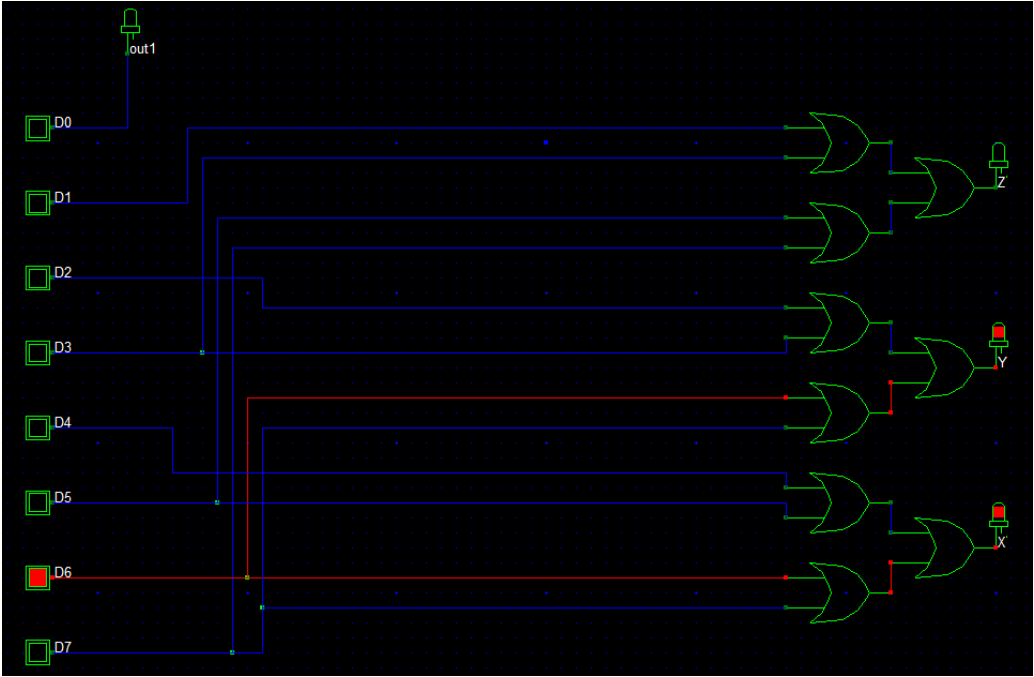
D₀	D₁	D₂	D₃	D₄	D₅	D₆	D₇
0	0	0	0	1	0	0	0



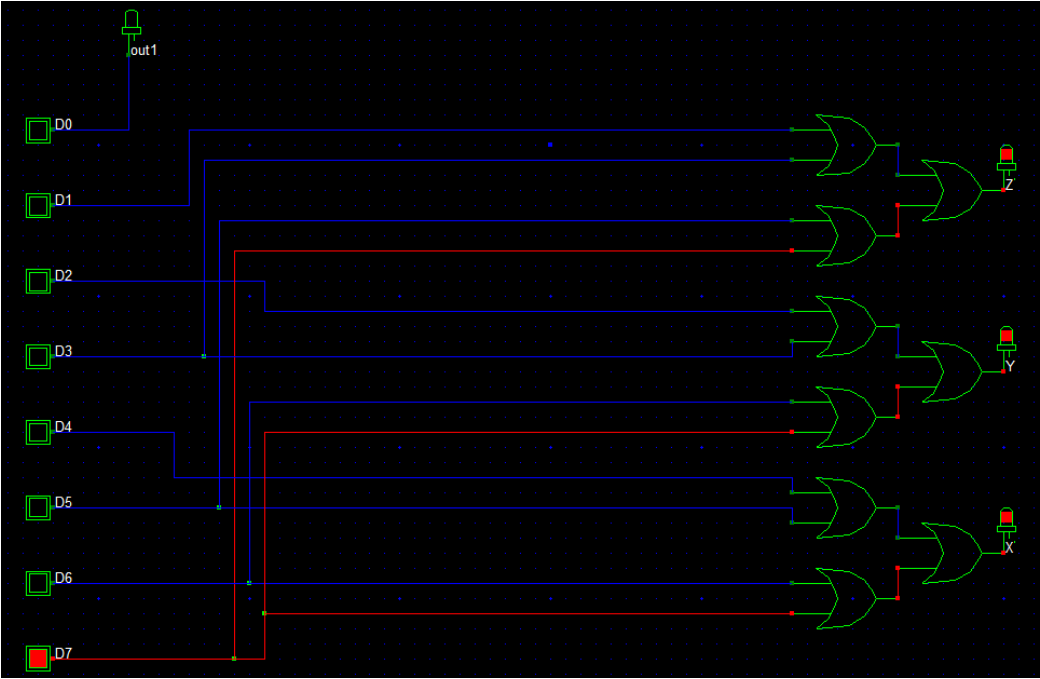
D₀	D₁	D₂	D₃	D₄	D₅	D₆	D₇
0	0	0	0	0	1	0	0



D₀	D₁	D₂	D₃	D₄	D₅	D₆	D₇
0	0	0	0	0	0	1	0

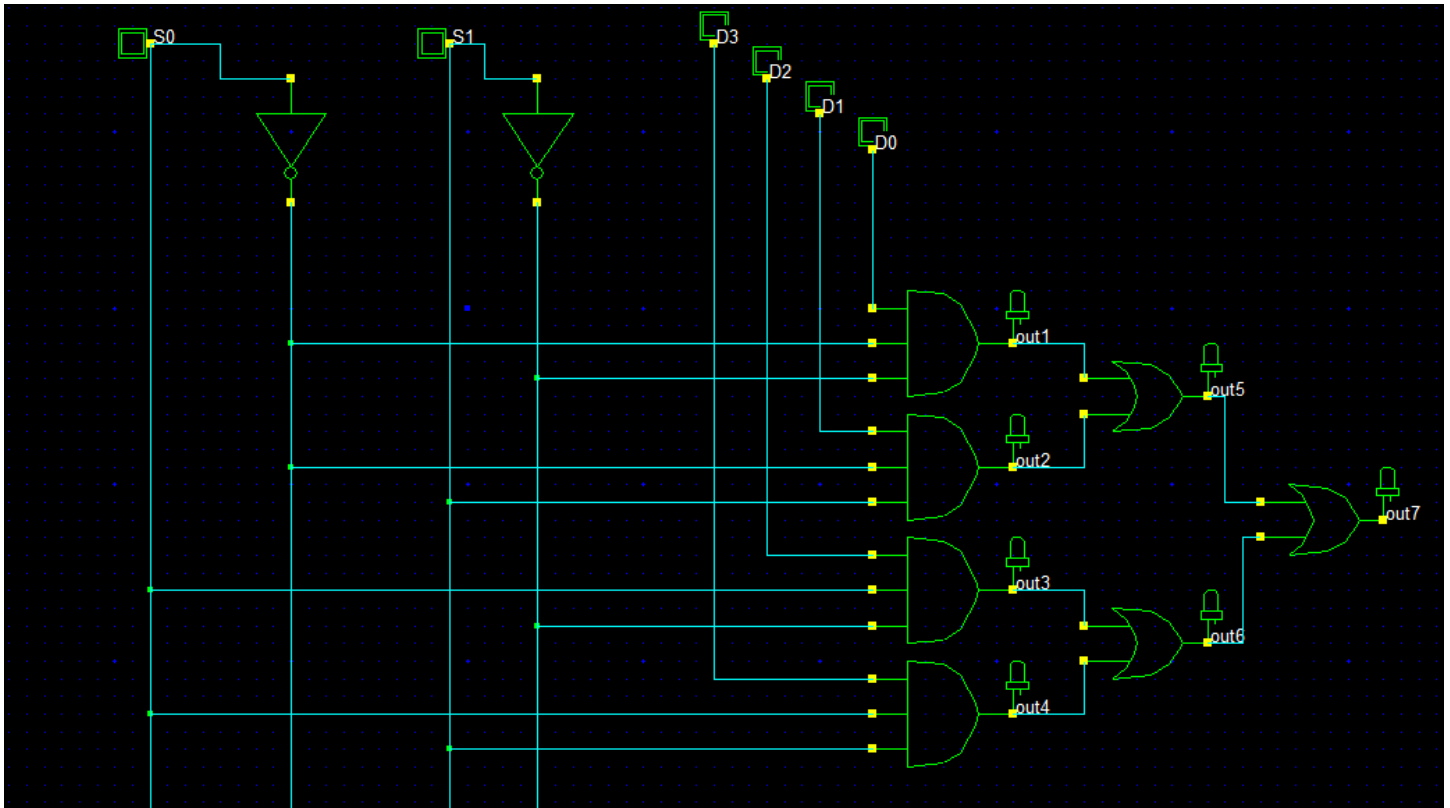


D₀	D₁	D₂	D₃	D₄	D₅	D₆	D₇
0	0	0	0	0	0	0	1

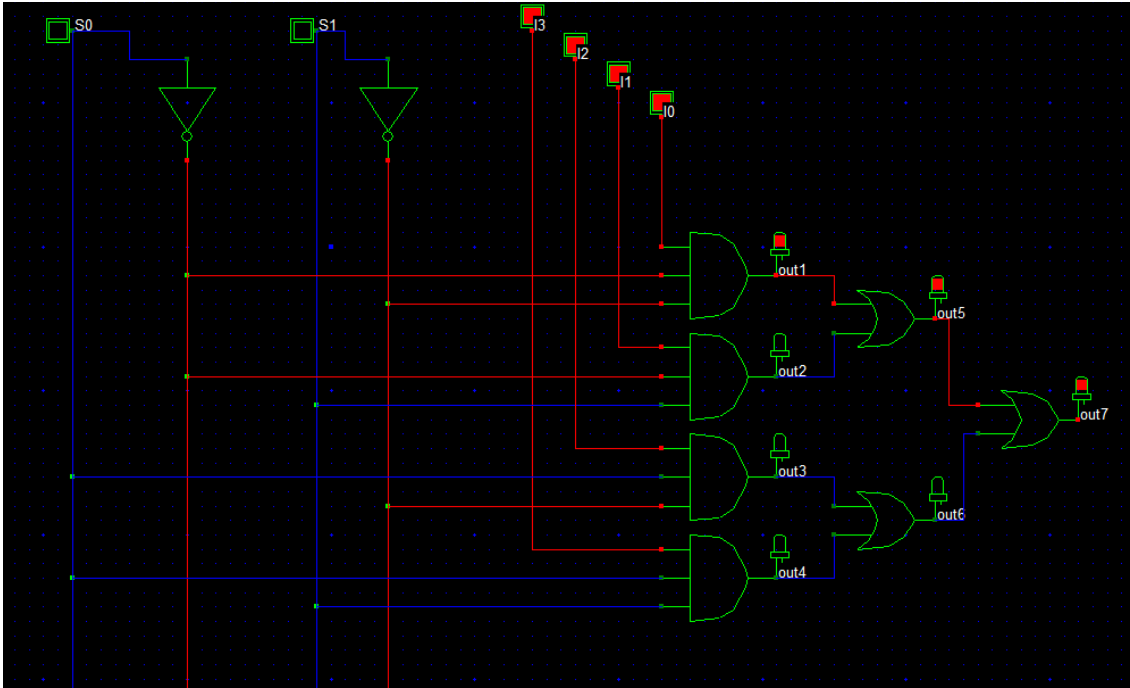


Mux

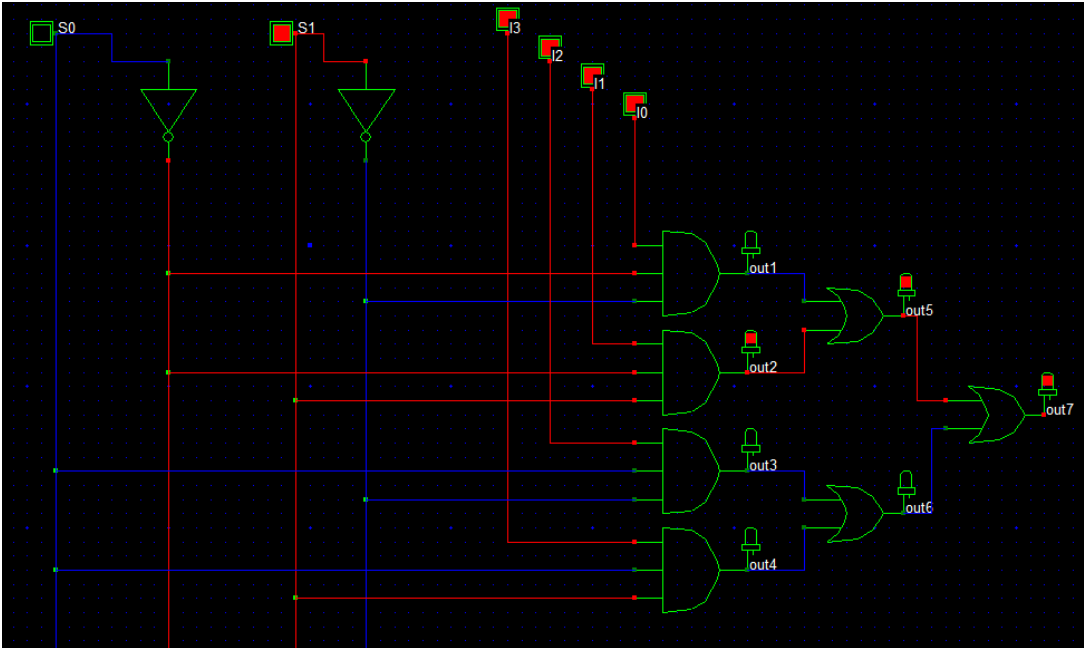
Multiple inputs \rightarrow Single Output



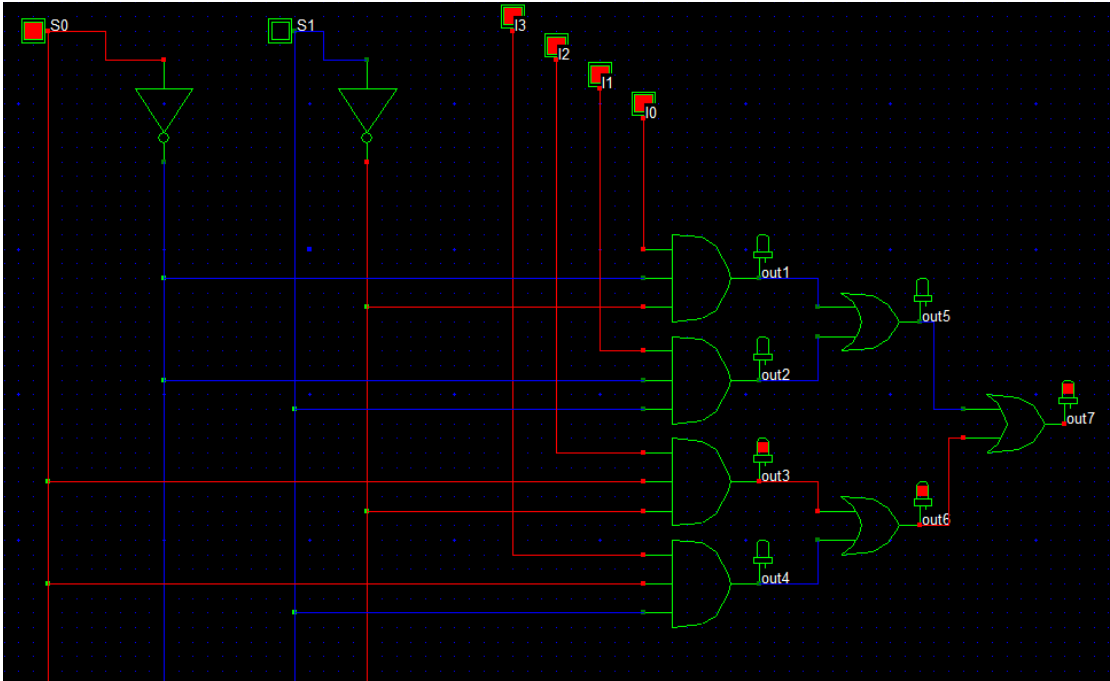
S_0	S_1	Output
0	0	D_0



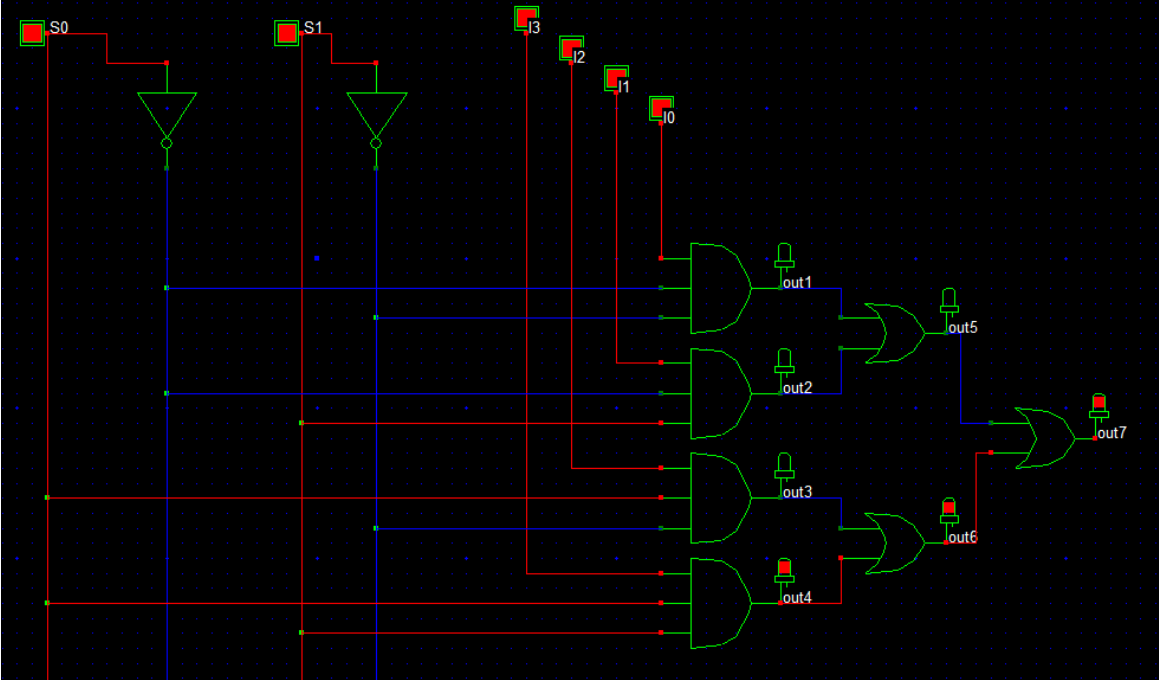
S_0	S_1	Output
0	1	D_1



S_0	S_1	Output
1	0	D_2



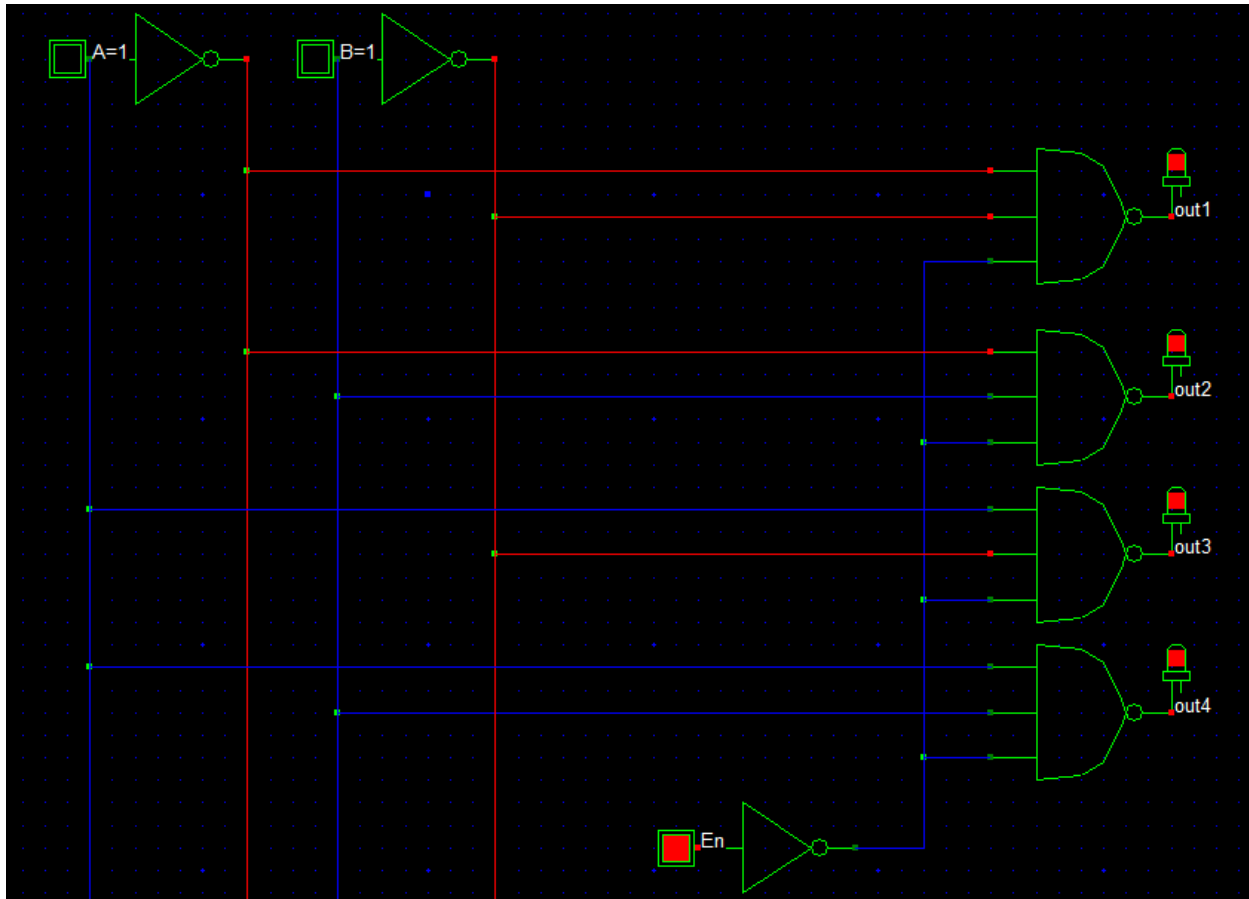
S_0	S_1	Output
1	1	D_3

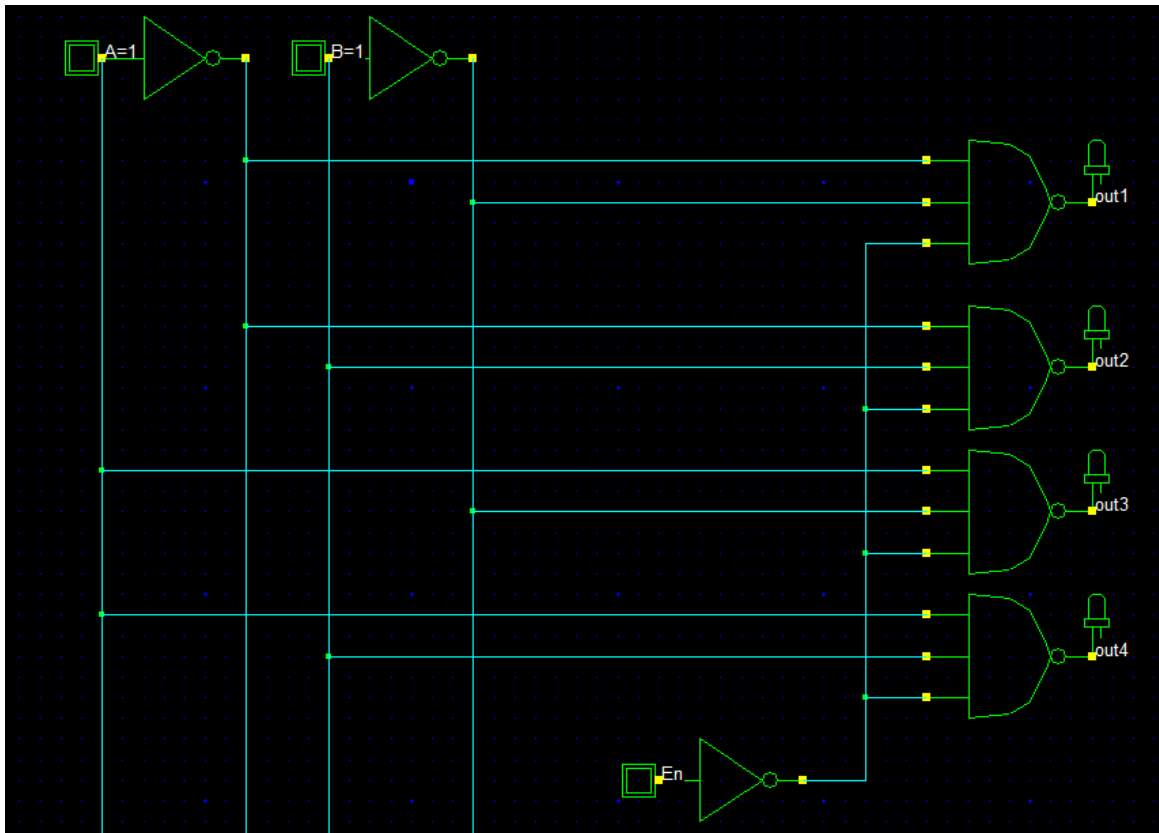


De-Mux

De-mux is a circuit that receives information on a single line and transmit this info to 2^n output lines

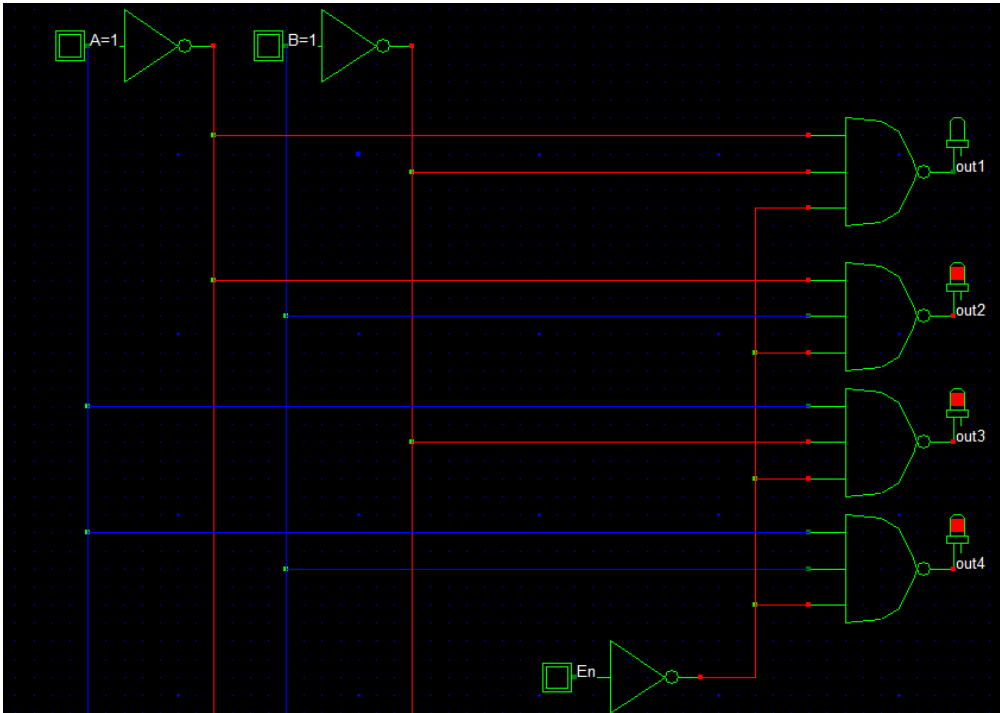
1×4 Demux

$$\mathbf{E}_n = \mathbf{0}$$

$$E_n = 0$$



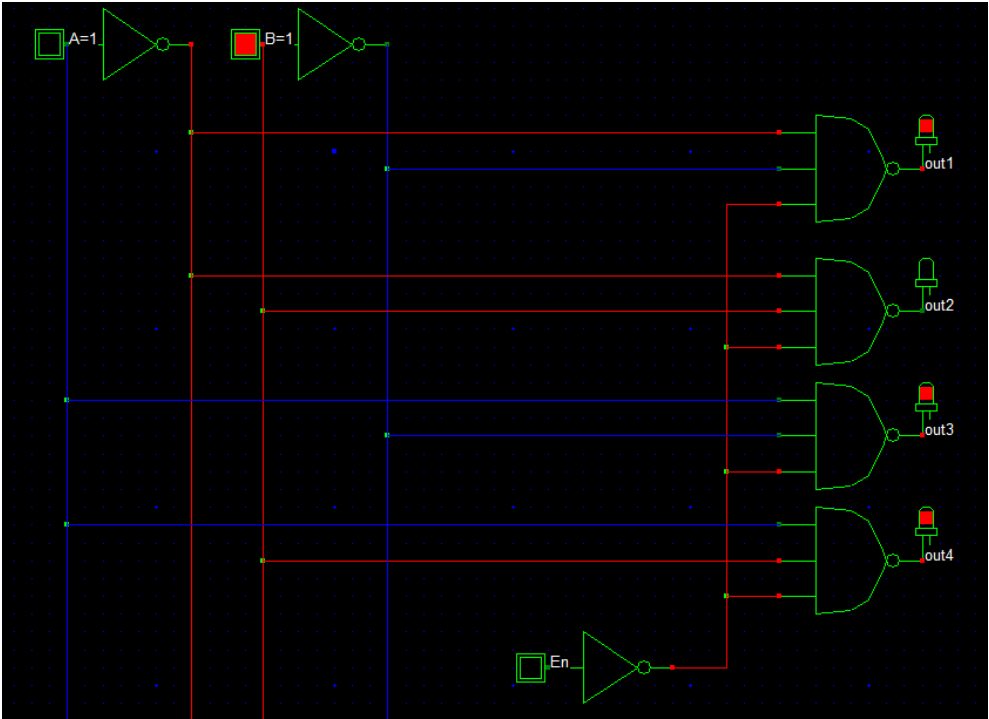
En	S ₀	S ₁	Output
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0	0	0	2,3,4
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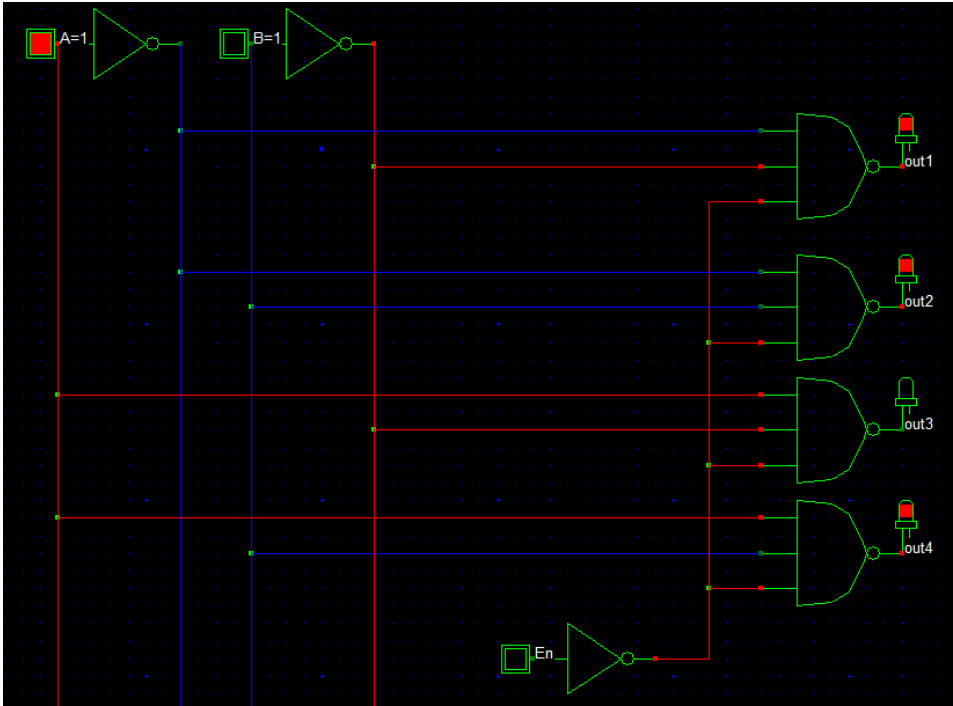
En	S ₀	S ₁	Output
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0	0	1	1,3,4
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En	S ₀	S ₁	Output
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0	1	0	1,2,4
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En	S ₀	S ₁	Output
0	1	1	1,2,3

