Journal of ELECTRONIC MATERIALS, Vol. 41, No. 6, 2012
DOI: 10.1007/s11664-012-1901-4

Top-Down Silicon Nanowire-Based Thermoelectric Generator: Design and Characterization

Y. LI,[1,2,3] K. BUDDHARAJU,[1] N. SINGH,[1] and S.J. LEE[3,4]

1.—Institute of Microelectronics, A*STAR (Agency for Science, Technology and Research), Singapore. 2.—Department of Electrical and Computer Engineering, NUS Graduate School for Integrative Sciences and Engineering, National University of Singapore, Singapore. 3.—SKKU Advanced Institute of Nano Technology, School of Information and Communication Engineering, Sungkyunkwan University, Suwon, Korea. 4.—e-mail: leesj@skku.edu.

A silicon nanowire (SiNW) array-based thermoelectric generator (TEG) was assembled and characterized. The SiNW array had pitch of 400 nm, and SiNW diameter and height of <100 nm and ~ 1 μm, respectively. The SiNW array was formed using a top-down approach: deep-ultraviolet (UV) lithography and dry reactive-ion etching. Specific groups of SiNWs were doped n- and p-type using ion implantation, and air gaps between the SiNWs were filled with silicon dioxide (SiO_2). The bottom and top electrodes were formed using a nickel silicidation process and aluminum metallization, respectively. Temperature difference across the TEG was generated with a heater and a commercial Peltier cooler. A maximum open-circuit voltage of 2.7 mV was measured for a temperature difference of 95 K across the whole experimental setup, corresponding to power output of 4.6 nW. For further improvement, we proposed the use of polyimide as a filler material to replace SiO_2. Polyimide, with a rated thermal conductivity value one order of magnitude lower than that of SiO_2, resulted in a larger measured thermal resistance when used as a filler material in a SiNW array. This advantage may be instrumental in future performance improvement of SiNW TEGs.

Key words: Silicon nanowires, thermoelectric, power generator

INTRODUCTION

It is a challenging task to scale down thermoelectric materials for use at the microlevel, for example, on microchips.[1] A major roadblock identified in the development of miniaturized thermoelectric technologies is the selection of a suitable material. Thermoelectric efficiency is dictated by the dimensionless figure of merit, defined as $ZT = S^2\sigma T/\kappa$ (S Seebeck coefficient, σ electrical conductivity, κ thermal conductivity, and T absolute temperature). Traditional thermoelectric materials are dominated by Bi_2Te_3 and Sb_2Te_3 with $ZT \approx 1$.[2] Unfortunately, despite having established technologies, traditional devices do not address the specific needs of thermal management in high-heat-flux applications such as optoelectronics, microprocessors, etc. Low-dimensional materials have been proposed as promising thermoelectric materials due to their enhanced performance as compared with bulk counterparts.[3–5] Recently, two-dimensional (2D) Bi_2Te_3 superlattice has even been demonstrated to be an efficient material for use in thermoelectric generators (TEGs).[6]

SiNWs have shown to be a much more efficient thermoelectric material than bulk silicon because of their lower thermal conductivity.[7–9] While the σ and S values of 50-nm-diameter SiNWs in Ref. 7 do not deviate much from those of bulk silicon, the measured κ values of 1.6 W/mK to 25 W/mK (depending on the surface roughness) are clearly lower than that of bulk silicon (150 W/mK), resulting in a best ZT value of 0.6 at room temperature. If these

(Received June 5, 2011; accepted January 2, 2012; published online February 10, 2012)

benefits are properly harnessed, SiNWs could be a promising candidate for use in applications such as microscale on-chip energy harvesting.

Nevertheless, fabricating a TEG using SiNWs is a great challenge due to their size and the process complexity at that scale. To date, discussion of SiNW TEGs has been restricted to fundamentals.[10,11] Although the bottom-up approach is widely used to synthesize SiNWs for research purposes,[7,9,12,13] the top-down approach is a much more feasible solution for fabrication of practical devices from a manufacturing perspective. In this work, we characterized a SiNW TEG fabricated using the top-down approach. With further analysis, we suggest that a marked improvement in thermal resistance can be obtained through integration of polyimide as a filler material, as opposed to our earlier choice of silicon dioxide (SiO_2).

EXPERIMENTAL PROCEDURES

Fabrication

A top-down approach was adopted in this work to define a SiNW array with minimal variations in diameter. Photoresist in the form of a nanodot array was first patterned by lithography on a silicon-on-insulator (SOI) wafer. Subsequent resist trimming through O_2 ashing reduced the size of the nanodots. Thereafter, dried reactive-ion etching (DRIE) was used to etch the silicon, with the nanodots acting as a hard mask. The SiNW array had pitch of 400 nm, and the SiNWs had length of $\sim$1.2 μm. Thermal self-limiting oxidation further reduced the wire diameter to 80 nm. Figure 1a–c show scanning electron microscopy (SEM) images of the SiNW array formation after etching, thermal oxidation, and removal of SiO_2 using diluted hydrofluoric acid (DHF) to reduce the average diameter of the SiNWs to $\sim$80 nm, respectively. Subsequently, specific groups of the SiNW array were doped n- and p-type as in a complete thermoelectric device.[14,15] The n/p thermocouples were then isolated through a silicon etching process and the bottom electrodes formed using a self-aligned nickel silicidation process. The air gap between the pillars was filled with SiO_2, which cushioned the SiNW array from any mechanical stress which might be induced during characterization. After etching away SiO_2 to reveal the SiNW tips as shown in Fig. 2, aluminum (Al) was deposited to form the top electrodes. To demonstrate the significance of the choice of filler material, we prepared another sample of SiNW array with polyimide integrated as the filler material. The polyimide used had a rated κ of 0.14 W/mK, one order of magnitude lower than that of SiO_2.[16] It should be noted that the additional sample prepared was not a working TEG but rather was used only for comparison of the thermal resistance with that of the SiO_2-filled SiNW sample.

Electrical and Thermal Characterization

I–V measurements of the SiNW TEG recorded device resistance of 400 Ω, including both the resistance of the SiNW as well as the electrical contact resistances present. For power generation characterization, we made use of an experimental setup which included a bottom heater and a heat

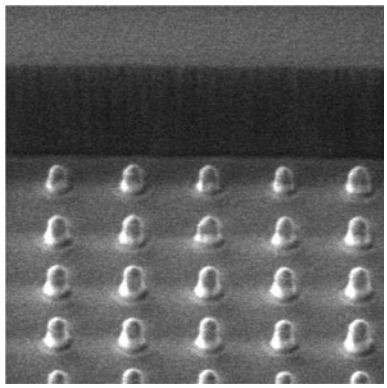

Fig. 2. SEM image of a SiNW array filled with SiO_2. The exposed SiNW tips after etching away the SiO_2 as shown were contacted with Al metal as the top electrode.

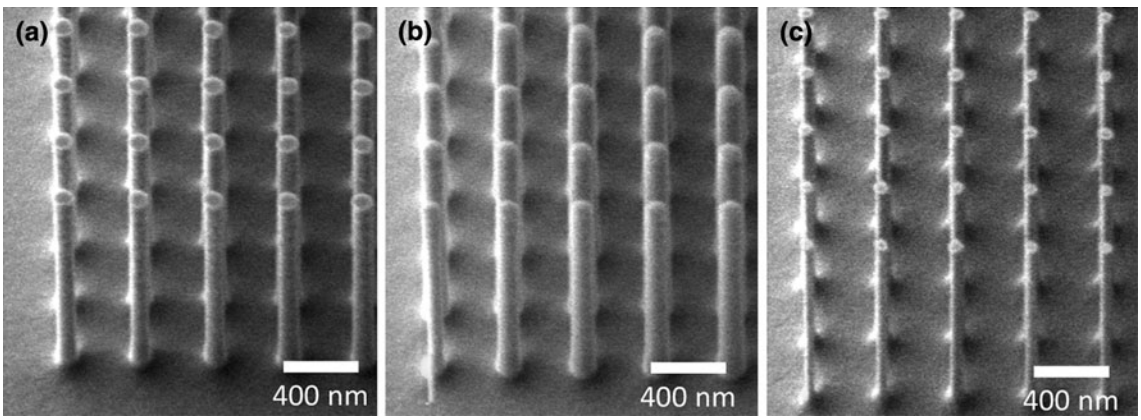

Fig. 1. SEM images of a SiNW array: (a) as etched, (b) after thermal oxidation to reduce the SiNW diameter, and (c) after removal of SiO_2 to confirm the reduction in diameter of the SiNWs.

sink at the top. Temperature sensors were integrated into the heater and a heat sink to record the temperature across the whole experimental setup accurately.[14] The TEG was wire-bonded and placed in between the heater and heat sink. A temperature difference (dT) was generated by powering the heater and cooling of the heat sink using a fan and a commercial Peltier cooler. In the experimental setup, the different layers, together with the size and κ (standard parameters) are as follows (from bottom): heater (brass, κ = 109 W/mK, 6 cm × 6 cm × 1 cm), thermal interface material (TIM)1 (κ = 0.7 W/mK, 5 mm × 5 mm × 50 μm), TEG on SOI, TIM2 (κ = 0.7 W/mK, 5 mm × 5 mm × 50 μm), and heat sink (Al, κ = 250 W/mK, 6 cm × 6 cm × 1 cm). The open-circuit voltage (V_{oc}) generated was measured with a Keithley 2400 multimeter while dT varied during testing. It should be noted that only the effective dT across the SiNW layer was involved in the V_{oc} generation. Figure 3 shows the results with both linear fit and polynomial fit across all data points. The deviation of the data points from a linear fit can be explained as follows: the V_{oc} generated is related to the Seebeck coefficient S as $V_{oc} = S \times \mathrm{d}T$. However, the Seebeck coefficient is an increasing function of the absolute temperature of the SiNW.[7] Hence, the data points for high dT (>70 K) in our measurement appear to deviate from a linear trend; this suggests the suitability of the TEG for use in high-temperature applications. Under a maximum applied dT of 95 K across the experimental setup, V_{oc} of 2.7 mV was measured. This corresponded to maximum power output of 4.6 nW when a load having the same resistance as the SiNW TEG was connected across it. It is worth pointing out that the generated V_{oc} is low considering the Seebeck coefficient of SiNWs of >200 μV/K.[7] However, this can be attributed to the ultrathin profile (~1 μm) of the SiNW layer and thermal parasitic losses such as due to the TIM present in the experimental setup.

Filler material was necessary in this work to cushion the SiNWs from external stress. SiO_2 was considered as a filler material because of its complementary metal–oxide–semiconductor (CMOS) compatibility. However, SiO_2 is not the best filler material considering its standard κ value of 1.4 W/mK. Theoretically, the lower the κ, the larger the thermal resistance ($R_{thermal}$) and hence the larger the dT that can be sustained across the SiNW layer. The $R_{thermal}$ of a layer is given by Eq. 1, and the effective $R_{thermal}$ of a SiNW layer with the inclusion of a filler material is given by Eq. 2.

$$R_{\mathrm{thermal}} = \frac{l}{\kappa A}, \tag{1}$$

$$\frac{1}{R_{\mathrm{effective}}} = \left(\frac{\kappa A}{l}\right)_{\mathrm{effective}} = \left(\frac{\kappa A}{l}\right)_{\mathrm{SiNW}} + \left(\frac{\kappa A}{l}\right)_{\mathrm{filling\,material}}. \tag{2}$$

Polymers, such as polyimide, clearly make a better candidate with a κ value one order of magnitude lower than that of SiO_2 (0.14 W/mK versus 1.4 W/mK).[16] The impact of the filler material was investigated by fabricating an identical SiNW array sample with polyimide replacing SiO_2. The $R_{thermal}$ contribution of the SiNW layer was measured in another experimental setup using a separately fabricated heating test chip. The test chip consisted of serpentine copper lines covering the surface uniformly, which can be heated up to specific known power. With the test chip, $R_{thermal}$ of the setup can be measured by plotting a dT versus power graph. In the plot, the gradient of the slope will reflect the $R_{thermal}$ of the experimental setup. The relationship of the heat transfer rate across a material is as shown in Eq. 3.

$$P = \kappa A \frac{\Delta T}{\mathrm{d}x}, \tag{3}$$

where P is the power supplied/heat transfer rate across the material, and A is the area of the material. In this experimental setup, the different layers, together with the size and κ (standard parameters) are as follows (from bottom): heater (silicon, κ = 150 W/mK, 1 cm × 1 cm × 700 μm), TIM1 (κ = 0.7 W/mK, 1 cm × 1 cm × 50 μm), sample, TIM2 (κ = 0.7 W/mK, 1 cm × 1 cm × 50 μm), and heat sink (Al, κ = 250 W/mK, 6 cm × 6 cm × 1 cm). The measurement was carried out in an indoor environment with the setup enclosed in an acrylic box to eliminate the possibility of moving air. Hence, negligible heat loss to the surroundings was assumed. A Keithley 2400 source meter was used to power the test chip while dT across the setup was monitored. Figure 4 shows the dT versus power relationship for the two different filler materials (SiO_2 versus polyimide). With all other layers in the setup remaining the same, the sample with polyimide as the filler material exhibited a larger $R_{thermal}$ as compared with that of SiO_2. Use of polyimide as a filler material lowered the effective κ of the SiNW layer. This preliminary analysis

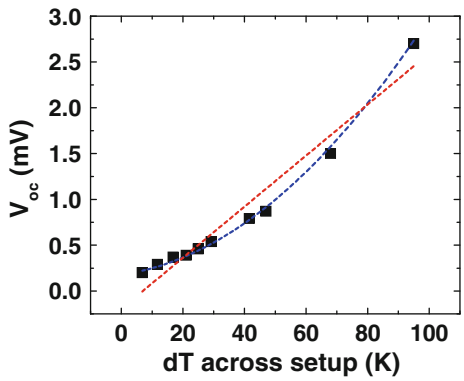

Fig. 3. Relationship between V_{oc} with varying dT across the setup. The red dotted line is a linear fit, while the blue dotted line is a polynomial fit of order 2 across all the data points (Color figure online).

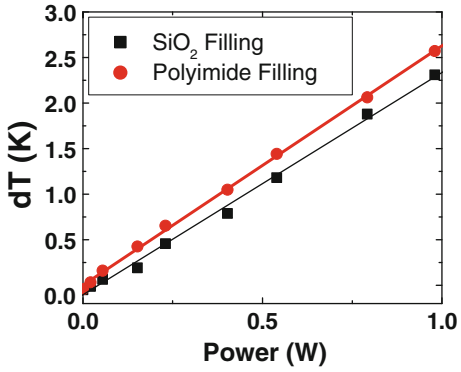

Fig. 4. dT versus power graph for different filler materials. The slope relates to the thermal resistance of the SiNW samples under test.

suggests that future work can consider the integration of polyimide, or materials with much lower κ value, to improve R_{thermal} and, hence, the performance of such SiNW TEGs.

CONCLUSIONS

We have presented a top-down integrated SiNW-based TEG technology together with its performance analysis up to large dT (95 K). The V_{oc} generated by the TEG increased in a polynomial fashion when dT was large. Further investigation of the SiNW layer's thermal resistance with a different filler material (polyimide) demonstrated the benefits of using a low-κ material in nanoscale thermoelectric power generation. Further design optimization and reduction of thermal parasitic losses of the SiNW TEG could greatly improve its performance and bring such devices to the forefront.

ACKNOWLEDGEMENTS

The authors would like to thank the staff at IME, Singapore, for assistance and discussion during paper writing and the anonymous reviewers for their efforts and suggestions that helped improve this paper.

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