

TOPICAL REVIEW

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Topical Review

Silicon-based nanostructures for integrated thermoelectric generators

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Abstract

Nanostructuring is a promising approach for enhancing thermoelectric properties of existing abundant and compatible materials such as silicon and silicon-based compounds. Recent works on different nanostructures have presented silicon-based materials as outstanding candidates for their implementation in thermoelectric generators. The compatibility of silicon with mainstream technologies, such as microelectronics and micro- and nano-fabrication, has attracted attention due to the integration of some of its nanostructures in micro-thermoelectric generators for energy harvesting applications. This topical review is focused on the most recent advances in fabrication, characterization and device integration of silicon-based thermoelectric nanomaterials, offering an outlook with an application-oriented focus. In particular, the use of doped silicon, silicon–germanium and silicides in the form of nanowires, thin films and superlattices as well as porous, nano-crystalline and nano-composite bulk is covered. Moreover, this paper provides future perspectives and research directions on the integration of silicon-based materials for energy applications in light of the recent findings reviewed.

Keywords: thermoelectricity, silicon, germanium, silicide, nanostructures, nanowires, thin film

(Some figures may appear in colour only in the online journal)

Abbreviations

BM	Ball milling	Ge	Germanium
L_B	Ballistic length	HMS	Higher manganese silicides
E_{gap}	Band gap energy	HP	Hot pressing
BiCMOS	Bipolar/CMOS	HM	Hydrothermal methods
k_B	Boltzmann constant	IC	Integrated circuit
CM	Wet chemical methods	MACE	Metal assisted chemical etching
CVD	Chemical vapour deposition	MFP	Mean free path
CMOS	Complementary metal-oxide-semiconductor	μ TEG	Micro-thermoelectric generator
CS	Core–shell	MBE	Molecular beam epitaxy
DRIE	Deep reactive ion etching	NB	Nanobulk
DCS	Direct current assisted sintering	NP	Nanoporous bulk
σ	Electrical conductivity	NW	Nanowire
ZT	Figure of merit	NWA	Nanowire array
		PnC	Phononic crystal
		ω	Phonon mode frequency

PAS	Plasma activated sintering
PECVD	Plasma enhanced chemical vapour deposition
PF	Power factor
RTG	Radioisotope thermoelectric generator
<i>S</i>	Seebeck coefficient
Si	Silicon
$\text{Si}_{1-x}\text{Ge}_x$	Silicon–germanium alloys
SL	Superlattice
κ	Thermal conductivity
TEG	Thermoelectric generator
TF	Thin film
VLS	Vapour liquid solid
WSN	Wireless sensor network

1. Introduction

1.1. Thermoelectric generation: basic principles and applications

Thermoelectric generators (TEGs) convert thermal to electrical energy by means of the Seebeck effect, allowing them to power electronic devices wherever a temperature difference is present, as illustrated in figure 1.

The lack of mobile or short lasting parts as well as scalable architecture makes TEGs suitable candidates for niche applications in which reliability, unmanned operation and miniaturization requirements have priority over conversion efficiency. Thus, TEGs have been used in space missions within radioisotope thermoelectric generators (RTGs) for powering remote stations in gas pipelines and more recently in thermal energy harvesting applications, i.e. for powering nodes of wireless sensor networks (WSNs) from ambient temperature differences [2]. Thermal energy harvesting is of particular interest for industrial environments, which need monitoring of many difficult access/remote spots where ambient thermal sources are available, namely, process-steam pipes, heat exchangers, exhaust chimneys or heavy duty motor carcasses. Due to the increasing trend of automation and data exchange in manufacturing—often termed Industry 4.0 or the Industrial Internet of Things—these miniaturized thermal energy harvesting technologies have raised a lot of interest lately [3]. Micro-thermoelectric generators (μ TEGs)—miniaturized TEG devices with overall sizes of 1–100 mm² and powers of 1–1000 μ W—are obtained by means of micro-fabrication techniques commonly employed in the microelectronics industry. Their small size and cost, the possibility of obtaining them directly connected to integrated circuits (ICs) and their capacity of generating 100–1000 mWh cm⁻² · yr⁻¹ when placed on top of hot surfaces—enough to power a WSN node—make them excellent candidates for energy harvesting applications [1].

The core element of TEG devices is the semiconductor thermoelectric material, which largely influences in the thermal to electrical conversion efficiency (typically 5%), the power density at fixed temperature differences (from 10⁻⁶ to 1 W cm⁻²) and the cost of energy converted (from 1 to 10⁴ \$ W⁻¹) [4]. These performance parameters increase with the dimensionless thermoelectric figure of merit ZT , defined as:

$$ZT = \frac{S^2\sigma T}{k} = \frac{P_F T}{\kappa_E + \kappa_L} \quad (1)$$

where S is the Seebeck coefficient, σ the electrical conductivity and κ the thermal conductivity of the material, which can be separated in electronic and lattice contributions κ_E and κ_L , respectively. The power factor $P_F = S^2\sigma$ indicates the degree of electronic performance of the material and needs to be maximized (i.e. high S and high σ) in order for the TEG to yield high voltages and currents, while the thermal behaviour is given by κ , which needs to be as low as possible in order for the thermoelectric material to be able to sustain high temperature differences. S and σ are mostly controlled by the carrier concentration and are interrelated in such manner that ZT is maximized for semiconductors, as in insulators σ is too low and in metals S is virtually null, as illustrated in figure 2(a).

The thermoelectric materials present in currently available commercial thermoelectric modules are tellurides, e.g. bismuth telluride (Bi₂Te₃) and lead telluride (PbTe), with ZT of ~1 and optimum temperature of application of 300–450 K [5]. Despite superior properties in this range, their ZT drops fast at higher temperatures due to their rather small bandgap ($E_{gap} = 0.21$ eV). An early intrinsic behaviour leads to the deleterious bipolar effect—i.e. cancelation of the Seebeck effect due to the opposite contribution from holes and electrons. On the other hand, Si_{0.2}Ge_{0.8} alloys employed in RTGs ($E_{gap} = 0.85$ eV) operate optimally at higher temperatures, presenting a maximum ZT of 0.5 (p-type) or 0.9 (n-type) at 1000–1100 K. Alternatively, highly performing thermoelectric materials with ZT approaching 2 have been proposed and are currently under research [6–8]. So far, they have not reached the commercial stage (figure 2(b)).

1.2. Silicon-based nanostructured materials for thermoelectric generation

Bulk silicon possesses very good electrical properties for application of the thermoelectric effect with a high power factor of 50–60 μ W K⁻² cm at room temperature, when optimally doped in the range of 10¹⁹–10²¹ cm⁻³ [9–11]. Besides, it has a relatively wide bandgap ($E_{gap} = 1.11$ eV) and an elevated melting point ($T_m = 1683$ K) allowing high temperature operation before the onset of intrinsic behaviour, which is interesting for many industrial applications [12]. However, the high thermal conductivity of heavily doped silicon (90–30 W m⁻¹ · K⁻¹ when going from 300 to 1200 K) yields a maximum ZT of 0.15–0.2 at 1100 K [13–15], insufficient in most of the cases. Thus, in order to increase the potential of silicon for thermoelectric applications, its thermal conductivity at intermediate temperatures must be reduced.

This may be attained by two major strategies which aim to reduce the lattice contribution to thermal conductivity κ_L , which is proportional to the phonon mean free path (MFP) and accounts for more than 95% of total κ in heavily doped silicon [14, 15]. In a first alloying-based approach, silicon-rich compounds—rather than pure silicon—are employed. Differently-sized, randomly-positioned atoms of different species serve as point defects that effectively scatter phonons of short

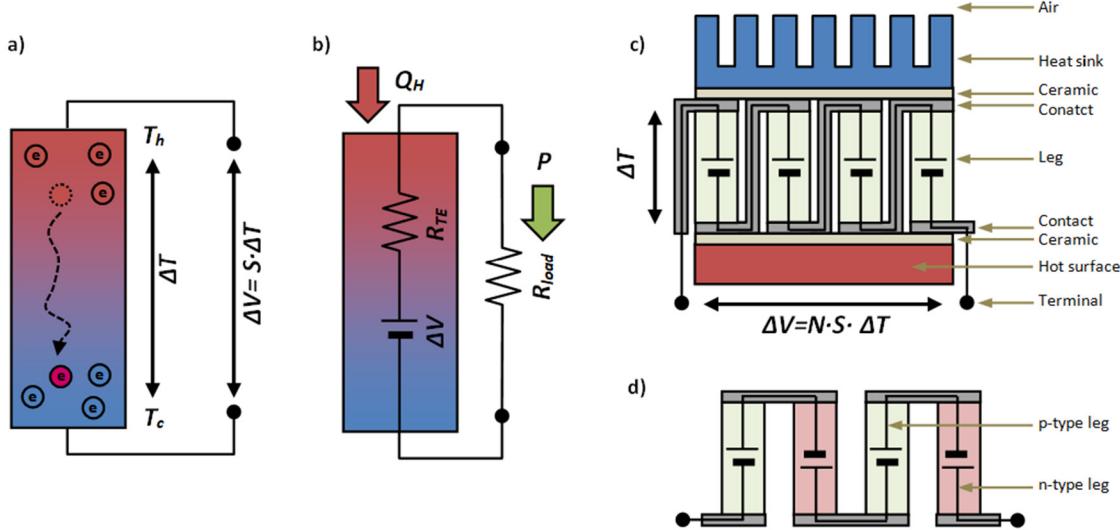


Figure 1. (a) Seebeck effect in a metal or n-type semiconductor. Electrons diffuse from the hot part to the cold part when the material is subjected to a temperature difference ΔT , leading to a Seebeck voltage $\Delta V = S \cdot \Delta T$, where S is the Seebeck coefficient. (b) Thermoelectric material connected to an electrical load, acting as a single-leg TEG. (c) Multiple-leg TEG in uni-leg configuration, with voltage build-up flow and parts indicated. (d) Multiple-leg TEG in uni-leg configuration, with voltage build-up indicated (only legs and contacts are shown). Reprinted from [1], Copyright (2018), with permission from Elsevier.

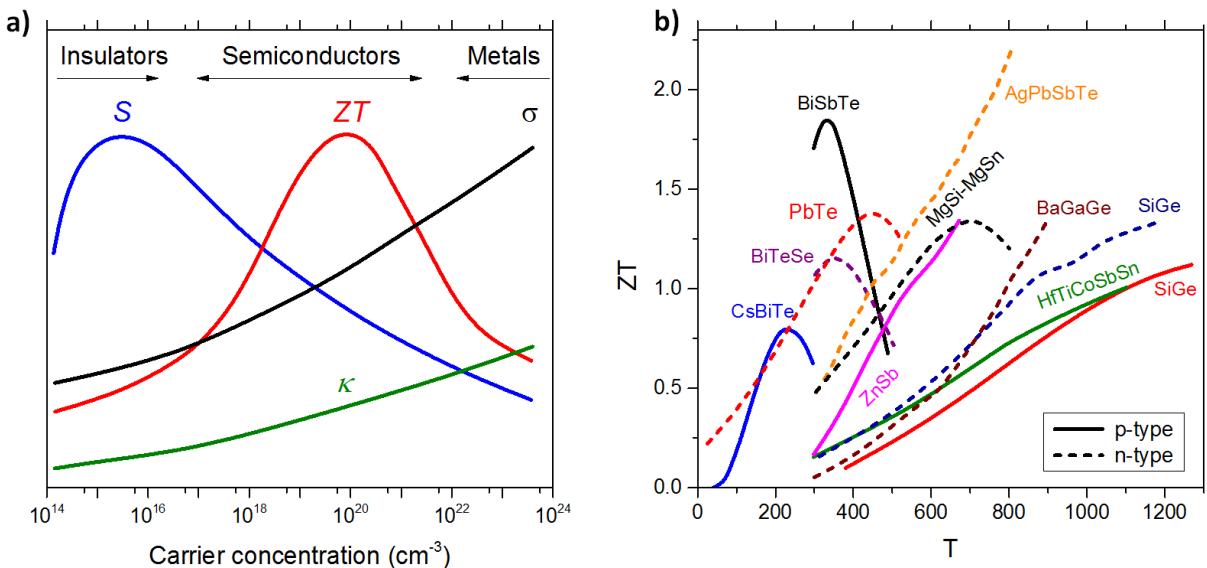


Figure 2. (a) Illustrative plot of Seebeck coefficient S , electrical conductivity σ , thermal conductivity κ and thermoelectric figure of merit ZT with respect to carrier concentration. (b) ZT with respect to temperature for some state of the art semiconductor materials. Reprinted from [1], Copyright (2018), with permission from Elsevier.

wavelengths, which account for most of the heat transport in silicon (i.e. with $\lambda < 3 \text{ nm}$) (figure 3(b)) [16]. Moreover, the incorporation of other atoms enables the use of complex unit cells with further reduced κ as the Nowotny chimney ladder structure in higher manganese silicides (HMS) or Si-based clathrate structures. The second and more recent approach is nanostructuration. Fabricating silicon and silicon-based materials with characteristic dimensions in the order of 10–100 nm introduces a high density of interfaces which leads to increased phonon boundary scattering. This mechanism reduces noticeably the MFP of phonons of intermediate to high wavelengths, more or less effectively depending on the type of nanostructure employed, as illustrated in figures 3(c)–(e). Additionally,

nanostructuration allows exploiting other size-effects that further enhance the thermoelectric behaviour as energy filtering in nano-grains and superlattices (SLs) (increasing S), dopant modulation in nano-composites and SLs (increasing σ) and surface roughness scattering and coherent effects in nanowires and phononic structures (further decreasing κ), as explained in forthcoming sections. Quantum effects as quantum confinement, semimetal-semiconductor transition, carrier pocket engineering or phonon localization have been theoretically predicted and demonstrated to some extent in rather small systems, so far non-scalable and thus incompatible with device integration [17]. While both alloying and nanostructuration introduce additional means for charge carrier scattering—i.e.

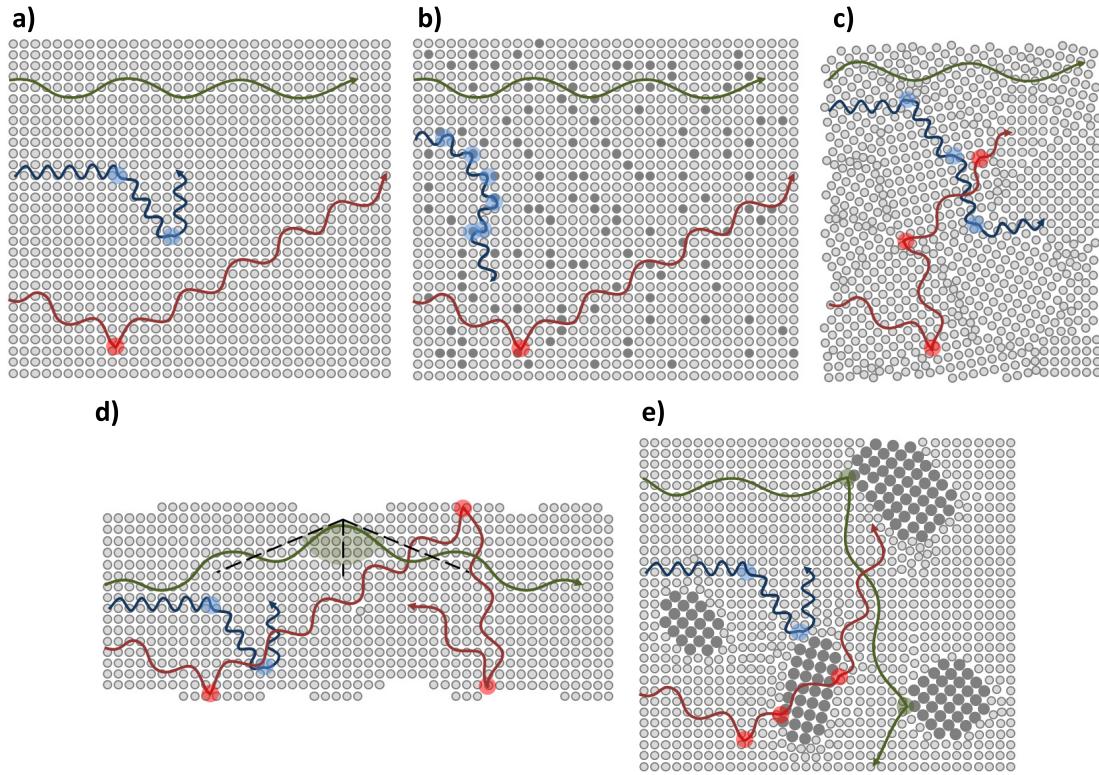


Figure 3. Scheme illustrating the effects of alloying and nanostructuring in phonon transport of silicon-based thermoelectric materials. Blue, red and green waves represent short, intermediate and long wavelength phonons, respectively, and shadowed areas indicate collision/scattering events. (a) Single crystal silicon bulk, in which MFP, determined by point scattering with dopants, increases with increasing wavelength. (b) Single-crystal alloyed silicon (e.g. $\text{Si}_{0.8}\text{Ge}_{0.2}$), in which short-wavelength phonon scattering is enhanced by Ge point defects. (c) Nano-crystalline silicon bulk, in which intermediate-wavelength phonon scattering is enhanced at grain boundaries. (d) Nanowire/thin film, in which intermediate-wavelength (diffuse) and long-wavelength (specular) phonon scattering are enhanced at boundaries. (e) Nano-composite in which long wavelength phonon scattering is enhanced by nano-inclusions.

electron/hole scattering at point defects and interface, respectively—they affect to a lower extent the electrical conductivity, so that the overall effect is an increase of σ/κ and thus and enhancement of ZT .

Thus, following these strategies, silicon and some compounds comprising silicon as one of its main components—referred hereon as silicon-based materials—constitute a family of thermoelectrics with high potential for moderate to high temperature application, with maximum ZT in the range of 800–1200 K. The most important silicon-based thermoelectric materials are nanostructured silicon (Si), silicon–germanium alloys ($\text{Si}_{1-x}\text{Ge}_x$) and silicides—i.e. metal–Si compounds in which the latter is the more electronegative element. Most important silicides for thermoelectric applications are those of chromium (CrSi_2), magnesium–tin ($\text{Mg}_2\text{Si}_{1-x}\text{Sn}_x$), manganese ($\text{MnSi}_{1.7}$), ruthenium (Ru_2Si_3), rhenium ($\text{ReSi}_{1.75}$) and iron ($\beta\text{-FeSi}_2$) [18].

Apart from the aforementioned material properties, silicon-based materials present two key characteristics, which make them excellent candidates for integration and application in TEG and μ TEG devices. First, microelectronics technology is based on processing of silicon wafers and relays on silicon-based materials for the fabrication of common semiconductor devices, e.g. Si–Ge strained channels for

high speed bipolar/CMOS (BiCMOS) transistors or low-resistive, highly-stable silicide contacts in all kind of micro-devices [19]. Thus, silicon-based materials benefit from the massive knowledge around microfabrication materials and techniques and an excellent compatibility with the latter, enabling a facile integration in μ TEG devices by means of mainstream/CMOS processes. Integration in μ TEG rather than TEG devices becomes a must when aiming to employ low-dimensional materials as nanowires or thin films due to their limited overall sizes related to available nanofabrication methods. For this reason, microtechnology compatibility is a particularly useful asset. The second feature of silicon is that it is an abundant raw material, being the second most abundant element in earth crust (28% in weight) and because of that, inexpensive. With exception of $\text{Si}_{1-x}\text{Ge}_x$ alloys, silicon-based thermoelectric materials exhibit a very low cost ($1\text{--}7 \text{ \$ kg}^{-1}$, while traditional thermoelectrics cost about $100 \text{ \$ kg}^{-1}$), being only above those of some polymer and oxide thermoelectrics with rather low efficiency ($ZT < 0.07$) [4]. In the case of $\text{Si}_{1-x}\text{Ge}_x$, nanostructuration allows to drastically reduce the amount of expensive Ge employed in the alloy ($900 \text{ \$ kg}^{-1}$), while achieving equal or superior ZT values than those employed in space missions, e.g. from $x = 0.3$ to $x = 0.05$ as in the work of Yu *et al* [20].

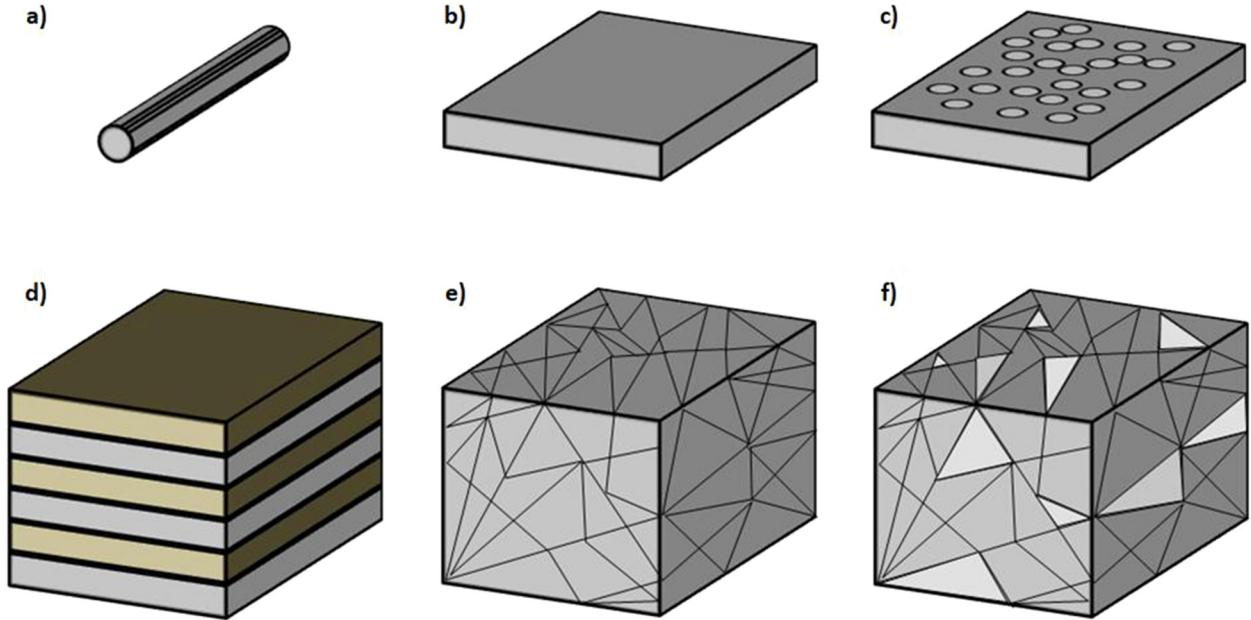


Figure 4. Different nanostructured materials considered in this work. (a) Nanowire, with diameter ≈ 100 nm. (b) Thin film, with thickness ≈ 100 nm. (c) Nano-porous and perforated membrane, with holes and necks of size ≈ 100 nm. (d) superlattice, with period and layer thickness ≈ 100 nm. (e) Nanocrystalline bulk, with crystal domain sizes ≈ 100 nm. (f) Nano-composite bulk, with crystal domain and inclusion sizes ≈ 100 nm.

1.3. Scope of the review

All in all, silicon-based nanostructured materials are outstanding candidates for the use of the thermoelectric effect in TEG and μ TEG devices for moderate to high temperature applications, combining diverse strategies for enhancing ZT and employing inexpensive and technology compatible materials, as illustrated in figure 5. Many theoretical and experimental works were conducted in the last decade in order to assess fabrication, thermoelectric behaviour and applicability of silicon based-materials for thermal to electrical energy conversion. Several excellent review works focused on specific topics [18, 21–26]. For instance, the work of Schierning *et al* covered the fabrication, characterization and device aspects for silicon nanostructures up to 2013 [11]. The comprehensive work of Nozariasbmarz *et al* reviewed the advances in fabrication and characterization of bulk, nano-crystalline bulk and nano-composite bulk of silicon germanium and silicides up to 2017 [18]. The overview of Fleuriol and Vining summarize the major results and challenges concerning bulk and micro-/nanostructured bulk $\text{Si}_{1-x}\text{Ge}_x$ alloys until 1993 [25]. Recently, Liu *et al* reviewed the topic of HMS, discussing their material, mechanical and thermoelectric properties, fabrication and potential applications [26]. Complementary, the present work covers recent advances in fabrication, characterization and device integration of nanostructured silicon-based thermoelectric materials with an application-oriented focus. Different forms of homogeneous and composite nanostructures of silicon-based materials were considered in this work, shown in figure 4. The paper is organized in three sections, apart from the introduction. Section 2 presents the recent advances in fabrication and thermoelectric characterization of silicon-based nanostructures. It is divided into subsections for

detailling the topics of nanowires, thin films and SLs, nanostructured bulk and nanoporous bulk. Section 3 presents TEG and μ TEG devices integrating silicon-based nanostructures as thermoelectric materials. Finally, in section 4, an overview and a prospective of the topic is included on the basis of the recent findings.

2. Silicon-based nanostructured thermoelectric materials

2.1. Nanowires

Nanowires are high aspect ratio elongated structures with a diameter smaller or in the order of 100 nm (figure 4(a)). The main effect driving thermoelectric behaviour enhancement in nanowires is the reduction of their thermal conductivity κ by enhanced diffuse phonon boundary scattering. Scattering of short-wavelength (high-frequency ω) phonons is dominated by other mechanisms also present in bulk, i.e. point defect scattering by ionized impurities and lattice vibrations with a rate $\propto \omega^4$ (figure 3(d), blue wave). On the other hand long-wavelength phonons are specularly rather than diffusively scattered at boundaries and thus keep their momentum unaltered (figure 3(d), green wave). Thus, regarding κ reduction, this mechanism has a significant effect in phonons with intermediate frequencies (figure 3(d), red wave).

2.1.1. Silicon and silicon–germanium nanowires—synthesis and integration. In order to exploit their thermoelectric behaviour, silicon-based nanowires must be grown with optimized carrier concentration—controlled by impurity doping in Si/Ge- and integrated in dense arrays of several million NWs cm^{-2} in μ TEGs so that the device is able to yield a high

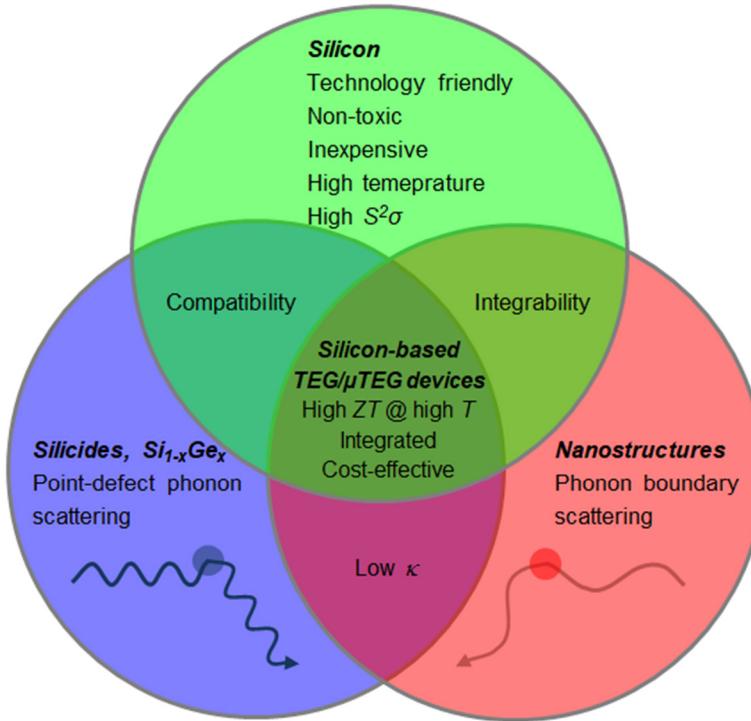


Figure 5. Diagram schematizing the advantages of employing silicon-based nanostructured materials for integration in thermoelectric generator (TEG) and micro-TEG (μ TEG) devices.

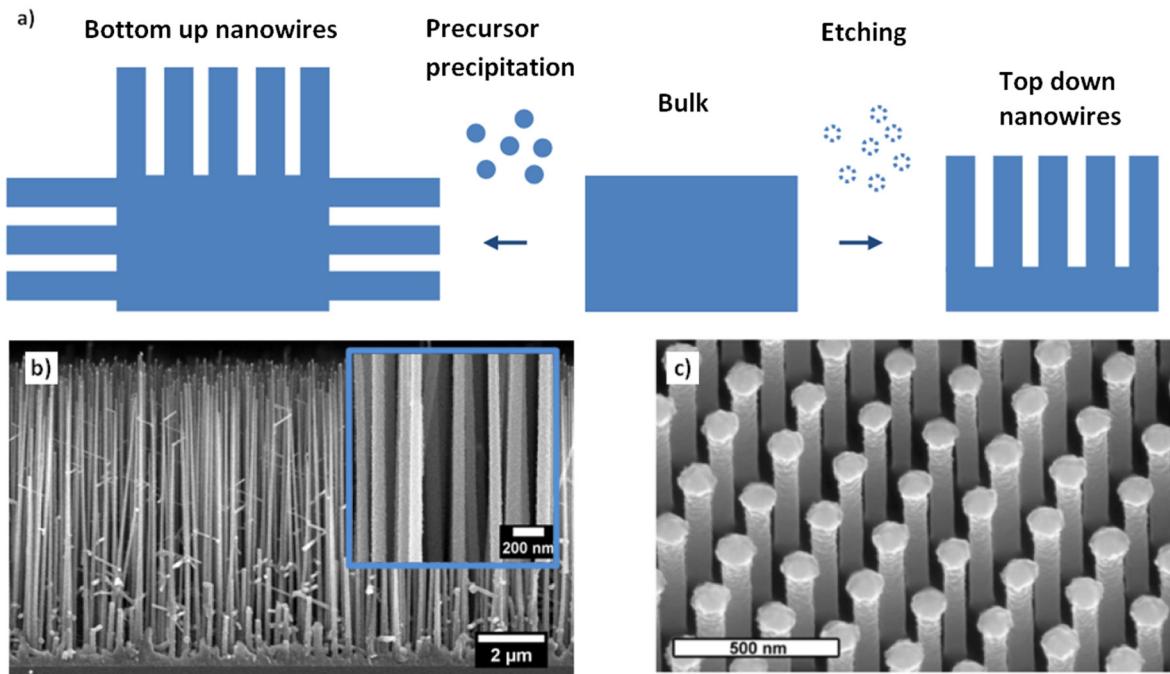


Figure 6. (a) (Top row) Schematic of bottom-up versus top-down nanowire growth methods. Reprinted from [1], Copyright (2018), with permission from Elsevier. From middle to left, bottom-up route, with direct formation of nanowire structures by precipitation of semiconductors in nanowire shape. From middle to right, top-down route, with etching of nanowires from a bulk semiconductor. (b) SEM image of a silicon–germanium nanowire array produced by a bottom-up method (vapour liquid solid growth). Reproduced from [27]. CC BY 3.0. (c) SEM image of silicon nanowire array grown by a top-down method (laser interference nanolithography) [28] (2012) © TMS 2012. With permission of Springer.

power. Moreover, this must be done in such a manner that electrical or thermal parasitic resistances are avoided. This can be achieved by forming low-resistive contacts with low voltage and thermal drops as well as by avoiding thermal leakages to

the surroundings, which will generate parallel thermalization reducing the Seebeck voltage.

Semiconductor nanowires for thermoelectric applications of different elements and compounds can be fabricated, doped

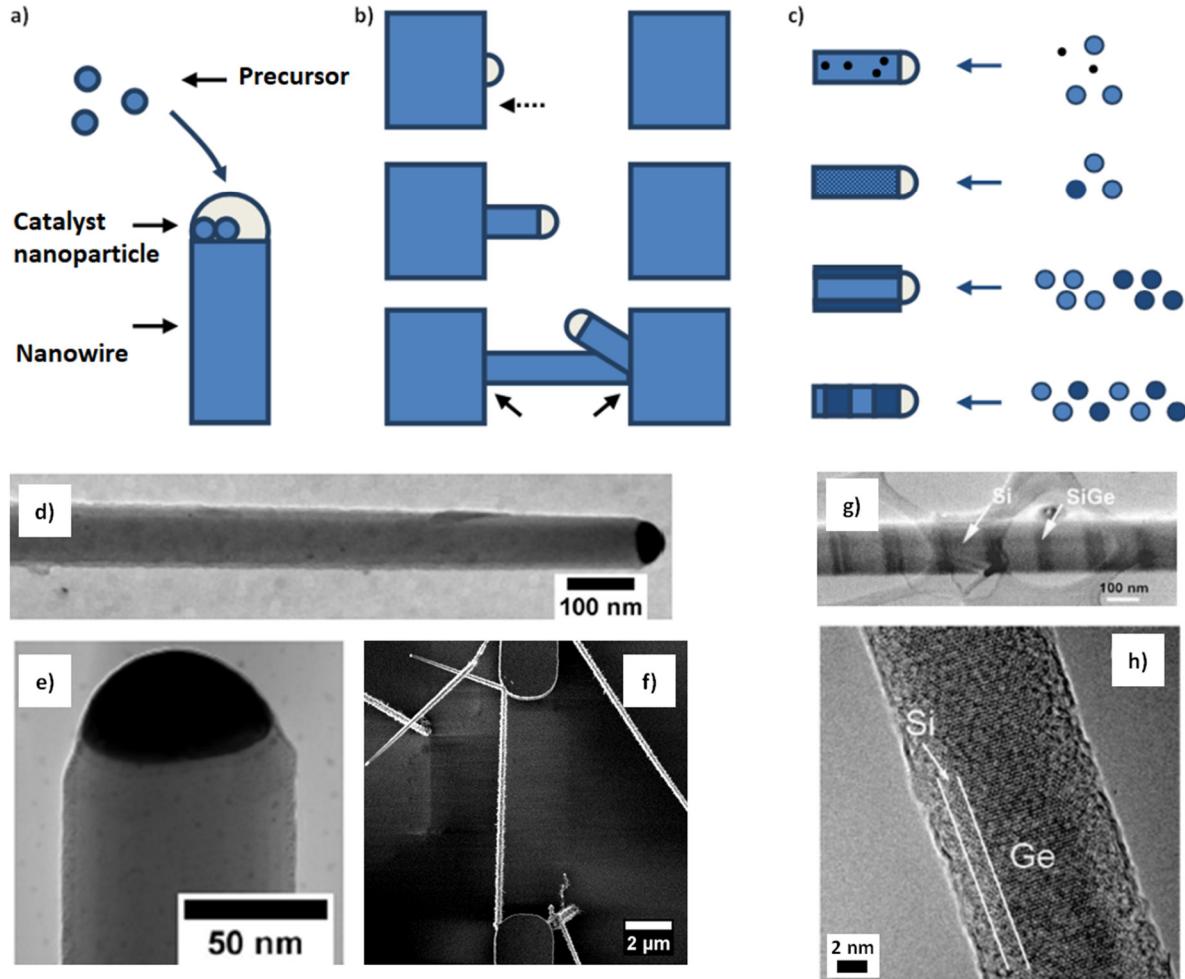


Figure 7. Metal-catalyzed based nanowire growth methods for Si and Ge alloys and heterostructures. (a) Metallic nanoparticle catalyst driven nanowire formation mechanism. (b) Epitaxial growth of nanowire from a crystalline plane (dotted arrow) and formation of monolithic connection (solid arrows). (c) From top to down: formation of doped nanowire, alloy nanowire, core shell nanowire and superlattice nanowire. (a)–(c) Reprinted from [1], Copyright (2018), with permission from Elsevier. (d)–(f) TEM and SEM images silicon nanowires obtained by vapor liquid solid (VLS) growth. (d), (e) Reproduced from [35]. CC BY 3.0. (f) Reproduced from [27]. CC BY 3.0. (g) TEM image of silicon/silicon–germanium superlattice nanowire grown by laser assisted VLS. Reprinted with permission from [36]. Copyright (2003), AIP Publishing LLC. (h) TEM image of germanium/silicon core/shell nanowire grown by VLS growth. Reprinted with permission from [37]. Copyright (2011) American Chemical Society.

and contacted by a myriad of methods, comprehensively reviewed in [1]. These can be categorized as bottom-up—in which precursors are precipitated in the form of a nanowire, as in figure 6(a)—or as top-down, in which nanowire structures are defined by etching a semiconductor wafer (typically silicon), as in figure 6(b). Both groups offer different advantages and drawbacks for the integration of nanowires in TEGs but, in general terms, it can be said that (i) bottom-up makes a more efficient use of precursors and allows to fabricate dense arrays of diverse materials, and (ii) top-down provides a finer control and enables a more facile integration, mostly with silicon.

Due to compatibility and ease of fabrication issues, most nanowires obtained in scalable processes compatible with device integration are made of Si and $\text{Si}_{1-x}\text{Ge}_x$. Dense arrays of doped silicon and silicon–germanium nanowires can be obtained by different bottom-up methods based in the use of metal vapour deposition techniques for providing silicon and metal catalyst nanoparticles to promote the nanowire growth, as illustrated in figure 7(a). Vapour liquid solid (VLS), vapour

solid–solid (VSS) and molecular beam epitaxy (MBE) growth routes are the most representative examples [29]. Introduction of different ratios of Si, Ge and dopant gas precursors in a chemical vapour deposition (CVD) or MBE reactor, and choosing of appropriate process conditions (T of $500\text{ }^\circ\text{C}$ – $900\text{ }^\circ\text{C}$ depending on precursors, P of 10^{-3} – 20 Torr) allow growing single crystalline, epitaxial Si and $\text{Si}_{1-x}\text{Ge}_x$ nanowires with a controlled doping level. Moreover, alternate introduction of Si/Ge precursors (figure 7(c)) may be employed for generation of Si/Ge nanowire heterostructures that, apart from phonon boundary scattering, may provide additional mechanisms to increase ZT . Epitaxial growth enables monolithic integration of nanowires in trench based micro-devices (figure 7(b)), as demonstrated in the works of Islam *et al*, Donmez *et al* and Gadea *et al* for single Si nanowires and for dense arrays of Si/Si–Ge NWs integrated in μ TEG devices [1, 30–34]. This integration pathway typically yields low electrical contact resistance, in the order of $1\text{ }\mu\Omega \cdot \text{cm}^2$ and negligible thermal contact resistance, which are critical for successful exploitation of the thermoelectric effect in μm -long structures [27, 34]. While

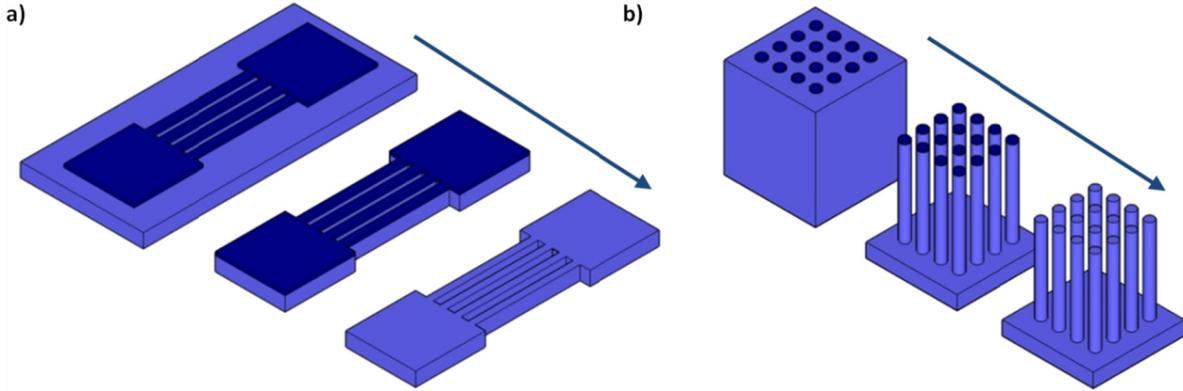


Figure 8. Top-down, nanolithography-based process for obtaining nanowires. (a) Horizontal and (b) vertical configuration. A mask is deposited on top of the semiconductor. Then, top-down etching process is performed leading to the definition of the wires. Then, the mask is removed and free-standing nanowires are obtained. Reprinted from [1], Copyright (2018), with permission from Elsevier.

control of nanowire properties is not as accurate as in top-down methods, bottom-up ones have a great potential as they enable easy fabrication of heterostructures and integration of relatively dense arrays of suspended nanowires in a single fabrication step.

Silicon nanowires were fabricated as well by top-down etching of doped silicon wafers, with nanolithography and metal assisted chemical etching (MACE) approaches [29, 38] (figures 8 and 9). Horizontal nanolithography enables full monolithic integration and moderate nanowire density, as nanowires are confined within a single plane (figure 8(a)). These were recently integrated in devices in the works of Pennelli *et al*—suspended in a robust interconnected network fashion—and Hashimoto *et al*—as aligned arrays laying on bulk Si [39–41]. Ferri *et al* and Tasdemir *et al* devised strategies for overcoming the density issue [42, 43]. The former employed a combined bottom-up deposition of polysilicon at nano-recessions/top-down definition of polysilicon nanowires in order to generate additional nanowire layers embedded in insulating materials, with a similar scalability than that of superlattice fabrication schemes. The latter took advantage of the scalloping artefact of the deep reactive ion etching process (DRIE) in order to define several layers of horizontal nanowires (figure 9(a)). While at an early stage with plenty of room for improvement, these methods posses great potential for fully monolithic integration of top-down nanowires in μ TEG devices.

Vertical top-down techniques (vertical nanolithography and MACE) yield monolithic contacts only in the bottom side and allow for a high density extending in the three dimensions. Yida *et al* and Curtin *et al* fabricated and integrated dense arrays of vertically aligned silicon nanowires in thermoelectric μ TEG devices with vertical nanolithography [28, 44]. Insulating filler (silicon oxide or polyimide) was deposited around the nanowires, and nickel/nickel–gold film was evaporated/sputtered at the upper exposed part, for forming Ni–Si contacts upon subsequent annealing. While formation of contacts according to this scheme yield indeed a non-limiting electrical contact resistance [45, 46], the implementation of a filler supposes an increase of the parallel parasitic thermal conductance, which might lead to a decrease of the naturally attainable ΔT and thus S voltage of

the devices. On the other hand, Xu *et al* grew dense arrays of Si nanowires by MACE and $\text{Si}_{1-x}\text{Ge}_x$ nanowires by a combination of poly $\text{Si}_{1-x}\text{Ge}_x$ deposition on a Si wafer and subsequent MACE [47]. In this case, the as-grown nanowire arrays were directly contacted by pressing them from above with a copper plate. As the nanowires could not be highly doped due to fabrication constraints (in MACE NW growth wafers with $\rho > 10^{-3} \Omega \cdot \text{cm}$ are required [38, 48]) this led to the formation of highly resistive Schottky contact, which hindered effective exploitation of the thermoelectric effect. This problem was solved later by increasing the carrier concentration of the uppermost part of the array after growth, up to $\sim 10^{19} \text{ cm}^{-3}$, using a spin-on-doping approach [49]. However, despite being reduced to a great extent, the resistance of the direct contacts was still of the same order than that of the nanowire arrays, probably related to a small surface of copper effectively contacting the Si nanowires. Recently, Dimaggio *et al* demonstrated how copper electrodeposition on the tips of silicon nanowires might serve to address this issue [50].

2.1.2. Silicon and silicon–germanium nanowires—thermoelectric properties. Nanowires offer a most interesting structure to study fundamental phenomena at the nanoscale as are in a balanced position between phenomenology (possessing two confined dimensions, rather than one as thin films) and accessibility (having one large dimension, rather than none as quantum dots). For this reason, many experimental and theoretical works concerning nanowire properties have arisen in the last years, more than in other nanostructured and low-dimensional systems. This applies as well for thermoelectric properties, and so up to date many measurements S , σ or κ of Si, $\text{Si}_{1-x}\text{Ge}_x$ and $\text{Si}/\text{Ge}/\text{Si}_{1-x}\text{Ge}_x$ heterostructure nanowires have been reported. These measurements are usually performed in microstructures and are thoroughly reviewed in [1, 52].

In most reported cases, a nanostructure-enabled enhancement of the thermoelectric figure of merit ZT was revealed, chiefly due to a reduction of κ . This was mostly attributed to an enhanced phonon boundary scattering conferred by the limited dimensions and the highly available surface area provided by the nanowire structure (figure 10(a)). In some cases,

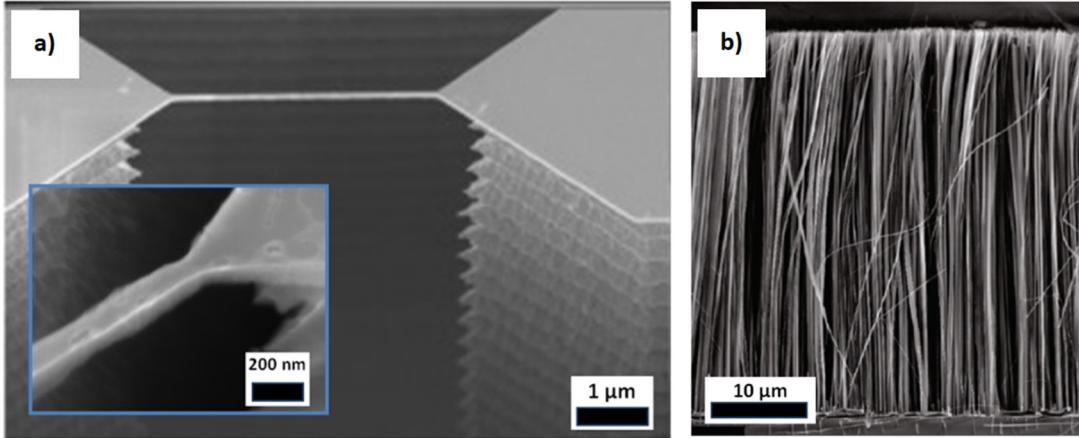


Figure 9. Nanowires defined by top-down methods. (a) Single nanowire defined by DRIE-based, horizontal nanolithography process. Reprinted from [51], Copyright (2017), with permission from Elsevier. (b) Rough silicon nanowires grown by MACE. Reprinted with permission from [48]. Copyright (2009) American Chemical Society.

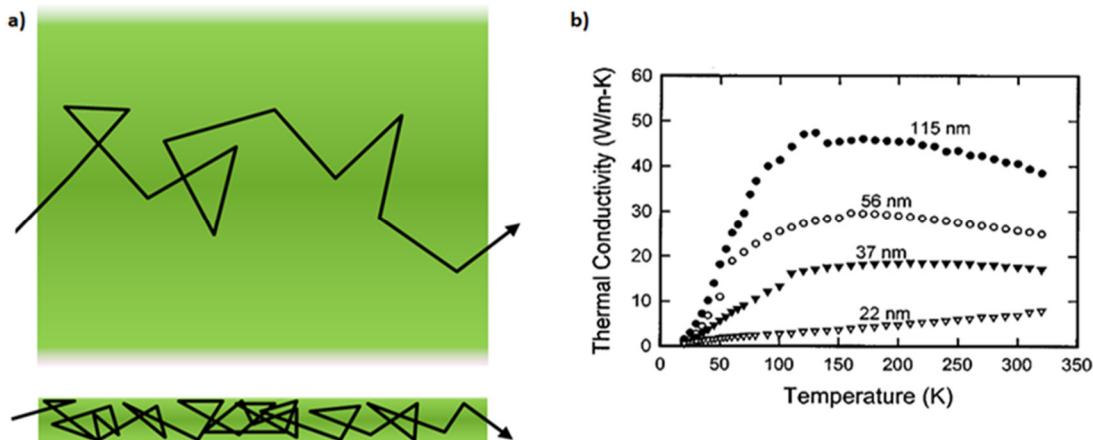


Figure 10. (a) Representation of heat transport in solid materials, in which heat is carried by phonons (black arrow). Top part shows a bulk material, with MFP not limited by boundaries. Bottom part shows a nanowire, with MFP limited by boundaries. Reprinted from [1], Copyright (2018), with permission from Elsevier. (b) Thermal conductivity of VLS-grown silicon nanowires. Reprinted with permission from [53]. Copyright (2003), AIP Publishing LLC.

other phononic effects and even electronic effects—not necessarily beneficial—were claimed.

2.1.2.1. Boundary and alloying phonon scattering. The κ reduction due to phonon boundary scattering was first observed in silicon nanowires by Li *et al* in 2003 [53]. The measuring method was that introduced by Shi *et al* the same year based on suspended heated microstructures [54]. This approach has been adopted by the community as the standard for determination of κ in nanostructures. In the work of Li *et al*, thermal conductivity of VLS-grown silicon nanowires decreased from 41 to 7 W m⁻¹ · K⁻¹ as diameter decreased from 115 to 22 nm (figure 10(b)). These results—and many others of VLS/etched nanowires—fitted well with the picture of diffusive phonon boundary scattering, i.e. assuming that dominant phonons fully randomize their momentum when arriving at a boundary [55–59], as illustrated in figures 3(d) and 11(a) (red wave). However, depending on the phonon wavelength and the surface roughness, scattering might be specular and thus not contribute to diminish thermal conductivity, as illustrated in figure 3(d) (green wave). Smoother nanowires and

long dominant wavelengths will lead to increased specularity [60]. Thus, surface roughness—determined by fabrication process—and dominant wavelength—determined by measurement temperature and composition—fluence in the effectivity of small diameters in reducing κ . However, this picture of diameter dependence of κ only relaying in boundary scattering events is expected to loss validity below 20 nm, as at this point phonon confinement effects are expected to arise, diminishing average propagation velocity and density of states [61].

In the case of Si_{1-x}Ge_x, alloying-induced scattering affects low-wavelength phonons leading to a drastically reduced thermal conductivity—from 150 W m⁻¹ · K⁻¹ in bulk Si to 10 W m⁻¹ · K⁻¹ in Si_{0.5}Ge_{0.5}—dominated by intermediate-to-long wavelength phonons, as reported in several experimental and theoretical works concerning single crystal bulk [16, 25, 62–64].

In nanowires, diffusive—i.e. κ -reducing—boundary scattering disturbs mostly the intermediate-wavelength phonons leaving behind a small fraction phonons unaffected by alloying and nanostructuration, with long-wavelengths and

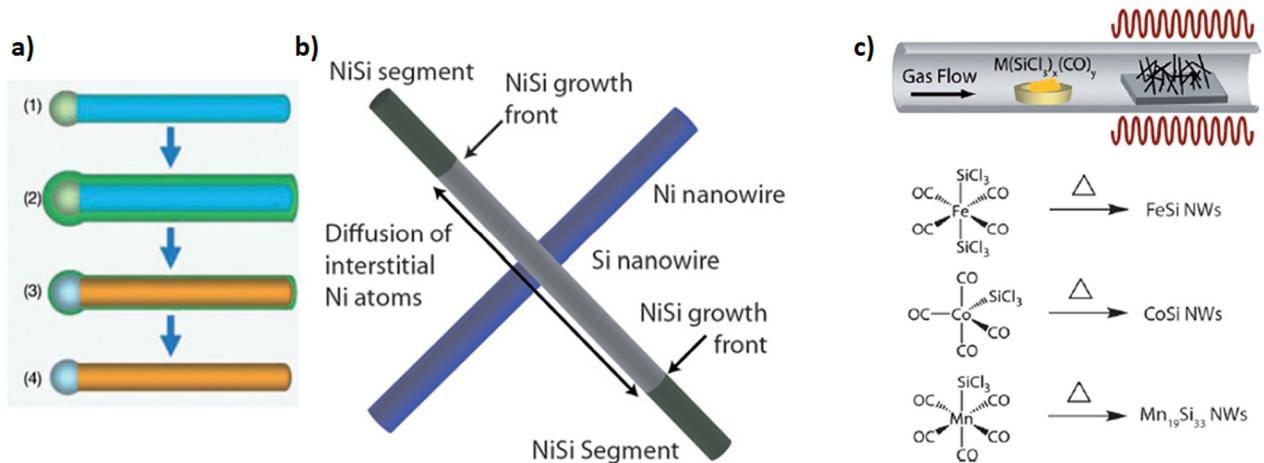


Figure 11. Methods for fabrication of silicide nanowires. Reproduced from [23] with permission of The Royal Society of Chemistry. (a) Silicidation by evaporation of metal on top of Si NWs and subsequent thermal annealing. (b) Silicidation by annealing contacting Si and Ni NWs and subsequent thermal annealing. (c) CVD method using single source precursors for direct precipitation of silicide nanowires on top of desired substrates. Precursors are evaporated upstream, transported by an inert gas and deposited downstream as they are cooled.

MFPs [65]. While not as evident as in pure silicon nanowires, the thermal conductivity of $\text{Si}_{1-x}\text{Ge}_x$ nanowires also decreased with decreasing diameter [66–69]. The weaker diameter dependence is explained by the fact that in $\text{Si}_{1-x}\text{Ge}_x$ only a reduced fraction of phonons is effectively affected by boundaries, with regards to κ reduction. Values as low as $1\text{--}2 \text{ W m}^{-1} \cdot \text{K}^{-1}$ were obtained in nanowires with 40–60 nm diameter in comparison of $4\text{--}5 \text{ W m}^{-1} \cdot \text{K}^{-1}$ for highly doped bulk of same composition [62, 67]. In a more detailed study, up to 450 K and with a broad range of compositions and diameters, Lee *et al* observed that boundary scattering effect was important down to $\sim 100 \text{ nm}$ [67]. Beyond that point, further improvement could only be attained by tuning the alloy concentration, coinciding with Amato *et al*, who reviewed this area up to 2014 [21].

2.1.2.2. Surface roughness enhanced phonon scattering. VLS grown Si/Si_{1-x}Ge_x nanowires presented a rather smooth surface compared to etched nanowires produced by MACE [56, 70, 71] or VLS-grown, intentionally-roughened nanowires [72]. Measurement of κ in these nanowires yielded low values down to $1.6 \text{ W m}^{-1} \cdot \text{K}^{-1}$ for 52 nm-thick silicon nanowires [70]. These values of κ are well below those calculated for fully diffusive phonon scattering at boundaries, which was already assumed to take place in the case of smoother nanowires [55, 61]. Thus, these trends observed in rough nanowires are often referred as sub-diffusive or said to be below the Casimir limit—who first reported a mathematical solution for a grey model in which fully diffusive boundaries were assumed [73]. Lim *et al* found a quantitative relation between roughness properties—as correlation length, root mean square roughness and power spectra parameters, determined by TEM—and the reduction of thermal conductivity in silicon nanowires [71]. Later, Kim *et al* demonstrated this effect in Si_{1-x}Ge_x, which presented a thermal conductivity four times smaller than that of a corresponding smooth nanowire and one order of magnitude below the bulk alloy [72]. Many works attempted to explain these results offering

explanations based in phonon localization extending from the rough surface, multiple phonon scattering events occurring at the nano-roughness recession, non-Gaussian roughness distributions and coherent effects [74–76]. Some of these effects support latest experimental results from Kim *et al*. However, it is still difficult to find a fully convincing explanation for the outstanding values of $\kappa \sim 1\text{--}2 \text{ W m}^{-1} \cdot \text{K}^{-1}$ (close to the amorphous limit) presented in 2008 by Hochbaum *et al* (for rough silicon nanowires) and Boukai *et al* (for smooth and etched Si NWs) [56, 70, 71, 77]. In this sense, forthcoming studies like that of Lim *et al* in which a reliable determination of critical properties as diameter and roughness parameters was carried out, would be of great interest for the community [71].

2.1.2.3. Silicon/germanium nanowire heterostructures. Superlattice-nanowire structures (figure 7(g)) are supposed to yield additional phonon scattering by introducing interfacial thermal resistances in series (Kapitsa resistances) and by affecting the phonon distribution (and thus density and group velocity of the modes) due to destructive interference of specular reflected phonons at these interfaces. Looking for highlighting this effect, Li *et al* grew Si/Si_{1-x}Ge_x superlattice nanowires of 58 and 83 nm in diameter by using a pulsed laser deposition assisted—VLS growth [36]. However, a rather low than expected κ reduction was attained ($6 \text{ W m}^{-1} \cdot \text{K}^{-1}$) suggesting that the main scattering mechanism was simply alloying. Similarly, Wingert *et al* grew and measured thermal conductive heterostructures of Ge/Si in the form of core–shell nanowires (CS NWs, figure 7(h)) [37]. Inner Ge cores had diameters as small as 10–20 nm. The core–shell structures presented a reduction of the value of κ with respect to bulk and similarly sized, shell-less Ge NWs. This, together with the observed anomalous temperature dependence of κ in the range 100–400 K, could be explained in terms of a modification of the phonon dispersion relation due to the presence of the Si shell. That is, a phonon quantum confinement effect could be observed pointing out the interest of this type of core–shell heterostructures for tuning the thermal behaviour

of nanowires. Recently, Hsiao *et al* measured the thermal conductivity of Si/Ge core–shell nanowires and reported a rather reduced κ with respect to bulk Si and Ge ($6 \text{ W m}^{-1} \cdot \text{K}^{-1}$ for a 23/41 nm CS NW) with weak diameter dependence and a long ballistic length ($\sim 5 \mu\text{m}$) [78]. As in their former work with $\text{Si}_{1-x}\text{Ge}_x$ nanowires, the authors attribute the effects to suppression of transmission of short-wavelength phonons [65]. In this case, localization induced by scattering of high-frequency phonons was invoked, which according to the authors would lead to a heat transport mostly mediated by the 0.1% of the remaining—long-wavelength—phonons, possibly confined at the Si–Ge interface.

2.1.2.4. Ballistic thermal transport. When the dimension across which κ is measured (the length L , in the case of a nanowire) goes below the average phonon MFP (referred as the ballistic length, L_B), the heat transport switches from a diffusive regime (with $\kappa \neq f(L)$) to a ballistic regime (with $\kappa \propto L$) [79]. Due to fabrication constraints, apart from a reduced diameter ($\sim 100 \text{ nm}$), the as-grown nanowires exhibit a typical L in the range of $1\text{--}100 \mu\text{m}$, which overlaps with MFPs of dominant phonons in silicon and $\text{Si}_{1-x}\text{Ge}_x$ alloys, according to first principle calculations and optical measurements performed in bulk and thin films [80–82]. κ dependence with L and determination of L_B allows to gain insight in phonon MFP, which may in turn serve to infer the controlling phonon scattering mechanism.

The aforementioned wavelength dependence of specularity of scattering events at boundaries can explain the recent results of Maire *et al* who observed silicon nanowires with diffusive thermal behaviour at 300 K (at which dominant wavelength = 0.3 nm) and ballistic transport at 4 K with $L_B = 4 \mu\text{m}$ (at which dominant wavelength $\sim 25 \text{ nm}$) [83, 84]. Conversely, Hsiao *et al* measured κ in VLS-grown $\text{Si}_{1-x}\text{Ge}_x$ nanowires and reported ballistic thermal conduction at room temperatures with $L_B = 8.3 \mu\text{m}$, which is high even when compared with the MFP for bulk inferred by first-principles calculations (50% of heat transport at 300 K by phonons with MFPs $< 1 \mu\text{m}$) [65, 85]. As discussed above, the heat transport in $\text{Si}_{1-x}\text{Ge}_x$ nanowires is dominated by a reduced fraction of phonons impervious to alloy-induced and boundary-induced scattering, with long-wavelengths and MFPs which yield such a high room temperature L_B .

In nanowires with $L < L_B$, κ is a function of L and is smaller than in the diffusive regime. In a similar fashion, thermal contact resistances have high weights in short structures as nanowires, and if ignored might lead to an apparently reduced κ or apparent ballistic behaviour ($\kappa \rightarrow 0$ as $L \rightarrow 0$, although not *linearly* in this case) [79]. As typical suspended lengths of nanowires used for thermal characterization are $L = 2\text{--}15 \mu\text{m}$ it is important to take both effects into account when measuring structures with MFP in the same order, i.e. silicon nanowires at low temperatures or $\text{Si}_{1-x}\text{Ge}_x$ nanowires up to room temperature in order to avoid an underestimation of κ or a mistaken perception of thermal ballistic transport signatures.

2.1.2.5. Electronic effects. Calculations done by Pichanusakorn and Bandaru revealed that positive quantum electronic

effects—i.e. able to raise, rather than decrease the thermoelectric power factor $S^2\sigma$ —would be expectable for Si–Ge NW structures with a diameter below $\sim 4 \text{ nm}$ [17]. However, up to the best of the authors' knowledge, such a thin nanowire has not been thermoelectrically characterized so far. Therefore, this interesting effect, although theoretically predicted, still needs to be experimentally demonstrated for Si/ $\text{Si}_{1-x}\text{Ge}_x$ nanowires. On the other hand, non-quantum undesired electronic effects have been observed to take place in nanowires reducing the effectiveness of their doping levels or carrier mobility, consequently, affecting σ . These phenomena are typically (i) depletion of carriers due to the presence of surface charges; (ii) dopant deactivation due to the absence of a continuous bulk around the impurity atoms; and (iii) scattering of charge carriers at nanowire boundaries.

Regarding the surface depletion of carriers, boron-doped silicon nanowires were investigated by Kimukin *et al* [86]. These authors reported a depletion layer at the surface of the nanowire and attributed it to electrostatic repulsion of holes by H^+ ions adsorbed on the surface, a phenomenon naturally taking place at room temperature. According to that work, the depleted charge density at surface was $2.8 \cdot 10^{12} \text{ cm}^{-2}$, which implied that, for their doping level of $2.1 \cdot 10^{18} \text{ cm}^{-3}$, only NWs thinner than 80 nm presented a significant decrease in conductivity affecting the thermoelectric properties. In principle, this effect could even be positive if an accumulation rather than a depletion layer was formed. For instance, in the work of Pennelli *et al* [87], it was suggested that the formation of surface states at a Si/SiO₂ interphase could be contributing to enhance σ in n-type silicon nanowires and, therefore, the ZT value.

The dopant deactivation effect was intensively investigated for boron in silicon nanowires by Diarra *et al* and Kimukin *et al* [86, 88]. The effect was explained in terms of an increase of the ionization energy in nanostructured materials with respect to the bulk counterpart. This in turn diminishes the fraction of boron atoms ionized and thus the effective doping level which determines S and σ . Full activation of the dopant atoms is allowed by values of the ionization energy close to $k_B T$ in bulk at room temperature. These values are low enough partially due to the electrostatic screening provided by mobile charge carriers nearby the dopant centre, which are abundant in bulk material. However, as the size of the material is reduced and its ends are dragged closer to the dopant centre, the number of carriers available for the screening becomes limited, consequently raising ionization energy. The same effect was studied by Kimukin *et al* [86] for phosphorous doped n-type silicon nanowires showing that diameters below 30 nm make the effect relevant for the thermoelectric properties.

The charge carrier MFP has typically values of 1–1000 nm depending on the material and temperature [89]. When the size of the material is reduced below the charge carrier MFP, important scattering of carriers at boundaries can take place. Since thermoelectric materials are heavily doped semiconductors, the dominant scattering mechanism is the ionized-impurity one, derived from the collisions of carriers—electrons and holes—with ionized dopant atoms, which present a large

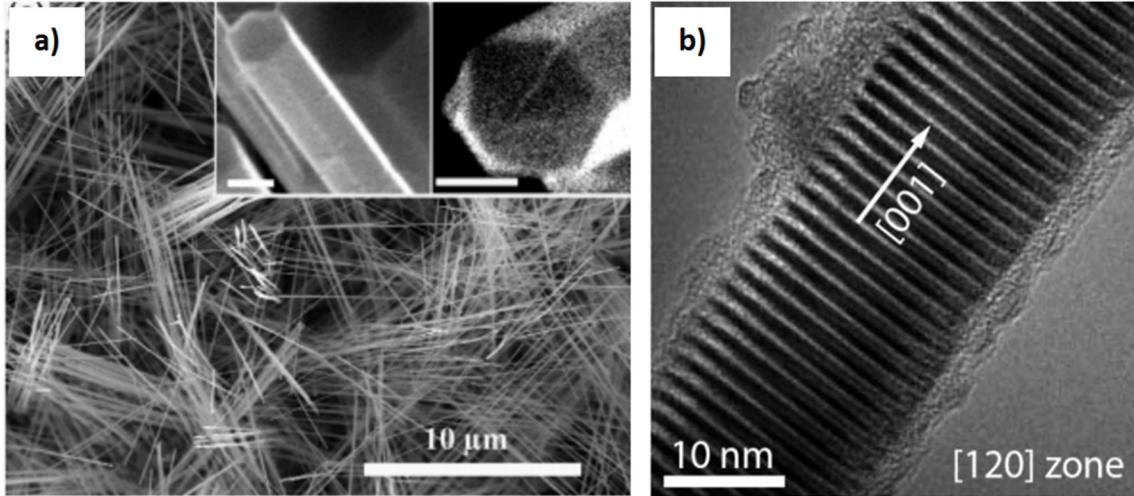


Figure 12. (a) Single crystalline CrSi_2 NWs grown by a CVD process on top of Si substrates. Reprinted with permission from [105]. Copyright (2007) American Chemical Society. (b) High resolution TEM image of higher manganese silicide nanowire (HMS) with a Nowotny chimney structure. Reprinted with permission from [106]. Copyright (2008) American Chemical Society.

radius of interaction. In this case, MFP in bulk is in the order of 2–5 nm, implying that significant σ reduction takes place only when the diameter of the nanowire is reduced below this threshold. This issue has been theoretically discussed by Seong *et al* and Shi *et al* [90, 91] but, so far, there is no experimental evidence of carrier scattering at nanowire boundaries affecting thermoelectric properties.

Finally, it is worth to mention that Mirza *et al* did not observe any of the previously mentioned conductivity degrading effects for nanowires as thin as 4 nm when using oxide-passivated top-down nanowires doped to $8 \cdot 10^{19} \text{ cm}^{-3}$ [92]. This suggests that achieving high quality surfaces might be a strategy to avoid these undesirable effects for thermoelectric applications.

2.1.2.6. Full thermoelectric characterization. So far the only works presenting a full ZT characterization (measuring S , σ and κ) of Si nanowires are those of Boukai *et al* in 2008 ($ZT = 0.4$ at 300 K and 1 at 200 K, $d = 20$ nm, by nanolithography), of Hochbaum *et al* in 2008 ($ZT = 0.6$ at 300 K, $d = 50$ nm, by MACE) and of Karg *et al* in 2013 ($ZT \sim 0.1$ at 300 K, $d = 60$ nm, by VLS) [70, 77, 93]. The disparities between the employed dimensions, growth methods and methodologies—and the fact that, in none of these works all the properties were measured for the same wire—makes difficult to perform any reliable comparative. Despite this fact, the pioneering works published in 2008 served as a demonstration of the possibility of converting silicon into an effective thermoelectric material, triggering the research in this field. In the case of $\text{Si}_{1-x}\text{Ge}_x$, the highest figure of merit was obtained by Lee *et al*, who attained 0.22 at 300 K and 0.46 at 450 K in a phosphorous-doped $\text{Si}_{0.73}\text{Ge}_{0.23}$ NW with $d = 23$ nm (with respect to 0.08 and 0.22 of the RTG bulk module with corresponding composition at 300 K and 450 K, respectively) [67].

Further works on full thermoelectric characterization of silicon nanowires—preferably analogous to that of Lee *et al* in which S , σ and κ were determined for the same nanowire—would be undoubtedly very welcomed in the field.

2.1.3. Silicide nanowires. Currently available methods for the fabrication of silicide nanowires are described in the review of Schmitt *et al* and can be generally classified in two types [23]: (i) silicidation, in which a metal is evaporated, sputtered or diffused to a silicon nanowire, followed by an annealing process at 550 °C–700 °C (figures 11(a) and (b)); (ii) vapour phase methods, in which metal/silicon precursors in gas phase at 750 °C–1000 °C are delivered by CVD or vapour transfer to a substrate containing (or not) complementary precursors, leading to the spontaneous growth of single crystal NW arrays. The first strategy was employed for partial and full silicidation of segments of nanowires for compositional, structural and growth-kinetics characterization purposes. On the other hand, vapour phase methods were successfully employed for growing dense arrays of silicide nanowires.

Four types of silicide nanowires with potential for thermoelectric applications were grown until now, namely, Cr–Si, Fe–Si, Co–Si and higher manganese silicides (MnSi_{2-x} , HMS) [94–97]. Figures 12(a) and (b) show CrSi_2 and HMS nanowires grown by vapour phase methods. Although figure 12(a) clearly shows the single crystalline nature of the CrSi_2 nanowires grown by CVD, it is worth mentioning that aligned growth of these nanowires could not be attained so far, hindering their integration in devices. In this direction, while epitaxial growth of silicide nanowires was observed in some metallic and rare earth silicides, unluckily, it could not be observed in group VI–VIII silicides [98, 99]. Therefore, endotaxial growth—i.e. growth of nanowires longitudinally attached to the substrate following a substrate-dependent crystalline structure (observed in CoSi_2 , HMS, and $\beta\text{-FeSi}_2$ nanowires)—and silicidation (attained in Co–Si, Fe–Si and Mn–Si nanowires) seem so far to be the best options for achieving a controllable growth suitable for future device integration [100]. According to Schmitt *et al*, further work in this area will likely focus on synthesizing new thermoelectric silicide nanowires such as Re_4Si_7 , $\beta\text{-FeSi}_2$, and Ru_2Si_3 [23].

As introduced above, combining silicides with nanostructuring allows harnessing the excellent electronic properties

of silicon for exploitation the thermoelectric effect by introducing phonon scattering mechanisms which reduce κ . Moreover, in the case of Mn or Ru higher silicides, the adoption of a complex, large-lattice structure such as the Nowotny chimney ladder enables further κ reduction by approaching to the phonon-glass electron-crystal behaviour in an analogous manner as skutterudites or clathrates do [101, 102]. However, despite their potential, only few works were devoted to characterize thermal and thermoelectric properties of silicide nanowires. In the recent work of Hsin *et al*, the thermal conductivity of a single β -FeSi₂ NW was measured from 300 to 500 K [103]. The results showed a reduction of κ , compared to a thin film counterpart with an inversion of the temperature dependence that indicates that thermal transport is not ruled by Umklapp scattering. This results suggest that further nanoengineering of this material could lead to improved thermoelectric performance. Up to the best of the authors' knowledge, the only full thermoelectric characterization of silicide nanowires corresponds to the work reporting on CrSi₂ nanowires carried out by Zhou *et al* in 2007, within the range of temperatures from 100 to 300 K [104]. Disappointingly, the reported figure of merit was the same as for doped bulk at room temperature, i.e. $ZT = 0.1$. This fact was attributed to a very small nanostructuring-derived reduction of κ —in contrast of what is observed in pure Si—which was naturally expected as the phonon MFP in bulk is much lower than diameter of the nanowire, according to the authors. However, nanowire κ values measured by Zhou *et al* were actually two times smaller than the ones reported in the literature for bulk (see data recently compiled by Nozariabmarz *et al* [18]) suggesting that indeed a size effect might be taking place. Complementary, an uncontrolled and not necessarily optimized carrier concentration—very sensitive to stoichiometry in CrSi₂—might be the reason for a low $S^2\sigma$ which might have shadowed the reduction of κ leading to a bulk-like ZT .

It is clear that further studies in aligned growth and thermoelectric characterization of silicide nanowires are required to fully understand the effect of the nanoscale on the thermoelectric properties and their potential to be suitable candidates for enhancing ZT in integrated, moderate-to-high temperature nanowire-based TEG devices.

2.2. Thin films

Thin films are structures in which one dimension has been restricted to the order of 100 nm (figure 4(b)). Thermoelectric thin film structures are used exploiting temperature differences along the in-plane direction, ideally allowing flow of charge carriers while blocking that of phonons due to enhanced phonon boundary scattering, and thus increasing the relation σ/κ . Having one, rather than two, limited dimensions, the set of size derived effects related to the ZT enhancement to which thin films are subjected are the same than those present in nanowire structures but to a lower extent [40]. For TEG implementation, the in-plane—rather than the cross-plane—configuration is preferred in order to be able to generate high temperature differences. The fabrication and integration

processes of thin films are generally easier than those required for nanowires, as the whole microfabrication technology is based in well-known silicon-based materials processing techniques. Obtaining polycrystalline Si and Si_{1-x}Ge_x thin films is relatively easy by using CVD processes, while achieving single crystal films can be attained by thinning a pristine wafer [107, 108].

Phonon boundary scattering effect in Si thin films was demonstrated in many works, in which thermal conductivity of thin films of single crystalline and polycrystalline Si [108–112] and Si_{1-x}Ge_x [113–117] was measured. Values of in-plane κ decrease with decreasing thickness as observed in figure 13, which shows data compiled in the recent works of Ferrando-Villalba *et al* and Cheaito *et al* [108, 113].

In the case of silicides, thin films were traditionally obtained in CMOS processes by sputtering or evaporating a metal on top of a silicon substrate and performing a high temperature annealing. However, lately other methods were developed, using magnetron-sputtering or pulsed laser deposition of both metal and silicon precursors followed by annealing (enabling finer composition/phase control) or MBE (enabling epitaxial growth) [103, 118, 119]. High power factors of as-deposited thin films of FeSi₂, CrSi₂ and HMS were demonstrated in several works [118–121]. Moreover, potentially enhanced thermal properties in β -FeSi₂ thin films were suggested in the recent work of Hsin *et al* with a temperature dependence of κ that indicates a suppression of the Umklapp scattering (similar to NWs)—usually dominating in the bulk material [103].

2.3. Superlattices (SLs)

Superlattices (SLs) are stacks of alternated thin films of two different materials (figure 4(d)). Each unit constituted by the two different materials is referred as a period. Typically SLs have few to hundreds of periods, each one with a thickness in the order of 100 nm. Due to their layer by layer fabrication process, they are anisotropic structures, with overall flat shape. These structures can be employed for harnessing the thermoelectric effect exploiting temperature differences along the in-plane or the cross-plane directions.

The in-plane approach is more interesting in terms of temperature difference generation, as larger distances between hot and cold parts can be achieved. In this configuration, phonon boundary scattering (reducing κ) and quantum confinement (increasing $S^2\sigma$ in very thin systems) are expected. Additionally, carrier pocket alignment might be observed in this direction which can lead to an increased σ . On the other hand, the cross-plane direction enables an easier device fabrication and application. In this case, a stronger phonon boundary scattering is expected, i.e. the Kapitsa resistance originated by the acoustic mismatch between the two systems (two-layer dissimilar materials). Moreover, cross plane coherent phononic effects might take place, leading to phonon spectra modification. Zone folding and band gap formation reduce propagation speed and density of states further reducing κ . Electronic effects can also be expected in the cross plane direction, analogous to those introduced in nano-bulk section,

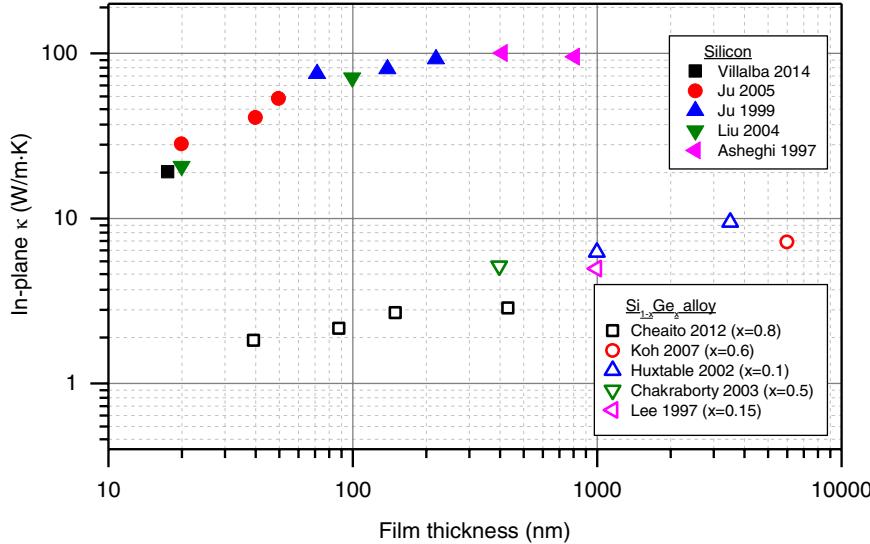


Figure 13. In-plane thermal conductivity of thin films at room temperature as a function of film thickness and crystallinity for Si ([108–112], filled symbols) and Si_{1-x}Ge_x thin films ([113–117], hollow symbols).

i.e. energy filtering and electron boundary scattering—which affect $S^2\sigma$ [17].

Silicon-based SLs were obtained by means of successive deposition of crystalline thin films using MBE, CVD, plasma enhanced CVD (PECVD) or electron-beam evaporation [116, 117, 122, 123]. Also, quantum dot SLs—i.e. SLs in which one of the two constituting layers is an embedded, discontinuous array of nanoparticles—were fabricated by quantum dot self assembly [124, 125]. In the work of Bao *et al*, for instance, each period was obtained by depositing a crystalline Si layer and subsequently several Ge monolayers, within a MBE reactor, which yielded to self-assembly of Ge quantum dot structures embedded in Si at the synthesis conditions.

The early motivation for Si/Ge/Si_{1-x}Ge_x SLs was based on the predictions from Hicks and Dresselhaus of ZT enhancement by a factor of 10 due to electronic, rather than thermal, effects in the in-plane transport properties [126]. However, most results coincided in that there was no such enhancement of $S^2\sigma$ [117, 127, 128], although the thermal conduction was effectively mitigated in Si/Ge/Si_{1-x}Ge_x SLs (mostly in the cross-plane direction). Calculations showed that the presence of quantum effects in these systems required thick barrier layers—Ge or Si in the case of Si/Si_{1-x}Ge_x or Ge/Si_{1-x}Ge_x SLs—which in case of being implemented would contribute excessively to increase κ , overthrowing the possible benefits of an increased $S^2\sigma$ [17]. Figure 14 shows cross-plane thermal conductivity measurements performed by Huxtable *et al* [116], of Si/Si_{0.7}Ge_{0.3} SLs of different periods, indicated in Å in each curve. The value of κ decreased with the period for these $x = 0.3$ samples. Another set of samples in which less Ge was employed—i.e. in which interfacial acoustic mismatch was smaller—revealed period-independent κ behaviour, saturating to the corresponding alloy value. This suggested that the dominant mechanism in slightly mismatched samples was alloying scattering while in the former set it was interfacial scattering derived from acoustic mismatch.

Later, Samarelli *et al* presented the full thermoelectric characterization of modulation-doped p-type Ge/Si_{1-x}Ge_x SLs, demonstrating higher ZT values than corresponding bulk alloys (0.14 at 300 K, with respect to ~0.01 of bulk), which was attained by a reduction of thermal conductivity of by a factor of 4–10 [122]. Recently, Ferrando-Villalba *et al* demonstrated that κ in SLs in the cross-plane direction could be further reduced by employing compositional gradients in the alloy layers of Si/Si_{1-x}Ge_x SLs [123].

Other silicon-based superlattice structures different than Si/Ge ones were reported in recent works. Li *et al* fabricated and measured the in-plane thermal conductivity of roll-like Si/SiO_x SLs (figure 15(a)) [129]. The novel fabrication technique consisted in releasing a stressed strip of Si-on-Ge thin film which could be compressed in order to form planar SL structures. A subsequent etching process from bottom released spontaneously-rolling, partially-oxidized membranes. Savelli *et al* fabricated and thermoelectrically characterized Si_{1-x}Ge_x/TiSi₂ quantum dot SLs (figure 15(b)) [124]. The results revealed that introduction of quantum dots allowed increasing the in-plane power factor with respect to only segmented Si_{1-x}Ge_x polycrystalline samples, while maintaining the cross-plane thermal conductivity.

2.4. Phononic structures

Phononic structures are nano- or micro-structures designed with periodic acoustic-mismatched features which repeat with a period of the order of the acoustic wavelength. The objective of a phononic structure is to alter the phonon dispersion relation by means of coherent effects based in Bragg and Mie resonant wave-interference [130]. The modification of the phonon dispersion leads to a reduction of the group velocity and density of states of the modes—even leading to the formation of acoustical bandgaps—and thus to a reduction of κ . Thin films with patterns of holes, nanowires with periodic diameter modulations and SLs in the cross-plane direction

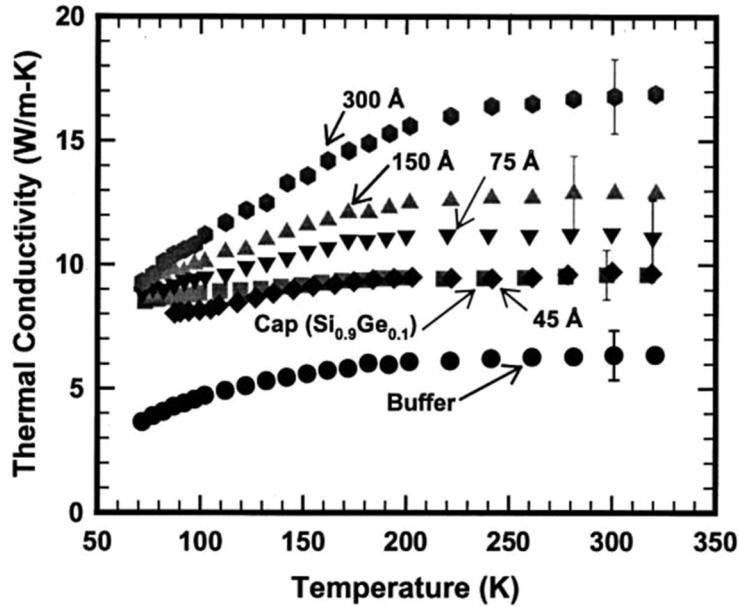


Figure 14. Thermal conductivity of Si/Si_{0.7}Ge_{0.3} SLs as a function of the temperature, and the superlattice period, indicated within plot. The ratio of Si to Si_{0.7}Ge_{0.3} is 2:1. ‘Cap’ is a thick film of composition Si_{0.9}Ge_{0.1}. ‘Buffer’ is a 1 μm film of ‘Cap’ in series with a 1 μm superlattice. Reprinted with permission from [116]. Copyright (2002), AIP Publishing LLC.

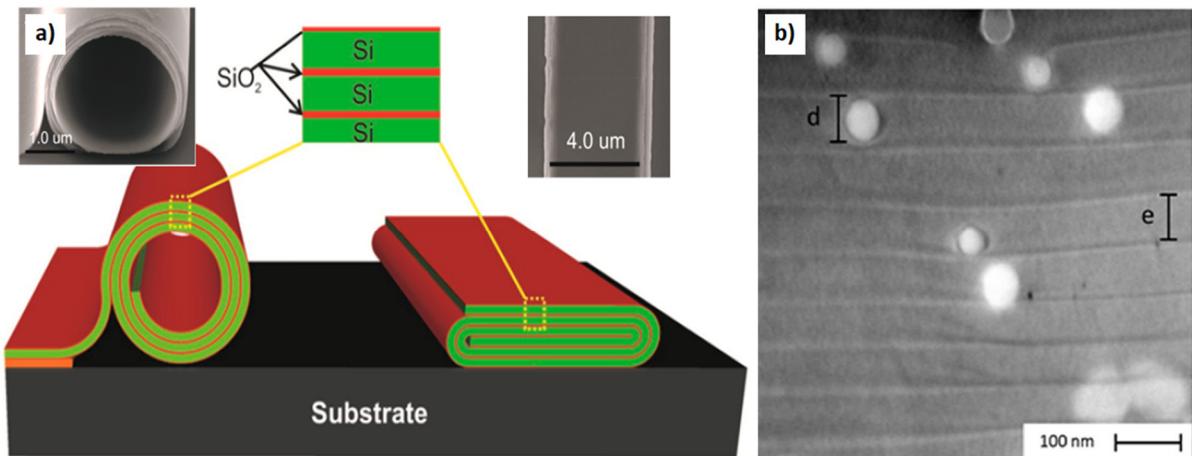


Figure 15. (a) Roll-like Si/SiO_x superlattice fabrication scheme (main frame) and SEM images (insets). The structure at left is presented as obtained after Si film release, oxidation and self-rolling, while a right in has been compressed to a flat superlattice structure. Reprinted with permission from [129]. Copyright (2017) American Chemical Society. (b) Si_{1-x}Ge_x/TiSi₂ quantum dot superlattice. Reproduced from [124]. © IOP Publishing Ltd. All rights reserved. The discontinuities between the layers are Si_{1-x}Ge_x crystal boundaries—due to alternation of precursor deposition necessary to form the TiSi₂ self-assembled quantum dots—bright in the figure.

can indeed be considered as phononic crystals if the repetition periods are regular and the spacing is properly chosen.

In the work of Yu *et al*, thermal conductivities of silicon thin films, nanowire networks and membranes with highly ordered holes (a phononic crystal, PnC) were measured and compared (figures 16(a) and (b)) [131]. Despite having a lower surface-to-volume relation, the PnC showed a lower κ than the nanowire network structures, indicating that phononic effects were indeed taking place. Later, similar results were obtained by Hopkins *et al* and Haras *et al* [132, 133]. More recently, Maire and Nomura investigated this effect in ‘fishbone-type’ modulated Si nanowires [134]. They measured thermal conductivity in smooth and diameter modulated

Si NWs of equivalent diameter (figures 16(c) and (d)) and the results confirmed the presence of a coherent effect in fishbone-like ones.

The fabrication of phononic structures is rather novel and diverse, but it generally implies features and pitches in the nanoscale generated with high spatial precision and often currently exclusive technologies. Therefore, with the exception of SLs, silicon nanolithography methods are employed, so far non-scalable for practical integration in TEG devices. Probably because of this and the relative novelty of the concept, a full thermoelectric characterization and device integration has not been reported for phononic semiconductor structures.

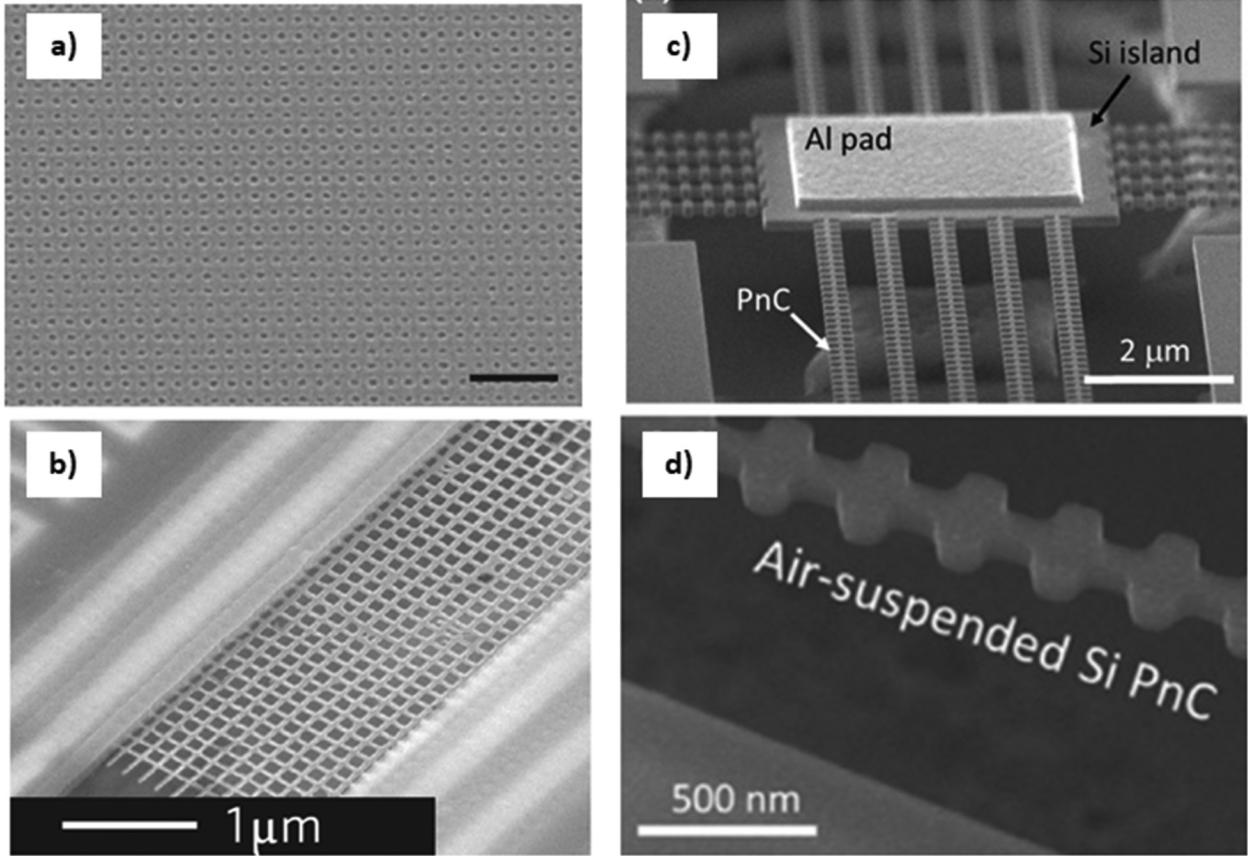


Figure 16. (a), (b) Phononic membrane (a) and nanowire network (b) employed by Yu *et al* for proving phononic effects in silicon micro-devices. [131] © Macmillan Publishers Limited. All rights reserved. With permission of Springer. (c), (d) Microstructure (c) featuring fishbone-like (d) phononic nanowire structures, from the work of Nomura and Maire. [134] (2015) © 2014 The Minerals, Metals & Materials Society. With permission of Springer.

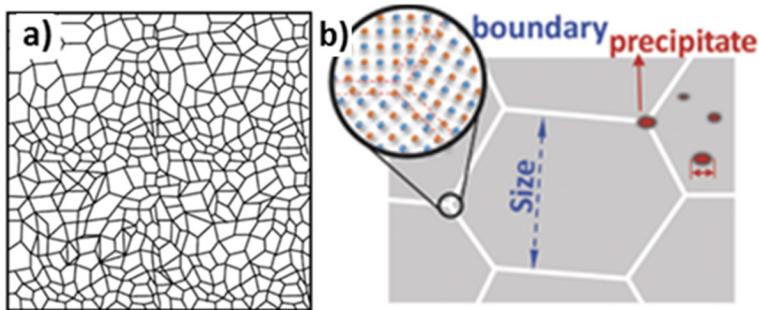


Figure 17. Strategies for bulk thermoelectric nanocomposites: (a) nanobulk material (b) nanocomposite. Formed by precipitation of nano-inclusions within grains/boundaries. The circular inset shows a grain boundary where three grains of the same composition—but different orientation—meet. [135] John Wiley & Sons. © 2018 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim.

2.5. Nanostructured bulk

A nano-bulk material is a poly-crystalline bulk with grains of sizes in the order of ~100 nm—with the same composition and phase in all the grains (figure 4(e)). A nanocomposite is an agglomeration of nano-grains—i.e. with crystal domain sizes below ~100 nm—with two or more different phases (figure 4(e)). If a nanocomposite is formed by a dominant phase—which might be or not polycrystalline and/or nano-structured—with few particles dispersed within, then these are termed nano-inclusions (figure 3(e)). A frequent type of nanocomposite is that obtained by precipitation of species at

grain boundaries of a nanostructured bulk material, as illustrated in figure 17(b).

The primary benefit from nanostructures, a reduced κ_L , does not require an atomically perfect interface or an exact geometry. All that is required is a material with a high density of interfaces, which can be present in any geometry [136]. This can be attained by employing nanostructured bulk—nanobulk and nanocomposites—which retain a high density of interfaces but do not have a special geometry or structure. As a consequence, a significant simplification of the fabrication process is attained, enabling production of the material in large quantities [137].

In order to produce nanostructured bulk thermoelectric materials, precursor nanoparticles are prepared first and then assembled into dense bulk solids. The nanoparticles can be produced by many methods, such as hydrothermal synthesis, wet chemical methods (CM), gas phase synthesis—e.g. plasma enhanced chemical vapour deposition (PECVD)—and ball-milling (BM). The particles are assembled into a dense solid using various methods referred as bottom-up e.g. plasma activated sintering (PAS), cold-pressing, direct current assisted sintering (DCS), hot-pressing (HP) and extrusion. Any combination of nanoparticle preparation and bottom-up assembly method can be employed. Many works reviewed the fabrication, properties and application of nanostructured bulk thermoelectric materials [138–140]. For the case of silicon, a comprehensive review is offered by Schierning [11].

Traditionally, the control of the chemical composition, doping and crystallinity has proven to be effective for the reduction of κ in silicon–germanium alloys, by promoting phonon scattering at Ge atoms—serving as point defects—and grain boundaries [63, 135, 141]. Electron–phonon scattering can also play an extremely important role in the decrease of κ in silicon-based thermoelectric materials. For instance, it has been shown that in fine-grained, heavily doped bulk silicon with optimized carrier concentration, electron–phonon scattering contributes to a reducing κ_L a 36% at room temperature [142, 143]. However, maintaining effective doping—i.e. high carrier concentration—after operation at high temperatures and controlling the state of grain boundaries—which can be easily oxidized—remains a challenge. The possibility to overcome these issues was recently demonstrated with gas phase synthesis based nanobulk fabrication techniques which were presented as low-cost and highly scalable [144–147].

Regarding the implementation of size effects in bulk $\text{Si}_{1-x}\text{Ge}_x$, early works reported that in micro-bulk—with grains down to $\sim 1 \mu\text{m}$ —the degradation of κ came with a proportional degradation in $S^2\sigma$ due to increased electron scattering at grain boundaries [25]. However, recent studies employing lower grain sizes below 100 nm reported an effective increase of ZT in both p and n-type alloys [148, 149]. The introduction of gallium-phosphide (GaP) micro- and nanoparticles within $\text{Si}_{1-x}\text{Ge}_x$ followed by a thermal annealing proved to enhance the thermoelectric figure of merit by 18% of the n-type alloy [25]. This improvement was attributed to the presence of highly soluble, electrically active Ga-O-P donor complexes, which allow to increase the doping level over the solubility limit of P in $\text{Si}_{1-x}\text{Ge}_x$ —otherwise underdoped for optimal thermoelectric application [25, 150].

The scattering of high-wavelength phonons—which are impervious to alloy-induced scattering—can be significantly enhanced by introducing nanoinclusions in the material, reducing κ [151]. Conveniently, σ is not significantly affected as the electron scattering by ionized impurities or acoustic phonons is still dominant. A large atomic mass mismatch can be used to scatter phonons effectively. At the same time, a similar work function and a small band offset are required to scatter electrons as weakly as possible [152]. It has recently been shown that the addition of silicide nanoinclusions to

$\text{Si}_{1-x}\text{Ge}_x$ maintained or increased the power factor while further reduced the thermal conductivity compared to the nanostructured single-phase alloys [18, 153, 154]. Moreover, a dispersion of SiC nanoparticles could significantly enhance the ZT of the $\text{Si}_{1-x}\text{Ge}_x/\text{SiC}$ nanocomposites [155].

Instead of attempting to reduce κ , other strategies focus on improving the thermoelectric power factor ($P_F = S^2\sigma$) employing diverse nanostructured bulk materials [139]. In the energy filtering approach, energy barriers are used to block the low-energy electrons and therefore, increase the average heat transported per carrier, raising S . Either nanoparticles or grain boundary interfaces play the role of energy filters [156]. Energy filtering for enhanced thermoelectric performances of nanocrystalline silicon and silicon alloys was reviewed by Narducci *et al* [157]. Another strategy is to increase the electron mobility—and thus σ —via modulation doping. This approach consists in spatially separating the charge carriers from their originating impurity atoms. This way excessive ionized impurity scattering—the controlling charge carrier scattering mechanism in thermoelectric materials—is avoided, allowing to increase σ [139]. A 40% enhancement of P_F was demonstrated for p-type modulation-doped $(\text{Si}_{80}\text{Ge}_{20})_{70}(\text{Si}_{100}\text{B}_5)$ when compared to uniformly alloyed nano-bulk of similar composition [20, 158].

Silicide nanocomposite engineering is another interesting direction that has been recently pursued. High ZTs in the moderate-to-high temperature range comparable to some of the good thermoelectric telluride materials has been demonstrated. The topic of silicides for thermoelectric applications was recently reviewed by Nozariasbmarz *et al* [18]. Under this context, HMS constitute a family of intermetallic silicon compounds which are regarded as potential, p-type thermoelectric materials efficient in the intermediate temperature range. Moreover, they are the most promising p-type compatible counterpart to the existing n-type Mg₂Si-based thermoelectric material, allowing the completion of two-leg efficient TEG made of earth-abundant, non-toxic elements [159, 160].

Some of the typical silicon-based thermoelectric nanostructured materials and their thermoelectric properties are summarized in table 1.

2.6. Nanoporous bulk

Porosity with features in the order of $\sim 100 \text{ nm}$ enhances the phonon boundary scattering, reducing κ [166]. The formation and application of porous silicon is reviewed in [167].

κ of nanoporous bulk Si generally decreases with increasing void fraction (f_v) and decreasing pore size [168–177], approaching the amorphous limit (0.2 to $0.5 \text{ W m}^{-1} \cdot \text{K}^{-1}$) at high f_v [168–170]. However, structures with high nanoporosity might have adverse electronic properties since interfaces yield enhanced charge carrier boundary scattering and provide traps for charge carriers. The reduction of the carrier mobility—and thus σ —presently limits the increase in thermoelectric efficiency [178]. However, thermoelectric characterization of both n- and p-doped porous silicon showed that by tailoring porosity is possible to reduce κ without

Table 1. Thermoelectric properties of some typical silicon-based nanocomposites.

Si-based nanostructured material		p/n	ZT ^a	κ @ max. ZT (W m ⁻¹ k ⁻¹) ^{a,b}	Methods ^{c,d}	Ref. and year
Pure Si	SiP _x	n	0.7 at 1275 K	12	BM (1 h) + HP (>1000 °C)	[13] 2009
	Si ₉₈ B ₁	p	0.32 at 1000 K	7.5	PECVD + DCS (1125 °C)	[145] 2013
	Si P _{0.5} /SiO _x	n	0.58 at 1125 K	5	PECVD + PAS	[161] 2015
	Si ₉₄ P ₆	n	0.6 at 1125 K	13.8	BM (4 h) + PAS (>1000 °C)	[142] 2016
Si _{1-x} Ge _x alloys	Si _{63.5} Ge _{36.5} P _x	n	0.128 (0.0937) at RT	3.82 (5.07)	BM + HP	[162] 1981
	Si ₈₀ Ge ₂₀ P ₂	n	1.3 (0.93) at 1175 K	2.5 (4.6)	BM + HP (1000 °C–1200 °C)	[149] 2008
	Si ₈₀ Ge ₂₀ B _x	p	0.95 (0.5) at 1175 K	2.5 (5.0)	BM (10–60 h) + HP (950 °C–1200 °C)	[148] 2008
	Si ₉₅ Ge ₅ P _{2.5}	n	0.95 (0.5) at 1175 K	5 (10)	BM + HP	[16] 2009
	Si ₉₇ Ge ₃ P ₃	n	0.6 at 1050 K	9	Arc melting + PAS	[163] 2014
	Si ₈₈ Ge ₁₂ P ₂	n	0.9 at 1130 K	3.1	BM (65 h) + HP (1100 °C)	[153] 2016
	Si ₈₀ Ge ₂₀ P ₂ –SiC _{0.23}	n	1.7 at 1175 K	1.9	BM + PAS	[155] 2017
Silicides	Mg ₂ Si	n	0.6 at 938 K	3.1	BM (23 h) + HP (800 °C)	[164]
	Mg ₆₇ Si ₃₃ Bi ₂	n				2014
	FeSi ₂	n	0.2 at 938 K	3.7	BM (50 h) + HP (1100 °C)	[153]
	Fe ₃₄ Si ₆₆ Cu ₁	n				2016
	SiGe-FeSi ₂	n	1.2 at 1073 K	2.8	BM (50 h) + HP (1000 °C)	[154]
	(Si ₈₈ Ge ₁₂ P ₂) _{92.5} –(Fe ₃₄ Si ₆₆ Cu ₁) ₅ –Ag ₂₅	n				2016
	SiGe-Mg ₂ Si	n	1.3 at 1225 K	2.7	BM (20 h) + HP (1250 °C)	[153]
	(Si ₈₈ Ge ₁₂ P ₂) ₉₅ –(Mg ₆₇ Si ₃₃ Bi ₂) _{0.05}	n				2016
	Mg ₂ Si	n	1.1 (0.3) at 773 K	2.5	BM + HP (700 °C 2 h)	[165]
	Mg ₂₀₀ Si _{39.25} Sn ₆₀ Sb _{0.75}	p				2008
	Al-doped MnSi _{1.73}	p	0.86 at 800 K	1.5	Melt spinning + PAS	[159] 2018

^a Data in parentheses are the values of single crystals or of nanocomposites without addition.

^b At room temperature (RT).

^c BM: ball-milling; HS: hydrothermal synthesis; CM: chemical method; MS: melting spinning; HP: hot-pressing; PAS: plasma activated sintering; PECVD: plasma enhanced chemical vapor deposition; DCS: direct current assisted sintering.

^d Experimental details are listed in parentheses.

excessively compromising σ , i.e. increasing ZT with respect to bulk [175, 178].

As opposed to individual Si NWs, arrays of nano-porous Si NWs experiment the combined effects on κ of NW morphology (diameter, length and roughness), internal porosity (that associated to nano-recessions within the NWs) and external porosity (that associated to the void spacing between NWs conforming the array) [179]. Internal porosity allows the phonon propagation to span the range from ballistic to diffusive thermal transport, greatly decreasing κ and increasing ZT value [179, 180].

Si thin films densely pierced with ~100 nm holes have also shown competitive thermoelectric properties. For instance, high-density nanoscopic holes have been created in thin, single-crystalline silicon films, leading to good mechanical

strength and reproducible low κ while keeping sufficient electrical quality [177], shown in figure 18. Similar results were achieved in nanomesh Si structures [131], in which the holes presented an ordered pattern. Nanomesh devices exhibit a κ lower than that of nanowire-array devices by a factor of two even at smaller surface-to-volume ratios. Numerical studies indicated that in nano-pierced silicon thin films not only f_v but also the film thickness has significant effect on κ . As f_v increases and film thickness κ decreases [181].

In nanoporous Si_{1-x}Ge_x, the thermal conduction is largely determined by alloy scattering and thus the dependence of κ on porosity features is much weaker than in the case of nanoporous Si [182]. Recently, large-area Si_{1-x}Ge_x nanomeshes were obtained by DC sputtering on highly ordered porous alumina matrices, constituting a more scalable approach than

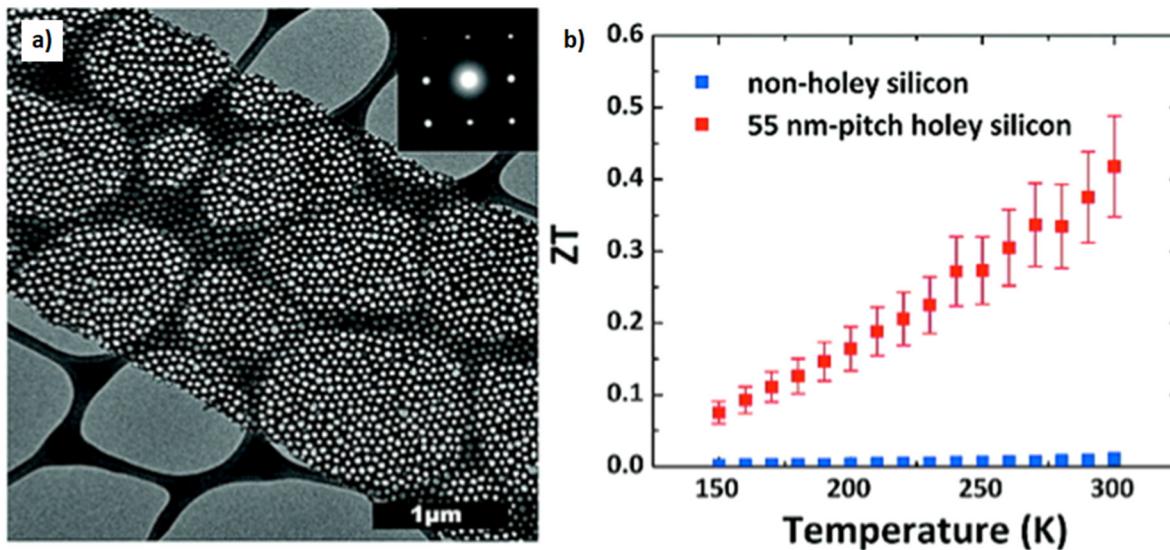


Figure 18. (a) SEM image of thin silicon membranes that have been decorated with high density of nanoscopic holes. Reprinted with permission from [177]. Copyright (2010) American Chemical Society. By reducing the pitch of the hexagonal holey pattern down to 55 nm with 35% porosity, the thermal conductivity is consistently reduced by 2 orders of magnitude and approaches the amorphous limit. (b) ZT versus T of the pierced thin film shown in (a), extracted from [177]. With a ZT value of ~ 0.4 at room temperature, the thermoelectric performance is comparable with the best value recorded in silicon nanowire system.

those employed in other works based in nanolithography. In this case, κ decreased with the diameter of the pores, down to $0.55 \text{ W m}^{-1} \cdot \text{K}^{-1}$, below the amorphous-limit [183].

3. Silicon-based nanostructures in thermoelectric generator devices

Table 2 shows the state of the art of existing μ TEG devices which use silicon-based nanostructured materials. Each colour indicates a type of structure: nanowires, SLs, thin films, nanobulk and bulk—included for comparison purposes. Discontinuous lines join different versions of the same device, presented in different works of the same groups.

By looking at table 2, several general conclusions can be drawn. First, this list is substantially shorter than those found in other reviews where macroscopic TEGs are listed. This can be attributed to the difficulty associated to the fabrication and integration of nanostructures of conventional thermoelectric materials in devices. Actually, among the 19 works reported, only the one of Kessler *et al* refers to a macroscopic device, which presents the traditional modular architecture, shown in figure 19(e). To date, there has been no technological solution able to make compatible nanobulk processing with microelectronic integration. While this might take away some advantages related to mass fabrication and processing cost, it allows the generation of power in the W scale, enabling the exploration of other applications than energy harvesting, for which so far μ TEG devices constitute the best solution. The μ TEG devices compiled herein implement diverse nanostructured materials in both planar and vertical architectures (figures 20(a)–(d)).

It is also worth mentioning that there is vast majority of pure silicon nanostructure based μ TEGs, surely because of the easy processing of this material, the immense knowledge already present around it and its high compatibility with

microtechnology—even with CMOS, as demonstrated for four of the devices [44, 190–192]—which is of great interest for enabling massive fabrication and implementation of these devices for energy harvesting applications. Moreover, purely silicon-based device concepts enable defining nanostructures directly on the device layers as in using top-down etch-based methods or in membrane thinning for ultra-thin film generation.

Apart from pure Si structures, an effort has also been done towards incorporation of silicon–germanium alloys in five works [27, 150, 185, 189, 190]—representing only a fourth of the total number of devices—because of the already established good thermoelectric properties in this material, so far attained by CVD on top of Si wafer based devices. In contrast, no silicide nanostructure comprising devices were found in the literature. This might be related to the fact that most works concerning silicide nanostructures for thermoelectric applications report on the nanobulk shape, rather than nanowire or thin films, which as discussed below account for the best nanostructured forms for integration in microdevices.

On the other hand, low dimensional structures (nanowires and thin films) clearly predominate over 3D structures (SLs, nanobulk and absent nanoporous bulk). This is because these are necessarily fabricated by means of microtechnology techniques and thus they can easily be further integrated in microfabricated devices by introducing additional steps in the workflow. While this should be applied as well to SLs—which one would expect to have the same scalability and integrability as thin films—so far there is only one work reporting on a superlattice with proven capacity of thermoelectric power generation [189].

Finally, it is hard to assess the performance of these devices as these works report data in non-comparable figures, mostly in power density ($\mu\text{W generated cm}^{-2}$ of the total device

Table 2. Silicon nanostructure based μ TEG and TEG devices^a.

Authors	Year	p/n	Material	Struct. ^b	Cryst. ^c	Dimension ^d (nm) ^d	Fabrication	TEG size (mm ²)	Performance	Conditions ^e
Li <i>et al</i> [184]	2012	p/n	Si	NW	SC	80	Nanolithography (DUV + sacrificial ox.) (CMOS) ^f	25	1.9 μ W cm ⁻²	Forced $\Delta T = 2.1$ K
Xu <i>et al</i> [185]	2012	p	Si _{0.8} Ge _{0.2}	NW	SC	150	CVD (for Si–Ge thick film) + MACE	225	0.0005 μ W cm ⁻²	Forced $\Delta T = 5.1$ K
Xu and Fobelets [49]	2014	p	Si	NW	SC	150	MACE + SOD (p-type doping)	400	0.16 μ W cm ⁻²	Forced $\Delta T = 8.1$ K
Curtin <i>et al</i> [28]	2012	n	Si	NW	SC	85	Nanolithography (laser interference)	0.0025	1200/000 μ W cm ⁻²	Forced $\Delta T = 56.1$ K
Penelli <i>et al</i> [87]	2013	n	Si	NW	SC	60	Contact doping (P) + nanolithography (sacrificial ox.)	2.4	0.7–1.2 mV	Forced $\Delta T = 3$ –5 K
Norris [186]	2015	p	Si	NW	SC/Poly	17–1600	PECVD-VLS	200	2.4 nW cm ⁻²	Forced $\Delta T = 70$ K
Roncaglia <i>et al</i> [187]	2016	p/n	Si	NW	Poly	70–100	Nanolithography + CVD	100	500 mV	Harvesting @ 50 °C
Choi <i>et al</i> [188]	2017	p/n	Si	NW	SC	70	Nanolithography + ion implantation	—	1.3 nW	Forced $\Delta T = 52.1$ K
Hashimoto <i>et al</i> [39]	2017	n	Si	NW	SC	46 × 36	Nanolithography (EBL + sacrificial ox.) + ion implantation	—	0.05 mV	—
Dávila <i>et al</i> [32]	2012	p	Si	NW	SC	100	CVD-VLS	1.5	960 μ W cm ⁻²	Forced $\Delta T = 300.1$ K
Gadea <i>et al</i> [27]	2017	p	Si	NW	SC	110	CVD-VLS	1.5	4.4 μ W cm ⁻²	Harvesting @ 300 °C ($\Delta T = 8.7$ K)
Gadea <i>et al</i> [27]	2017	p	Si _{0.7} Ge _{0.3}	NW	SC	68	CVD-VLS	1.5	4.9 μ W cm ⁻²	Harvesting @ 300 °C ($\Delta T = 8.7$ K)
Samarelli [189]	2014	p/n	Si _{1-x} Ge _x	SL	SC	~30	PECVD	—	13 nW cm ⁻²	Forced $\Delta T = 20$ K
Schaevitz <i>et al</i> [150]	2001	p/n	Si _{0.8} Ge _{0.2}	TF	Poly	—	CVD + ion implantation	—	55 μ W	Combusting H ₂ @ 500 °C
Strasser <i>et al</i> [190]	2003	p/n	Si	TF	Poly	400	CVD (CMOS) ^f	100	4 μ W cm ⁻²	Forced $\Delta T = 8.2$ K
Strasser <i>et al</i> [190]	2003	p/n	Si _{0.7} Ge _{0.3}	TF	Poly	400	CVD (CMOS) ^f	100	2.5 μ W cm ⁻²	Forced $\Delta T = 9.8.2$ K
Xie <i>et al</i> [191]	2010	p/n	Si	TF	Poly	700	CVD (CMOS) ^f	100	1.3 μ W cm ⁻²	Harvesting (forced convection, $\Delta T = 5$)
Perez-Marín [192]	2014	p/n	Si	TF	SC	100	Sacrificial oxidation (Si thinning) (CMOS) ^f	100	4.5 μ W cm ⁻²	Harvesting (forced convection, $\Delta T = 5.5$)
Kessler (TEG) [193]	2014	p/n	Si	NB	NB	40–80	Microwave-plasma CVD + sintering	~4000–5000	1 W	Forced $\Delta T = 300$ K
Glosch <i>et al</i> [194]	1999	p	Si	Bulk	SC	~ μ m	Optical lithography + DRIE	17	5 μ W cm ⁻²	Forced $\Delta T = 20$ K

^a Except in the case of Kessler *et al* (indicated) all of them are μ TEG, rather than TEG devices.

^b Structure. May be: NW (nanowire), TF (thin film), SL (superlattice), NB (nanobulk) and bulk.

^c Crystal form. May be: SC (single crystal), Poly (polycrystalline) and NB (nanobulk).

^d Dimension, refers to average diameter in nanowires, period in SLs, thickness in thin films and crystallite size in nanobulk and bulk.

^e Conditions at which the performance measurement was carried out and ΔT applied to the device. Harvesting means naturally generating power on top of hot surfaces (by natural convection if not indicated). Forced means temperature ΔT generated by means of micro-heaters.

^f CMOS-compatible route, according to the authors.

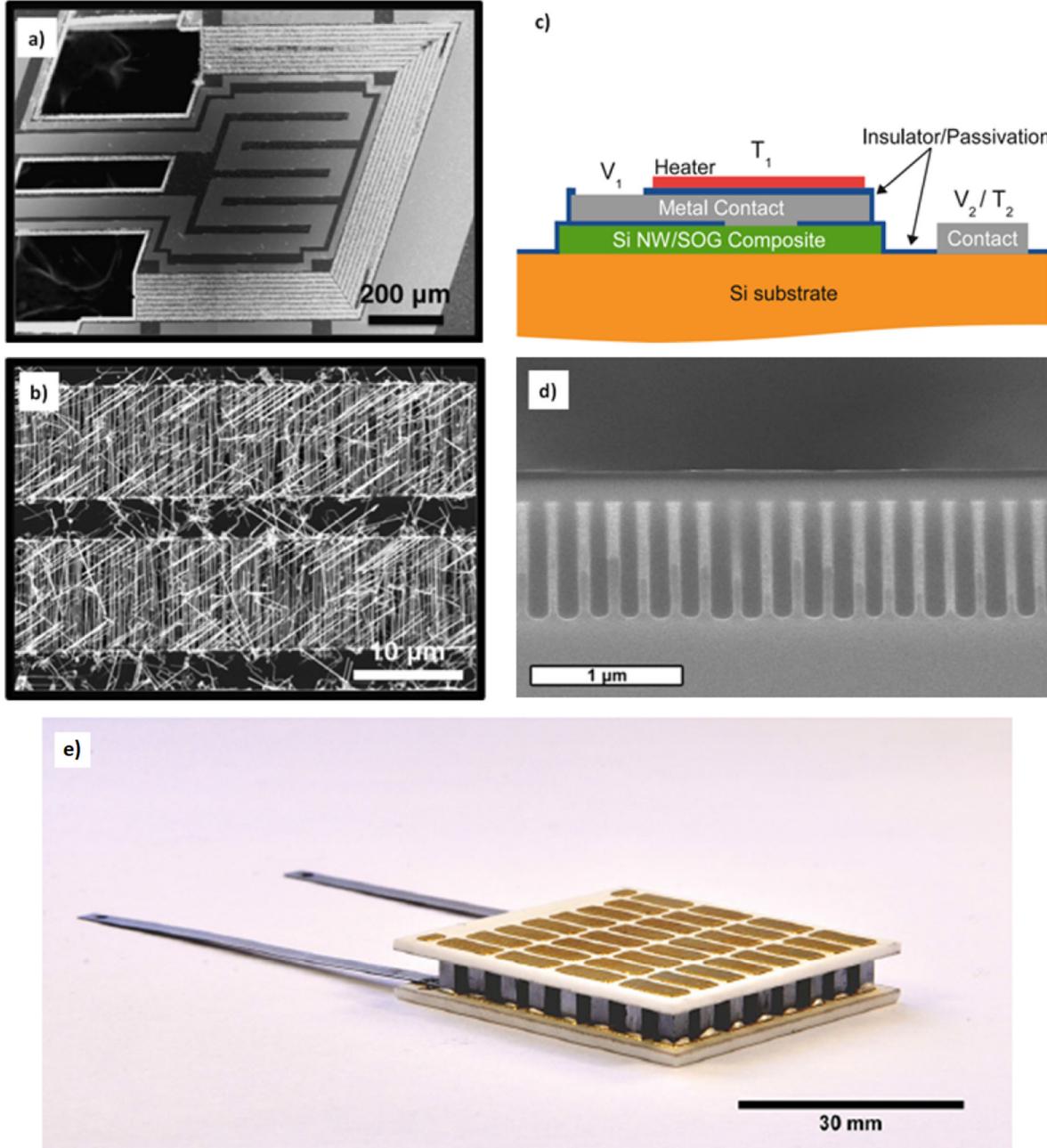


Figure 19. (a), (b) SEM top-views of the Si NW based device devised by Davila *et al* with planar architecture. Reprinted from [32], Copyright (2012), with permission from Elsevier. Bottom-up aligned nanowires monolithically integrated in microtrenches are magnified in (b). (c), (d) The Si NW based device of Curtin *et al*, comprising vertically defined top-down nanowires. [28] (2012) © TMS 2012. With permission of Springer. (c) A schematic cross section of the device, with the nanowire array coloured in green. An actual SEM cross section of the array of nanowires embedded in spin-on-glass (SOG) is shown in (d). (e) Silicon nanobulk based modular thermoelectric generator. [193] (2014) © TMS 2014. With permission of Springer.

surface) at a forced ΔT , but also in the total μW of mV generated without information on area or temperature differences employed. The power density and also the power density divided by ΔT^2 [2] seem to be the preferred magnitudes of merit, possibly because they are the standard for comparison of macroscopic commercial modules. This may yield misleading conclusions regarding micro-device efficiency in real operation environments if the gradient is forced—as it usually is—by means of a heater, as discussed in [1]. However, this value may still serve to provide insight on the electronic

efficiency of the device along with its integrated nanostructures, if the thickness of the device is taken into consideration. Still in general lines, it can be stated that the power produced by these devices is in some cases enough to feed low power electronics. Together with the fact that most of these devices were obtained by means of mainstream microfabrication techniques, this renders them excellent candidates for energy harvesting applications. Further research towards their coupling with microdevices and MEMS based sensors is likely to be seen in the following years.

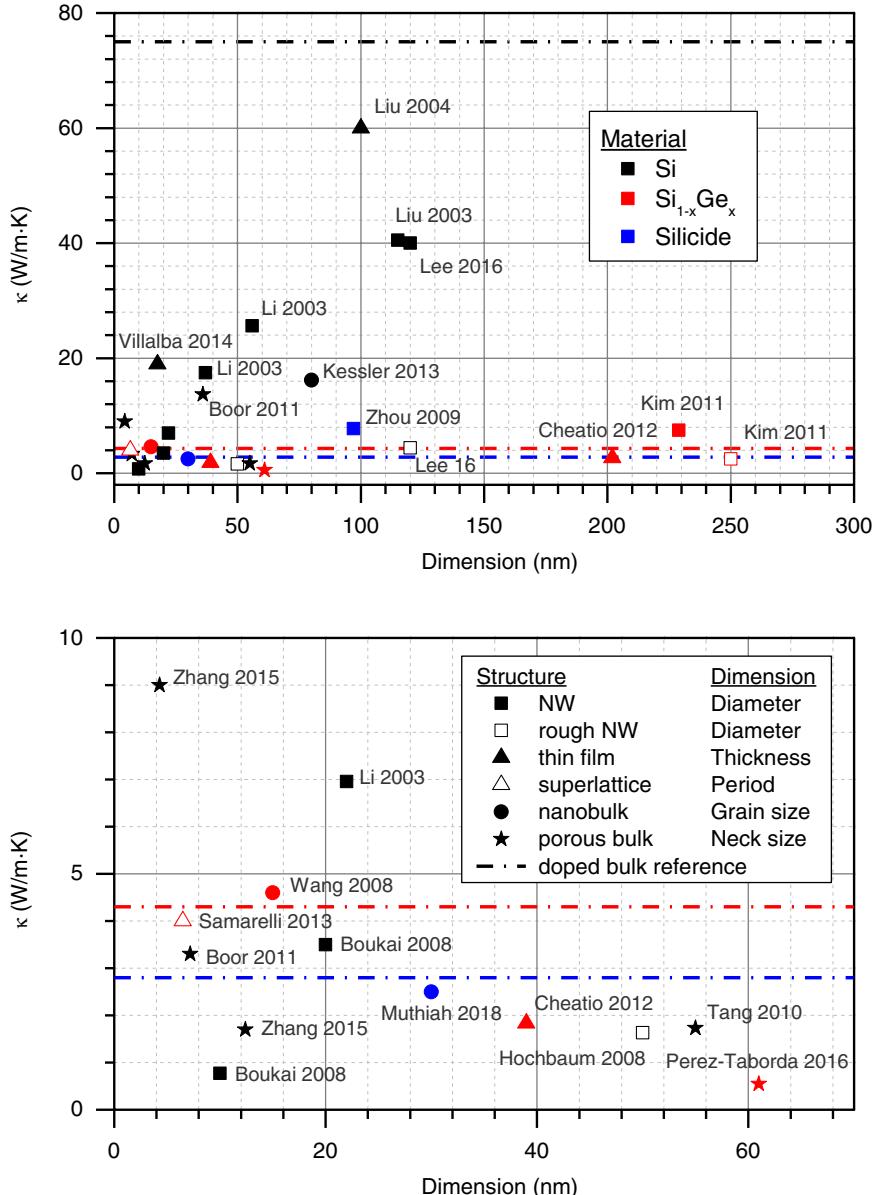


Figure 20. Thermal conductivity (κ) of nanostructured silicon-based thermoelectric materials as a function of their characteristic dimension. (a) All the data points and (b) an extract of the samples with $\kappa < 10 \text{ W m}^{-1} \cdot \text{K}^{-1}$ and $d < 70 \text{ nm}$. The material composition is indicated by the colour (legend in (a)) and the nanostructure is indicated by the symbol (legend in (b)), along with the specific magnitude corresponding to the dimension for each substructure type. Labels indicate the first author and year of the works from which the data was extracted [53, 56, 70, 72, 77, 104, 108, 112, 113, 122, 145, 149, 172, 177, 180, 183, 159]. Dot-dash lines corresponding to heavily doped bulk Si, $\text{Si}_{0.8}\text{Ge}_{0.2}$ and HMS (MnSi_x) are included for comparison purposes [14, 195, 196].

4. Overview and future perspectives

Figure 20 shows the thermal conductivity of some silicon-based nanostructured materials with respect to their characteristic dimension, e.g. diameter for nanowires or grain size for nanobulk. Data from representative works was chosen, as well as the lowest values of κ attained for each kind of structure and for bulk (for comparison purposes). Figure 21 shows the maximum ZT obtained by different silicon-based nanostructured materials.

Research in silicon-based nanostructured materials keeps pushing towards higher performances by exploiting all the very diverse micro-nanofabrication tools available. Pure silicon nanostructured materials have demonstrated to possess

lower κ and higher ZT than corresponding bulk materials. Fabrication of nanostructures with even smaller feature sizes is likely to further increase in ZT , approaching silicon-based nanomaterials to real thermoelectric applications. In contrast, the benefits of nanostructuration in $\text{Si}_{1-x}\text{Ge}_x$ alloys are still not rigorously demonstrated. Despite this, the reduced amounts of Ge required for achieving high ZT $\text{Si}_{1-x}\text{Ge}_x$ nanostructures can pave the path for the implementation of these alloys in commercial applications, even considering the high cost and scarcity. While the low dimensionality effect has been widely studied in silicon and silicon–germanium thin films and nanowires, the thermoelectric behaviour of these structures was rather unexplored in silicides.

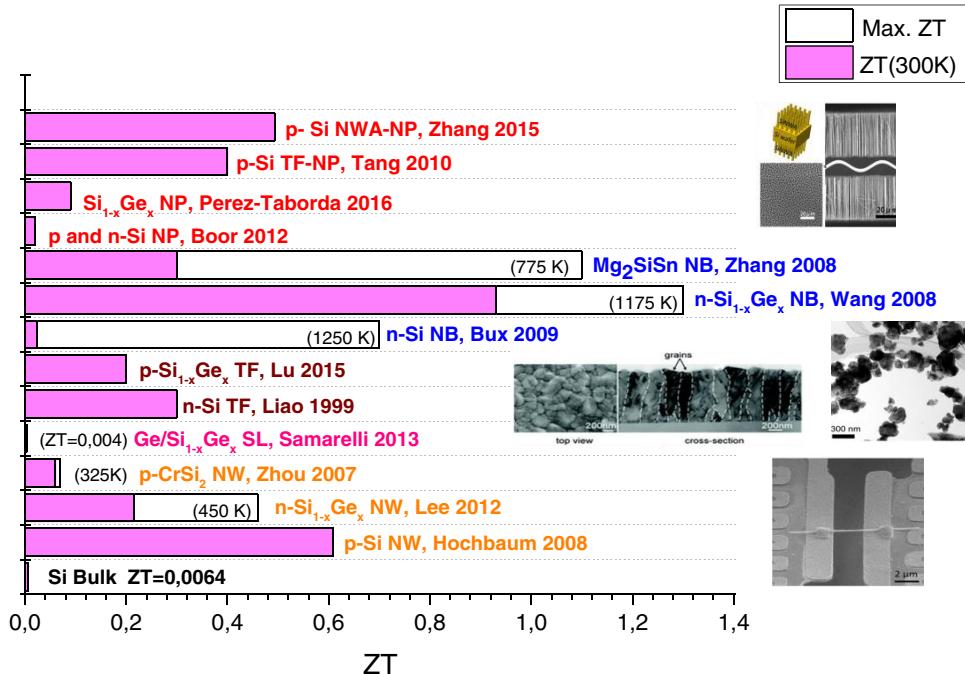


Figure 21. Figure of merit ZT of state of the art silicon-based nanostructures. From top to bottom, data extracted from [13, 104, 122, 149, 165, 177, 178, 180, 183, 197, 198]; and [67], and bulk [70]. Label indicates composition, structure, first author and year of the work. Nanostructure abbreviations stand for: nanoporous bulk (NP), nanowire array-nanoporous bulk (NWA-NPB), nanobulk (NB), thin film (TF), superlattice (SL), nanowire (NW). Representative images reproduced with permission included at right: cross-section and top-view SEM images of the porous Si NW arrays. (Top) Reprinted from [180], Copyright (2015), with permission from Elsevier. HRTEM image of ball-milled $\text{Si}_{1-x}\text{Ge}_x$ nanobulk. (Mid right) Reprinted with permission from [149]. Copyright (2018), AIP Publishing LLC. SEM image of the top surface morphology and TEM image of the cross-sectional structure of a polycrystalline $\text{Si}_{1-x}\text{Ge}_x$ thin film. Some grain boundaries are sketched using dashed lines. (Mid left) Reproduced from [197] with permission of The Royal Society of Chemistry. SEM image of a Pt-bonded, MACE-grown rough Si nanowire. (Bottom) [70] (2008) © 2007 Nature Publishing Group. With permission of Springer.

The range of power densities supplied by silicon-based μTEGs of $10\text{--}100 \mu\text{W cm}^{-2}$ cover the needs for energy harvesting applications in which reliability, long-term stable operation at high temperatures and autonomy are of utmost importance. Moreover, their easy microfabrication approach, enabling co-integration with other small electronics or MEMS devices makes them even more suitable for this purpose. This integrability factor is further boosted in the case of total CMOS compatible process, which was attained for some nanowire, thin film and superlattice silicon-based μTEG devices. Thus, silicon-based thermoelectric microfabricated nano-materials do really constitute a feasible solution for implementation autonomous WSN nodes systems powered by the thermoelectric effect, wherever a hot source in the broad range of $600\text{--}1300\text{ K}$ is available, enabled by their high stability and melting point.

More works reporting on silicon-based thermoelectric nano-materials are expected in forthcoming years, centring both in material characterization and device integration, which is already attainable by already existing technologies. As some devices with demonstrated functionality have already been fabricated at a proof-of-concept stage, dense integration and stability at simulated operation conditions studies are of particular interest. Specifically, a deeper research towards growth and integration of silicide nanostructures, and the thermoelectric characterization of their properties is due to be a relevant topic.

Regarding non-integrable nanostructured materials (nanobulk, nanocomposites and nanoporous bulk) a great advance

has been seen in the last few years, with increased ZTs with respect to analogous bulk systems. As these materials are obtained by powder metallurgy and milling approaches, they are more suitable for integration in macroscopic devices with conventional modular architecture. This implies different target applications such as the niche of space in $\text{Si}_{1-x}\text{Ge}_x$ based RTGs, in which a long-term generation of power from a hot nuclear source is required. The paper of nanostructure implementation here is increasing the efficiency per unit mass—making lighter systems—and allowing reduction of the Ge content—diminishing the price. Since stability is of major importance in this application, further studies are encouraged in order to elucidate degradation mechanisms and help to prevent the loss of interfaces/doping during long-term operation of these alloys at high temperature. In parallel, efforts should be devoted to look for integration strategies with the aim of finding suitable application niches for these low-cost abundant materials with fascinating structures.

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References

- [1] Gadea G, Morata Á and Tarancón A 2018 Semiconductor nanowires for thermoelectric generation *SEMI: Nanowires For Energy Applications* vol 98 eds Mokkapati S and Jagadish C (New York: Elsevier)
- [2] Stark I 2015 Micro thermoelectric generators *Micro Energy Harvesting* eds Briand D, Yeatman E and Roundy S ch 12 (Berlin: Wiley) pp 245–69
- [3] Briand D, Yeatman E and Roundy S 2015 *Micro Energy Harvesting* (Berlin: Wiley)
- [4] LeBlanc S, Yee S K, Scullin M L, Dames C and Goodson K E 2014 Material and manufacturing cost considerations for thermoelectrics *Renew. Sustain. Energy Rev.* **32** 313–27
- [5] He J and Tritt T M 2017 Advances in thermoelectric materials research: looking back and moving forward *Science* **357** 6358
- [6] Chen Z-G, Shi X, Zhao L-D and Zou J 2018 High-performance SnSe thermoelectric materials: progress and future challenge *Prog. Mater. Sci.* **97** 283–346
- [7] Yang L, Chen Z-G, Dargusch M S and Zou J 2018 High performance thermoelectric materials: progress and their applications *Adv. Energy Mater.* **8** 1701797
- [8] Gorai P, Stevanović V and Toberer E S 2017 Computationally guided discovery of thermoelectric materials *Nat. Rev. Mater.* **2** 17053
- [9] Nieveld G D 1982 Thermopiles fabricated using silicon planar technology *Sensors Actuators* **3** 179–83
- [10] Van Herwaarden A W 1984 The Seebeck effect in silicon ICs *Sensors Actuators* **6** 245–54
- [11] Schiering G 2014 Silicon nanostructures for thermoelectric devices: a review of the current state of the art *Phys. Status Solidi a* **211** 1235–49
- [12] Rowe D M 1995 *Handbook of Thermoelectrics* vol 16 (New York: CRC Press) pp 1251–6
- [13] Bux S K, Blair R G, Gogna P K, Lee H, Chen G, Dresselhaus M S, Kaner R B and Fleurial J P 2009 Nanostructured bulk silicon as an effective thermoelectric material *Adv. Funct. Mater.* **19** 2445–52
- [14] Ohishi Y, Xie J, Miyazaki Y, Aikebaier Y, Muta H, Kurosaki K, Yamanaka S, Uchida N and Tada T 2015 Thermoelectric properties of heavily boron- and phosphorus-doped silicon *Japan. J. Appl. Phys.* **54** 071301
- [15] Stranz A, Kähler J, Waag A and Peiner E 2013 Thermoelectric properties of high-doped silicon from room temperature to 900 K *J. Electron. Mater.* **42** 2381–7
- [16] Chen G *et al* 2009 Increased phonon scattering by nanograins and point defects in nanostructured silicon with a low concentration of germanium *Phys. Rev. Lett.* **102** 196803
- [17] Pichanusakorn P and Bandaru P 2010 Nanostructured thermoelectrics *Mater. Sci. Eng. R* **67** 19–63
- [18] Nozariabmarz A *et al* 2017 Thermoelectric silicides: a review *Japan. J. Appl. Phys.* **56** 05DA04
- [19] Franssila S 2010 *Introduction to Microfabrication* (Berlin: Wiley) (<https://doi.org/10.1002/9781119990413>)
- [20] Yu B, Zebarjadi M, Wang H H, Lukas K, Wang H H, Wang D, Opeil C, Dresselhaus M, Chen G and Ren Z 2012 Enhancement of thermoelectric properties by modulation-doping in silicon germanium alloy nanocomposites *Nano Lett.* **12** 2077–82
- [21] Amato M, Palummo M, Rurali R and Ossicini S 2014 Silicon–germanium nanowires: chemistry and physics in play, from basic principles to advanced applications *Chem. Rev.* **114** 1371–412
- [22] Schiering G *et al* 2016 Silicon-based nanocomposites for thermoelectric application *Phys. Status Solidi* **213** 497–514
- [23] Schmitt A L, Higgins J M, Szczech J R and Jin S 2010 Synthesis and applications of metal silicide nanowires *J. Mater. Chem.* **20** 223
- [24] Vineis C J, Shakouri A, Majumdar A and Kanatzidis M G 2010 Nanostructured thermoelectrics: big efficiency gains from small features *Adv. Mater.* **22** 3970–80
- [25] Cronin B and Vining J-P F 1993 Silicon–germanium: an overview of recent developments *Proc. 10th Int. Conf. on Thermoelectrics* pp 1–14
- [26] Liu W-D, Chen Z-G and Zou J 2018 Eco-friendly higher manganese silicide thermoelectric materials: progress and future challenges *Adv. Energy Mater.* **1800056**
- [27] Gadea G 2017 Integration of Si/Si–Ge nanostructures in micro-thermoelectric generators *PhD Thesis* University of Barcelona
- [28] Curtin B M, Fang E W and Bowers J E 2012 Highly ordered vertical silicon nanowire array composite thin films for thermoelectric devices *J. Electron. Mater.* **41** 887–94
- [29] Dasgupta N P, Sun J, Liu C, Britzman S, Andrews S C, Lim J, Gao H, Yan R and Yang P 2014 25th anniversary article: semiconductor nanowires—synthesis, characterization, and applications *Adv. Mater.* **26** 2137–83
- [30] Donmez I, Salleras M, Calaza C, Gadea G, Morata A, Tarancón A and Fonseca L 2017 Improved thermal and electrical design for an all-Si thermoelectric micropower source *Proc. SPIE* **10246** 102460Y
- [31] Donmez I, Salleras M, Calaza C, Santos J D, Gadea G, Morata A, Dávila D, Tarancón A and Fonseca L 2015 Interdigitated design of a thermoelectric microgenerator based on silicon nanowire arrays *Proc. SPIE* **9517** 95172C
- [32] Dávila D, Tarancón A, Calaza C, Salleras M, Fernández-Regúlez M, San Paulo A and Fonseca L L 2012 Monolithically integrated thermoelectric energy harvester based on silicon nanowire arrays for powering micro/nanodevices *Nano Energy* **1** 812–9
- [33] Santos J D, Salleras M, Donmez I, Gadea G, Calaza C, Morata A, Tarancón A and Fonseca L 2016 Power response of a planar thermoelectric microgenerator based on silicon nanowires at different convection regimes *Energy Harvest. Syst.* **3** 335–42
- [34] Islam M S, Sharma S, Kamins T I and Williams R S 2004 Ultrahigh-density silicon nanobridges formed between two vertical silicon surfaces *Nanotechnology* **15** L5–8
- [35] Gadea G, Morata Á, Santos J D, Dávila D, Calaza C, Salleras M, Fonseca L and Tarancón A 2015 Towards a full integration of vertically aligned silicon nanowires in MEMS using silane as a precursor *Nanotechnology* **26** 195302
- [36] Li D, Wu Y, Fan R, Yang P and Majumdar A 2003 Thermal conductivity of Si/SiGe superlattice nanowires *Appl. Phys. Lett.* **83** 3186–8
- [37] Wingert M C, Chen Z C Y Y, Dechaumphai E, Moon J, Kim J H, Xiang J and Chen R 2011 Thermal conductivity of Ge and Ge–Si core–shell nanowires in the phonon confinement regime *Nano Lett.* **11** 5507–13
- [38] Huang Z, Geyer N, Werner P, De Boor J and Gösele U 2011 Metal-assisted chemical etching of silicon: a review *Adv. Mater.* **23** 285–308
- [39] Hashimoto S, Asada S, Xu T, Oba S, Himeda Y, Yamato R, Matsukawa T, Matsuki T and Watanabe T 2017 Anomalous Seebeck coefficient observed in silicon nanowire micro thermoelectric generator *Appl. Phys. Lett.* **111** 023105

- [40] Pennelli G and Macucci M 2016 High-power thermoelectric generators based on nanostructured silicon *Semicond. Sci. Technol.* **31** 54001
- [41] Pennelli G 2014 Review of nanostructured devices for thermoelectric applications *Beilstein J. Nanotechnol.* **5** 1268–84
- [42] Ferri M, Suriano F, Roncaglia A, Solmi S, Cerofolini G F, Romano E and Narducci D 2011 Ultradense silicon nanowire arrays produced via top-down planar technology *Microelectron. Eng.* **88** 877–81
- [43] Tasdemir Z, Wollschläger N, Österle W, Leblebici Y and Alaca B E 2016 A deep etching mechanism for trench-bridging silicon nanowires *Nanotechnology* **27** 095303
- [44] Li Y, Buddharaju K, Singh N and Lee S J 2012 Top-down silicon nanowire-based thermoelectric generator: design and characterization *J. Electron. Mater.* **41** 989–92
- [45] Hong S H, Kang M G, Kim B S, Kim D S, Ahn J H, Whang D, Sull S H and Hwang S W 2011 Electrical characteristics of nickel silicide-silicon heterojunction in suspended silicon nanowires *Solid. State. Electron.* **56** 130–4
- [46] Lin Y C, Lu K C, Wu W W, Bai J, Chen L J, Tu K N and Huang Y 2008 Single crystalline PtSi nanowires, PtSi/Si/PtSi nanowire heterostructures, and nanodevices *Nano Lett.* **8** 913–8
- [47] Xu B, Li C, Myronov M and Fobelets K 2013 N-Si-p-Si_{1-x}Ge_x nanowire arrays for thermoelectric power generation *Solid. State. Electron.* **83** 107–12
- [48] Hochbaum A I, Gargas D, Hwang Y J and Yang P 2009 Single crystalline mesoporous silicon nanowires *Nano Lett.* **9** 3550–4
- [49] Xu B and Fobelets K 2014 Spin-on-doping for output power improvement of silicon nanowire array based thermoelectric power generators *J. Appl. Phys.* **115** 214306
- [50] Dimaggio E and Pennelli G 2016 Reliable fabrication of metal contacts on silicon nanowire forests *Nano Lett.* **16** 4348–54
- [51] Nasr Esfahani M, Yilmaz M, Wollschläger N, Rangelow I W, Leblebici Y and Alaca B E 2017 Monolithic technology for silicon nanowires in high-topography architectures *Microelectron. Eng.* **183–4** 42–7
- [52] Rojo M M, Calero O C, Lopeandia A F, Rodriguez-Viejo J and Martín-Gonzalez M 2013 Review on measurement techniques of transport properties of nanowires *Nanoscale* **5** 11526
- [53] Li D, Wu Y, Kim P, Shi L, Yang P and Majumdar A 2003 Thermal conductivity of individual silicon nanowires *Appl. Phys. Lett.* **83** 2934–6
- [54] Shi L, Li D, Yu C, Jang W, Kim D, Yao Z, Kim P and Majumdar A 2003 Measuring thermal and thermoelectric properties of one-dimensional nanostructures using a microfabricated device *J. Heat Transfer* **125** 881
- [55] Mingo N, Yang L, Li D and Majumdar A 2003 Predicting the thermal conductivity of Si and Ge nanowires *Nano Lett.* **3** 1713–6
- [56] Lee J, Lee W, Lim J, Yu Y, Kong Q, Urban J J and Yang P 2016 Thermal transport in silicon nanowires at high temperature up to 700 K *Nano Lett.* **16** 4133–40
- [57] Natarajan Raja S, Rhyner R, Vuttivorakulchai K, Luisier M and Poulikakos D 2017 Length scale of diffusive phonon transport in suspended thin silicon nanowires *Nano Lett.* **17** 276–83
- [58] Park Y H, Kim J, Kim H, Kim I, Lee K-Y Y, Seo D, Choi H J and Kim W 2011 Thermal conductivity of VLS-grown rough Si nanowires with various surface roughnesses and diameters *Appl. Phys. A* **104** 7–14
- [59] Bosseboeuf A, Etienne Allain P, Parrain F, Le Roux X, Isac N, Jacob S, Poizat A, Coste P, Maaroufi S and Walther A 2015 Thermal and electromechanical characterization of top-down fabricated p-type silicon nanowires *Adv. Nat. Sci. Nanosci. Nanotechnol.* **6** 25001
- [60] Ziman J M 1960 Electrons and phonons: the theory of transport phenomena in solids *Endeavour* **20** 555
- [61] Balandin A and Wang K L 1998 Effect of phonon confinement on the thermoelectric figure of merit of quantum wells *J. Appl. Phys.* **84** 6149–53
- [62] Dismukes J P, Ekstrom L, Steigmeier E F, Kudman I and Beers D S 1964 Thermal and electrical properties of heavily doped Ge–Si alloys up to 1300 °K *J. Appl. Phys.* **35** 2899–907
- [63] Vining C B, Laskow W, Hanson J O, Van der Beck R R and Gorsuch P D 1991 Thermoelectric properties of pressure-sintered Si_{0.8}Ge_{0.2} thermoelectric alloys *J. Appl. Phys.* **69** 4333–40
- [64] Steele M C and Rosi F D 1958 Thermal conductivity and thermoelectric power of germanium-silicon alloys *J. Appl. Phys.* **29** 1517–20
- [65] Hsiao T K, Chang H K, Liou S C, Chu M W, Lee S C and Chang C W 2013 Observation of room erature ballistic thermal conduction persisting over 8.3 μm in SiGe nanowires *Nat. Nanotechnol.* **8** 534–8
- [66] Martinez J A, Provencio P P, Picraux S T, Sullivan J P and Swartzentruber B S 2011 Enhanced thermoelectric figure of merit in SiGe alloy nanowires by boundary and hole-phonon scattering *J. Appl. Phys.* **110** 074317
- [67] Lee E K *et al* 2012 Large thermoelectric figure-of-merits from SiGe nanowires by simultaneously measuring electrical and thermal transport properties *Nano Lett.* **12** 2918–23
- [68] Yin L, Kyung Lee E, Woon Lee J, Whang D, Lyong Choi B and Yu C 2012 The influence of phonon scatterings on the thermal conductivity of SiGe nanowires *Appl. Phys. Lett.* **101** 043114
- [69] Kim H, Kim I, Choi H J and Kim W 2010 Thermal conductivities of Si_{1-x}Ge_x nanowires with different germanium concentrations and diameters *Appl. Phys. Lett.* **96** 233106
- [70] Hochbaum A I, Chen R, Delgado R D, Liang W, Garnett E C, Najarian M, Majumdar A and Yang P 2008 Enhanced thermoelectric performance of rough silicon nanowires *Nature* **451** 163–7
- [71] Lim J, Hippalgaonkar K, Andrews S C, Majumdar A and Yang P 2012 Quantifying surface roughness effects on phonon transport in silicon nanowires *Nano Lett.* **12** 2475–82
- [72] Kim H, Park Y-H, Kim I, Kim J, Choi H-J and Kim W 2011 Effect of surface roughness on thermal conductivity of VLS-grown rough Si_{1-x}Ge_x nanowires *Appl. Phys. a-Materials Sci. Process.* **104** 23–8
- [73] Casimir H B G 1938 Note on the conduction of heat in crystals *Physica* **5** 495–500
- [74] Sadhu J and Sinha S 2011 Room-temperature phonon boundary scattering below the Casimir limit *Phys. Rev. B* **84** 115450
- [75] Martin P, Aksamija Z, Pop E and Ravaioli U 2009 Impact of phonon-surface roughness scattering on thermal conductivity of thin Si nanowires *Phys. Rev. Lett.* **102** 125503
- [76] Ghossoub M G, Valavalá K V, Seong M, Azeredo B, Hsu K, Sadhu J S, Singh P K and Sinha S 2013 Spectral phonon scattering from sub-10 nm surface roughness wavelengths in metal-assisted chemically etched Si nanowires *Nano Lett.* **13** 1564–71
- [77] Boukai A I, Bunimovich Y, Tahir-Kheli J, Yu J K, Goddard W A and Heath J R 2008 Silicon nanowires as efficient thermoelectric materials *Nature* **451** 168–71
- [78] Hsiao T K, Huang B W, Chang H K, Liou S C, Chu M W, Lee S C and Chang C W 2015 Micron-scale

- ballistic thermal conduction and suppressed thermal conductivity in heterogeneously interfaced nanowires *Phys. Rev. B* **91** 035406
- [79] Huang B W, Hsiao T K, Lin K H, Chiou D W and Chang C W 2015 Length-dependent thermal transport and ballistic thermal conduction *AIP Adv.* **5** 077187
- [80] Johnson J A, Maznev A A, Cuffe J, Eliason J K, Minnich A J, Kehoe T, Torres C M S, Chen G and Nelson K A 2013 Direct measurement of room-temperature nondiffusive thermal transport over micron distances in a silicon membrane *Phys. Rev. Lett.* **110** 217206
- [81] Minnich A J, Johnson J A, Schmidt A J, Esfarjani K, Dresselhaus M S, Nelson K A and Chen G 2011 Thermal conductivity spectroscopy technique to measure phonon mean free paths *Phys. Rev. Lett.* **107** 095901
- [82] Regner K T, Sellan D P, Su Z, Amon C H, McGaughey A J H and Malen J A 2013 Broadband phonon mean free path contributions to thermal conductivity measured using frequency domain thermoreflectance *Nat. Commun.* **4** 1640
- [83] Maire J, Anufriev R and Nomura M 2017 Ballistic thermal transport in silicon nanowires *Sci. Rep.* **7** 41794
- [84] Prasher R, Tong T and Majumdar A 2008 Approximate analytical models for phonon specific heat and ballistic thermal conductance of nanowires *Nano Lett.* **8** 99–103
- [85] Garg J, Bonini N, Kozinsky B and Marzari N 2011 Role of disorder and anharmonicity in the thermal conductivity of silicon–germanium alloys: a first-principles study *Phys. Rev. Lett.* **106** 045901
- [86] Kimukin I, Islam M S and Williams R S 2006 Surface depletion thickness of p-doped silicon nanowires grown using metal-catalysed chemical vapour deposition *Nanotechnology* **17** S240–5
- [87] Pennelli G, Totaro M, Piotto M and Bruschi P 2013 Seebeck coefficient of nanowires interconnected into large area networks *Nano Lett.* **13** 2592–7
- [88] Diarra M, Niquet Y M, Delerue C and Allan G 2007 Ionization energy of donor and acceptor impurities in semiconductor nanowires: importance of dielectric confinement *Phys. Rev. B* **75** 045301
- [89] Kittel C 2005 *Introduction to Solid State Physics* (Hoboken, NJ: Wiley)
- [90] Seong M, Sadhu J S, Ma J, Ghossoub M G and Sinha S 2012 Modeling and theoretical efficiency of a silicon nanowire based thermoelectric junction with area enhancement *J. Appl. Phys.* **111** 124319
- [91] Shi L 2012 Thermal and thermoelectric transport in nanostructures and low-dimensional systems *Nanoscale Microscale Thermophys. Eng.* **16** 79–116
- [92] Mirza M M, MacLaren D A, Samarelli A, Holmes B M, Zhou H, Thoms S, Macintyre D and Paul D J 2014 Determining the electronic performance limitations in top-down-fabricated Si nanowires with mean widths down to 4 nm *Nano Lett.* **14** 6056–60
- [93] Karg S, Mensch P, Gotsmann B, Schmid H, Kanungo P Das, Ghoneim H, Schmidt V, Björk M T, Troncale V and Riel H 2013 Measurement of thermoelectric properties of single semiconductor nanowires *J. Electron. Mater.* **42** 2409–14
- [94] Pokhrel A, Degregorio Z P, Higgins J M, Girard S N and Jin S 2013 Vapor phase conversion synthesis of higher manganese silicide ($MnSi_{1.75}$) nanowire arrays for thermoelectric applications *Chem. Mater.* **25** 632–8
- [95] Yamamoto K, Kohno H, Takeda S and Ichikawa S 2006 Fabrication of iron suicide nanowires from nanowire templates *Appl. Phys. Lett.* **89** 032903
- [96] Liang Y H, Yu S Y, Hsin C L, Huang C W and Wu W W 2011 Growth of single-crystalline cobalt silicide nanowires with excellent physical properties *J. Appl. Phys.* **110** 096103
- [97] Szczecz J R, Schmitt A L, Bierman M J and Jin S 2007 Single-crystal semiconducting chromium disilicide nanowires synthesized via chemical vapor transport *Chem. Mater.* **19** 3238–43
- [98] Chen Y, Ohlberg D A A and Williams R S 2002 Nanowires of four epitaxial hexagonal silicides grown on Si(001) *J. Appl. Phys.* **91** 3213–8
- [99] Hsu H C, Wu W W, Hsu N F and Chen L J 2007 Growth of high-density titanium suicide nanowires in a single direction on a silicon surface *Nano Lett.* **7** 885–9
- [100] Bennett P A, He Z, Smith D J and Ross F M 2011 Endotaxial silicide nanowires: a review *Thin Solid Films* **519** 8434–40
- [101] Ponnambalam V and Morelli D T 2012 Effect of Cr and Fe substitution on the transport properties of the nowotny chimney-ladder $MnSi_\delta$ ($1.73 < \delta < 1.75$) compounds *J. Electron. Mater.* **41** 1389–94
- [102] Ponnambalam V, Lehr G and Morelli D T 2011 Influence of p- and n-type doping on the transport properties of the Nowotny chimney-ladder compounds $RuAl_2$ and $RuGa_2$ *J. Mater. Res.* **26** 1907–12
- [103] Hsin C-L, Liu Y-T and Tsai Y-Y 2017 Suppressed Umklapp scattering of β - $FeSi_2$ thin film and single crystalline nanowires *Nanotechnology* **28** 485702
- [104] Zhou F, Szczecz J, Pettes M T, Moore A L, Jin S and Shi L 2007 Determination of transport properties in chromium disilicide nanowires via combined thermoelectric and structural characterizations *Nano Lett.* **7** 1649–54
- [105] Seo K, Varadwaj K S K, Cha D, In J, Kim J, Park J and Kim B 2007 Synthesis and electrical and properties of single and crystalline CrSi and nanowires *J. Phys. Chem. B* **111** 9072–6
- [106] Higgins J M, Schmitt A L, Guzei I A and Jin S 2008 Higher manganese silicide nanowires of nowotny chimney ladder phase *J. Am. Chem. Soc.* **130** 16086–94
- [107] King T-J and Saraswat K C 1994 Deposition and properties of low-pressure chemical-vapor deposited polycrystalline silicon–germanium films *J. Electrochem. Soc.* **141** 2235
- [108] Ferrando-Villalba P *et al* 2014 In-plane thermal conductivity of sub-20 nm thick suspended mono-crystalline Si layers *Nanotechnology* **25** 185402
- [109] Ju Y S 2005 Phonon heat transport in silicon nanostructures *Appl. Phys. Lett.* **87** 153106
- [110] Ju Y S and Goodson K E 1999 Phonon scattering in silicon films with thickness of order 100 nm *Appl. Phys. Lett.* **74** 3005–7
- [111] Asheghi M, Leung Y K, Wong S S and Goodson K E 1997 Phonon-boundary scattering in thin silicon layers *Appl. Phys. Lett.* **71** 1798–800
- [112] Liu W and Asheghi M 2004 Phonon-boundary scattering in ultrathin single-crystal silicon layers *Appl. Phys. Lett.* **84** 3819–21
- [113] Cheaito R, Duda J C, Beechem T E, Hattar K, Ihlefeld J F, Medlin D L, Rodriguez M A, Campion M J, Piekos E S and Hopkins P E 2012 Experimental investigation of size effects on the thermal conductivity of silicon–germanium alloy thin films *Phys. Rev. Lett.* **109** 195901
- [114] Koh Y K and Cahill D G 2007 Frequency dependence of the thermal conductivity of semiconductor alloys *Phys. Rev. B* **76** 75207
- [115] Chakraborty S, Kleint C A, Heinrich A, Schneider C M, Schumann J, Falke M and Teichert S 2003 Thermal conductivity in strain symmetrized Si/Ge superlattices on Si(111) *Appl. Phys. Lett.* **83** 4184–6
- [116] Huxtable S T, Abramson A R, Tien C L, Majumdar A, Labounty C, Fan X, Zeng G, Bowers J E, Shakouri A and Croke E T 2002 Thermal conductivity of Si/SiGe and SiGe/SiGe superlattices *Appl. Phys. Lett.* **80** 1737–9

- [117] Lee S M, Cahill D G and Venkatasubramanian R 1997 Thermal conductivity of Si–Ge superlattices *Appl. Phys. Lett.* **70** 2957–9
- [118] Taniguchi T, Sakane S, Aoki S, Okuhata R, Ishibe T, Watanabe K, Suzuki T, Fujita T, Sawano K and Nakamura Y 2017 Thermoelectric properties of epitaxial β -FeSi₂ thin films on Si(111) and approach for their enhancement *J. Electron. Mater.* **46** 3235–41
- [119] Hou Q R, Zhao W, Chen Y B, Liang D, Feng X, Zhang H Y and He Y J 2007 Thermoelectric properties of higher manganese silicide films with addition of chromium *Appl. Phys. A* **86** 385–9
- [120] Schumann J, Gladun C, Mönch J I, Heinrich A, Thomas J and Pitschke W 1994 Nanodispersed Cr_xSi_{1-x} thin films: transport properties and thermoelectric application *Thin Solid Films* **246** 24–9
- [121] Heinrich A, Griessmann H, Behr G, Ivanenko K, Schumann J and Vinzelberg H 2001 Thermoelectric properties of beta-FeSi₂ single crystals and polycrystalline β -FeSi_{2+x} thin films *Thin Solid Films* **381** 287–95
- [122] Samarelli A *et al* 2013 The thermoelectric properties of Ge/SiGe modulation doped superlattices *J. Appl. Phys.* **113** 233704
- [123] Ferrando-Villalba P *et al* 2015 Tailoring thermal conductivity by engineering compositional gradients in Si_{1-x}Ge_x superlattices *Nano Res.* **8** 2833–41
- [124] Saveli G, Silveira Stein S, Bernard-Granger G, Faucherand P, Montés L, Dilhaire S and Pernot G 2015 Titanium-based silicide quantum dot superlattices for thermoelectrics applications *Nanotechnology* **26** 275605
- [125] Bao Y, Liu W L, Shamsa M, Alim K, Balandin A A and Liu J L 2005 Electrical and thermal conductivity of Ge/Si quantum dot superlattices *J. Electrochem. Soc.* **152** G432
- [126] Hicks L D and Dresselhaus M S 1993 Effect of quantum-well structures on the thermoelectric figure of merit *Phys. Rev. B* **47** 12727–31
- [127] Borca-Tasciuc T *et al* 2000 Thermal conductivity of symmetrically strained Si/Ge superlattices *Superlattices Microstruct.* **28** 199–206
- [128] Liu W L, Borca-Tasciuc T, Chen G, Liu J L and Wang K L 2001 Anisotropic thermal conductivity of Ge quantum-dot and symmetrically strained Si/Ge superlattices *J. Nanosci. Nanotechnol.* **1** 39–42
- [129] Li G *et al* 2017 In-plane thermal conductivity of radial and planar Si/SiO_x hybrid nanomembrane superlattices *ACS Nano* **11** 8215–22
- [130] Olsson R H III and El-Kady I 2009 Microfabricated phononic crystal devices and applications *Meas. Sci. Technol.* **20** 12002
- [131] Yu J K, Mitrovic S, Tham D, Varghese J and Heath J R 2010 Reduction of thermal conductivity in phononic nanomesh structures *Nat. Nanotechnol.* **5** 718–21
- [132] Hopkins P E, Reinke C M, Su M F, Olsson R H, Shaner E A, Leseman Z C, Serrano J R, Phinney L M and El-Kady I 2011 Reduction in the thermal conductivity of single crystalline silicon by phononic crystal patterning *Nano Lett.* **11** 107–12
- [133] Haras M, Lacatena V, Bah T M, Didenko S, Robillard J F, Monfray S, Skotnicki T and Dubois E 2016 Fabrication of thin-film silicon membranes with phononic crystals for thermal conductivity measurements *IEEE Electron Device Lett.* **37** 1358–61
- [134] Nomura M and Maire J 2015 Mechanism of the reduced thermal conductivity of fishbone-type Si phononic crystal nanostructures *J. Electron. Mater.* **44** 1426–31
- [135] Chen Z, Zhang X and Pei Y 2018 Manipulation of phonon transport in thermoelectrics *Adv. Mater.* **30** 1705617
- [136] Jeng M-S, Yang R, Song D and Chen G 2008 Modeling the thermal conductivity and phonon transport in nanoparticle composites using Monte Carlo simulation *J. Heat Transfer* **130** 42410
- [137] Yang R, Chen G and Dresselhaus M S 2005 Thermal conductivity of simple and tubular nanowire composites in the longitudinal direction *Phys. Rev. B* **72** 125418
- [138] Lan Y, Minnich A J, Chen G and Ren Z 2010 Enhancement of thermoelectric figure-of-merit by a bulk nanostructuring approach *Adv. Funct. Mater.* **20** 357–76
- [139] Zebarjadi M, Esfarjani K, Dresselhaus M S, Ren Z F and Chen G 2012 Perspectives on thermoelectrics: from fundamentals to device applications *Energy Environ. Sci.* **5** 5147
- [140] Minnich A J, Dresselhaus M S, Ren Z F and Chen G 2009 Bulk nanostructured thermoelectric materials: current research and future prospects *Energy Environ. Sci.* **2** 466
- [141] Savvides N and Goldsmid H J 1980 Boundary scattering of phonons in fine-grained hot-pressed Ge–Si alloys. I. The dependence of lattice thermal conductivity on grain size and porosity *J. Phys. C: Solid State Phys.* **13** 4657–70
- [142] Zhu T, Yu G, Xu J, Wu H, Fu C, Liu X, He J and Zhao X 2016 The role of electron–phonon interaction in heavily doped fine-grained bulk silicones as thermoelectric materials *Adv. Electron. Mater.* **2** 1600171
- [143] Liao B, Qiu B, Zhou J, Huberman S, Esfarjani K and Chen G 2015 Significant reduction of lattice thermal conductivity by the electron–phonon interaction in silicon with high carrier concentrations: a first-principles study *Phys. Rev. Lett.* **114** 216601
- [144] Schierning G *et al* 2011 Role of oxygen on microstructure and thermoelectric properties of silicon nanocomposites *J. Appl. Phys.* **110** 113515
- [145] Kessler V, Gautam D, Hülser T, Spree M, Theissmann R, Winterer M, Wiggers H, Schierning G and Schmehel R 2013 Thermoelectric properties of nanocrystalline silicon from a scaled-up synthesis plant *Adv. Eng. Mater.* **15** 379–85
- [146] Claudio T, Stein N, Stroppa D G, Klobergs B, Koza M M, Kudejova P, Petermann N, Wiggers H, Schierning G and Hermann R P 2014 Nanocrystalline silicon: lattice dynamics and enhanced thermoelectric properties *Phys. Chem. Chem. Phys.* **16** 25701–9
- [147] Murugasami R, Vivekanandhan P, Kumaran S, Suresh Kumar R and John Tharakan T 2018 Thermoelectric power factor performance of silicon–germanium alloy doped with phosphorus prepared by spark plasma assisted transient liquid phase sintering *Scr. Mater.* **143** 35–9
- [148] Joshi G *et al* 2008 Enhanced thermoelectric figure-of-merit in nanostructured p-type silicon germanium bulk alloys *Nano Lett.* **8** 4670–4
- [149] Wang X W *et al* 2008 Enhanced thermoelectric figure of merit in nanostructured n-type silicon germanium bulk alloy *Appl. Phys. Lett.* **93** 193121
- [150] Schaevitz S B, Franz A J, Jensen K F and Schmidt M A 2001 A combustion-based MEMS thermoelectric power generator *Transducers '01 Eurosensors 15* pp 30–3
- [151] Kim W and Majumdar A 2006 Phonon scattering cross section of polydispersed spherical nanoparticles *J. Appl. Phys.* **99** 129901
- [152] Mingo N, Hauser D, Kobayashi N P, Plissonnier M and Shakouri A 2009 ‘Nanoparticle-in-alloy’ approach to efficient thermoelectrics: silicides in SiGe *Nano Lett.* **9** 711–5
- [153] Nozariasbmarz A, Roy P, Zamanipour Z, Dycus J H, Cabral M J, LeBeau J M, Krasinski J S and Vashaei D 2016 Comparison of thermoelectric properties of nanostructured Mg₂Si, FeSi₂, SiGe, and nanocomposites of SiGe–Mg₂Si, SiGe–FeSi₂ *APL Mater.* **4** 104814

- [154] Nozariasbmarz A, Zamanipour Z, Norouzzadeh P, Krasinski J S and Vashaee D 2016 Enhanced thermoelectric performance in a metal/semiconductor nanocomposite of iron silicide/silicon germanium *RSC Adv.* **6** 49643–50
- [155] Bathula S, Jayasimhadri M, Gahtori B, Kumar A, Srivastava A K and Dhar A 2017 Enhancement in thermoelectric performance of SiGe nanoalloys dispersed with SiC nanoparticles *Phys. Chem. Chem. Phys.* **19** 25180–5
- [156] Bahk J-H, Bian Z and Shakouri A 2013 Electron energy filtering by a nonplanar potential to enhance the thermoelectric power factor in bulk materials *Phys. Rev. B* **87** 75204
- [157] Narducci D, Frabboni S and Zianni X 2015 Silicon de novo: energy filtering and enhanced thermoelectric performances of nanocrystalline silicon and silicon alloys *J. Mater. Chem. C* **3** 12176–85
- [158] Zebarjadi M, Joshi G, Zhu G, Yu B, Minnich A, Lan Y, Wang X, Dresselhaus M, Ren Z and Chen G 2011 Power factor enhancement by modulation doping in bulk nanocomposites *Nano Lett.* **11** 2225–30
- [159] Muthiah S, Singh R C, Pathak B D, Avasthi P K, Kumar R, Kumar A, Srivastava A K and Dhar A 2018 Significant enhancement in thermoelectric performance of nanostructured higher manganese silicides synthesized employing a melt spinning technique *Nanoscale* **10** 1970–7
- [160] Thimont Y, Presmanes L, Baylac V, Tailhades P, Berthebaud D and Gascoin F 2018 Thermoelectric higher manganese silicide: synthetized, sintered and shaped simultaneously by selective laser sintering/melting additive manufacturing technique *Mater. Lett.* **214** 236–9
- [161] Miura A, Zhou S, Nozaki T and Shiomi J 2015 Crystalline-amorphous silicon nanocomposites with reduced thermal conductivity for bulk thermoelectrics *ACS Appl. Mater. Interfaces* **7** 13484–9
- [162] Rowe D M, Shukla V S and Savvides N 1981 Phonon scattering at grain boundaries in heavily doped fine-grained silicon–germanium alloys *Nature* **290** 765–6
- [163] Yusufu A, Kurosaki K, Miyazaki Y, Ishimaru M, Kosuga A, Ohishi Y, Muta H and Yamanaka S 2014 Bottom-up nanostructured bulk silicon: a practical high-efficiency thermoelectric material *Nanoscale* **6** 13921–7
- [164] Satyala N, Krasinski J S and Vashaee D 2014 Simultaneous enhancement of mechanical and thermoelectric properties of polycrystalline magnesium silicide with conductive glass inclusion *Acta Mater.* **74** 141–50
- [165] Zhang Q, He J, Zhu T J, Zhang S N, Zhao X B and Tritt T M 2008 High figures of merit and natural nanostructures in $Mg_2Si_{0.4}Sn_{0.6}$ based thermoelectric materials *Appl. Phys. Lett.* **93** 102109
- [166] Cahill D G, Ford W K, Goodson K E, Mahan G D, Majumdar A, Maris H J, Merlin R and Phillpot S R 2003 Nanoscale thermal transport *J. Appl. Phys.* **93** 793–818
- [167] Föll H, Christoffersen M, Carstensen J and Hasse G 2002 Formation and application of porous silicon *Mater. Sci. Eng. R* **39** 93–141
- [168] Gesele G, Linsmeier J, Drach V, Fricke J and Arens-Fischer R 1997 Temperature-dependent thermal conductivity of porous silicon *J. Phys. D: Appl. Phys.* **30** 2911–6
- [169] Yang C C and Li S 2011 Basic principles for rational design of high-performance nanostructured silicon-based thermoelectric materials *ChemPhysChem* **12** 3614–8
- [170] Miyazaki K, Tanaka S and Nagai D 2012 Heat conduction of a porous material *J. Heat Transfer* **134** 51018
- [171] Alvarez F X, Jou D and Sellitto A 2010 Pore-size dependence of the thermal conductivity of porous silicon: a phonon hydrodynamic approach *Appl. Phys. Lett.* **97** 033103
- [172] de Boor J, Kim D S, Ao X, Hagen D, Cojocaru A, Föll H and Schmidt V 2011 Temperature and structure size dependence of the thermal conductivity of porous silicon *Europhysics Lett.* **96** 16001
- [173] Gomès S, David L, Lysenko V, Descamps A, Nychyporuk T and Raynaud M 2007 Application of scanning thermal microscopy for thermal conductivity measurements on meso-porous silicon thin films *J. Phys. D: Appl. Phys.* **40** 6677–83
- [174] He Y, Donadio D, Lee J H, Grossman J C and Galli G 2011 Thermal transport in nanoporous silicon: interplay between disorder at mesoscopic and atomic scales *ACS Nano* **5** 1839–44
- [175] Lee J H, Galli G A and Grossman J C 2008 Nanoporous Si as an efficient thermoelectric material *Nano Lett.* **8** 3750–4
- [176] Romano G, Di Carlo A and Grossman J C 2012 Mesoscale modeling of phononic thermal conductivity of porous Si: interplay between porosity, morphology and surface roughness *J. Comput. Electron.* **11** 8–13
- [177] Tang J, Wang H T, Lee D H, Fardy M, Huo Z, Russell T P and Yang P 2010 Holey silicon as an efficient thermoelectric material *Nano Lett.* **10** 4279–83
- [178] Boor J, Kim D S, Ao X, Becker M, Hinsche N F, Mertig I, Zahn P and Schmidt V 2012 Thermoelectric properties of porous silicon *Appl. Phys. A* **107** 789–94
- [179] Weisse J M, Marconnet A M, Kim D, Rao P M, Panzer M A, Goodson K E and Zheng X 2012 Thermal conductivity in porous silicon nanowire arrays *Nanoscale Res. Lett.* **7** 554
- [180] Zhang T, Wu S, Xu J, Zheng R and Cheng G 2015 High thermoelectric figure-of-merits from large-area porous silicon nanowire arrays *Nano Energy* **13** 433–41
- [181] Tang G H, Bi C and Fu B 2013 Thermal conduction in nanoporous silicon thin film *J. Appl. Phys.* **114** 184302
- [182] He Y, Donadio D and Galli G 2011 Morphology and temperature dependence of the thermal conductivity of nanoporous SiGe *Nano Lett.* **11** 3608–11
- [183] Perez-Taborda J A, Muñoz Rojo M, Maiz J, Neophytou N and Martin-Gonzalez M 2016 Ultra-low thermal conductivities in large-area Si–Ge nanomeshes for thermoelectric applications *Sci. Rep.* **6** 32778
- [184] Li Y, Buddharaju K, Tinh B C, Singh N and Lee S J 2012 Improved vertical silicon nanowire based thermoelectric power generator with polyimide filling *IEEE Electron Device Lett.* **33** 715–7
- [185] Xu B, Li C, Thielemans K, Myronov M and Fobelets K 2012 Thermoelectric performance of $Si_{0.8}Ge_{0.2}$ nanowire arrays *IEEE Trans. Electron Devices* **59** 3193–8
- [186] Norris K J, Garrett M P, Zhang J, Coleman E, Tompa G S and Kobayashi N P 2015 Silicon nanowire networks for multi-stage thermoelectric modules *Energy Convers. Manag.* **96** 100–4
- [187] Fonseca L *et al* 2016 Smart integration of silicon nanowire arrays in all-silicon thermoelectric micro-nanogenerators *Semicond. Sci. Technol.* **31** 084001
- [188] Choi J, Cho K and Kim S 2017 Flexible thermoelectric generators composed of n-and p-type silicon nanowires fabricated by top-down method *Adv. Energy Mater.* **7** 1602138
- [189] Samarelli A *et al* 2014 Prospects for SiGe thermoelectric generators *Solid. State. Electron.* **98** 70–4
- [190] Strasser M, Aigner R, Lauterbach C, Sturm T F, Franosh M and Wachutka G 2003 Micromachined CMOS thermoelectric generators as on-chip power

- supply *TRANSDUCERS '03. 12th Int. Conf. on Solid-State Sensors, Actuators and Microsystems. Digest of Technical Papers (Cat. No.03TH8664)* vol 1 (IEEE) pp 45–8
- [191] Xie J, Lee C and Feng H 2010 Design, fabrication, and characterization of CMOS MEMS-Based thermoelectric power generators *J. Microelectromech. Syst.* **19** 317–24
- [192] Perez-Marín A P, Lopeandía A F, Abad L, Ferrando-Villaba P, García G, Lopez A M, Muñoz-Pascual F X and Rodríguez-Viejo J 2014 Micropower thermoelectric generator from thin Si membranes *Nano Energy* **4** 73–80
- [193] Kessler V *et al* 2014 Fabrication of high-temperature-stable thermoelectric generator modules based on nanocrystalline silicon *J. Electron. Mater.* **43** 1389–96
- [194] Glosch H, Ashauer M, Pfeiffer U and Lang W 1999 Thermoelectric converter for energy supply *Sensors Actuators A* **74** 246–50
- [195] She X, Su X, Du H, Liang T, Zheng G, Yan Y, Akram R, Uher C and Tang X 2015 High thermoelectric performance of higher manganese silicides prepared by ultra-fast thermal explosion *J. Mater. Chem. C* **3** 12116–22
- [196] Rowe D M 2005 *Thermoelectrics Handbook: Macro to Nano* vol 80 (New York: CRC Press) p 1014
- [197] Lu J, Guo R, Dai W and Huang B 2015 Enhanced in-plane thermoelectric figure of merit in p-type SiGe thin films by nanograin boundaries *Nanoscale* **7** 7331–9
- [198] Liao C N, Chen C and Tu K N 1999 Thermoelectric characterization of Si thin films in silicon-on-insulator wafers *J. Appl. Phys.* **86** 3204