

Calvin Deutschbein (they/them)

CONTACT INFORMATION

Assistant Professor of [Computer Science](#)
[Willamette University](#)
[Computing & Data Science](#)
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RESEARCH INTERESTS

Mining Secure Behavior of Hardware Designs: specification mining, data mining, machine learning, computer security, cybersecurity, hardware security, secure design, security validation, computer architecture hardware design languages (HDL), information flow tracking (IFT), logics of specification, register transfer level (RTL), instruction set architecture (ISA), hyperproperties, reduced instruction set computers (RISC), complex instruction set computers (CISC), x86, temporal logics, linear temporal logic (LTL)

CURRENT ACADEMIC APPOINTMENTS

Assistant Professor, [Willamette University](#)
[Computer Science](#)
[Computing & Data Science Programs](#)

August 2021 to present

PREVIOUS ACADEMIC APPOINTMENTS

Adjunct Professor, [Elon University](#)
[Department of Computer Science](#)

Spring 2020

- Instructor of Record: [CSC 130 Computer Science I](#)

Instructor, [The University of North Carolina at Chapel Hill](#)
[Department of Computer Science](#)

Summer 2018

- Instructor of Record: [COMP 116 Introduction to Scientific Programming](#)

Research Scholar, [Semiconductor Research Corporation](#)
[SRC Research Scholars Program](#)

October 2018 to August 2021

- Tasks:
 - [Tackling the Corner Cases: Finding Security Vulnerabilities in CPU Designs](#)
 - [Automatically Generating Information Flow Properties](#)

EDUCATION

The University of North Carolina at Chapel Hill, Chapel Hill, NC

Ph.D., [Computer Science](#), August 2021

- Thesis: [Mining Secure Behavior of Hardware Designs](#)
- Advisor: [Cynthia Sturton](#)
- Area: [Hardware Security](#)

M.S., [Computer Science](#), August 2017

- Thesis: [Multi-core Cyclic Executives for Safety-Critical Systems](#)
- Advisor: [Sanjoy Baruah](#)
- Area: [Real-Time Systems](#)

The University of Chicago, Chicago, IL

B.S., [Computer Science](#), March 2015

- Thesis: [Performance and Energy Limits of a Processor-integrated FFT Accelerator](#)
- Advisor: [Andrew A. Chien](#)
- Area: [Computer Architecture](#)

B.A., [Mathematics](#), March 2015

REFEREED
JOURNAL
PUBLICATIONS

- [1] R. Zhang, C. Deutschbein, P. Huang, C. Sturton. End-to-End Automated Exploit Generation for Processor Security Validation. *IEEE Design & Test Special Issue: Hardware Security Top Picks*. 2021.
doi:[10.1109/MDAT.2021.3063314](https://doi.org/10.1109/MDAT.2021.3063314)
- [2] C. Deutschbein, T. Fleming, A. Burns, S. Baruah. Multi-core Cyclic Executives for Safety-Critical Systems. *Science of Computer Programming*, March 2019.
doi:[10.1016/j.scico.2018.11.004](https://doi.org/10.1016/j.scico.2018.11.004)

REFEREED
CONFERENCE
PUBLICATIONS

- [3] C. Deutschbein, C. Sturton. Evaluating Security Specification Mining for a CISC Architecture. In: *Proceedings of the IEEE International Symposium on Hardware Oriented Security and Trust (HOST)*, December 2020.
doi:[10.1109/HOST45689.2020.9300291](https://doi.org/10.1109/HOST45689.2020.9300291)
- [4] R. Zhang, C. Deutschbein, P. Huang, C. Sturton. End-to-End Automated Exploit Generation for Processor Security Validation. In: *MICRO-51: Proceedings of the 51st Annual IEEE/ACM International Symposium on Microarchitecture*, October 2018.
doi:[10.1109/MICRO.2018.00071](https://doi.org/10.1109/MICRO.2018.00071)
- [5] C. Deutschbein, T. Fleming, A. Burns, S. Baruah. Multi-core Cyclic Executives for Safety-Critical Systems. In: *Proceedings of the Third International Symposium on Dependable Software Engineering: Theories, Repositorys, and Applications, SETTA 2017*, October 2017.
doi:[10.1016/j.scico.2018.11.004](https://doi.org/10.1016/j.scico.2018.11.004)
- [6] C. Deutschbein, S. Baruah. Preemptive Uniprocessor EDF Schedulability Analysis with Preemption Costs Considered. In: *Proceedings of the 2016 IEEE Real-Time Systems Symposium (RTSS)*, November 2016.
doi:[10.1109/RTSS.2016.047](https://doi.org/10.1109/RTSS.2016.047)
- [7] T. Thanh-Hoang, A. Shambayati, C. Deutschbein, H. Hoffmann, A. A. Chien Performance and energy limits of a processor-integrated FFT accelerator. In: *Proceedings of the 2014 IEEE High Performance Extreme Computing Conference (HPEC)*, September 2014.
doi:[10.1109/HPEC.2014.7040951](https://doi.org/10.1109/HPEC.2014.7040951)

INVITED TALKS

- [8] C. Deutschbein. Creating Information Flow Specifications. Radix Presentation for Tortuga Logic. August 20, 2021.
- [9] C. Deutschbein. Extracting IF specifications from HW designs. University of Illinois–Urbana Champaign July 20, 2021.