37. Octal Serial Peripheral Interface (OSPI)

This is the OSPI_B version of the OSPI peripheral module.

OSPI_B is referred to as OSPI in this chapter.

37.1 Overview

The xSPI (eXpanded Serial Peripheral Interface) protocol specifies the interface for Non-Volatile Memory Devices, which provides high data throughput, low signal count, and limited backward compatibility with legacy SPI devices. The electrical interface can deliver up to 200 Mbytes per second raw data throughput. The OSPI is compliant with JEDEC standard JESD251(Profile 1.0 and 2.0), JESD251-1 and JESD252.

JESD251 specifies two interface profiles where profile 1.0 is Octal SPI and profile 2.0 is HyperBus™ (HyperRAM™ and HyperFlash™).

OSPI supports QSPI protocol.

Table 37.1 lists the OSPI specifications, Figure 37.1 shows a block diagram, and Table 37.2 lists the I/O pins.

Table 37.1 OSPI specifications

Item	Description
Protocol	Compliant with the xSPI protocol
Data transmission and reception	Issue the transaction for up to 2 Slave as Master Only one of the memory devices can operate at a time.
Transfer speed	Support the transfer at xSPI200
Mode	• Support Protocol modes below – 1/4/8pin with SDR/DDR (1S-1S-1S, 4S-4D-4D, 8D-8D-8D) – 2/4pin with SDR (1S-2S-2S, 2S-2S-2S, 1S-4S-4S, 4S-4S-4S) • Configurable address length • Configurable initial access latency cycle • Support XiP mode
OSPI function	• Support Write Data Mask • Support In-band Reset • Memory-mapping – Support up to 256 MB address space each CS – Prefetch function for burst-read with low latency – Outstanding buffer for burst-write with high throughput • Manual command – Configurable up to 4 commands – Status Register Polling function • Input Strobe port timing shift
Transfer target	Each bus master More details, see section 14, Buses
Decryption function	Decryption on the fly is available for memory map read
Interrupt source	Error interrupt Completion interrupt
Module-stop function	Module-stop state can be set to reduce power consumption
TrustZone Filter	Security attribution can be set for IO register area External address space is defined as Non-secure

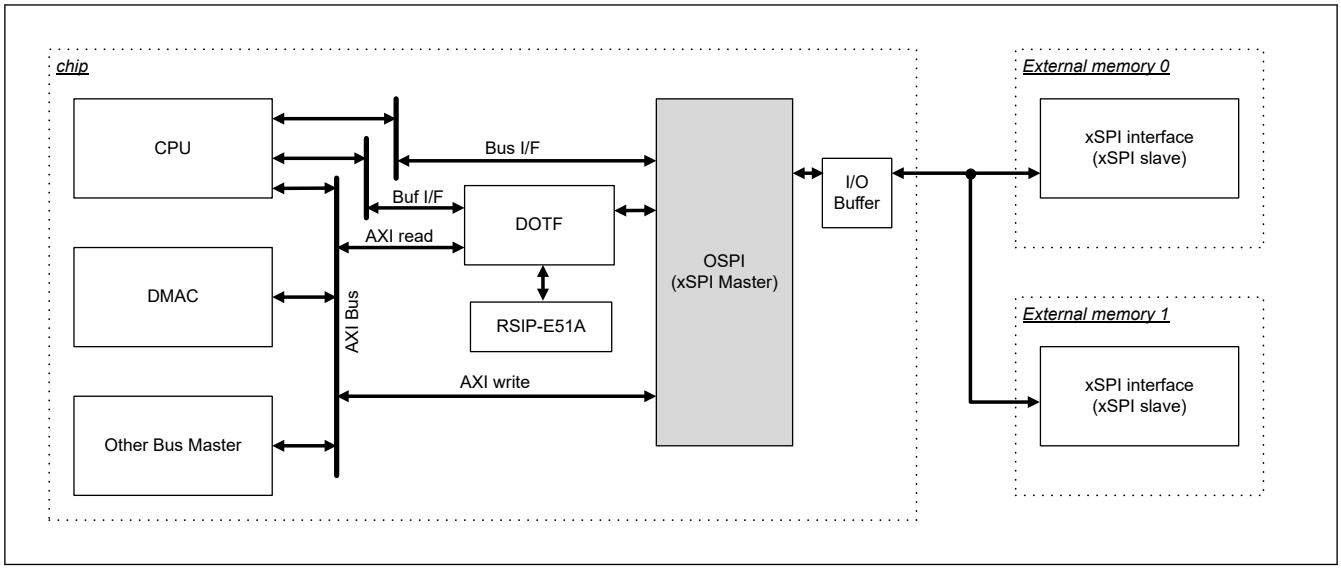


Figure 37.1 Block diagram

Table 37.2 OSPI I/O pins

Pin name	I/O	Function
OM_SCLK	Output	Clock Positive
OM_SCLKN	Output	Clock Negative
OM_CS0	Output	Chip Select for slave0
OM_CS1	Output	Chip Select for slave1
OM_DQS	I/O	Read Data Strobe / Write Data Mask
OM_SIO0	I/O	Data 0 input/output
OM_SIO1	I/O	Data 1 input/output
OM_SIO2	I/O	Data 2 input/output
OM_SIO3	I/O	Data 3 input/output
OM_SIO4	I/O	Data 4 input/output
OM_SIO5	I/O	Data 5 input/output
OM_SIO6	I/O	Data 6 input/output
OM_SIO7	I/O	Data 7 input/output
OM_RESET	Output	Master reset status for slave0,1
OM_RSTO1	Input	Slave reset status for slave1
OM_ECSINT1	Input	Interrupt for slave1 / Error Correction Status for slave1
OM_WP1	Output	Write Protect for slave1

Note: For OM_SIO7-0, OM_SCLK, OM_SCKN and OM_DQS pins, 36Ω±5% resistor need to be put on the board to comply with JESD251 I/O driver definition. It is recommended for the operation with proper signal quality.

37.2 Register Descriptions

37.2.1 OSPI Configuration Registers

These registers configure xSPI Master function. These registers should be configured in the initialization phase before issuing xSPI transaction.

37.2.1.1 WRAPCFG : OSPI Wrapper Configuration Register

Base address: OSPI0_B = 0x4026_8000
OSPI0_B_NS = 0x5026_8000

Offset address: 0x000

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	DSSFTCS1[4:0]					—	—	—	—	—	—	—	—	—	—	—	DSSFTCS0[4:0]					—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	—	These bits are read as 0. The write value should be 0.	R/W
12:8	DSSFTCS0[4:0]	OM_DQS shift for slave0 This field configures the number of delay cell for a OM_DQS port. It is used to adjust the OM_DQS sampling timing. When automatic calibration is enabled, it could be updated automatically. In this case, it shall not be written by user. 0x00: No shift 0x01: Add a delay of 1 cell ⋮ 0x1E: Add a delay of 30 cells 0x1F: Add a delay of 31 cells	R/W
23:13	—	These bits are read as 0. The write value should be 0.	R/W
28:24	DSSFTCS1[4:0]	OM_DQS shift for slave1 The function is same as one of slave0.	R/W
31:29	—	These bits are read as 0. The write value should be 0.	R/W

Note: S-TYPE-3, P-TYPE-3

This register has functions to configure xSPI Master function.

37.2.1.2 COMCFG : OSPI Common Configuration Register

Base address: OSPI0_B = 0x4026_8000
OSPI0_B_NS = 0x5026_8000

Offset address: 0x004

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	OENEGEX	OEASTEX	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	—	These bits are read as 0. The write value should be 0.	R/W
16	OEASTEX	Output Enable Asserting extension This bit extends 1 cycle output enable of OM_SIO7-0 and OM_DQS during output enable asserting. When set to 1, OM_CSn (n = 0, 1) asserting should be extended (LIOCFGCSn.CSASTEX = 1 (n = 0, 1)). This bit shall not be used in case of no latency cycle. Because OSPI output data could be conflicted with OSPI input data. 0: No extend 1 cycle Output enable 1: Extend 1 cycle Output enable	R/W

Bit	Symbol	Function	R/W
17	OENEGEX	Output Enable Negating extension This bit extends 1 cycle output enable of OM_SIO7-0 and OM_DQS during output enable negating. This bit should not be used in case of no latency cycle. Because OSPI output data could be conflicted with OSPI input data. 0: No extend 1 cycle Output enable 1: Extend 1 cycle Output enable	R/W
31:18	—	These bits are read as 0. The write value should be 0.	R/W

Note: S-TYPE-3, P-TYPE-3

This register has functions to configure xSPI Master function.

37.2.1.3 BMCFGCHn : OSPI Bridge Map Configuration Register chn (n = 0, 1)

Base address: OSPI0_B = 0x4026_8000
OSPI0_B_NS = 0x5026_8000

Offset address: 0x008 + 0x004 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	CMBTIM[7:0]								—	—	—	—	—	—	—	PREEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	MWRSIZE[7:0]								MWRCOMB	—	—	—	—	—	—	WRMD
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	WRMD	System bus Write Response mode This bit selects the timing of System bus write response in memory-mapping mode. When set to 1, it returns the response after transmitting a frame on xSPI bus. When enabled this mode, Memory Write Combination mode must be disabled. 0: Return response after storing to Internal Write Buffer 1: Return response after issuing write transaction to xSPI bus	R/W
6:1	—	These bits are read as 0. The write value should be 0.	R/W
7	MWRCOMB	Memory Write Combination mode This bit selects to combine the OSPI data in write access of memory-mapping mode. When set to 0, OSPI data size depends on system bus's burst type and size. When this field is set to "1", the data size depends on MWRSIZE[7:0] field.*1 When set to 1, any write transaction could be held in this xSPI master temporarily. 0: Disable combination mode 1: Enable combination mode	R/W
15:8	MWRSIZE[7:0]	Memory Write Size These bits select the size to combine incremental address in memory-mapping mode. It transmits an xSPI frame with the data combined up to the configured size while the address is incremental. When detected non-incremental address or a read transaction before reaching to the target size, it transmits the pending data into xSPI bus. 0x00: Combine incremental address up to 4 bytes 0x01: Combine incremental address up to 8 bytes ⋮ 0x0E: Combine incremental address up to 60 bytes 0x0F: Combine incremental address up to 64 bytes 0xFF: Combine incremental address up to 2 bytes Others: Setting prohibited	R/W
16	PREEN	Prefetch enable This bit enables prefetch function for read transaction in memory-mapping mode. It could reduce the latency for read transaction with incremental address. 0: Disable prefetch function 1: Enable prefetch function	R/W

Bit	Symbol	Function	R/W
23:17	—	These bits are read as 0. The write value should be 0.	R/W
31:24	CMBTIM[7:0]	Combination timer This field specifies expiration period of combination timer. This timer is counted by PCLKA. 0x00 means disabling the combination timer. When the timer is expired, the data in the combination buffer is pushed to memory device.	R/W

Note: S-TYPE-3, P-TYPE-3
Note 1. Writing to OSPI memory space other than 64 bit is prohibited during combination mode.

This register has functions to configure xSPI Master function.

37.2.1.4 CMCFG0CSn : OSPI Command Map Configuration Register 0 CSn (n = 0, 1)

Base address: OSPI0_B = 0x4026_8000
OSPI0_B_NS = 0x5026_8000

Offset address: 0x010 + 0x010 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	ADDRPCD[7:0]								ADDRPEN[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	ARYAMD	WPBSTMD	ADDSIZE[1:0]		FFMT[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	FFMT[1:0]	Frame format These bits configure xSPI frame format in memory-mapping mode. Please see Table 37.7 for detail. 0 0: Normal format: Command 1 byte, Address ADDSIZE, Data up to system bus transaction. 0 1: 8D-8D-8D profile 1.0 format: Command 2 bytes, Address ADDSIZE, Data up to system bus transaction 1 0: 8D-8D-8D profile 2.0 Command Modifier format: Command & Modifier 6 bytes, Data up to system bus transaction 1 1: 8D-8D-8D profile 2.0 Commands with Extended Command Modifier format: Command & Modifier 6 bytes, Data up to system bus transaction	R/W
3:2	ADDSIZE[1:0]	Address size These bits configure the number of address byte in memory-mapping mode. In case of 8D-8D-8D profile 2.0, it should be configured to 4 bytes. 0 0: 1 byte (256-byte address space) 0 1: 2 bytes (64 KB address space) 1 0: 3 bytes (16 MB address space) 1 1: 4 bytes (4 GB address space)	R/W
4	WPBSTMD	Wrapping burst mode When this field is set to 1, the wrapping boundary between system bus access and xSPI memory shall be mached. 0: Separate xSPI transfer at the wrapping address boundary 1: Not separate xSPI transfer at the wrapping address boundary	R/W
5	ARYAMD	Array address mode When this field is set to 1, address for memory is mapped as {A[25:10], A[9:4], 6{RSV}, A[3:0]} where A[25:0] is normal address, and RSV is reserved value(0b). This field is effective only when FFMT=1d. 0: Normal address mode 1: Array address mode	R/W
15:6	—	These bits are read as 0. The write value should be 0.	R/W

Bit	Symbol	Function	R/W
23:16	ADDRPEN[7:0]	Address Replace Enable These bits select the bits to replace for MSByte of System bus address in memory-mapping mode. 0: No replacement (xSPI frame address field is same as System bus address) 1: Replacement	R/W
31:24	ADDRPCD[7:0]	Address Replace Code These bits configure the code to replace the MSByte of System bus address in memory-mapping mode. It replaces the corresponding bits when Address Replace Enable bit is set to 1.	R/W

Note: S-TYPE-3, P-TYPE-3

This register has functions to configure xSPI Master function.

37.2.1.5 CMCFG1CSn : OSPI Command Map Configuration Register 1 CSn (n = 0, 1)

Base address: OSPI0_B = 0x4026_8000
OSPI0_B_NS = 0x5026_8000

Offset address: 0x014 + 0x010 × n

Bit position:	31											20			16	15														0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	RDLATE[4:0]				RDCMD[15:0]														
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	RDCMD[15:0]	Read command These bits configure the command field of read transaction in memory-mapping mode. Normal format and 8D-8D-8D profile 2.0 format use only upper 1 byte. 8D-8D-8D profile 1.0 format uses 2 bytes.	R/W
20:16	RDLATE[4:0]	Read latency cycle These bits configure the latency cycle of read transaction in memory-mapping mode. 0x00: No latency 0x01: 1 cycle ⋮ 0x08: 8 cycle (default) ⋮ 0x1E: 30 cycles 0x1F: 31 cycles Others: Setting prohibited	R/W
31:21	—	These bits are read as 0. The write value should be 0.	R/W

Note: S-TYPE-3, P-TYPE-3

This register has functions to configure xSPI Master function.

37.2.1.6 CMCFG2CSn : OSPI Command Map Configuration Register 2 CSn (n = 0, 1)

Base address: OSPI0_B = 0x4026_8000
OSPI0_B_NS = 0x5026_8000

Offset address: 0x018 + 0x010 × n

Bit position:	31											20			16	15														0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	WRLATE[4:0]				WRCMD[15:0]														
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	WRCMD[15:0]	Write command These bits configure the command field of write transaction in memory-mapping mode. Normal format and 8D-8D-8D profile 2.0 format use only upper 1 byte. 8D-8D-8D profile 1.0 format uses 2 bytes.	R/W
20:16	WRLATE[4:0]	Write latency cycle These bits configure the latency cycle of write transaction in memory-mapping mode. 0x00: No latency 0x01: 1 cycle ⋮ 0x08: 8 cycle (default) ⋮ 0x1E: 30 cycles 0x1F: 31 cycles Others: Setting prohibited	R/W
31:21	—	These bits are read as 0. The write value should be 0.	R/W

Note: S-TYPE-3, P-TYPE-3

This register has functions to configure xSPI Master function.

37.2.1.7 LIOCFGCSn : OSPI Link I/O Configuration Register CSn (n = 0, 1)

Base address: OSPI0_B = 0x4026_8000
OSPI0_B_NS = 0x5026_8000

Offset address: 0x050 + 0x004 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	DDRSMPEX[3:0]				SDRSMPSFT[3:0]				SDRSMPMD	SDRDRV	CSNEGEX	CSASTEX	CSMIN[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	WRMSKMD	LATEMD	PRTMD[9:0]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
9:0	PRTMD[9:0]	Protocol mode These bits configure the protocol mode and the pin to sample data inputs. In case of using not SPI clock but Data strobe for sampling in SDR mode, it is required to set PRTMD[9] to 1. 0x000: 1S-1S-1S 0x3B2: 4S-4D-4D 0x3FF: 8D-8D-8D 0x048: 1S-2S-2S 0x049: 2S-2S-2S 0x090: 1S-4S-4S 0x092: 4S-4S-4S Others: Setting prohibited	R/W

<table>
<tr><th>Bit</th><th>Symbol</th><th>Function</th><th>R/W</th></tr>
<tr><td>10</td><td>LATEMD</td><td>Latency mode
This bit selects the behavior of initial access latency phase for both direct-manual mode and memory-mapping mode. When set to 0, the latency cycle is equal to each configured cycle from transmitting address field. When set to 1, the latency cycle is incremented from the last byte-pair of Address field and is extended 2 times of each configured cycle depending on OM_DQS port.
It is used only for profile 2.0 frame format of 8D-8D-8D protocol mode with 6 bytes command/address field. Please refer to xSPI protocol for detail.
<table>
<tr><th>Value: Function</th><th>Frame format</th><th>Usage</th></tr>
<tr><td rowspan="2">0: Configurable latency</td><td>profile 2.0</td><td>The configurable latency cycle should be set as minus 1.</td></tr>
<tr><td>Others</td><td>Latency cycle increments after address field.</td></tr>
<tr><td rowspan="2">1: Variable latency</td><td>profile 2.0</td><td>Latency cycle increments from address [23:16]. And it should not be set to 1.</td></tr>
<tr><td>Others</td><td>Not support</td></tr>
</table></td><td>R/W</td></tr>
<tr><td>11</td><td>WRMSKMD</td><td>Write mask mode
This bit selects to use OM_DQS port as write data mask. It could be useful for write access of odd byte.
It is used only for 8D-8D-8D protocol mode.
0: Write mask disable
1: Write mask enable</td><td>R/W</td></tr>
<tr><td>15:12</td><td>—</td><td>These bits are read as 0. The write value should be 0.</td><td>R/W</td></tr>
<tr><td>19:16</td><td>CSMIN[3:0]</td><td>CS minimum idle term
This bit configures the minimum cycle between xSPI frames.
0x0: 1 cycle
0x1: 2 cycles
⋮
0x7: 8 cycles (default)
⋮
0xE: 15 cycles
0xF: 16 cycles
Others: Setting prohibited</td><td>R/W</td></tr>
<tr><td>20</td><td>CSASTEX</td><td>CS asserting extension
This bit extends 1 cycle chip select pins when asserting.
0: No extension
1: Extend 1 cycle</td><td>R/W</td></tr>
<tr><td>21</td><td>CSNEGEX</td><td>CS negating extension
This bit extends 1 cycle chip select pins when negating.
0: No extension
1: Extend 1 cycle</td><td>R/W</td></tr>
<tr><td>22</td><td>SDRDRV</td><td>SDR driving timing
This bit configures the timing of data output in SDR.
This bit should not be set to 1 in case of no latency cycle. Because OSPI output data could be conflicted with OSPI input data.
0: Drive at 1/2 cycle before CK rising-edge
1: Drive at CK rising-edge</td><td>R/W</td></tr>
<tr><td>23</td><td>SDRSMPMD</td><td>SDR Sampling mode
This bit selects the edge of sampling in SDR. In DDR, regardless of this setting, it samples OM_SIOn (n = 0 to 7) ports with both edges of OM_DQS.
When set to 1, it samples at rising-edge before falling-edge.
0: Samples data input at falling-edge
1: Samples data input at rising-edge</td><td>R/W</td></tr>
</table>

Bit	Symbol	Function	R/W
27:24	SDRSMPSFT[3:0]	SDR Sampling window shift These bits shift the timing of CK sampling in SDR. In case of using OM_DQS in SDR, there is no influence on the behavior. In case of DDR or using OM_DQS in SDR, it should be set to 0. 0x0: Sample without delay 0x1: Sample at 1 cycle delay ⋮ 0x6: Sample at 6 cycle delay 0x7: Sample at 7 cycle delay Others: Setting prohibited	R/W
31:28	DDRSMPEX[3:0]	DDR sampling window extend These bits configure the cycle of extending the sampling window in DDR. In DDR, the input data is sampled during the expected cycle soon after latency cycle. The input data out of range is ignored. It can be configured depending on OM_DQS propagation delay. 0x0: Expand no cycle 0x1: Expand 1 cycle ⋮ 0x6: Expand 6 cycles 0x7: Expand 7 cycles Others: Setting prohibited	R/W

Note: S-TYPE-3, P-TYPE-3

This register has functions to configure xSPI Master function.

37.2.2 OSPI Control Registers

These registers control xSPI Master function.

37.2.2.1 BMCTL0 : OSPI Bridge Map Control Register 0

Base address: OSPI0_B = 0x4026_8000
OSPI0_B_NS = 0x5026_8000

Offset address: 0x060

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	CH0CS1ACC[1:0]		CH0CS0ACC[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
1:0	CH0CS0ACC[1:0]	System bus ch0 to slave0 memory area access enable This field enables the access from ch0 to CS0 memory. 0 0: Read/Write disable 0 1: Read enable, Write disable 1 0: Read disable, Write enable 1 1: Read/Write enable	R/W
3:2	CH0CS1ACC[1:0]	System bus ch0 to slave1 memory area access enable This field enables the access from ch0 to CS1 memory. 0 0: Read/Write disable 0 1: Read enable, Write disable 1 0: Read disable, Write enable 1 1: Read/Write enable	R/W
7:4	—	These bits are read as 1. The write value should be 1.	R/W
31:8	—	These bits are read as 0. The write value should be 0.	R/W

Note: S-TYPE-3, P-TYPE-3

This register has functions to control xSPI Master function.

This register shall be configured in the initialization phase. When setting is needed to be changed after beginning xSPI transaction, please stop all communication, see section 37.3.7.2. Flow of Communication Stop before changing the value of BMCTL0.

37.2.2.2 BMCTL1 : OSPI Bridge Map Control Register 1

Base address: OSPI0_B = 0x4026_8000
OSPI0_B_NS = 0x5026_8000

Offset address: 0x064

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	PBUFCLRCH0	—	MWRPUSHCH0	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	—	The write value should be 0.	W
8	MWRPUSHCH0	Memory Write Data Push for ch0 This field requests to push the pending data in combination mode.*1 0: No command 1: Push request	W
9	—	The write value should be 0.	W
10	PBUFCLRCH0	Prefetch Buffer clear for ch0 This field requests to clear the prefetch buffer when the prefetch function is enabled.*1 It should not be set during memory access (COMSTT.MEMACCCH0 = 1). 0: No command 1: Clear request	W
31:11	—	The write value should be 0.	W

Note: S-TYPE-3, P-TYPE-3
Note 1. Prefetch/Combination behavior is not defined when cycle base race condition between asserting these bits and system bus access is occurred.

This register has functions to control xSPI Master function.

37.2.2.3 CMCTLCHn : OSPI Command Map Control register chn (n = 0, 1)

Base address: OSPI0_B = 0x4026_8000
OSPI0_B_NS = 0x5026_8000

Offset address: 0x0068 + 0x004 × n (n = 0, 1)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XIPEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	XIPEXCODE[7:0]								XIPENCODE[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	XIPENCODE[7:0]	XiP mode enter code These bits configure the code to enter XiP mode in memory-mapping mode.	R/W
15:8	XIPEXCODE[7:0]	XiP mode exit code These bits configure the code to exit XiP mode in memory-mapping mode.	R/W
16	XIPEN	XiP mode enable This bit enables XiP mode in memory-mapping mode. When set to 1, XiP enter code is inserted in the latency field, and the command field in next transaction is omitted. When set to 0, XiP exit code is inserted in the latency field. And it is set to 0 automatically when transmitting XiP disable pattern. It should not be used for 8D-8D-8D protocol mode profile 2.0 frame format. 0: Disable XiP mode 1: Enable XiP mode	R/W
31:17	—	These bits are read as 0. The write value should be 0.	R/W

Note: S-TYPE-3, P-TYPE-3

This register has functions to control xSPI Master function.

37.2.2.4 CDCTL0 : OSPI Command Manual Control Register 0

Base address: OSPI0_B = 0x4026_8000
OSPI0_B_NS = 0x5026_8000

Offset address: 0x070

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	PERREP[3:0]				—	—	—	PERITV[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	TRNUM[1:0]		CSSEL	—	PERMD	TRREQ
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TRREQ	Transaction request This bit requests to issue the transaction of manual-command. When set to 1, it starts the transaction. It is cleared to 0 when the transaction completed. The transaction is canceled by clearing to 0 while the transaction is ongoing. 0: No transaction 1: Request transaction	R/W
1	PERMD	Periodic mode This bit enables the periodic transaction mode. When set to 1, it repeats a transaction periodically and compares the read value with the expected value. It alternates the status polling operation for external memory. 0: Direct manual-command mode 1: Periodic manual-command mode	R/W
2	—	This bit is read as 0. The write value should be 0.	R/W
3	CSSEL	Chip select This bit selects a target memory to issue manual-command. 0: CS0 1: CS1	R/W
5:4	TRNUM[1:0]	Transaction number These bits configure the number of transactions in normal manual-command mode. In periodic manual-command, regardless of this setting, the read data of last command is compared. 0 0: Issue 1 command (using command buffer 0) 0 1: Issue 2 commands (using command buffer 0-1) 1 0: Issue 3 commands (using command buffer 0-2) 1 1: Issue 4 commands (using command buffer 0-3)	R/W

Bit	Symbol	Function	R/W
15:6	—	These bits are read as 0. The write value should be 0.	R/W
20:16	PERITV[4:0]	Periodic transaction interval These bits configure the interval of transaction in periodic manual-command mode. Too short interval compared with CPU bus cycle could result in no store into command buffer0. The interval should be longer than 4 times of CPU bus cycle. 0x00: 2 (= 2^1) cycles 0x01: 4 (= 2^2) cycles ⋮ 0x1E: 2,147,483,648 (= 2^{31}) cycles 0x1F: 4,294,967,296 (= 2^{32}) cycles	R/W
23:21	—	These bits are read as 0. The write value should be 0.	R/W
27:24	PERREP[3:0]	Periodic transaction repeat These bits configure the number of transaction repetitions in periodic manual-command mode. 0x0: 1 (= 2^0) time 0x1: 2 (= 2^1) times ⋮ 0xE: 16384 (= 2^{14}) times 0xF: 32768 (= 2^{15}) times	R/W
31:28	—	These bits are read as 0. The write value should be 0.	R/W

Note: S-TYPE-3, P-TYPE-3

This register has functions to control xSPI Master function.

37.2.2.5 CDCTL1 : OSPI Command Manual Control Register 1

Base address: OSPI0_B = 0x4026_8000
OSPI0_B_NS = 0x5026_8000

Offset address: 0x074

Bit position:	31																												0
Bit field:	PEREXP[31:0]																												
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	PEREXP[31:0]	Periodic transaction expected value These bits configure the expected value to compare with the read value in periodic manual-command mode. For example, in case of comparing 1 byte, the lower byte should be configured.	R/W

Note: S-TYPE-3, P-TYPE-3

This register has functions to control xSPI Master function.

37.2.2.6 CDCTL2 : OSPI Command Manual Control Register 2

Base address: OSPI0_B = 0x4026_8000
OSPI0_B_NS = 0x5026_8000

Offset address: 0x078

Bit position:	31																												0
Bit field:	PERMSK[31:0]																												
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	PERMSK[31:0]	Periodic transaction masked value These bits configure the masked value for the expected value in periodic manual-command mode. When set 1 to any bit, the corresponding bit configured as expected value (CDCTL1.PEREXP[31:0]) is ignored. In 8D-8D-8D, the data bytes are transferred only in byte pairs on xSPI bus. It means the dummy read data could be stored. It should be masked for unused bits. For example, in case of read lower 1 byte, it should be configured to 0xFFFFFF00.	R/W

Note: S-TYPE-3, P-TYPE-3

This register has functions to control xSPI Master function.

37.2.2.7 CDTBUFn : OSPI Command Manual Type Buf n (n = 0 to 3)

Base address: OSPI0_B = 0x4026_8000
OSPI0_B_NS = 0x5026_8000

Offset address: 0x080 + 0x010 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	CMD[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	TRTYPE	—	LATE[4:0]					DATASIZE[3:0]				ADDSIZE[2:0]			CMDSIZE[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	CMDSIZE[1:0]	Command Size These bits configure the size of command field. In case of 8D-8D-8D, it should be fixed to 10b. It should not be configured both command size and address size to zero. 0 0: 0 bytes (No command phase) 0 1: 1 byte 1 0: 2 bytes Others: Setting prohibited	R/W
4:2	ADDSIZE[2:0]	Address size These bits configure the size of address field. 0 0 0: 0 bytes (No address phase) 0 0 1: 1 byte 0 1 0: 2 bytes 0 1 1: 3 bytes 1 0 0: 4 bytes Others: Setting prohibited	R/W
8:5	DATASIZE[3:0]	Write/Read Data Size These bits configure the size of data field. In 8D-8D-8D, the data bytes are transferred only in byte pairs on xSPI bus. For example, even if configuring 1 byte for read, 2 bytes data is received. The last byte should be ignored. The 0 bytes must not configured for read transaction. 0x0: 0 bytes (No data phase) 0x1: 1 byte ⋮ 0x7: 7 bytes 0x8: 8 bytes Others: Setting prohibited	R/W

Bit	Symbol	Function	R/W
13:9	LATE[4:0]	Latency cycle These bits configure the latency cycle in manual-command mode. 0x0: No latency 0x1: 1 cycle ⋮ 0x1E: 30 cycles 0x1F: 31 cycles	R/W
14	—	This bit is read as 0. The write value should be 0.	R/W
15	TRTYPE	Transaction Type This bit selects the type of transaction. 0: Read transaction (Readout data from slave device) 1: Not read transaction	R/W
31:16	CMD[15:0]	Command (1-2 bytes) These bits configure the command field in manual-command mode. The number of bytes configured in Command Size bit is transferred. 1S-1S-1S, 4S-4D-4D: CMD[15:8] is command field, CMD[7:0] is not used. 8D-8D-8D profile 1.0: CMD[15:8] is command field, CMD[7:0] is extension field. 8D-8D-8D profile 2.0: CMD[15:0] is upper 2 bytes of command & modifier field. (bit 47-32 in xSPI protocol)	R/W

Note: S-TYPE-3, P-TYPE-3

This register has functions to control xSPI Master function.

37.2.2.8 CDABUFn : OSPI Command Manual Address Buf n (n = 0 to 3)

Base address: OSPI0_B = 0x4026_8000
OSPI0_B_NS = 0x5026_8000

Offset address: 0x084 + 0x10 × n

Bit position:	31																													0
Bit field:	ADD[31:0]																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	ADD[31:0]	Address These bits configure the address field in manual-command mode. 1S-1S-1S, 4S-4D-4D, 8D-8D-8D profile 1.0: It is address field. 8D-8D-8D profile 2.0: It is lower 4 bytes of command & modifier field. (bit 31-0 in xSPI protocol)	R/W

Note: S-TYPE-3, P-TYPE-3

This register has functions to control xSPI Master function.

37.2.2.9 CDD0BUFn : OSPI Command Manual Data 0 Buf n (n = 0 to 3)

Base address: OSPI0_B = 0x4026_8000
OSPI0_B_NS = 0x5026_8000

Offset address: 0x088 + 0x10 × n

Bit position:	31																													0
Bit field:	DATA[31:0]																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	DATA[31:0]	Write/Read Data These bits configure the data field in manual-command mode. In case of write transaction, the write data should be configured. In case of read transaction, the read data is stored.	R/W

Note: S-TYPE-3, P-TYPE-3

This register has functions to control xSPI Master function.

37.2.2.10 CDD1BUFn : OSPI Command Manual Data 1 Buf n (n = 0 to 3)

Base address: OSPI0_B = 0x4026_8000
OSPI0_B_NS = 0x5026_8000

Offset address: 0x08C + 0x10 × n

Bit position:	31																												0
Bit field:	DATA[31:0]																												
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	DATA[31:0]	Write/Read Data These bits configure the data field in manual-command mode. In case of write transaction, the write data should be configured. In case of read transaction, the read data is stored.	R/W

Note: S-TYPE-3, P-TYPE-3

This register has functions to control xSPI Master function.

37.2.2.11 LPCTL0 : OSPI Link Pattern Control Register 0

Base address: OSPI0_B = 0x4026_8000
OSPI0_B_NS = 0x5026_8000

Offset address: 0x100

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	XD2VAL	—	—	XD2LEN[4:0]					XD1VAL	—	—	XD1LEN[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	XDPIN[1:0]		CSSEL	—	—	PATREQ
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PATREQ	Pattern request This bit requests to issue the pattern. When set to 1, it starts the pattern. It is cleared to 0 when the pattern completed. 0: No request XiP Disable pattern 1: Request XiP Disable pattern	R/W
2:1	—	These bits are read as 0. The write value should be 0.	R/W
3	CSSEL	Chip select This bit selects a target memory to issue a pattern. 0: slave0 (CS0) 1: slave1 (CS1)	R/W

Bit	Symbol	Function	R/W
5:4	XDPIN[1:0]	XiP Disable pattern pin These bits select the data output pins to transmit XiP Disable pattern. 0 0: 1 pin 0 1: 2 pins 1 0: 4 pins 1 1: 8 pins	R/W
15:6	—	These bits are read as 0. The write value should be 0.	R/W
20:16	XD1LEN[4:0]	XiP Disable pattern 1st phase length These bits select the length of 1st phase in XiP disable pattern. The pattern with zero-length both 1st phase and 2nd phase should not be configured. 0x0: 0 cycles 0x1: 1 cycle ⋮ 0x1E: 30 cycles 0x1F: 31 cycles	R/W
22:21	—	These bits are read as 0. The write value should be 0.	R/W
23	XD1VAL	XiP Disable pattern 1st phase value This bit selects the value of 1st phase in XiP disable pattern. 0: Low drive 1: High drive	R/W
28:24	XD2LEN[4:0]	XiP Disable pattern 2nd phase length These bits select the length of 2nd phase in XiP disable pattern. 0x00: 0 cycles 0x01: 1 cycle ⋮ 0x1E: 30 cycles 0x1F: 31 cycles	R/W
30:29	—	These bits are read as 0. The write value should be 0.	R/W
31	XD2VAL	XiP Disable pattern 2nd phase value This bit selects the value of 2nd phase in XiP disable pattern. 0: Low drive 1: High drive	R/W

Note: S-TYPE-3, P-TYPE-3

This register has functions to control xSPI Master function.

37.2.2.12 LPCTL1 : OSPI Link Pattern Control Register 1

Base address: OSPI0_B = 0x4026_8000
OSPI0_B_NS = 0x5026_8000

Offset address: 0x104

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	RSTSU[2:0]			—	RSTWID[2:0]			—	—	RSTREP[1:0]		CSSEL	—	PATREQ[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	PATREQ[1:0]	Pattern request These bits request to issue the pattern. When set to 01b or 10b, it starts the pattern. It is cleared to 00b when the pattern completed. 0 0: No request 0 1: Request Reset pattern 1 0: Request CS only pattern 1 1: Setting prohibited	R/W
2	—	This bit is read as 0. The write value should be 0.	R/W
3	CSSEL	Chip select This bit selects a target memory to issue a pattern. 0: slave0 (CS0) 1: slave1 (CS1)	R/W
5:4	RSTREP[1:0]	Reset pattern repeat These bits select the repeating time to toggle CS from LOW to HIGH. 0 0: 4 times (Specified on Reset Signaling Protocol) 0 1: 5 times 1 0: 6 times 1 1: 7 times	R/W
7:6	—	These bits are read as 0. The write value should be 0.	R/W
10:8	RSTWID[2:0]	Reset pattern width These bits configure the width of cycle in reset pattern and CS only pattern. It toggles CS with the configured cycle. 0 0 0: 2 (= 2^1) cycles 0 0 1: 4 (= 2^2) cycles ⋮ 1 1 0: 128 (= 2^7) cycles 1 1 1: 256 (= 2^8) cycles	R/W
11	—	This bit is read as 0. The write value should be 0.	R/W
14:12	RSTSU[2:0]	Reset pattern data output setup time These bits configure the number of setup cycle for data output based on the edge of CS in reset pattern. It needs enough setup time because xSPI slave samples any data at the rising edge of CS. This cycle of setup time should be less than the cycle of reset pattern width (RSTWID[2:0]). 0 0 0: 1 cycle 0 0 1: 2 cycles ⋮ 1 1 0: 7 cycles 1 1 1: 8 cycles	R/W
31:15	—	These bits are read as 0. The write value should be 0.	R/W

Note: S-TYPE-3, P-TYPE-3

This register has functions to control xSPI Master function.

37.2.2.13 LIOCTL : OSPI Link I/O Control Register

Base address: OSPI0_B = 0x4026_8000
OSPI0_B_NS = 0x5026_8000

Offset address: 0x108

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RSTCS0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	WPCS1	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bit	Symbol	Function	R/W
0	—	This bit is read as 1. The write value should be 1.	R/W
1	WPCS1	WP drive for slave1 This bit controls the value of OM_WP1 port. It can be useful only for xSPI slave with write protect port. 0: Drive Low level 1: Drive High level	R/W
15:2	—	These bits are read as 0. The write value should be 0.	R/W
16	RSTCS0	Reset drive This bit controls the value of OM_RESET port. It could be useful only for xSPI slave with reset port. 0: Drive Low level 1: Drive High level	R/W
17	—	This bit is read as 1. The write value should be 1.	R/W
31:18	—	These bits are read as 0. The write value should be 0.	R/W

Note: S-TYPE-3, P-TYPE-3

This register has functions to control xSPI Master function.

37.2.2.14 CCCTL0CSn : OSPI Command Calibration Control Register 0 CSn (n = 0, 1)

Base address: OSPI0_B = 0x4026_8000
OSPI0_B_NS = 0x5026_8000

Offset address: 0x130 + 0x020 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	CASFTEND[4:0]					—	—	—	CASFTSTA[4:0]				
Value after reset:	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	CAITV[4:0]					—	—	—	—	—	—	CANOWR	CAEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CAEN	Automatic Calibration Enable This bit enables the automatic calibration. When set to 1, it transmits the calibration sequence periodically and adjusts the value of phase shift. When set to 0 during the calibration sequence, it stops after completed ongoing calibration sequence, and then this bit is cleared. 0: Disable automatic calibration 1: Enable automatic calibration	R/W
1	CANOWR	Calibration no write mode This bit selects to omit write command in calibration sequence. It can be used for any slave device with fixed calibration pattern data. 0: Calibration sequence with write command 1: Calibration sequence without write command	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W
12:8	CAITV[4:0]	Calibration interval These bits configure the interval between calibration patterns. 0x00: 2 (= 2^1) cycle wait 0x01: 4 (= 2^2) cycle wait ⋮ 0x1E: 2,147,483,648 (= 2^{31}) cycle wait 0x1F: 4,294,967,296 (= 2^{32}) cycle wait	R/W
15:13	—	These bits are read as 0. The write value should be 0.	R/W

Bit	Symbol	Function	R/W
20:16	CASFTSTA[4:0]	Calibration OM_DQS shift start value These bits configure the start value of OM_DQS shift.	R/W
23:21	—	These bits are read as 0. The write value should be 0.	R/W
28:24	CASFTEND[4:0]	Calibration OM_DQS shift end value These bits configure the end value of OM_DQS shift. It should be equal or more than the start value (CASFTSTA[4:0]).	R/W
31:29	—	These bits are read as 0. The write value should be 0.	R/W

Note: S-TYPE-3, P-TYPE-3

This register has functions to control xSPI Master function.

37.2.2.15 CCCTL1CSn : OSPI Command Calibration Control Register 1 CSn (n = 0, 1)

Base address: OSPI0_B = 0x4026_8000
OSPI0_B_NS = 0x5026_8000

Offset address: 0x134 + 0x020 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	CARDLATE[4:0]					—	—	—	CAWRLATE[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	CADATASIZE[3:0]				CAADDSIZE[2:0]			CACMDSIZE[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	CACMDSIZE[1:0]	Command Size These bits configure the size of command field. In case of 8D-8D-8D, it should be fixed to 10b. It should not be configured both command size and address size to zero. 0 0: 0 bytes (No command phase) 0 1: 1 byte 1 0: 2 bytes 1 1: Setting prohibited	R/W
4:2	CAADDSIZE[2:0]	Address size These bits configure the size of address field. 0 0 0: 0 bytes (No address phase) 0 0 1: 1 byte 0 1 0: 2 bytes 0 1 1: 3 bytes 1 0 0: 4 bytes Others: Setting prohibited	R/W
8:5	CADATASIZE[3:0]	Write/Read Data Size These bits configure the size of data field. In 8D-8D-8D, it should be configured with even byte. 0x0: 1 byte 0x1: 2 bytes ⋮ 0xE: 15 bytes 0xF: 16 bytes	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W

Bit	Symbol	Function	R/W
20:16	CAWRLATE[4:0]	Write Latency cycle These bits configure the latency cycle in calibration frame. 0x00: No latency 0x01: 1 cycle ⋮ 0x1E: 30 cycles 0x1F: 31 cycles	R/W
23:21	—	These bits are read as 0. The write value should be 0.	R/W
28:24	CARDLATE[4:0]	Read Latency cycle These bits configure the latency cycle in calibration frame. 0x00: No latency 0x01: 1 cycle ⋮ 0x1E: 30 cycles 0x1F: 31 cycles	R/W
31:29	—	These bits are read as 0. The write value should be 0.	R/W

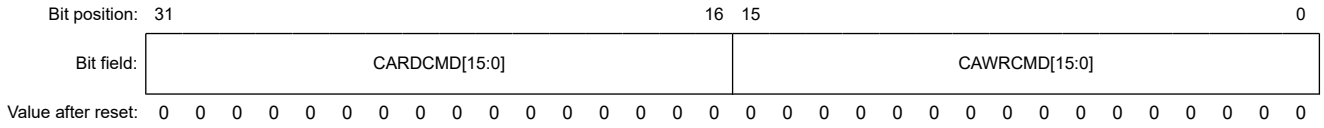
Note: S-TYPE-3, P-TYPE-3

This register has functions to control xSPI Master function. It should be updated while Automatic Calibration Enable is disabled.

37.2.2.16 CCCTL2CSn : OSPI Command Calibration Control Register 2 CSn (n = 0, 1)

Base address: OSPI0_B = 0x4026_8000
OSPI0_B_NS = 0x5026_8000

Offset address: 0x138 + 0x020 × n



Bit	Symbol	Function	R/W
15:0	CAWRCMD[15:0]	Calibration pattern write command These bits configure the calibration pattern write command.	R/W
31:16	CARDCMD[15:0]	Calibration pattern read command These bits configure the calibration pattern read command.	R/W

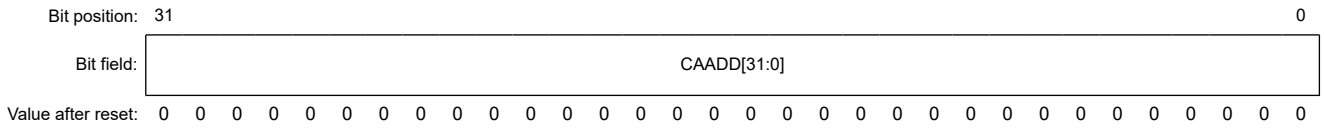
Note: S-TYPE-3, P-TYPE-3

This register has functions to control xSPI Master function. It should be updated while Automatic Calibration Enable is disabled.

37.2.2.17 CCCTL3CSn : OSPI Command Calibration Control Register 3 CSn (n = 0, 1)

Base address: OSPI0_B = 0x4026_8000
OSPI0_B_NS = 0x5026_8000

Offset address: 0x13C + 0x020 × n



Bit	Symbol	Function	R/W
31:0	CAADD[31:0]	Calibration pattern address These bits configure the calibration pattern address.	R/W

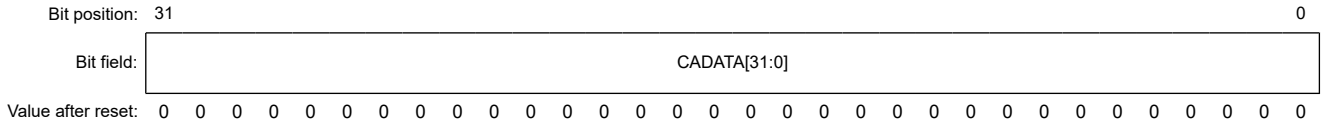
Note: S-TYPE-3, P-TYPE-3

This register has functions to control xSPI Master function. It should be updated while Automatic Calibration Enable is disabled.

37.2.2.18 CCCTL4CSn : OSPI Command Calibration Control Register 4 CSn (n = 0, 1)

Base address: OSPI0_B = 0x4026_8000
OSPI0_B_NS = 0x5026_8000

Offset address: 0x140 + 0x020 × n



Bit	Symbol	Function	R/W
31:0	CADATA[31:0]	Calibration pattern data These bits configure the calibration pattern data.	R/W

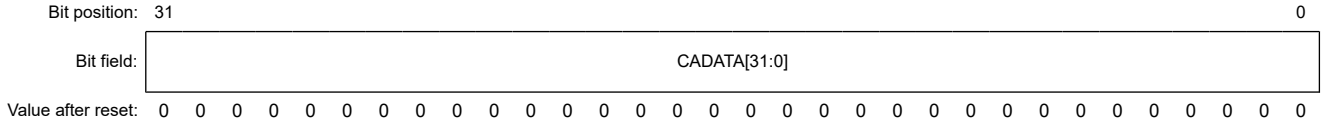
Note: S-TYPE-3, P-TYPE-3

This register has functions to control xSPI Master function. It should be updated while Automatic Calibration Enable is disabled.

37.2.2.19 CCCTL5CSn : OSPI Command Calibration Control Register 5 CSn (n = 0, 1)

Base address: OSPI0_B = 0x4026_8000
OSPI0_B_NS = 0x5026_8000

Offset address: 0x144 + 0x020 × n



Bit	Symbol	Function	R/W
31:0	CADATA[31:0]	Calibration pattern data These bits configure the calibration pattern data.	R/W

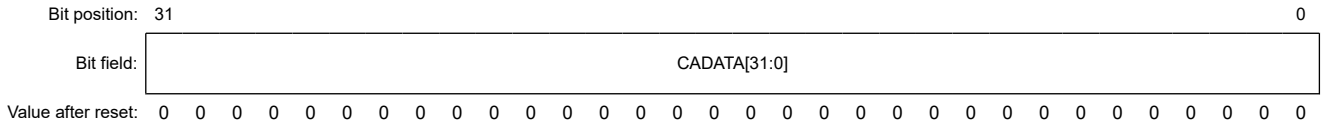
Note: S-TYPE-3, P-TYPE-3

This register has functions to control xSPI Master function. It should be updated while Automatic Calibration Enable is disabled.

37.2.2.20 CCCTL6CSn : OSPI Command Calibration Control Register 6 CSn (n = 0, 1)

Base address: OSPI0_B = 0x4026_8000
OSPI0_B_NS = 0x5026_8000

Offset address: 0x148 + 0x020 × n



Bit	Symbol	Function	R/W
31:0	CADATA[31:0]	Calibration pattern data These bits configure the calibration pattern data.	R/W

Note: S-TYPE-3, P-TYPE-3

This register has functions to control xSPI Master function. It should be updated while Automatic Calibration Enable is disabled.

37.2.2.21 CCCTL7CSn : OSPI Command Calibration Control Register 7 CSn (n = 0, 1)

Base address: OSPI0_B = 0x4026_8000
OSPI0_B_NS = 0x5026_8000

Offset address: 0x14C + 0x020 × n

Bit position:	31																												0
Bit field:	CADATA[31:0]																												
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	CADATA[31:0]	Calibration pattern data These bits configure the calibration pattern data.	R/W

Note: S-TYPE-3, P-TYPE-3

This register has functions to control xSPI Master function. It should be updated while Automatic Calibration Enable is disabled.

37.2.3 OSPI Status Registers

These registers monitor the status of xSPI Master.

37.2.3.1 COMSTT : OSPI Common Status Register

Base address: OSPI0_B = 0x4026_8000
OSPI0_B_NS = 0x5026_8000

Offset address: 0x184

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	RSTOCS1	INTCS1	ECSCS1	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	WRBUFNECH0	—	PBUFNECH0	—	—	—	MEMACCCH0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	MEMACCCH0	Memory access ongoing from ch0 This bit is only valid in the section 37.3.7.2. Flow of Communication Stop and section 37.3.7.6. Flow of Memory-mapping Stop flows. 0: System bus bridge ch0 is not accessing to memory. 1: System bus bridge ch0 is accessing to memory.	R
3:1	—	These bits are read as 0.	R
4	PBUFNECH0	Prefetch Buffer Not Empty for ch0 0: Empty 1: Not empty	R
5	—	This bit is read as 0.	R
6	WRBUFNECH0	Write Buffer Not Empty for ch0 This bit is only valid in the section 37.3.7.2. Flow of Communication Stop and section 37.3.7.6. Flow of Memory-mapping Stop flows. 0: Empty 1: Not empty	R
19:7	—	These bits are read as 0.	R

Bit	Symbol	Function	R/W
20	ECSCS1	ECS monitor for slave1 This bit indicates the value of OM_ECSINT1 port. 0: Low level 1: High level	R
21	INTCS1	INT monitor for slave1 This bit indicates the value of OM_ECSINT1 port. 0: Low level 1: High level	R
22	RSTOCS1	RSTO monitor for slave1 This bit indicates the value of OM_RSTO1 port. 0: Low level 1: High level	R
31:23	—	These bits are read as 0.	R

Note: S-TYPE-3, P-TYPE-3

This register indicates the status of xSPI Master.

37.2.3.2 CASTTCSn : OSPI Calibration Status Register CSn (n = 0, 1)

Base address: OSPI0_B = 0x4026_8000
OSPI0_B_NS = 0x5026_8000

Offset address: 0x188 + 0x004 × n

Bit position:	31																												0
Bit field:	CASUC[31:0]																												
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	CASUC[31:0]	Calibration Success These bits indicate the calibration success for each OM_DQS shift value. It is updated when completed each calibration sequence. CASUC[x] indicates calibration success in OM_DQS shift value = x.	R

Note: S-TYPE-3, P-TYPE-3

This register indicates the status of xSPI Master.

37.2.4 OSPI Interrupt Registers

These registers control the interrupt function of xSPI Master.

37.2.4.1 INTS : OSPI Interrupt Status Register

Base address: OSPI0_B = 0x4026_8000
OSPI0_B_NS = 0x5026_8000

Offset address: 0x190

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	CASUCCS1	CASUCCS0	CAFAILCS1	CAFAILCS0	—	—	—	—	—	—	—	BUSERRCH0	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	INTCS1	—	—	—	ECSCS1	—	—	—	DSTOCS1	DSTOCS0	PERTO	—	PATCMP	CMDCMP
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CMDCMP	Command Completed This bit is set to 1 when completed the requested manual-command. In direct manual-command, it means all transactions completed. In periodic manual-command, it means the read data matches with the expected data. 0: No detection 1: Detection	R
1	PATCMP	Pattern Completed This bit is set to 1 when completed the requested pattern. 0: No detection 1: Detection	R
2	—	This bit is read as 0.	R
3	PERTO	Periodic transaction timeout This bit is set to 1 when the read value does not match with the expected value in periodic manual-command mode. 0: No detection 1: Detection	R
4	DSTOCS0	OM_DQS timeout for slave0 This bit is set to 1 when lost OM_DQS in read transaction with using OM_DQS. It means not receiving the data during expected read phase. In this case, xSPI master stops the read transaction and the following transaction. This error may issue error response to system bus. 0: No detection 1: Detection	R
5	DSTOCS1	OM_DQS timeout for slave1 This function is same as DSTOCS0. 0: No detection 1: Detection	R
8:6	—	These bits are read as 0.	R
9	ECSCS1	ECC error detection for slave1 This bit is set to 1 when detected the falling edge on OM_ECSINT1 port. It can be useful only for xSPI slave with ECC detection function. 0: No detection 1: Detection	R
12:10	—	These bits are read as 0.	R
13	INTCS1	Interrupt detection for slave1 This bit is set to 1 when detected the falling edge on OM_ECSINT1 port. It can be useful only for xSPI slave with interrupt function. 0: No detection 1: Detection	R
19:14	—	These bits are read as 0.	R
20	BUSERRCH0	System bus error for ch0 This bit is set to 1 when an error response occurs on system bus channel0.	R
27:21	—	These bits are read as 0.	R
28	CAFAILCS0	Calibration failed for slave0 This bit is set to 1 when failed calibration. 0: No detection 1: Detection	R
29	CAFAILCS1	Calibration failed for slave1 This function is same as CAFAILCS0. 0: No detection 1: Detection	R
30	CASUCCS0	Calibration success for slave0 This bit is set to 1 when success calibration. 0: No detection 1: Detection	R

Bit	Symbol	Function	R/W
31	CASUCCS1	Calibration success for slave1 This function is same as CASUCCS0. 0: No detection 1: Detection	R

Note: S-TYPE-3, P-TYPE-3

This register indicates the status of interrupt. The bits in this register are cleared to 0 when writing 1 on the corresponding bit of INTC register.

37.2.4.2 INTC : OSPI Interrupt Clear Register

Base address: OSPI0_B = 0x4026_8000
OSPI0_B_NS = 0x5026_8000

Offset address: 0x194

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	CASUCCS1C	CASUCCS0C	CAFAILCS1C	CAFAILCS0C	—	—	—	—	—	—	—	BUSERRCH0C	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	INTCS1C	—	—	—	ECSCS1C	—	—	—	DSTOCS1C	DSTOCS0C	PERTOC	—	PATCMPC	CMDCMPC
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CMDCMPC	Command Completed interrupt clear 0: No change interrupt status 1: Clear interrupt status	W
1	PATCMPC	Pattern Completed interrupt clear 0: No change interrupt status 1: Clear interrupt status	W
2	—	The write value should be 0.	W
3	PERTOC	Periodic transaction timeout interrupt clear 0: No change interrupt status 1: Clear interrupt status	W
4	DSTOCS0C	OM_DQS timeout for slave0 interrupt clear 0: No change interrupt status 1: Clear interrupt status	W
5	DSTOCS1C	OM_DQS timeout for slave1 interrupt clear 0: No change interrupt status 1: Clear interrupt status	W
8:6	—	The write value should be 0.	W
9	ECSCS1C	ECC error detection for slave1 interrupt clear 0: No change interrupt status 1: Clear interrupt status	W
12:10	—	The write value should be 0.	W
13	INTCS1C	Interrupt detection for slave1 interrupt clear 0: No change interrupt status 1: Clear interrupt status	W
19:14	—	The write value should be 0.	W
20	BUSERRCH0C	System bus error for ch0 interrupt clear 0: No change interrupt status 1: Clear interrupt status	W
27:21	—	The write value should be 0.	W

Bit	Symbol	Function	R/W
28	CAFAILCS0C	Calibration failed for slave0 interrupt clear 0: No change interrupt status 1: Clear interrupt status	W
29	CAFAILCS1C	Calibration failed for slave1 interrupt clear 0: No change interrupt status 1: Clear interrupt status	W
30	CASUCCS0C	Calibration success for slave0 interrupt clear 0: No change interrupt status 1: Clear interrupt status	W
31	CASUCCS1C	Calibration success for slave1 interrupt clear 0: No change interrupt status 1: Clear interrupt status	W

Note: S-TYPE-3, P-TYPE-3

This register clears the status of interrupt.

37.2.4.3 INTE : OSPI Interrupt Enable Register

Base address: OSPI0_B = 0x4026_8000
OSPI0_B_NS = 0x5026_8000

Offset address: 0x198

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	CASUCCS1E	CASUCCS0E	CAFAILCS1E	CAFAILCS0E	—	—	—	—	—	—	—	BUSERRCH0E	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	INTCS1E	—	—	—	ECSCS1E	—	—	—	DSTOCS1E	DSTOCS0E	PERTOE	—	PATCMPE	CMDCMPE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CMDCMPE	Command Completed interrupt enable 0: Disabled 1: Enabled	R/W
1	PATCMPE	Pattern Completed interrupt enable 0: Disabled 1: Enabled	R/W
2	—	This bit is read as 0. The write value should be 0.	R/W
3	PERTOE	Periodic transaction timeout interrupt enable 0: Disabled 1: Enabled	R/W
4	DSTOCS0E	OM_DQS timeout for slave0 interrupt enable 0: Disabled 1: Enabled	R/W
5	DSTOCS1E	OM_DQS timeout for slave1 interrupt enable 0: Disabled 1: Enabled	R/W
8:6	—	These bits are read as 0. The write value should be 0.	R/W
9	ECSCS1E	ECC error detection for slave1 interrupt enable 0: Disabled 1: Enabled	R/W
12:10	—	These bits are read as 0. The write value should be 0.	R/W

Bit	Symbol	Function	R/W
13	INTCS1E	Interrupt detection for slave1 interrupt enable 0: Disabled 1: Enabled	R/W
19:14	—	These bits are read as 0. The write value should be 0.	R/W
20	BUSERRCH0E	System bus error for ch0 interrupt enable 0: Disabled 1: Enabled	R/W
27:21	—	These bits are read as 0. The write value should be 0.	R/W
28	CAFAILCS0E	Calibration failed for slave0 interrupt enable 0: Disabled 1: Enabled	R/W
29	CAFAILCS1E	Calibration failed for slave1 interrupt enable 0: Disabled 1: Enabled	R/W
30	CASUCCS0E	Calibration success for slave0 interrupt enable 0: Disabled 1: Enabled	R/W
31	CASUCCS1E	Calibration success for slave1 interrupt enable 0: Disabled 1: Enabled	R/W

Note: S-TYPE-3, P-TYPE-3

This register enables the interrupt.

37.3 Operation

xSPI Master interface has the functions to issue the transaction for external memory with xSPI Slave interface. It allows to write to registers in external memory or read from it.

This xSPI Master mainly has two modes to issue the transaction. One is a manual-command mode; Software configures all fields of xSPI frame and starts the transaction by software request. The other is a memory-mapping mode; it automatically converts system bus for pre-configured memory area into xSPI transaction. It enables to access from system bus to external memory area outside of chip via xSPI bus.

This section describes the xSPI bus operation, the direct control of xSPI frame (manual-command), the control of memory access (memory-mapping), the error operation, and the flow to operation.

37.3.1 xSPI Bus

This section describes the xSPI bus operation.

Figure 37.2 shows an example of connections between OSPI and memory devices.

In this case, OM_CS0 should be connected to the RAM device and OM_CS1 should be connected to the Flash device.

Pull-up resistors should be specified according to the instructions for each device.

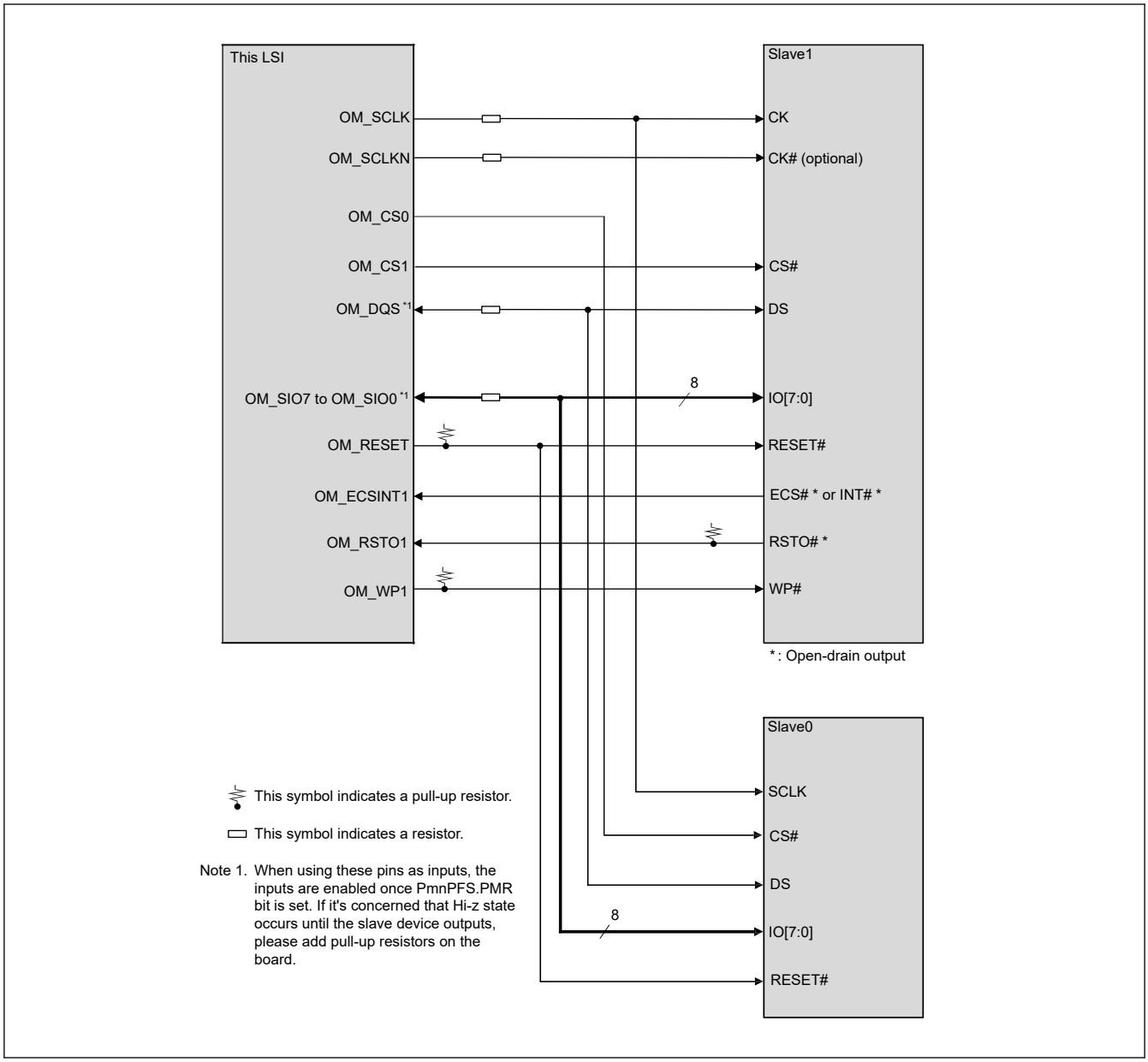


Figure 37.2 Example of Connection between this and memory devices

37.3.1.1 Supported Protocol Mode

This xSPI Master supports various protocol modes. It is configured by Protocol mode bits (LIOCFGCSn.PRTMD[9:0]). Table 37.3 shows the summary of protocol modes.

Table 37.3 Supported protocol mode (1 of 2)

Protocol mode	Function	PRTMD[9:0]	Note
1S-1S-1S	Command, Address and Data field are transferred at SDR with using 1 data input pin and 1 data output pin. Read data is sampled with CK.	0x000	Specified by xSPI protocol
4S-4D-4D	Command field is transferred at SDR with using 4 data pins. Address and Data fields are transferred at DDR with using 4 data pins. Read data is sampled with OM_DQS.	0x3B2	Specified by xSPI protocol
8D-8D-8D	Command, Address and Data fields are transferred at DDR with using 8 data pins. Read data is sampled with OM_DQS.	0x3FF	Specified by xSPI protocol
1S-2S-2S	Command field is transferred at SDR with using 1 data pin. Address and Data fields are transferred at SDR with using 2 data pins. Read data is sampled with CK.	0x048	—

Table 37.3 Supported protocol mode (2 of 2)

Protocol mode	Function	PRTMD[9:0]	Note
2S-2S-2S	Command, Address and Data fields are transferred at SDR with using 2 data pins. Read data is sampled with CK.	0x049	—
1S-4S-4S	Command field is transferred at SDR with using 1 data pin. Address and Data fields are transferred at SDR with using 4 data pins. Read data is sampled with CK.	0x090	—
4S-4S-4S	Command, Address, and Data fields are transferred at SDR with using 4 data pins. Read data is sampled with CK.	0x092	—

Note: In case of XiP mode enable, XiP code is inserted in Latency field. It is valid only for memory-mapping mode.

The bytes of Command and Address fields are transferred in highest order to lowest order sequence. The sequential bytes of Data field are transferred in lowest address to highest address order. In case of using multiple pins, the least significant bit of each byte is placed on OM_SIO0 with each higher order bit on the successively higher numbered OM_SIOn (n = 1 to 7) signals.

Figure 37.3 shows timing-chart for 1S-1S-1S protocol mode. The OM_SIO0 signal is used for output data and the OM_SIO1 signal is used for input data.

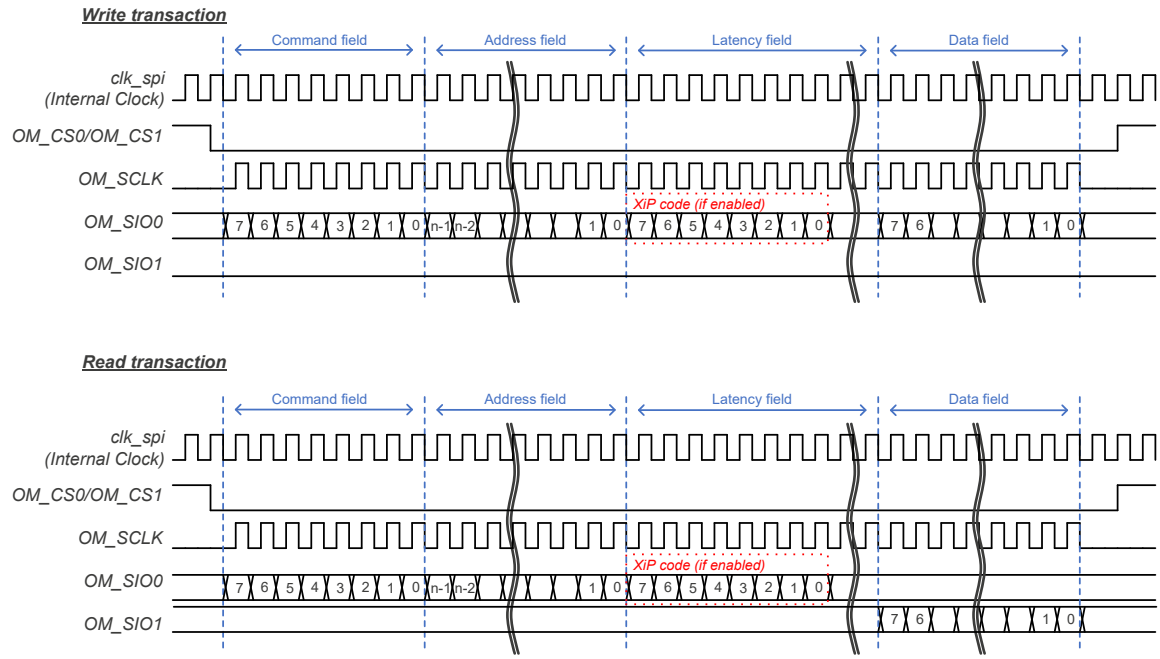


Figure 37.3 1S-1S-1S timing-chart

Figure 37.4 shows timing-chart for 1S-2S-2S protocol mode.

Figure 37.4 1S-2S-2S timing-chart

Figure 37.5 shows timing-chart for 4S-4D-4D protocol mode.

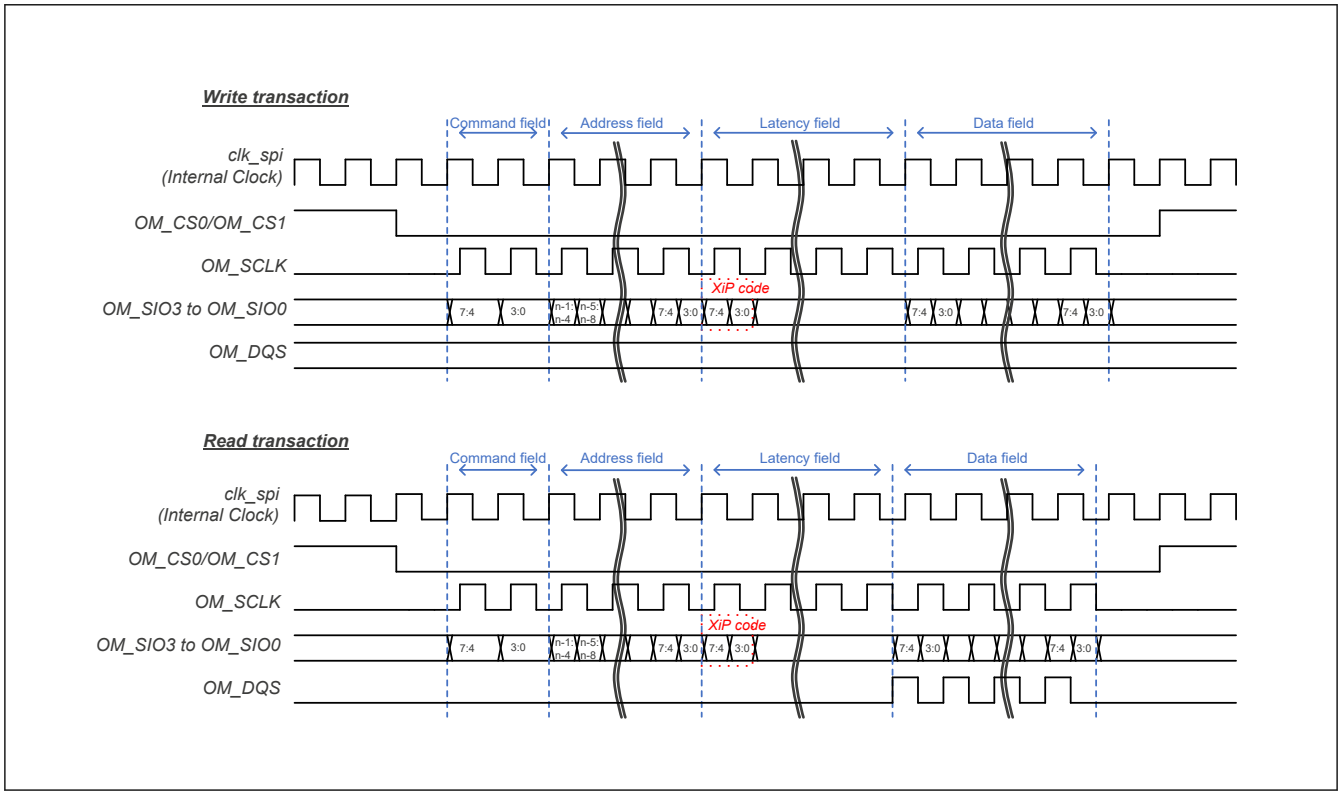


Figure 37.5 4S-4D-4D timing-chart

Figure 37.6 shows timing-chart for 8D-8D-8D profile 1.0 protocol mode. In 8D-8D-8D, the data is always transmitted with byte-pair. In case each field is odd byte, last one byte is padded with invalid data.

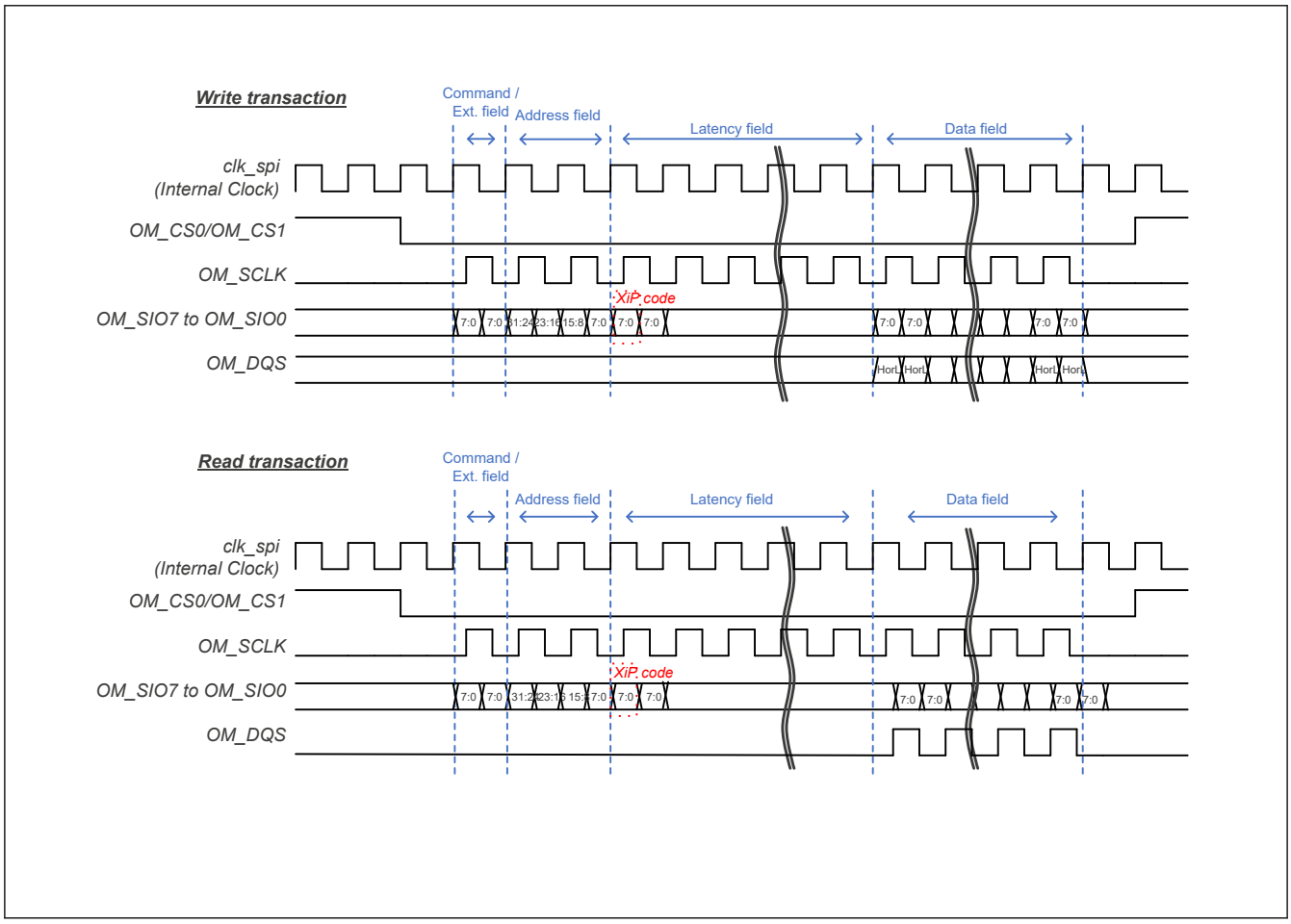


Figure 37.6 8D-8D-8D profile 1.0 timing-chart

Figure 37.7 shows timing-chart for 8D-8D-8D profile 2.0 protocol mode. In 8D-8D-8D, the data is always transmitted with byte-pair. In case each field is odd byte, last one byte is padded with invalid data.

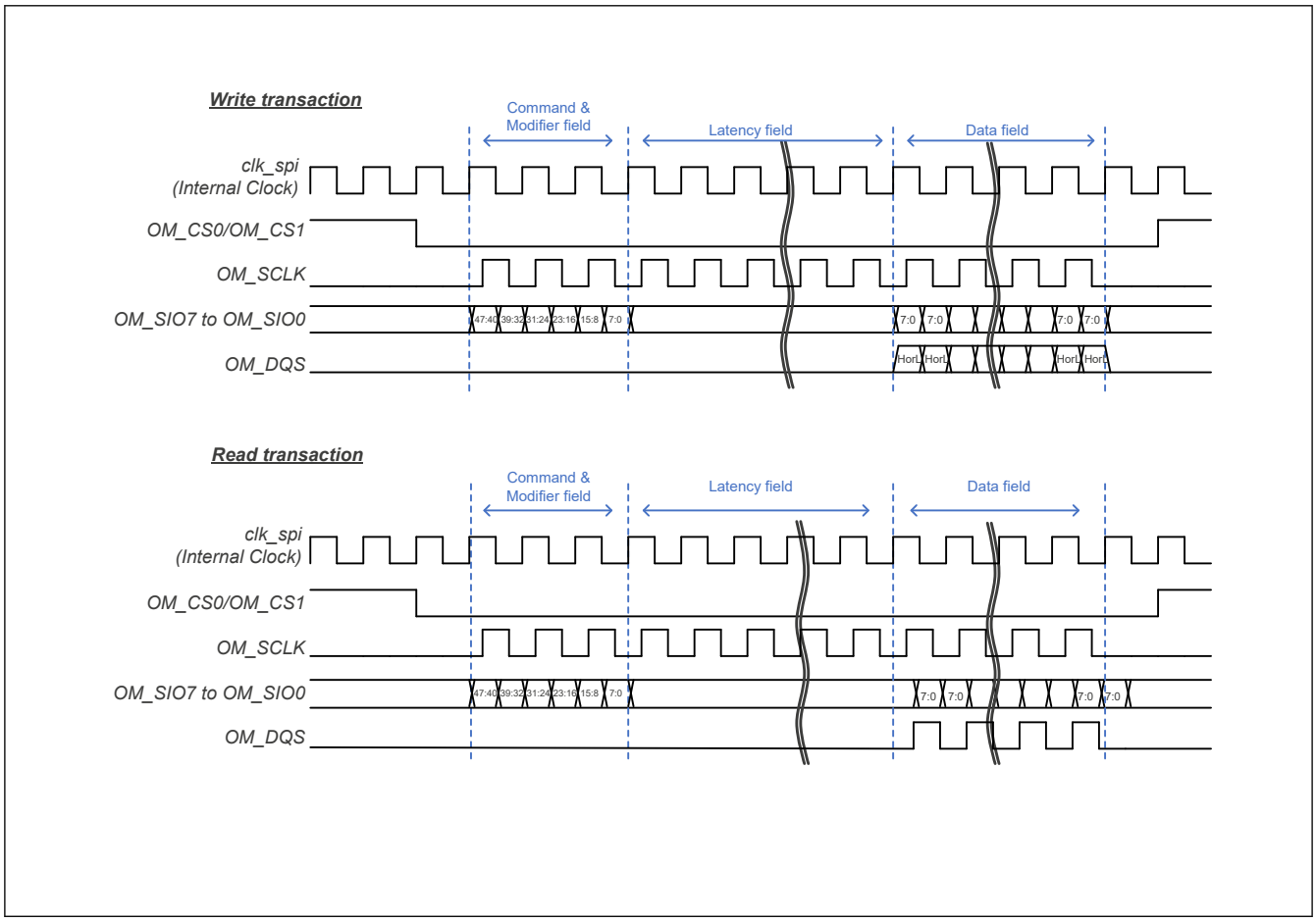


Figure 37.7 8D-8D-8D profile 2.0 timing-chart

37.3.1.2 xSPI Frame Interval

The interval between xSPI frames is configured with CS minimum idle term bits (LIOCFGCSn.CSMIN[3:0]). It depends on the specification of xSPI slave device.

37.3.1.3 OSPI Signals Timing Control

This xSPI Master supports both SDR and DDR. It is possible to sample input data with Data-Strobe (OM_DQS) signal at SDR. For various modes and easy implementation, this xSPI Master could adjust the timing to drive/sample xSPI interface signals statically. Table 37.4 shows the summary of xSPI Interface signal timing control.

Table 37.4 Summary of OSPI signals timing control (1 of 2)

Signal	Mode	Default operation	Timing control (n = 0, 1)
OM_CS0, OM_CS1 drive	—	Asserting 1 cycle before the rising-edge of first OM_SCLK	1 cycle extension for asserting with LIOCFGCSn.CSASTEX bit
		Negating 1.5 cycle after the falling-edge of last OM_SCLK	1 cycle extension for negating with LIOCFGCSn.CSNEGEX bit
OM_SCLK drive	SDR without OM_DQS SDR with OM_DQS	Reference point	—
	DDR with OM_DQS	Reference point	—

Table 37.4 Summary of OSPI signals timing control (2 of 2)

Signal	Mode	Default operation	Timing control (n = 0, 1)
OM_SIOn (n = 0 to 7) output drive	SDR without OM_DQS SDR with OM_DQS	Falling edge of clk_spi (Internal Clock)	0 or 0.5 cycle shift with LIOCFGCSn.SDRDRV bit
	DDR with OM_DQS	Both edges of clk_spi (Internal Clock)	—
OM_SIOn (n = 0 to 7) input sample	SDR without OM_DQS	Falling edge of OM_SCLK on expected data size	0 to 7 cycle shift (1 cycle unit) with LIOCFGCSn.SDRSMPSFT[3:0] bits 0 or 0.5 cycle shift with LIOCFGCSn.SDRSMPMD bit
	SDR with OM_DQS	Falling edge of OM_DQS signal on expected data size	Sample at rising edge with LIOCFGCSn.SDRSMPMD bit 0 to 1 cycle phase shift with WRAPCFG.DSSFTCSn[4:0] bits 0 to 7 cycle extension with LIOCFGCSn.DDRSMPEX[3:0] bits
	DDR with OM_DQS	Both edges of OM_DQS signal on expected data size	0 to 1 cycle phase shift with WRAPCFG.DSSFTCSn[4:0] bits 0 to 7 cycle extension with LIOCFGCSn.DDRSMPEX[3:0] bits

Note: In DDR on xSPI protocol, OM_DQS should be aligned for center of data. It means to shift the phase by 0.25 cycle (90 degrees). This xSPI master supports to adjust this phase depending on the usage conditions.

Figure 37.8 shows the default operation and timing control for SDR without OM_DQS.

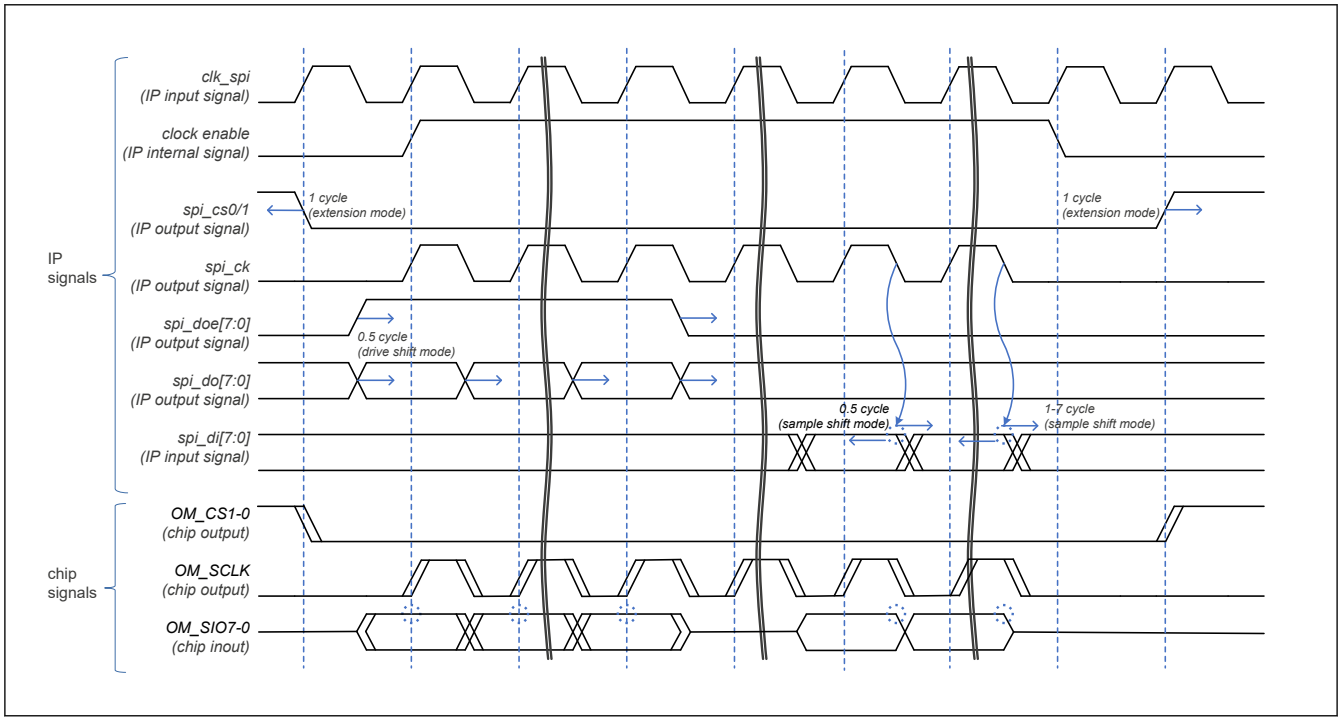


Figure 37.8 Timing control for SDR without OM_DQS

Figure 37.9 shows the default operation and timing control for SDR with OM_DQS.

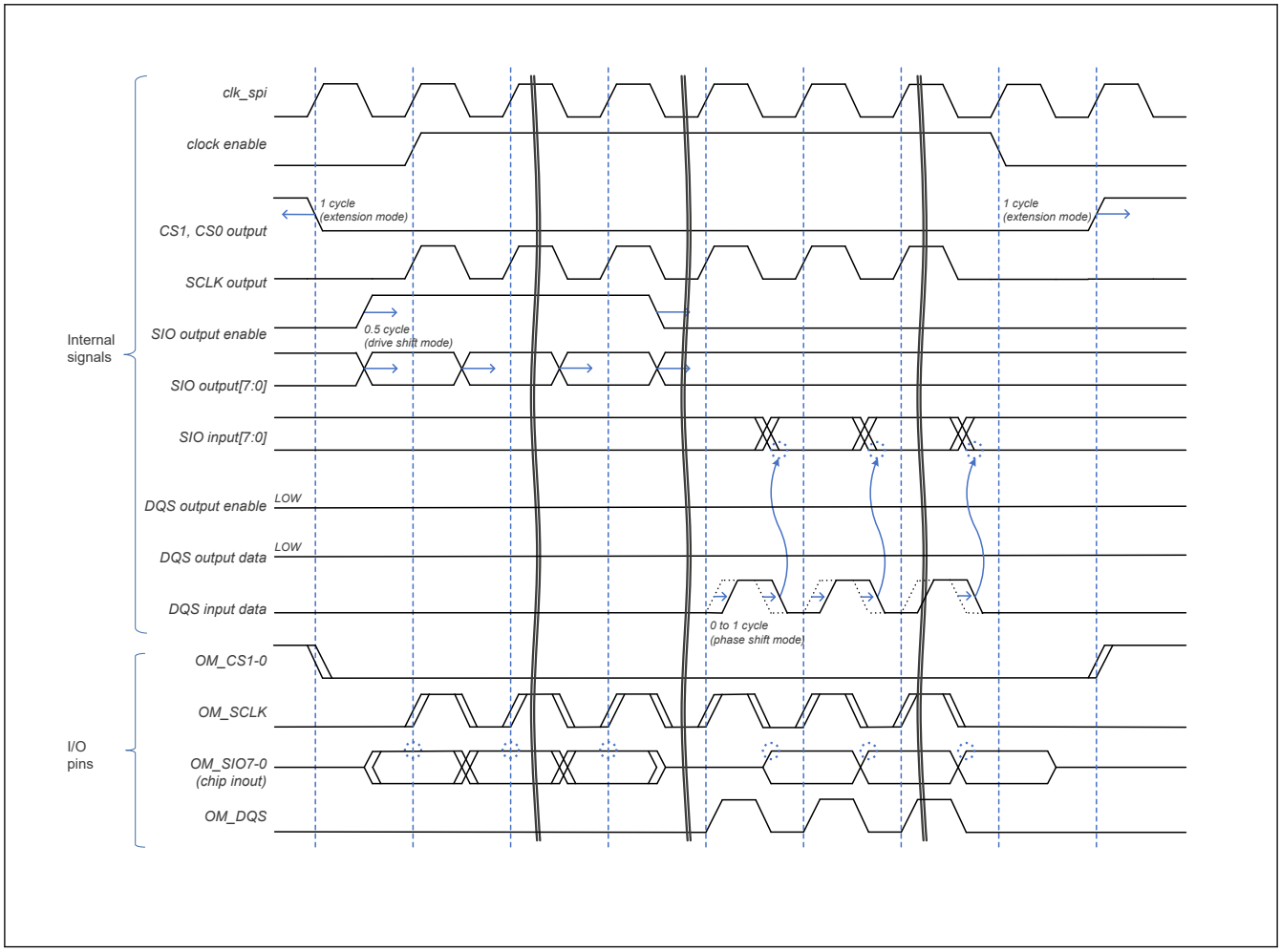


Figure 37.9 Timing control for SDR with OM_DQS

Figure 37.10 shows the default operation and timing control for DDR with OM_DQS.

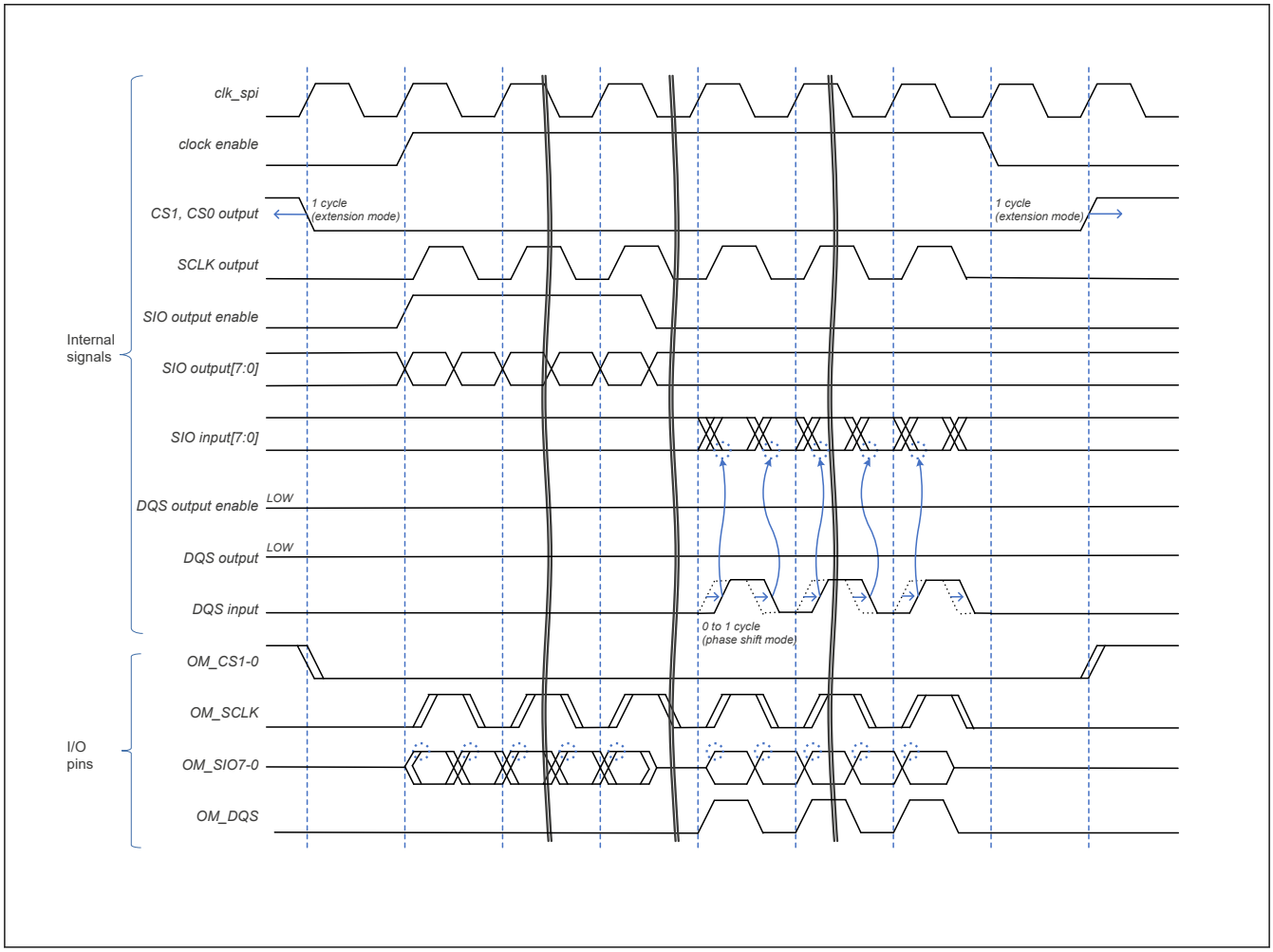


Figure 37.10 Timing control for DDR with OM_DQS

37.3.1.4 Automatic calibration

This xSPI master supports the function to adjust OM_DQS shift value (WRAPCFG.DSSFTCSn (n = 0, 1)) automatically. When this function is enabled (CCCTL0CSn.CAEN = 1), this xSPI master transmits the calibration sequence periodically and adjusts the value of phase shift.

When all read compare is mismatched in read transaction during the calibration sequence, the calibration fail bit (INTS.CAFAILCSn = 1 (n = 0, 1)) is asserted and OM_DQS shift value is not updated. When at least one read compare is matched, the calibration success bit (INTS.CASUCCSn = 1 (n = 0, 1)) is asserted and OM_DQS shift value is updated. The result of each OM_DQS shift value is monitored by Calibration Status register (CASTTCSn). Figure 37.11 shows automatic calibration.

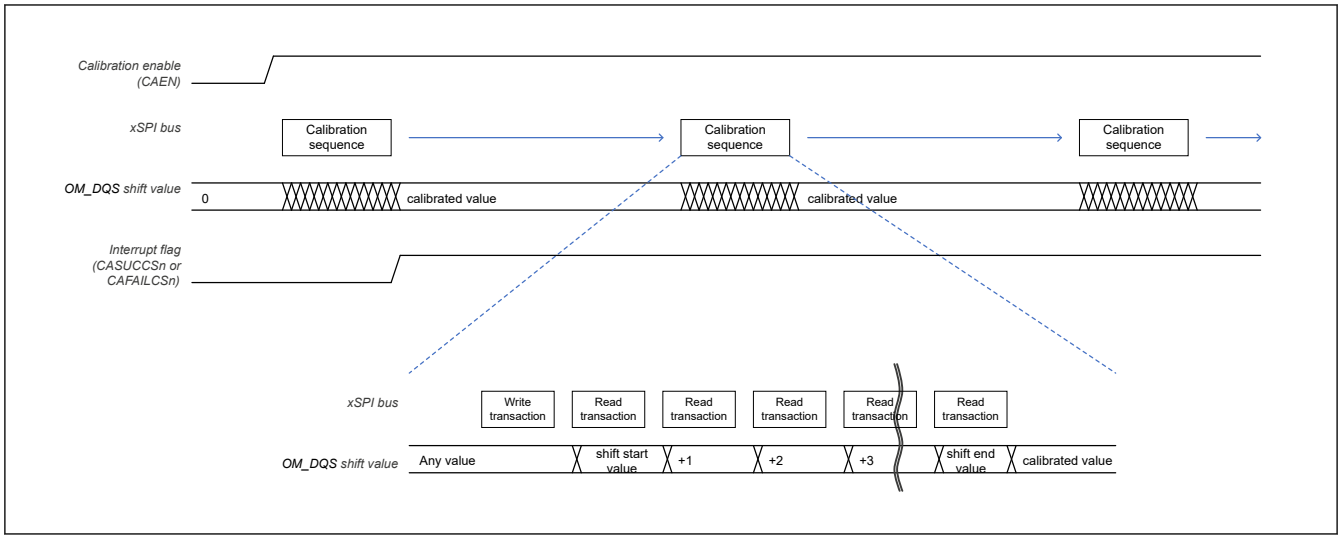


Figure 37.11 Automatic calibration

37.3.2 Manual-command

This section describes the manual-command mode. The manual-command has two functional modes: direct mode and periodic mode.

37.3.2.1 Direct Mode

This mode sequentially can issue up to four xSPI transactions configured and requested by Software. A series of transaction can be issued by a transaction request (CDCTL0.TRREQ = 1 with PERMD = 0). The number of transactions (CDCTL0.TRNUM[1:0]) can be configured up to 4. It can be used to change the mode or read the status of xSPI slave device.

Table 37.5 shows the configured register bits for direct manual-command. The operating flow is illustrated in Figure 37.25.

Table 37.5 Manual-command configuration for direct mode

Transaction	Transaction type	Command	Command size	Address	Address size	Data (x = 0, 1)	Data size	Latency cycle
1st Transaction	CDTBUF0.TRTYPE	CDTBUF0.CMD[15:0]	CDTBUF0.CMDSIZE[1:0]	CDABUF0.ADD[31:0]	CDTBUF0.ADDSIZE[2:0]	CDDxBUF0.DATA[31:0]	CDTBUF0.DATASIZE[3:0]	CDTBUF0.LATE[4:0]
2nd Transaction	CDTBUF1.TRTYPE	CDTBUF1.CMD[15:0]	CDTBUF1.CMDSIZE[1:0]	CDABUF1.ADD[31:0]	CDTBUF1.ADDSIZE[2:0]	CDDxBUF1.DATA[31:0]	CDTBUF1.DATASIZE[3:0]	CDTBUF1.LATE[4:0]
3rd Transaction	CDTBUF2.TRTYPE	CDTBUF2.CMD[15:0]	CDTBUF2.CMDSIZE[1:0]	CDABUF2.ADD[31:0]	CDTBUF2.ADDSIZE[2:0]	CDDxBUF2.DATA[31:0]	CDTBUF2.DATASIZE[3:0]	CDTBUF2.LATE[4:0]
4th Transaction	CDTBUF3.TRTYPE	CDTBUF3.CMD[15:0]	CDTBUF3.CMDSIZE[1:0]	CDABUF3.ADD[31:0]	CDTBUF3.ADDSIZE[2:0]	CDDxBUF3.DATA[31:0]	CDTBUF3.DATASIZE[3:0]	CDTBUF3.LATE[4:0]

37.3.2.2 Periodic Mode

This mode periodically issues an xSPI read transaction configured and requested by Software. And it can compare the read value up to 4 bytes with expected value. The transaction is issued by a transaction request (CDCTL0.TRREQ = 1 with PERMD = 1). It can be used to alternate the status polling operation of xSPI slave device.

The periodic term is configured in Periodic transaction interval bits (CDCTL0.PERITV[4:0]). The expected value is configured in Periodic transaction expected and masked value bits (CDCTL1.PEREXP[31:0] and CDCTL2.PERMSK[31:0]). Table 37.6 shows the configured register bits for periodic manual-command. The operating flow is illustrated in Figure 37.26.

Table 37.6 Manual-command configuration for periodic mode

Transaction	Transaction type	Command	Command size	Address	Address size	Data (x = 0, 1)	Data size	Latency cycle
Read Transaction	CDTBUF0. TRTYPE	CDTBUF0. CMD[15:0]	CDTBUF0. CMDSIZE[1:0]	CDABUF0. ADD[31:0]	CDTBUF0. ADDSIZE[2:0]	CDDxBUF0. DATA[31:0]	CDTBUF0. DATASIZE[3:0]	CDTBUF0. LATE[4:0]

37.3.3 Memory-mapping

This section describes the memory-mapping mode. This mode automatically converts system bus access for pre-configured memory area into xSPI transaction.

37.3.3.1 Configuration

In this operation, the payload of address and data field are delivered from system bus signals. The information of command field and size are delivered from the configured register bits. Table 37.7 shows the register bits configured for memory-mapping.

Table 37.7 Memory-mapping configuration for memory area access (n = 0, 1)

System bus Transaction	Format Change mode	Command	Command size	Address	Address size	Data	Data size	Latency cycle
Write for slave n memory area	Normal	CMCFG2CSn. WRCMD[15:8]	1 byte	SAWADDR[x:0]	CMCFG0CSn. ADDSIZE[1:0]	SWDATA	Up to SAWLEN and SAWSIZE	CMCFG2CSn. WRLATE[4:0]
	8D-8D-8D profile 1.0	CMCFG2CSn. WRCMD[15:0]	2 bytes					
	8D-8D-8D profile 2.0 Command Modifier	CMCFG2CSn. WRCMD[15:8]	1 byte	{SAWADDR[27:4], 0000000000000b, SAWADDR[3:1]}	5 bytes			
	8D-8D-8D profile 2.0 Extended Command Modifier	CMCFG2CSn. WRCMD[15:13]	3 bits	{0b, SAWADDR[31:4], 0000000000000b, SAWADDR[3:1]	45 bits			
Read for slave n memory area	Normal	CMCFG1CSn. RDCMD[15:8]	1 byte	SARADDR[x:0]	CMCFG0CSn. ADDSIZE[1:0]	SRDATA	Up to SARLEN and SARSIZE	CMCFG1CSn. RDLATE[4:0]
	8D-8D-8D profile 1.0	CMCFG1CSn. RDCMD[15:0]	2 bytes					
	8D-8D-8D profile 2.0 Command Modifier	CMCFG1CSn. RDCMD[15:8]	1 byte	{SARADDR[27:4], 0000000000000b, SARADDR[3:1]}	5 bytes			
	8D-8D-8D profile 2.0 Extended Command Modifier	CMCFG1CSn. RDCMD[15:13]	3 bits	{0b, SARADDR[31:4], 0000000000000b, SARADDR[3:1]}	45 bits			

Note: The MSByte of Address can be replaced with Address Replace Enable and Code bits (CMCFG0CSn.ADDRPEN[7:0] / ADDRPCD[7:0]).

37.3.3.2 Write Access Operation

At accepting write access for memory area from system bus, this xSPI Master stores all payload data in internal bridge buffer and then issues a write transaction into xSPI slave. Figure 37.12 shows the operation summary.

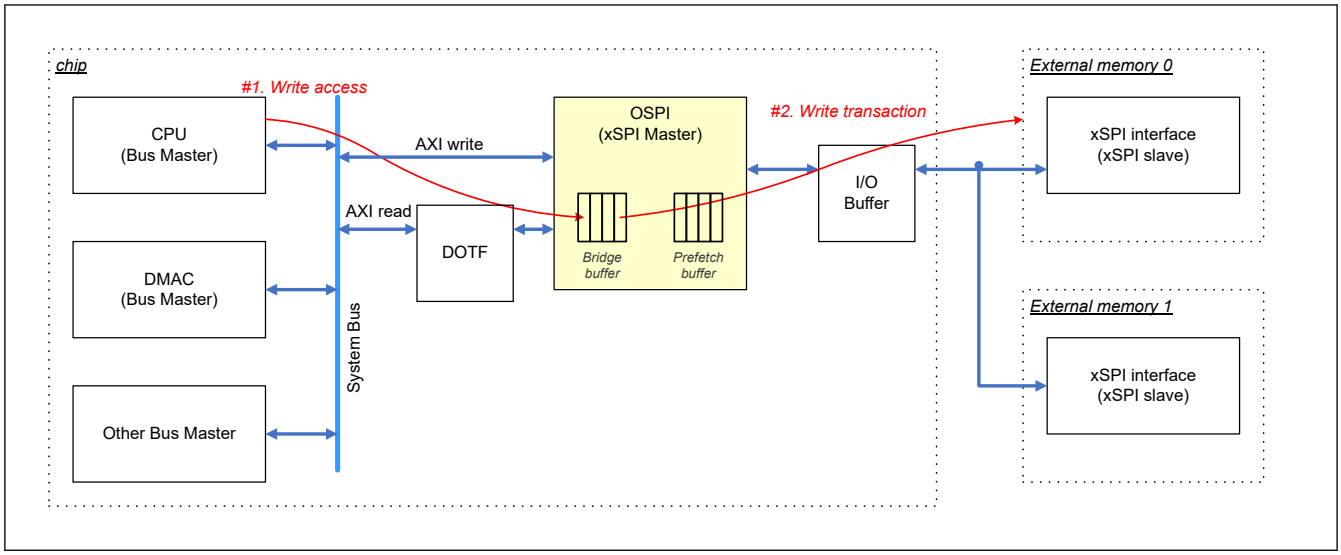


Figure 37.12 Write access for memory area

The operation of xSPI bus changes depending on system bus's burst type. When the burst type is single type or incremental type, one system bus transaction triggers for one xSPI frame. When the burst type is wrap type and the CMCFG0CSn.WPBSTMD is 0, one system bus transaction triggers two xSPI frames. Figure 37.13 shows the relationship between AXI and xSPI frames.

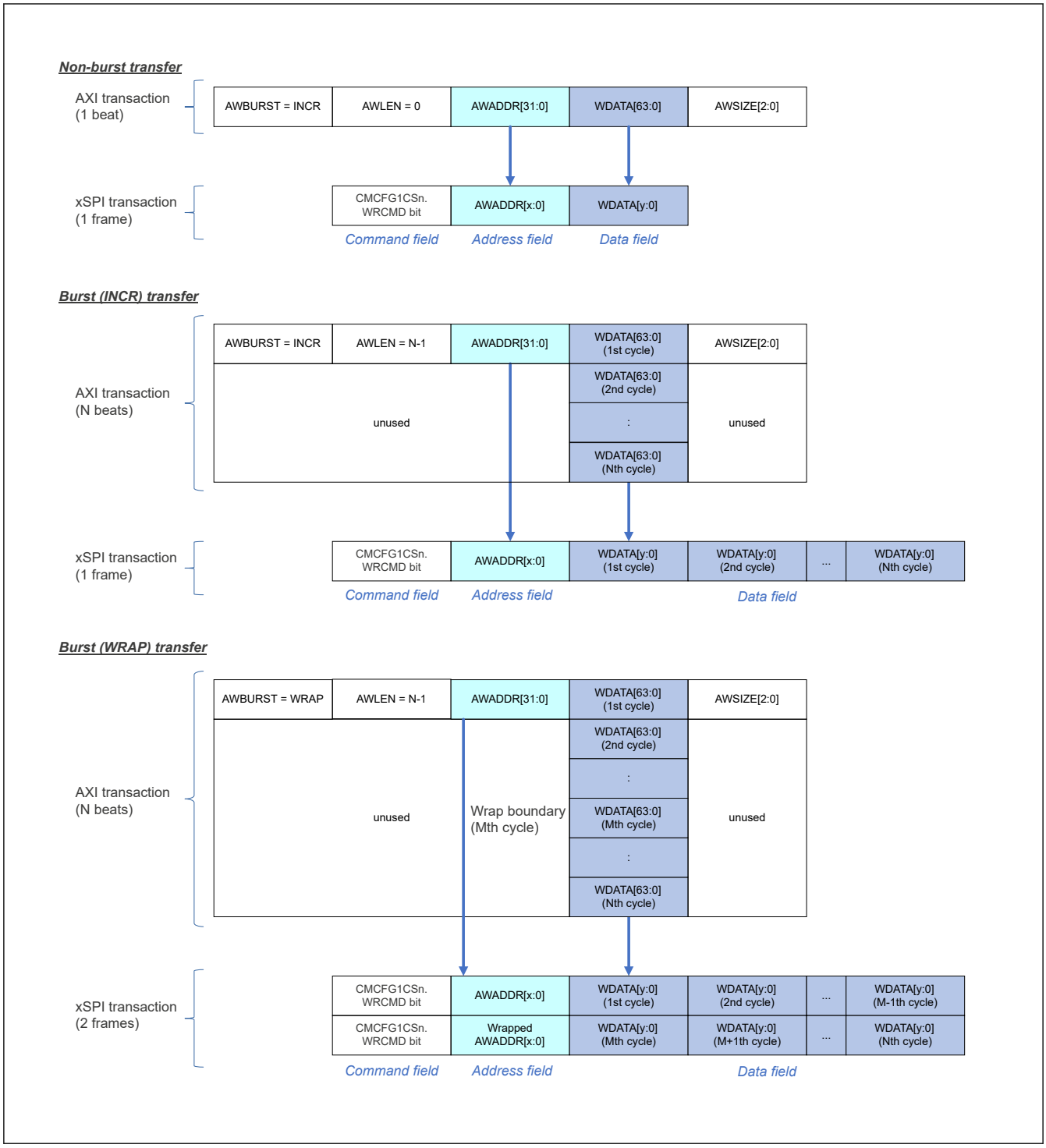


Figure 37.13 xSPI frame format in write access (Normal format)

37.3.3.3 Combination Function

At the system bus write access for memory area, this xSPI master has the function to combinate the write data for high throughput on xSPI bus. When this function is enabled (BMCFGCHn.MWRCOMB = 1), this xSPI master transmits a xSPI frame with the selected size while the sequential address is incremental[*1]. When one of the below conditions is detected, even though not reaching to the target size (BMCFGCHn.MWRSIZE[7:0]), this xSPI master transmits the pending data into xSPI bus.

- Non-incremental address is detected.
- Different burst type is detected.

- Read transaction is detected.
- Access for different slave is detected.
- Memory Write Data Push bit (BMCTL1.MWRPUSHCHn (n = 0, 1)) is set.

This function could be useful for any slave device to request a chunk of data at a time. In the case, system bus master shall continue to provide the fixed data size with incremental address. e.g. there is any device to request to write in page unit.

Figure 37.14 shows the operation when enable the combination function.

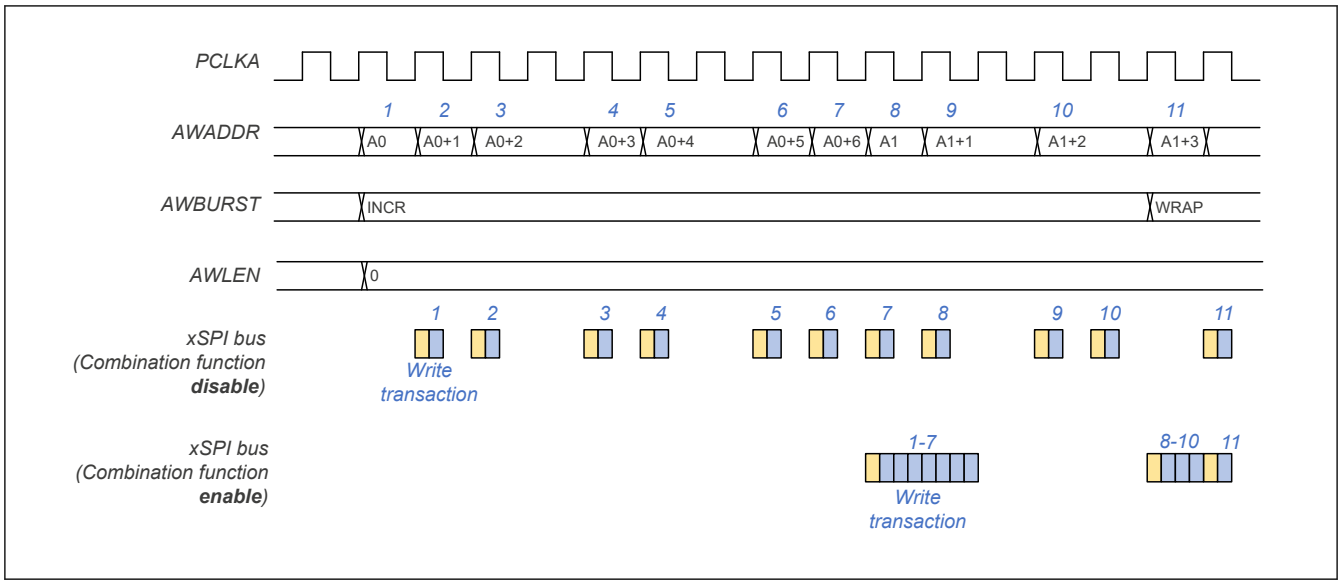


Figure 37.14 Combination function

Note 1. The access which comply all below condition is considered as incremental address.

- Transaction type is INCR.
- The access's start address is continuous to the previous last write address.
  - The access's start position of WSTRB is treated as start address.
  - Previous access's last WSTRB is treated last write address.

Figure 37.15 shows data combined example with AXI access.

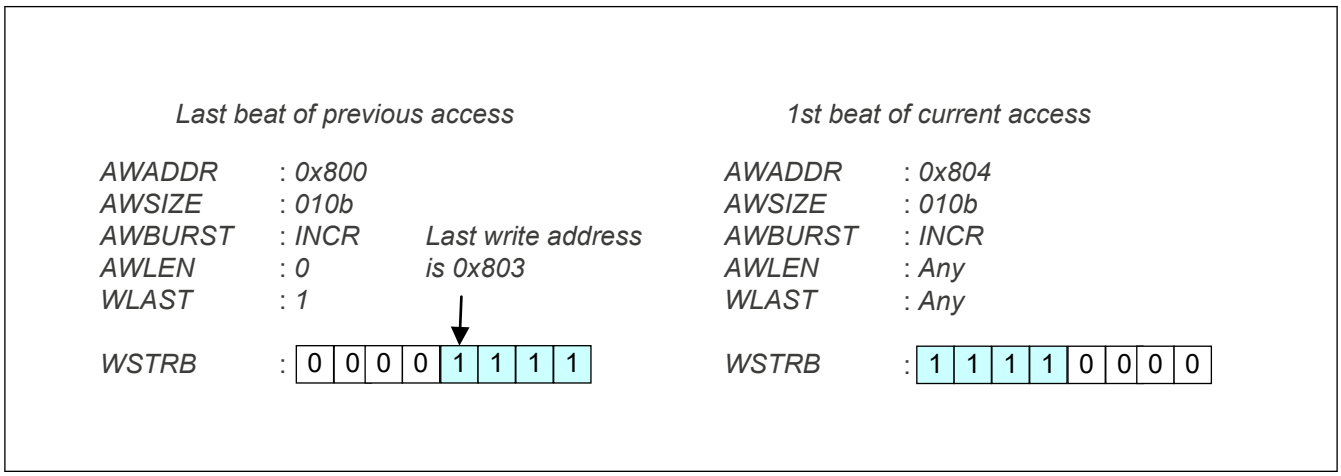


Figure 37.15 Data combined example with AXI access

37.3.3.4 Read Access Operation

At the read access for memory area, soon after detected the read access, this xSPI Master issues a read transaction into xSPI slave. Figure 37.16 shows the operation summary.

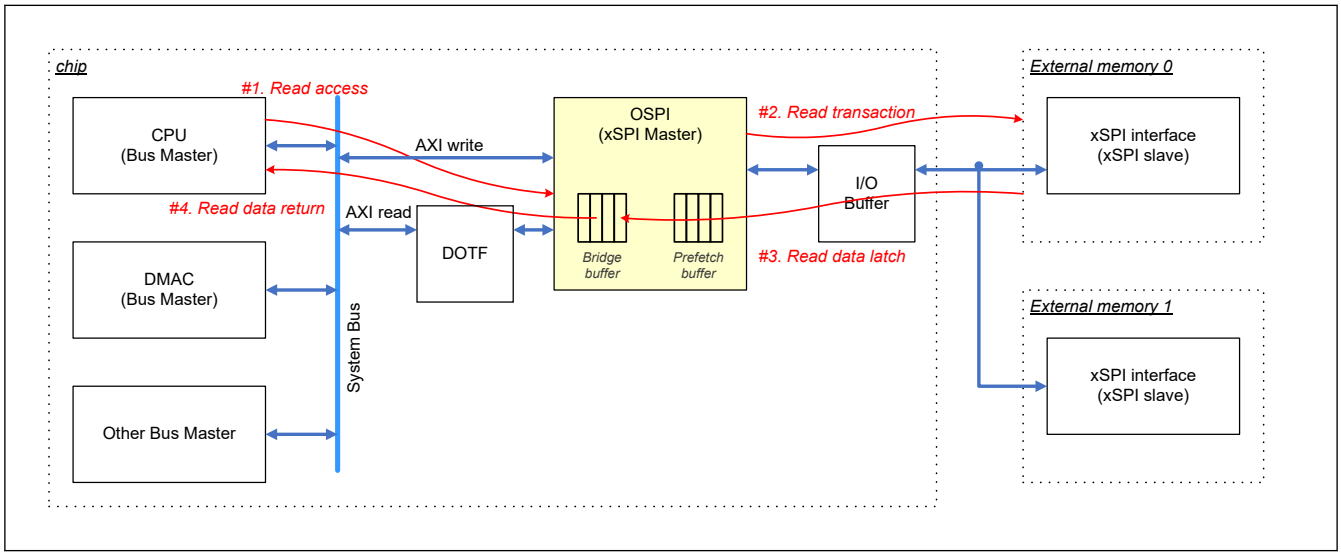


Figure 37.16 Read access for memory area

The operation of xSPI bus changes depending on burst type. When the type is single or increment type, one system bus's read transaction triggers one xSPI frame. When the type is wrap type and the CMCFG0CSn.WPBSTMD is 0, one system bus read transactions triggers two xSPI frames. Figure 37.17 shows the relationship between AXI and xSPI frames.

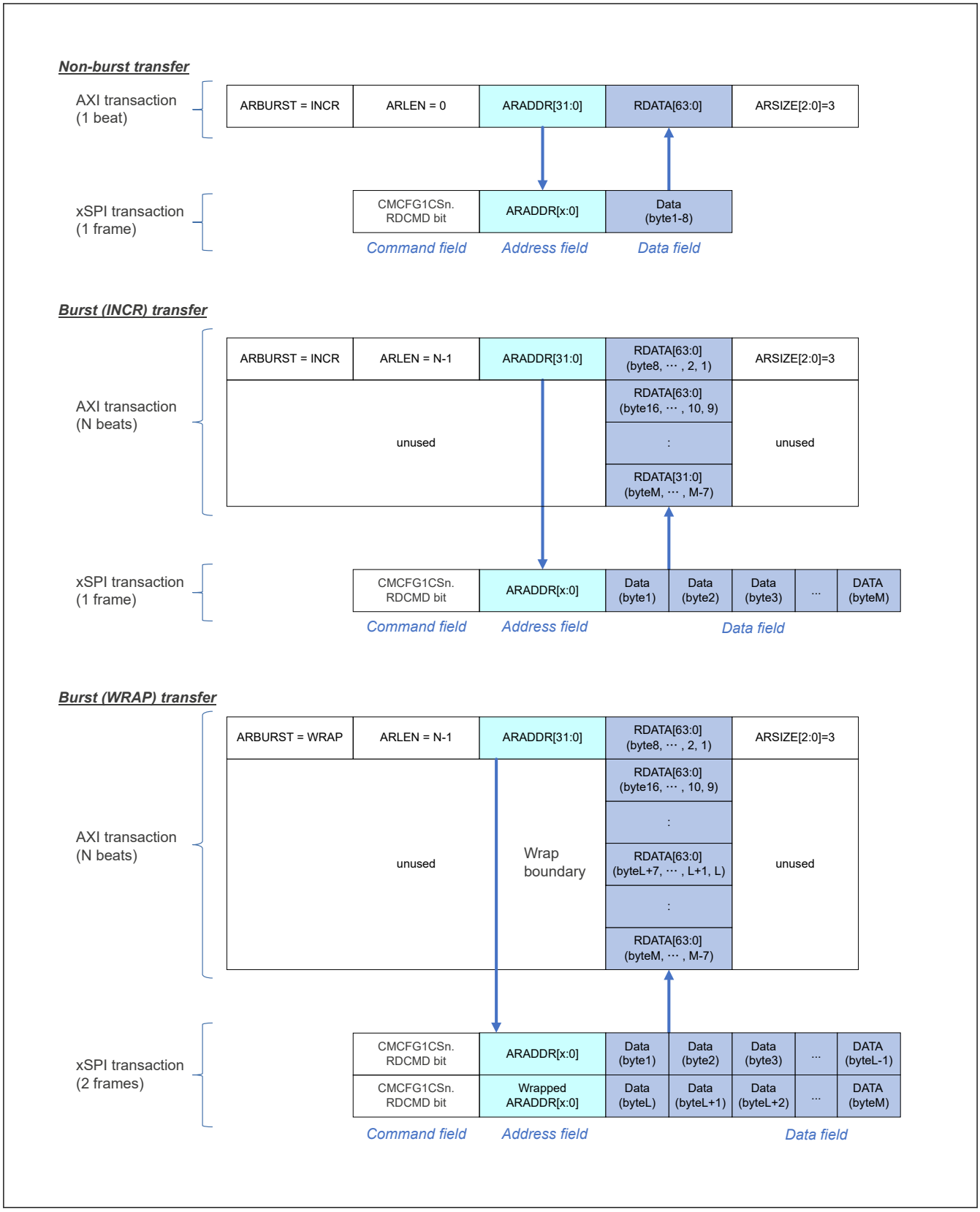


Figure 37.17 xSPI frame format in read access (Normal format)

37.3.3.5 Prefetch Function

At the read access for memory area from system bus, this xSPI Master has the function to prefetch the read data for reducing the latency. When enabled this function (BMCFGCHn.PREEN = 1), this xSPI Master continues to read the

incremental address and store the read data from xSPI slave in internal prefetch buffer. And this xSPI master searches in prefetch buffer for the following read access from system bus. If found the target read data in prefetch buffer, this xSPI Master returns the data from prefetch buffer. If not found, this xSPI Master clears prefetch buffer and newly issues a read transaction into xSPI slave. This function is effective in application such as the consecutive read addresses are close. But it is not effective in application such as the consecutive read addresses are not incremental because xSPI read frame for prefetch uses xSPI bus. Figure 37.18 shows the operation summary.

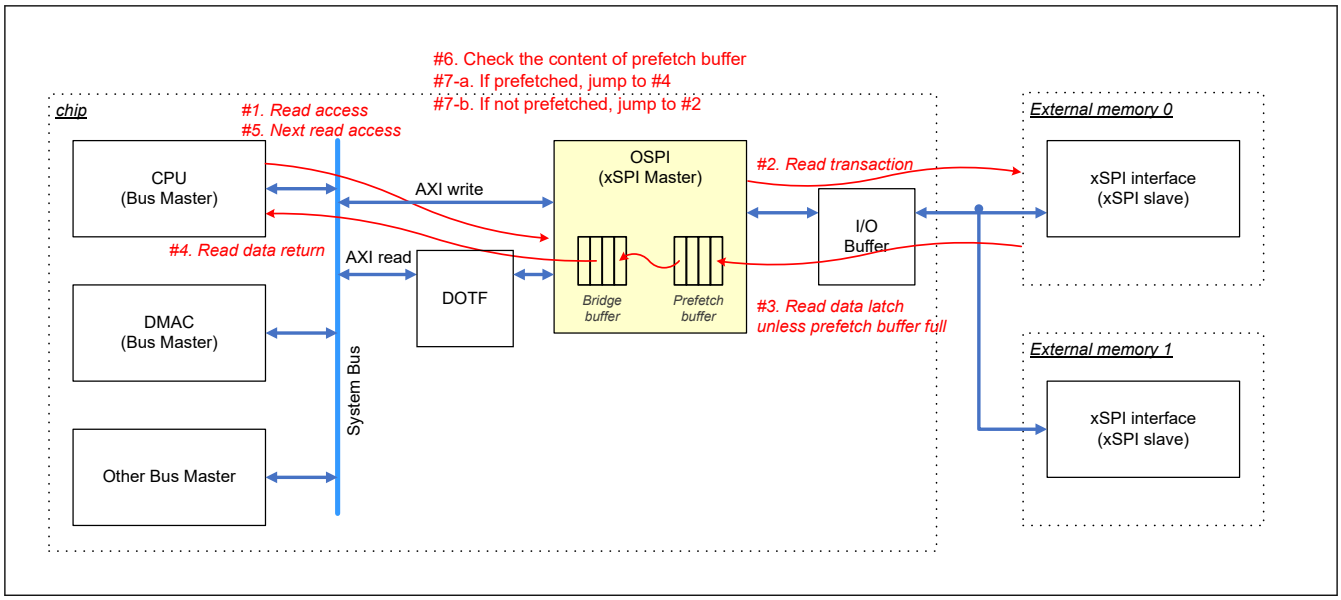


Figure 37.18 Read access for memory area with prefetch enabled

Note: When enabled this prefetch function, Bus Master could read from not a slave device but the internal prefetch buffer. When accessed to the same address from multiple Bus Masters, this xSPI Master does not guarantee to read the latest data. If Bus Master wish to read the latest data from a slave device, it should read after cleared the prefetch buffer (BMCTL1.PBUFCLRCHn (n = 0, 1)).

Note: Prefetch buffer is implemented as FIFO-based, and when read access is issued, the data before the access address is discarded from the buffer. And when next access is issued to the region which is discarded at previous access, this module issues the xSPI read access again to fill the prefetch buffer.

Note: OSPI has the 1line buffer which keeps the last 8Byte read data from prefetch buffer. When read access is issued to the same address to the data in 1line buffer, OSPI returns read data from 1line buffer.

37.3.3.6 XiP Mode

Some slave devices have a mode (XiP mode) in which the command phase is not required for lower latency. While in this mode, the xSPI master skips sending the command and the slave device implicitly performs the command that was executed in the previous transaction. When enabled XiP mode bit (CMCTLCHn.XIPEN = 1), this xSPI master inserts XiP enter code (CMCTLCHn.XIPENCODE[7:0]) in latency field. When disabled XiP mode bit (CMCTLCHn.XIPEN = 0), this xSPI master inserts XiP exit code (CMCTLCHn.XIPEXCODE[7:0]) in latency field. This function is available only for memory-mapping mode.

And when this xSPI master transmits XiP disable pattern, this master clears XiP mode bit and disables XiP mode configured for both channels. Note that it is not possible to disable XiP mode for only one channel by transmitting XiP disable pattern.

Note: When enough latency cycle does not exist for XiP code, this xSPI Master could not insert XiP code.

Note: XiP mode could be used only for unidirectional access to a slave. The write transaction and read transaction should be separated.

Note: The XiP exit code is inserted once when disabled. More details, See Figure 37.30.

37.3.4 Pattern Control

This xSPI Master has the function to transmit 3 type of patterns which is not xSPI frame format. The pattern is triggered by setting trigger bit (LPCTL0-1.PATREQ).

37.3.4.1 XiP Disable Pattern

XiP Disable pattern transmits any pattern with the configured length and value (LPCTL0.XD1LEN[4:0] / XD1VAL / XD2LEN[4:0] / XD2VAL). It uses OM_SCLK, OM_SIO7-0 signals. The number of output pin can be configured by XiP Disable pattern pin bits (LPCTL0.XDPIN[1:0]). It may be used to disable XiP mode for legacy SPI. Figure 37.19 shows the timing-chart.

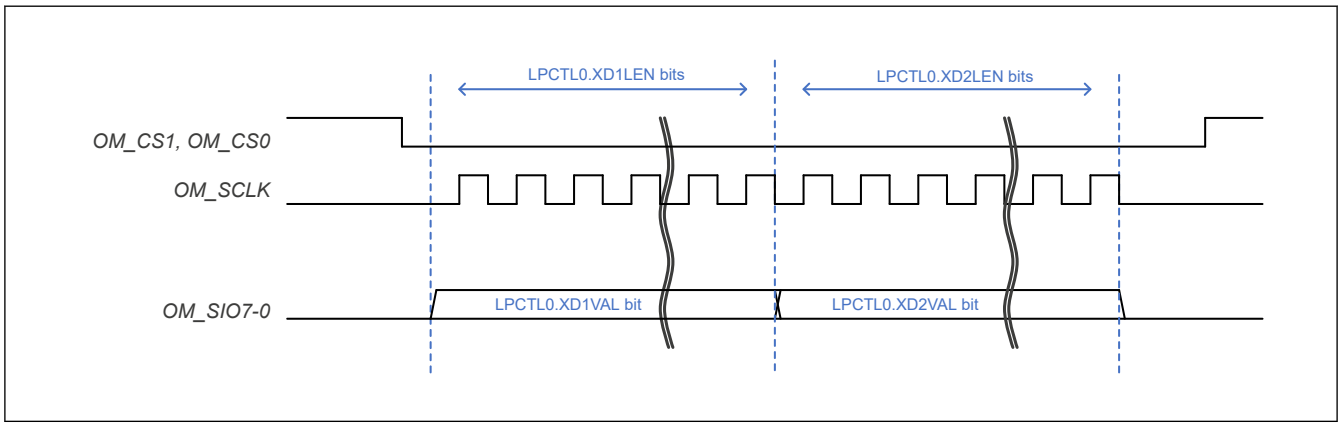


Figure 37.19 XiP Disable pattern

37.3.4.2 Reset Pattern

Reset pattern transmits the pattern specified in Serial Flash Reset Signaling Protocol. Figure 37.20 shows the timing chart.

CS Low/High width is configured with Reset Pattern Length bits (LPCTL1.RSTWID[2:0]). xSPI slave will sample the data input at the rising edge of CS. Setup time for data output is configured with Reset pattern data output setup time bits (LPCTL1.RSTSU[2:0]). The setup time should be less than Reset pattern width always.

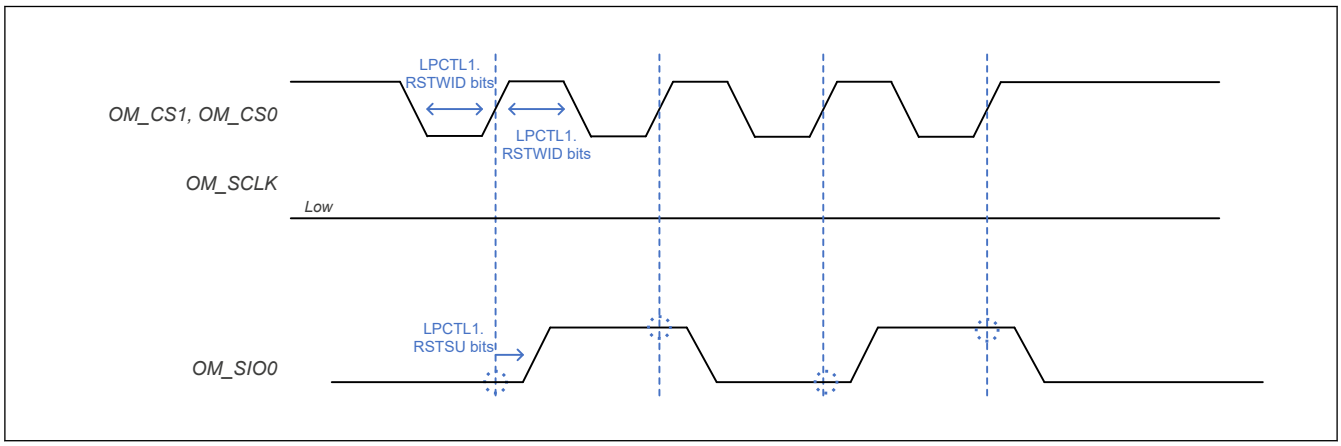


Figure 37.20 Reset pattern

Note: In the protocol, CS Low/High width is defined as minimum 500 ns and Setup time is defined as minimum 6 ns.

37.3.4.3 CS Only Pattern

CS Only pattern activates CS port with the configured length bits (LPCTL1.RSTWID[2:0]). It may be used to resume from Deep Power Down state. Figure 37.21 shows the timing-chart.

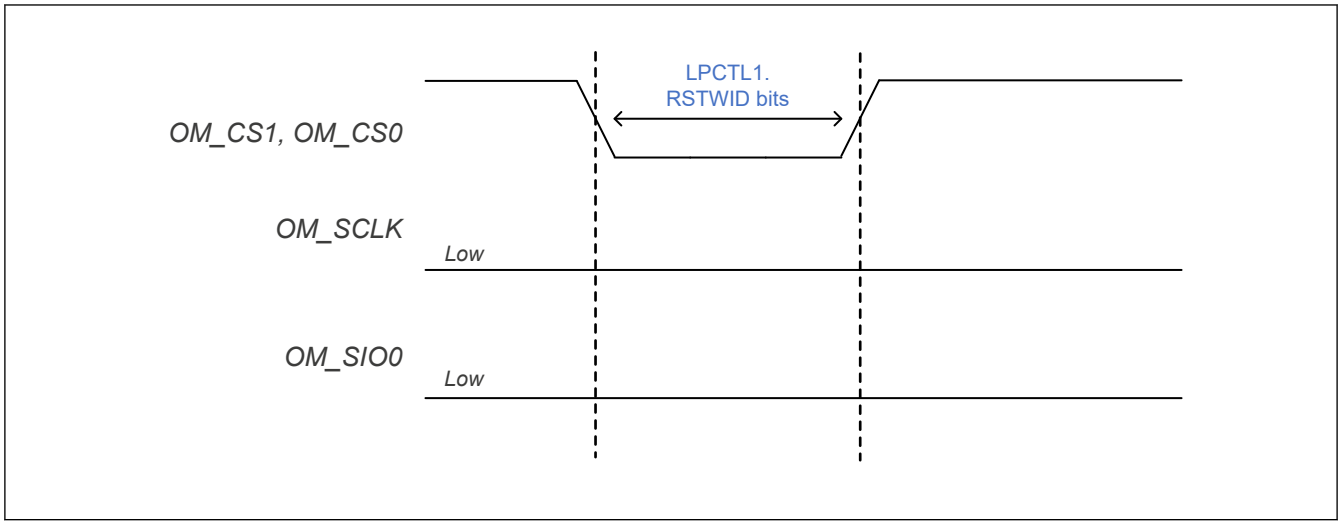


Figure 37.21 CS Only pattern

37.3.5 Integrity Checking

This xSPI Master can detect some errors. Table 37.8 shows the error list and the detail behavior.

Table 37.8 Error list (n = 0, 1)

Error type	Event	Flag bit	Note (action)
Calibration failed	When the read data did not match the expected value during automatic calibration.	INTS.CAFAILCSn	It results in writing unexpected data to xSPI slave.
System bus error	When an error response occurred on AXI slave interface for memory-mapping.	INTS.BUSERRCHn	This xSPI master shall be reset for fatal error.
ECC error detection	When detected the falling edge on OM_ECSINT1 port. It can be useful only for xSPI slave with ECC detection function.	INTS.ECSCS1	Only notify the error event of xSPI slave.
OM_DQS timeout	When OM_DQS does not toggle in read transaction with using OM_DQS.	INTS.DSTOCSn	Both xSPI master and xSPI slave should be reset for fatal error.
Periodic transaction timeout	When the read value does not match with the expected value in periodic manual-command mode.	INTS.PERTO	Depending on the status of function.

37.3.6 Interrupts

This xSPI Master has an interrupt port.

It can monitor with Interrupt Status Register (INTS). In case of initialization phase, it can be programmable with Interrupt Enable register (INTE). Table 37.9 shows OSPI interrupt sources, and Table 37.10 shows the related register bit.

Note: Interrupt pulse port signal is not asserted when the corresponding bit of INTE is set after the interrupt event is detected.

Table 37.9 OSPI interrupt sources

Name	Interrupt sources	DMAC activation
OSPI0_ERR	Error	Not possible
OSPI0_CMP	Complete	Not possible

Table 37.10 Interrupt register bit

Flag bit	Enable bit	Clear bit	Interrupt sources
CASUCCS1	CASUCCS1E	CASUCCS1C	OSPI0_CMP
CASUCCS0	CASUCCS0E	CASUCCS0C	
CAFAILCS1	CAFAILCS1E	CAFAILCS1C	OSPI0_ERR
CAFAILCS0	CAFAILCS0E	CAFAILCS0C	
BUSERRCH0	BUSERRCH0E	BUSERRCH0C	OSPI0_ERR
INTCS1	INTCS1E	INTCS1C	OSPI0_ERR
ECSCS1	ECSCS1E	ECSCS1C	OSPI0_ERR
DSTOCS1	DSTOCS1E	DSTOCS1C	OSPI0_ERR
DSTOCS0	DSTOCS0E	DSTOCS0C	
PERTO	PERTOE	PERTOC	OSPI0_ERR
PATCMP	PATCMPE	PATCMPC	OSPI0_CMP
CMDCMP	CMDCMPE	CMDCMPC	OSPI0_CMP

37.3.7 Flows of Operations

37.3.7.1 Flow of Configuration

Figure 37.22 shows flow of configuration.

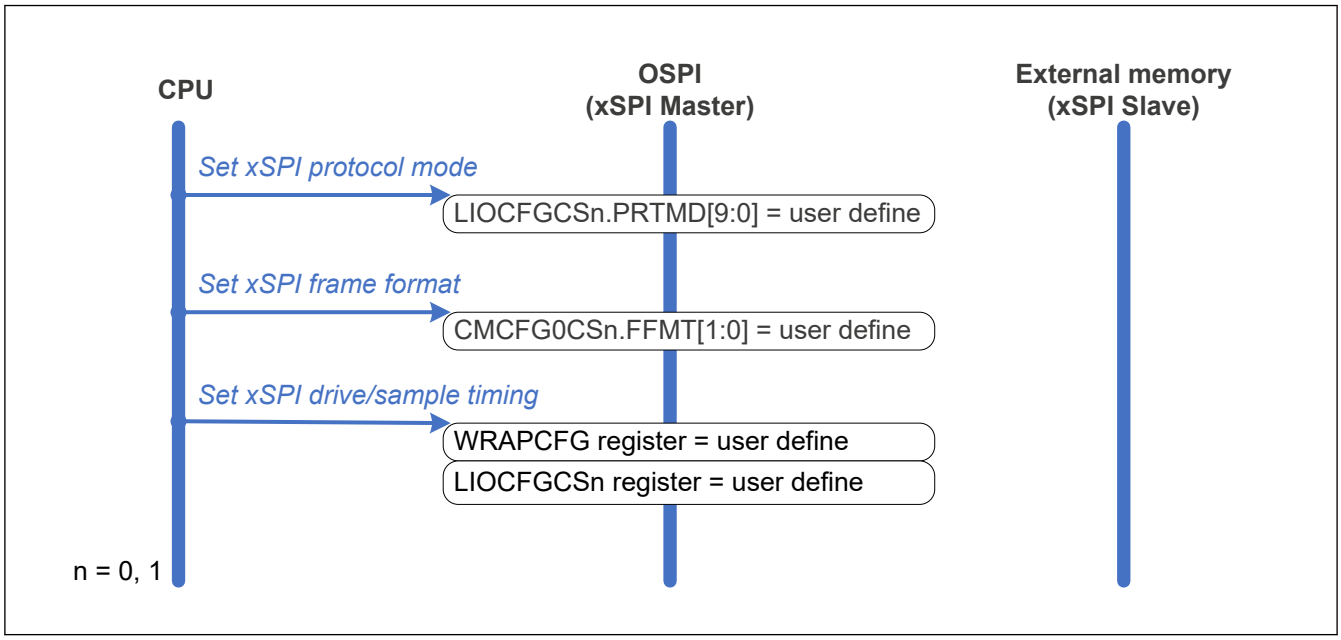


Figure 37.22 Flow of configuration

37.3.7.2 Flow of Communication Stop

Figure 37.23 shows flow of communication stop.

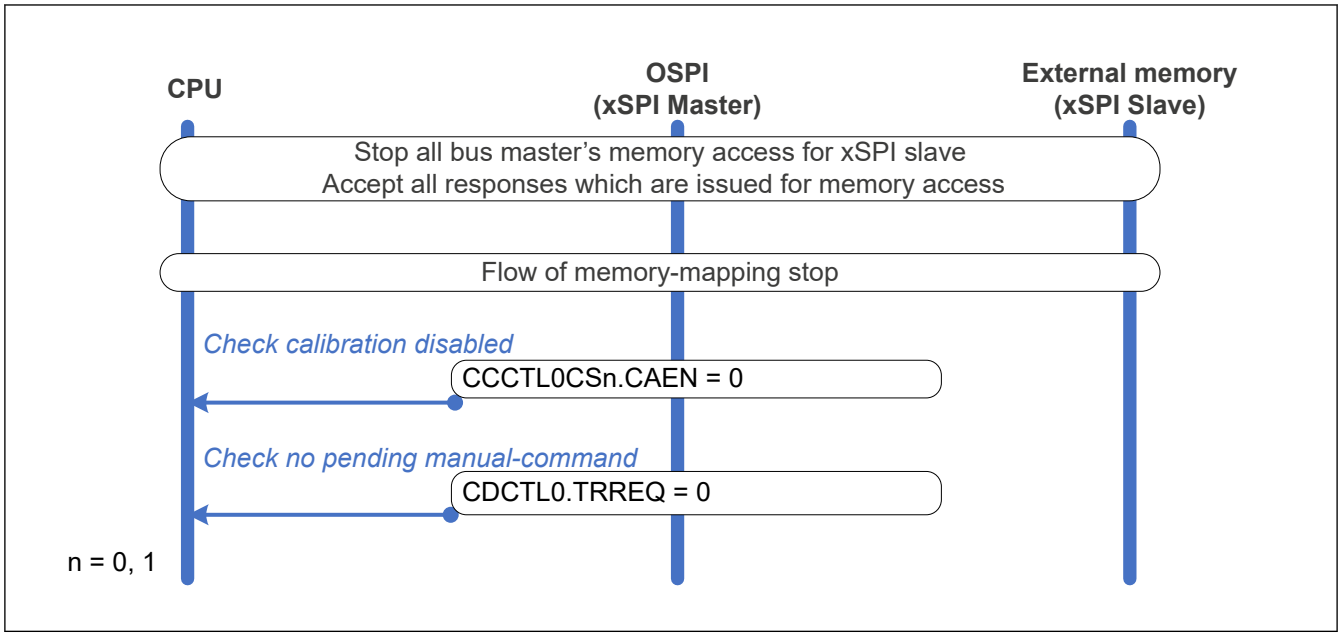


Figure 37.23 Flow of communication stop

Note: In case of re-config of any configuration register, all communication with xSPI slave shall be stopped surely to avoid race condition between register setting and memory access. It means that the automatic calibration is disabled, and there is no pending manual-command and memory-mapping access.

37.3.7.3 Flow of Automatic Calibration

Figure 37.24 shows flow of automatic calibration.

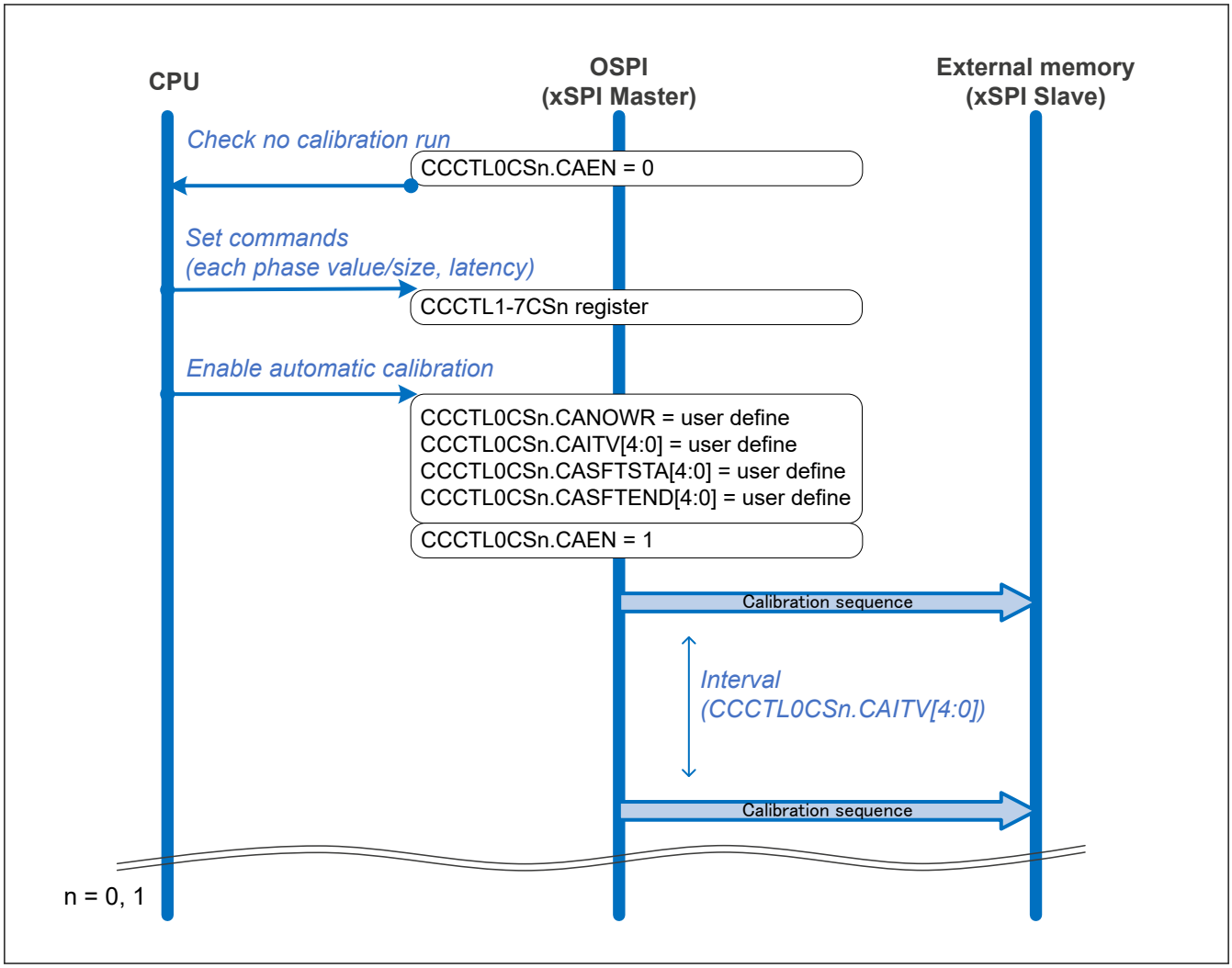


Figure 37.24 Flow of automatic calibration

37.3.7.4 Flow of Manual-command Procedure

Figure 37.25 shows manual-command procedure for direct mode.

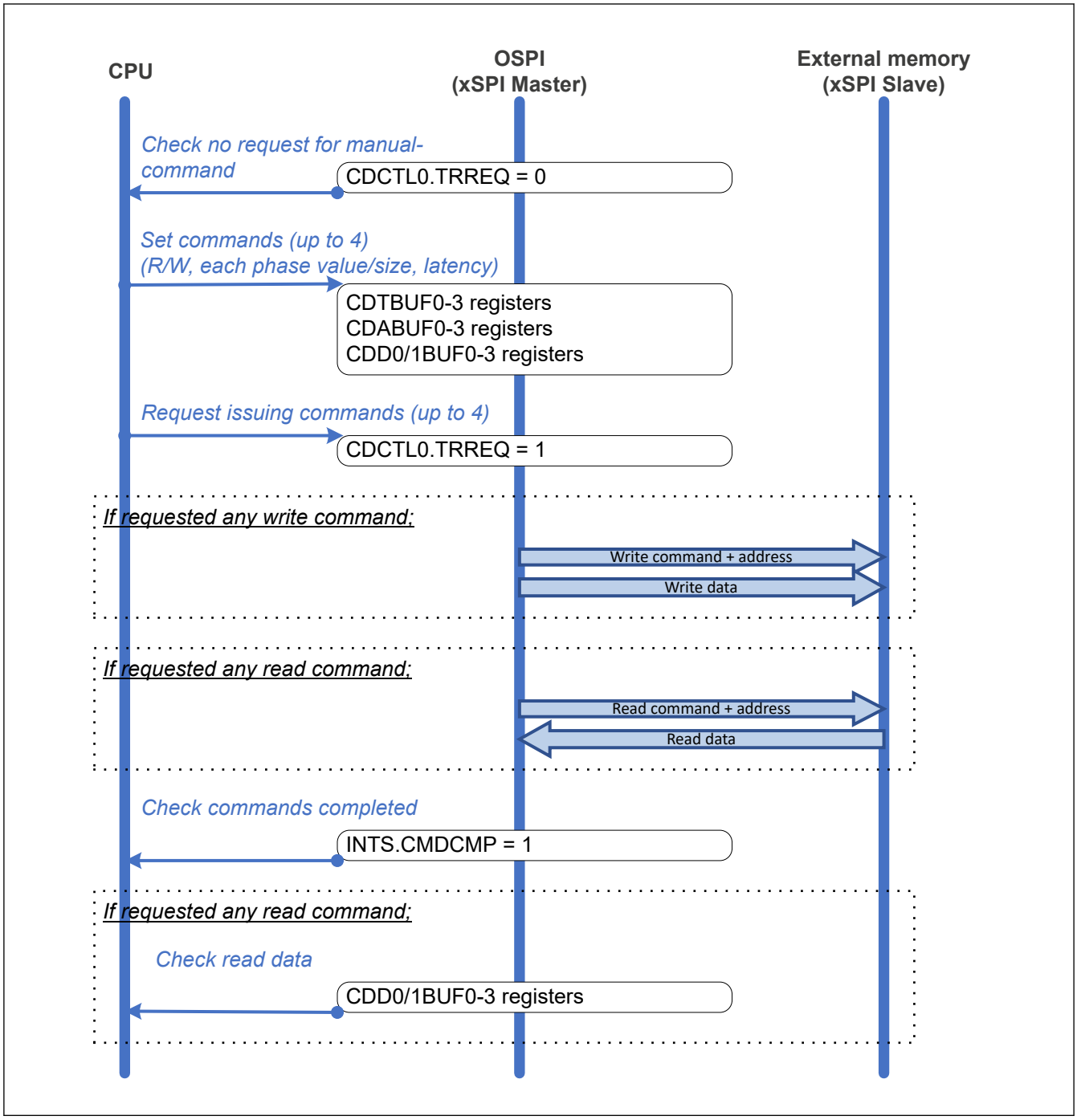


Figure 37.25 Flow of manual-command procedure for direct mode

Figure 37.26 shows manual-command procedure for periodic mode.

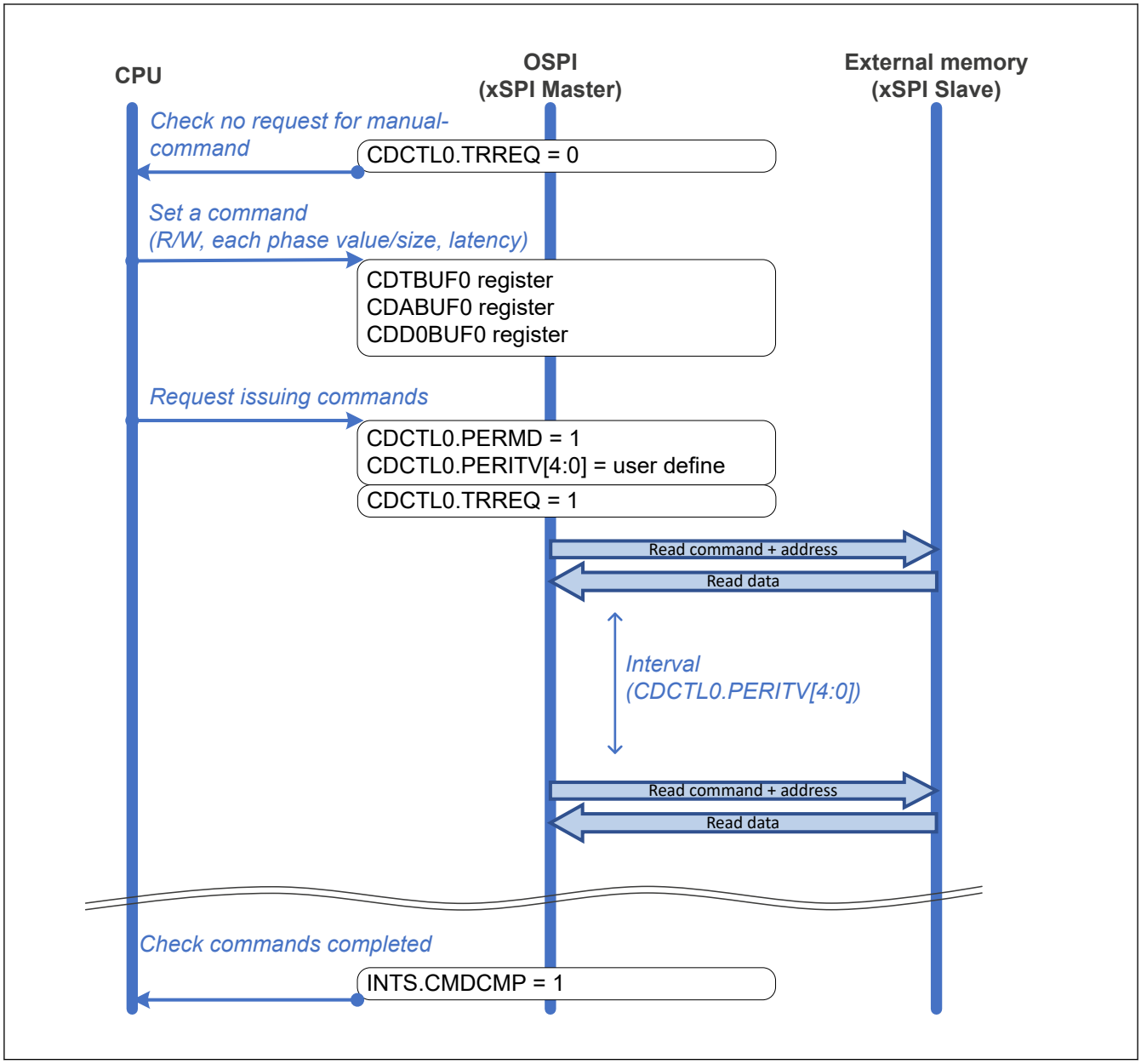


Figure 37.26 Flow of manual-command procedure for periodic mode

37.3.7.5 Flow of Memory-mapping

Figure 37.27 shows flow of memory-mapping.

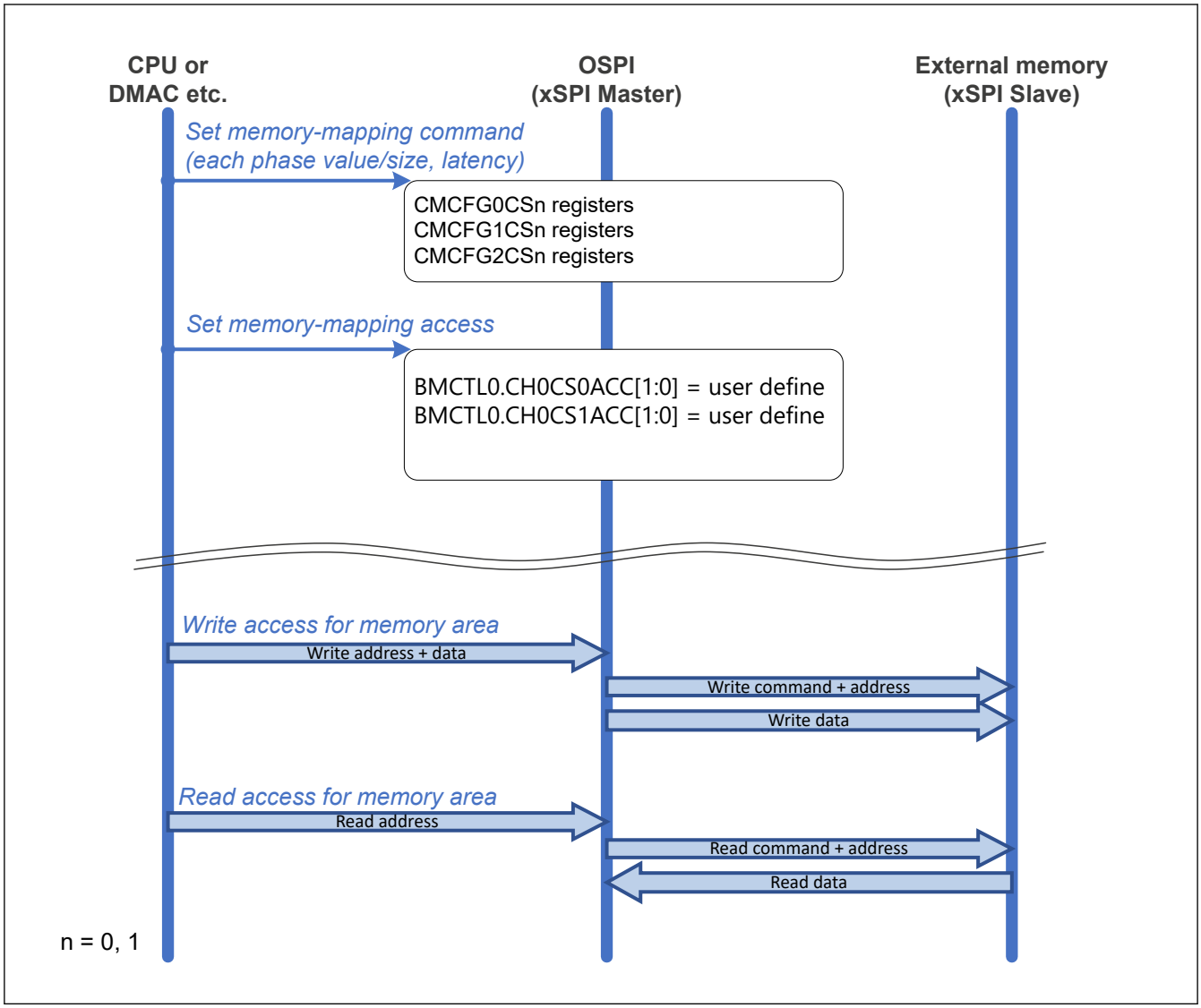


Figure 37.27 Flow of memory-mapping

37.3.7.6 Flow of Memory-mapping Stop

Figure 37.28 shows flow of memory-mapping stop.

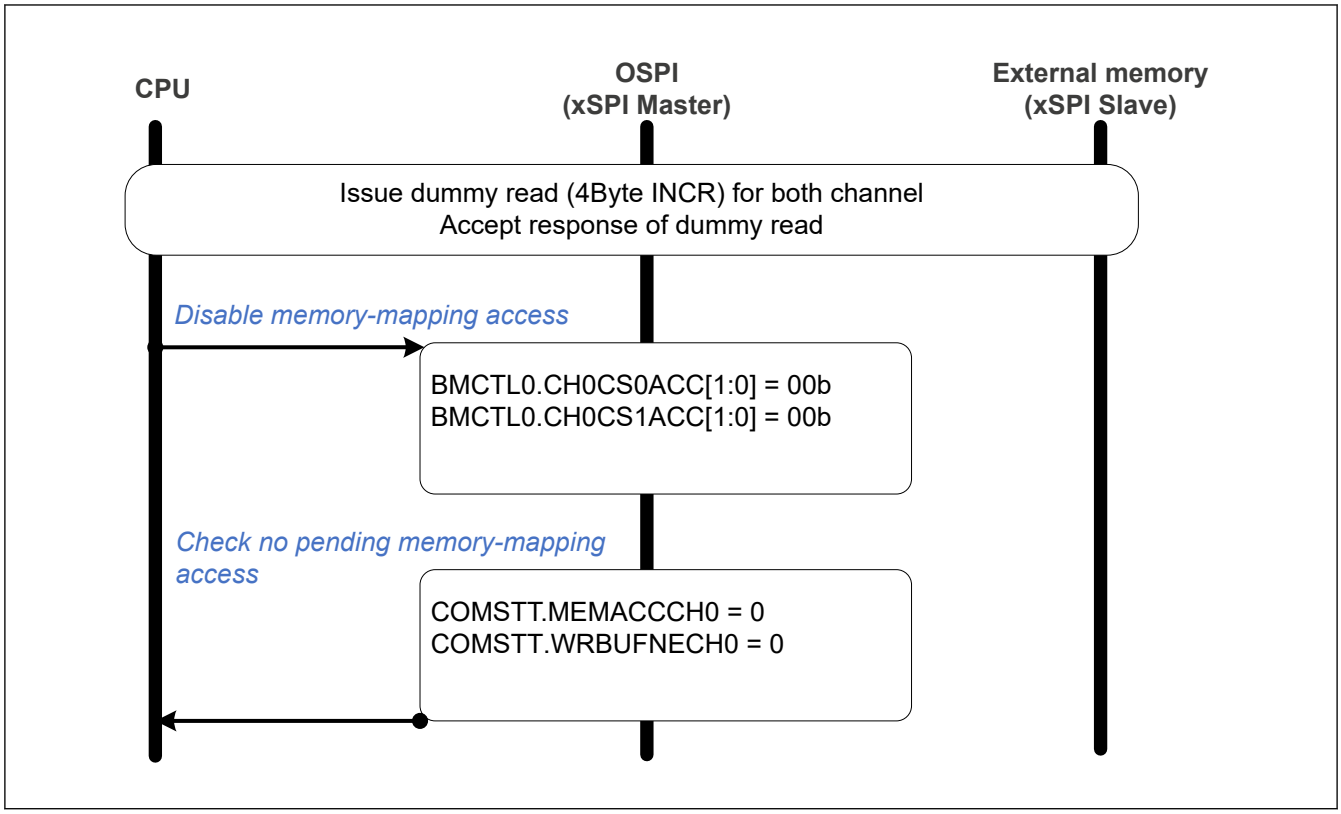


Figure 37.28 Flow of memory-mapping stop

37.3.7.7 Flow of Pattern Request

Figure 37.29 shows flow of pattern request. Before requesting any pattern, any ongoing commands should be completed or canceled.

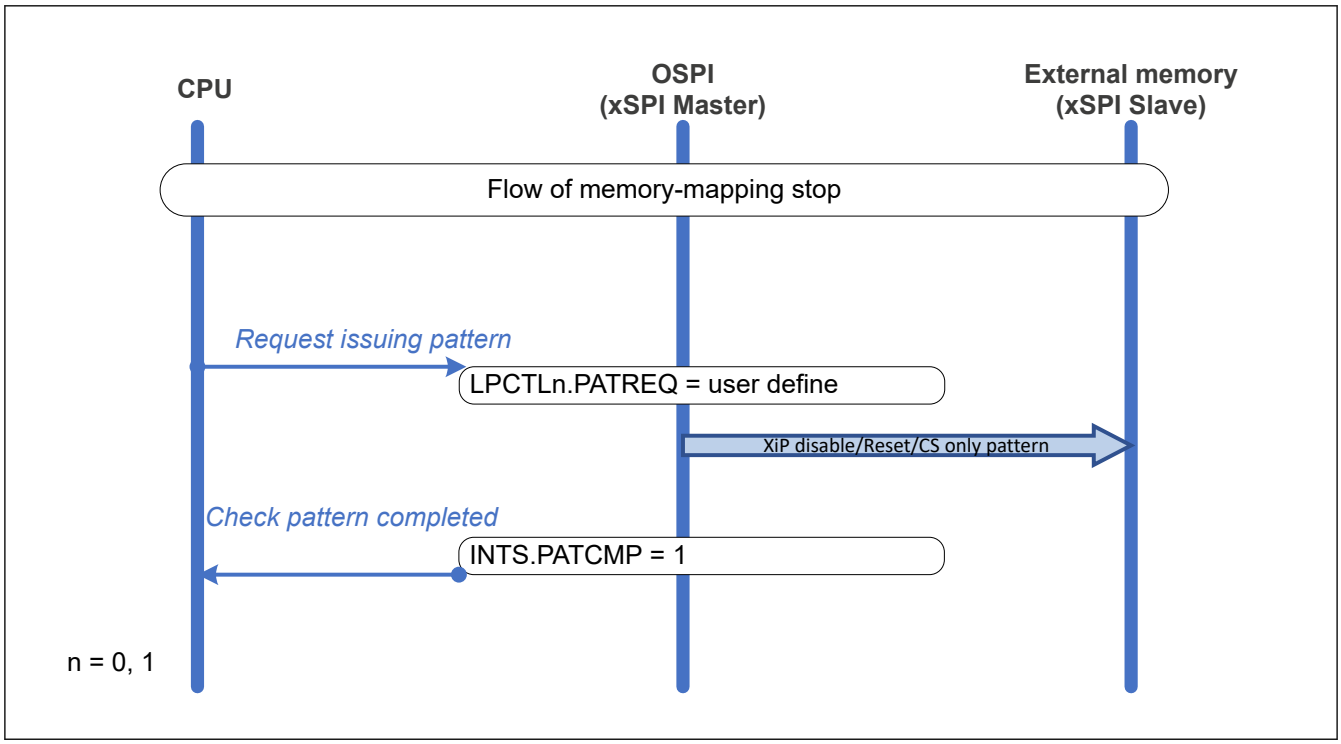


Figure 37.29 Flow of pattern request

37.3.7.8 Flow of XiP Mode

Figure 37.30 shows flow of XiP mode enable/disable.

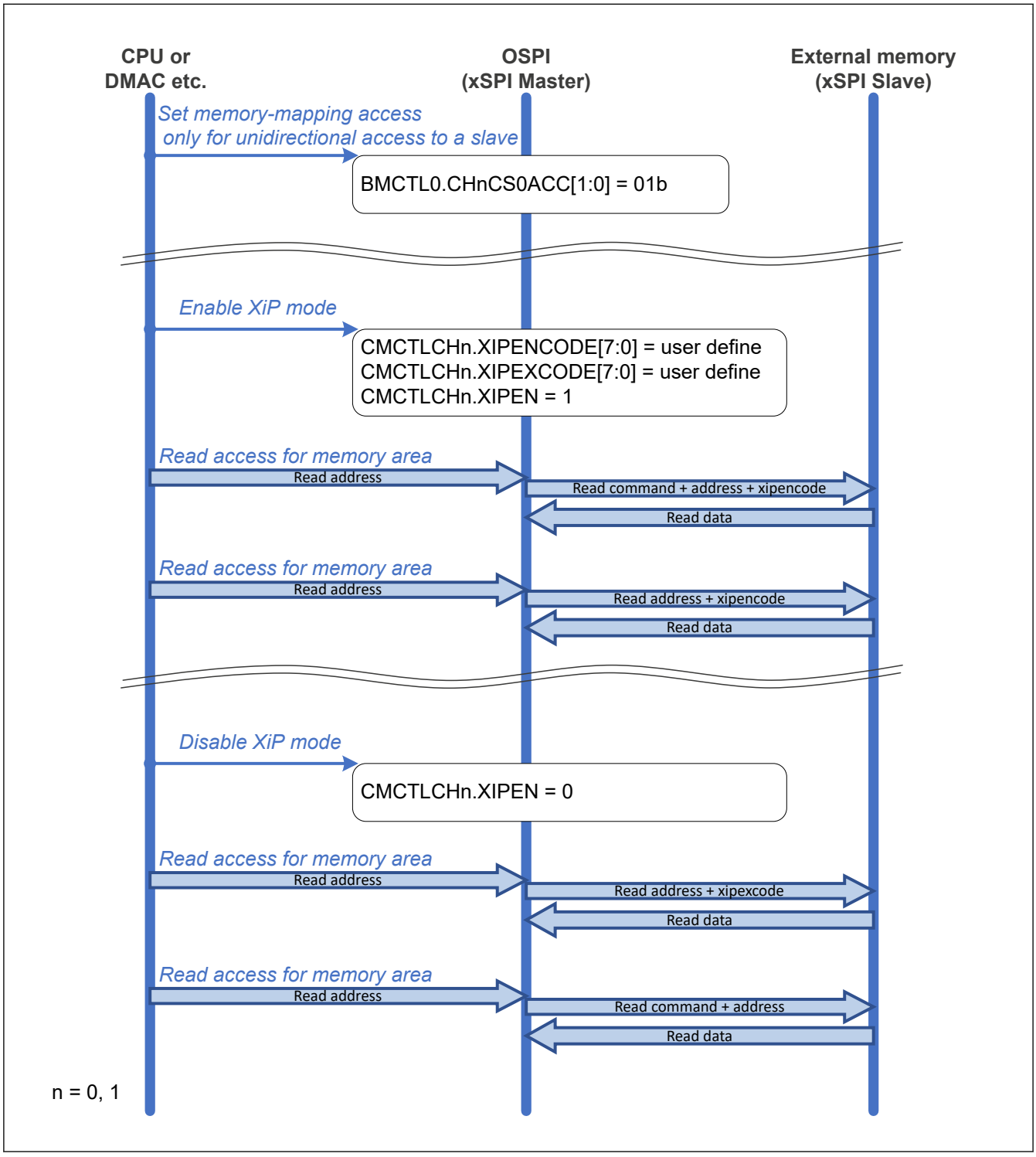


Figure 37.30 Flow of XiP mode enable/disable

37.3.7.9 Flow of Read While Write

Figure 37.31 shows example flow of read while write.

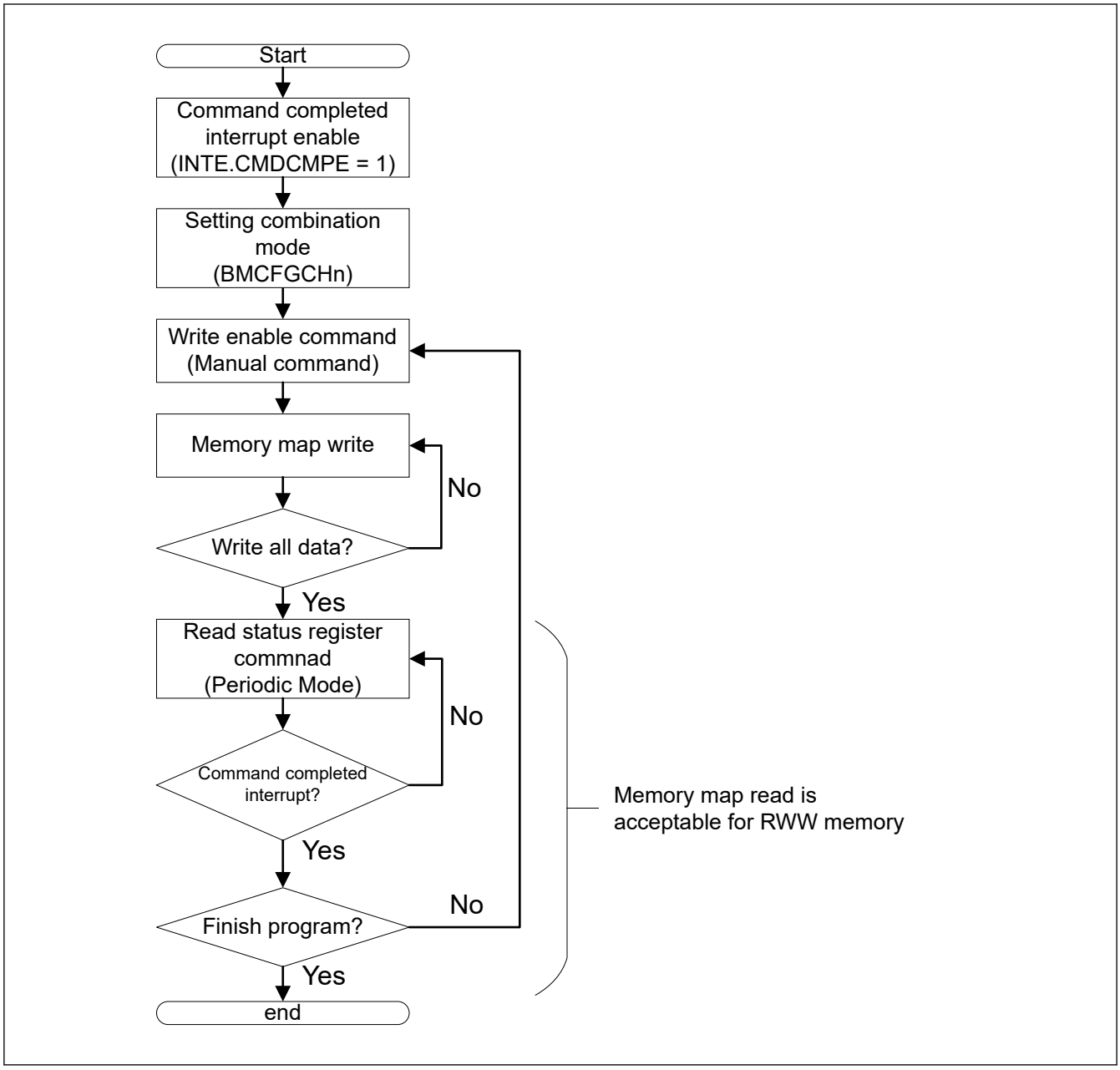


Figure 37.31 Flow of read while write

37.3.8 Usage Notes

37.3.8.1 Constraint on Memory Access

The memory access has the following constraints:

- Prohibit to access last 128 byte area of memory support area.
- Not using prefetch function if application access to the last 128 byte area

37.3.8.2 Constraint on Burst Length

AXI bus master must have a Burst Length of 16 or less.

37.3.8.3 Memory Write Combination Mode

When BMCFGCHn.MWRCOMB is 1, memory write combination mode is enabled. However, combination does not work if the bus master is CPU, and OSPI data is under 32bit. Table 37.11 shows the possibility of data write for each bus master.

Table 37.11 Data write possibility for each bus master

Bus Master	Combination Enable	Combination Disable
CPU under 64 bit Access	Not possible	Possible
CPU 64 bit Access	Possible	Possible
DMAC/DTC	Possible	Possible
EDMAC	Possible	Possible
CEU	Possible	Possible

37.3.8.4 Module-stop function

OSPI operation can be disabled or enabled using Module Stop Control Register B (MSTPCRB). The OSPI module is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 10, Low Power Modes.

37.3.8.5 Restriction in 8D-8D-8D profile 1.0 format

"When read or write access to the Octal Serial Peripheral Interface (OSPI) is performed from the following bus masters with 8-bit wide, access to odd addresses is prohibited as it will not be worked correctly. See Table 37.12 for the applicable conditions and their workarounds for each bus master"

Table 37.12 Workaround for the restriction in 8D-8D-8D profile 1.0 format

Bus master		Conditions that require workaround	Workaround
CPU	Normal memory	Debugger is connected	Access only even addresses.
	Device memory	Always	Access only even addresses.
DMAC/DTC	DMAC	DMTMD.SZ[1:0] = 00b	Access only even addresses.
	DTC	MRA.SZ[1:0] = 00b	Access only even addresses.

37.3.8.6 Byte data order in 8pin-DDR mode

In 8pin-DDR mode, OSPI read and write data in the order of byte0 at rising edge and byte1 at falling edge.

Some memory devices read and write in the swapped order in 8pin-DDR mode. For these devices, if 8pin-DDR read the data which is written in other than 8pin-DDR mode, this data should be written in swapped order.

38. Decryption On The Fly (DOTF)

38.1 Overview

DOTF has a function to decode read data of the AXI bus using AES core.

Table 38.1 lists the DOTF specifications and for a system using DOTF, see section 37.1. Overview.

Table 38.1 DOTF Specification

Item	Description
Clock Source	Register clock : PCLKB AES core clock : PCLKA
AES core function	• Utilize for on-the-fly decryption of encrypted software stored in external memory. • Block size: 128-bit • Key size: 128-bit, 192-bit, 256-bit • Support the following block cipher mode. − Counter (CTR) mode following NIST SP800-38A • Support side channel counter measure function. • Supports self-test function. • Counter[127:0] = {IV[127:28], Address[31:4]}, where Address is the memory mapped address of the encrypted data, aligned to the AES block size of 128 bits (16 bytes). The IV shall be chosen according to the recommendations provided in appendix B of SP800-38A. See section 37, Octal Serial Peripheral Interface (OSPI) and section 4.1. Address Space for details. See NIST SP800-38A for details of AES counter mode operation.
Tamper Resistance	Countermeasures available for side-channel attacks, including SPA/DPA and timing attacks
Module-stop function	Module-stop state can be set to reduce power consumption. same as OSPI module stop
TrustZone Filter	Security and Privilege attribution can be set for each channel. same as TZF of OSPI

38.2 Block Diagram

The block diagram of DOTF is shown in Figure 38.1. See Figure 37.1 for a diagram including the OSPI.

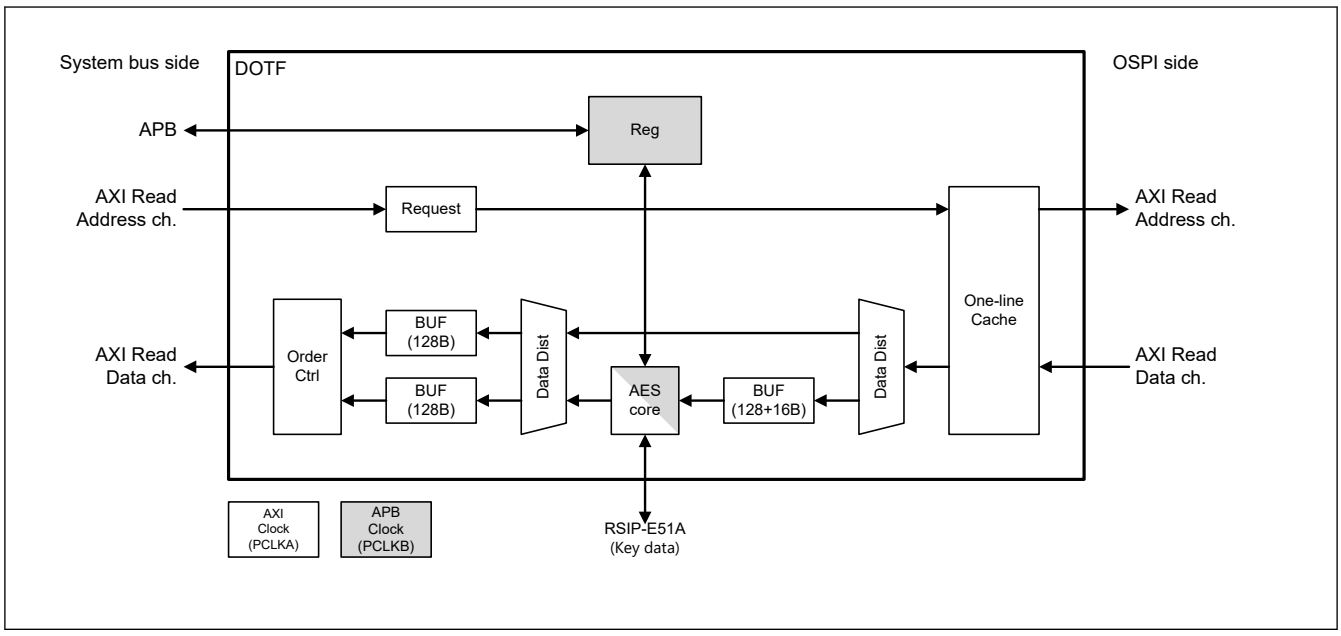


Figure 38.1 Block diagram

38.3 Register Descriptions

DOTF allows the entire area to be an accessible area, but the area where decryption processing is performed can be specified as the entire area or one contiguous area. The region can be specified by setting the start and end addresses to the CONVAREAST and CONAREAED registers, respectively.

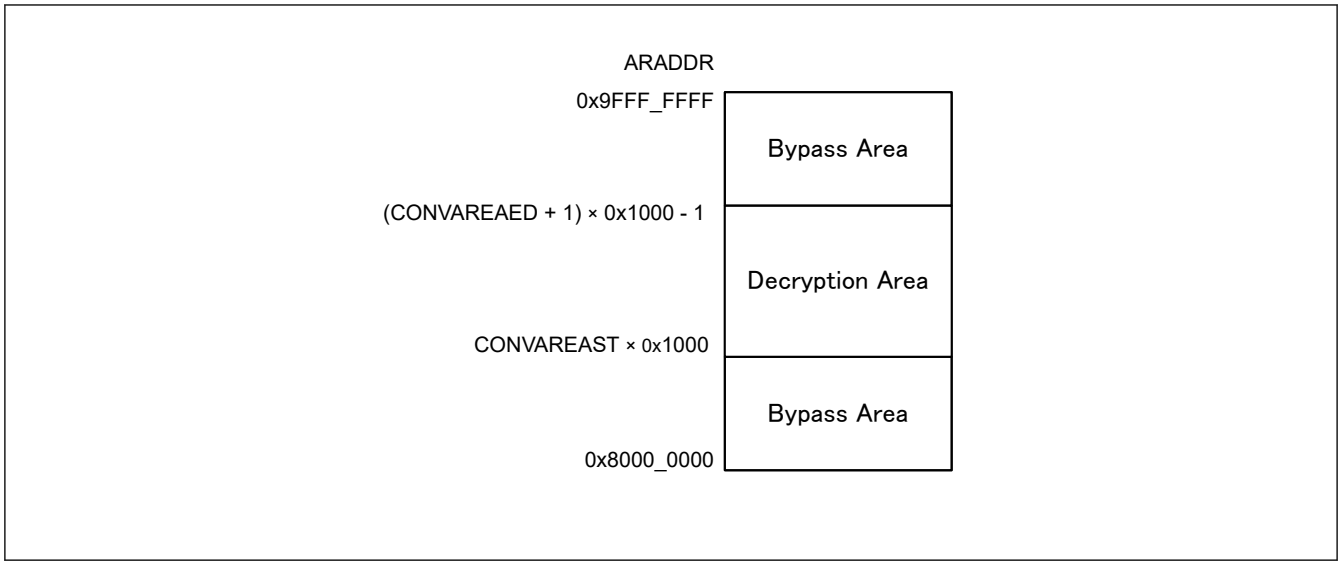


Figure 38.2 Image of decryption area setting

38.3.1 CONVAREAST : DOTF Conversion Area Start Address Register

Base address: DOTF0 = 0x4026_8800
DOTF0_NS = 0x5026_8800

Offset address: 0x00

Bit position:	31												12												0
Bit field:	CONVAREAST[31:12]													—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
11:0	—	These bits are read as 0.	R/W
31:12	CONVAREAST[31:12]	The first address of the decryption processing area. The actual address is CONVAREAST[31:12] × 0x1000.	R/W

Note: S-TYPE-3, P-TYPE-3

Specify the first address of the decryption processing area. Set before the AXI transfer request and do not make any further changes. Setting CONVAREAST[31:12] > CONVAREAED[31:12] is prohibited.

38.3.2 CONVAREAD : DOTF Conversion Area End Address Register

Base address: DOTF0 = 0x4026_8800
DOTF0_NS = 0x5026_8800

Offset address: 0x04

Bit position:	31												12												0
Bit field:	CONVAREAED[31:12]													—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
11:0	—	These bits are read as 0.	R/W
31:12	CONVAREAED[31:12]	The end address of the decryption processing area. The actual address is CONVAREAED[31:12] ×0x1000.	R/W

Note: S-TYPE-3, P-TYPE-3
Note: Setting CONVAREAST[31:12] > CONVAREAED[31:12] is prohibited.

Specify the tail address of the decryption processing area. Set before the AXI transfer request and do not make any further changes. Setting CONVAREAST[31:12] > CONVAREAED[31:12] is prohibited.

38.4 Operation

DOTF has one AXI Read Slave Interface and one AXI Read Master Interface.

An AXI transfer request received on the AXI Slave Address channel is issued to the AXI Master's Read Address channel, and the Slave data is received from the Master's AXI Read data channel and sent to the AXI Slave Read data channel.

At this time, the necessity of decryption is determined by the requested address area, and the decrypted data is transmitted through AES core if necessary. When decryption is not required, the received response is sent without conversion.

38.5 System flow

The initialization flow after HW reset is shown in Figure 38.3.

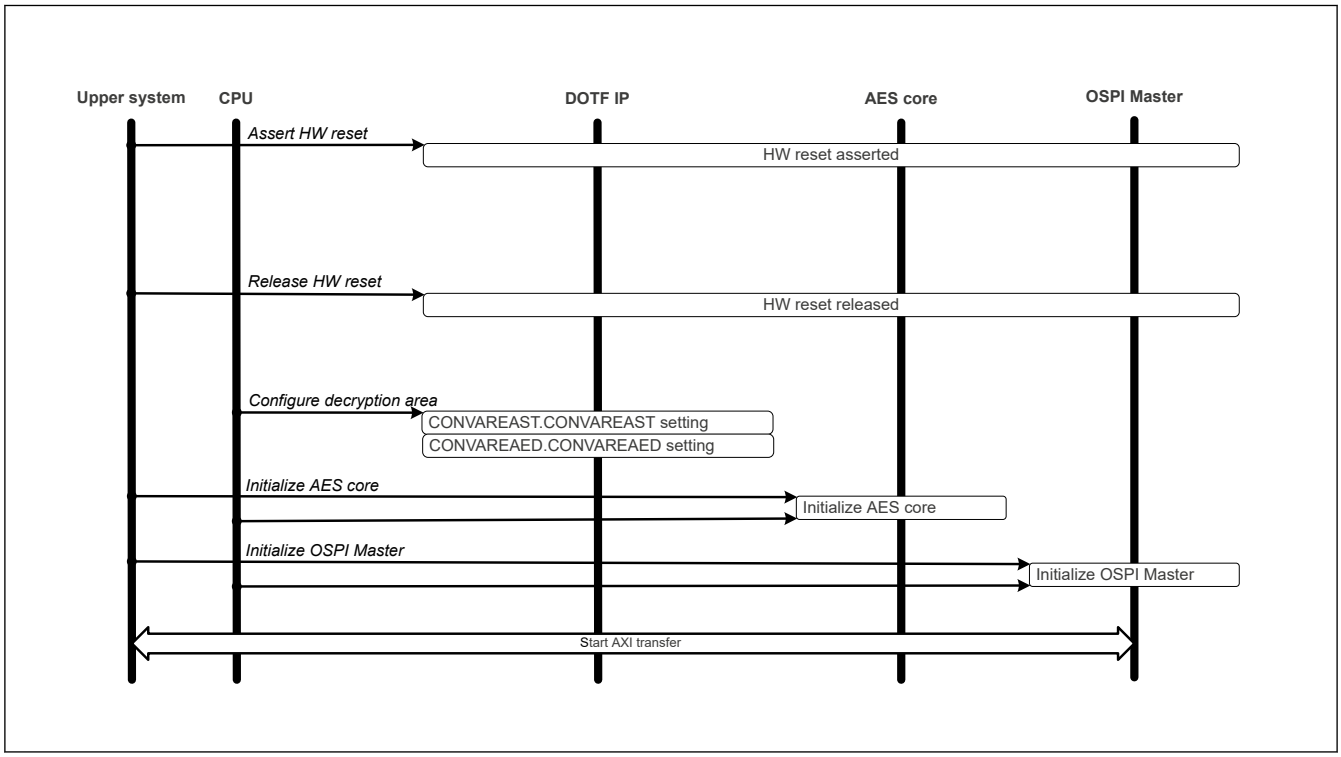


Figure 38.3 Initialization flow

38.6 Usage notes

38.6.1 Module-stop function

DOTF operation can be disabled or enabled using Module Stop Control Register B (MSTPCRB). The DOTF module is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 10, Low Power Modes.

Appendix 1. Port States in Each Processing Mode

Function	Pin function	Reset	Software Standby mode(SSTBY)		Deep Software Standby mode 1,2,3 (DSTBY1,2,3)		After Deep Software Standby mode is canceled (return to startup mode)	
			OPE=0	OPE=1	DSTBY1	DSTBY2/ DSTBY3	IOKEEP = 0	IOKEEP = 1[*1]
Mode	MD	Pull-up	Keep-I		Keep		Pull-up	Keep
JTAG/SWD	TCK/TMS/TDI/SWCLK	Pull-up	TCK/TDI/TMS/SWCLK input		TCK/TDI/TMS/SWCLK input		TCK/TDI/TMS/SWCLK input	
	TDO	Output	TDO output		TDO output		TDO output	
	SWDIO	Pull-up	SWDIO inout		SWDIO inout		SWDIO inout	
Trace	TCLK/TDATAx/SWO	TCLK/ TDATAx/SWO output	TCLK/TDATAx/SWO output		TCLK/TDATAx/SWO output		TCLK/TDATAx/SWO output	
IRQ	IRQx	Hi-Z	Hi-Z[*2]		Keep		Hi-Z	Keep
	IRQx-DS (x:Other than 5)	Hi-Z	Hi-Z[*2]		Keep[*3]		Hi-Z	Keep
	IRQ5-DS	Hi-Z	Hi-Z[*2]		Keep[*3]		Hi-Z	
AGT	AGTIOn	Hi-Z	AGTIOn inout		Keep		Hi-Z	Keep
	AGTOn/AGTOAn/ AGTOBn	Hi-Z	AGTOn/AGTOAn/AGTOBn output		Keep		Hi-Z	Keep
ULPT	ULPTEEn/ULPTEVIn	Hi-Z	ULPTEEn/ULPTEVIn input		Keep		Hi-Z	Keep
	ULPTEEn-DS/ ULPTEVIn-DS	Hi-Z	ULPTEEn-DS/ULPTEVIn-DS input		ULPTEEn-DS/ ULPTEVIn-DS input	Hi-Z	Hi-Z	Keep
	ULPTOn/ ULPTOAn/ ULPTOBn	Hi-Z	ULPTOn/ULPTOAn/ULPTOBn output		Keep		Hi-Z	Keep
	ULPTOn-DS/ ULPTOAn-DS/ ULPTOBn-DS	Hi-Z	ULPTOn/ULPTOAn-DS/ ULPTOBn-DS output		ULPTOn/ ULPTOAn-DS/ ULPTOBn-DS output	Keep	Hi-Z	From DSTBY1: ULPTOn/ ULPTOAn-DS/ ULPTOBn-DS output From DSTBY2,3: Keep
IIC	SCLn/SDAn	Hi-Z	Keep-O[*2]		Keep		Hi-Z	Keep
I3C	I3C_SCL0/I3C_SDA0	Hi-Z	Keep-O[*2]		Hi-Z		Hi-Z	
USBFS	USB_OVRCURx	Hi-Z	Hi-Z[*2]		Keep		Hi-Z	Keep
	USB_OVRCURx-DS/ USB_VBUS	Hi-Z	Hi-Z[*2]		Keep[*3]	Keep	Hi-Z	Keep
	USB_DP/USB_DM	Hi-Z	Keep-O[*4]		Keep[*3]	Keep	Hi-Z	Keep
USBHS	USBHS_OVRCURx	Hi-Z	Hi-Z[*2]		Keep		Hi-Z	Keep
	USBHS_OVRCURx-DS /USBHS_VBUS	Hi-Z	Hi-Z[*2]		Keep[*3]	Keep	Hi-Z	Keep
	USBHS_DP/ USBHS_DM	Hi-Z	Keep-O[*4]		Keep[*5]	Keep	Hi-Z	Keep
RTC	RTCICx	Hi-Z	Hi-Z[*2]		Keep[*3]		Hi-Z	Keep
	RTCOUT	Hi-Z	RTCOUT output		Keep		Hi-Z	Keep
ACMPHS	VCOUT	Hi-Z	VCOUT output		Keep		Hi-Z	Keep
CLKOUT	CLKOUT	Hi-Z	CLKOUT output		Keep		Hi-Z	Keep
DAC	DAn	Hi-Z	D/A output retained		Hi-Z		Hi-Z	