CHAPTER 5 DIGITAL SAMPLE-RATE CONVERSION

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The increasing need of processing digital data at more than one sampling frequency has resulted in the development of a new area of digital signal processing known as multirate signal processing. The basic operations in multirate signal processing are decimation and interpolation ([12]-[13]). Decimation reduces the sampling rate effectively by compressing the data and retaining the desired information. Interpolation increases the sampling rate. Sampling rate conversion can be done either in analog domain or in digital domain. In the first method, the digital signal is passed through a digital-to analog converter (DAC) and then the analog signal is resampled at the desired rate. In the second method, the resampling of digital data at the desired rate is carried in the digital domain itself.

In this chapter, a new technique of digital sample-rate conversion will be explained. Firstly, the question is posed (and answered) why sample-rate conversion is necessary in audio systems. Conventional methods of sample-rate conversion will be discussed. Then the principle of operation of a new digital sample-rate converter will be explained. Furthermore, the block diagram will be presented.

5.1 Why sample-rate conversion?

In digital audio applications, a number of sample frequencies is in use (see table 5.1); it is to be expected that with the arrival of multi-media the variety of sample-rates will only increase.

Table 5.1 Sample frequencies used for digital audio

Sample frequency	Application
44.1 kHz	CD, DCC, DAT
32 kHz	NICAM, DSR, DCC, DAT, MAC
48 kHz	DAT, DCC, DAB, S-VHS, prof. audio Equipment
16 kHz	MAC

18.9 kHz	CD-I (level C)
37.8 kHz	CD-I (level A & B)
31.5 kHz	8mm VCR
44.056 kHz	U-matic VCR
38 kHz	Digital FM stereo decoders

There are three important situations in which the application of sample-rate conversion is very useful: they are listed below:

i) When two digital audio systems are linked together, the sample frequency of one of the two systems may have to be altered. However, only one master clock can issue the correct moment of sampling in a digital system, so this inevitably leads to synchronization problems. Due to the different standards listed in table 5.1, the interconnection of two audio devices becomes very cumbersome. Here, the application of sample-rate conversion is desireable.

ii) Even when the two devices to be connected have equal sample frequencies, synchronization problems will occur due to a (very) small difference in sampling frequency. This is especially true for systems where a lot of digital sources have to be aligned to one sample frequency before they can be mixed or processed, like in digital audio mixers or in digital broadcast stations. Here, sample-rate conversion can be applied to (re)synchronize the different sources.

iii) Although digital audio links are normally not subject to loss of code information, they definitely introduce a loss of timing information (jitter), due to long transmission lines. When such a jittering signal is used as a clock source for the DAC section, the analog performance at the output can be seriously degraded. Here also, sample-rate conversion in combination with a digital PLL can be used for jitter removal.

5.2 Conventional sample-rate conversion methods

The aim of (digital) sample-rate conversion is to bring a digital audio signal from one sample frequency to another. The distortion of the audio signal, introduced by the sample-rate converter, should be as low as possible. The generation of output samples from the input samples may be performed by the application of various methods.

One solution is depicted in figure 5.1. The input samples at a sampling rate F_i are upsampled by an integer factor N. The signal at NF_i is low-pass filtered and decimated by an integer factor M to obtain the output sample rate F_o. This solution implies that the conversion factor Fo/F_i is equal to N/M which is a rational number. The master clocks from which F_i and F_o are obtained have to be locked.

The implementation of this method is for small values of N and M not so difficult. For large N and M the filter becomes more complicated as the required stop-band attenuation increases with increasing N and M.

When for instance a 16-bit digital audio signal at a sampling rate of 48 kHz must be converted to a sampling rate of 44.1 kHz, this method leads to N=147 and M=160. In this example the common frequency, which is also the operating frequency of the filter, becomes 7.056MHz. Due to the folding products which results from decimating by 160, the required stop-band attenuation must at least be 120 dB.

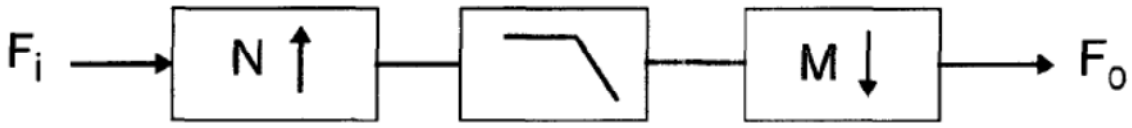

Fig.(5.1) Sample-rate conversion for a fixed rational ratio N/M

Most digital sample-rate converters work with upsampling, construct a continuous-time equivalent from the samples coming out of the upsample filter and resample this signal with the

output sample frequency Fo. This situation is depicted in figure 5.2. For these solutions the common multiple of the frequencies Fi and Fo is not needed.

The number of input samples is increased to NFi so that the shape of output signal looks more like a continuous-time waveform. The reconstruction filter constructs a continuous-time signal which is fed to the output sampler. The reconstruction of the time-signal may be performed by a first-order hold function or by linear interpolation.

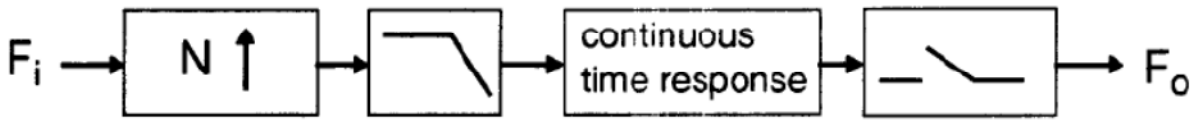

Fig. (5.2) Conventional digital sample-rate conversion

Table 5.2 shows the required upsample factor N and the required stop-band attenuation for these two reconstruction methods in order to achieve a 16-bit performance.

Table 5.2 Oversampling factor and stop-band attenuation for 'hold' and for 'linear interpolation'

Continuous-time filter	**N**	**Stop-band attenuation**
Hold	30000	150dB
Linear-interpolation	100	120dB

The large stop-band attenuation that is required leads to large filters so there is a lot of hardware needed for the implementation. The calculation of the output samples leads to large number of multiplication and addition operations.

In the next sub-paragraph a new method of digital sample-rate conversion is described. The output samples of this sample-rate converter are not calculated from the input samples, but they are obtained by simply taking over or repeating the input samples.

5.3 A new method of digital sample-rate conversion

The operation principle of the new method of sample rate conversion is very simple. An input sample is directly transferred to the output, while per unit of time, a certain amount of these samples is omitted or repeated, depending on the difference in input and output sample frequencies. The omission, acceptance or repetition of a sample is called 'validation'. In order to get the simplest hardware implementation, the choice has been made to use only the take-over operation and the repetition operation in the current system solution. This means that the output sampling frequency of the sample rate converter is always larger than the input sample frequency.

The process of repeating samples inevitably introduces errors. The resulting output samples will have correct values, but as a result of the validation operation, they are placed on the output time grid with a variable time delay with respect to the input time grid. As a consequence, the output sequence should be viewed as the input sequence, having the correct signal amplitude, which is sampled at wrong time moments. The effect is the same as sampling the input signal by a jittered clock. As a result, it can be stated that the time error mechanism introduced by the validation algorithm is time jitter.

If all input samples would be transferred to the output grid without the repetition or omission of a certain amount of them, then the output signal would be just a delayed version of the input signal, exhibiting the same shape. It is the repetition and omission (in the current system setup only the repetition) of input samples that give rise to a variation in time delay for each individual output sample. This variation in individual time delays introduces phase errors. As a result of this, the shape of the output signal will be distorted.

The time errors introduced by the conversion process can be reduced considerably by applying upsampling and downsampling techniques. The input sample rate of the converter will be higher so that the conversion errors are smaller, resulting in smaller time jitter. These techniques do not suffice when we want to achieve the very high analog audio performance required for professional applications. By using a sigma-delta modulator (noise shaper) as control source for

the conversion process, the time errors will be shaped to the higher frequency region. As a result, the audio quality (in the baseband) of the signal will be preserved, provided that enough bandwidth is created by upsampling of the input signal. The high frequency (out of base band) phase modulation terms can be filtered by a decimation filter or an analog low-pass filter which is directly placed after the sample-rate converter. Figure 5.3 shows the block diagram of the complete sample-rate converter.

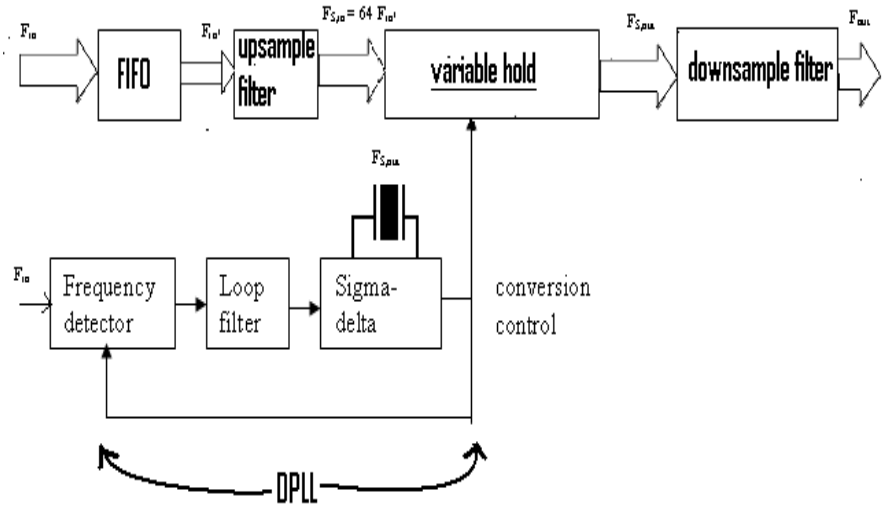

Fig. (5.3) Block diagram of the sample-rate converter

As has already been mentioned, only the input sample take over operation will be employed here in order to get the simplest hardware. This means that the input sample frequency of the converter must be always be smaller than the output sample frequency. With this restriction imposed, it is assured that all input samples are used in the output sequence, none of them being omitted. The extra output samples per unit of time are inserted in the output sequence by repetition of their previous output samples.

5.3.1 Upsampling and Downsampling

The sample-rate converter contains an upsample and a downsample filter, with in between a variable hold function, which performs the actual sample rate conversion.
The input samples are written into a FIFO with an input sampling frequency F_{in}. The FIFO is read out with a 'staggering' frequency Fin* that is on the average equal to F_{in}. This staggering frequency is upsampled to a sampling frequency of 64 $F_{in*}(F_{S,in})$; the samples coming out of the upsample filter are supplied to the variable hold function, which performs the actual sample-rate conversion. Within this function it is decided whether the next output sample is obtained by taking over a new input sample or by repeating its previous output sample. The output sample frequency of the variable hold ($F_{S,out}$) is downsampled with a factor 128 to obtain the output sampling frequency of the total sample-rate converter F_{out}. The values of the upsampling and downsampling factors can be chosen to have another value.

5.3.2 Conversion Controlled by a Sigma-Delta Modulator

The conversion process from $F_{S,in}$ to $F_{S,out}$ is controlled by the sigma-delta modulator inside the PLL, which runs on a high quality crystal clock with frequency $F_{S,out}$.The output signal of the sigma-delta modulator consists of '1' pulses and '-1' pulses and is a pulse density modulated version of its input signal. If for instance the input signal is DC 0.5, then the sigma-delta modulator will generate three '1' pulses and one '-1' pulse on the average 0.5.

If the clock frequency of the sigma-delta modulator is FS,out, it will generate FS,out pulses in one second. When this clock frequency is chosen to be the same as the output sampling frequency of the sample-rate converter, then the output pulses of the sigma-delta modulator can be used to control the conversion process. The input signal of the sigma-delta modulator is a DC value which is dependent on the input and output sampling frequencies of the sample-rate converter. Table 5.3 shows the setup that is chosen for the control of the sample-rate converter.

Table 5.3 Conversion Control in the Sample-Rate Conversion Process

Sigma-delta Output	**Control Action**
-1	Take over a new input sample
1	Repeat the previous output sample

Every second, $F_{S,in}$ input samples must be converted to $F_{S,out}$ output samples. As was mentioned before, all input samples are used in the output sequence. This means that the sigma-delta modulator has to generate $F_{S,in}$ '-1' pulses in 1 second. The remaining $F_{S,out}$-FS,in output samples are obtained by repeating some of the input samples (actually by repeating some of the output samples: such a repetition sample is obtained by holding the previous output sample). Therefore, the sigma-delta modulator has to generate $F_{S,out}$-$F_{S,in}$ '1' pulses in one second. The following equations give the relationship between the input DC of the sigma-delta modulator and the conversion factor $F_{S,out}/F_{S,in}$:

$$DC_{SD} = \frac{F_{S,in}.(-1) + (F_{S,out} - F_{S,in}).(1)}{F_{S,out}} = \frac{F_{S,out-} 2F_{S,in}}{F_{S,out}} = 1 - 2\frac{F_{S,in}}{F_{S,out}} \quad (5\text{-}1)$$

$$\frac{F_{S,out}}{F_{S,in}} = \frac{2}{1 - DC_{SD}} \quad (5\text{-}2)$$

The second equation immediately determines the conversion control range of the sample-rate converter. It is assumed at first that a third order sigma delta modulator is used to control the

conversion process. In order to avoid stability problems, the absolute value of the input voltage of this third order sigma-delta modulator must not exceed -3dB. The usable input ranges from -0.7 to 0.7, which implies that the conversion factor $F_{S,out}/F_{S,in}$ of the variable hold function can vary between 1.18 and 6.67. By using an downsampling factor which is twice as large as the upsampling factor, the conversion ratio of the total sample-rate converter can vary between 0.59 and 3.33. In figure 5.4 the conversion factor and the conversion ratio are shown as function of the DC input of the sigma-delta modulator. It follows that the control range is sufficient to cover the frequency range of the sample frequencies of digital audio applications.

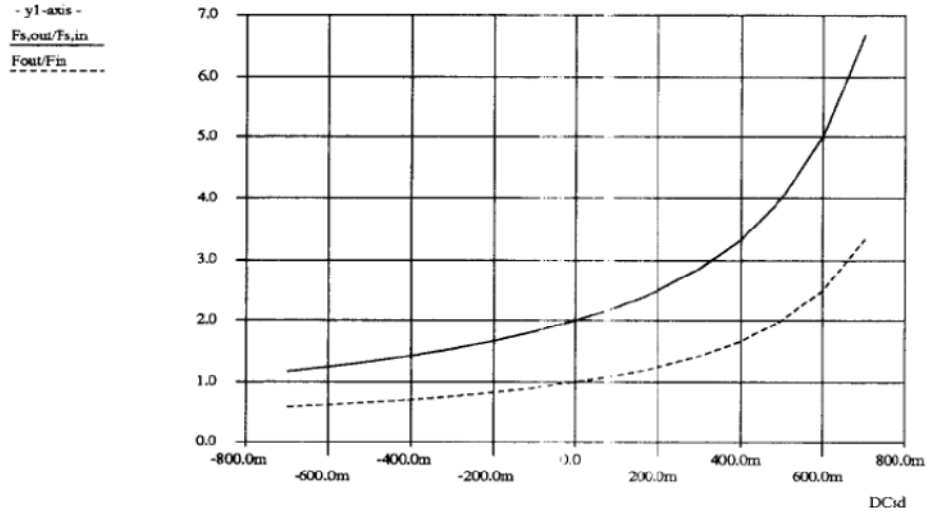

Fig.(5.4) The conversion factor and the conversion ratio as a function of the DC input of the sigma-delta modulator.

5.3.3 Digital Phase Lock Loop

The digital phase lock loop generates the correct DC for the sigma-delta modulator. It consists next to the sigma-delta modulator, of a frequency detector and a loop filter. The 'steady state' bandwidth of this loop filter is fixed to 0.5Hz in order to get a good suppression of jitter components in the incoming clock F_{in}. This bandwidth normally leads to unacceptable long lock-in times. The solution to this problem is to use an adaptive loop filter. During start-up, it has a 'large' bandwidth to ensure a fast locking to the input frequency. By modifying the multiplication coefficients inside the loop filter the bandwidth can be reduced. This loop filter

contains three sets of coefficients, which leads to three different bandwidths. After start-up the bandwidth is gradually reduced to its steady-state value of 0.5 Hz.

5.3.3.1 Block Diagram of Digital Phase Lock Loop

Figure (5.5) shows the simplified block diagram of the digital PLL. It consists of a frequency detector, a loopfilter and the 1-bit sigma delta modulator. The frequency detector takes as input signals F_{in} and the output of the sigma-delta modulator. The output of the frequency detector is fed to the second-order loopfilter which has a 'steady-state' bandwidth of 0.5 Hz. The output of the loopfilter is fed to the 1-bit sigma-delta modulator, which generates on the average the correct number of '1' pulses and '-1' pulses on its output.

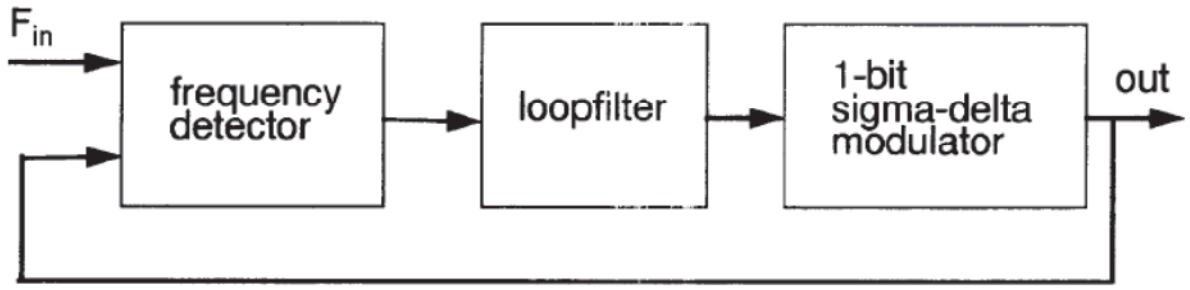

Fig. (5.5) The Digital PLL used in the sample-rate converter

In the next sub-paragraphs the frequency detector and the loopfilter will be explained.

5.3.3.2 Frequency Detector

The block diagram of the frequency detector is shown in figure (5.6).

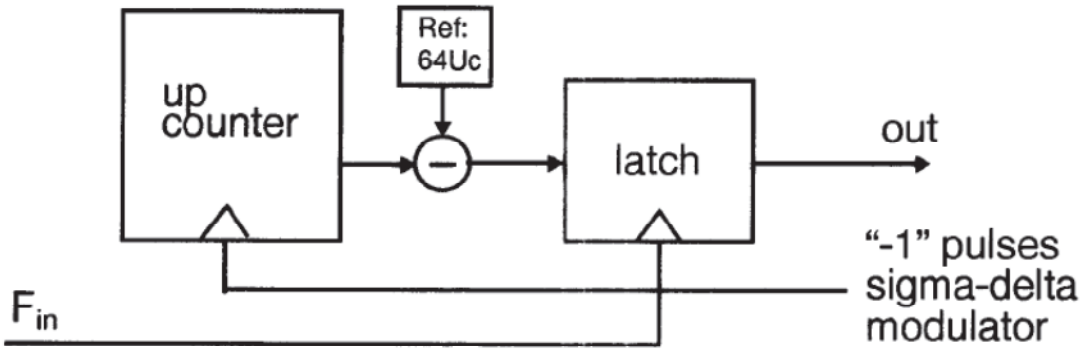

Fig. (5.6) Frequency Detector of the Digital PLL

The frequency detector consists of an upcounter and a latch. We have to remind that the sigma-delta modulator generates on the average $F_{S,in}$ "-1" pulses when the system is working properly. This frequency $F_{S,in}$ is equal to $64F_{in*}$ (compare the block diagram shown in figure 5.3).

The upcounter counts the number of "-1" pulses generated by the sigma-delta modulator. The count result is latched out with a frequency of F_{in}. When the system is working properly, the count result should be 64 count units. In the frequency detector a reference DC signal of 64 U_c (units of count) is subtracted from the count result. In this way a measure is obtained of the frequency of the two signals. This signal is fed to the loopfilter.

At start-up osf the system, the sigma-delta modulator could be zeroed in order to eliminate start-up uncertainty and instability [25]. The number of bits needed for the upcounter is obtained by looking at the worst case situation. When the sigma-delta modulator is zeroed, it generates a number of "-1" pulses equal to $F_{S,out}/2$ ($=64F_{out}$). The worst case input sampling frequency is determined by the smallest possible conversion ratio $F_{out}/F_{in}=3.33$ which is obtained from figure 5.4. The largest possible count result is then equal to 64*3.33=214. This number can be represented by 8-bits (256 count units). This means that also an 8-bit latch must be used.

5.3.3.3 Loop Filter

The output signal of the frequency detector is a measurement of the frequency difference of the two input signals. When a first-order loop filter is used, this frequency difference will be controlled to zero by the phase lock loop. However, in the sample-rate converter a second order loop filter containing two integrators is used. The phase is the integral of the frequency. So, in case of a second-order loop the digital PLL will minimize the phase errors accumulated in the FIFO. In order to avoid a total undamped behavior, the second integrator has to be bypassed [25].

The transfer function in the analog frequency domain will look alike [25]:

$$H(s) = K.\frac{1}{s}.\frac{s+\alpha}{s} = K.\frac{1}{s}.\left(1+\frac{\alpha}{s}\right) = \frac{K}{s} + \frac{K\alpha}{s^2} \qquad (5\text{-}3)$$

While in the analog frequency domain an integrator is described by the term 1/s, in the discrete frequency domain this factor becomes $1/(1\text{-}z^{-1})$. When the factor 1/s in (5-3) is replaced by $1/(1\text{-}z^{-1})$, the transfer function in the z-domain is obtained. In order to get a correct transformation to the z-domain, the integrators must be preceded by a gain factor $1/f_{in}$. The gain factors K and α will be transformed to the new gain factors k' and α':

$$H(z) = \frac{k'}{1-z^{-1}} + \frac{k'\alpha'}{(1-z^{-1})^2} = k'.\frac{(1-z^{-1})+\alpha'}{(1-z^{-1})^2} \qquad (5\text{-}4)$$

A block diagram of this loop filter is shown in figure 5.7. From start-up towards steady state behavior, the coefficients k' and α' will be reduced so that the loop bandwidth is reduced. The coefficients for the start-up setting are obtained by optimizing the acquisition behavior of the loop. For k' and α' the values 0.34 and 0.024 are found respectively [25]. As it is much easier to implement shift factors than gain factors, k' and α' are chosen 2^{-1} and 2^{-4} respectively. During 512 input clock cycles, this initial filter setting is active. During this time, the sigma-delta modulator input is zeroed and no signal processing is done in the sample-rate converter. A difference frequency of 1 Hz between input and output is reached within about 10ms. Then k'

and α' will be changed to 2^{-7} and 2^{-10} respectively, so that the bandwidth of the loop is reduced. In this period, the signal processing in the sample-rate converter is started. This filter setting is active during 16384 input clock cycles. After this time period, the third filter setting becomes active. The coefficients k' and α' are now 2^{-12} and 2^{-15} respectively. For this steady-state setting of the filter the bandwidth of the loop is about 0.5 Hz, so that the sample-rate converter operates within specifications. In [25] a more detailed description of the design procedure of this digital phase lock loop has been given.

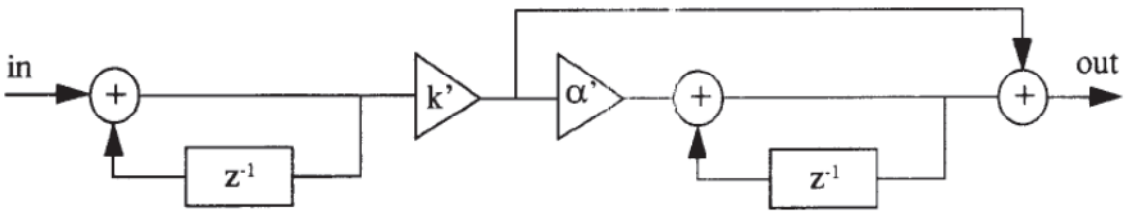

Fig. (5.7) The loop filter inside the digital phase lock loop

The loop filter generates the correct DC level for the sigma-delta modulator and filters the time-uncertainties inherent to the system. When a frequency step takes place at the input, the steady-state filter setting implies that the loop will follow very slowly. As the resulting phase errors accumulate in the FIFO, it could be possible that the FIFO shifts one or more places due to such a frequency step. This could lead to overflow or underflow depending on the 'direction' of the frequency step. The solution to this problem is given by switching the filter setting to the fast state as soon as the FIFO shifts one place in either direction. After acquisition, the filter setting is again gradually reduced to the steady-state bandwidth of 0.5Hz.

In the next section, a few methods of clock recovery will be described. Clock recovery is a very important aspect when designing a D/A converter. The quality of the clock recovery normally limits the performance of the D/A converter.

5.3.4 Clock Recovery

The performance of a D/A converter is normally limited by the quality of the clock recovery. This clock recovery can be accomplished in the analog as well as in the digital domain. A few possible solutions will be described in following section:

5.3.4.1 A few methods for clock recovery

In the analog domain, an analog phase lock loop is used for clock recovery. The PLL locks on the incoming clock signal. It contains a loopfilter so that jitter components, present in the clock signal, are filtered.

When an analog phase lock loop is used, its bandwidth has to be fixed at about 50 kHz, otherwise it introduces too much phase jitter [26]. The influence of these jitter components would be visible as a degradation of the signal-to-noise ratio at the analog output. The bandwidth of approximately 50 kHz gives rise to a disadvantage: if there are jitter components with a frequency less than 50 kHz present in the clock signal, they will pass the phase lock loop. This means that the clock signal should be generated by a high-quality crystal clock and that the transmission line should be correctly terminated. Therefore this solution is not convenient for the professional area; for *consumer applications* however it is suitable enough [26].

In *professional applications,* the D/A conversion system should have a good performance even in the presence of a considerable amount of jitter on the input clock signal. Therefore, the phase lock loop must suppress these jitter components efficiently. There exists two solutions to this problem, which are summarized below [26]:

- ANALOG clock recovery by a high-quality phase lock loop or a VCXO (voltage-controlled crystal oscillator; the phase lock loop should have a very small bandwidth to filter out the jitter components of the clock input signal. A small bandwidth implies that the VCO (Voltage-Controlled Oscillator) of the phase lock loop should have very low circuit noise otherwise it generates too much phase noise and degrades the analog

performance too much. The required performance of the phase lock loop can only be reached by using very expensive discrete components, while IC solutions generate far too much circuit noise. This jitter problem can be overcome by using VCXO's, which are much more insensitive to clock jitter, but they have the disadvantage of a small input frequency capturing range. So, when the system has to lock on different input frequencies several VCXO's have to be incorporated.

- DIGITAL sample rate conversion; In these solutions, the system runs on a high-quality crystal clock with low jitter, which implies that the performance degradation at the analog output is almost negligible. Digital sample-rate conversion can be applied with an arbitrary accuracy at the cost of computation power and IC-area. The conversion of input samples to the crystal output sample rate is performed in the digital domain. Most techniques that are used to perform this conversion are based on a polynomial reconstruction of the output samples or by means of interpolation filtering in the time domain, which inevitably leads to large ROM tables to store the required filter coefficients (see sub-paragraph 5.2). Therefore, IC-implimentattions of digital sample-rate converters are large and as a matter of fact, they are only used for professional applications.

The new digital sample-rate converter described in this report is very well suited for clock recovery. The digital PLL has a bandwidth of 0.5 Hz, which effectively filters the jitter components with a frequency higher than 0.5 Hz out of the incoming clock signal. The application of this sample-rate converter in an oversampled D/A converter would yield a very flexible and competitive D/A converter, when the increase in IC-area is not too large.

In the next chapter, a time-domain analysis of the new digital sample-rate converter will be given.