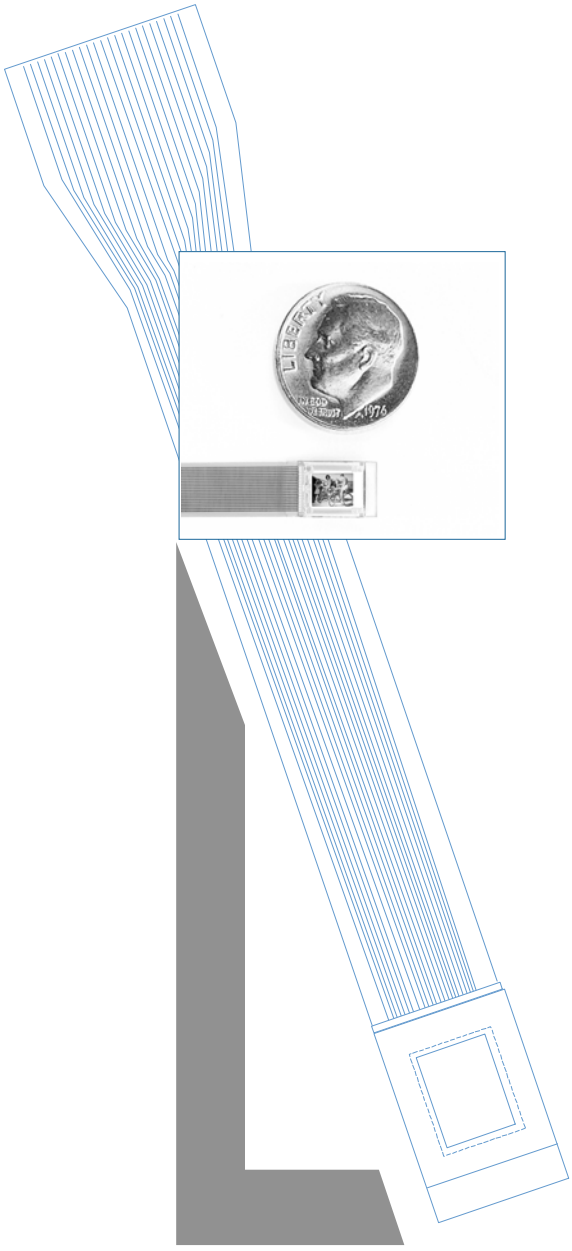
KOPIN

CyberDisplay™



CyberDisplay™ 320 Monochrome Display KCD-QD01-AA

Kopin Corporation

125 North Drive, Westborough, MA 01581
T 508.870.5959, F 508.870.0660

PS-00## Rev. 0

1. Table of Contents

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2. General Description

The CyberDisplay™ 320 is an active-matrix liquid crystal display, with 320 × 240 spatial resolution. The display is fabricated in a high speed, low power CMOS process utilizing single crystal silicon-on-insulator (SOI) starting material. The display's integrated horizontal and vertical shift registers with thin film transistors meet the performance demands of high-speed video applications. The display uses complementary analog video inputs. All digital control inputs accept 3.3 – 5.0 -volt levels.

2.1 Features

- 320 (H) × 240 (V) spatial resolution (76,800 pixels).
- Active pixels 320 × 240 (76,800 pixels).
- 3.3 – 5.0 volt CMOS logic compatible control signals with built-in level-shifter
- Low power consumption: 12mW
- High performance: up to 72 frames per second
- 1 positive and 1 negative polarity staggered analog video inputs
- Integrated horizontal and vertical shift registers
- Right to Left or Left to Right Scanning
- Ultra-compact size: Active display area 4.80 mm × 3.60 mm (0.24 inches diagonally)

The display products and systems described herein are covered by numerous issued U.S. and foreign patents and pending applications owned by or licensed to Kopin Corporation.

These specifications are subject to change without notice.

3. Electrical Specifications

3.1 AMLCD Specifications

Figure 3-1: CyberDisplay™ 320 Block Diagram

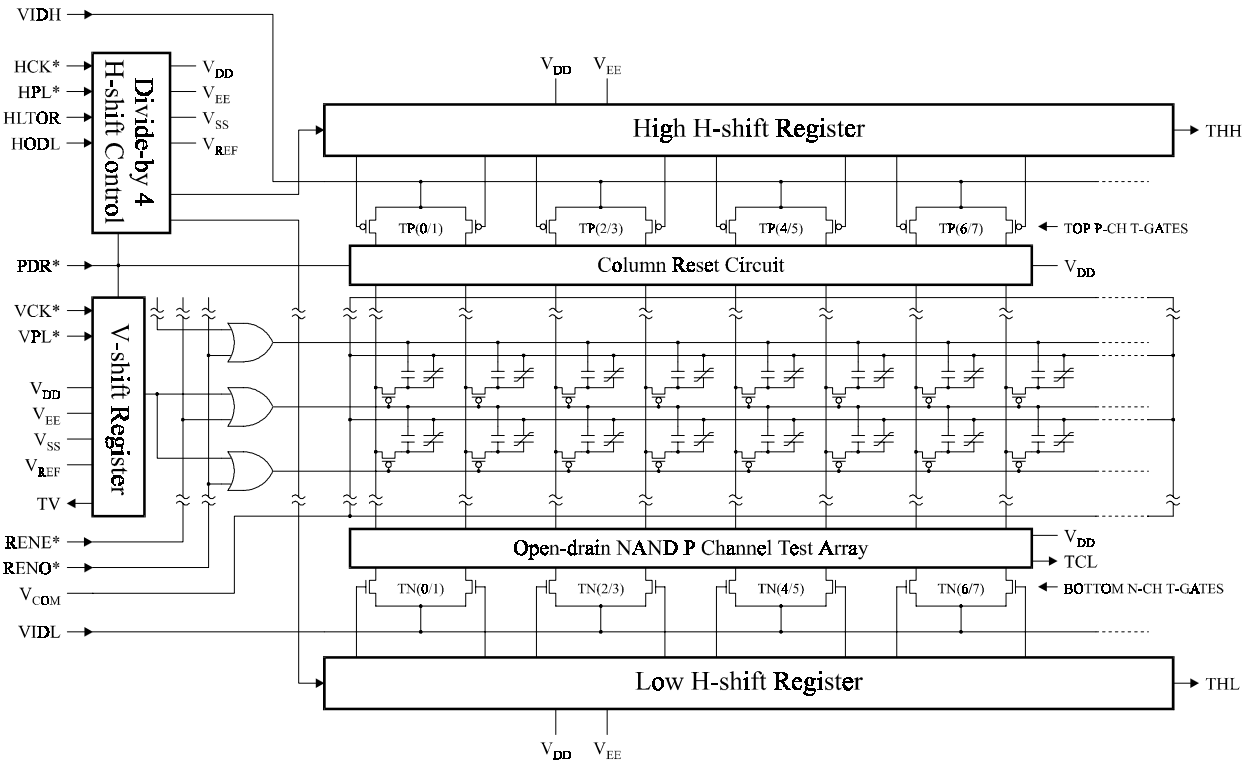


Table 3-1: Absolute Maximum Ratings

Parameter/Condition	Symbol	Rated Value	Units
Supply Voltage — Source	V_{DD}	–0.5 to +12	V
Supply Voltage — Sink	V_{EE}	V_{DD} – 11 (≥ -0.5) to V_{DD} + 0.5	V
High Video Signal	VIDH	–0.5 to V_{DD} + 0.5	V
Low Video Signal	VIDL	–0.5 to V_{DD} + 0.5	V
All Inputs	V_I	–0.5 to V_{DD} + 0.5	V

Note Permanent damage to the display may result if Absolute Maximum Ratings in Table 3-1 are exceeded. The Absolute Maximum Ratings are not typical operating conditions.

Table 3-2: Electrical Characteristics and Recommended DC Operating Conditions

(Notes: 1, 2, 3) (V_{DD}= 9V ± 0.5V, V_{EE}= 2V ± 0.2V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage - Source	V_{DD}	8.5	9.0	9.5	V
Supply Voltage - Sink	V_{EE}	1.8	2.0	2.2	V
Operating Current: Power Supply - Source	I_{VDD}		1.6	2.6	mA
Operating Current: Power Supply - Sink	I_{VEE}		-1.0	-1.7	mA
Operating Current: GND	I_{VSS}			-0.9	mA
Video Signal Center Voltage	V_{VC}		½(V_{DD}+V_{EE})		V
Video Common Voltage	V_{COM}		V_{VC}+0.4		V
Video Common Current	I_{VCOM}			10	µA
High Video Voltage (VIDH)	V_{VIDH}	V_{VC} (Wht)		V_{DD} (Blk)	V
Low Video Voltage (VIDL)	V_{VIDL}	V_{EE} (Blk)		V_{VC} (Wht)	V
Input Reference Voltage	V_{REF} (3.3V Logic)	1.7	1.8	1.9	V
	V_{REF} (5.0 V Logic)	2.2	2.3	2.4	V
Input Reference Current	I_{VREF} (3.3V Logic)			10	µA
	I_{VREF} (5.0V Logic)			10	µA
Input High Voltage, excluding PDR*	V_{IH} (3.3V Logic)	2.9			V
(See note 8)	V_{IH} (5.0V Logic)	4.4			V
Input Low Voltage, excluding PDR*	V_{IL} (3.3V Logic)			0.3	V
(See note 8)	V_{IL} (5.0V Logic)			0.5	V
Input High Voltage, PDR*(See note 9)	V_{IHPDR}	3.3			V
Input Low Voltage, PDR* (See note 9)	V_{ILPDR}			0.5	V
Input Current	I_{IPDR}			10	µA

Table 3-3: Capacitance

Parameter	Symbol	Min.	Typ.	Max.	Units
Input Capacitance: HPL*, VPL*, HCK*, VCK*, PDR* RENE*, RENO*, HODL, HLTOR	C_C			10	pF
Input Capacitance: VREF	C_{VREF}			40	pF
Input Capacitance: VCOM	C_{VCOM}			300	pF
Input Capacitance: VIDH, VIDL	C_V	40	50	60	pF

Table 3-4: Display Power Consumption

Parameter	Symbol	Min.	Typ.	Max.	Units
Power consumption of the display	PWR		12.0	22.0	mW

Table 3-5: Electrical Characteristics and Recommended AC Operating Conditions

(Notes: 4,5,6) (V_{DD}= 9V ± 0.5V, V_{EE}= 2V ± 0.2V)

Parameter	Symbol	Min.	Typ.	Max.	Units
VCK* period	^{t}VC	101.4			µs
VCK* high pulse width	^{t}VCH	290			ns
VCK* low pulse width	^{t}VCL	290			ns
VPL* setup time	^{t}VPS	140			ns
VPL* hold time	^{t}VPH	140			ns
VCK* to RENE*/RENO* delay time	^{t}VCRD	440			ns
RENE*/RENO* to VCK* delay time	^{t}VRCD	440			ns
RENE*/RENO* to RENO*/RENE* delay time	^{t}VRED	890			ns
HODL to HCK* time	^{t}HOH			40	ns
HCK* period	^{t}HC	150			ns
HCK* high pulse width	^{t}HCH	65			ns
HCK* low pulse width	^{t}HCL	65			ns
HPL* setup time	^{t}HPS	60			ns
HPL* hold time	^{t}HPH	40			ns
Transition time (rise or fall)	^{t}T	3		10	ns
HCK* to video setup time	^{t}HVS			70	ns
HCK* to video hold time	^{t}HVH	190			ns
Video delay time	^{t}VD	890			ns
Video lead time	^{t}VL	890			ns
RENE*/RENO* power down pulse width	^{t}VRP	6.0			µs
PDR* to RENE*/RENO*	^{t}PRD	90			ns
Power Down Hold Time	^{t}PDH	890			ns

Notes

1. All voltages referenced to V_{SS}.
2. I_{VDD}, I_{VEE}, I_{VSS}, and PWR are dependent on operating frequency.
3. Values are obtained with display operating at 72 frames per second.
4. AC characteristics assume ^{t}T = 3 ns. Transition times are measured between V_{IH} (MIN) and V_{IL} (MAX), or between V_{IL}(MAX) and V_{IH} (MIN). All control signals must transit in a monotonic manner.
5. Alternation of HODL's logic state for every row plus alternation at row 0 of successive frames is required to support the pixel inversion driving scheme (see Figure 3-1). Alternation of HODL's logic state between successive frames is required to support the column inversion driving scheme (see Figure 3-3).
6. In order to equalize charge in the pixel array, a reset operation must be performed before power is removed from the CyberDisplay™ 320 . The PDR* signal is provided for this purpose, with the proper timing shown in Figure 3-6. It is generally sufficient to perform three complete row cycles after PDR* falls and before power is removed, but see the note with Figure 3-6 for a precise statement of timing requirements.
7. The "*" symbol indicates signal is active low.
8. Parameters for signals HCK*, HPL*, VCK*, VPL*, RENE*, RENO*, HODL, HLTOR.
9. Parameters for signal PDR*.

Figure 3-2: Vertical Timing

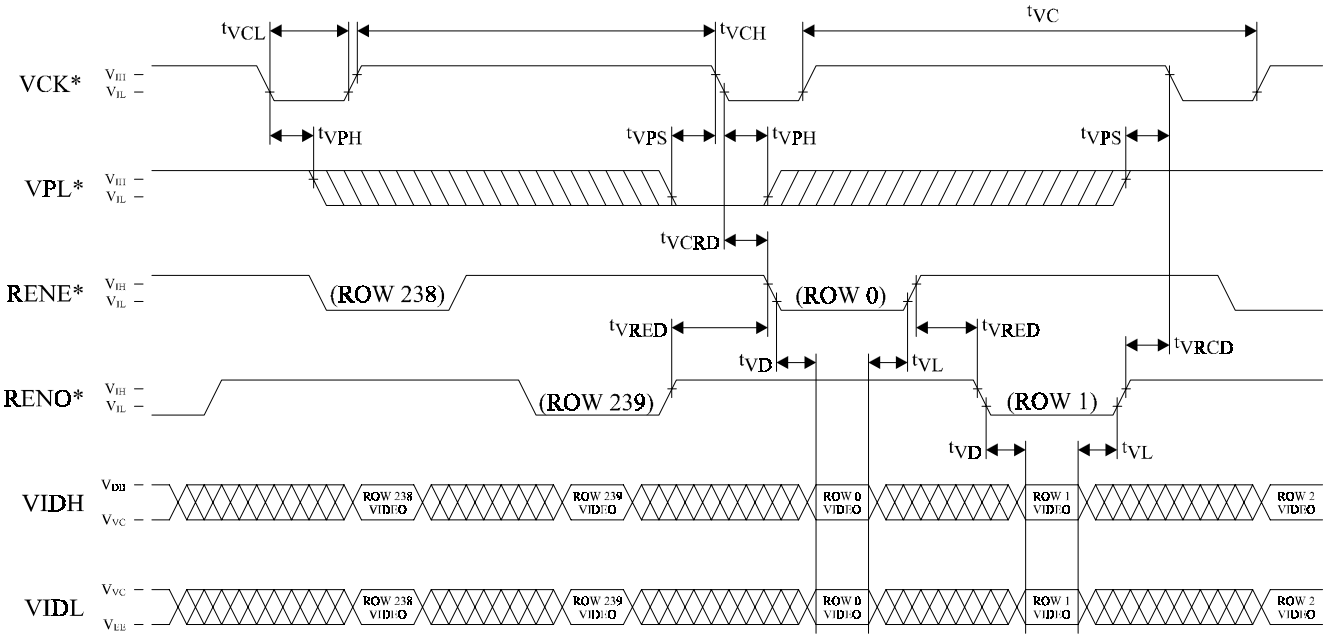
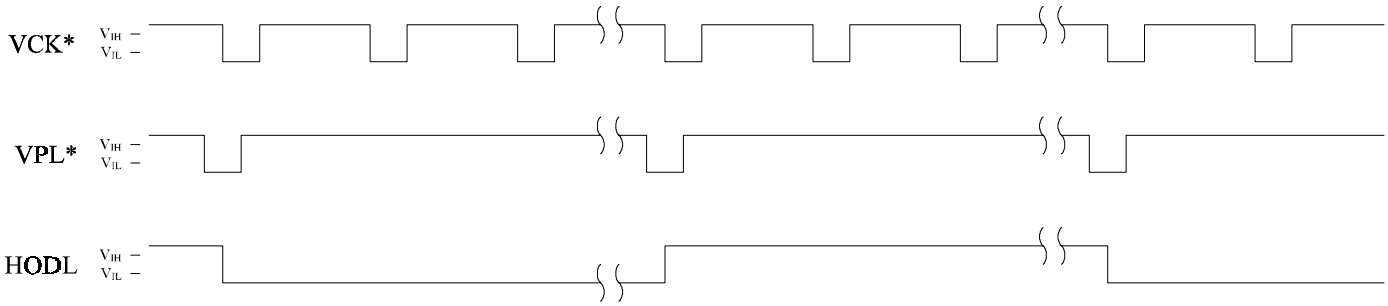
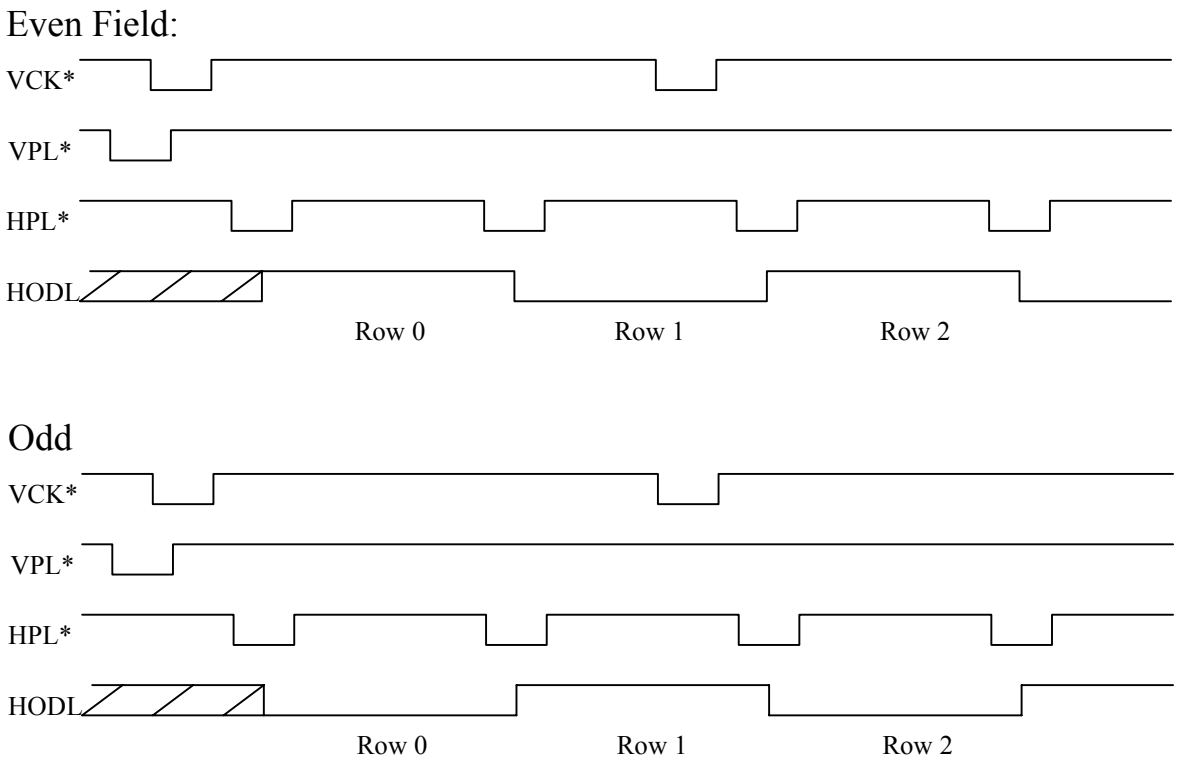


Figure 3-3: Column Inversion Timing



Note HODL's logic state must be altered between successive frames to support the column inversion driving scheme.

Figure 3-4: Pixel Inversion Timing



Note HODL must toggle every row, additionally the phase shall toggle every field.

Figure 3-5: Horizontal Timing

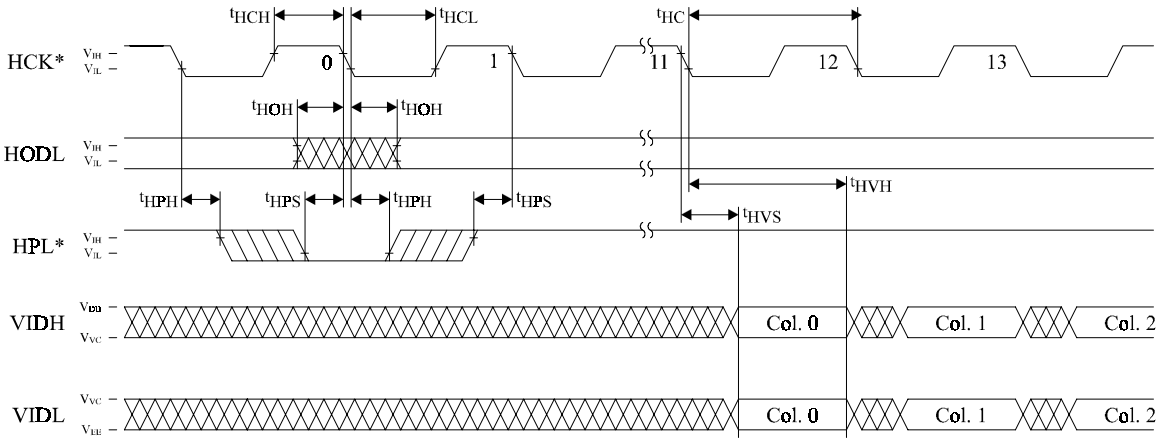
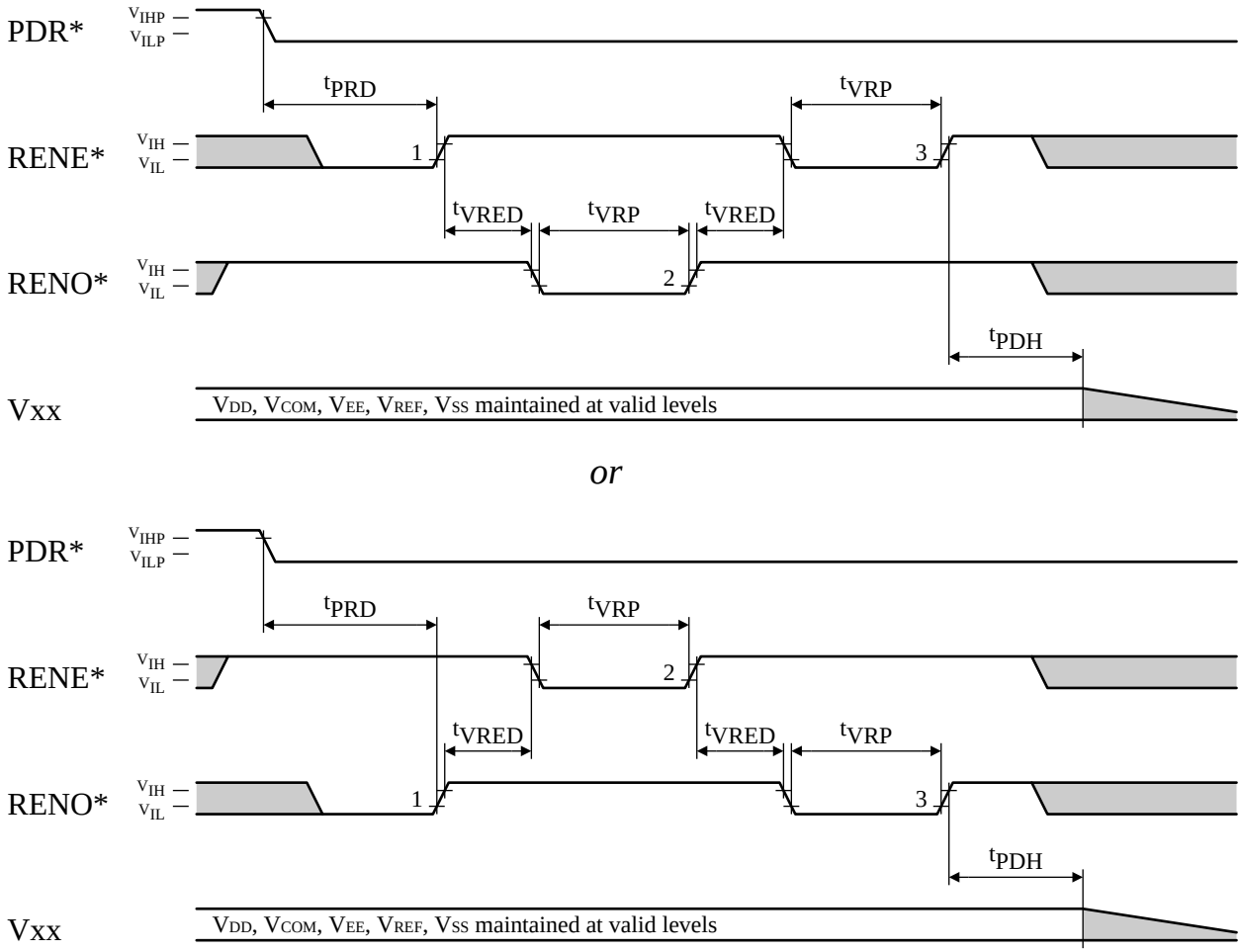


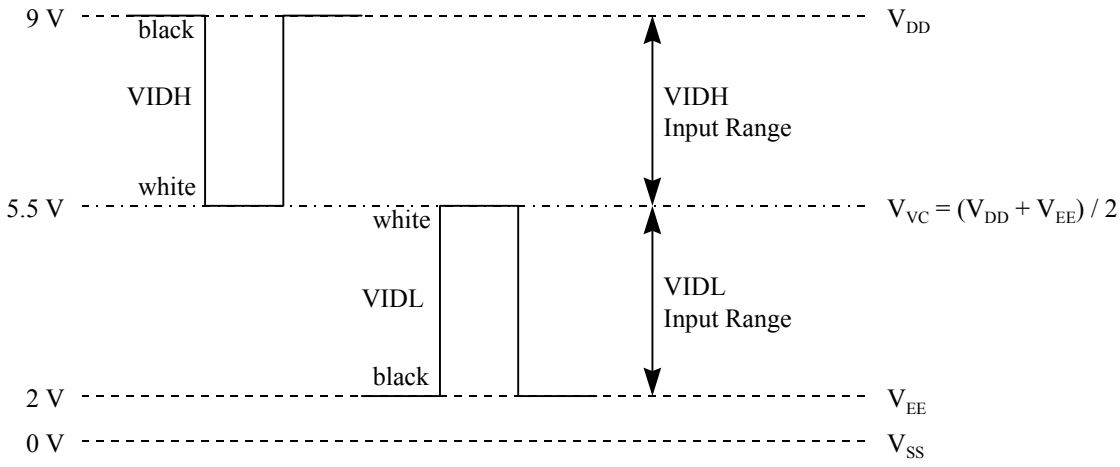
Figure 3-6: Power Down Cycle Timing



Note

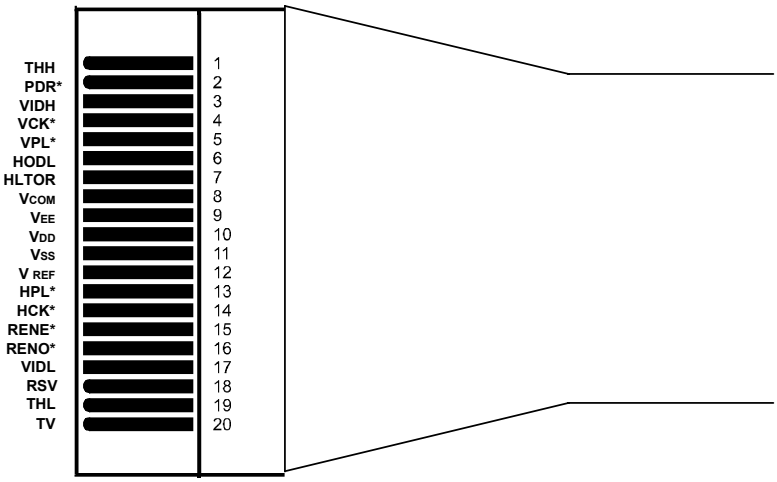
The power down timing requirements are satisfied if (1) at least three rising edges occur alternately on signals RENE* and RENO* at a time later than ^{t}PRD after PDR* falls, (2) supply voltages are held for at least ^{t}PDH after the third rising edge, and (3) the usual ^{t}VRED and ^{t}VRP constraints are met.

Figure 3-7: Typical Operating Voltages



3.2 Pinout Assignment

Figure 3-8: Pin Assignment Flex End



View through circuit flex. Contacts exposed on far side.

Table 3-6: Pinout Assignment

Pin No.	Symbol	Description
1	THH	Test pin. High H-shift register output
2	PDR*	Power Down Reset. Asserted low during power-down cycle
3	VIDH	High (positive polarity) video signal
4	VCK*	Vertical clock , V-shift register
5	VPL*	Vertical start pulse, V-shift register
6	HODL	Horizontal odd low. Asserted high for odd columns to receive low video input
7	HLTOR	Horizontal left to right. Asserted high for left-to-right scan
8	V_{COM}	Common voltage
9	V_{EE}	Supply voltage - Sink
10	V_{DD}	Supply voltage - Source
11	V_{SS}	GND
12	V_{REF}	Input level reference voltage
13	HPL*	Horizontal start pulse, H-shift register
14	HCK*	Horizontal clock, H-shift register
15	RENE*	Even rows enable
16	RENO*	Odd rows enable
17	VIDL	Low (negative polarity) video signal
18	RSV	Test pin. Must be grounded for proper operation of display
19	THL	Test pin. Low H-shift register output
20	TV	Test pin. V-shift register output

The * symbol indicates signal is active low

Note Pin 18 (RSV) must be tied to ground for proper operation of the display.

3.3 Display Interconnect

Display Interconnect	Flex PC, 1.86in free length, 20 conductor, 0.5mm pitch to mate with Molex 54550-2017, or equivalent connector.

3.4 Optical Characteristics

Table 3-7: Optical Characteristics

Parameter		Symbol	Min	Typ	Max	Units	Notes
Contrast ratio		CR_{25}	60	110			1
Optical transmittance		T	5.5	6.5		%	
Voltage-transmission characteristics	@ 90%	$V_{90\ 25}$	0.25	0.50	0.75	V	2
	@ 50%	$V_{50\ 25}$	0.75	1.25	1.75	V	
	@ 10%	$V_{10\ 25}$	1.5	2.0	2.5	V	
Response time		$t_{ON\ 25}$		15	20	ms	3
		$t_{ON\ 25}$		50	80	ms	
Flicker		F_{25}			–40	dB	4
Inter-column flicker		ICF_{25}			–40	dB	5
Image retention time		IRT_{25}			60	s	6
Line stick retention intensity	t=0	$LRI_{0\ 25}$			–8	dB	7
	t=120s	$LRI_{120\ 25}$			–13	dB	
Transmission uniformity		TU		0.5	1.5	Δ%	8
Chromatic uniformity		CU		0.002	0.01	u',v'	9
Color gain		CG		2000	2500	K	10

3.4.1 Measurement Conditions

All measurements performed at 25°C ambient temperature. Powered measurements are performed with displays driven at 50 Hz field rate, 25 Hz pixel inversion, and typical voltage settings of Table 3-2.
Polarizer orientation 90 degrees ITO side (facing viewer), 0 degrees TFT side (facing backlight).

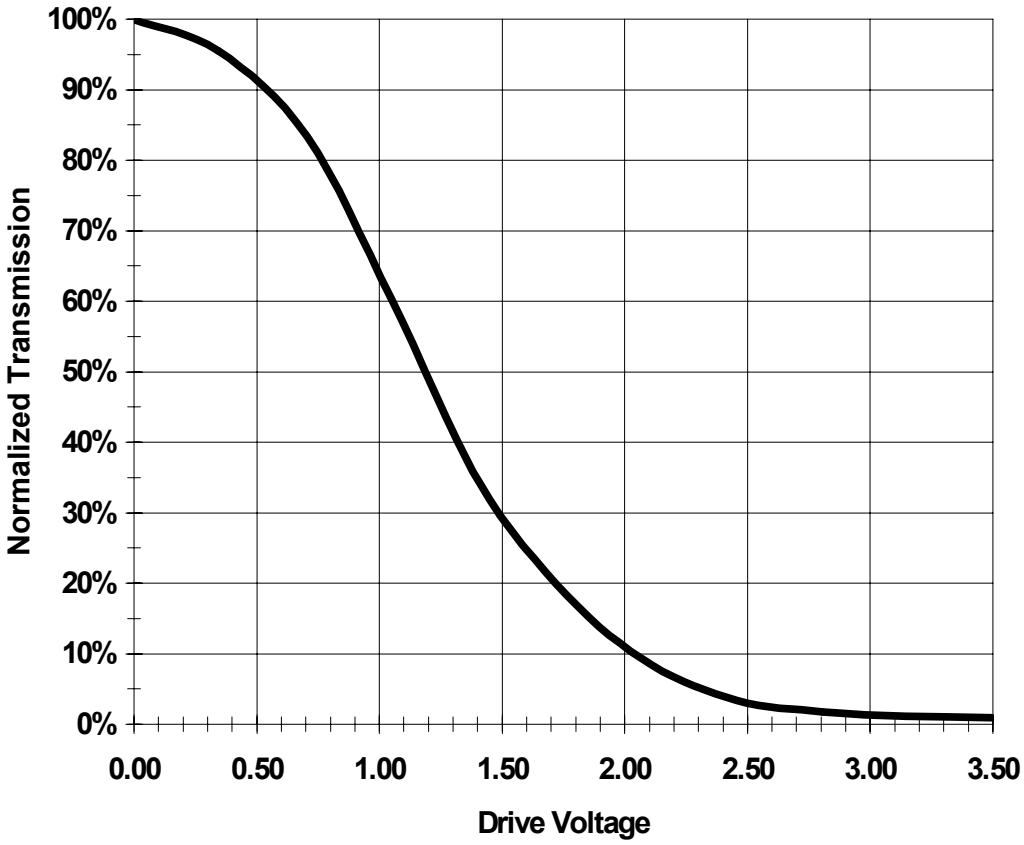
3.4.2 Measurement Equipment

Parameters TU, CU, and CG are measured with unpowered displays using a PR650 Spectrometer.
Image retention time (IRT_{25}) is a visual measurement.
All other parameters are measured using a PR880 Photo Research Photometer, with optics having 3° acceptance angle.

Notes

1. Ratio of white image/black image (White 0, Black 3.5V).
2. Drive voltages specified are half peak-to-peak amplitudes.
3. Parameters t_{ON} and t_{OFF} measure 90–10% and 10–90% transitions respectively.
4. 20log (50Hz AC / DC) with 50% gray image.
5. 20log (25Hz AC / DC) with alternating black and white columns.
6. Decay time to less than 1% full gray scale.
7. 20log(25Hz AC / DC) with 50% gray image.
8. 5-point measurement of percent transmission, reporting maximum difference from center.
9. 5-point measurement of CIE 1976 color coordinates, reporting radius in (u', v') space.
10. Absolute difference in color temperature of light entering and exiting unpowered display. Typical backlight color temperature is 8000K.

Figure 3-9: Transmission-Voltage Characteristics



4. Mechanical Specifications

4.1 Display Packaging

The CyberDisplay™ 320 display is factory sealed into a polycarbonate module. This module performs the following important functions:

- Seals the display from the environment.
- Contains and protects the two polarizing elements.
- Provides robust strain relief for flex PC cable.
- Provides visual framing of the display aperture.
- Masks extraneous light from the backlight.
- Provides mechanical interface with precise registration.

The CyberDisplay 320 Display Module is designed for snap assembly to Kopin CyberLite™ backlight module. Customers providing their own backlights can register to the features provided on the display module. Four notches in the viewing face are intended to interface with snap features on the backlight. Two notches in the input face of the module can be used to attach the module from the other side.

The flexible PC cable is strain relieved, but tugging forces should be limited to less than 1 lb. in any direction. The minimum inside bend radius for the cable is .03 inches. Repeated reformings are not recommended.

Figure 4-1. CyberDisplay™ 320 Display Package

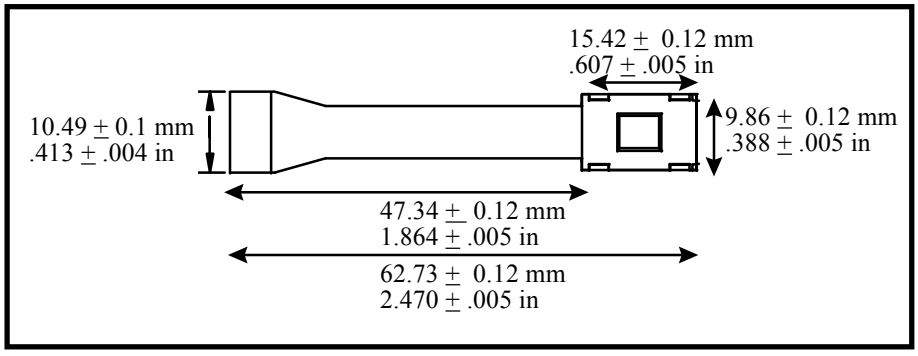
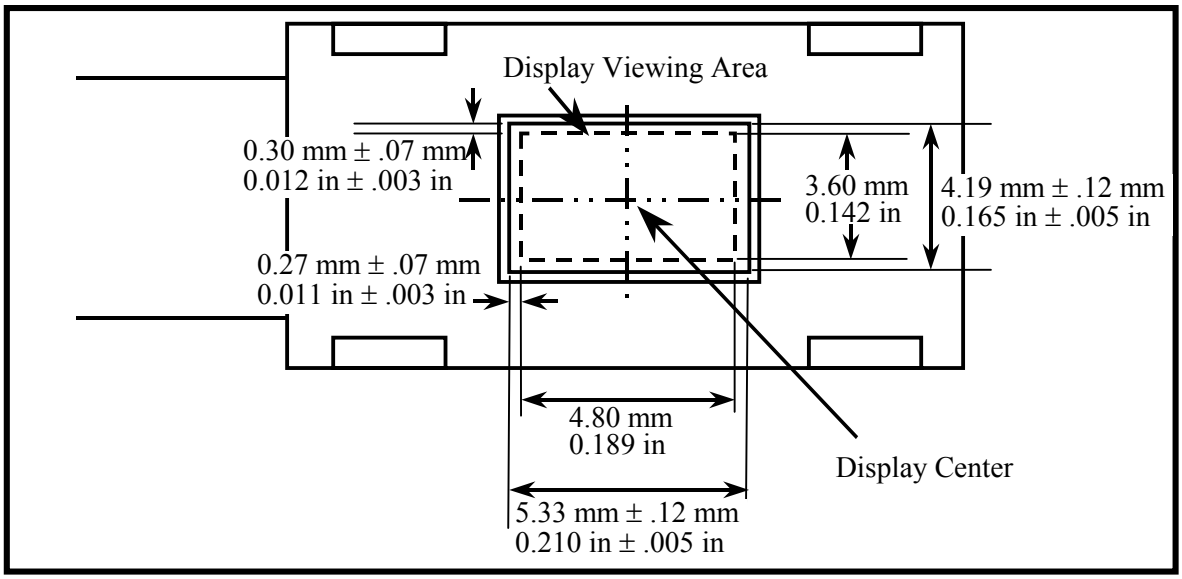


Figure 4-2. CyberDisplay™ 320 Display Dimensions Side View

Figure 4-3. CyberDisplay™ 320 Display Dimensions Viewing Area



4.2 Display Packaging

The flexible PC cable is strain relieved, but tugging forces should be limited to less than 0.5 kg perpendicular to the display and less than 1 kg parallel to the display. The minimum inside bend radius for the cable is .03 inches. Repeated reformings are not recommended.

Table 4-1: CyberDisplay™ 320 Display Environmental Specification

Storage Temperature	-20°C to 80°C
Operating Temperature	-20°C to 60°C
Humidity - Storage	40°C at 80% humidity for 240 hours
Vibration	20 to 2,000 Hz, 6G's RMS maximum 3 axes 10 minutes each axis
ESD - Human Body Model	2500V Electrical Discharge

5. Display Appearance

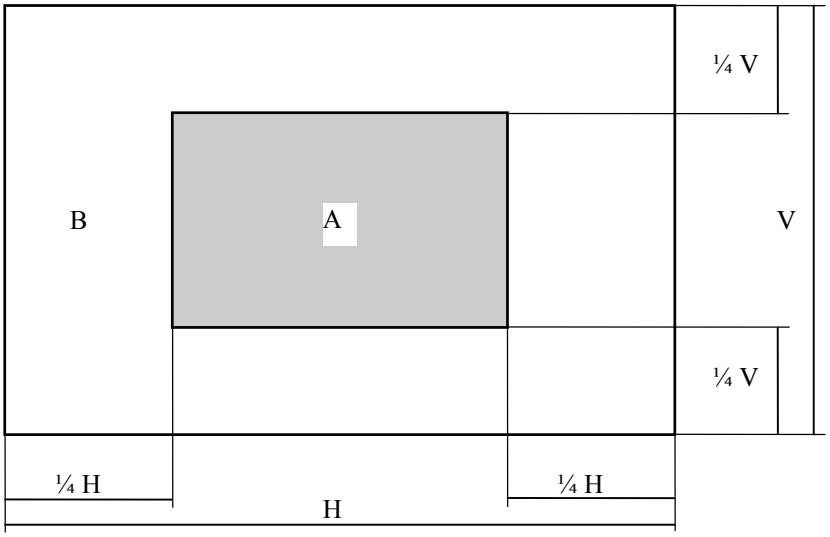
Table 5-1: Display Appearance

Defect Type	Defect Criteria
Circuit	No partial or faded image, no streaking or shadow, no unstable image, no alternating columns or rows
Line	No lines out Very faint lines allowable based on limit samples
Pixel	See Figure 5-1
Adjacent pixels	Two: Same criteria as for pixel defects, based on aggregate brightness (See Figure 5-1) Three or more: Not allowed

Test Conditions: Test board runs in pixel inversion at 30 or 25 Hz frame rate (NTSC or PAL). Visual focal plane is on the pixel array.

Limit Samples: Limit samples to be used for pixel and other cosmetic defects.

Figure 5-1: Display Appearance Specification



ZONE	DEFECT	NUMBER
A	S, M, or L	1
B	S or M	4
	L	1

where:

Small (S) defect differs from nominal pixel brightness by 10–25%.
Medium (M) defect differs from nominal pixel brightness by 25–75%.
Large (L) defect differs from nominal pixel brightness by ≥ 75%.
Defect can be black or white spot.