Lab Zero [Warmup and Recap]

Variable Latency Multiplier

Implement a 16 bit unsigned fixed point multiplier [fixed latency].

Now improve the multiplier so that it becomes a variable latency implementation. We discussed very briefly the Booth Multiplier. You can go through this link for a succinct introduction. A more rigorous treatment is available in Moodle.

Report the area degradation in the new implementation. Your top level module should have clock, *a* and *b* as inputs and should produce ***c*** and *number of clock cycles* as output. The Test Bench should instantiate this module and you should run the simulation with ~500 random a's and b's to show that statistically, the variable latency multiplier uses a lower number of cycles. Also record at least 5 instances of a and b which result in *poorer* performance wrt time.

Deliverable:

Zip file containing your HDL code and a pdf document detailing the design principles used and the results [screenshots] of the running the simulation.