**Documentation** 15CS01025

**Components:**

1)General purpose registers - 32

2) Memory- R.A.M(14-bit Address &32-bit Data)

3) Special Registers- RA, RB, RC, RZ, RY

4) Instructions- 8(ADD, SUB, AND, OR, MVI, LOV, LOAD, STORE)

\* Clock cycles per instruction- 4

**Instruction Register:**

OOO AAAAA BBBBB CCCCC XXXXXXXXXXXXXX (32-BIT)

OOO (3) - OPCODE

AAAAA (5) - RA (SOUR 1)

BBBBBB (5) - RB (SOUR 2)

CCCCC (5) - RC (DEST)

XXXXXXXXXXXXXX (14) - IMMED

**Instruction Set:**

|  |  |  |
| --- | --- | --- |
| **Opcode** | **Instruction** | **RTN** |
| 000 | ADD RA, RB, RC | RC<-[RA]+[RB] |
| 001 | SUB RA, RB, RC | RC<-[RA]-[RB] |
| 010 | AND RA, RB, RC | RC<-[RA]AND[RB] |
| 011 | OR RA, RB, RC | RC<-[RA]OR[RB] |
| 100 | MVI X, RC | RC<-X |
| 101 | MOV RB, RC | RC<-[RA]+[RB] |
| 110 | Load (RB), RC | RC<-[[RB]] |
| 111 | Store RA, (RB) | ([RB]) <-[RA] |

**Example Instructions:**

|  |  |  |
| --- | --- | --- |
| **INSTRUCTIONS** | **ENCODED INSTRUCTION (IR CONTENT)** | **Following Changes** |
| 1. MVI 2H, R2 | 100 00000 00010 00000 00000000000010 | R2 = 2 |
| 1. MVI 1H, R1 | 100 00000 00001 00000 00000000000001 | R1 = 1 |
| 1. MOV R2, R3 | 101 00000 00011 00010 00000000000000 | R3 = R2 = 2 |
| 1. STORE R1, (R2) | 111 00001 00000 00010 00000000000000 | MEM\_DATA\_WITH\_ADDRESS (2) = 1 |
| 1. LOAD (R2), R4 | 110 00000 00100 00010 00000000000000 | R4 = MEM\_DATA\_WITH\_ADDRESS (2) |
| 1. ADD R1, R2, R5 | 000 00001 00101 00010 00000000000000 | R5 = R1 + R2 = 3 |
| 1. SUB R2, R1, R6 | 001 00010 00110 00001 00000000000000 | R6 = R2 – R1 = 1 |
| 1. AND R1, R2, R7 | 010 00001 00111 00010 00000000000000 | R7 = R1 AND R2 = 0 |
| 1. OR R1, R2, R8 | 011 00001 01000 00010 00000000000000 | R8 = R1 OR R3 = 3 |