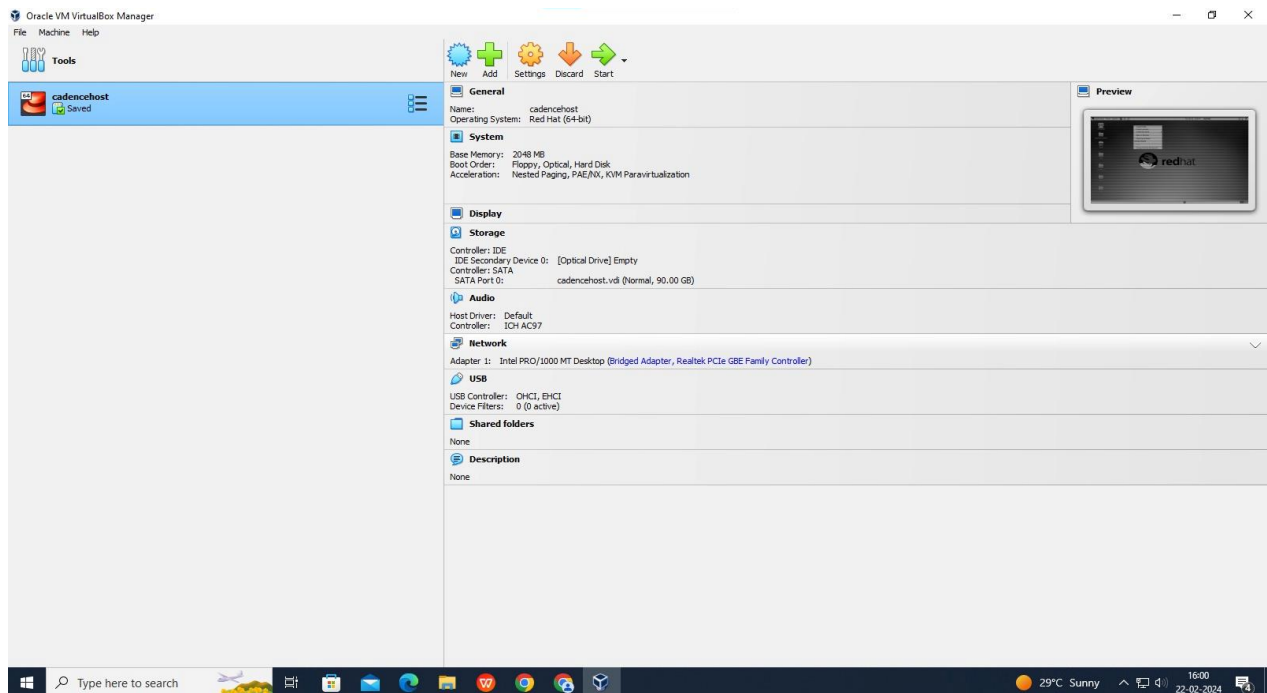


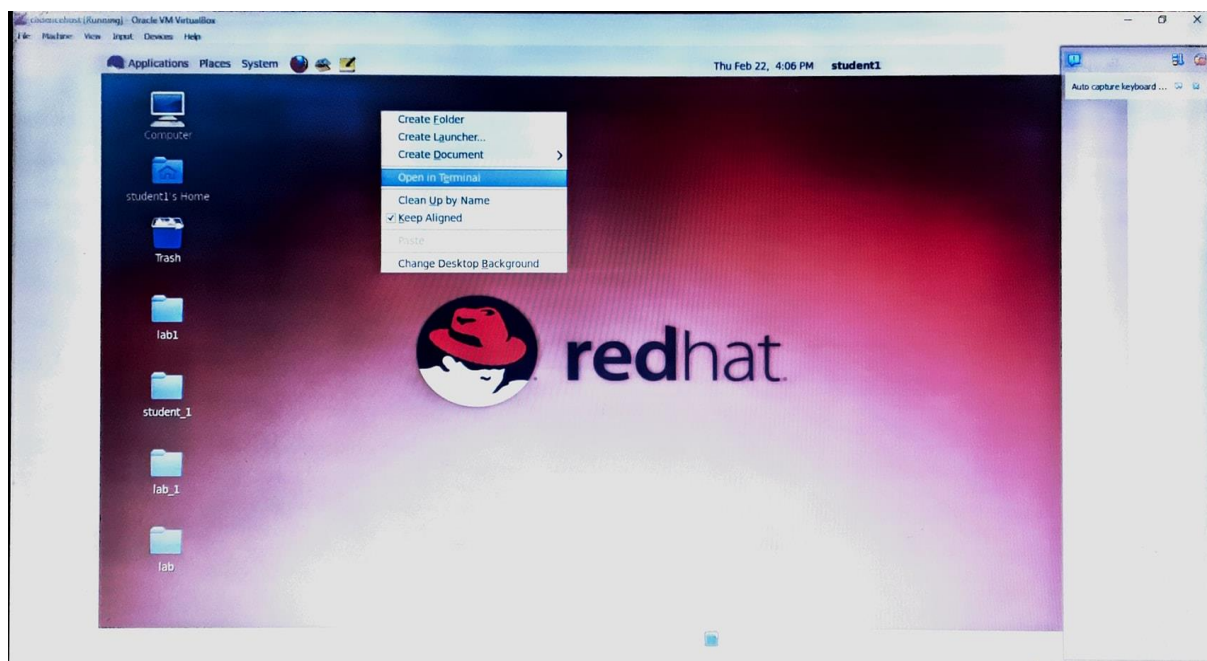
# STEPS TO IMPLEMENT IV CHARACTERISTICS OF NMOS USING CADENCE TOOL

## STEP-1: LIBRARY CREATION

- 1) Open oracle VM virtual box
- 2) Click on start



- 3) Right click on workspace, select **open in terminal**



4) Type the commands

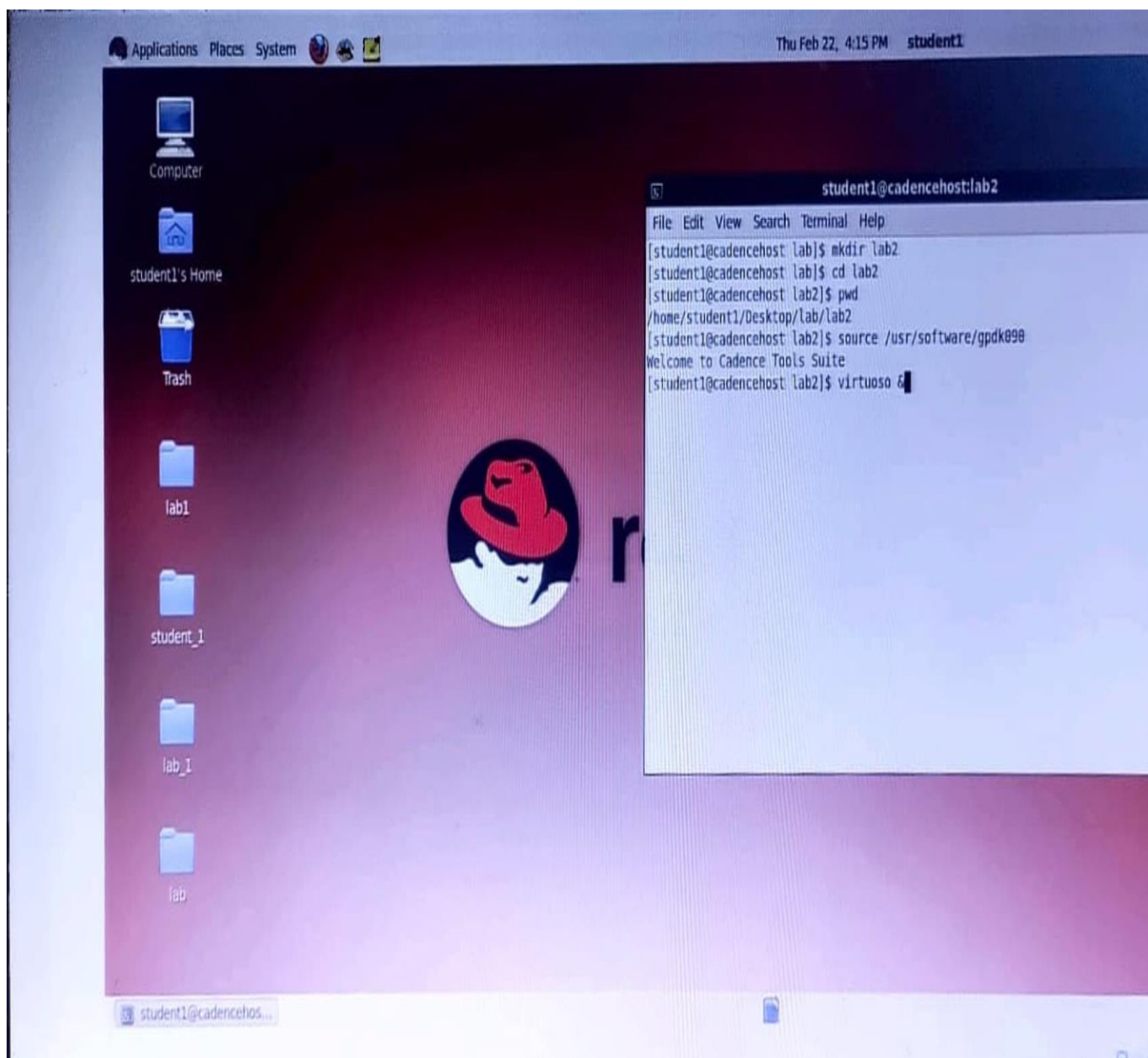
**mkdir** <any name> (ENTER)

**cd** <any name> (ENTER)

**pwd** (ENTER)

**source /usr/software/gpdk090** (ENTER)

**virtuoso &** (ENTER)



### EXPLANATION:

mkdir: This command is used to create a new directory (folder) within the current directory.

cd: Short for "**change directory**," this command is used to navigate between directories. For example, `cd folder_name` would move you into the directory named "folder\_name."

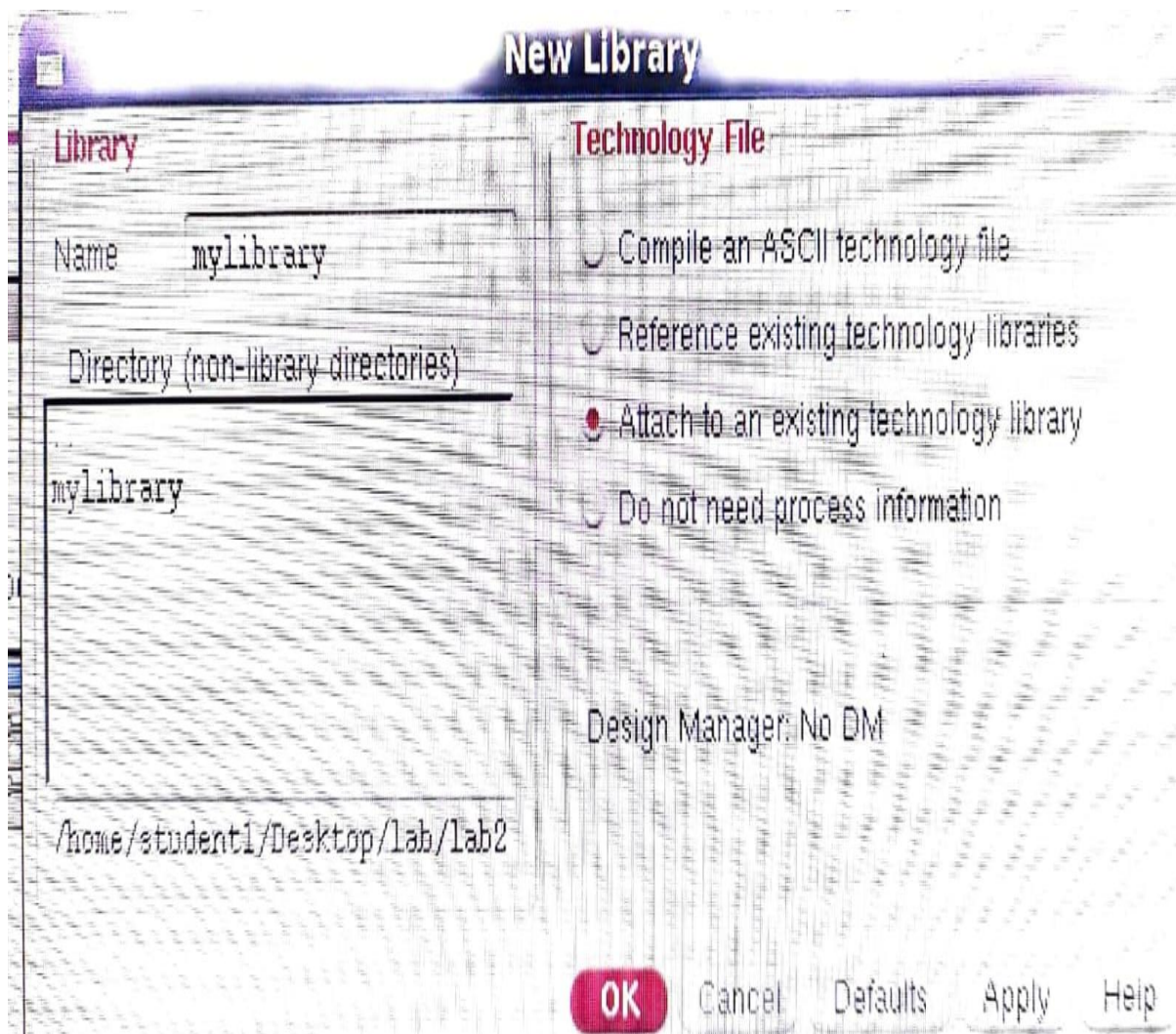
pwd: Short for "**print working directory**," this command shows you the full path of the current directory you are in.

virtuoso: Virtuoso is a widely-used tool within Cadence for electronic design automation (EDA). It's primarily used for designing and simulating integrated circuits (ICs) and electronic systems. It includes various modules for schematic capture, layout editing, simulation, and more.

5)virtuso tab appears

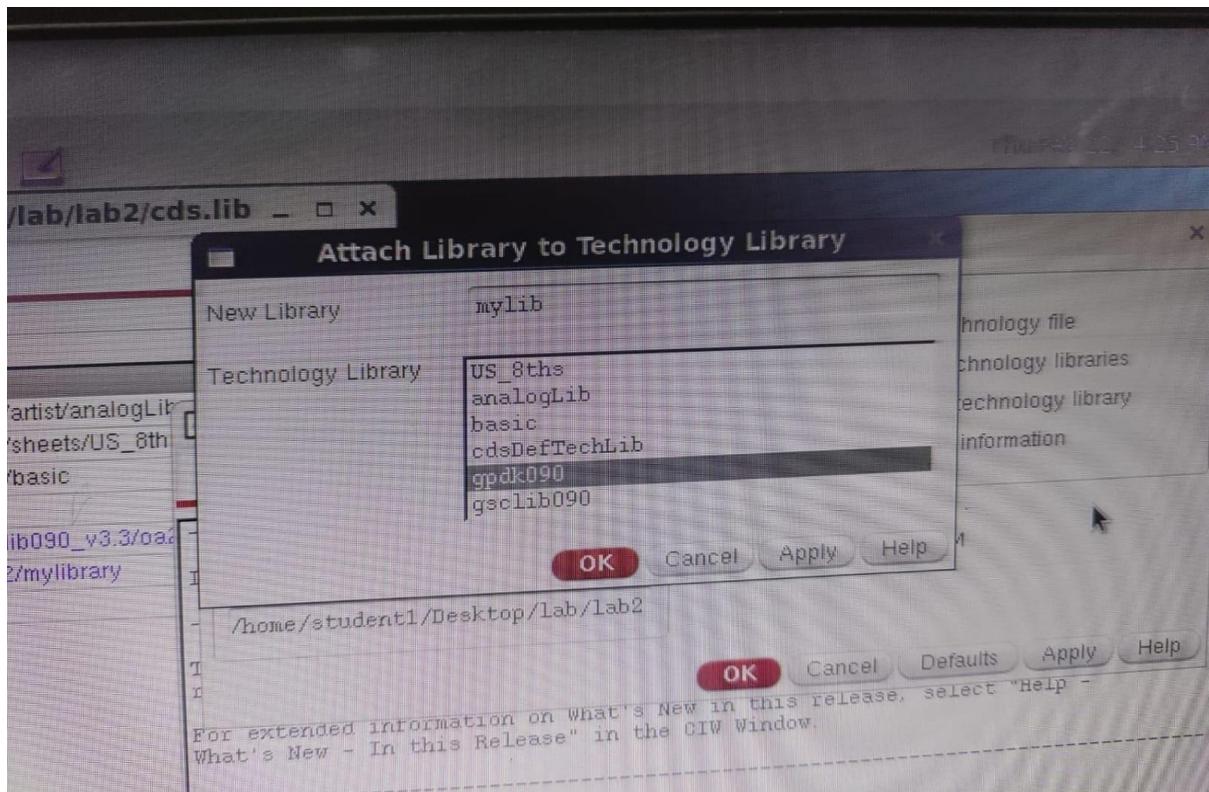
6)In virtuoso tab

- File>New>Library>mylib(give any name)>select Attach library to technology>Ok



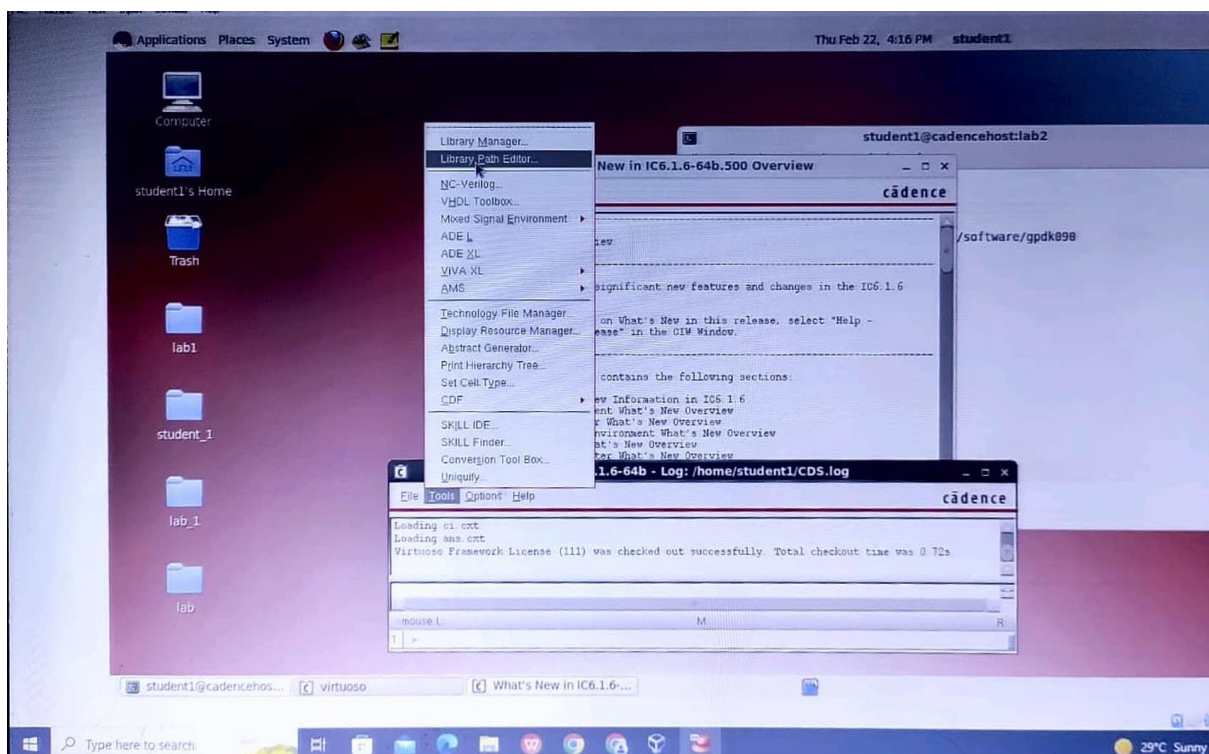


- Select **gpdK090**>Ok



Again in Virtuoso tab

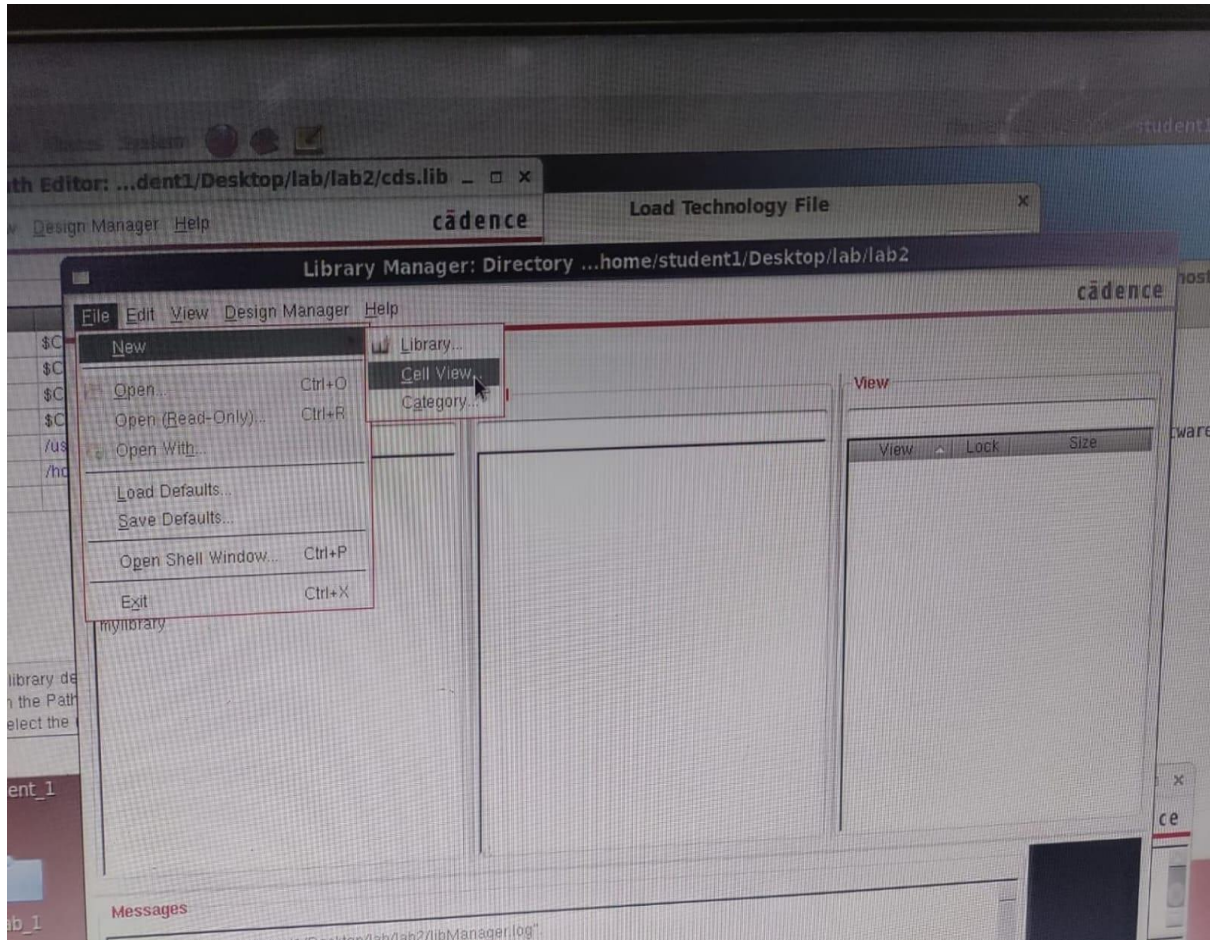
- Tools>Library Manager>mylib



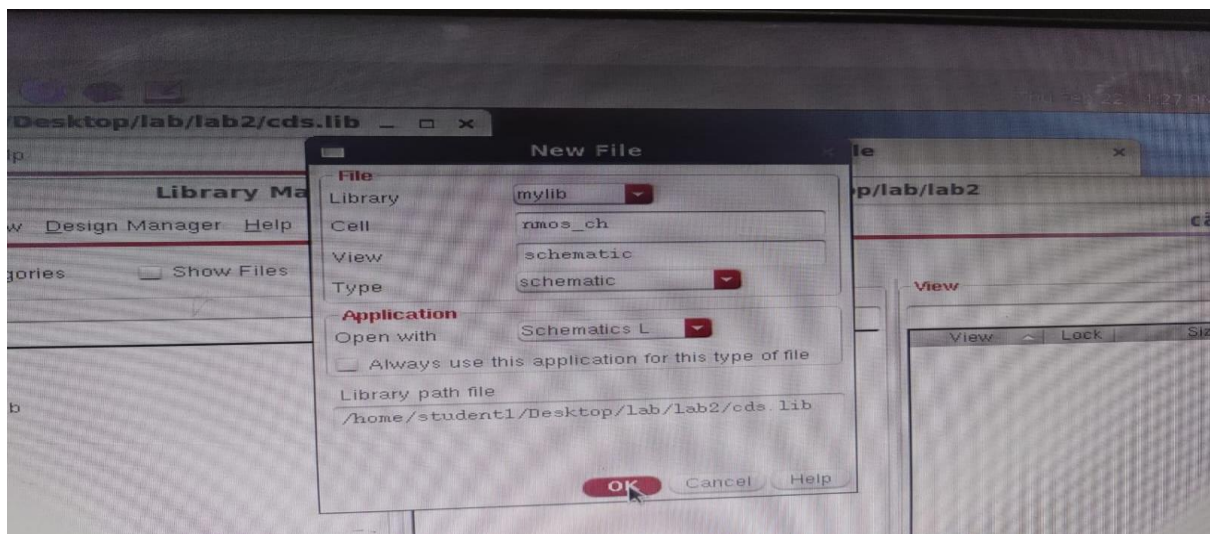
## STEP-2:LIBRARY MANAGING(SET UP CONNECTIONS AND ADD VALUES)

7)In mylib

- File>New>cell view



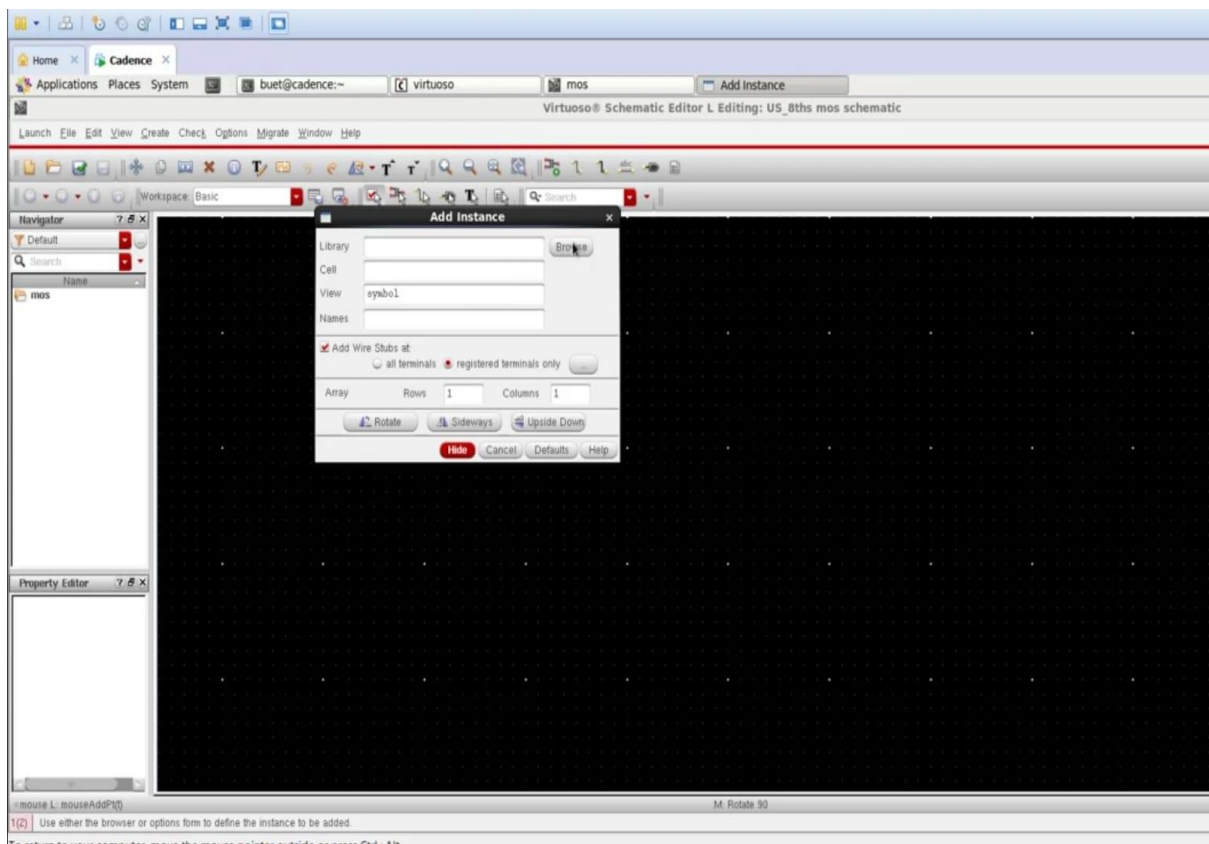
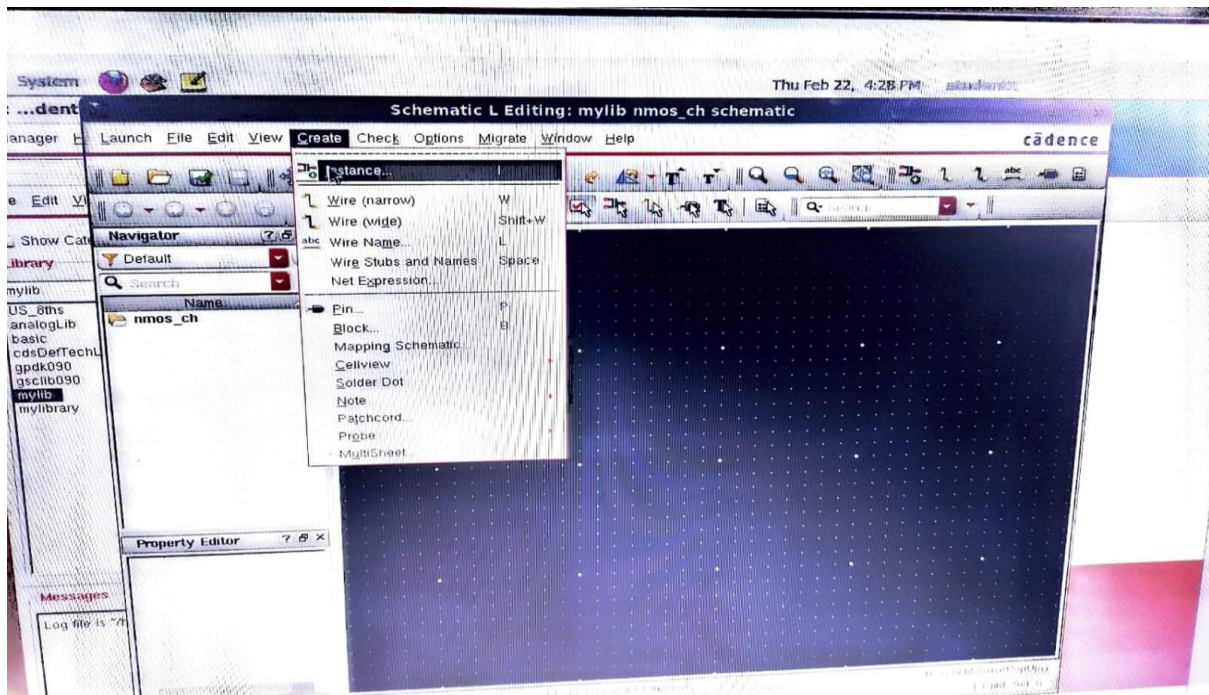
- Enter cell view:nmos\_ch



- Select OK



8) Create>Instance(shortcut-press “I”)>Browse



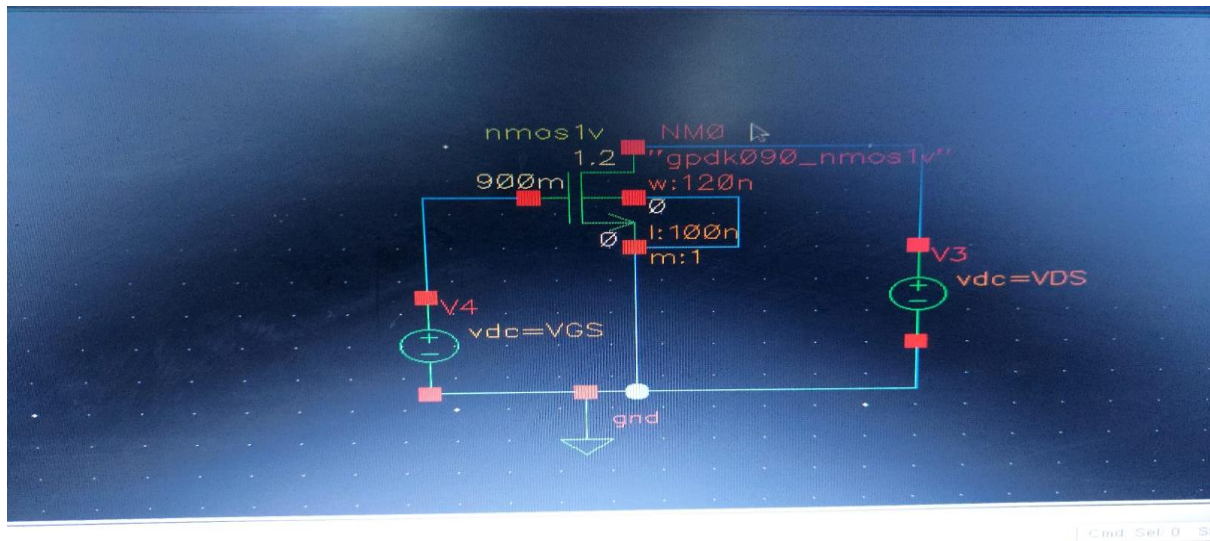
- Select the following and place it on the schematic Editing window each time.

- Select vdc twice.

Library	Cell	View
gpd090	nmos1v	symbol
analoglib	vdc	symbol
analoglib	gnd	symbol

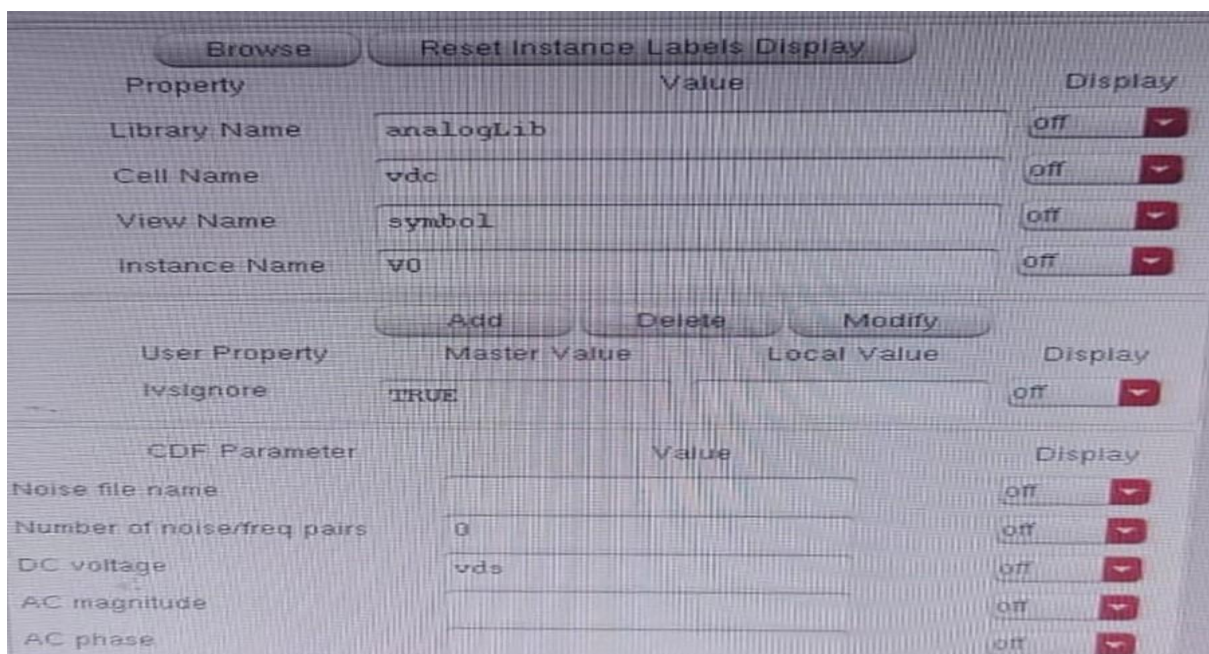
9) Set up the connections as shown

Press “W” for wire to connect the circuit



10) Select vdc connected to drain

- Right click > Properties (or) Press “Q” (shortcut key for properties)
- Type DC Voltage: **vds**



11) Select vdc connected to gate

- Press “Q”
- Type DC Voltage: **vgs**

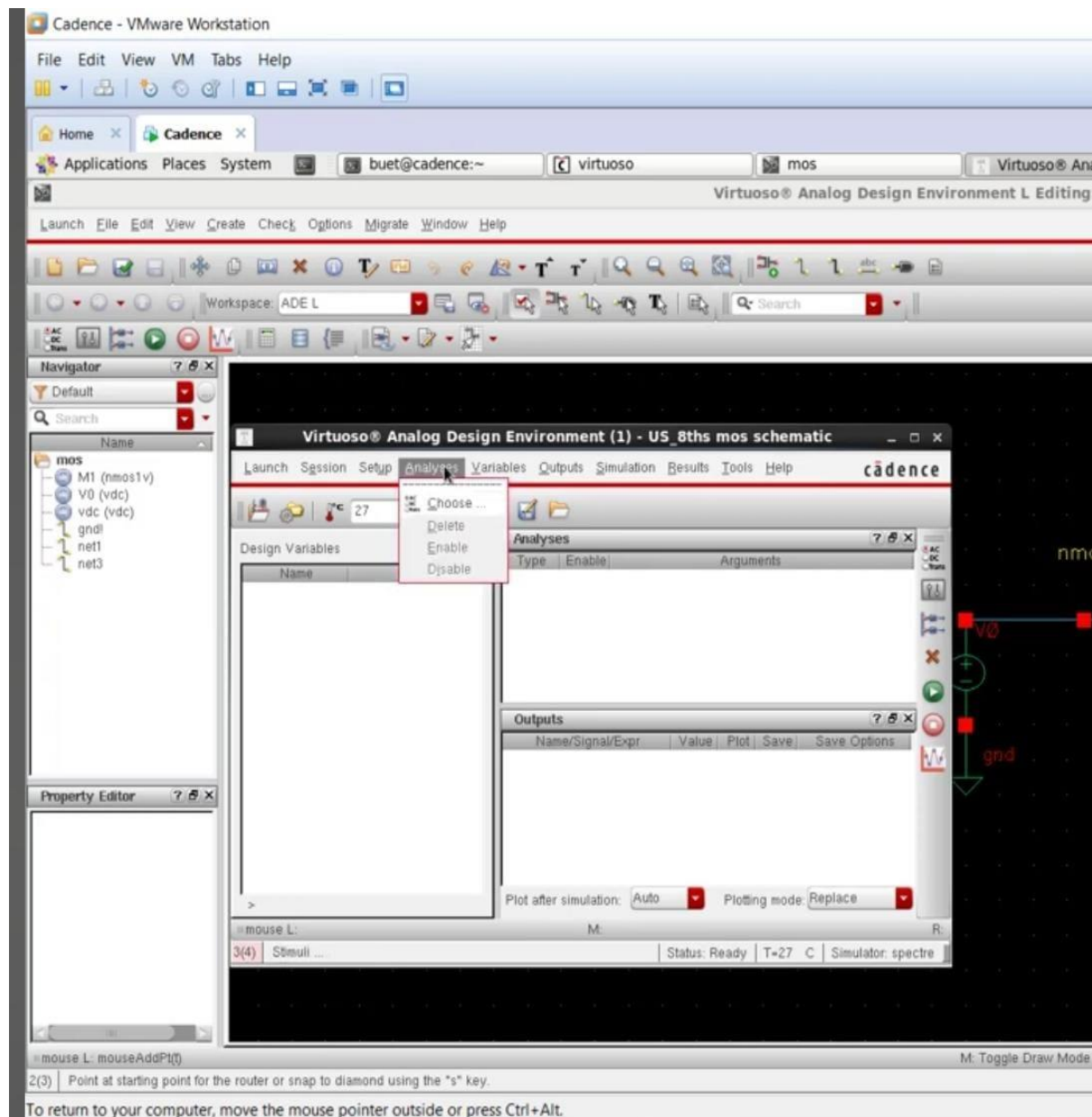
12) Launch > ADE L

- Select variables > copy from cell view
- Give values as **vds:900m, vgs:1.2m**

### STEP-3: INPUT CHARACTERISTICS

13) In ADE L right corner

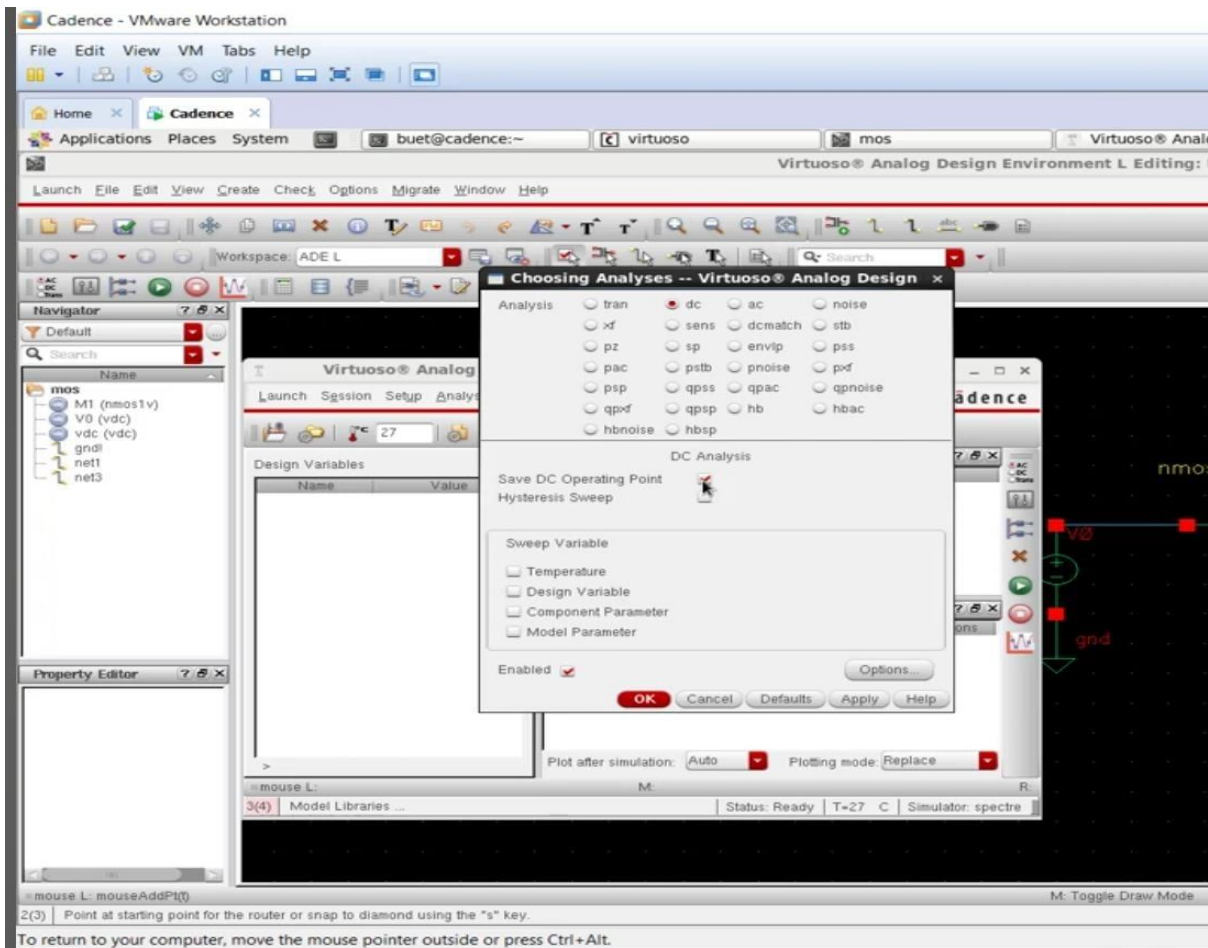
Analyses > Right corner Choose **DC**



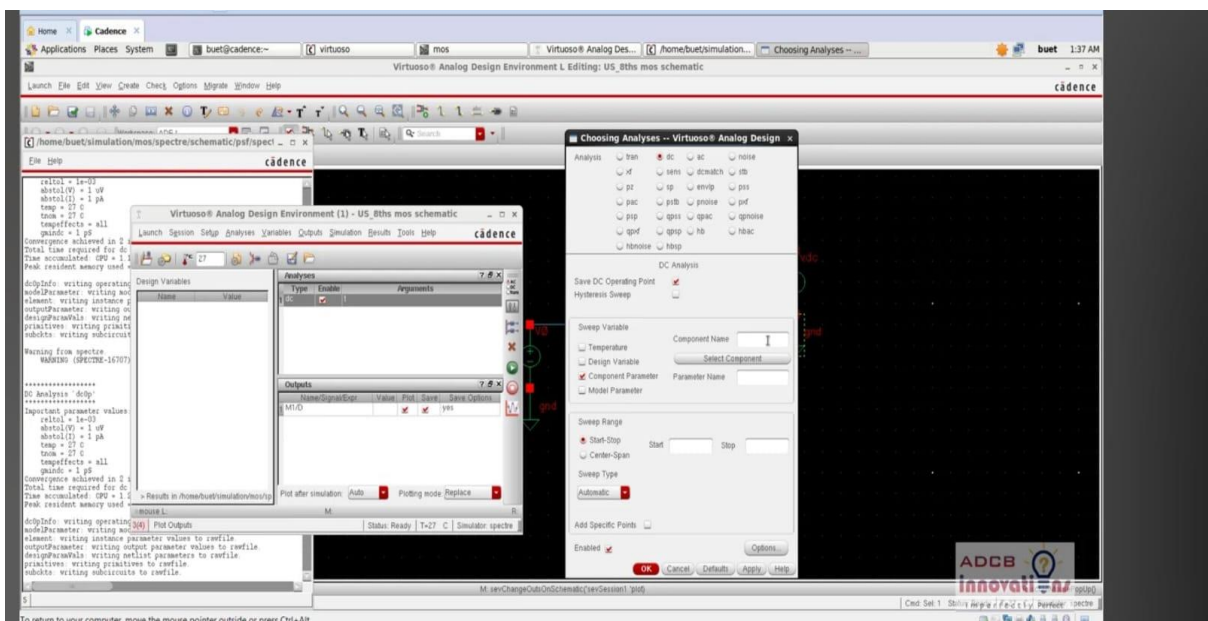


In DC

- Select save DC
- Select DC Analyses



Component parameter>Select Component

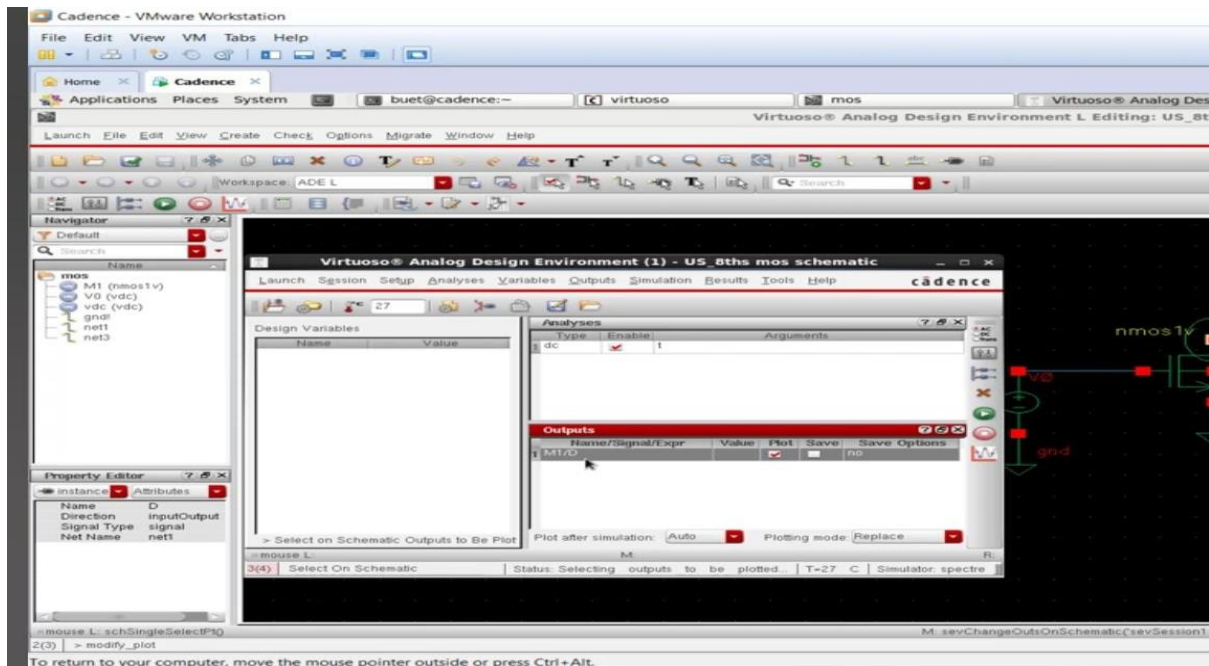


14) Again in Analyses Tab

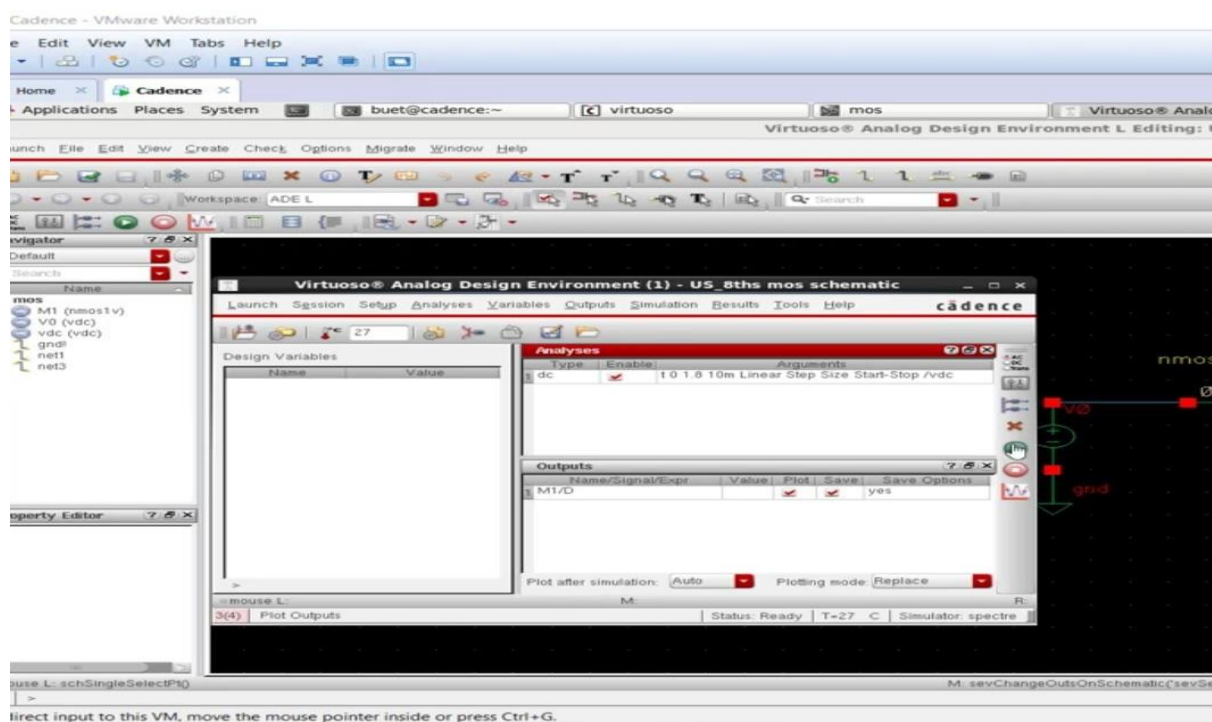
Set values as Start:0 Stop:1.2

15) Select **Output Setup**(Right corner side in ADEL Tab)

- Click on drain node and select from schematic window to obtain drain current



Select **Netlist and Run**(Right Corner side in ADE L Tab)





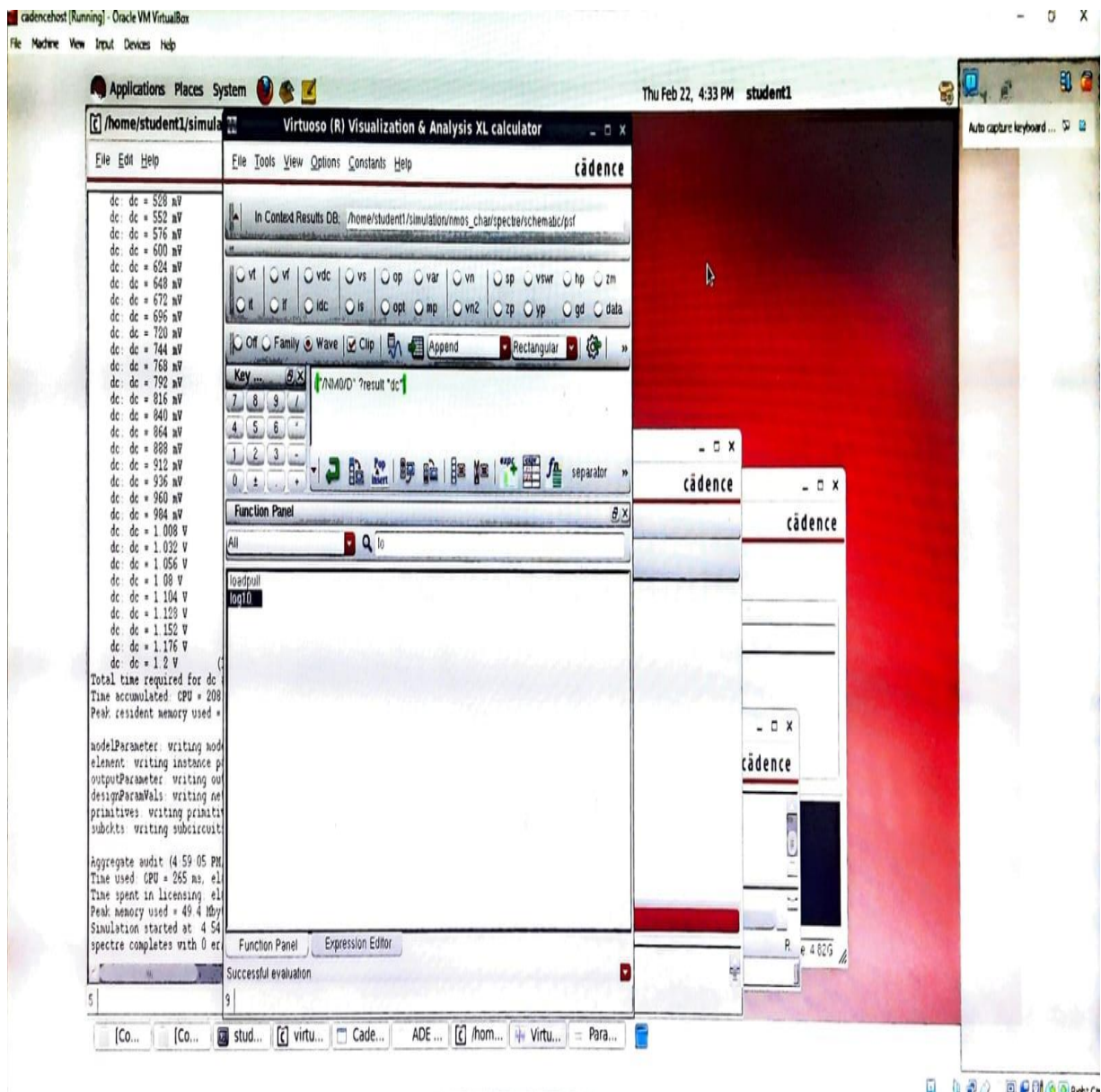


- Right click on graph>Properties>choose background color

Select “V”(shortcut to check the Threshold Voltage)

16)In Graph tab

- Click on calculator symbol on the top of the window)
- In that select wave and click on wave form window



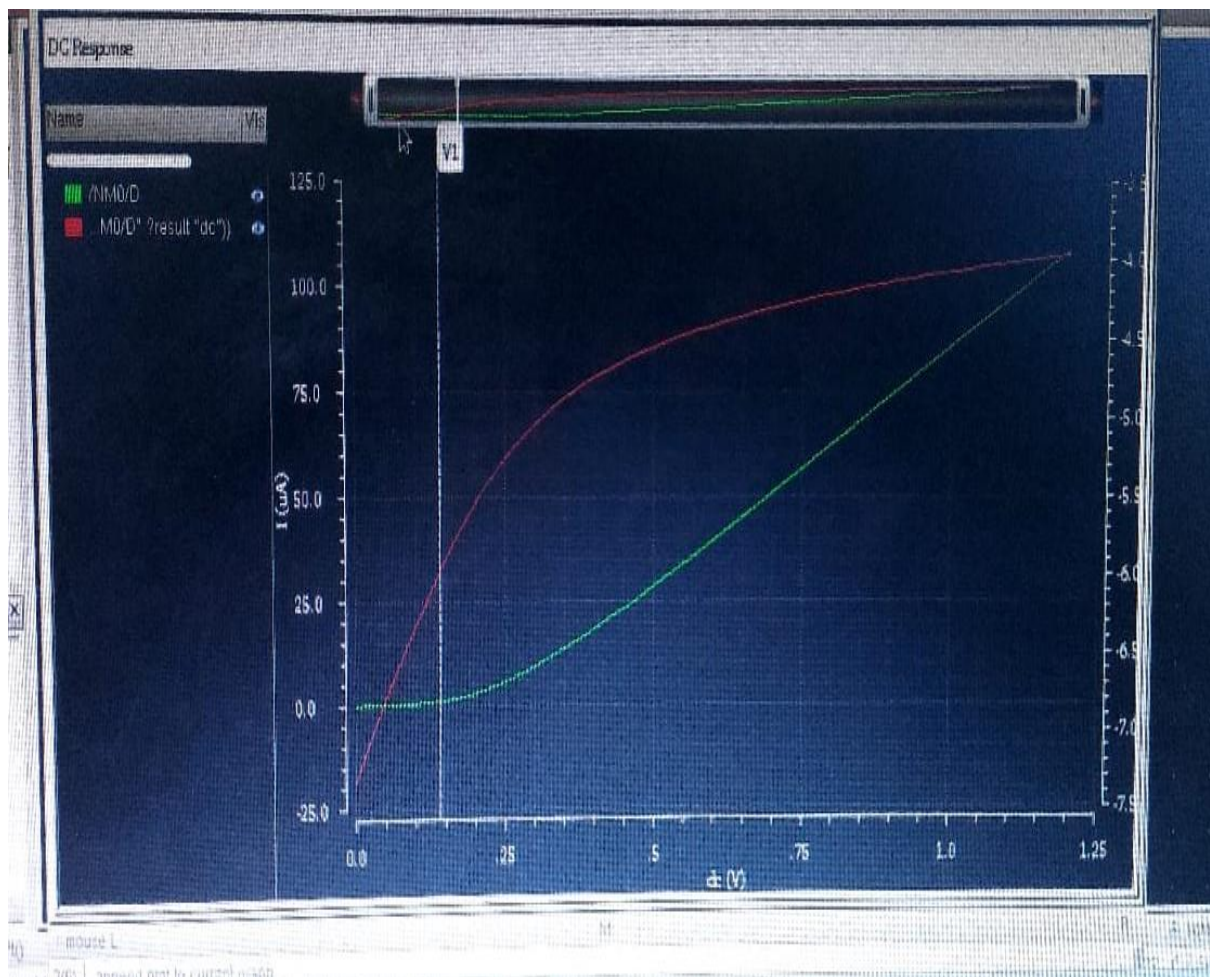
In Stack window>Function panel>Select All in function drop down>search for log10>select log10>click plot(present on top of the window adjacent to calculator)

#### STEP-4:OUTPUT CHARACTERISTICS

17)Go back to ADE L Window > Choose Analyses Dc>Choose parameter>Select vds on schematic window

In Pop-up:Select dc>Ok>Run

In ADE L > Change plotting mode to New win



#### **PARAMETRIC ANALYSIS**

18)In ADE L window

Tools>Parametric Analysis>Parametric set>Click on Add variable>select vgs

Value list:0 0.2 0.4 0.6 0.8 1.0 1.2

