



## 1. Description

### 1.1. Project

Project Name	iW-CORE-BOARD
Board Name	custom
Generated with:	STM32CubeMX 6.13.0
Date	05/23/2025

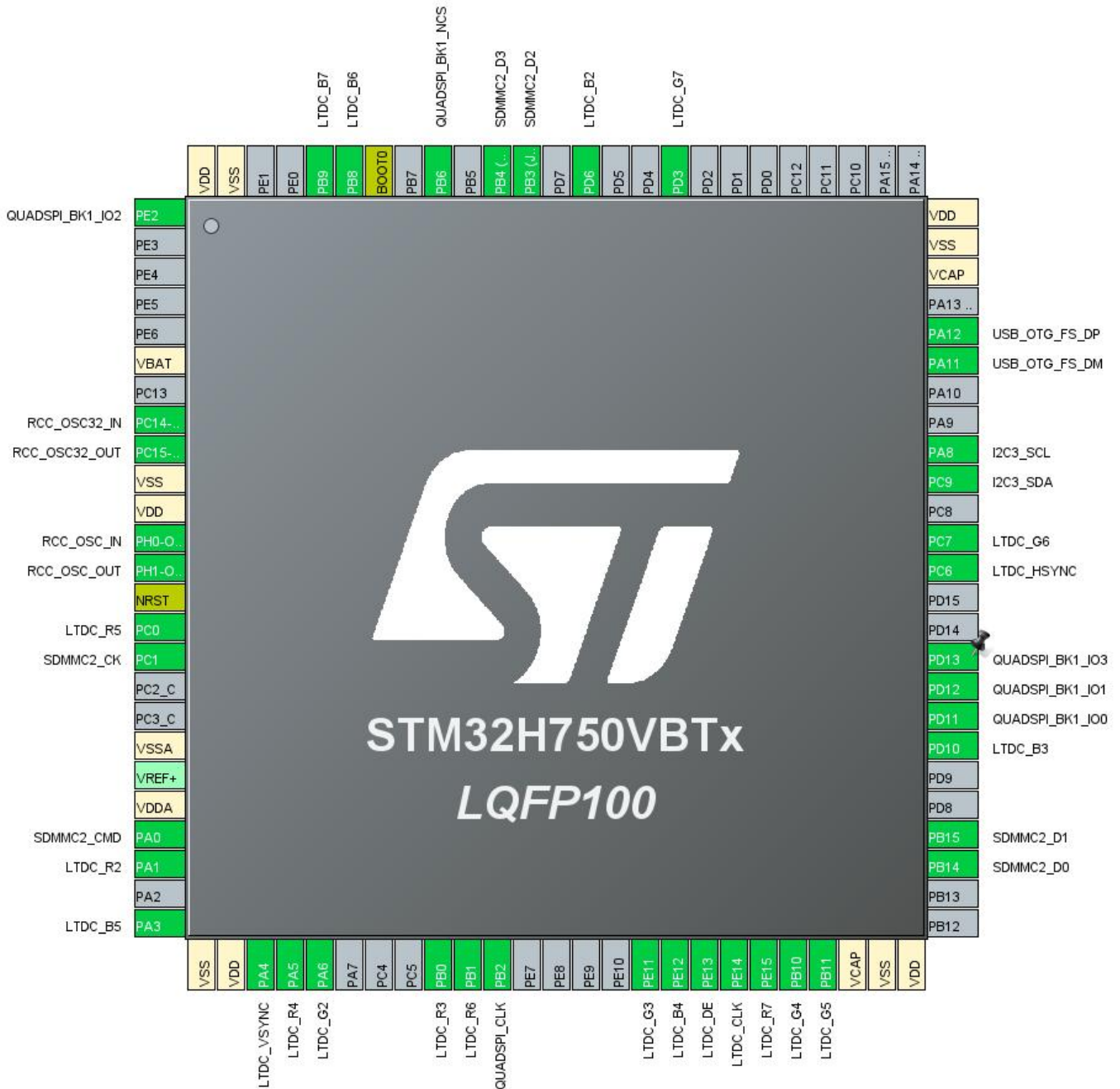
### 1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H750 Value line
MCU name	STM32H750VBTx
MCU Package	LQFP100
MCU Pin number	100

### 1.3. Core(s) information

Core(s)	ARM Cortex-M7
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## 2. Pinout Configuration

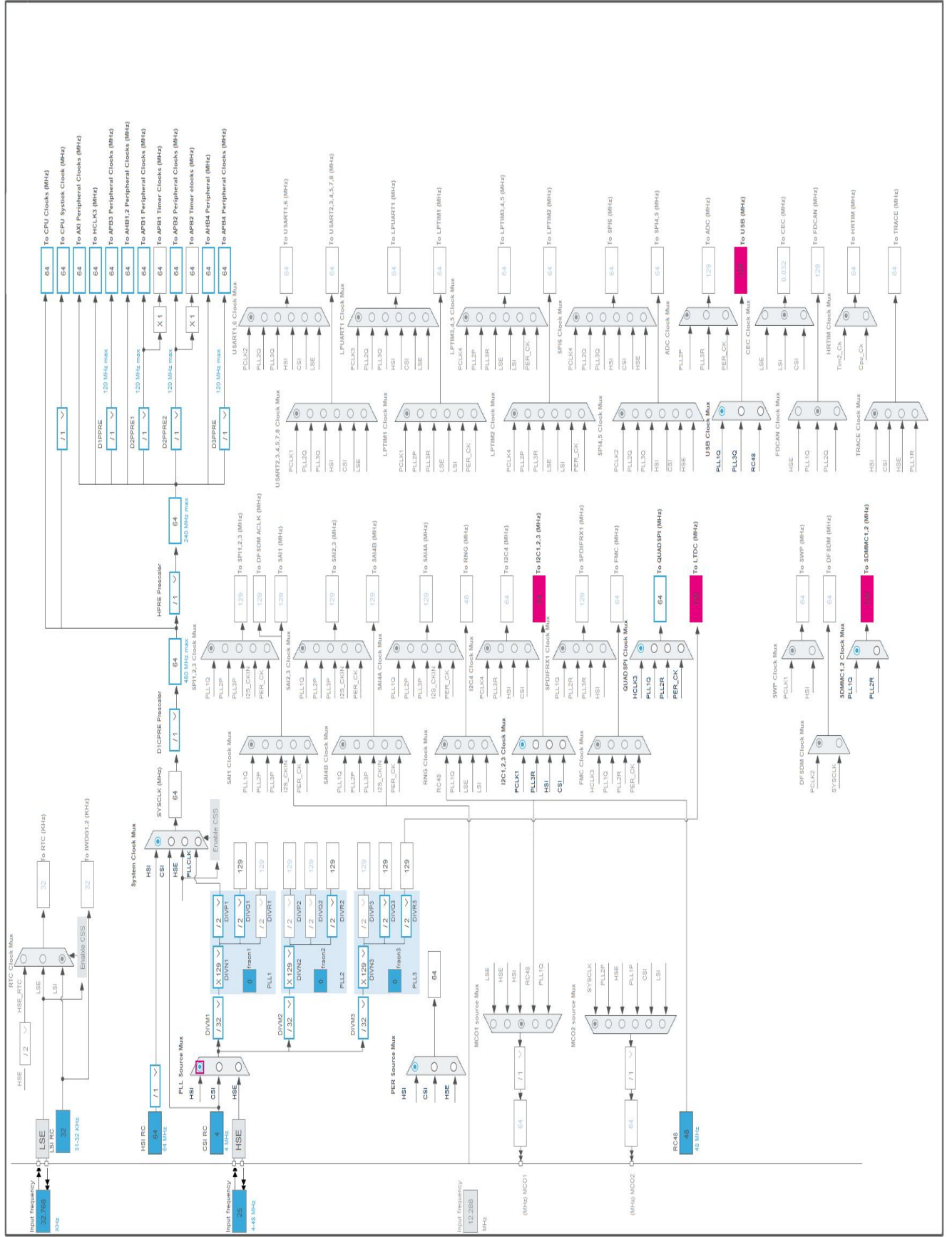


### 3. Pins Configuration

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2	I/O	QUADSPI_BK1_IO2	
6	VBAT	Power		
8	PC14-OSC32_IN (OSC32_IN)	I/O	RCC_OSC32_IN	
9	PC15-OSC32_OUT (OSC32_OUT)	I/O	RCC_OSC32_OUT	
10	VSS	Power		
11	VDD	Power		
12	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	
13	PH1-OSC_OUT (PH1)	I/O	RCC_OSC_OUT	
14	NRST	Reset		
15	PC0	I/O	LTDC_R5	
16	PC1	I/O	SDMMC2_CK	
19	VSSA	Power		
21	VDDA	Power		
22	PA0	I/O	SDMMC2_CMD	
23	PA1	I/O	LTDC_R2	
25	PA3	I/O	LTDC_B5	
26	VSS	Power		
27	VDD	Power		
28	PA4	I/O	LTDC_VSYNC	
29	PA5	I/O	LTDC_R4	
30	PA6	I/O	LTDC_G2	
34	PB0	I/O	LTDC_R3	
35	PB1	I/O	LTDC_R6	
36	PB2	I/O	QUADSPI_CLK	
41	PE11	I/O	LTDC_G3	
42	PE12	I/O	LTDC_B4	
43	PE13	I/O	LTDC_DE	
44	PE14	I/O	LTDC_CLK	
45	PE15	I/O	LTDC_R7	
46	PB10	I/O	LTDC_G4	
47	PB11	I/O	LTDC_G5	
48	VCAP	Power		
49	VSS	Power		
50	VDD	Power		

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
53	PB14	I/O	SDMMC2_D0	
54	PB15	I/O	SDMMC2_D1	
57	PD10	I/O	LTDC_B3	
58	PD11	I/O	QUADSPI_BK1_IO0	
59	PD12	I/O	QUADSPI_BK1_IO1	
60	PD13	I/O	QUADSPI_BK1_IO3	
63	PC6	I/O	LTDC_HSYNC	
64	PC7	I/O	LTDC_G6	
66	PC9	I/O	I2C3_SDA	
67	PA8	I/O	I2C3_SCL	
70	PA11	I/O	USB_OTG_FS_DM	
71	PA12	I/O	USB_OTG_FS_DP	
73	VCAP	Power		
74	VSS	Power		
75	VDD	Power		
84	PD3	I/O	LTDC_G7	
87	PD6	I/O	LTDC_B2	
89	PB3 (JTDO/TRACESWO)	I/O	SDMMC2_D2	
90	PB4 (NJTRST)	I/O	SDMMC2_D3	
92	PB6	I/O	QUADSPI_BK1_NCS	
94	BOOT0	Boot		
95	PB8	I/O	LTDC_B6	
96	PB9	I/O	LTDC_B7	
99	VSS	Power		
100	VDD	Power		

## 4. Clock Tree Configuration



## 1. Power Consumption Calculator report

### 1.1. Microcontroller Selection

Series	STM32H7
Line	STM32H750 Value line
MCU	STM32H750VBTx
Datasheet	DS12556_Rev6

### 1.2. Parameter Selection

Temperature	25
Vdd	3.0

### 1.3. Battery Selection

Battery	Alkaline(9V)
Capacity	625.0 mAh
Self Discharge	0.3 %/month
Nominal Voltage	9.0 V
Max Cont Current	200.0 mA
Max Pulse Current	0.0 mA
Cells in series	1
Cells in parallel	1

#### 1.4. Sequence

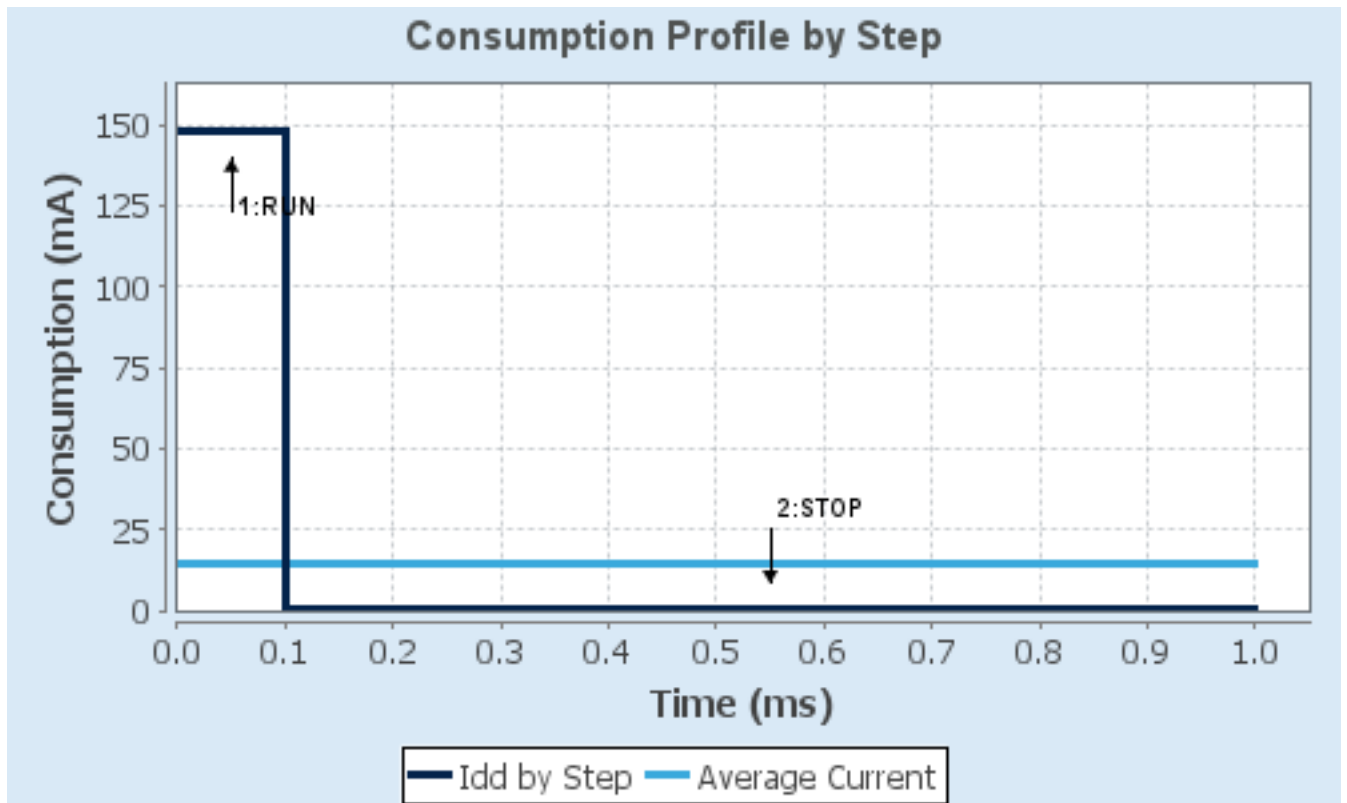
<b>Step</b>	Step1	Step2
<b>Mode</b>	RUN	STOP
<b>Vdd</b>	3.0	3.0
<b>Voltage Source</b>	Battery	Battery
<b>Range</b>	VOS0: Scale0-High	SVOS5: System-Scale5
<b>D1 Mode</b>	DRUN/CRUN	DSTANDBY
<b>D2 Mode</b>	DRUN	DSTANDBY
<b>D3 Mode</b>	DRUN	DSTOP
<b>Fetch Type</b>	ITCM	NA
<b>CPU Frequency</b>	480 MHz	0 Hz
<b>Clock Configuration</b>	HSE BYP PLL	Flash-OFF
<b>Clock Source Frequency</b>	24 MHz	0 Hz
<b>Peripherals</b>		
<b>Additional Cons.</b>	0 mA	0 mA
<b>Average Current</b>	148 mA	150 $\mu$ A
<b>Duration</b>	0.1 ms	0.9 ms
<b>DMIPS</b>	1027.0	0.0
<b>Ta Max</b>	105.02	124.98
<b>Category</b>	In DS Table	In DS Table

#### 1.5. Results

Sequence Time	1 ms	Average Current	14.94 mA
Battery Life	1 day, 17 hours	Average DMIPS	1027.2001 DMIPS

#### 1.6. Chart





## 2. Software Project

### 2.1. Project Settings

Name	Value
Project Name	iW-CORE-BOARD
Project Folder	C:\Users\Lorrane Azevedo\Documents\industrias-william\iW-CORE-
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_H7 V1.12.1
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

### 2.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

### 2.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_I2C3_Init	I2C3
4	MX_LTDC_Init	LTDC
5	MX_QUADSPI_Init	QUADSPI
6	MX_SDMMC2_MMC_Init	SDMMC2
7	MX_USB_OTG_FS_PCD_Init	USB_OTG_FS

## 3. Peripherals and Middlewares Configuration

### 3.1. CORTEX\_M7

#### 3.1.1. Parameter Settings:

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##### Speculation default mode Settings:

Speculation default mode Enabled

##### Cortex Interface Settings:

CPU ICache Disabled

CPU DCache Disabled

##### Cortex Memory Protection Unit Control Settings:

MPU Control Mode Background Region Privileged accesses only + MPU Disabled during hard fault, NMI and FAULTMASK handlers

##### Cortex Memory Protection Unit Region 0 Settings:

MPU Region Enabled

MPU Region Base Address **0x0 \***

MPU Region Size 4GB

MPU SubRegion Disable **0x87 \***

MPU TEX field level level 0

MPU Access Permission ALL ACCESS NOT PERMITTED

MPU Instruction Access DISABLE

MPU Shareability Permission ENABLE

MPU Cacheable Permission DISABLE

MPU Bufferable Permission DISABLE

##### Cortex Memory Protection Unit Region 1 Settings:

MPU Region Disabled

##### Cortex Memory Protection Unit Region 2 Settings:

MPU Region Disabled

##### Cortex Memory Protection Unit Region 3 Settings:

MPU Region Disabled

##### Cortex Memory Protection Unit Region 4 Settings:

MPU Region Disabled

##### Cortex Memory Protection Unit Region 5 Settings:

MPU Region Disabled

##### Cortex Memory Protection Unit Region 6 Settings:

MPU Region Disabled

##### Cortex Memory Protection Unit Region 7 Settings:

MPU Region Disabled

##### Cortex Memory Protection Unit Region 8 Settings:

MPU Region Disabled

**Cortex Memory Protection Unit Region 9 Settings:**

MPU Region Disabled

**Cortex Memory Protection Unit Region 10 Settings:**

MPU Region Disabled

**Cortex Memory Protection Unit Region 11 Settings:**

MPU Region Disabled

**Cortex Memory Protection Unit Region 12 Settings:**

MPU Region Disabled

**Cortex Memory Protection Unit Region 13 Settings:**

MPU Region Disabled

**Cortex Memory Protection Unit Region 14 Settings:**

MPU Region Disabled

**Cortex Memory Protection Unit Region 15 Settings:**

MPU Region Disabled

### 3.2. I2C3

#### I2C: I2C

##### 3.2.1. Parameter Settings:

**Timing configuration:**

Custom Timing	Disabled
I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	0x10707DBC

**Slave Features:**

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

### 3.3. LTDC

## Display Type: RGB666 (18 bits)

### 3.3.1. Parameter Settings:

#### **Synchronization for Width:**

Horizontal Synchronization Width	8
Horizontal Back Porch	7
Active Width	640
Horizontal Front Porch	6
HSync Width	7
Accumulated Horizontal Back Porch Width	14
Accumulated Active Width	654
Total Width	660

#### **Synchronization for Height:**

Vertical Synchronization Height	4
Vertical Back Porch	2
Active Height	480
Vertical Front Porch	2
VSyn Height	3
Accumulated Vertical Back Porch Height	5
Accumulated Active Height	485
Total Height	487

#### **Signal Polarity:**

Horizontal Synchronization Polarity	Active Low
Vertical Synchronization Polarity	Active Low
Data Enable Polarity	Active Low
Pixel Clock Polarity	Normal Input

#### **Layer Default Color:**

Red	0
Green	0
Blue	0

### 3.3.2. Layer Settings:

#### **Layer Default Color:**

Layer 0 - Alpha	0
Layer 0 - Blue	0
Layer 0 - Green	0
Layer 0 - Red	0
Layer 1 - Alpha	0
Layer 1 - Blue	0
Layer 1 - Green	0

Layer 1 - Red 0

**Number of Layers:**

Number of Layers 2 layers

**Windows Position:**

Layer 0 - Window Horizontal Start 0

Layer 0 - Window Horizontal Stop 0

Layer 0 - Window Vertical Start 0

Layer 0 - Window Vertical Stop 0

Layer 1 - Window Horizontal Start 0

Layer 1 - Window Horizontal Stop 0

Layer 1 - Window Vertical Start 0

Layer 1 - Window Vertical Stop 0

**Pixel Parameters:**

Layer 0 - Pixel Format ARGB8888

Layer 1 - Pixel Format ARGB8888

**Blending:**

Layer 0 - Alpha constant for blending 0

Layer 0 - Blending Factor1 Alpha constant

Layer 0 - Blending Factor2 Alpha constant

Layer 1 - Alpha constant for blending 0

Layer 1 - Blending Factor1 Alpha constant

Layer 1 - Blending Factor2 Alpha constant

**Frame Buffer:**

Layer 0 - Color Frame Buffer Start Address 0

Layer 0 - Color Frame Buffer Line Length (Image Width) 0

Layer 0 - Color Frame Buffer Number of Lines (Image Height) 0

Layer 1 - Color Frame Buffer Start Address 0

Layer 1 - Color Frame Buffer Line Length (Image Width) 0

Layer 1 - Color Frame Buffer Number of Lines (Image Height) 0

### 3.4. MEMORYMAP

mode: Activated

### 3.5. QUADSPI

QuadSPI Mode: Bank1 with Quad SPI Lines

### 3.5.1. Parameter Settings:

#### **General Parameters:**

Clock Prescaler	255
Fifo Threshold	1
Sample Shifting	No Sample Shifting
Flash Size	1
Device Type	Not defined
Chip Select High Time	1 Cycle
Clock Mode	Low
Flash ID	Flash ID 1
Dual Flash	Disabled

### **3.6. RCC**

**High Speed Clock (HSE): Crystal/Ceramic Resonator**

**Low Speed Clock (LSE) : Crystal/Ceramic Resonator**

#### 3.6.1. Parameter Settings:

#### **Power Parameters:**

SupplySource	PWR_LDO_SUPPLY
Power Regulator Voltage Scale	Power Regulator Voltage Scale 3

#### **RCC Parameters:**

TIM Prescaler Selection	Disabled
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000
CSI Calibration Value	32
HSI Calibration Value	64

#### **System Parameters:**

VDD voltage (V)	3.3
Flash Latency(WS)	1 WS (2 CPU cycle)
Product revision	rev.V

#### **PLL range Parameters:**

PLL1 clock Input range	Between 2 and 4 MHz
PLL3 input frequency range	Between 2 and 4 MHz
PLL1 clock Output range	Wide VCO range
PLL3 clock Output range	Wide VCO range

### 3.7. SDMMC2

**Mode: MMC 4 bits Wide bus**

#### 3.7.1. Parameter Settings:

**SDMMC parameters:**

Clock transition on which the bit capture is made	Rising transition
SDMMC Clock output enable when the bus is idle	Disable the power save for the clock
SDMMC hardware flow control	The hardware control flow is disabled
SDMMC clock divide factor	0
Is external transceiver present ?	no

### 3.8. SYS

**Timebase Source: SysTick**

### 3.9. USB\_OTG\_FS

**Mode: Device\_Only**

#### 3.9.1. Parameter Settings:

Speed	Full Speed 12MBit/s
Enable internal IP DMA	Disabled
Low power	Disabled
Battery charging	Disabled
Link Power Management	Disabled
Use dedicated end point 1 interrupt	Disabled
VBUS sensing	Disabled
Signal start of frame	Disabled

**\* User modified value**



## 4. System Configuration

### 4.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
I2C3	PC9	I2C3_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	
	PA8	I2C3_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	
LTDC	PC0	LTDC_R5	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA1	LTDC_R2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA3	LTDC_B5	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA4	LTDC_VSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA5	LTDC_R4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA6	LTDC_G2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB0	LTDC_R3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB1	LTDC_R6	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE11	LTDC_G3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE12	LTDC_B4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE13	LTDC_DE	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE14	LTDC_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE15	LTDC_R7	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB10	LTDC_G4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB11	LTDC_G5	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD10	LTDC_B3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC6	LTDC_HSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC7	LTDC_G6	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD3	LTDC_G7	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD6	LTDC_B2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB8	LTDC_B6	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB9	LTDC_B7	Alternate Function Push Pull	No pull-up and no pull-down	Low	
QUADSPI	PE2	QUADSPI_BK1_I02	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB2	QUADSPI_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD11	QUADSPI_BK1_I00	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD12	QUADSPI_BK1_I01	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD13	QUADSPI_BK1_I03	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB6	QUADSPI_BK1_NCS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
RCC	PC14-	RCC_OSC32_IN	n/a	n/a	n/a	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	OSC32_IN (OSC32_IN)					
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0-OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT (PH1)	RCC_OSC_OUT	n/a	n/a	n/a	
SDMMC2	PC1	SDMMC2_CK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PA0	SDMMC2_CMD	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PB14	SDMMC2_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PB15	SDMMC2_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PB3 (JTDO/TRACESWO)	SDMMC2_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PB4 (NJTRST)	SDMMC2_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
USB_OTG_FS	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	No pull-up and no pull-down	Low	

#### 4.2. DMA configuration

nothing configured in DMA service

#### 4.3. BDMA configuration

nothing configured in DMA service

#### 4.4. MDMA configuration

nothing configured in DMA service

## 4.5. NVIC configuration

### 4.5.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
PVD and AVD interrupts through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
I2C3 event interrupt	unused		
I2C3 error interrupt	unused		
FPU global interrupt	unused		
LTDC global interrupt	unused		
LTDC global error interrupt	unused		
QUADSPI global interrupt	unused		
USB On The Go FS End Point 1 Out global interrupt	unused		
USB On The Go FS End Point 1 In global interrupt	unused		
USB On The Go FS global interrupt	unused		
SDMMC2 global interrupt	unused		
HSEM1 global interrupt	unused		

### 4.5.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
System tick timer	false	true	true




\* User modified value

## 5. System Views

### 5.1. Category view

#### 5.1.1. Current

Category view   Power Domain view

   Choose filters ...

... by Power Domain




☐ D1   ☐ D2   ☐ D3   ☒ None

#### Middleware

System Core	Analog	Timers	Connectivity	Multimedia	Security	Computing	Trace and Debug	Power and Thermal	Other
BDMA			I2C3 ✓	LTDC ✓					
CORTEX_M7 ✓			QUADSPI ✓						
DMA			SDMMC2 ✓						
GPIO ✓			USB_FS ✓						
MDMA									
IVIC ✓									
RCC ✓									
SYS ✓									

### 5.1.2. Without filters

Category view   Power Domain view

   Choose filters ...

... by Power Domain  
☐ D1   ☐ D2   ☐ D3   ☒ None

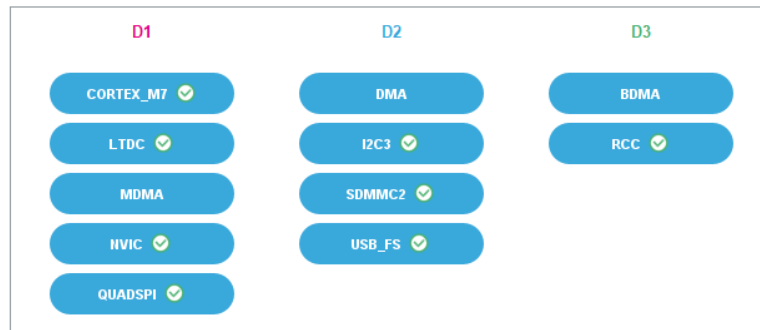
#### Middleware

System Core	Analog	Timers	Connectivity	Multimedia	Security	Computing	Trace and Debug	Power and Thermal	Other
BDMA			I2C3 ✓	LTDC ✓					
CORTEX_M7 ✓			QUADSPI ✓						
DMA			SDMMC2 ✓						
GPIO ✓			USB_FS ✓						
MDMA									
IVIC ✓									
RCC ✓									
SYS ✓									

## 5.2. Power Domain view

Category view

Power Domain view



## 6. Docs & Resources

Type	Link
BSDL files	<a href="https://www.st.com/resource/en/bsdl_model/stm32h7_bsd1.zip">https://www.st.com/resource/en/bsdl_model/stm32h7_bsd1.zip</a>
IBIS models	<a href="https://www.st.com/resource/en/ibis_model/stm32h7_ibis.zip">https://www.st.com/resource/en/ibis_model/stm32h7_ibis.zip</a>
System View Description	<a href="https://www.st.com/resource/en/svd/stm32h7-svd.zip">https://www.st.com/resource/en/svd/stm32h7-svd.zip</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/microcontrollers_stm32h7_series_product_overview.pdf">https://www.st.com/resource/en/product_presentation/microcontrollers_stm32h7_series_product_overview.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf">https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32_eval-tools_portfolio.pdf">https://www.st.com/resource/en/product_presentation/stm32_eval-tools_portfolio.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32_stm8_functional-safety-packages.pdf">https://www.st.com/resource/en/product_presentation/stm32_stm8_functional-safety-packages.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32-stm8_software_development_tools.pdf">https://www.st.com/resource/en/product_presentation/stm32-stm8_software_development_tools.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/microcontrollers-stm32-family-overview.pdf">https://www.st.com/resource/en/product_presentation/microcontrollers-stm32-family-overview.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/microcontrollers-stm32h7rs-lines-overview.pdf">https://www.st.com/resource/en/product_presentation/microcontrollers-stm32h7rs-lines-overview.pdf</a>
Brochures	<a href="https://www.st.com/resource/en/brochure/brstm32h7.pdf">https://www.st.com/resource/en/brochure/brstm32h7.pdf</a>
Flyers	<a href="https://www.st.com/resource/en/flyer/flstm32nucleo.pdf">https://www.st.com/resource/en/flyer/flstm32nucleo.pdf</a>
Flyers	<a href="https://www.st.com/resource/en/flyer/flstm32trust.pdf">https://www.st.com/resource/en/flyer/flstm32trust.pdf</a>
Flyers	<a href="https://www.st.com/resource/en/flyer/flstm32f7h7.pdf">https://www.st.com/resource/en/flyer/flstm32f7h7.pdf</a>
Flyers	<a href="https://www.st.com/resource/en/flyer/flstm32h7vl.pdf">https://www.st.com/resource/en/flyer/flstm32h7vl.pdf</a>
Flyers	<a href="https://www.st.com/resource/en/flyer/flstm32h7rs.pdf">https://www.st.com/resource/en/flyer/flstm32h7rs.pdf</a>
Security Bulletin	<a href="https://www.st.com/resource/en/security_bulletin/sb0023-eucleak-protection-statement-for-stmicroelectronics-certified-products-stmicroelectronics.pdf">https://www.st.com/resource/en/security_bulletin/sb0023-eucleak-protection-statement-for-stmicroelectronics-certified-products-stmicroelectronics.pdf</a>
Application Notes	<a href="https://www.st.com/resource/en/application_note/an1709-emc-design-guide-for-stm8-stm32-and-legacy-mcus-stmicroelectronics.pdf">https://www.st.com/resource/en/application_note/an1709-emc-design-guide-for-stm8-stm32-and-legacy-mcus-stmicroelectronics.pdf</a>



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