Lab 7

7-Segment Display

CS1050 Computer Organization and Digital Design

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Group 41

Introduction:

- **Task**

  We have to implement a 7-segment display to present outcomes from the prebuilt 4-bit Arithmetic Unit (AU). The AU will produce a sum, a carry, and a zero flag based on the two input 4-bit numbers given to the registers in the AU. The 4-bit sum from the RCA will appear as a hexadecimal number on the 7-segment display. To achieve this, we first created a lookup table using a ROM. This table maps the output from the AU to the 7-segment display. Finally, we verified the functionality of the 7-segment display by simulating it on the BYASIS 3 board.

- **Table of segments to switch on**

Output from RC					**Segments to Switch On**						
S_3	**S_2**	**S_1**	**S_0**	**Hex. Value**	**A**	**B**	**C**	**D**	**E**	**F**	**G**
0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	1	1	0	0	1	1	1	1
0	0	1	0	2	0	0	1	0	0	1	0
0	0	1	1	3	0	0	0	0	1	1	0
0	1	0	0	4	1	0	0	1	1	0	0
0	1	0	1	5	0	1	0	0	1	0	0
0	1	1	0	6	0	1	0	0	0	0	0
0	1	1	1	7	0	0	0	1	1	1	1
1	0	0	0	8	0	0	0	0	0	0	0
1	0	0	1	9	0	0	0	0	1	0	0

1	0	1	0	A	0	0	0	1	0	0	0
1	0	1	1	B	1	1	0	0	0	0	0
1	1	0	0	C	0	1	1	0	0	0	1
1	1	0	1	D	1	0	0	0	0	1	0
1	1	1	0	E	0	1	1	0	0	0	0
1	1	1	1	F	0	1	1	1	0	0	0

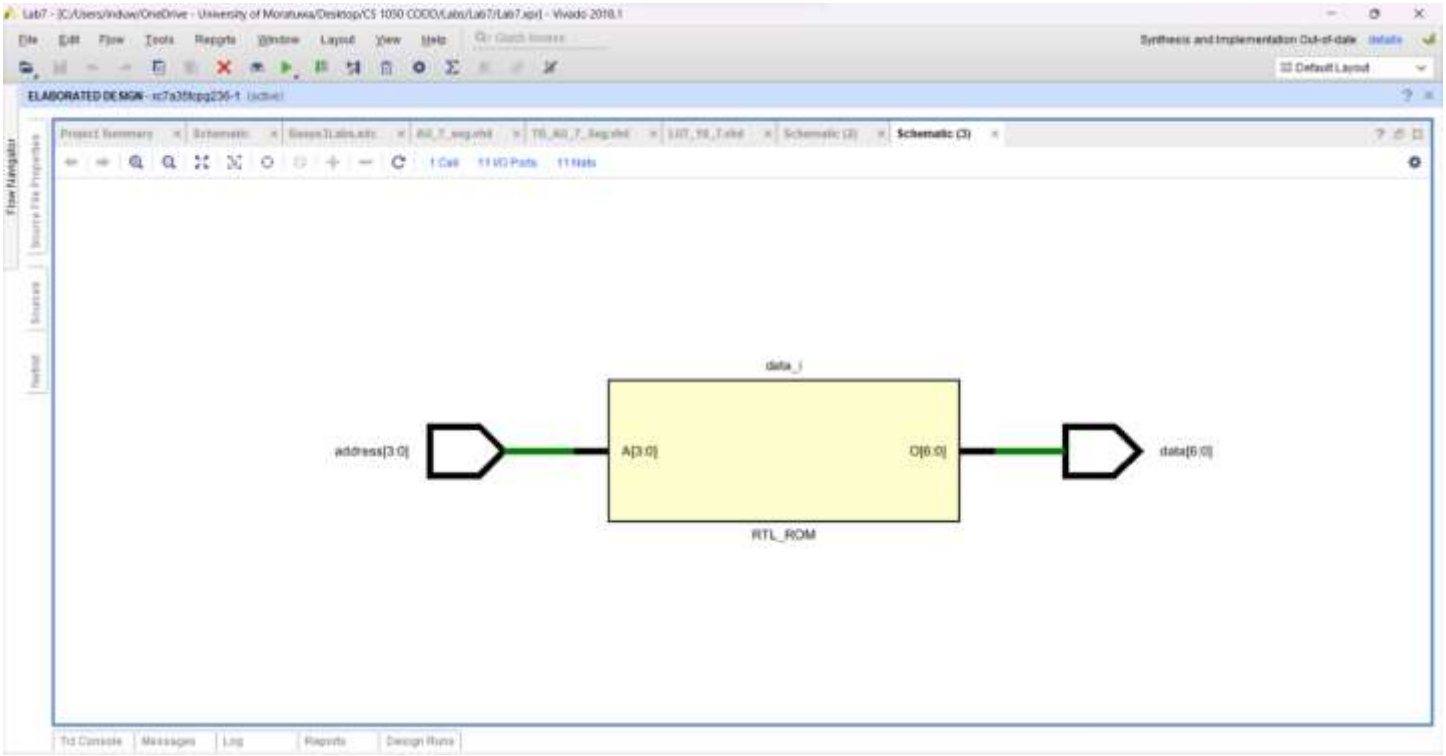
1. **Lookup Table**

- **Design source file**

```
----------------------------------------------------------------------------
--------
-- Company:
-- Engineer:
--
-- Create Date: 03/20/2024 11:06:49 AM
-- Design Name:
-- Module Name: LUT_16_7 - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------
--------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use ieee.numeric_std.all;
```

```
-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity LUT_16_7 is
    Port ( address : in STD_LOGIC_VECTOR (3 downto 0);
           data : out STD_LOGIC_VECTOR (6 downto 0));
end LUT_16_7;

architecture Behavioral of LUT_16_7 is

type rom_type is array (0 to 15) of std_logic_vector (6 downto 0);
    signal sevenSegment_ROM : rom_type := (
                              "1000000", -- 0
                              "1111001", -- 1
                              "0100100", --2
                              "0110000", --3
                              "0011001", --4
                              "0010010", --5
                              "0000010", --6
                              "1111000", --7
                              "0000000", --8
                              "0010000", --9
                              "0001000", --a
                              "0000011", --b
                              "1000110", --c
                              "0100001", --d
                              "0000110", --e
                              "0001110" --f
          );

begin
data <= sevenSegment_ROM(to_integer(unsigned(address)));

end Behavioral;
```

- **Elaborated design schematic**



- **Simulation source file**

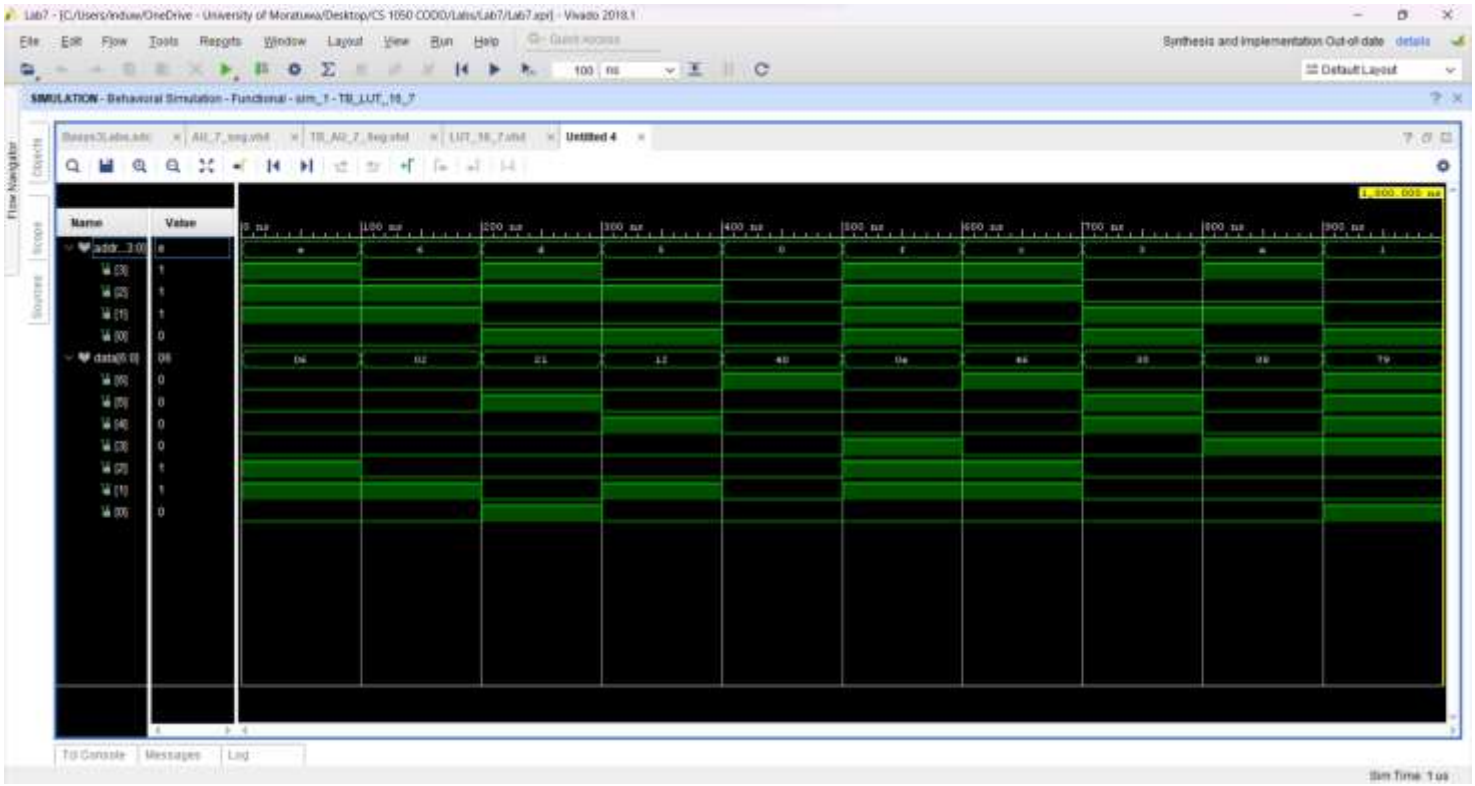
```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 03/20/2024 11:20:47 AM
-- Design Name:
-- Module Name: TB_LUT_16_7 - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
```

```
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------
--------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity TB_LUT_16_7 is
--  Port ( );
end TB_LUT_16_7;

architecture Behavioral of TB_LUT_16_7 is

component LUT_16_7 is
    Port ( address : in STD_LOGIC_VECTOR (3 downto 0);
           data : out STD_LOGIC_VECTOR (6 downto 0));
end component;

signal  address : STD_LOGIC_VECTOR (3 downto 0);
signal  data : STD_LOGIC_VECTOR (6 downto 0);
```

```
begin
UUT : LUT_16_7 port map(
        address => address,
        data => data);

process begin
    address <= "1110";
    wait for 100ns;

    address <= "0110";
    wait for 100ns;

    address <= "1101";
    wait for 100ns;

    address <= "0101";
    wait for 100ns;

    address <= "0000";
    wait for 100ns;

    address <= "1111";
    wait for 100ns;

    address <= "1100";
    wait for 100ns;

    address <= "0011";
    wait for 100ns;

    address <= "1010";
    wait for 100ns;
```

```
    address <= "0001";
    wait for 100ns;


end process;

end Behavioral;
```

- **Time diagram**



2. 7-Segment Display

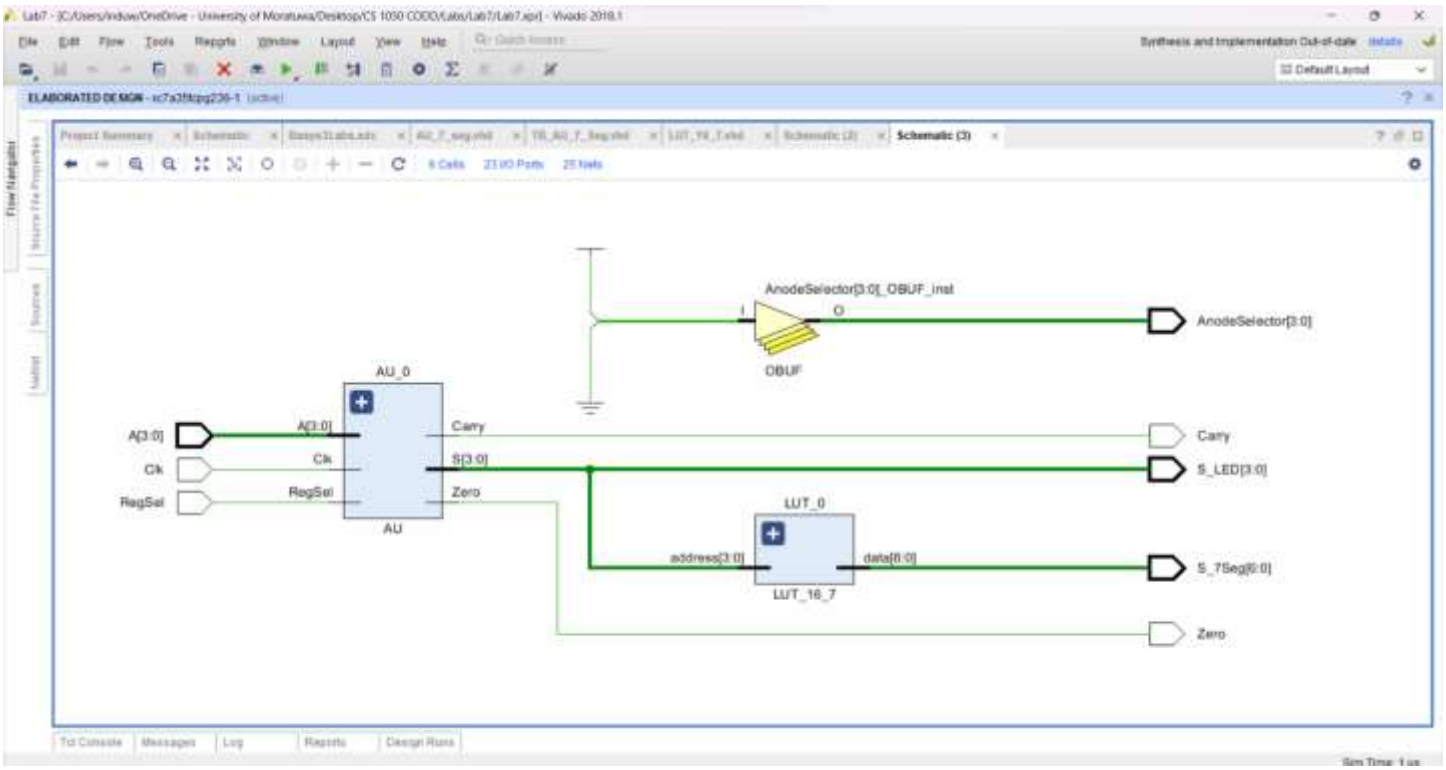
- **Design source file**

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 03/20/2024 11:46:02 AM
-- Design Name:
-- Module Name: AU_7_seg - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;
```

```
entity AU_7_seg is
    Port ( A : in STD_LOGIC_VECTOR (3 downto 0);
           Clk : in STD_LOGIC;
           RegSel : in STD_LOGIC;
           S_LED : out STD_LOGIC_VECTOR (3 downto 0);
           S_7Seg : out STD_LOGIC_VECTOR (6 downto 0);
           Carry : out STD_LOGIC;
           Zero : out STD_LOGIC;
           AnodeSelector : out STD_LOGIC_VECTOR (3 downto 0));
end AU_7_seg;

architecture Behavioral of AU_7_seg is

component AU is
    Port ( A : in STD_LOGIC_VECTOR (3 downto 0);
           RegSel : in STD_LOGIC;
           Clk : in STD_LOGIC;
           S : out STD_LOGIC_VECTOR (3 downto 0);
           Zero : out STD_LOGIC;
           Carry : out STD_LOGIC);
end component;

component LUT_16_7 is
    Port ( address : in STD_LOGIC_VECTOR (3 downto 0);
           data : out STD_LOGIC_VECTOR (6 downto 0));
end component;

signal AUOutput : STD_LOGIC_VECTOR (3 downto 0);

begin

AU_0 : AU
    port map (
        A => A,
        RegSel => RegSel,
```

```
        Clk => Clk,
        Carry => Carry,
        Zero => Zero,
        S => AUOutput
    );

LUT_0 : LUT_16_7
    port map (
        address => AUOutput,
        data => S_7Seg
        );

S_LED <= AUOutput;
AnodeSelector <= "1110";

end Behavioral;
```

- **Elaborated design schematic**



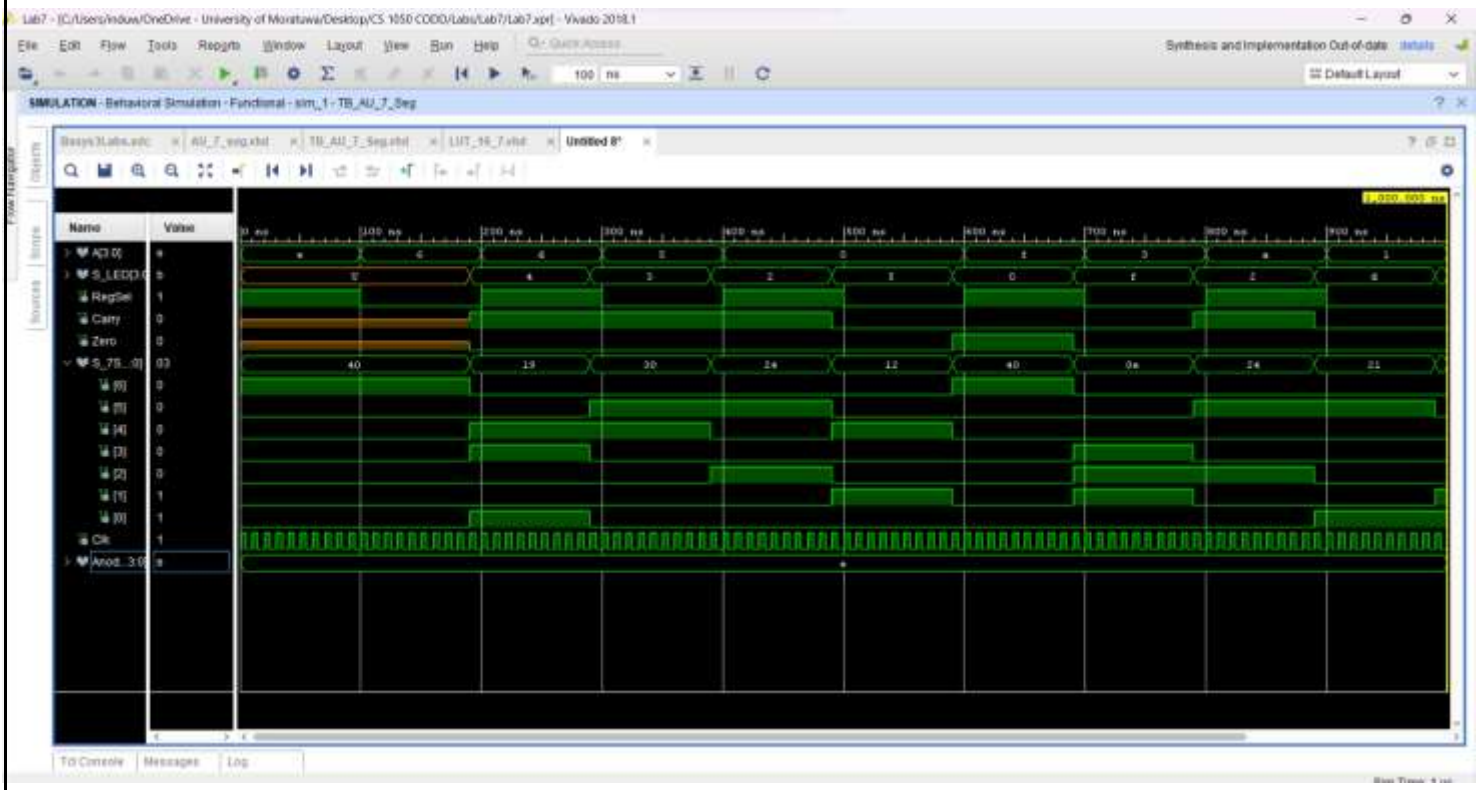
- **Simulation source file**

```
----------------------------------------------------------------------------
--------
-- Company:
-- Engineer:
--
-- Create Date: 03/20/2024 12:07:39 PM
-- Design Name:
-- Module Name: TB_AU_7_Seg - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------
--------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity TB_AU_7_Seg is
--  Port ( );
end TB_AU_7_Seg;

architecture Behavioral of TB_AU_7_Seg is
```

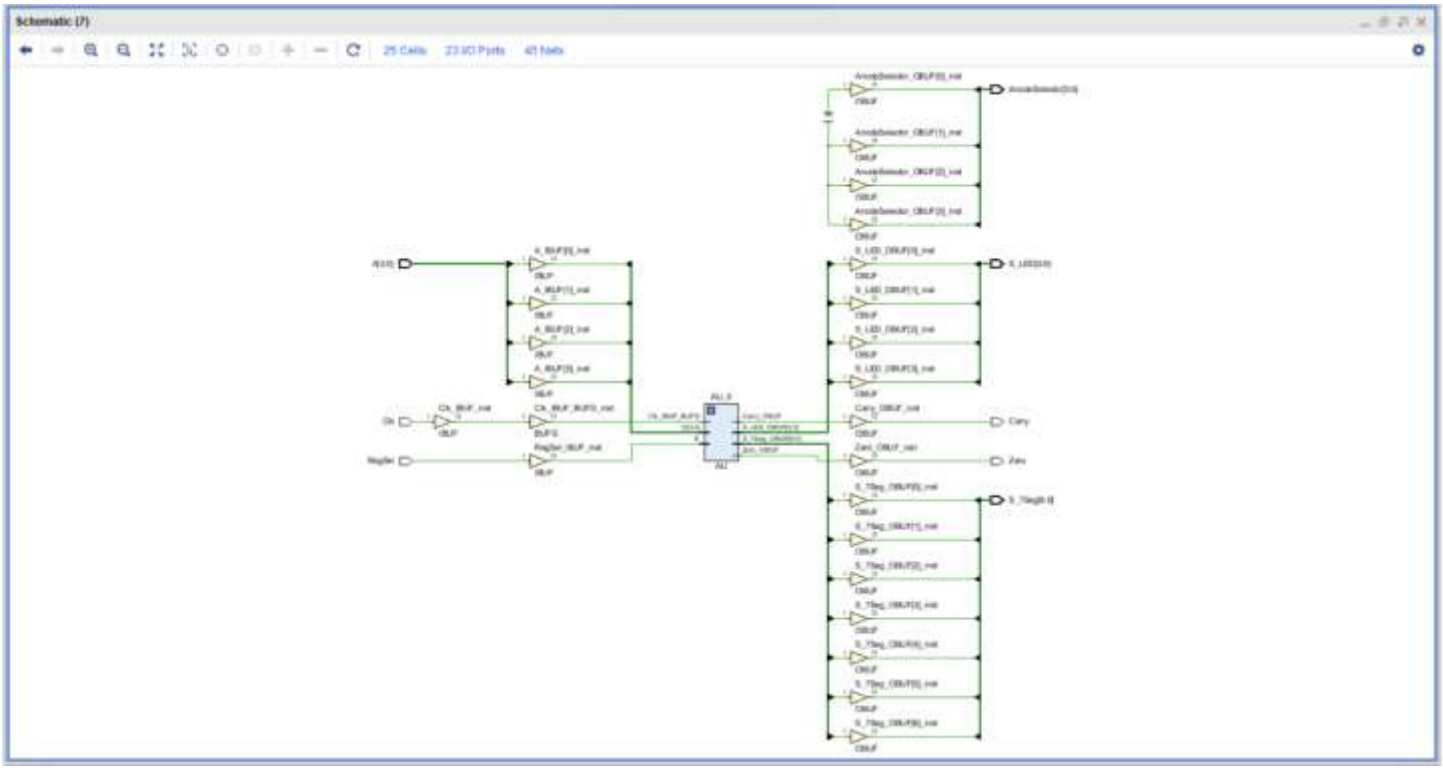
```
component AU_7_seg is
    Port ( A : in STD_LOGIC_VECTOR (3 downto 0);
           Clk : in STD_LOGIC;
           RegSel : in STD_LOGIC;
           S_LED : out STD_LOGIC_VECTOR (3 downto 0);
           S_7Seg : out STD_LOGIC_VECTOR (6 downto 0);
           Carry : out STD_LOGIC;
           Zero : out STD_LOGIC;
           AnodeSelector : out STD_LOGIC_VECTOR (3 downto 0));
end component;

signal A, S_LED, AnodeSelector : STD_LOGIC_VECTOR (3 downto 0);
signal RegSel, Carry, Zero : STD_LOGIC;
signal S_7Seg : STD_LOGIC_VECTOR (6 downto 0);
signal Clk : STD_LOGIC := '0';

begin
UUT : AU_7_seg
    port map (
        A => A,
        Clk => Clk,
        RegSel => RegSel,
        S_LED => S_LED,
        S_7Seg => S_7Seg,
        Carry => Carry,
        Zero => Zero,
        AnodeSelector => AnodeSelector
        );

process begin
    Clk <= not Clk;
    wait for 5ns;
end process;

process begin

    RegSel <= '1';
    A<= "1110";
    wait for 100ns;
```

```
    RegSel <= '0';
    A<= "0110";
    wait for 100ns;

    RegSel <= '1';
    A<= "1101";
    wait for 100ns;

    RegSel <= '0';
    A<= "0101";
    wait for 100ns;

    RegSel <= '1';
    A<= "0000";
    wait for 100ns;

    RegSel <= '0';
    A<= "0000";
    wait for 100ns;

    RegSel <= '1';
    A<= "1111";
    wait for 100ns;

    RegSel <= '0';
    A<= "0011";
    wait for 100ns;

    RegSel <= '1';
    A<= "1010";
    wait for 100ns;

    RegSel <= '0';
    A<= "0001";
    wait for 100ns;

end process;

end Behavioral;
```

- **Time diagram**



- **Implemented design schematic**



- **Constraints file**

```
## Clock signal
set_property PACKAGE_PIN W5 [get_ports Clk]
     set_property IOSTANDARD LVCMOS33 [get_ports Clk]
     create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports Clk]

## Switches
set_property PACKAGE_PIN V17 [get_ports {A[0]}]
     set_property IOSTANDARD LVCMOS33 [get_ports {A[0]}]
set_property PACKAGE_PIN V16 [get_ports {A[1]}]
     set_property IOSTANDARD LVCMOS33 [get_ports {A[1]}]
set_property PACKAGE_PIN W16 [get_ports {A[2]}]
     set_property IOSTANDARD LVCMOS33 [get_ports {A[2]}]
set_property PACKAGE_PIN W17 [get_ports {A[3]}]
     set_property IOSTANDARD LVCMOS33 [get_ports {A[3]}]
set_property PACKAGE_PIN R2 [get_ports {RegSel}]
     set_property IOSTANDARD LVCMOS33 [get_ports {RegSel}]


## LEDs
set_property PACKAGE_PIN U16 [get_ports {S_LED[0]}]
     set_property IOSTANDARD LVCMOS33 [get_ports {S_LED[0]}]
set_property PACKAGE_PIN E19 [get_ports {S_LED[1]}]
     set_property IOSTANDARD LVCMOS33 [get_ports {S_LED[1]}]
set_property PACKAGE_PIN U19 [get_ports {S_LED[2]}]
     set_property IOSTANDARD LVCMOS33 [get_ports {S_LED[2]}]
set_property PACKAGE_PIN V19 [get_ports {S_LED[3]}]
     set_property IOSTANDARD LVCMOS33 [get_ports {S_LED[3]}]

set_property PACKAGE_PIN P1 [get_ports {Carry}]
     set_property IOSTANDARD LVCMOS33 [get_ports {Carry}]
set_property PACKAGE_PIN L1 [get_ports {Zero}]
```

```
    set_property IOSTANDARD LVCMOS33 [get_ports {Zero}]


##7 segment display
set_property PACKAGE_PIN W7 [get_ports {S_7Seg[0]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {S_7Seg[0]}]
set_property PACKAGE_PIN W6 [get_ports {S_7Seg[1]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {S_7Seg[1]}]
set_property PACKAGE_PIN U8 [get_ports {S_7Seg[2]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {S_7Seg[2]}]
set_property PACKAGE_PIN V8 [get_ports {S_7Seg[3]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {S_7Seg[3]}]
set_property PACKAGE_PIN U5 [get_ports {S_7Seg[4]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {S_7Seg[4]}]
set_property PACKAGE_PIN V5 [get_ports {S_7Seg[5]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {S_7Seg[5]}]
set_property PACKAGE_PIN U7 [get_ports {S_7Seg[6]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {S_7Seg[6]}]

set_property PACKAGE_PIN U2 [get_ports {AnodeSelector[0]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {AnodeSelector[0]}]
set_property PACKAGE_PIN U4 [get_ports {AnodeSelector[1]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {AnodeSelector[1]}]
set_property PACKAGE_PIN V4 [get_ports {AnodeSelector[2]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {AnodeSelector[2]}]
set_property PACKAGE_PIN W4 [get_ports {AnodeSelector[3]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {AnodeSelector[3]}]
```

Conclusion

Instead of deriving logic equations for the inputs of each segment using K-maps, we can obtain the corresponding inputs using a lookup table.

We can use a 7-segment display to represent hexadecimal, decimal, octal, and binary numbers.

To illuminate a specific section of a display, the anode must be set to high, while the cathode should be set to low. However, the Basys 3 system uses transistors to supply enough current to the common anode point, which causes the anode enables to be inverted. This means that when a section is active, both the cathode and anode signals are driven low.

- As an example when we want to light up the rightmost segment, we have to give “1110” to the anode.