Lab 5

Counter with External Input

CS1050 Computer Organization and Digital Design

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Group 41

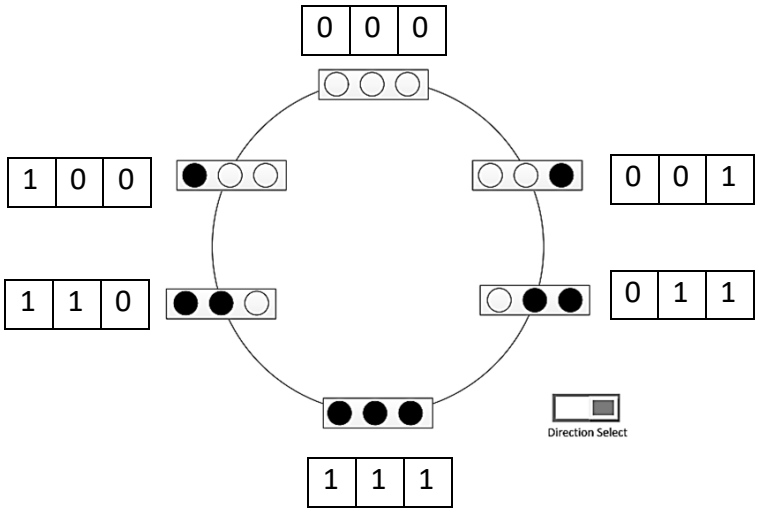
Introduction

Task:

We have to implement a 3-bit counter that can count in clockwise and anticlockwise directions based on an external input. A counter, which is a fundamental component of a circuit, is used for sequentially counting through a list of states.

We created a 3-bit counter that displays the sequence of LEDs. When the input button is turned off, we count in the clockwise direction. When it is turned on, we shall count in an anticlockwise manner.

The counting pattern as shown below:



According to the state diagram, we built the transition table using the excitation table of the D-flipflop. We used K-maps to simplify the expressions. Then we implemented a D-filipflop, a slow clock, and a counter. At last, we verified the functionality of the counter via simulation and on the BASYS 3 board.

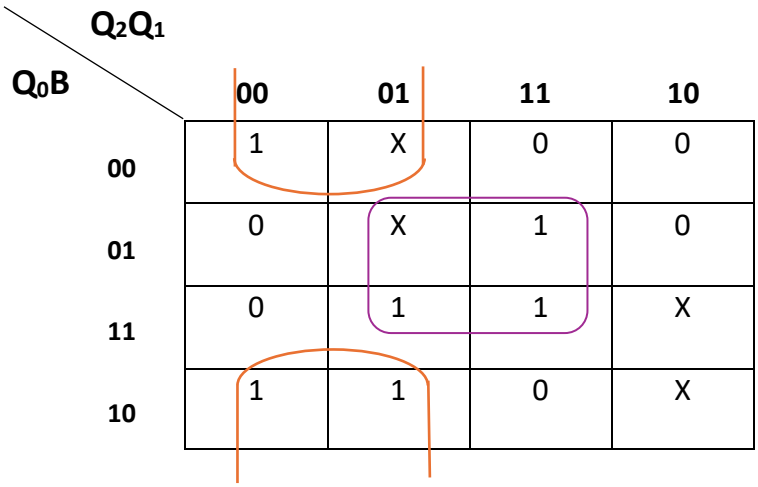
- **Excitation Table:**

Q_t	Q_{t+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

- **Transition Table:**

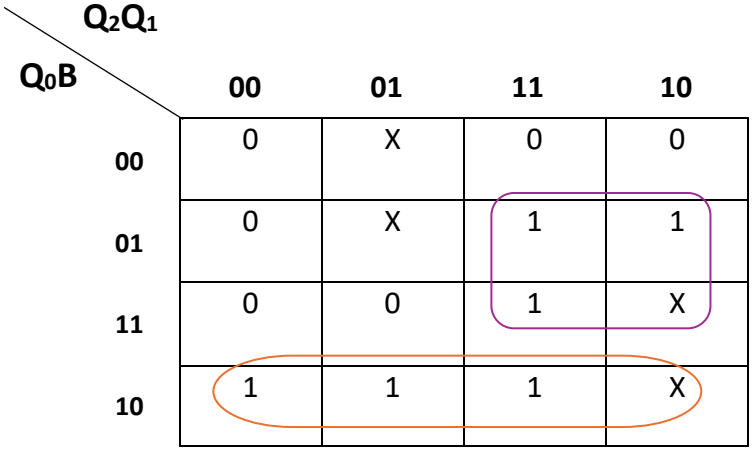
Q_t			B	Q_{t+1}			D		
$Q_{(2)}$	$Q_{(1)}$	$Q_{(0)}$		$Q_{(2)}$	$Q_{(1)}$	$Q_{(0)}$	$D_{(2)}$	$D_{(1)}$	$D_{(0)}$
0	0	0	0	0	0	1	0	0	1
0	0	0	1	1	0	0	1	0	0
0	0	1	0	0	1	1	0	1	1
0	0	1	1	0	0	0	0	0	0
0	1	1	0	1	1	1	1	1	1
0	1	1	1	0	0	1	0	0	1
1	1	1	0	1	1	0	1	1	0
1	1	1	1	0	1	1	0	1	1
1	1	0	0	1	0	0	1	0	0
1	1	0	1	1	1	1	1	1	1
1	0	0	0	0	0	0	0	0	0
1	0	0	1	1	1	0	1	1	0

- **K-maps**



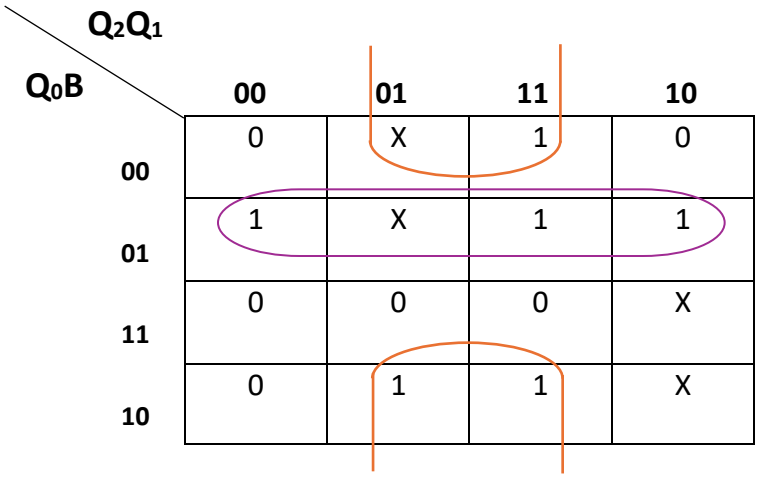
For D_0:

$$D_0 = \overline{B}\,\overline{Q_2} + BQ_1$$



For D_1:

$$D_1 = \overline{B}\,Q_0 + BQ_2$$



For D_2:

$$D_2 = \overline{Q_0}\,B + \bar{B}Q_1$$

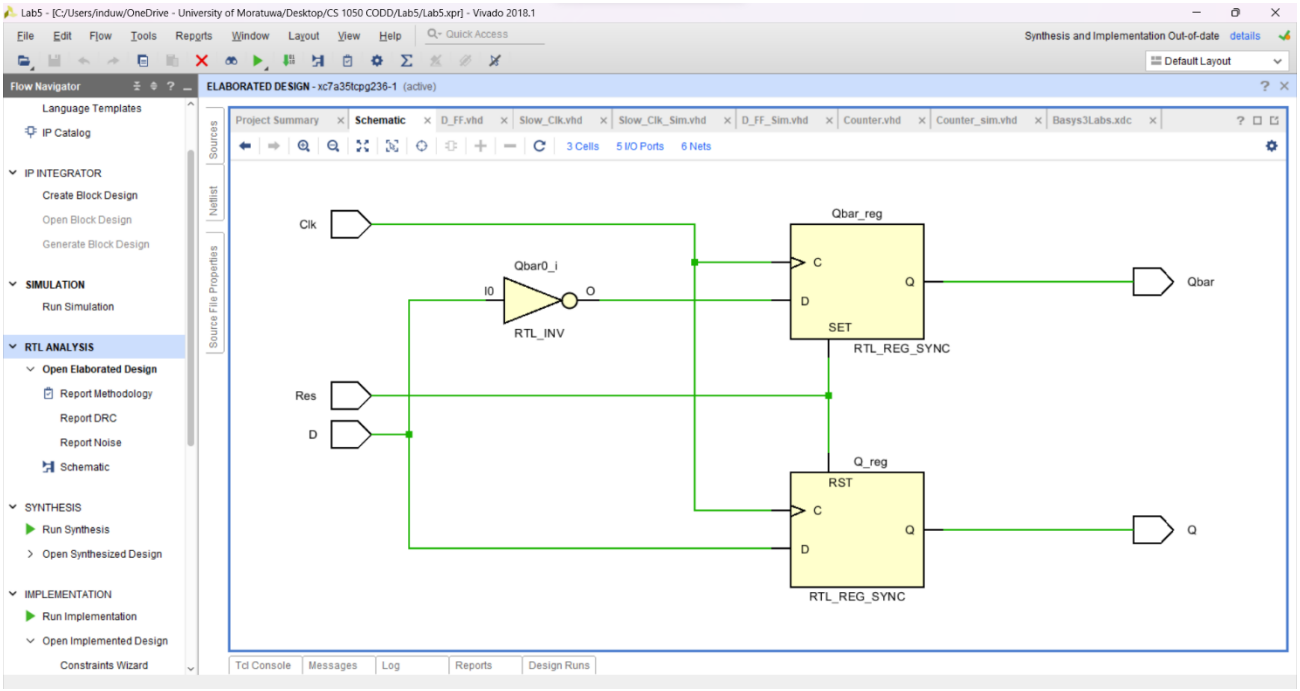
1. D Flip Flop

- **Design source file**

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 03/05/2024 02:16:03 PM
-- Design Name:
-- Module Name: D_FF - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity D_FF is
    Port ( D : in STD_LOGIC;
```

```
            Res : in STD_LOGIC;
            Clk : in STD_LOGIC;
            Q : out STD_LOGIC;
            Qbar : out STD_LOGIC);
end D_FF;

architecture Behavioral of D_FF is

begin
    process (Clk) begin
        if (rising_edge(Clk)) then
            if Res = '1' then
                Q <= '0';
                Qbar <= '1';
            else
                Q <= D;
                Qbar <= not D;
            end if;
        end if;
    end process;

end Behavioral;
```

- **Elaborated design schematic**



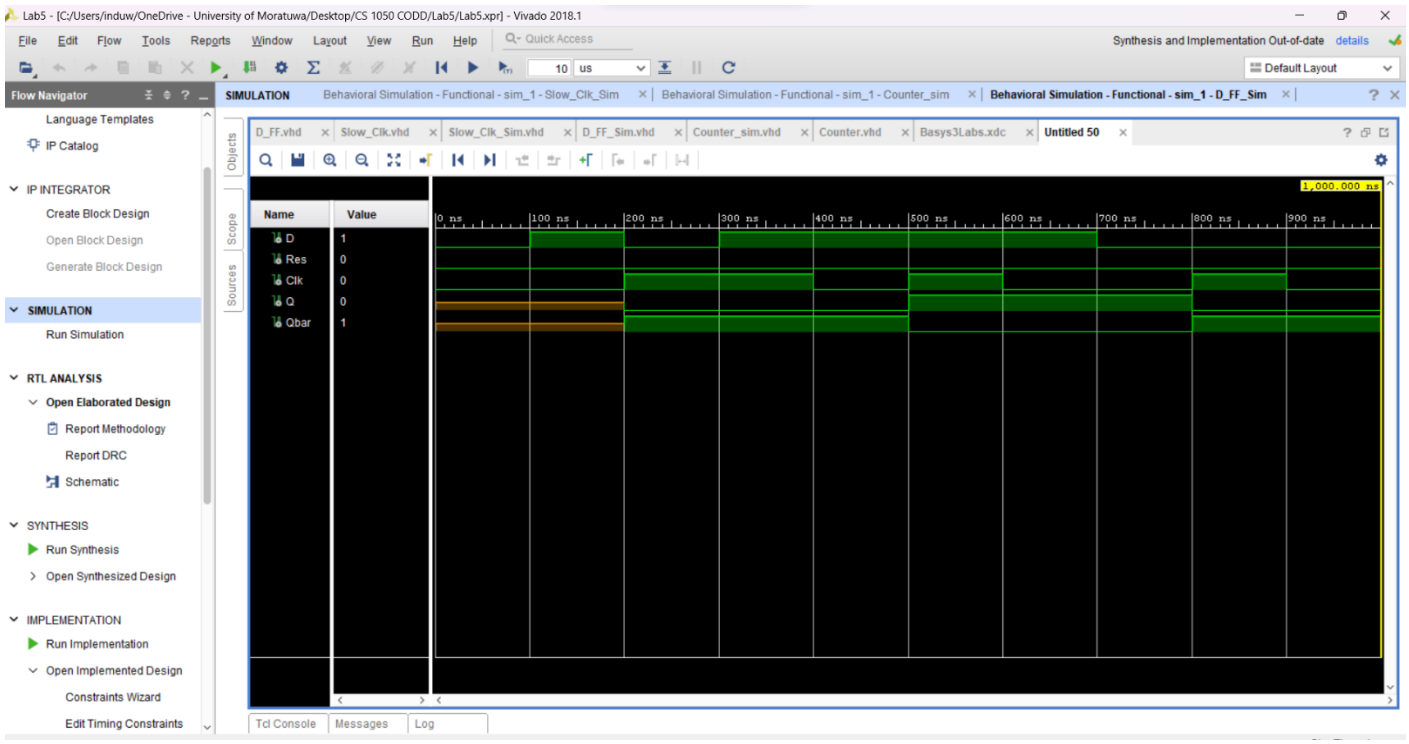
- **Simulation source file**

```
----------------------------------------------------------------------------
--------
-- Company:
-- Engineer:
--
-- Create Date: 03/05/2024 02:23:10 PM
-- Design Name:
-- Module Name: D_FF_Sim - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------
--------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity D_FF_Sim is
--  Port ( );
end D_FF_Sim;
```

```
architecture Behavioral of D_FF_Sim is

component D_FF
    Port ( D : in STD_LOGIC;
           Res : in STD_LOGIC;
           Clk : in STD_LOGIC;
           Q : out STD_LOGIC;
           Qbar : out STD_LOGIC);
end component;

signal D, Res, Clk : std_logic;
signal Q, Qbar : std_logic;

begin
UUT: D_FF port map(D,Res,Clk,Q,Qbar);

process begin
    D <= '0';
    Res <= '0';
    Clk <= '0';

    wait for 100 ns;
    D <= '1';

    wait for 100 ns;
    D <= '0';
    Clk <= '1';

    wait for 100 ns;
    D <= '1';

    wait for 100 ns;
    Clk <= '0';

    wait for 100 ns;
    Clk <= '1';

    wait for 100 ns;
    Clk <= '0';
```

```
    wait for 100 ns;
    D <= '0';

    wait for 100 ns;
    Clk <= '1';

    wait for 100 ns;
    Clk <= '0';

    wait for 100 ns;
    D <= '1';

    wait for 100 ns;
    Clk <= '1';

    wait for 100 ns;
    Clk <= '0';

    wait for 100ns;
    Res <='1';

    wait for 100 ns;
    Clk <= '1';

    wait for 100 ns;
    Clk <= '0';

    wait for 100 ns;
    D <= '0';

    wait;
end process;

end Behavioral;
```

- **Time diagram**



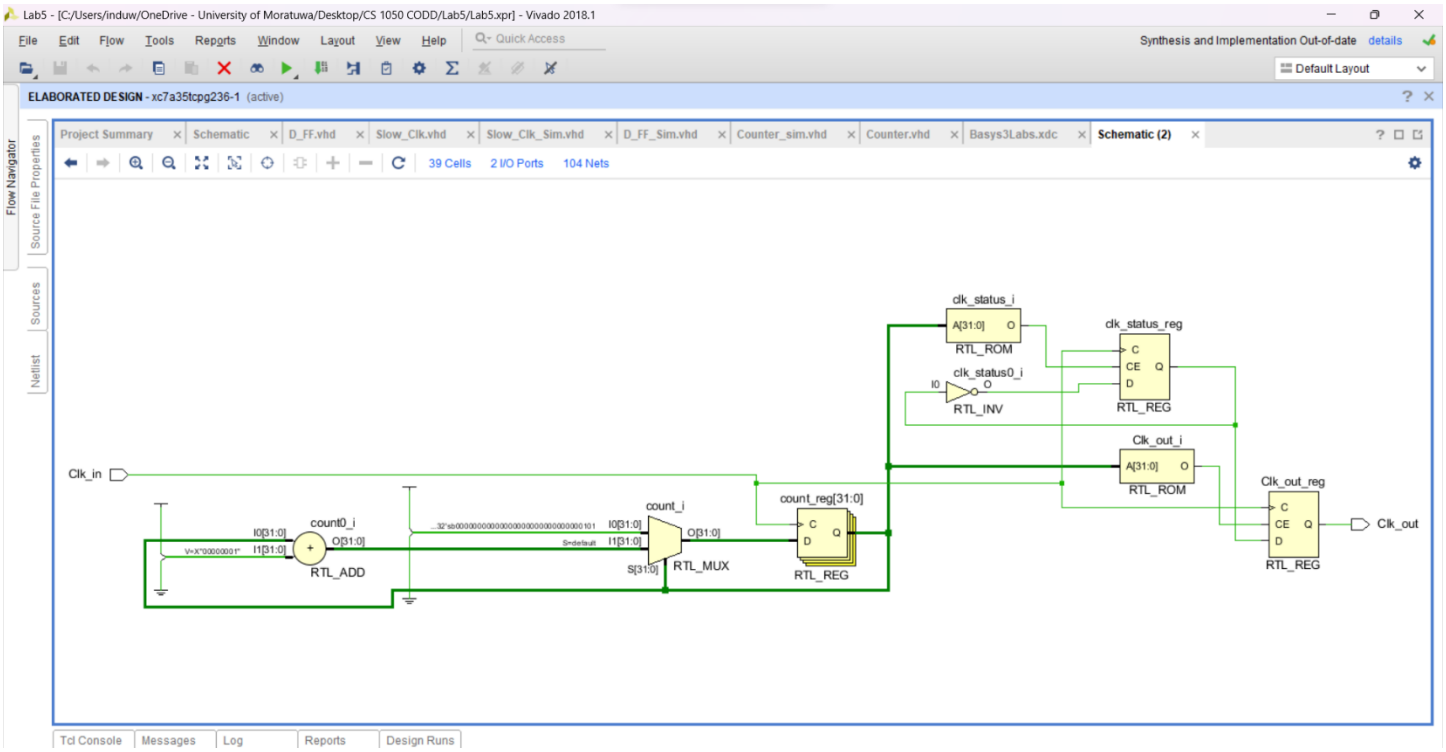
2. Slow Clock

- **Design source file**

```
----------------------------------------------------------------------------------
--------
-- Company:
-- Engineer:
--
-- Create Date: 03/05/2024 04:35:23 PM
-- Design Name:
-- Module Name: Slow_Clk - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
```

```
----------------------------------------------------------------------------
--------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Slow_Clk is
    Port ( Clk_in : in STD_LOGIC;
           Clk_out : out STD_LOGIC);
end Slow_Clk;

architecture Behavioral of Slow_Clk is

signal count : integer := 1;
signal clk_status : std_logic := '0';

begin
    process (Clk_in) begin
        if (rising_edge(Clk_in)) then
          count <= count + 1;
          if(count = 5) then--For simulation purposes,reduce 50000000 to 5
                clk_status <= not clk_status;
                Clk_out <= clk_status;
                count <= 1;
          end if;
      end if;
  end process;

end Behavioral;
```

- **Elaborated design schematic**



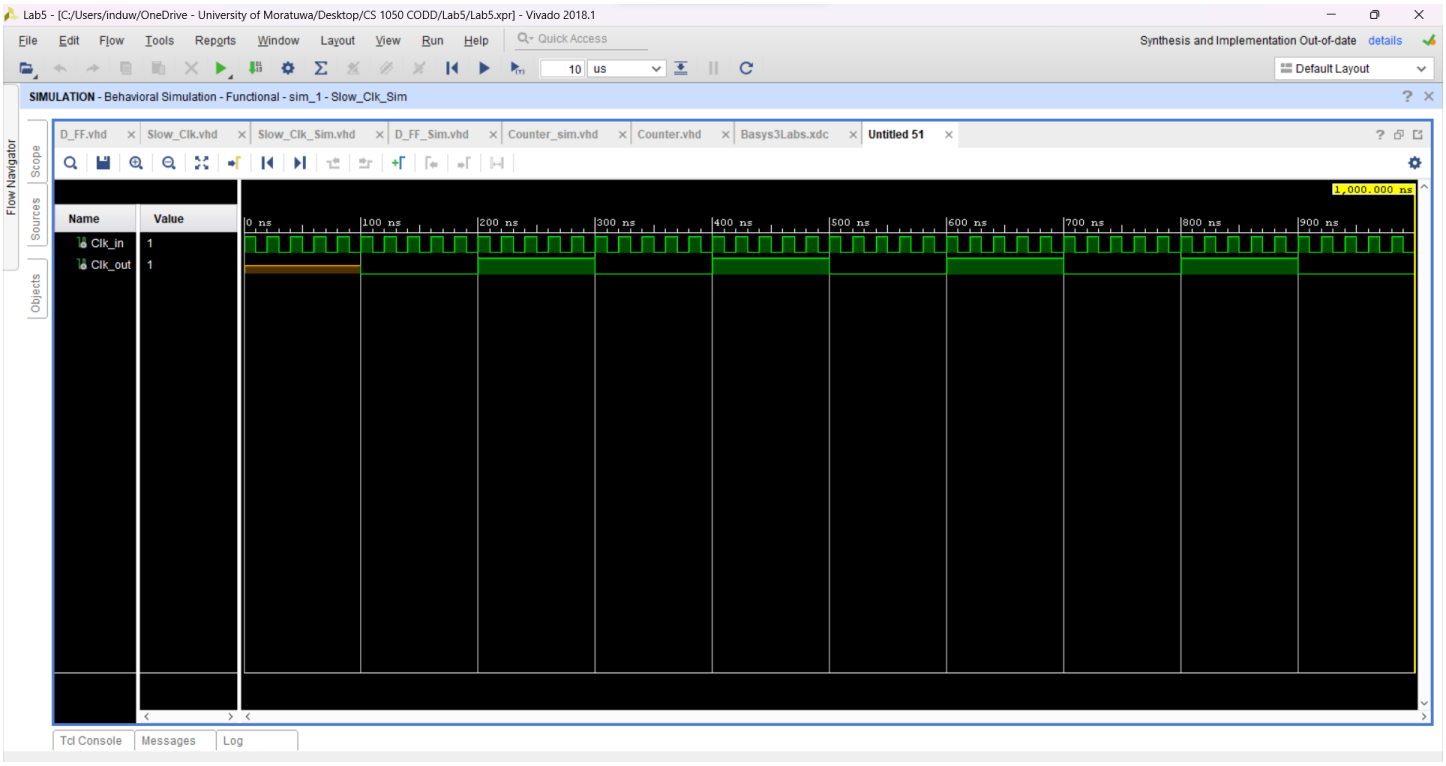
- **Simulation source file**

```
----------------------------------------------------------------------------------
--------
-- Company:
-- Engineer:
--
-- Create Date: 03/05/2024 04:48:53 PM
-- Design Name:
-- Module Name: Slow_Clk_Sim - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
```

```
----------------------------------------------------------------------------
--------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Slow_Clk_Sim is
--  Port ( );
end Slow_Clk_Sim;

architecture Behavioral of Slow_Clk_Sim is

component Slow_Clk is
    Port ( Clk_in : in STD_LOGIC;
           Clk_out : out STD_LOGIC);
end component;

signal Clk_in: std_logic;
signal Clk_out : std_logic;

begin

UUT: Slow_Clk port map(Clk_in,Clk_out);

process begin

    Clk_in <= '1';
    wait for 10 ns;

    Clk_in <= '0';
```

```
    wait for 10 ns;

end process;
end Behavioral;
```

- **Time diagram**



3. 3-bit Counter

- **Design source file**

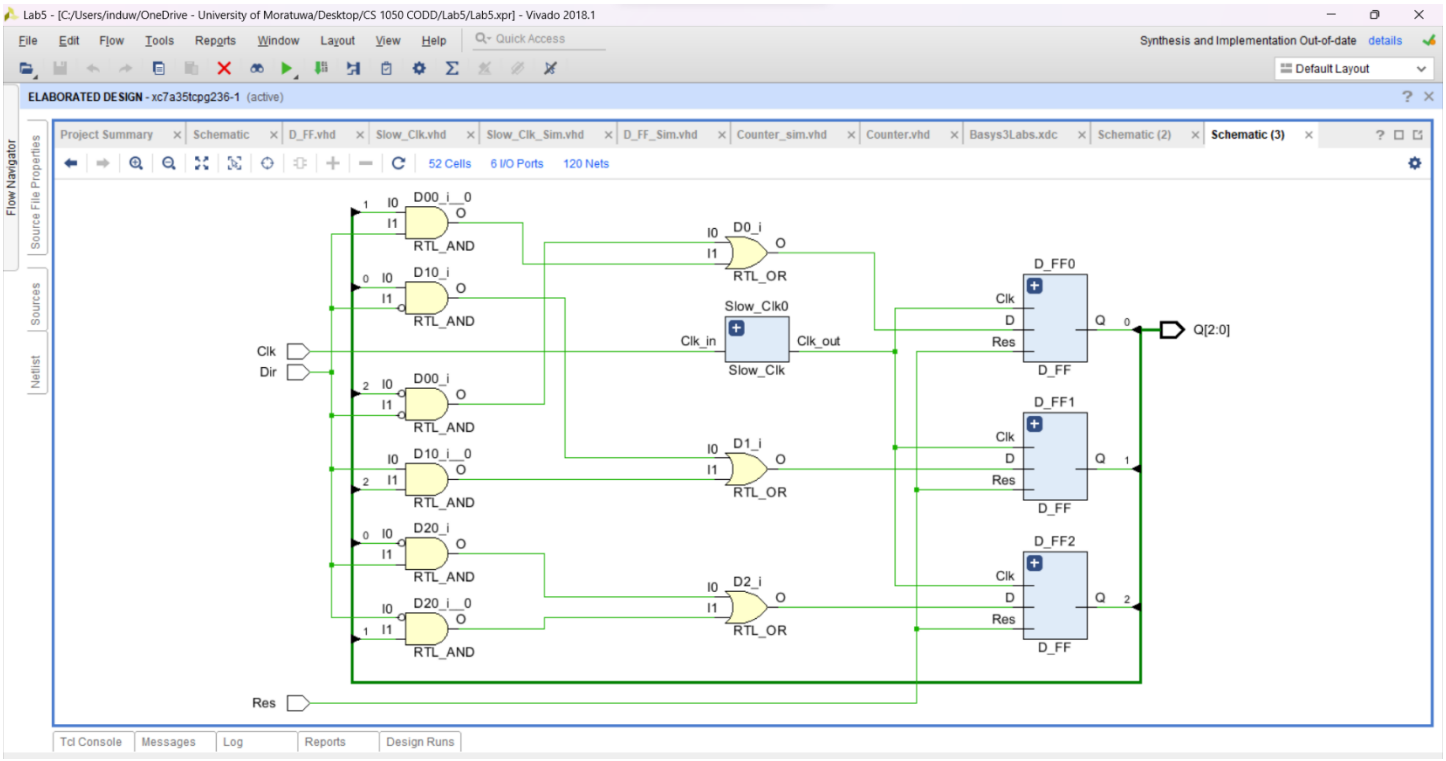
```
----------------------------------------------------------------------------------
--------
-- Company:
-- Engineer:
--
-- Create Date: 03/05/2024 05:18:15 PM
-- Design Name:
-- Module Name: Counter - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
```

```
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------
--------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Counter is
    Port ( Dir : in STD_LOGIC;
           Res : in STD_LOGIC;
           Clk : in STD_LOGIC;
           Q : out STD_LOGIC_VECTOR (2 downto 0));
end Counter;

architecture Behavioral of Counter is
component D_FF
    port (
    D : in STD_LOGIC;
    Res: in STD_LOGIC;
    Clk : in STD_LOGIC;
    Q : out STD_LOGIC;
    Qbar : out STD_LOGIC);
    end component;
```

```
component Slow_Clk
    port (
    Clk_in : in STD_LOGIC;
    Clk_out: out STD_LOGIC);
    end component;

signal D0, D1, D2 : std_logic;
signal Q0, Q1, Q2 : std_logic;
signal Clk_slow : std_logic;

begin
Slow_Clk0 : Slow_Clk
    port map (
    Clk_in => Clk,
    Clk_out => Clk_slow);

D0 <= ((not Q2) and (not Dir)) or (Q1 and Dir);
D1 <= (Q0 and (not Dir)) or (Dir and Q2);
D2 <= ((not Q0) and Dir) or ((not Dir) and Q1);

D_FF0 : D_FF
    port map (
    D => D0,
    Res => Res,
    Clk => Clk_slow,
    Q => Q0);

 D_FF1 : D_FF
    port map (
     D => D1,
     Res => Res,
     Clk => Clk_slow,
     Q => Q1);

 D_FF2 : D_FF
    port map (
    D => D2,
    Res => Res,
    Clk => Clk_slow,
    Q => Q2);
```

```
Q(0) <= Q0;
Q(1) <= Q1;
Q(2) <= Q2;

end Behavioral;
```

- **Elaborated design schematic**



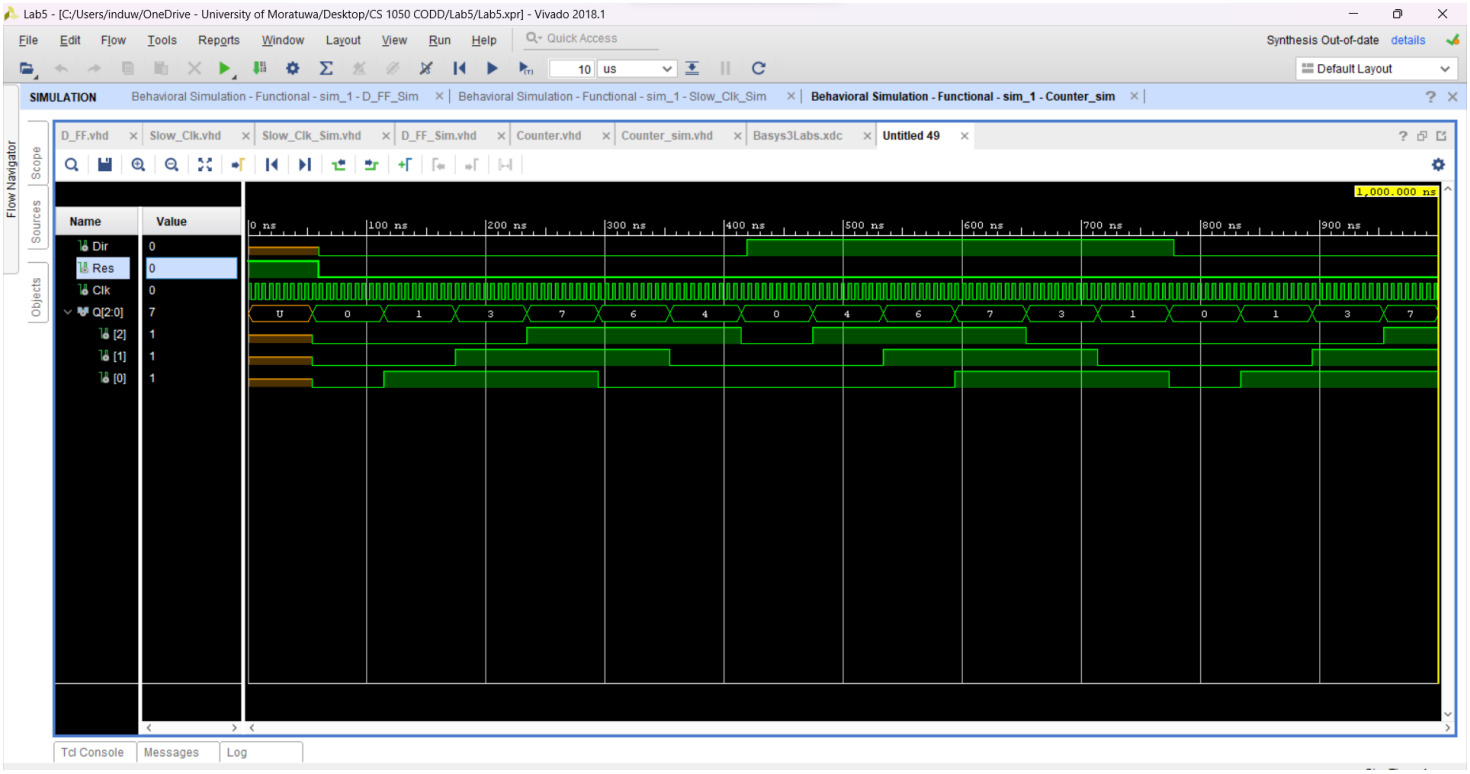
- **Simulation source file**

```
----------------------------------------------------------------------------------
--------
-- Company:
-- Engineer:
--
-- Create Date: 03/05/2024 05:27:58 PM
-- Design Name:
-- Module Name: Counter_sim - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
```

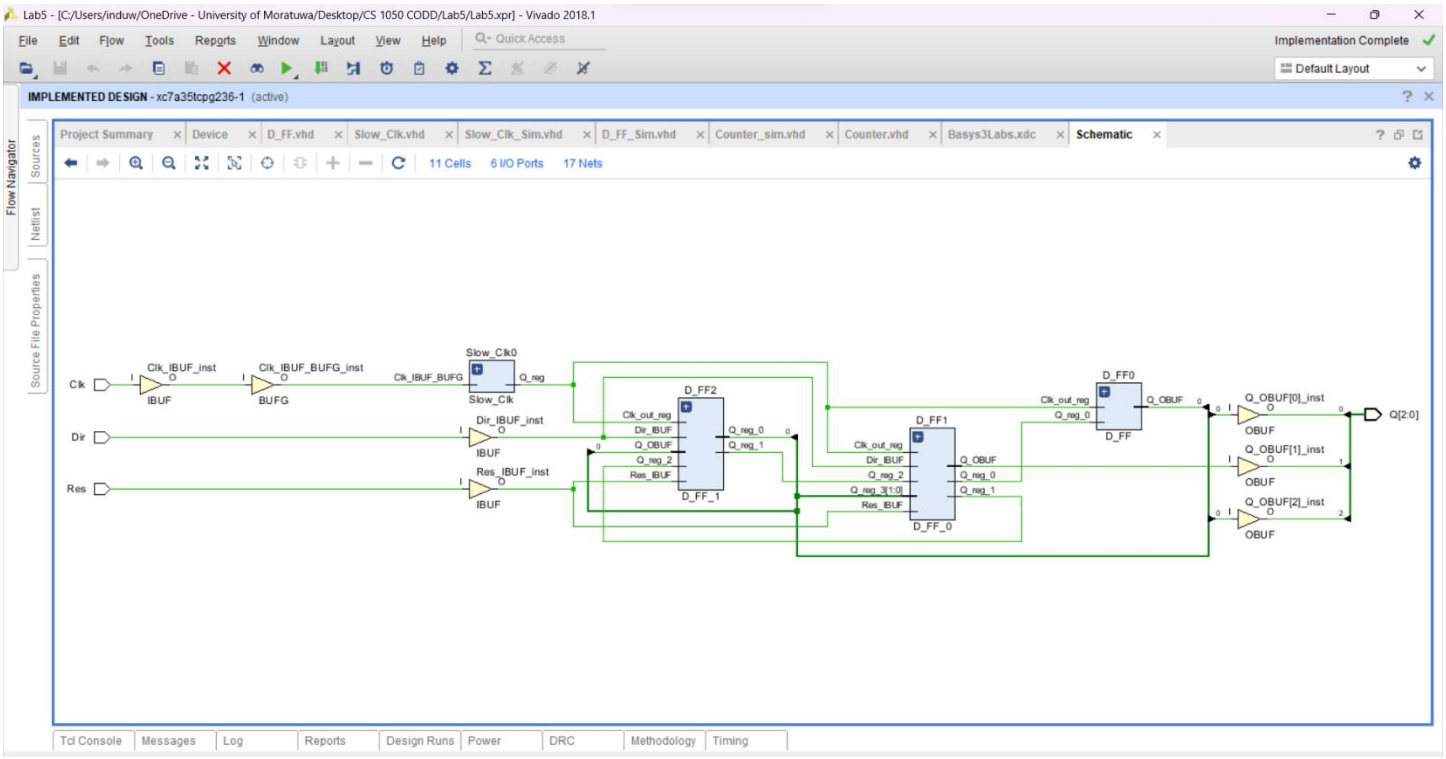
```
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------
--------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Counter_sim is
--  Port ( );
end Counter_sim;

architecture Behavioral of Counter_sim is
component Counter is
    Port ( Dir : in STD_LOGIC;
           Res : in STD_LOGIC;
           Clk : in STD_LOGIC;
           Q : out STD_LOGIC_VECTOR (2 downto 0));
end component;

signal Dir, Res: std_logic;
signal Clk: std_logic := '0';
signal Q : std_logic_vector(2 downto 0);

begin
UUT : Counter port map(Dir, Res, Clk, Q);

process begin
```

```
    Clk <= not Clk;
    wait for 3ns;
end process;

process begin

    Res <= '1';
    wait for 60ns;

    Res <= '0';
    Dir <= '0';
    wait for 359  ns;

    Dir <= '1';
    wait for 359  ns;

    Dir <= '0';
    wait;

end process;
end Behavioral;
```

- **Time diagram**



- **Implemented design schematic**



- **Constraints file**

```
## Clock signal
set_property PACKAGE_PIN W5 [get_ports {Clk}]
     set_property IOSTANDARD LVCMOS33 [get_ports {Clk}]
     create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports {Clk}]


## Switches
set_property PACKAGE_PIN V17 [get_ports {Dir}]
     set_property IOSTANDARD LVCMOS33 [get_ports {Dir}]


## LEDs
set_property PACKAGE_PIN U16 [get_ports {Q[0]}]
     set_property IOSTANDARD LVCMOS33 [get_ports {Q[0]}]
set_property PACKAGE_PIN E19 [get_ports {Q[1]}]
     set_property IOSTANDARD LVCMOS33 [get_ports {Q[1]}]
set_property PACKAGE_PIN U19 [get_ports {Q[2]}]
```

```
    set_property IOSTANDARD LVCMOS33 [get_ports {Q[2]}]

##Buttons
set_property PACKAGE_PIN U17 [get_ports Res]
    set_property IOSTANDARD LVCMOS33 [get_ports Res]
```

Conclusion

A simple counter can be created using basic logic gates and D-flipflops. Also, it can be implemented using JK-flipflops or T-flipflops instead of D-flipflops. An external switch can control the direction of the counter, while the clock pulse can increment or decrement that.