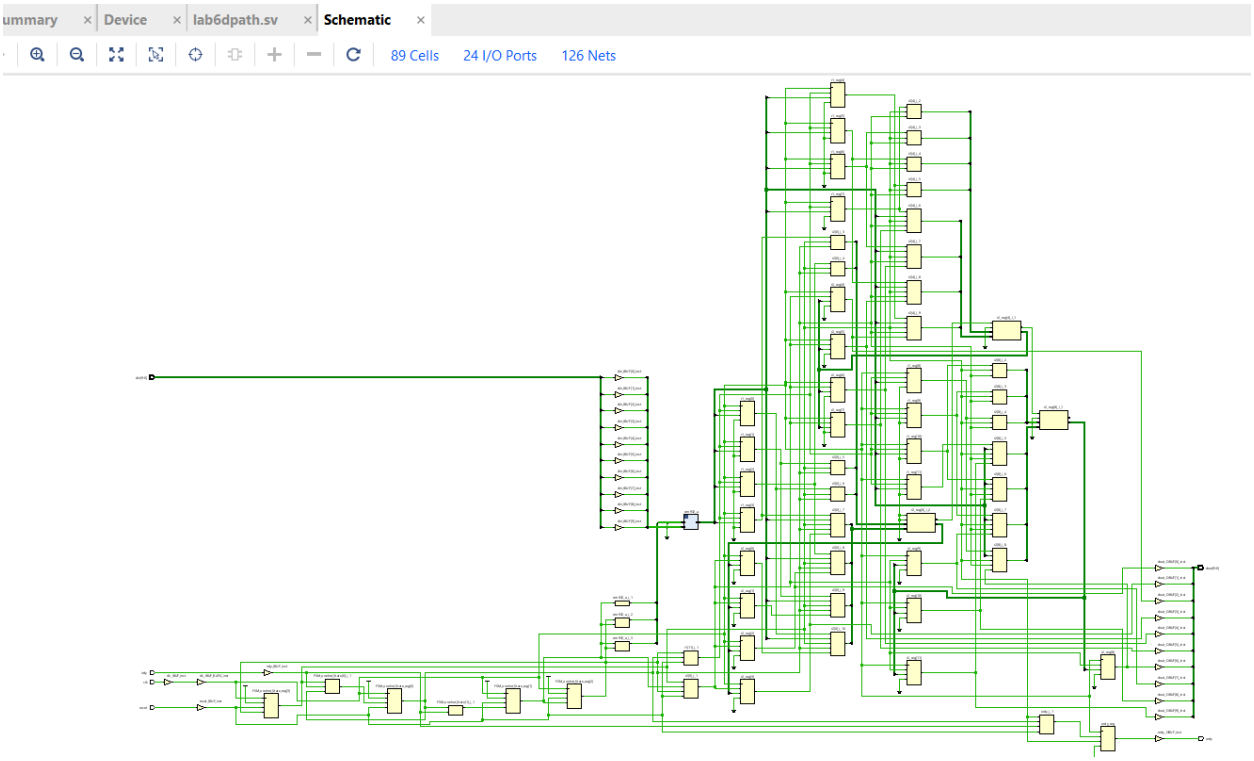
# Name: Cooper Medved

# Netid: Crm932

1. Part 1, Correct Design (50 pts).




2. Part 1, Resource Tables (Slice Logic, Summary of Registers by Type, DSP) ( 10 pts)

## 1. Slice Logic

| Site Type | Used | Fixed | Prohibited | Available | Util% |
|---|---|---|---|---|---|
| Slice LUTs | 19 | 0 | 0 | 8000 | 0.24 |
| LUT as Logic | 19 | 0 | 0 | 8000 | 0.24 |
| LUT as Memory | 0 | 0 | 0 | 5000 | 0.00 |
| Slice Registers | 29 | 0 | 0 | 16000 | 0.18 |
| Register as Flip Flop | 29 | 0 | 0 | 16000 | 0.18 |
| Register as Latch | 0 | 0 | 0 | 16000 | 0.00 |
| F7 Muxes | 0 | 0 | 0 | 7300 | 0.00 |
| F8 Muxes | 0 | 0 | 0 | 3650 | 0.00 |

* Warning! LUT value is adjusted to account for LUT combining.

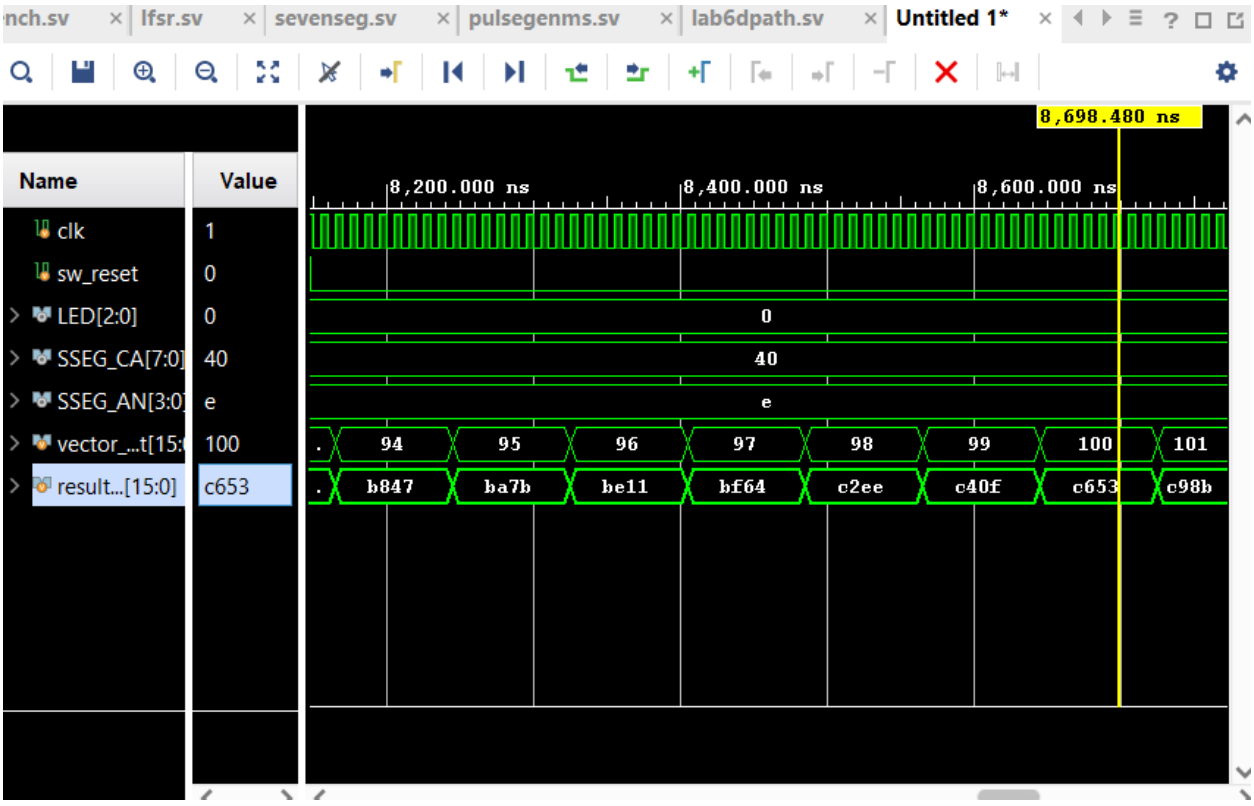
### 1.1 Summary of Registers by Type

| Total | Clock Enable | Synchronous | Asynchronous |
|---|---|---|---|
| 0 | _ | - | - |
| 0 | _ | - | Set |
| 0 | _ | - | Reset |
| 0 | _ | Set | - |
| 0 | _ | Reset | - |
| 0 | Yes | - | - |
| 1 | Yes | - | Set |
| 3 | Yes | - | Reset |
| 0 | Yes | Set | - |
| 25 | Yes | Reset | - |

## 4. DSP

| Site Type | Used | Fixed | Prohibited | Available | Util% |
|---|---|---|---|---|---|
| DSPs | 1 | 0 | 0 | 40 | 2.50 |
| DSP48E1 only | 1 | | | | |

3. Part 2, screenshot of checksum after 100 vectors (Part 2) (10 pts)




4. Part 2, Downloaded into board and verified by TA (30 pts).