Name: Cooper Medved

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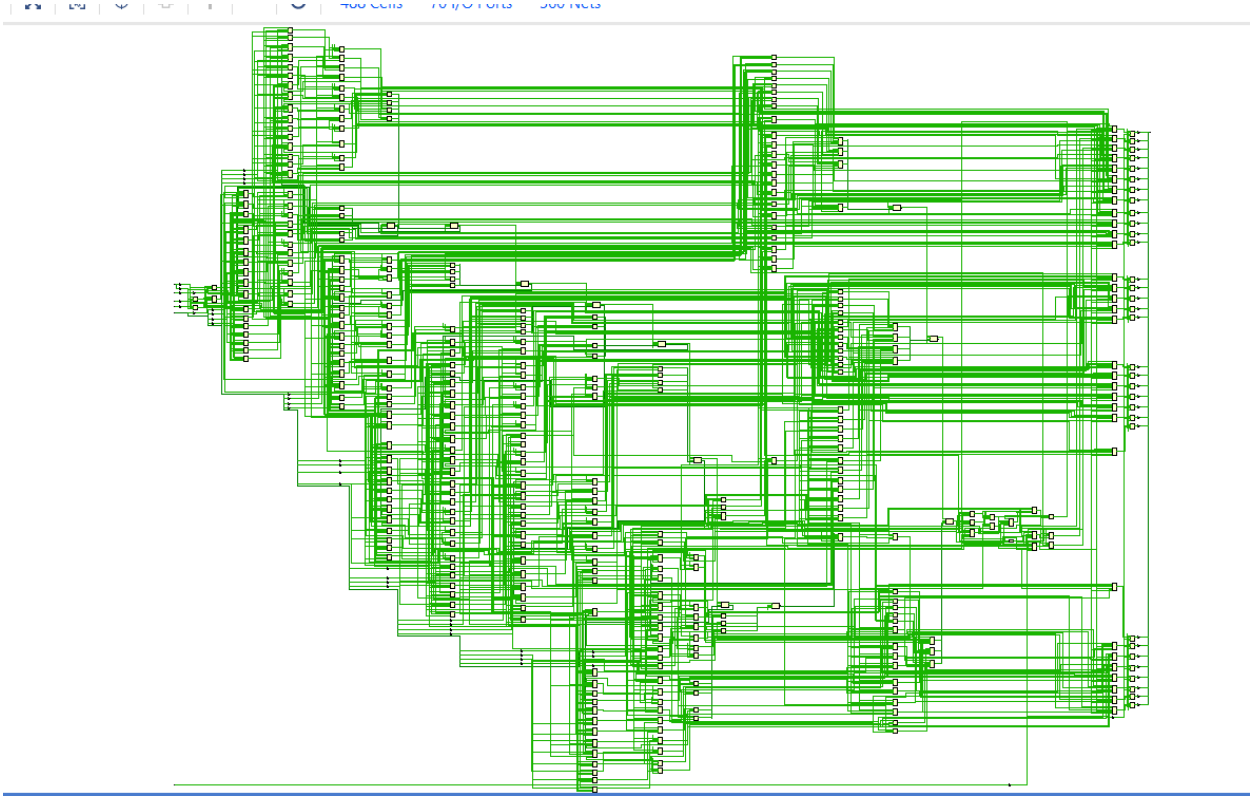
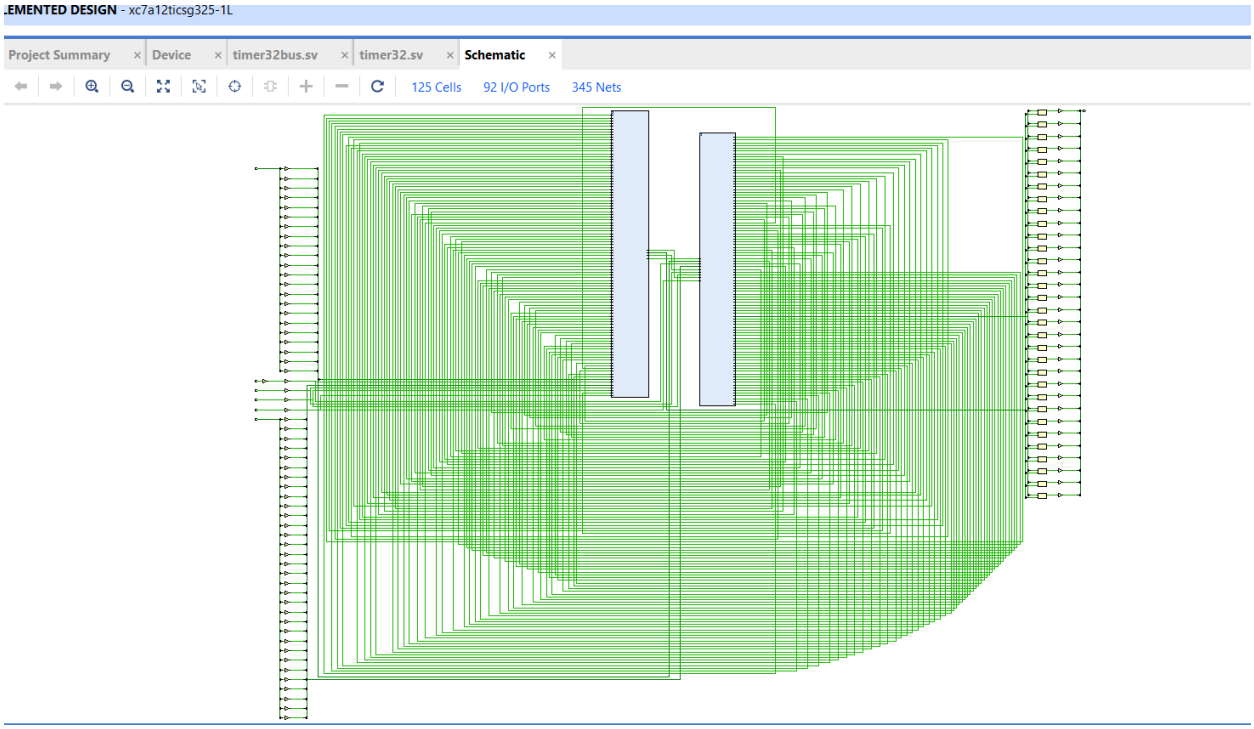
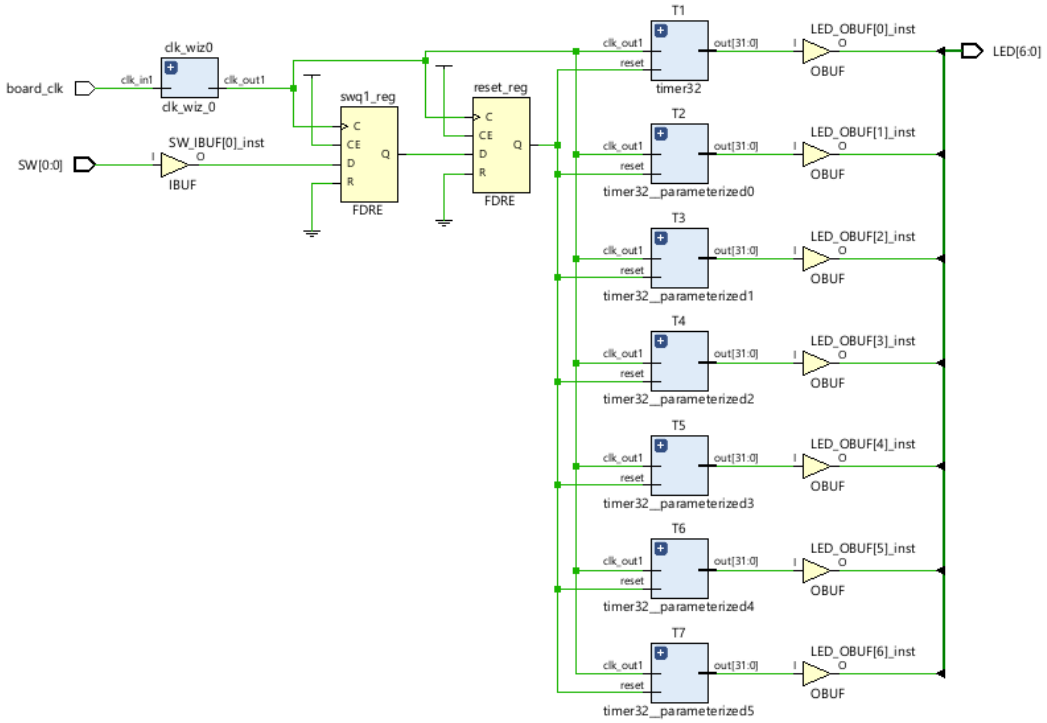
1. Correct Design part 1 (40 pts)



2. Correct Design part 2 (25 pts)



3. Correct Design part 3 (25 pts) with TA checkoff, design resources (Slice Logic, Summary of Registers by Type)



1. Slice Logic

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs	196	0	0	20800	0.94
LUT as Logic	196	0	0	20800	0.94
LUT as Memory	0	0	0	9600	0.00
Slice Registers	233	0	0	41600	0.56
Register as Flip Flop	233	0	0	41600	0.56
Register as Latch	0	0	0	41600	0.00
F7 Muxes	0	0	0	16300	0.00
F8 Muxes	0	0	0	8150	0.00

* Warning! LUT value is adjusted to account for LUT combining.

1.1 Summary of Registers by Type

Total	Clock Enable	Synchronous	Asynchronous
0	_	-	-
0	_	-	Set
0	_	-	Reset
0	_	Set	-
0	_	Reset	-
0	Yes	-	-
0	Yes	-	Set
231	Yes	-	Reset
0	Yes	Set	-
2	Yes	Reset	-

3. Memory

Site Type	Used	Fixed	Prohibited	Available	Util%
Block RAM Tile	0	0	0	50	0.00
RAMB36/FIFO*	0	0	0	50	0.00
RAMB18	0	0	0	100	0.00

* Note: Each Block RAM Tile only has one FIFO logic available and therefore can accommodate only one FIFO36E1 or one FIFO18E1. However, if a FIFO18E1 occupies a

4. DSP

4. (10 pts) Timing Analysis, part 3. Capture a screen shot from the timing analysis of the implemented design that gives the worst slack for Intra-clock paths for our 50 MHz clock (clk_out1_clk_wiz). This design is supposed to run at 50 MHz. Could this design run at 100 MHz based on the slack in the timing report (explain your answer in order to get credit, you cannot just say 'yes' or 'no').
   Yes cause the worst negative slack for the 50mhz was at 15ns so the clock period for 50mhz is 20ns and for 100mhz is 10 which reduced is 10ns subtract 15ns -10ns you get 5ns which is still positive slack for the worst negative slack so Yes I believe it would work.