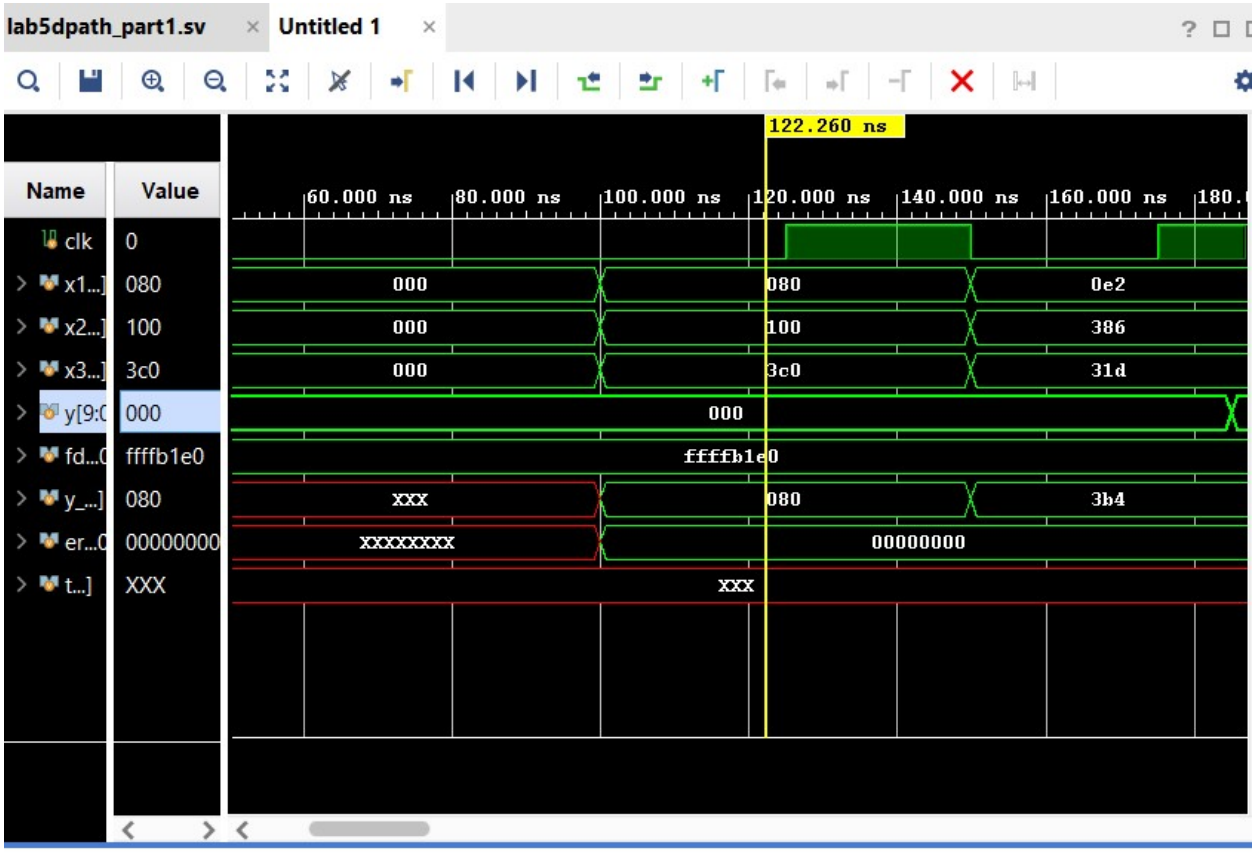
Name: Cooper Medved

Netid: crm932

1. Correct Design part 1 (25 pts with simulation screenshot, table data)

    a. Simulation Screenshot (includes screenshot of line from vector file that is being used in the screenshot). Simulation screenshot annotated to show latency. (13 pts)



    b. Resource Tables—Slice Logic, Summary of Registers, DSP Table (3 pts)

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs	12	0	0	8000	0.15
LUT as Logic	12	0	0	8000	0.15
LUT as Memory	0	0	0	5000	0.00
Slice Registers	40	0	0	16000	0.25
Register as Flip Flop	40	0	0	16000	0.25
Register as Latch	0	0	0	16000	0.00
F7 Muxes	0	0	0	7300	0.00
F8 Muxes	0	0	0	3650	0.00

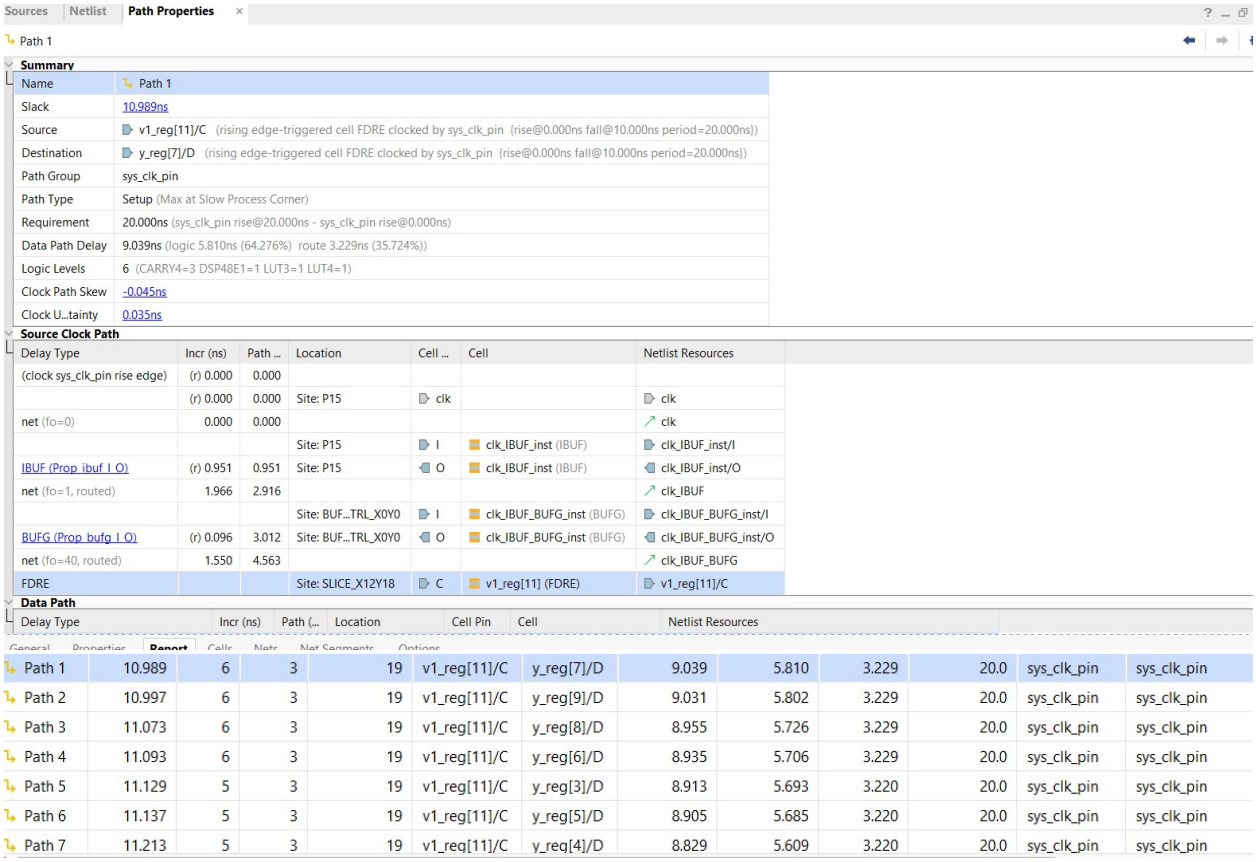
* Warning! LUT value is adjusted to account for LUT combining

Total	Clock Enable	Synchronous	Asynchronous
0	_	-	-
0	_	-	Set
0	_	-	Reset
0	_	Set	-
0	_	Reset	-
0	Yes	-	-
0	Yes	-	Set
0	Yes	-	Reset
0	Yes	Set	-
40	Yes	Reset	-

4. DSP

Site Type	Used	Fixed	Prohibited	Available	Util%
DSPs	3	0	0	40	7.50
DSP48E1 only	3				

c. Timing: longest register to register path: (3 pts)



Sources | Netlist | **Path Properties**

Path 1

Summary

Name	Path 1
Slack	10.989ns
Source	v1_reg[11]/C (rising edge-triggered cell FDRE clocked by sys_clk_pin {rise@0.000ns fall@10.000ns period=20.000ns})
Destination	y_reg[7]/D (rising edge-triggered cell FDRE clocked by sys_clk_pin {rise@0.000ns fall@10.000ns period=20.000ns})
Path Group	sys_clk_pin
Path Type	Setup (Max at Slow Process Corner)
Requirement	20.000ns (sys_clk_pin rise@20.000ns - sys_clk_pin rise@0.000ns)
Data Path Delay	9.039ns (logic 5.810ns (64.276%) route 3.229ns (35.724%))
Logic Levels	6 (CARRY4=3 DSP48E1=1 LUT3=1 LUT4=1)
Clock Path Skew	-0.045ns
Clock U...tainty	0.035ns

Source Clock Path

Delay Type	Incr (ns)	Path ...	Location	Cell ...	Cell	Netlist Resources
(clock sys_clk_pin rise edge)	(r) 0.000	0.000				
	(r) 0.000	0.000	Site: P15	clk		clk
net (fo=0)	0.000	0.000				clk
			Site: P15	I	clk_IBUF_inst (IBUF)	clk_IBUF_inst/I
IBUF (Prop_ibuf_I_O)	(r) 0.951	0.951	Site: P15	O	clk_IBUF_inst (IBUF)	clk_IBUF_inst/O
net (fo=1, routed)	1.966	2.916				clk_IBUF
			Site: BUF...TRL_X0Y0	I	clk_IBUF_BUFG_inst (BUFG)	clk_IBUF_BUFG_inst/I
BUFG (Prop_bufg_I_O)	(r) 0.096	3.012	Site: BUF...TRL_X0Y0	O	clk_IBUF_BUFG_inst (BUFG)	clk_IBUF_BUFG_inst/O
net (fo=40, routed)	1.550	4.563				clk_IBUF_BUFG
FDRE			Site: SLICE_X12Y18	C	v1_reg[11] (FDRE)	v1_reg[11]/C

Data Path

Delay Type	Incr (ns)	Path (...	Location	Cell Pin	Cell	Netlist Resources

General | Properties | **Report** | Cells | Nets | Net Segments | Options

Path 1	10.989	6	3	19	v1_reg[11]/C	y_reg[7]/D	9.039	5.810	3.229	20.0	sys_clk_pin	sys_clk_pin
Path 2	10.997	6	3	19	v1_reg[11]/C	y_reg[9]/D	9.031	5.802	3.229	20.0	sys_clk_pin	sys_clk_pin
Path 3	11.073	6	3	19	v1_reg[11]/C	y_reg[8]/D	8.955	5.726	3.229	20.0	sys_clk_pin	sys_clk_pin
Path 4	11.093	6	3	19	v1_reg[11]/C	y_reg[6]/D	8.935	5.706	3.229	20.0	sys_clk_pin	sys_clk_pin
Path 5	11.129	5	3	19	v1_reg[11]/C	y_reg[3]/D	8.913	5.693	3.220	20.0	sys_clk_pin	sys_clk_pin
Path 6	11.137	5	3	19	v1_reg[11]/C	y_reg[5]/D	8.905	5.685	3.220	20.0	sys_clk_pin	sys_clk_pin
Path 7	11.213	5	3	19	v1_reg[11]/C	y_reg[4]/D	8.829	5.609	3.220	20.0	sys_clk_pin	sys_clk_pin

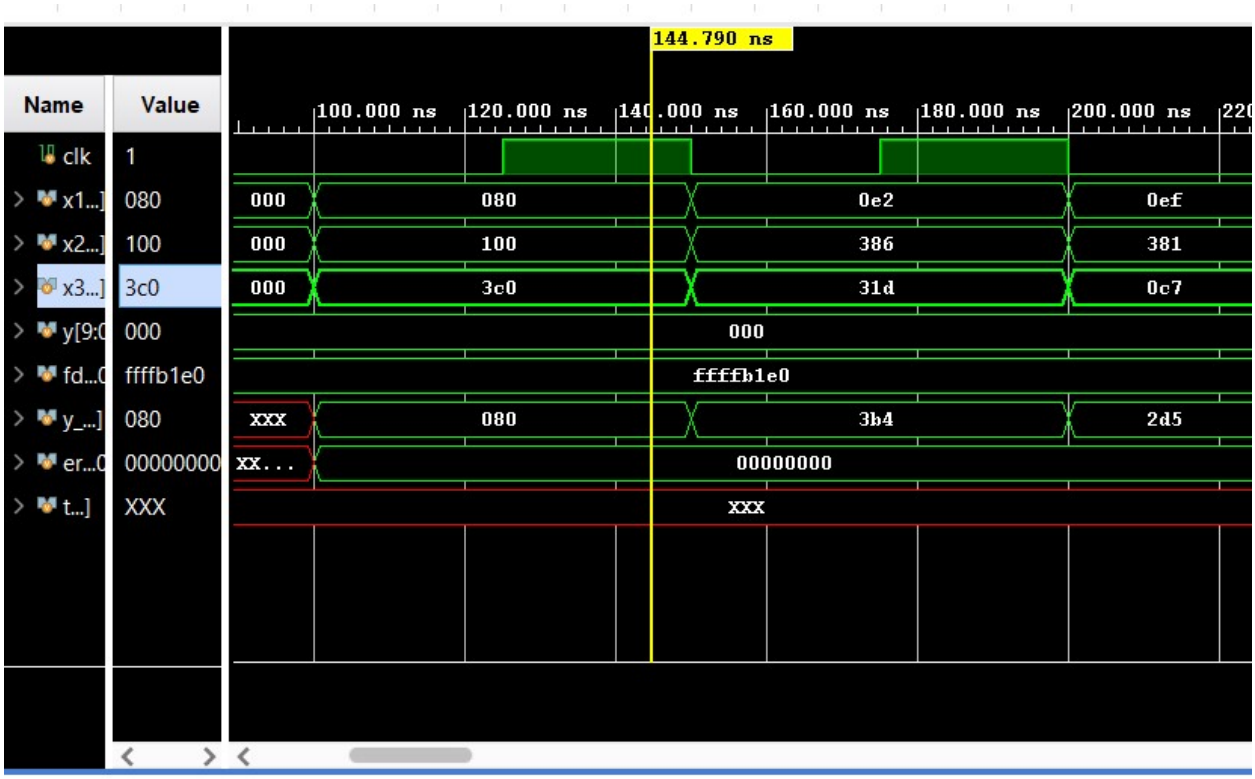
d. Timing: longest clock to output path: (3 pts)

Path 21	∞	1	1	1	x1[1]	v1_reg[3]/D	2.770	0.979	1.791	∞	input port clock	sys_clk_pin
Path 22	∞	1	1	1	x1[2]	v1_reg[4]/D	2.746	0.978	1.768	∞	input port clock	sys_clk_pin
Path 23	∞	1	1	1	x1[4]	v1_reg[6]/D	2.721	0.955	1.766	∞	input port clock	sys_clk_pin
Path 24	∞	1	1	1	x1[5]	v1_reg[7]/D	2.595	0.954	1.641	∞	input port clock	sys_clk_pin
Path 25	∞	1	1	1	x1[3]	v1_reg[5]/D	2.588	0.958	1.630	∞	input port clock	sys_clk_pin
Path 26	∞	1	1	1	x1[0]	v1_reg[2]/D	2.579	0.949	1.630	∞	input port clock	sys_clk_pin
Path 27	∞	1	1	1	x1[7]	v1_reg[9]/D	2.556	0.962	1.594	∞	input port clock	sys_clk_pin

e. Timing: longest input pin to input register path: (3 pts)

Path 41	∞	1	1	1	y_reg[9]/C	y[9]	5.665	3.123	2.541	∞	sys_clk_pin	
Path 42	∞	1	1	1	y_reg[8]/C	y[8]	5.655	3.126	2.529	∞	sys_clk_pin	
Path 43	∞	1	1	1	y_reg[5]/C	y[5]	5.544	3.127	2.417	∞	sys_clk_pin	
Path 44	∞	1	1	1	y_reg[2]/C	y[2]	5.536	3.138	2.398	∞	sys_clk_pin	
Path 45	∞	1	1	1	y_reg[4]/C	y[4]	5.516	3.126	2.390	∞	sys_clk_pin	
Path 46	∞	1	1	1	y_reg[3]/C	y[3]	5.512	3.134	2.378	∞	sys_clk_pin	
Path 47	∞	1	1	1	y_reg[7]/C	y[7]	5.507	3.113	2.393	∞	sys_clk_pin	

2. Correct Design part 2 (25 pts, with simulation screenshot, table data)
    a. Simulation screenshot (includes screenshot of line from vector file that is being used in the screenshot). Simulation screenshot annotated to show latency. (14 pts)



b. Resource usage: Slice Logic, Summary of Registers, DSP Table (3 pts)

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs	12	0	0	8000	0.15
LUT as Logic	12	0	0	8000	0.15
LUT as Memory	0	0	0	5000	0.00
Slice Registers	40	0	0	16000	0.25
Register as Flip Flop	40	0	0	16000	0.25
Register as Latch	0	0	0	16000	0.00
F7 Muxes	0	0	0	7300	0.00
F8 Muxes	0	0	0	3650	0.00

* Warning! LUT value is adjusted to account for LUT combining.

Total	Clock Enable	Synchronous	Asynchronous
0	_	-	-
0	_	-	Set
0	_	-	Reset
0	_	Set	-
0	_	Reset	-
0	Yes	-	-
0	Yes	-	Set
0	Yes	-	Reset
0	Yes	Set	-
40	Yes	Reset	-

4. DSP

Site Type	Used	Fixed	Prohibited	Available	Util%
DSPs	3	0	0	40	7.50
DSP48E1 only	3				

c. Timing – longest register to register path (3 pts)

Name	Path 1
Slack	14.358ns
Source	v1_reg[11]/C (rising edge-triggered cell FDRE clocked by sys_clk_pin {rise@0.000ns fall@10.000ns period=20.000ns})
Destination	crm932_a/U0/i_mult/gDSP.gDSP_only.iDSP/inferred_dsp.reg_mult.m_reg_reg/A[16] (rising edge-triggered cell DSP48E1 clocked by sys_clk_pin {rise@0.000ns fall@10.000ns period=20.000ns})
Path Group	sys_clk_pin
Path Type	Setup (Max at Slow Process Corner)
Requirement	20.000ns (sys_clk_pin rise@20.000ns - sys_clk_pin rise@0.000ns)
Data Path Delay	1.935ns (logic 0.518ns (26.769%) route 1.417ns (73.231%))
Logic Levels	0
Clock Path Skew	0.051ns
Clock U...tainty	0.035ns

Source Clock Path

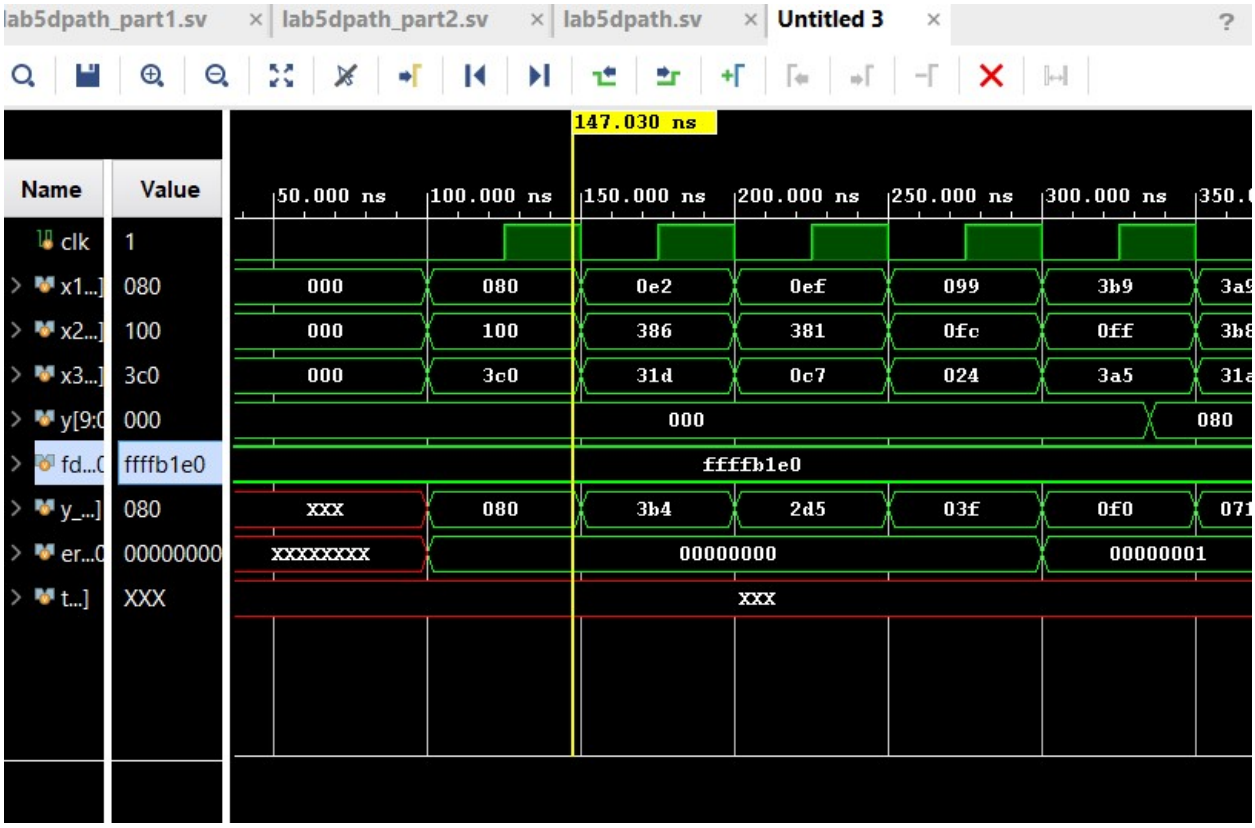
Delay Type	Incr (ns)	Path ...	Location	Cell ...	Cell	Netlist Resources
(clock sys_clk_pin rise edge)	(r) 0.000	0.000				
	(r) 0.000	0.000	Site: P15	clk		clk
net (fo=0)	0.000	0.000				clk
			Site: P15	I	clk_IBUF_inst (IBUF)	clk_IBUF_inst/I
IBUF (Prop_ibuf_I_O)	(r) 0.951	0.951	Site: P15	O	clk_IBUF_inst (IBUF)	clk_IBUF_inst/O
net (fo=1, routed)	1.966	2.916				clk_IBUF
			Site: BUF...TRL_X0Y0	I	clk_IBUF_BUFG_inst (BUFG)	clk_IBUF_BUFG_inst/I
BUFG (Prop_bufg_I_O)	(r) 0.096	3.012	Site: BUF...TRL_X0Y0	O	clk_IBUF_BUFG_inst (BUFG)	clk_IBUF_BUFG_inst/O
net (fo=43, routed)	1.550	4.563				clk_IBUF_BUFG
FDRE			Site: SLICE_X12Y18	C	v1_reg[11] (FDRE)	v1_reg[11]/C

Path 1	14.358	0	1	19	v1_reg[11]/C	crm932_a/U0/i_..._reg_reg/A[16]	1.935	0.518	1.417	20.0	sys_clk_pin
Path 2	14.358	0	1	19	v1_reg[11]/C	crm932_a/U0/i_..._reg_reg/A[17]	1.935	0.518	1.417	20.0	sys_clk_pin
Path 3	14.358	0	1	19	v1_reg[11]/C	crm932_a/U0/i_..._reg_reg/A[18]	1.935	0.518	1.417	20.0	sys_clk_pin
Path 4	14.358	0	1	19	v1_reg[11]/C	crm932_a/U0/i_..._reg_reg/A[19]	1.935	0.518	1.417	20.0	sys_clk_pin
Path 5	14.525	0	1	19	v1_reg[11]/C	crm932_a/U0/i_..._reg_reg/A[12]	1.768	0.518	1.250	20.0	sys_clk_pin
Path 6	14.525	0	1	19	v1_reg[11]/C	crm932_a/U0/i_..._reg_reg/A[13]	1.768	0.518	1.250	20.0	sys_clk_pin
Path 7	14.525	0	1	19	v1_reg[11]/C	crm932_a/U0/i_..._reg_reg/A[14]	1.768	0.518	1.250	20.0	sys_clk_pin

d. Is the above path from the output of the input register to the multiplier input or is it from the output of the multiplier to input of the output register? (5 pts)
Output of the multiplier to input of the output register

3. Correct Design part 3 (40 pts, with simulation screenshot, table data)

    a. Simulation screenshot (includes screenshot of line from vector file that is being used in the screenshot). Simulation screenshot annotated to show latency. (20 pts)



    b. Resource Usage: Slice Logic, Summary of Registers, DSP Table (5 pts)

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs	120	0	0	8000	1.50
LUT as Logic	120	0	0	8000	1.50
LUT as Memory	0	0	0	5000	0.00
Slice Registers	156	0	0	16000	0.98
Register as Flip Flop	156	0	0	16000	0.98
Register as Latch	0	0	0	16000	0.00
F7 Muxes	0	0	0	7300	0.00
F8 Muxes	0	0	0	3650	0.00

* Warning! LUT value is adjusted to account for LUT combining.

Total	Clock Enable	Synchronous	Asynchronous
0	_	-	-
0	_	-	Set
0	_	-	Reset
0	_	Set	-
0	_	Reset	-
0	Yes	-	-
0	Yes	-	Set
0	Yes	-	Reset
0	Yes	Set	-
156	Yes	Reset	-

4. DSP

Site Type	Used	Fixed	Prohibited	Available	Util%
DSPs	0	0	0	40	0.00

c. Timing, longest register to register path: (5 pts)

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock
Path 1	15.298	7	2	4	v2_reg[3]/C	crm932_b/U0/i_m...t_reg[2][15]/D	4.743	2.413	2.330	20.0	sys_clk_pin
Path 2	15.402	7	2	4	v2_reg[3]/C	crm932_b/U0/i_m...t_reg[2][14]/D	4.639	2.309	2.330	20.0	sys_clk_pin
Path 3	15.443	6	2	3	v2_reg[3]/C	crm932_b/U0/i_m...t_reg[2][11]/D	4.598	2.299	2.299	20.0	sys_clk_pin
Path 4	15.451	6	2	3	v2_reg[3]/C	crm932_b/U0/i_m...t_reg[2][13]/D	4.590	2.291	2.299	20.0	sys_clk_pin
Path 5	15.527	6	2	3	v2_reg[3]/C	crm932_b/U0/i_m...t_reg[2][12]/D	4.514	2.215	2.299	20.0	sys_clk_pin
Path 6	15.547	6	2	3	v2_reg[3]/C	crm932_b/U0/i_m...t_reg[2][10]/D	4.494	2.195	2.299	20.0	sys_clk_pin
Path 7	15.601	5	2	4	v1_reg[4]/C	crm932_a/U0/i_m...t_reg[2][15]/D	4.442	2.448	1.994	20.0	sys_clk_pin

Path Properties

Path 1

Summary

Name	Path 1
Slack	15.298ns
Source	v2_reg[3]/C (rising edge-triggered cell FDRE clocked by sys_clk_pin {rise@0.000ns fall@10.000ns period=20.000ns})
Destination	crm932_b/U0/i_mult/gLUT.gLUT_speed.iLUT/NxM_mult.stage_1_add.stage_1_pipeline.s1_add_out_reg[2][15]/D (rising edge-triggered cell FDRE clocked by sys_clk_pin {rise@0.000ns fall@10.000ns period=20.000ns})
Path Group	sys_clk_pin
Path Type	Setup (Max at Slow Process Corner)
Requirement	20.000ns (sys_clk_pin rise@20.000ns - sys_clk_pin rise@0.000ns)
Data Path Delay	4.743ns (logic 2.413ns (50.871%) route 2.330ns (49.129%))
Logic Levels	7 (CARRY4=5 LUT1=1 LUT2=1)
Clock Path Skew	-0.032ns
Clock U...tainty	0.035ns

Source Clock Path

Delay Type	Incr (ns)	Path ...	Location	Cell ...	Cell	Netlist Resources
(clock sys_clk_pin rise edge)	(r) 0.000	0.000				
	(r) 0.000	0.000	Site: P15	clk		clk
net (fo=0)	0.000	0.000				clk
			Site: P15	I	clk_IBUF_inst (IBUF)	clk_IBUF_inst/I
IBUF (Prop_ibuf_I_O)	(r) 0.951	0.951	Site: P15	O	clk_IBUF_inst (IBUF)	clk_IBUF_inst/O
net (fo=1, routed)	1.966	2.916				clk_IBUF
			Site: BUF...TRL_X0Y0	I	clk_IBUF_BUFG_inst (BUFG)	clk_IBUF_BUFG_inst/I
BUFG (Prop_bufg_I_O)	(r) 0.096	3.012	Site: BUF...TRL_X0Y0	O	clk_IBUF_BUFG_inst (BUFG)	clk_IBUF_BUFG_inst/O
net (fo=156, routed)	1.625	4.638				clk_IBUF_BUFG
FDRE			Site: SLICE_X5Y12	C	v2_reg[3] (FDRE)	v2_reg[3]/C

Data Path

d. Is the above longest registers path in Path group A, B, C, D? Explain your justification. (10 pts)

C to D based on the longest path timing properties report

4. Question (10 pts): From the utilization data for part 1, show a calculation verifying the number of DFFs in the design (these DFFs are all 'Slice Registers as Flip Flops). FYI, this number does not increase in part 2 because the register used on the output of the Multiplier is inside the DSP48 block, not in the Slices. Also show a calculation verifying the number of Slice Registers (DFFS) for part 3 (do not count any of the registers associated with the multiplier).

   Dr. jones said don't do