# Lab Report #2

# Name: \_\_\_\_\_\_\_\_\_\_ Netid: \_\_\_\_\_\_\_\_\_\_\_

**Note: for this lab, you need to submit your corrected "max3sint16b.v" file and this report. Zip them together and name the zip folder after your netid.**

1. (10 pts) What is the third error identified in the video? What is the first test vector that fails because of this error (warning: the test vectors that you have are different from what is in the video. Capture a screen shot of the simulation showing the vectors the fail and explain why it fails. The vectors need to be formatted as signed decimal as shown in the video. Arrange the signals in the waveform viewer from top to bottom in the following order: a, b, u1\_lt, max\_ab, c, u2\_lt, y . The screenshot MUST have the yellow cursor over the failing vector.
2. (10 pts) What is the fourth error identified in the video? What is the first test vector that fails because of this error (warning: the test vectors that you have are different from what is in the video. Capture a screen shot of the simulation showing the vectors the fail and explain why it fails. The screenshot MUST have the yellow cursor over the failing vector.
3. (10 pts) What is the fifth error identified in the video? What is the first test vector that fails because of this error (warning: the test vectors that you have are different from what is in the video. Capture a screen shot of the simulation showing the vectors the fail and explain why it fails. The screenshot MUST have the yellow cursor over the failing vector.
4. (5 pts) After correcting all errors, capture a screenshot showing the last vector that causes the message ‘All vectors passed’ to be printed (can capture this message in the screenshot as well).
5. (5pts) Run the implementation, then run the ‘Post Implementation Timing Simulation’. Capture a screenshot showing the message ‘All vectors passed’. In the screenshot, have the ‘uut’ selected in the ‘Scope’ tab, and have the screenshot include some of the signals from the ‘uut’ (there will be some signals named ‘…OBUF’ in here in addition to other signals).
6. (10 pts) What is the difference between declaring a signed versus an unsigned wire?
7. (10 pts) What type does Verilog assume if a wire isn’t declared? How can this cause a problem for a multi-bit signal?
8. (10 pts) Why use behavioral simulation instead of other simulations when debugging Verilog?
9. (10 pts) After you run behavioral simulation, what should you do next to find useful waveform that helps you debug? If there is no waveform presents in your simulation, how to do? How do you know the total time that you should run to pass all your test vectors when you execute “run” command in TCL?
10. (20 pts) Based your understanding of the video, how should we do hardware debugging? Make a clear summary.