NOTES: UNLESS OTHERWISE SPECIFIED

1. SPECIFICATIONS/TOLERANCES:
   A. FABRICATE PER IPC-6012, CLASS 2, USING PROVIDED DATA FILES 610-60500-01_22.ZIP.
   B. ALL SPECIFICATIONS USED SHALL BE PER THEIR LATEST REVISIONS.
   C. THE DIMENSIONS OF CIRCUIT FEATURES IN THE PROVIDED DATA MAY BE ADJUSTED ONLY TO COMPENSATE FOR PROCESS TOLERANCES; ADDING, REMOVING OR RELOCATING CIRCUIT FEATURES, INCLUDING NON-FUNCTIONAL PADS, IS NOT ALLOWED, AND THE DESIGN OF ALL PLANE STRUCTURES MUST BE MAINTAINED TO ENSURE PROPER ELECTRICAL PERFORMANCE.
   D. REMOVE ALL BURRS AND BREAK SHARP EDGES, .381 [.015] MAX RADIUS.
   E. PARENTHETICAL INFORMATION IS FOR REFERENCE ONLY.
   F. REPAIR OF PCB DEFECTS IS NOT PERMITTED.

2. DIELECTRIC MATERIAL:
   A. DIELECTRIC MATERIAL SHALL BE PER IPC-4101/99, /124, /126 OR /129 (RoHS COMPLIANT EPOXY-GLASS).
   B. MINIMUM DIELECTRIC THICKNESS SHALL BE .051 [.002] FOR REFERENCED STACK-UP DIMENSIONS OF.076 [.003] OR GREATER; IPC-6012 REQUIREMENTS SHALL OTHERWISE APPLY. SINGLE-PLY CONSTRUCTION IS ALLOWED.
   C. SEE LAYER STACK-UP FOR REQUIRED COPPER WEIGHTS AND THE FINISHED PCB THICKNESS. IF SPECIFIED, 1/3 OZ. STARTING FOIL MAY BE ACHIEVED BY 1/2 OZ. FOIL REDUCTION.
   D. FINISHED PCB THICKNESS SHALL BE MEASURED OVER LANDS AND/OR CONDUCTORS NOT COVERED BY SOLDER MASK.

3. DRILLING:
   A. VIA DIAMETERS (TOL. = +.051/- DRILL DIAMETER [+.0020/- DRILL DIAMETER]) SHALL BE VERIFIED BEFORE PLATING; ALL OTHER HOLE DIAMETERS SHALL BE VERIFIED AT FINAL INSPECTION.
   B. LAYER-TO-LAYER MISREGISTRATION SHALL BE .127 [.005] MAXIMUM.

4. SOLDER MASK:
   A. APPLY LPI SOLDER MASK USING PROVIDED DATA.
   B. SOLDER MASK SHALL BE PER IPC-SM-840, CLASS T, COLOR RED.
   C. THE DIMENSIONS OF SOLDER MASK-DEFINED PADS ON PLANES AND/OR WIDE CONDUCTORS SHALL NOT BE MODIFIED.

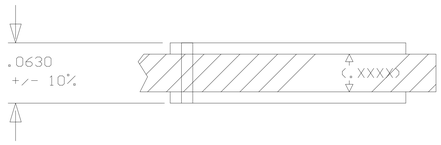
5. MARKING:
   A. MARK PCB PER PROVIDED DATA USING SILKSCREEN OR AUTOMATED INJET PROCESSING WITH PERMANENT, NON-CONDUCTIVE INK, COLOR WHITE.
   B. SUPPLIER ID AND TRACEABILITY INFORMATION SHALL BE APPLIED USING PERMANENT, NON-CONDUCTIVE INK, COLOR WHITE.
   C. INK SHALL NOT BE APPLIED TO ANY SOLDERABLE SURFACE.

6. ELECTRICAL TEST:
   A. DESIGN VERIFICATION SHALL BE DONE PRIOR TO PCB FABRICATION USING SUPPLIED VALOR ODB++ DATABASE, OR GERBER DATA AND AN IPC-D-356 NETLIST.
   B. ALL PCBS SHALL BE 100% ELECTRICALLY TESTED FOR OPENS AND SHORTS USING PROVIDED DATA.
   C. APPLY TEST STAMP IN NON-LEGEND AREA ON REAR SIDE OF PCB; OK TO APPLY TO PANEL RAILS IF SPACE DOES NOT PERMIT.

7. FINAL FINISH:
   A. FINAL FINISH SHALL BE ELECTROLESS NICKEL/IMMERSION GOLD (ENIG) PER IPC-4552.

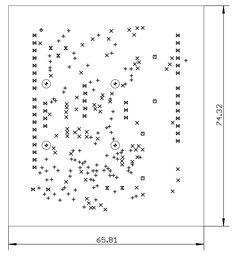
8. IMPEDANCE:
   A. IMPEDANCE MATCHING NOT REQUIRED

9. IF PANELIZATION SPECIFICATIONS ARE PROVIDED, THE PCBS SHALL BE DELIVERED IN PANEL FORM. HOWEVER, THESE SPECIFICATIONS MAY BE CHANGED AS REQUIRED BY THE CONTRACT MANUFACTURER TO SUPPORT VOLUME ASSEMBLY REQUIREMENTS.



LAYER DESCRIPTION	START COPPER WT	SE IMP OHMS	SE TRACE WIDTH	CPW SPACE	DIFF IMP OHMS	DIFF TRACE WIDTH/SPACE	CPW SPACE
L01 - TOP	1/2 OZ	--	.-----	-----	---	.-----/.-----	-----
L02 - BOTTOM	1/2 OZ	--	.-----	-----	---	.-----/.-----	-----

STACK-UP - INCH



LAYER-STACK
01-16
01-20

Sym	NC	Mils	MM	Qty	Plated
+	1	13	0.33	180	YES
×	2	14	0.35	73	YES
⊡	3	14	0.36	4	YES
⊕	4	31	0.79	1	YES
⊠	5	32	0.81	5	YES
⊞	6	40	1.02	46	YES
⊕	7	113	2.88	4	NOT

CYPRESS SEMICONDUCTOR
SAN JOSE, CA 95134
(408) 943-2600

PROJECT:	CY8CKIT-032 PSoC 4 AFE SHIELD
DRAWN BY:	ARH/PLTO/SSG
DATA:	FAB-LAYER
DWG NO: 610-60500-01	REV: 2.2 DATE: 20/11/17

SEE BOM | SEE BOM
NEXT ASSY | USED ON
APPLICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN METRIC WITH INCHES IN BRACKETS
.XXX ±.064 [±.005] .XX ±.13 [±.01] ANGLES ±.5°

MATERIAL 2
FINISH 7

DO NOT SCALE DRAWING

APPROVALS	DATE
DRAWN ARH/PLTO/SSG	20/11/17
ENGINEER GJL	20/11/17
CHECKER NMIT	20/11/17
QA -	-
PROJ. ENG. -	-

CYPRESS EMBEDDED IN TOMORROW
198 CHAMPION COURT
SAN JOSE, CA 95134
(408) 943-2600

TITLE: PCB FABRICATION, CY8CKIT-032 PSoC 4 AFE SHIELD

SIZE	CAGE CODE	P/N	
D	-	610-60500-01	

SCALE		SHEET	REV
1/1		1 OF 1	2.2

COMPUTER GENERATED DRAWING
DO NOT CHANGE MANUALLY