CE220762 – PSoC 6 MCU PDM to I2S Example

Objective

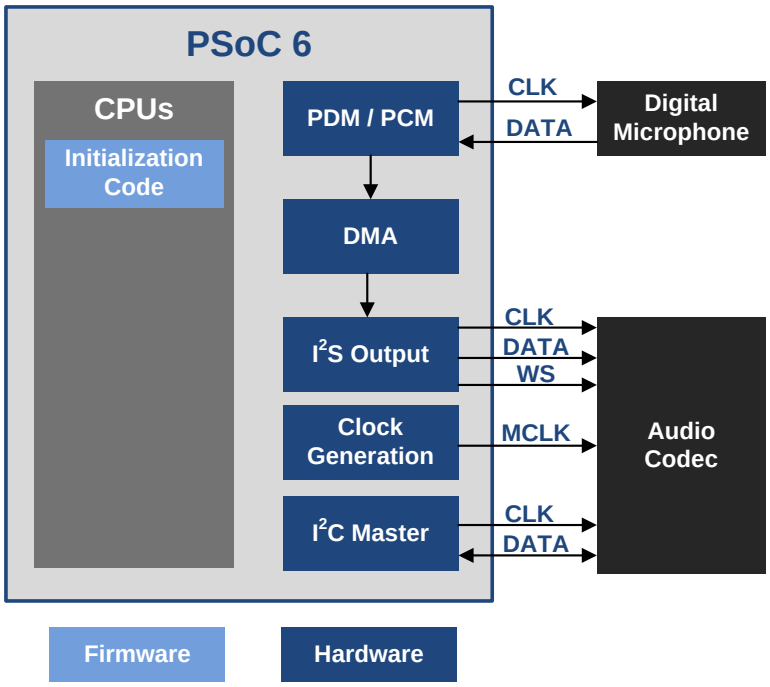
This example demonstrates how to route Pulse-Density Modulation (PDM) audio data to the Inter-IC Sound (I^2S) Interface in PSoC® 6 MCU.

Overview

This code example shows how to record a short audio sample from a microphone to SRAM, then play it on a speaker or headphone. The example uses DMA to transfer data from the PDM/PCM hardware block, which interfaces with a microphone, to SRAM. Once the recording is complete, other DMAs transfer the recorded data to the I^2S hardware block, which interfaces with an audio codec chip. This configuration frees the CPU completely, so it can execute other tasks.

Figure 1 shows the high level-block diagram of this application.

Figure 1. Block Diagram



Requirements

Tool: PSoC Creator™ 4.2

Programming Language: C (Arm® GCC 5.4-2016-q2-update)

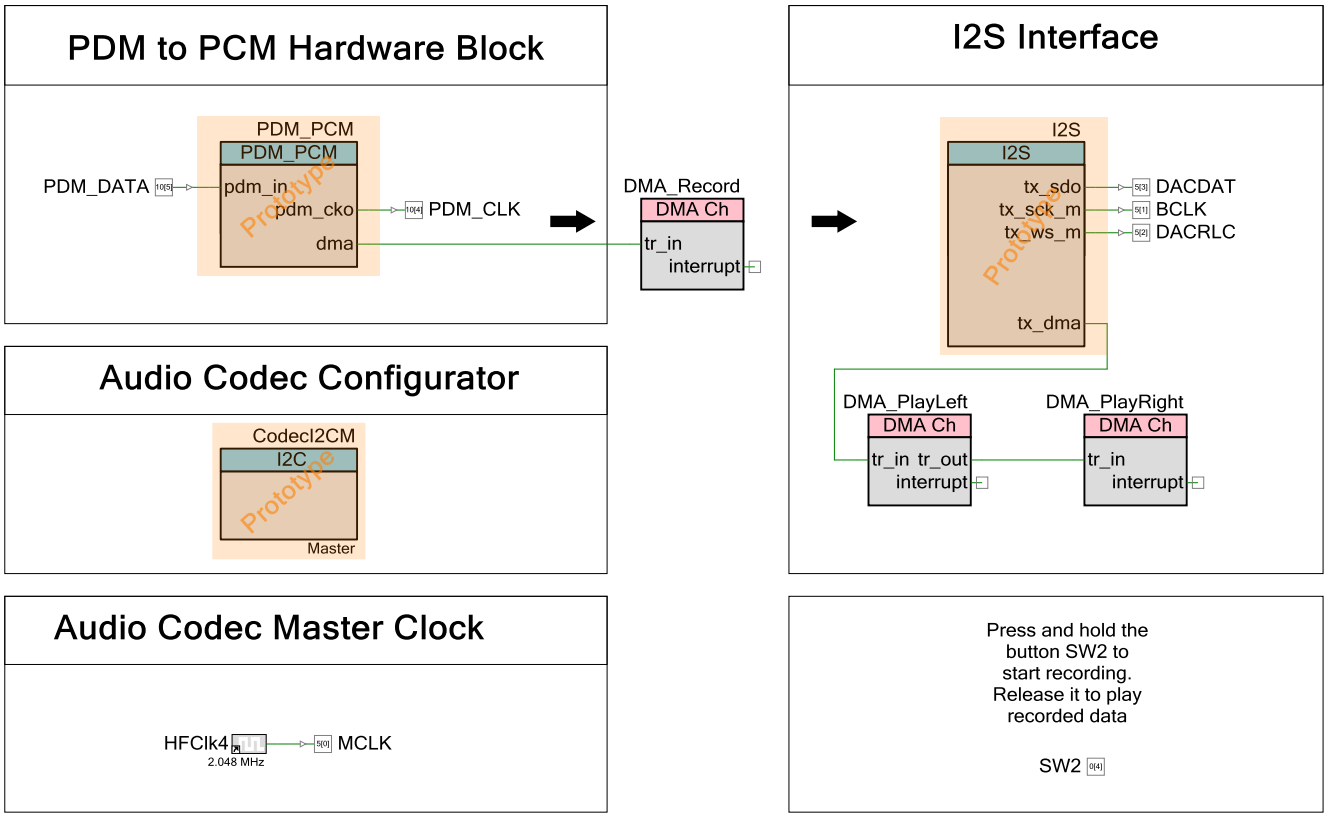
Associated Parts: All PSoC 6 MCU parts with I^2S and PDM/PCM

Related Hardware: CY8CKIT-062 or CY8CKIT-062-BLE, CY8CKIT-028-TFT

Design

Figure 2 shows the PSoC Creator schematic of this code example.

Figure 2. Project Schematics



The CY8CKIT-028-TFT shield contains the audio codec AK4954A, an audio jack and a digital microphone. This allows you to record data using the microphone and play it with the audio codec. You can connect a speaker or headphone to the audio jack.

The first stage is to record any sound coming from the microphone and place it in the SRAM of PSoC 6 MCU. This whole process can be achieved using DMA to transfer from the PDM/PCM RX buffer to an array allocated in the SRAM. Once the sound is recorded, other DMA Components move data from the SRAM to the I2S TX buffer. In this example, two DMAs are used to transfer data to the I^2S TX buffer: one for the left channel and one for the right channel. There is only one microphone in the CY8CKIT-028-TFT shield, so the same data is transferred for both channels.

To record a longer audio stream from the microphone, a sample rate of only 8 ksps is configured in both components – PDM/PCM and I2S. Both the word length of the PCM data output and the I2S TX buffer data size are set to 16 bits. The number of elements allocated for the recorded data array is 65,536, consuming a total of 128 Kbytes of SRAM.

PSoC 6 MCU also generates the clock fed to the audio codec. Based on the AK4954A datasheet, this codec requires an MCLK 256x the frame rate (256 × 8 ksps), which translates to a 2.048-MHz clock. The code example contains an I^2C Master, through which PSoC 6 MCU configures the audio codec. The code example provides an API to easily configure the AK4954A codec.

Design Considerations

This code example runs on CY8CKIT-062-BLE or CY8CKIT-062 kits, which have a PSoC 6 MCU device. To port the design to other PSoC 6 MCU devices and kits, change the target device in **Project** > **Device Selector**, and update pin assignments in the Design Wide Resources. For single-core PSoC 6 MCU devices, port the code from *main_cm4.c* to *main.c*.

Hardware Setup

This example requires the CY8CKIT-028-TFT shield to be connected to the CY8CKIT-062 (-BLE) kit.

Operation

1. Connect the CY8CKIT-028-TFT shield to the CY8CKIT-062 kit.
2. Build the “CE220762_PDM_I2S” project and program the CY8CKIT-062 kit. For more information on building projects and device programming, see PSoC Creator Help.
3. Connect a headphone or speaker to the audio jack of the CY8CKIT-028-TFT shield.
4. Press the CY8CKIT-062 SW2 button and hold it. Speak over the microphone to record a short message (up to 8 seconds).
5. Release the SW2 button and listen the recorded data with the headphone or speaker.

Components

Table 1 lists the PSoC Creator Components used in this example, as well as the hardware resources used by each.

Table 1. List of PSoC Creator Components

Component	Instance Name	Hardware Resources
I2S	I2S	I2S Block
I2C (Master)	CodecI2CM	SCB
Clock	HFClk4	High Frequency Clock
PDM/PCM	PDM_PCM	PDM/PCM Block
DMA	DMA_Record	DMA Channel
DMA	DMA_PlayLeft	DMA Channel
DMA	DMA_PlayRight	DMA Channel
Digital Output Pin	MCLK	GPIO
Digital Output Pin	TX_SDO	GPIO
Digital Output Pin	TX_SCK	GPIO
Digital Output Pin	TX_WS	GPIO
Digital Input Pin	PDM_DATA	GPIO
Digital Output Pin	PDM_CLK	GPIO
Digital Input Pin	SW2	GPIO

Parameter Settings

This section shows the changed settings for various Components as well as the system clocks.

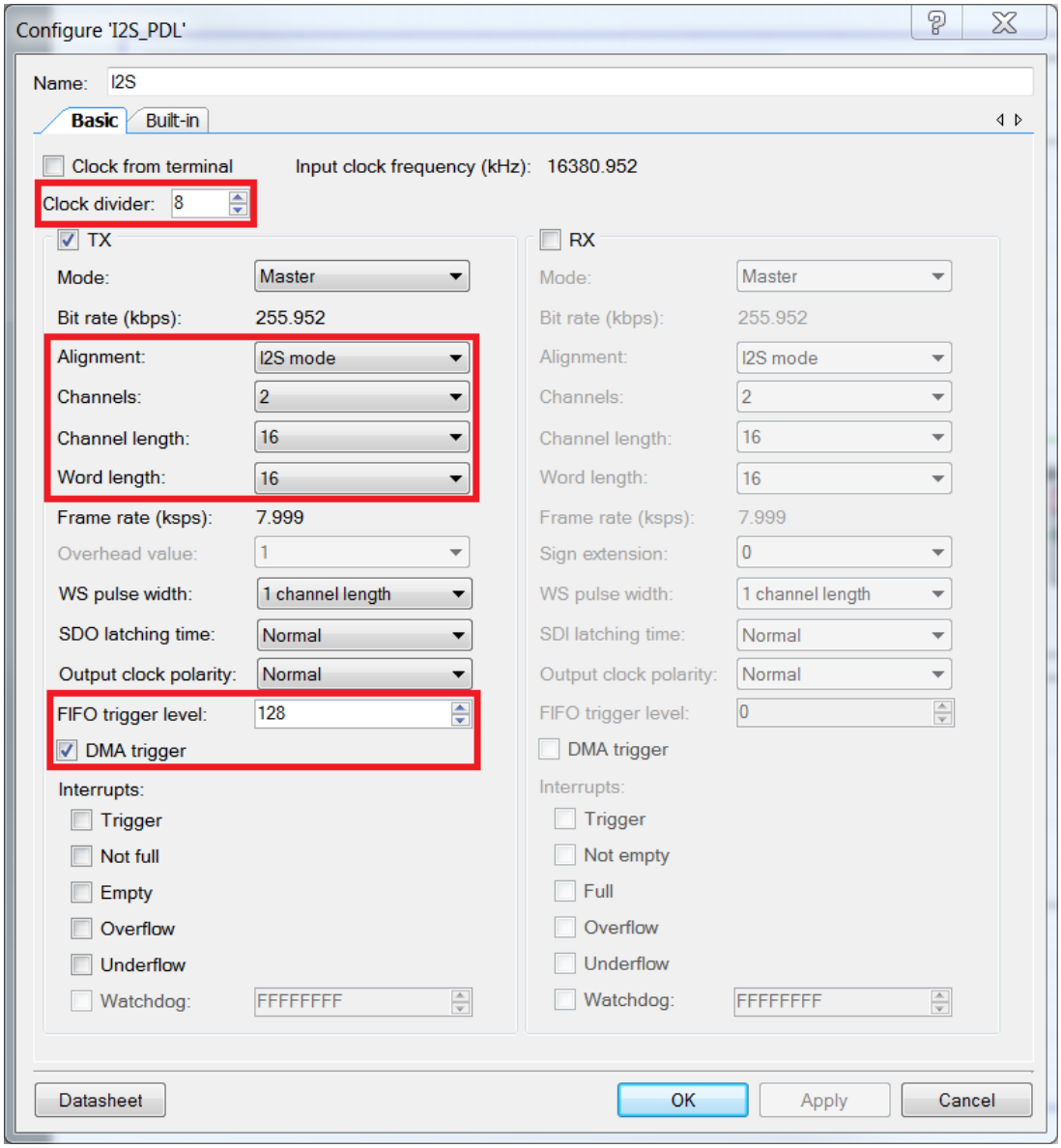
I2S

The I2S Component is configured for a frame rate of 8 ksps. Configure the HFClk1 clock to a specific frequency (see below). The Input clock frequency displayed in the Component is derived from HFClk1. The frame rate is calculated as follows:

$$Frame\ Rate\ (ksps) = \frac{HFClk1}{Clock\ divider\ \times 16 \times Channel\ Length}$$

Figure 3 shows the I2S configuration window. Note that the frame rate is not exactly 8 ksps because the PLL cannot achieve the desired output frequency of 16.384 MHz.

Figure 3. I2S Component Configuration Window



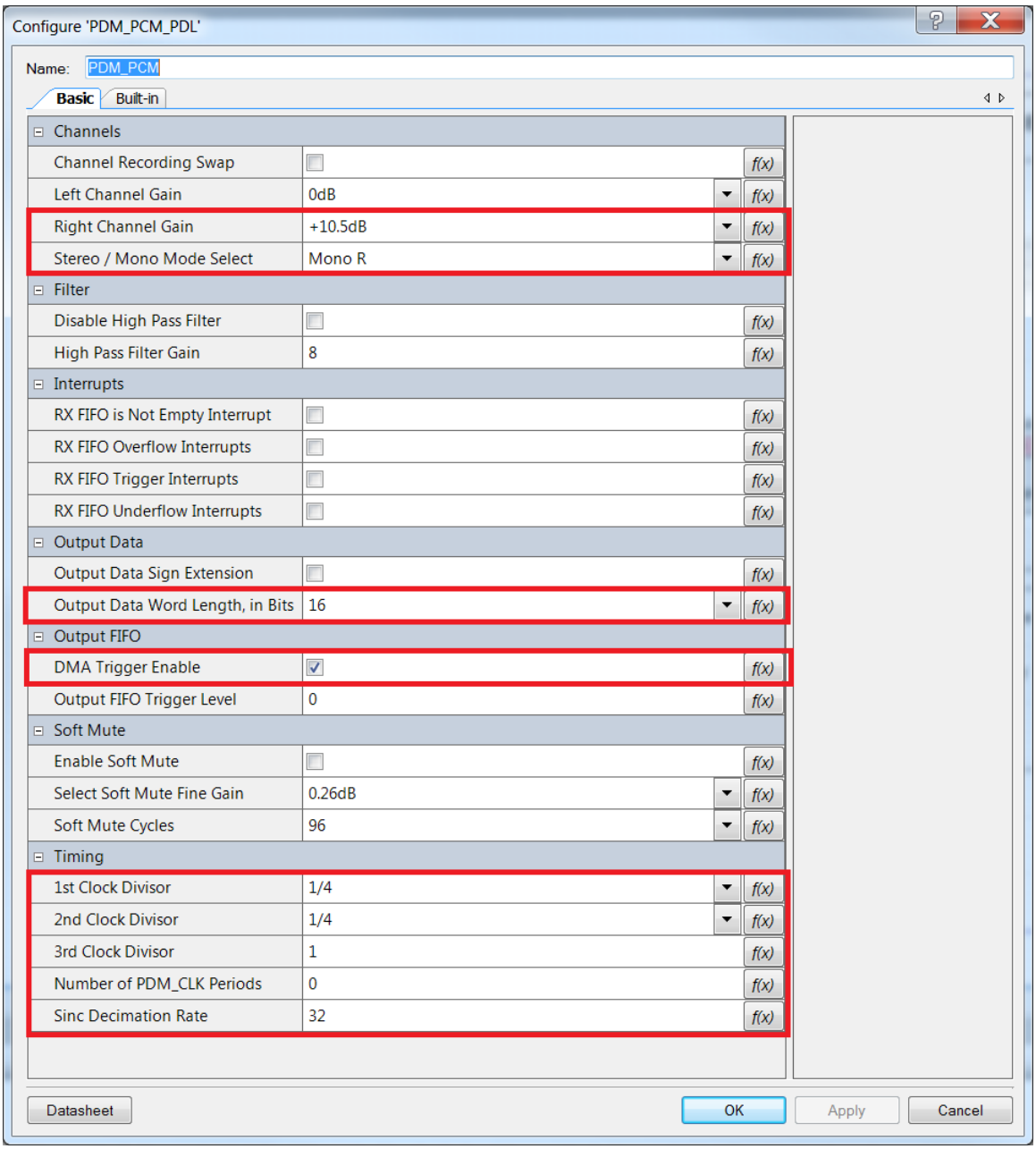
PDM_PCM

The PDM_PCM Component is configured for a frame rate of 8 ksps. The frame rate for this component is calculated as follows:

$$Frame\ Rate\ (ksps) = \frac{HFClk1}{1st\ Clock\ Divisor \times 2nd\ Clock\ Divisor \times (3rd\ Clock\ Divisor + 1) \times 2 \times Sinc\ Decimation\ Rate}$$

Figure 4 shows the configuration window.

Figure 4. PDM/PCM Component Configuration Window



HFClk4

The Component clock is configured to be 2.048 MHz, which is sourced from the PLL output and divided by 8.

SW2

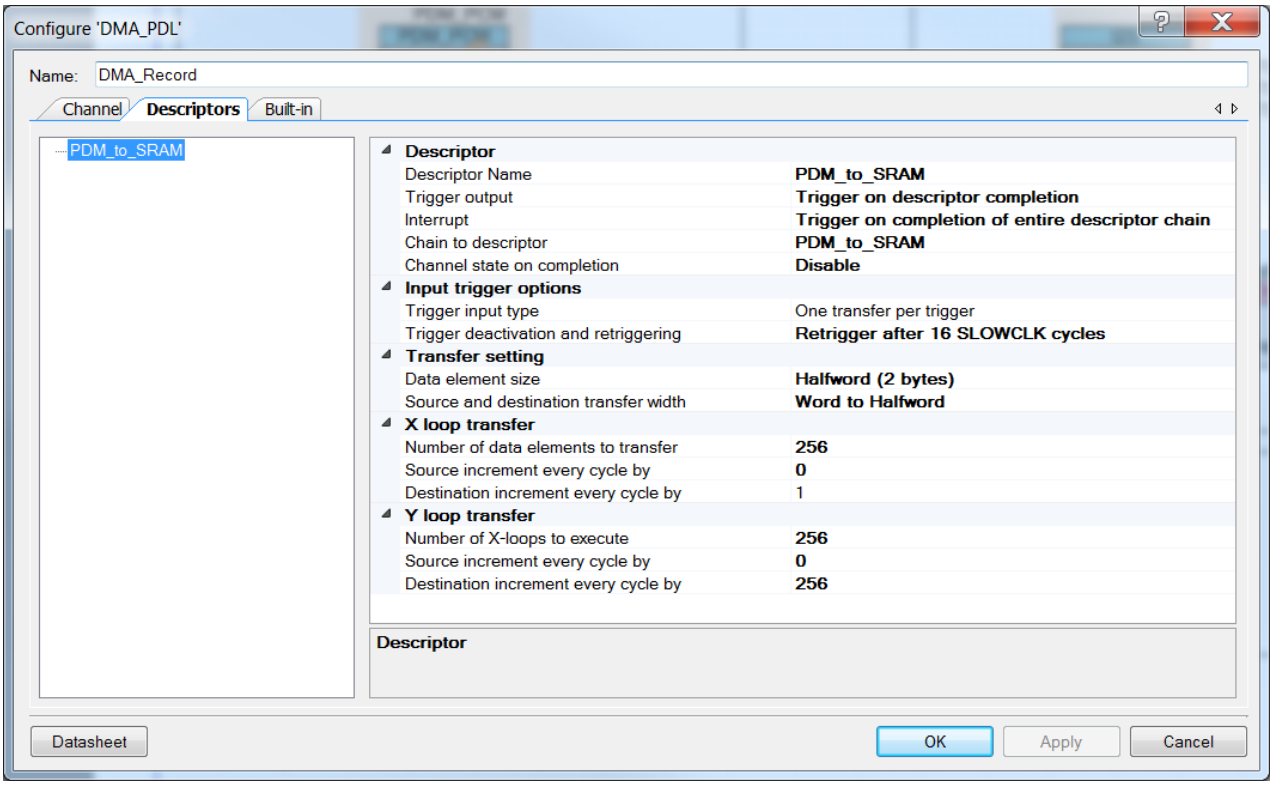
The pin drive mode is configured to be Resistive Pull Up.

DMA_Record

This DMA is configured to transfer data from the PDM RX Buffer to the recorded data array placed in SRAM. When enabled, it triggers when there is at least one element in the PDM RX Buffer.

Figure 5 shows the configuration window of this DMA.

Figure 5. DMA_Record Configuration Window



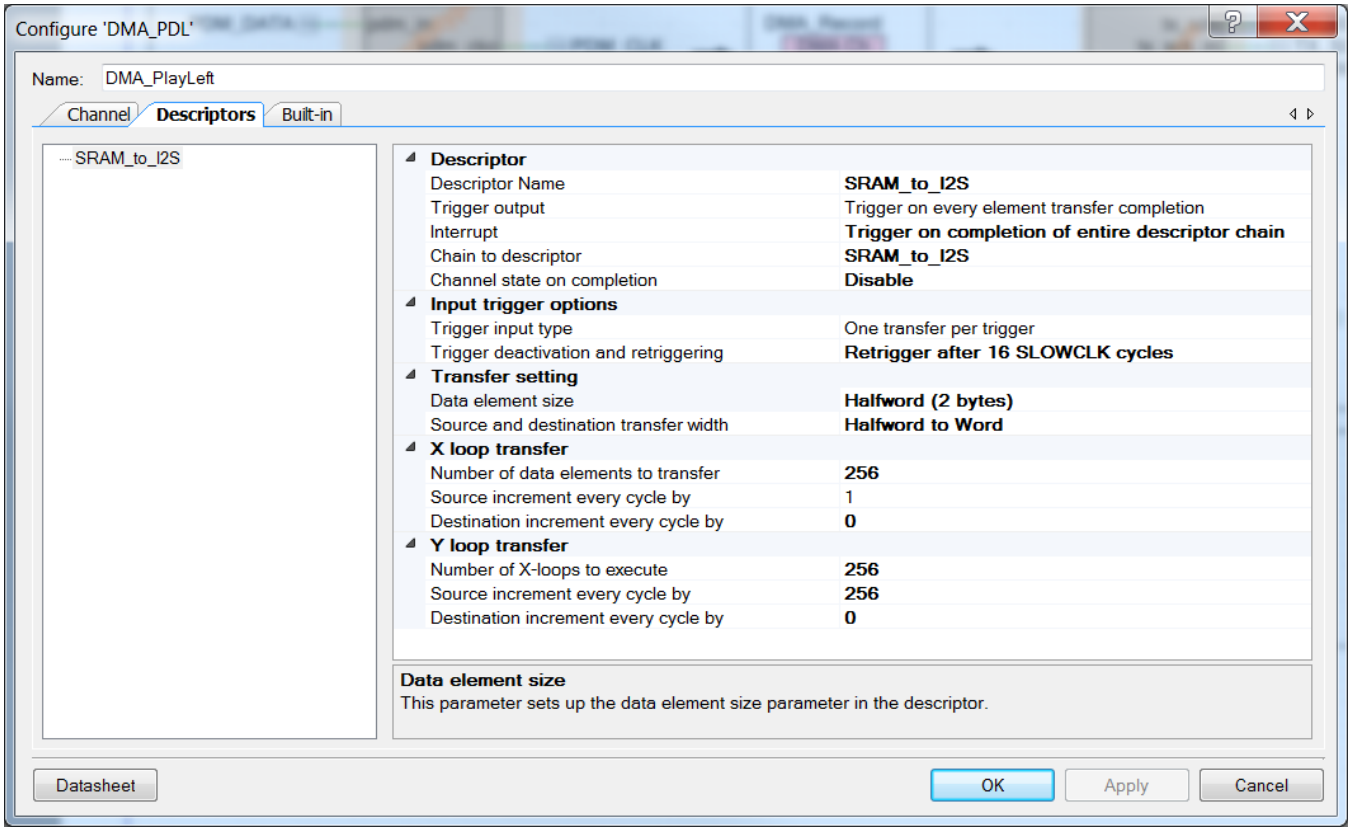
Note that the maximum number of elements to transfer in each loop is 256.

DMA_PlayRight/Left

These DMAs are configured to transfer data from the recorded data array placed in SRAM to the I2S TX Buffer. When enabled, the first DMA triggers when the I2S buffer has less than 128 elements. The second DMA is cascaded and triggers when the first completes one element transfer.

Figure 6 shows the configuration window of these DMAs (both have the same configuration).

Figure 6. DMA_PlayLeft/Right Configuration Window



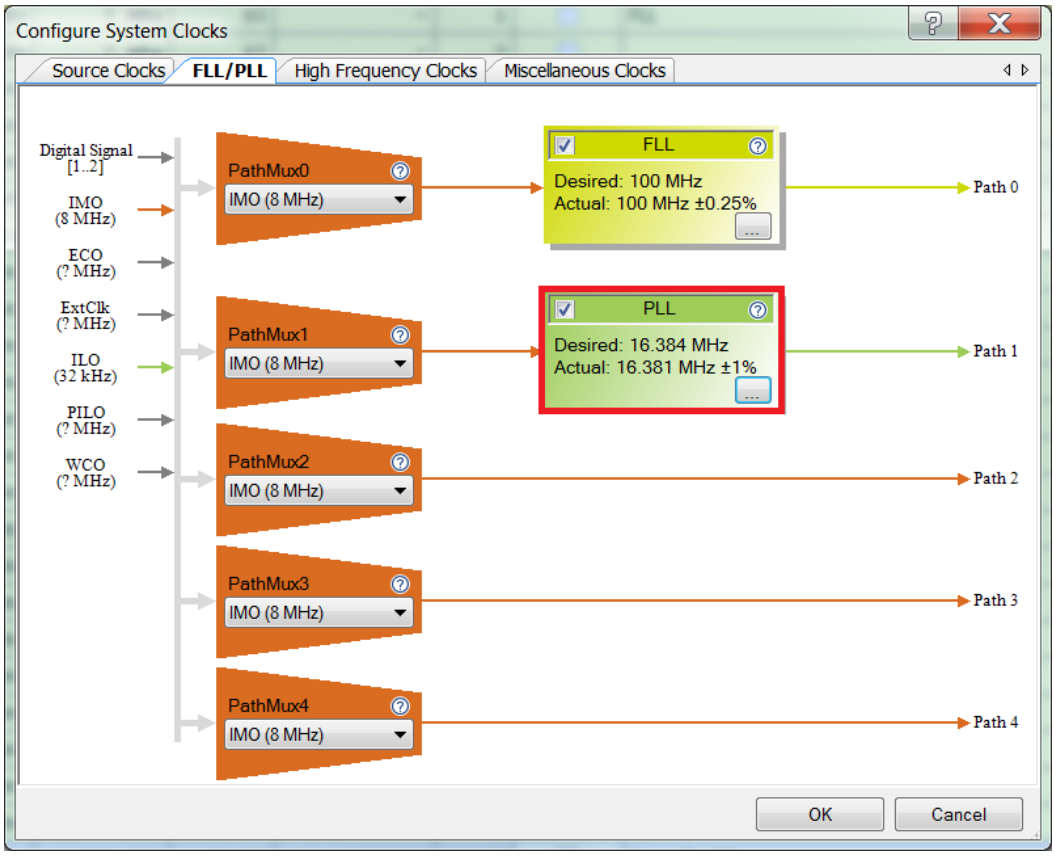
Design-Wide Resources

In the FLL/PLL tab, enable the PLL to be 16.384 MHz. This clock frequency comes from the following equation:

$$HFClk1 = Frame\ Rate \times I2S\ Clock\ divider\ \times 16 \times Channel\ Length = 8k\ \times 8 \times 16 \times 16 = 16384\ kHz$$

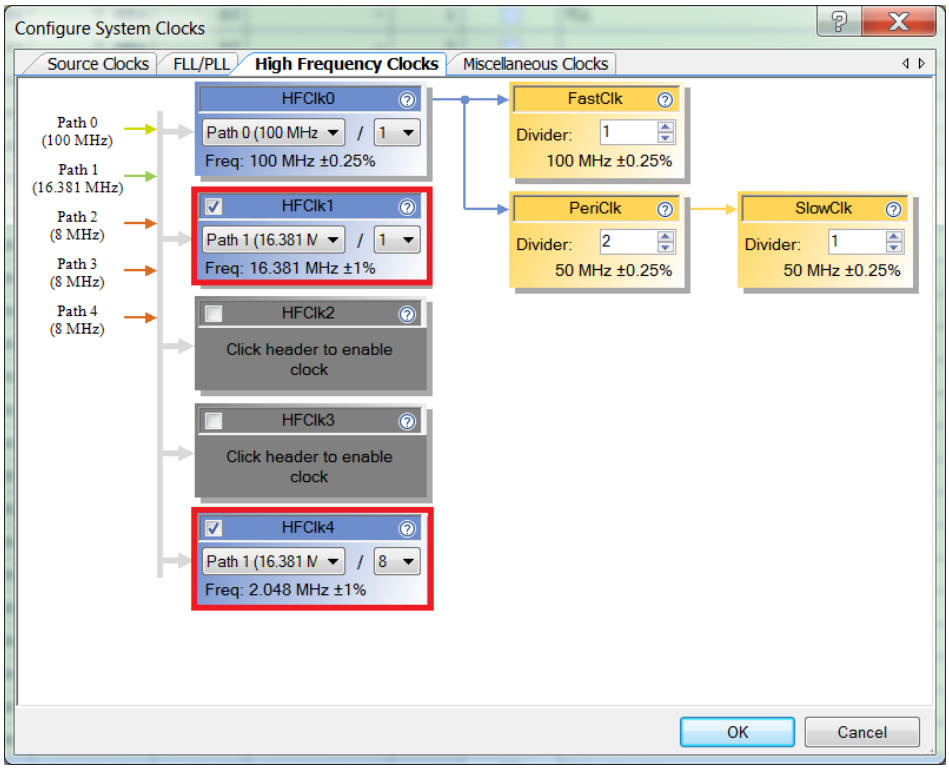
Figure 7 shows the configuration of the PLL. Note that the actual frequency is 16.381 MHz, instead of the desired frequency of 16.384 MHz.

Figure 7. Clock Configuration Window



Configure the High Frequency Clocks HFClk1 and HFClk4 to be linked to Path 1. Note that ideally both the clocks created for the I2S block (MCLK and TX_CLK) should come from the same source. Figure 8 shows how the high-frequency clocks are configured.

Figure 8. High Frequency Clock Configuration



Related Documents

Application Notes	
AN210781 – Getting Started with PSoC 6 MCU with Bluetooth Low Energy (BLE) Connectivity	Describes the PSoC 6 BLE, and how to build this code example
AN217666 – PSoC 6 MCU Interrupts	Describes how to use interrupts in PSoC 6
PSoC Creator Component Datasheets	
Inter-IC Sound Bus (I2S) Component	Sends digital audio streaming data to external I2S devices
Intra-Integrated Circuit (I2C) Component	Supports I^2C slave, master, and master-slave operation configurations.
PDM to PCM Decoder Component	Converts a PDM signal to PCM.
Direct Memory Access (DMA) Component	Transfers data to and from memory and registers.
Device Documentation	
PSoC 6 MCU: PSoC 63 with BLE Datasheet (PRELIMINARY)	
PSoC 6 MCU: PSoC 62 Datasheet	
PSoC 6 MCU: PSoC 63 with BLE Architecture Technical Reference Manual	
PSoC 6 MCU: PSoC 63 with BLE Register Technical Reference Manual	
Development Kit (DVK) Documentation	
CY8CKIT-062-BLE PSoC 6 BLE Pioneer Kit	

Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	5945171	RLOS	06/21/2017	New Code Example

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