ILO_Trim_Compensate Example Project
1.0

Features

- Fixed Function compensation for 32 kHz ILO on PSoC 4.
- Compensation accuracy to +/- 10% of target time.
- Compensated time value visible through an oscilloscope

General Description

The compensation procedure of the ILO Trim component is demonstrated in this example project. An internal Watchdog Timer is used to generate an interrupt at an interval defined by the compensated counter value. The watchdog timer is sourced from LFCLK (which is sourced from the ILO), and clears it when it reaches the desired counter value. The firmware provides the target counter value. This value is compensated by the ILO Trim component to offset the error in the ILO. The counter value is then updated periodically such that the generated interrupt occurs at an accuracy of +/-10% of the target time.

Development Kit Configuration

The following configuration instructions provide a guideline to test this design. For simplicity, the instructions describe the stepwise process to be followed when testing this design with the PSoC Development Kit (CY8CKIT-001) board.

1. Set SW3 to 3V and leave the rest of the board at default configuration. This ensures Vdda=Vddd=3V.
2. Connect the oscilloscope to P0[2].
3. Build the ILO_Trim_Compensate project and then program the hex file onto the PSoC 4 device using the MiniProg3. After programming is complete, disconnect the MiniProg3.
4. Reset the PSoC device.

Project Configuration

The top design schematic for this project is shown in Figure 1. ILO_Trim is configured in Fixed Function mode with a reference clock (Ref_Clk) of 4 MHz. A Global Signal Component is used to access the interrupt from the Watchdog Timer. This is used to trigger the interrupt component, isr_1. Pin_WT is toggled using software inside the ISR. This is configured on pin P0[2] and is connected externally by the user to an oscilloscope.

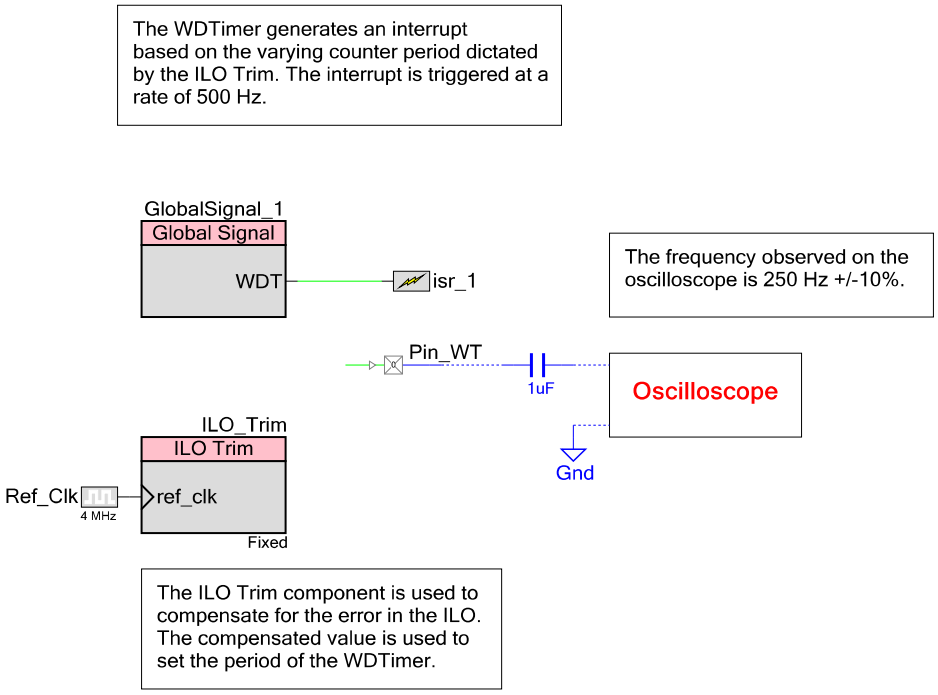

Figure 1. TopDesign Schematic

Project Description

The target time for the timer is 2ms. Since the ILO clock sourcing the timer is 32 kHz, this equates to a counter period value of 64. Therefore the timer reaches terminal count at a rate of 500 Hz. The ISR is triggered and is used to toggle Pin_WT. However due to temperature and voltage variations, the ILO frequency may drift from 32 kHz. The ILO Trim component uses the compensation procedure to correct for this drift by providing the compensated counter value.

The c code for this project goes through the following steps. The Watchdog Timer 0 is configured to generate an interrupt when the counter reaches the target counter value, and then resets. The ILO_Trim component is started and the interrupt enabled. Every 1 seconds, ILO_Trim_Compensate() API is called, and the retrieved compensated counter value is used to update the timer's target count value. The ISR is triggered at a rate of 500 Hz, and this is used to toggle Pin_WT. This pin then toggles at a rate of 250 Hz +/-10%.

Expected Results

The ILO Trim component should give compensated values with an accuracy of +/-10% of target. The signal on P0[2] should toggle at a rate of 250 Hz +/-10%.

Related Material

Application Notes

- AN80248 - PSoC® 3 / PSoC 5LP: Improving the Accuracy of Internal Oscillators