1KW LLC XDPP1100 Firmware Patch

XDPP1100 Firmware Patch

About this document

Scope and purpose

XDPP1100 is designed to operate in close-loop regulation and configurable via GUI. However, it is also possible to intentionally operate XDPP1100 in open-loop mode. This document describes a custom firmware implementation for XDPP1100 microcontroller to regulate an LLC topology in open-loop mode with a soft-startup.

Open loop LLC implemented features are listed below:

- open-loop regulation
- 3-slope PWM ramp up
- frequency sweep (described under 3-slope PWM ramp-up)
- SCP (short circuit protection) variable threshold
- SCP fault response
- Vout UV fault disable during ramp
- VIN_TRIM

Each feature is described in its respective section in this document. Moreover, we show how the user might use them.

Intended audience

Power management engineers who wish to explore open-loop LLC solution with XDPP1100.

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1 Open-loop LLC firmware

The custom open-loop LLC firmware is developed and combined into one single XDPP1100 patch. In case you are unfamiliar with XDPP1100 firmware projects, refer to “XDPP1100 Firmware Development Guide” and “XDPP1100 Firmware Examples Code”.

1.1 Patch usage

The open-loop LLC patch is delivered with a pre-built image, which the user can find in /build folder. This image can be stored to XDPP1100 RAM or OTP via GUI. Upload /src/shasta_pmbus.xlsx to GUI to use open-loop LLC features through MFR PMBus commands.

Table 1 Buck-boost MFR PMBus commands

PMBus address	PMBus command name	Read / Write	Description
(0xB7)	MFR_VIN_TRIMMING_ACTIVE	Read only	Configure the vin_pwl_slope and vin_trim in active mode. The upper two bytes defines vin_pwl_slope register. 0xB0C0, Linear11 format, convert to decimal = 0.188, it sets the vin_pwl_slope = 0.188*2^14 = 3080 The lower two bytes defines vin_trim register. 0x0000, linear 11 format, convert to decimal = 1, it sets the vin_trim = 1/0.0625 = 16
(0xB8)	MFR_VIN_TRIMMING_STANDBY	Write / Read	Configure the vin_pwl_slope and vin_trim in standby mode. The upper two bytes defines vin_pwl_slope register. 0xB0C0, Linear11 format, convert to decimal = 0.188, it sets the vin_pwl_slope = 0.188*2^14 = 3080 The lower two bytes defines vin_trim register.

(0xBA)	MFR_SCP_FAULT_RESPONSE	Write / Read	Config the SCP fault response. The fault response follows the voltage fault response. For example: 0x00 (00 000 000) = ignore 0x80 (10 000 000) = shutdown with no retry 0x88 (10 001 000) = shutdown and retry once 0x90 (10 010 000) = shutdown and retry twice 0x98 (10 011 000) = shutdown and retry 3 times 0xA0 (10 100 000) = shutdown and retry 4 times 0xA8 (10 101 000) = shutdown and retry 5 times 0xB0 (10 110 000) = shutdown and retry 6 times 0xB8 (10 111 000) = shutdown and retry continuously Set the last 3 bit to config retry delay time following the equation: delay time = 2'n. Example: (10 xxx 000) = shutdown, retry delay 2'0 = 1 ms (10 xxx 011) = shutdown, retry delay 2'3 = 8 ms 0xBB (10 111 011) = shutdown, retry continuously with 8 ms delay between each retry.
(0xBB)	MFR_STARTUP_SCP_THRESH	Write / Read	Config the SCP threshold at startup. 0x78 = 120 in decimal, the startup SCP threshold is set to 120 A.
(0xBC)	MFR_STEADY_SCP_THRESH	Write / Read	Config the SCP threshold at steady state. 0x6E = 115, the startup SCP threshold is set to 115 A.
(0xBE)	MFR_SOFTSTART_MAX_FREQUENCY	Write / Read	To set desired MAX frequency in soft start. 0x1F4 = 500D, set the Fmax to 500 kHz. Default is frequency defined by (0x33) FREQUENCY_SWITCH.
(0xBF)	MFR_SOFTSTART_IRQ_RATE_SEL	Write / Read	To set desired IRQ_RATE. [0:3] - number of CYCLES, where: 5 = every 16 Tsw 6 = every 32 Tsw 7 = every 64 Tsw [4:7] - number of COUNTS: from 1 to 15. IRQ_RATE = COUNTS * CYCLES. Refer to section 1.2.5.

(0xC0)	MFR_SOFTSTART_PWM_STEPSIZE	Write / Read	To set 3-slope PWM step size: from 0 to 15. LSB = 0.3906%. The first byte is not use, leave it “00”. The second byte “01” defines the steps size of t0-t1 The third byte “02” defines the steps size of t1-t2 The forth byte “03” defines the steps size of t2-t3
(0xC1)	MFR_SOFTSTART_CYCLE_COUNT	Write / Read	To set the number of switching cycles in each slope. LSB = 8 cycles. The first byte is not use, leave it “00”. The second byte “60” defines the switching cycles of t0-t1. The third byte “40” defines the switching cycles of t1-t2 The forth byte “20” defines the switching cycles of t2-t3 Please note the value is in HEX. i.e. 0x60 =96D

1.2 Open-loop regulation

The following diagram shows XDPP1100 modules that enable closed-loop regulation. In order to enable open-loop regulation, some modules have to be disabled, i.e. PID compensator, feed-forward compensator and flux-balancing. In addition, PWM can be forced to operate at specific values through pwm_ramp register. For example, by setting pwm.RAMP_FORCE_DUTY (format U0.8) to value ‘0x80’, it will force the PWM to operate at 50% duty cycle.

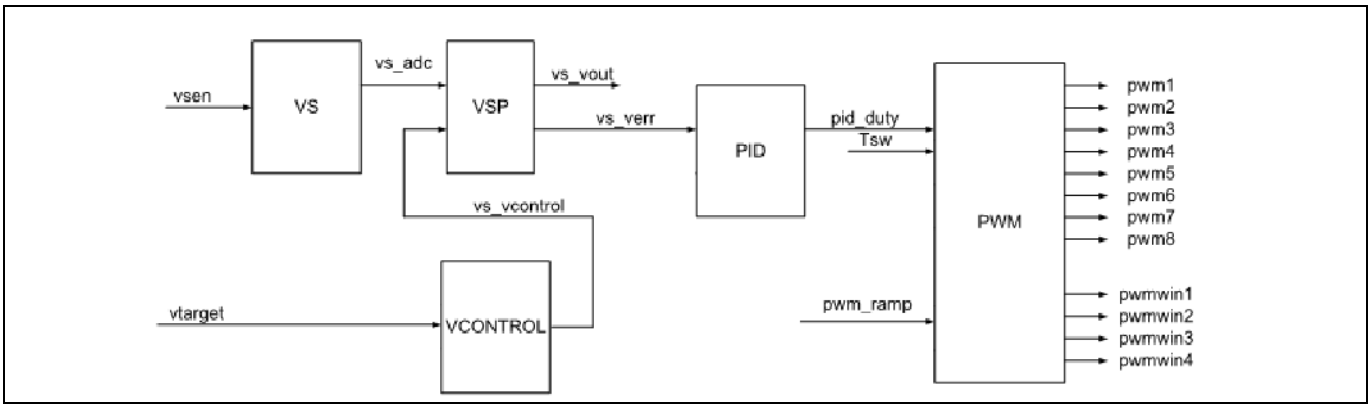

Figure 1 Voltage mode control diagram

1.2.1 Open-loop soft-startup

Open-loop soft-startup can be implemented by forcing PWM to operate from a small duty-cycle to the targeted duty-cycle. This ensures a smooth output voltage ramp-up during startup in the open-loop operation. PWM duty-cycle adjustment can be done using interrupt callback function which occurs periodically.

XDPP1100 has a possibility to execute user's code periodically for several regulation states (examples are REGULATION_STATE_TON_RISE, REGULATION_STATE_TON_DELAY, etc.) with a programmed numbers of callback cycles: from 16 to 64 cycles (8 and less is not recommended).

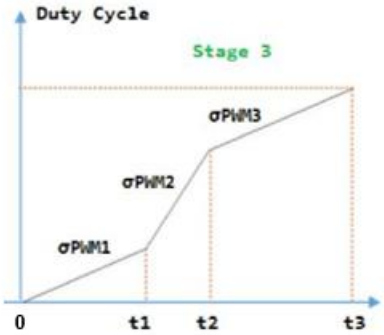

Figure 2 LLC soft start

1.2.2 Three slope startups

The three-slope open loop soft startup was designed to provide a flexibility to create various startup functions. Please, refer to the Figure 3.

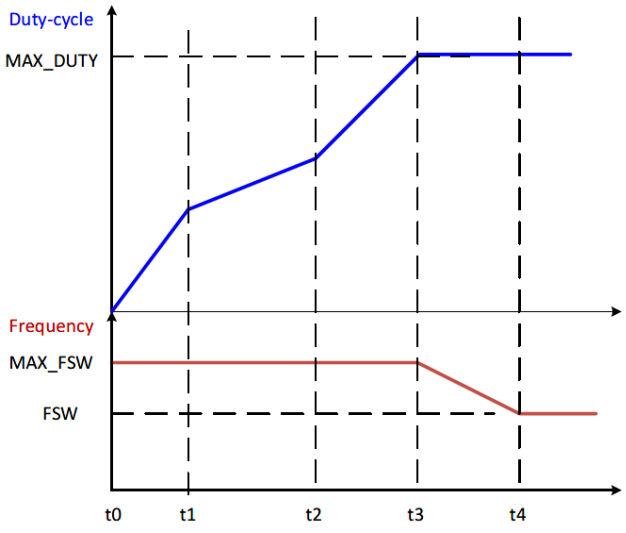

Figure 3 Three slope schema

The user is available to set his unique PWM and time actuation configuration via relevant PMBus MFR commands per Table 1. Refer to /doxy/ 3_Open_Loop_SoftStart_v1_1.xlsx for detailed configuration explanation and to perform an initial calculation.

The soft-start implementation is ramps duty-cycle at Fmax (defined by MFR_SOFTSTART_MAX_FREQUENCY) until duty-cycle equals to the MAX_DUTY, then sweeping frequency to Fsw (defined by (0x33) FREQUENCY_SWITCH).

There is modified SR turn-on sequence: switching primary PWMs (PWM1, PWM2 and PWM5) and keep SR (PWM3 and PWM4) OFF until the duty-cycle reaching to the MAX_DUTY. Once duty-cycle = max_duty, PWM3 and PWM4 are turned on. Those changed and PWMs' settings are hardcoded into the firmware.

1.2.3 Startup IRQ rate

In order to increase startup time or to set a specific IRQ rate, the user can define a desired cycle sampling with (0xBF) MFR_SOFTSTART_IRQ_RATE_SEL, which defines IRQ_RATE as CYCLES * COUNTS.

CYCLES – number of internal XDPP1100 iteration defined by present frequency switch. CYCLES can be defined as shown in Table 2.

Table 2 CYCLES definition

[0:3] bits CYCLES	XDPP internal cycles
5	16
6	32
7 or default	64

COUNTS – extended firmware number of iteration, built on top of native XDPP1100 CYCLES. COUNTS is "1" by default and can be changed by the user per [4:7] bits in MFR_SOFTSTART_IRQ_RATE_SEL. COUNTS can be from 1 to 15.

Example

0x36 means 3 counts and 6 (or 32 cycles), then IRQ_RATE = CYCLES * COUNTS = 3*32=96.
0x00 means 0 (will be changed to 1) counts and 0 (will be changed to 7 or 64 cycles), IRQ_RATE = 1*64 = 64.

1.2.4 Short circuit protection

Or SCP. The inrush current at startup is higher than the steady state current, thus the SCP threshold should set higher for startup to avoid false triggering, and reduced to a lower level when converter is in steady state.

1.2.5 Vout fault disabling

To avoid triggering unwanted faults, we disable Vout fault during startup. Once startup completes stage 3, Vout fault is enabled.

1.2.6 Input voltage trim

This feature allows to have different input voltage trim settings (vin_trim and vin_pwl_slope) for standby and active regulation modes. Input voltage trip is applied only when the input voltage is sensed at PRISEN pin and when tlm_vin_src_sel = 3 (TS ADC Vin).

Use MFR_VIN_TRIMMING_ACTIVE and MFR_VIN_TRIMMING_STANDBY commands to set desired input voltage trim settings for active and standby modes accordingly. Default value is 0.

MFR_VIN_TRIMMING_ACTIVE and MFR_VIN_TRIMMING_STANDBY are 32 bits commands each, where:

- [31:16] vin_pwl_slope in format u-2.14;
- [15:0] vin_trim in format s.6.4.

Feature example

If the user wants to use 0.15625 as the VIN slope, then its register value vin_pwl_slope (u-2.14 format) will be

$$\frac{0.15625}{2^{-14}} = 2560 \text{ or } '0xA00'$$

Now, covert gotten value into linear11 format with exponent '-10' to get '**0xB0A0**'.

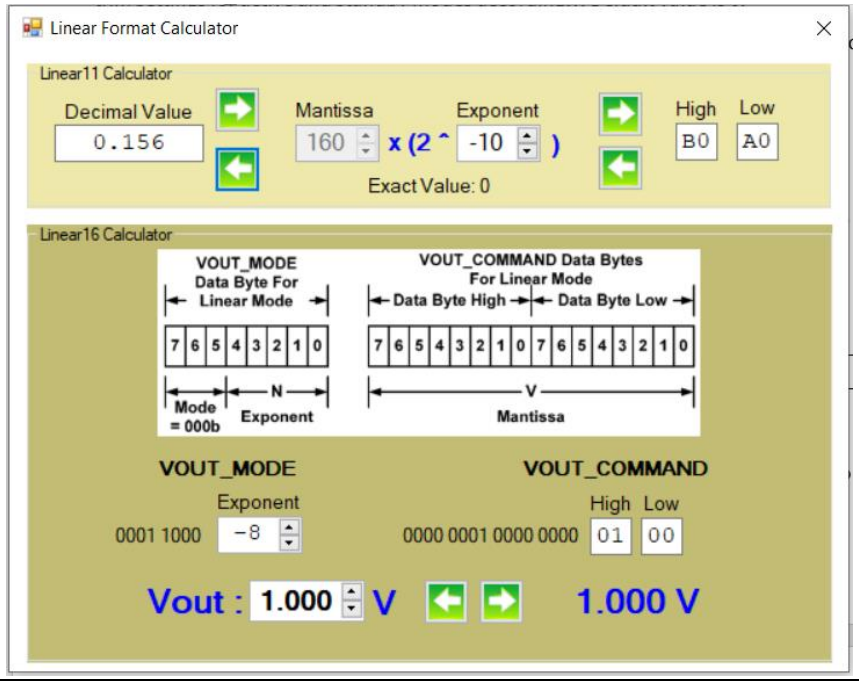

Figure 4 Linear11 calculator for 0.15625

If the user wants to use -7.875 as the VIN offset, then its register value vin_trim (s6.4 format) will be

$$\frac{-7.875}{2^{-4}} = -126 \text{ or } '0x382'$$

Now, covert gotten value into linear11 format with exponent '-4' to get '***0xE782***'.

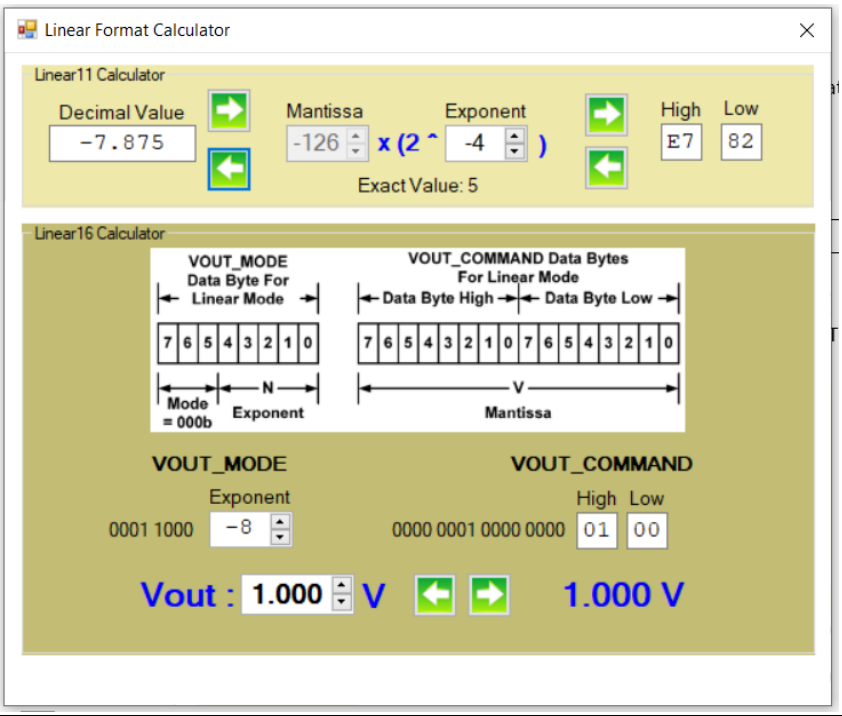

Figure 5 Linear11 calculator for -7.875

Put together gotten values into one ‘0x**B0A0***E782*’ and set it into MFR_VIN_TRIMMING_ACTIVE or MFR_VIN_TRIMMING_STANBY.

References

[1] XDPP1100 Firmware Development Guide.

[2] XDPP1100 Firmware Examples Code.

Revision history

Document version	Date	Description of changes
V1.0	13-12-2021	First version open loop llc with three slope startup

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