

## PHY for the Evaluation of Analog Defect Simulation Tools

adstestsuite@infineon.com

September 27, 2021

# Disclaimer: THIS FILE IS PROVIDED AS IS AND WITH:

- A **NO WARRANTY OF ANY KIND**, express, implied or statutory, including any implied warranties of merchantability, fitness for a particular purpose and noninfringement, which Infineon disclaims to the maximum extent permitted by applicable law; and
- B NO INDEMNIFICATION FOR INFRINGEMENT OF INTEL-LECTUAL PROPERTY RIGHTS.
- C LIMITATION OF LIABILITY: IN NO EVENT SHALL INFINEON BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES (INCLUDING LOST PROFITS OR SAVINGS) WHATSOEVER, WHETHER BASED ON CONTRACT, TORT OR ANY OTHER LEGAL THEORY, EVEN IF ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.
- © 2021 Infineon Technologies AG. All rights reserved.

#### Note:

The CMOS transistor models used, were freely available models downloaded from: http://ptm.asu.edu.

The bipolar transistor models are from: **The Development of Bipolar Log-Domain Filters in a Standard CMOS Process**, G. D. Duerden, G. W. Roberts, M. J. Deen, 2001

## **Contents**

1	Ove	rview 5
	1.1	Lane
	1.2	Pin List
	1.3	Characteristics
	1.4	Clock Source         15
2		Test Bench 16
	2.1	Tests
L	ist c	of Figures
	1	Concept overview of the phy
	2	Top level symbol of the phy
	3	Internals of a lane
	4	DLL symbol
	5	DLL schematic
	6	Test bench of the phy
L	ist c	of Tables
	1	Pin list of the phy
	2	Characteristics of the phy

## **Abstract:**

This document introduces you to the schematic and the internal circuits of the delivered phy. The purpose is to enable the reader to understand, run and extend the test benches of this circuit.

Audience: Tool evaluators



### 1 Overview

This document gives you the most important information about the 16 bit, 1/2 Gprs phy that is used to test EDA software for Analog Fault Simulation. The circuit has been implemented in an 130 nm open source technology taken from <a href="http://ptm.asu.edu/">http://ptm.asu.edu/</a>. The top level symbol of the phy is shown in figure 2. Figure 1 shows the concept of the phy. It consists out of 4 identical data lanes and one clock lane which outputs a 90° shifted output signal. The phy has a 1 Gprs and a 2 Gprs mode. Each lane includes an high speed transmitter (HSTX) and a low power transmitter (LPTX).

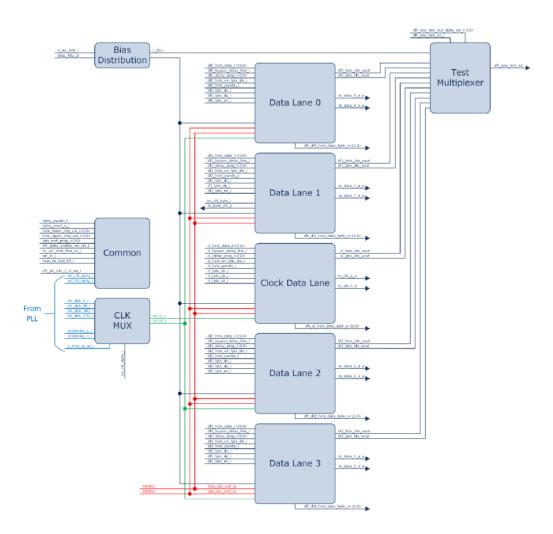


Figure 1: Concept overview of the phy.



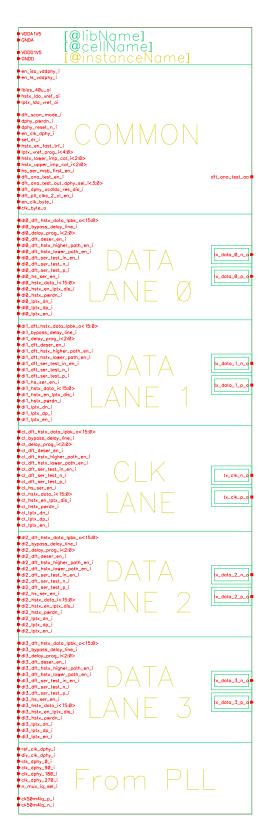


Figure 2: Top level symbol of the phy.





#### 1.1 Lane

Each lane is build up identical. Figure 3 shows the structure. It consists out of a serializer that takes the 16 bit input word and outputs a bitstream. A deserializer can be used for dft purposes to check the correctness of the serializer. A configurable delay line follows the serializer and can be used to introduce an additional delay to the lane to counter act mismatches of PCB trace lengths. The next component is a pre-driver that can be configured in two modes: normal (1 Gbps) or fast mode (2 Gbps). The four output signals of the pre-driver control the gates of an H-bridge inside of the HSTX OCD. This H-bridge is fed by the internal HSTX LDO that produces a 400 mV. In LPTX mode, the HSTX output stages are disabled, giving the LPTX drivers the possibility to drive the pad outputs to either 1.2 V or GND. The 1.2 V voltage is generated by another internal LDO.

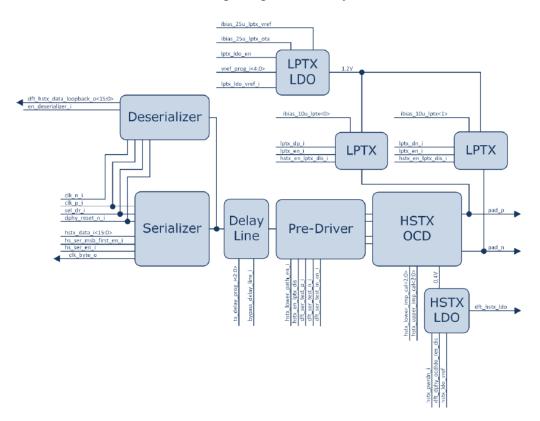


Figure 3: Internals of a lane.

#### 1.2 Pin List

The phy offers many pins. The following list shows all of them.

Public



Table 1: Pin list of the phy.

Terminal Name	Dir	Min	Тур	Max	Unit	Description
GNDA	input	О	0	О	V	Analog ground
GNDD	input	О	О	О	V	Digital ground
VDDA <sub>1</sub> V <sub>5</sub>	input	О	1.5	1.5	V	Analog supply
VDDD <sub>1</sub> V <sub>5</sub>	input	О	1.5	1.5	V	Digital supply
clk_dphy_o_i	input	О	-	1.5	V	Clock input
						from DLL
						(phase: 0°)
clk_dphy_9o_i	input	О	_	1.5	V	Clock input
						from DLL
						(phase: 90°)
clk_dphy_18o_i	input	О	_	1.5	V	Clock input
						from DLL
						(phase: 180°)
clk_dphy_270_i	input	О	_	1.5	V	Clock input
						from DLL
						(phase: 270°)
ck50m4iq_n_i	input	О	_	1.5	V	not used
ck50m4iq_p_i	input	О	-	1.5	V	not used
clk_byte_o	output	О	_	1.5	V	Output to syn-
						chronize the re-
						ceiver for de-
						sign for test
						(DfT) purposes
dft_ana_test_ao	output	О	_	1.5	V	Output of Ana-
						log DfT Test-
16.						mux
dft_ana_test_en_i	input	О	_	1.5	V	
dft_ana_test_out	input	О	_	1.5	V	
_dphy_sel_i<3:0>					<b>T</b> 7	
dft_dphy_ocdldo	input	О	_	1.5	V	
_res_dis_i					<b>T</b> 7	
dft_pll_clks_2_cl	input	О	_	1.5	V	
_en_i					<b>X</b> 7	
dft_scan_mode_i	input	О	_	1.5	V	
div_clk_dphy_i	input	О	_	1.5	V	



Terminal Name   Dir   Min   Typ   Max   Unit   Description							
cl_bypass_delay_line_i		0	ТУР		V	If 1 then by-	
ci_by pass_delay_lifle_i	niput		_	1.5	·	pass the delay	
						line	
al delay progrission	innut			4 -	V	Delay setting	
cl_delay_prog_i<2:0>	input	0	-	1.5		Enable the	
cl_dft_deser_en_i	input	0	_	1.5	V	deserializer for	
cl_dft_hstx_data	autaut			<b>4</b> -	V	DfT purposes	
	output	0	_	1.5	v	Output of the deserializer for	
_lpbk_o<15:0>							
al dft bety bigher	innut			<b>4</b> -	V	DfT purposes Enable the	
cl_dft_hstx_higher	input	О	_	1.5	v		
_path_en_i						HSTX pull up transistors	
al dft baty larger	innut			<b>4</b> -	V	Enable the	
cl_dft_hstx_lower _path_en_i	input	О	_	1.5	v	HSTX pull	
_paur_en_r						down transis-	
						tors	
al dft car tast in an i	innut			4 -	V	tors	
cl_dft_ser_test_in_en_i	-	0	_	1.5	V		
cl_dft_ser_test_n_i	input	0	_	1.5	V		
cl_dft_ser_test_p_i	input	0	_	1.5	V		
cl_hs_ser_en_i	input	0	_	1.5	V		
cl_hstx_data_i<15:0>	input	0	_	1.5	V		
cl_hstx_en_lptx_dis_i	input	0	_	1.5	V		
cl_hstx_pwrdn_i	input	0	_	1.5	V	Input to the	
cl_lptx_dn_i	input	0	_	1.5	V	Input to the pull down tran-	
						sistors of the	
						LPTX driver	
al late da i	innut				17		
cl_lptx_dp_i	input	0	_	1.5	V	Input to the	
						pull up tran-	
						sistors of the	
-1 1( :		_			<b>3</b> 7	LPTX driver	
cl_lptx_en_i	input	0	_	1.5	V	Enable/Disable	
						the LPTX	
11 1 1 1					<b>T</b> 7	driver	
dlo_bypass_delay_line	ınput	О	_	1.5	V	All lanes have	
_i						the same sig-	
						nals	





dlo_dft_deser_en_i dlo_dft_hstx_data _lpbk_o<15:0>	input input output	0 0 0	Typ - -	<b>Max</b> 1.5	Unit V	Description
dlo_dft_deser_en_i dlo_dft_hstx_data _lpbk_o<15:0>	input output	O	_		v	
dlo_dft_hstx_data _lpbk_o<15:0>	output			1.5	V	
_lpbk_o<15:0>			_	1.5	V	
		O		1.5	•	
dlo_dft_hstx_higher	input	O	_	1 -	V	
_path_en_i	niput	U	_	1.5	v	
dlo_dft_hstx_lower	innut	0		4 F	V	
_path_en_i	input	О	_	1.5	v	
_patit_eft_1 dlo_dft_ser_test_in	innut	0		4 F	V	
_en_i	input	О	_	1.5	v	
	innut	0		4 F	V	
dlo_dft_ser_test_n_i	input	0	_	1.5	V	
dlo_dft_ser_test_p_i	input	0	_	1.5		
dlo_hs_ser_en_i	input	0	_	1.5	V	
dlo_hstx_data_i<15:0>	input	0	-	1.5	V	
dlo_hstx_en_lptx	input	O	_	1.5	V	
_dis_i					<b>3</b> 7	
dlo_hstx_pwrdn_i	input	0	_	1.5	V	
dlo_lptx_dn_i	input	0	_	1.5	V	
dlo_lptx_dp_i	input	0	_	1.5	V	
dlo_lptx_en_i	input	О	_	1.5	V	
dl1_bypass_delay_line	input	О	_	1.5	V	
_i					* 7	
dl1_delay_prog_i<2:0>	input	О	_	1.5	V	
dl1_dft_deser_en_i	input	О	_	1.5	V	
dl1_dft_hstx_data	output	О	_	1.5	V	
_lpbk_o<15:0>						
dl1_dft_hstx_higher	input	O	_	1.5	V	
_path_en_i						
dl1_dft_hstx_lower	input	O	_	1.5	V	
_path_en_i						
dl1_dft_ser_test_in	input	O	_	1.5	V	
_en_i						
dl1_dft_ser_test_n_i	input	O	-	1.5	V	
dl1_dft_ser_test_p_i	input	O	-	1.5	V	
dl1_hs_ser_en_i	input	O	-	1.5	V	
dl1_hstx_data_i<15:0>	input	O	-	1.5	V	
dl1_hstx_en_lptx	input	O	-	1.5	V	
_dis_i						





Terminal Name	Dir	Min	Тур	Max	Unit	Description
dl1_hstx_pwrdn_i	input	0	-JP -	1.5	V	
dl1_lptx_dn_i	input	0	_	1.5	V	
dl1_lptx_dp_i	input	0	_	1.5	V	
dl1_lptx_en_i	input	0	_	1.5	V	
dl2_bypass_delay_line	input	0	_	1.5	V	
_ i _ jı j_	1					
dl2_delay_prog_i<2:0>	input	0	_	1.5	V	
dl2_dft_deser_en_i	input	О	_	1.5	V	
dl2_dft_hstx_data	output	О	_	1.5	V	
_lpbk_o<15:0>	1					
dl2_dft_hstx_higher	input	О	_	1.5	V	
_path_en_i	-					
dl2_dft_hstx_lower	input	0	_	1.5	V	
_path_en_i						
dl2_dft_ser_test_in	input	О	_	1.5	V	
_en_i						
dl2_dft_ser_test_n_i	input	О	_	1.5	V	
dl2_dft_ser_test_p_i	input	О	_	1.5	V	
dl2_hs_ser_en_i	input	О	_	1.5	V	
dl2_hstx_data_i<15:0>	input	О	_	1.5	V	
dl2_hstx_en_lptx	input	О	_	1.5	V	
_dis_i						
dl2_hstx_pwrdn_i	input	О	_	1.5	V	
dl2_lptx_dn_i	input	О	_	1.5	V	
dl2_lptx_dp_i	input	О	_	1.5	V	
dl2_lptx_en_i	input	О	_	1.5	V	
dl3_bypass_delay_line	input	О	_	1.5	V	
_i						
dl3_delay_prog_i<2:0>	input	О	_	1.5	V	
dl3_dft_deser_en_i	input	О	_	1.5	V	
dl3_dft_hstx_data	output	О	_	1.5	V	
_lpbk_o<15:0>						
dl3_dft_hstx_higher	input	О	_	1.5	V	
_path_en_i						
dl3_dft_hstx_lower	input	0	_	1.5	V	
_path_en_i						
dl3_dft_ser_test_in	input	0	_	1.5	V	
_en_i						ed on nevt page





Terminal Name   Dir   Min   Typ   Max   Unit   Description							
			Тур			Description	
dl3_dft_ser_test_n_i	input	О	_	1.5	V		
dl3_dft_ser_test_p_i	input	О	_	1.5	V		
dl3_hs_ser_en_i	input	О	_	1.5	V		
dl3_hstx_data_i<15:0>	input	О	_	1.5	V		
dl3_hstx_en_lptx	input	О	_	1.5	V		
_dis_i							
dl3_hstx_pwrdn_i	input	О	_	1.5	V		
dl3_lptx_dn_i	input	О	_	1.5	V		
dl3_lptx_dp_i	input	О	_	1.5	V		
dl3_lptx_en_i	input	0	-	1.5	V		
dphy_pwrdn_i	input	О	_	1.5	V		
dphy_reset_n_i	input	О	_	1.5	V		
en_clk_byte_i	input	О	_	1.5	V		
en_clk_dphy_i	input	О	_	1.5	V		
en_iso_vddphy_i	input	О	_	1.5	V		
en_ls_vddphy_i	input	О	_	1.5	V		
hs_ser_msb_first_en_i	input	О	_	1.5	V		
hstx_en_fast_trf_i	input	О	_	1.5	V		
hstx_ldo_vref_ai	input	О	0.4	0.6	V		
hstx_lower_imp_cal	input	О	_	1.5	V		
_i<2:0>							
hstx_upper_imp_cal	input	О	_	1.5	V		
_i<2:0>	-						
ibias_4ou_ai	input	О	40	40	μΑ		
lptx_ldo_vref_ai	input	О	0.6	1	V		
lptx_vref_prog_i<4:o>	input	О	_	1.5	V		
n_mux_iq_sel_i	input	О	_	1.5	V		
ref_clk_dphy_i	input	О	_	1.5	V		
sel_dr_i	input	О	_	1.5	V	Select 1 Gbps	
	1					or 2 Gbps	
						mode	
tx_clk_n_o	output	О	_	1.2	V	N-Output of	
	I					clock lane	
tx_clk_p_o	output	О	_	1.2	V	P-Output of	
rr	F					clock lane	
tx_data_o_n_o	output	o	_	1.2	V	N-Output of	
	2 and ac				•	data lane o	
					l Combine	ed on next page	



## 1 OVERVIEW



Continued from previous page

Terminal Name	Dir	Min	Typ	Max	Unit	Description	1
tx_data_o_p_o	output	0	-	1.2	V	P-Output	of
						data lane o	
tx_data_1_n_o	output	О	_	1.2	V	N-Output	of
						data lane 1	
tx_data_1_p_o	output	О	_	1.2	V	P-Output	of
						data lane 1	
tx_data_2_n_o	output	О	_	1.2	V	N-Output	of
						data lane 2	
tx_data_2_p_o	output	О	_	1.2	V	P-Output	of
						data lane 2	
tx_data_3_n_o	output	О	_	1.2	V	N-Output	of
						data lane 3	
tx_data_3_p_o	output	О	_	1.2	V	P-Output	of
						data lane 3	



## 1.3 Characteristics

Table  ${\color{red} 2}$  shows the typical electrical characteristics of the phy.

Table 2: Characteristics of the phy.

Symbol	Min	Тур	Max	Unit	Description
Number of lanes		5			Number of lanes
Bit width of one lane		16			Bit width of one lane
$f_{\text{PLL,out}} = f_{\text{DLL,in}}$	-	200	-	MHz	Output frequency of the
					PLL and input frequency
					of the DLL
$f_{\rm DLL,out}$	_	1	_	GHz	Output frequency of the
					four phase clock generated
					by the DLL



### 1.4 Clock Source

The phy is powered by a DLL that generates the for phase clock from the output of a PLL. The DLL is shown in figure 4 and 5. The output frequency of the DLL is a four phase 1 GHz signal.

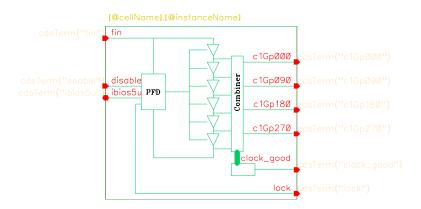


Figure 4: DLL symbol.

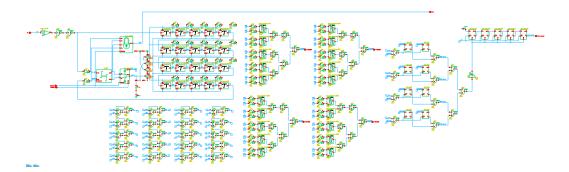


Figure 5: DLL schematic.



### 2 The Test Bench

The test bench consists out of the device under test (DUT) in the middle and the it is surrounded by the test program, see figure 6. Additionally, it includes a bandgap and bias circuit that produces the  $40\,\mu\text{A}$  bias current and the required  $600\,\text{mV}$  and  $400\,\text{mV}$  reference voltages. Furthermore, the test bench offers multiple measurement and stimuli blocks that have been implemented with Verilog-A or in schematic which should not be part of the fault injection.

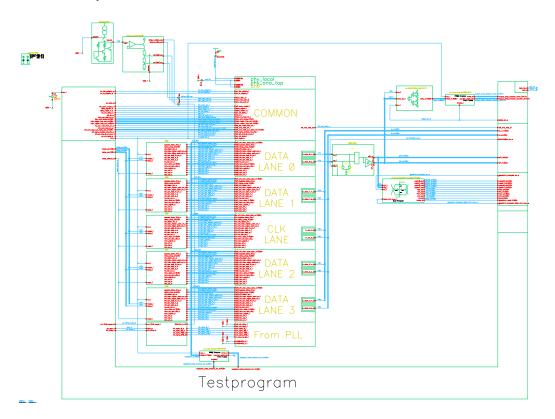


Figure 6: Test bench of the phy.

#### 2.1 Tests

The following tests are performed sequentially:

- Ramp up: Enable the phy and wait till the internal LDOs settle.
- LDO checks: Test all HSTX LDOs and LPTX LDOs via the analog DfT bus.



- LPTX checks: Check the voltage levels and timing of the LPTX output stages.
- DC checks: Measure the output voltage levels for various loads (impedance measurement).
- Delay line checks: Go through all delay line settings and check the introduced delay.
- HSTX PRBS check: Finally, input a PRBS-9 bitstream to the input and check the received output words.

If one test fails, the simulation is stopped and an error is indicated by the test\_id signal.