LDO for the Evaluation of Analog Defect Simulation Tools

adstestsuite@infineon.com

December 16, 2020

Note:
The CMOS transistor models used, were freely available models downloaded from: http://ptm.asu.edu.
The bipolar transistor models are from: **The Development of Bipolar Log-Domain Filters in a Standard CMOS Process**, G. D. Duerden, G. W. Roberts, M. J. Deen, 2001

Contents

List of Figures

List of Tables

Abstract:

This document introduces you to the schematic and the internal circuits of the delivered LDO. The purpose is to enable the reader to understand, run and extend the test benches of this circuit.

Audience: Tool evaluators

1 Overview

This document gives you the most important information about the chopped LDO that is used to test EDA software for Analog Fault Simulation. The circuit has been implemented in an 130 nm open source technology taken from . The top-level symbol of the LDO is shown in figure 1.

Figure 1: Symbol of the top-level LDO.

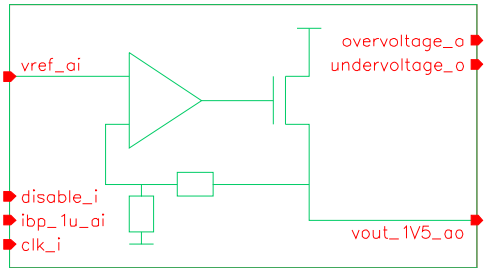


Table 1 shows the description of all pins.

Table 1: The pin list of the LDO.

Pin name	Direction	Min	Typ	Max	Unit	Description
vref_ai	input		1.2		V	Reference voltage
ibp_1u_ai	input		1		µA	Bias current
clk_i	input	0		VDDA	V	400 kHz input clock
vout_1V5_ao	output		1.5		V	Output
disable_i	input		0		V	If high, disable
undervoltage_o	output	0	0	VDDA	V	High if VDDA is lower than 2.3 V
overvoltage_o	output	0	0	VDDA	V	High if VDDA is higher than 2.8 V

2 Electrical Characteristics

Table 2 shows the typical electrical characteristics of the LDO.

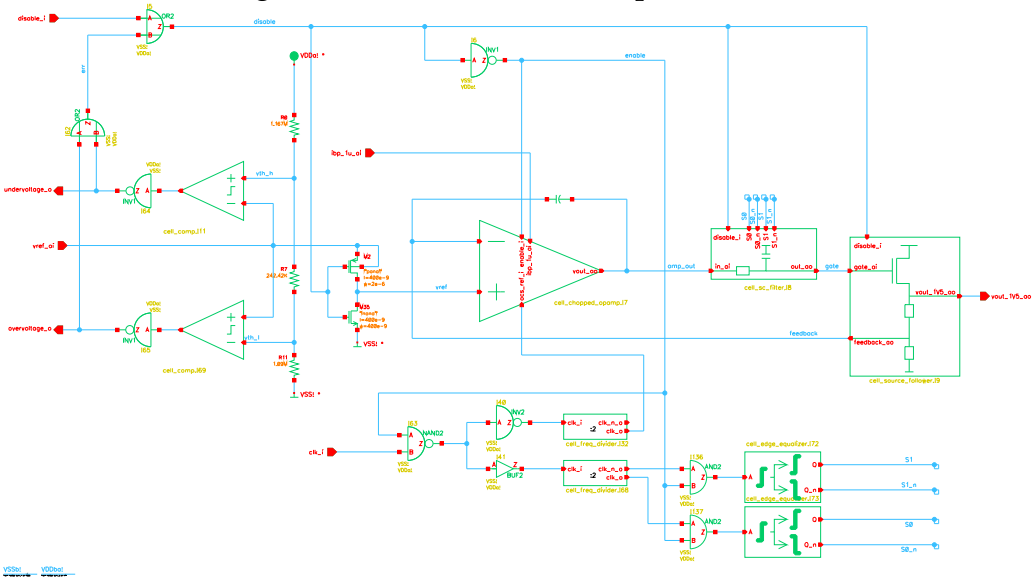
Table 2: Electrical characteristics of the LDO.

Symbol	Min	Typ	Max	Unit	Description
VDDA	-	2.5	-	V	Supply voltage for the analog core
f	-	400	-	kHz	Clock frequency
Vrefp	-	1.2	-	V	Bandgap reference voltage
Iout	0	-	25	mA	Output current

3 LDO Core

The LDO schematic is shown in figure 2. On the left side, you will find the over and under voltage detection, which monitors the supply voltage V_{DDA} and triggers if the supply is increased above or decreased below a certain threshold. In the middle of the schematic, the chopped opamp can be seen. It requires a clock and an input bias current as input. A capacitor in the feedback path makes the opamp behave like an integrator. The output of the opamp is connected to a switched capacitor (SC) filter. The clocks driving the chopping of the opamp and the SC-filter have a phase shift of 90°. The output of the SC-filter is connected to the source follower that drives the output. The output voltage is divided down so that for a 1.5 V output voltage the feedback signal is equal to the 1.2 V bandgap reference. On the bottom of the schematic, you will find the clock generation circuit. It provides the 90° phase shift signals and aligns the rising and falling edges for the switched capacitor filter.

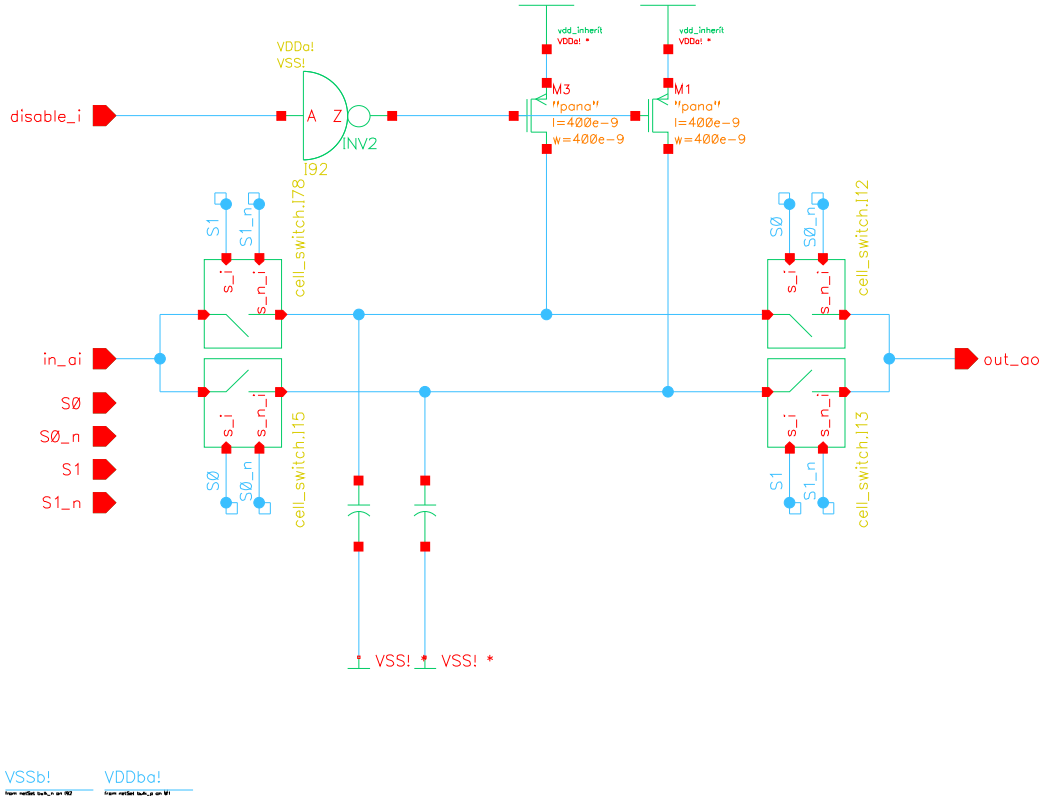
Figure 2: Schematic of the top level LDO.



4 Switched Capacitor Filter

The switched capacitor filter is built with two capacitors and can be seen in figure 3. The provided clocks must be non-overlapping.

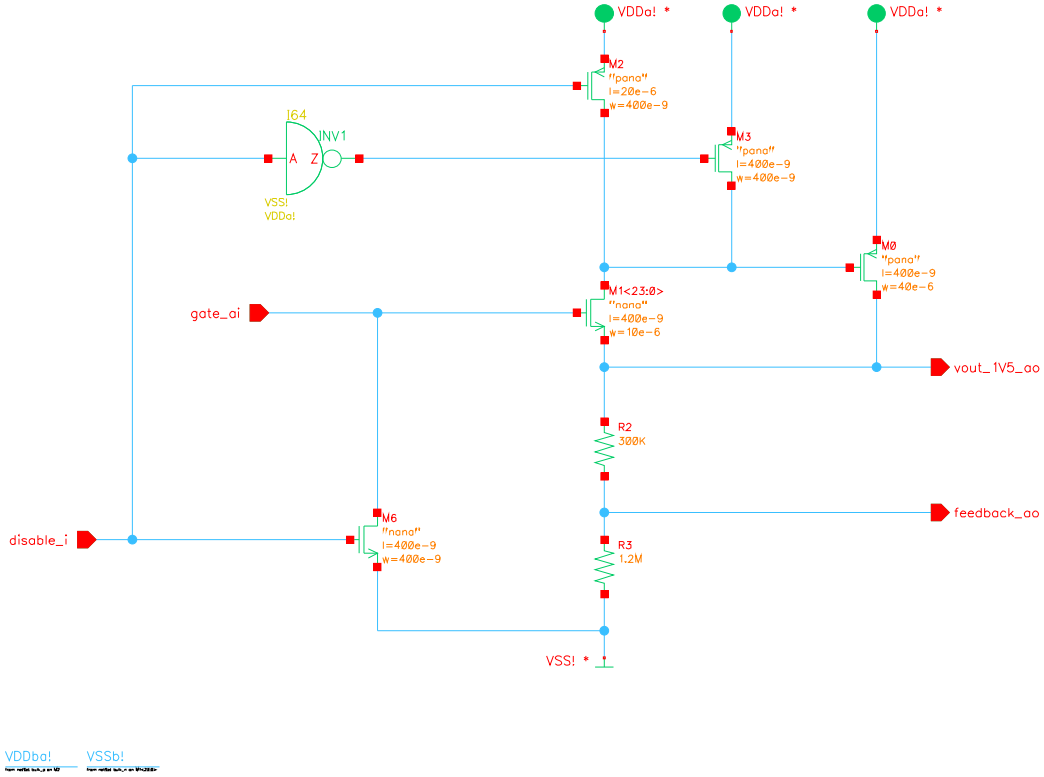
Figure 3: Schematic of the switched capacitor filter.



5 Source Follower

The output of the SC-filter is connected to a source follower that is supported by the transistor M_0 in figure 4. The transistor M_2 acts as a resistor so that the voltage drop across it turns on transistor M_0. Transistor M_3 and M_6 will turn off this structure. The resistors R2 and R3 divide the 1.5 V output to the bandgap voltage of 1.2 V.

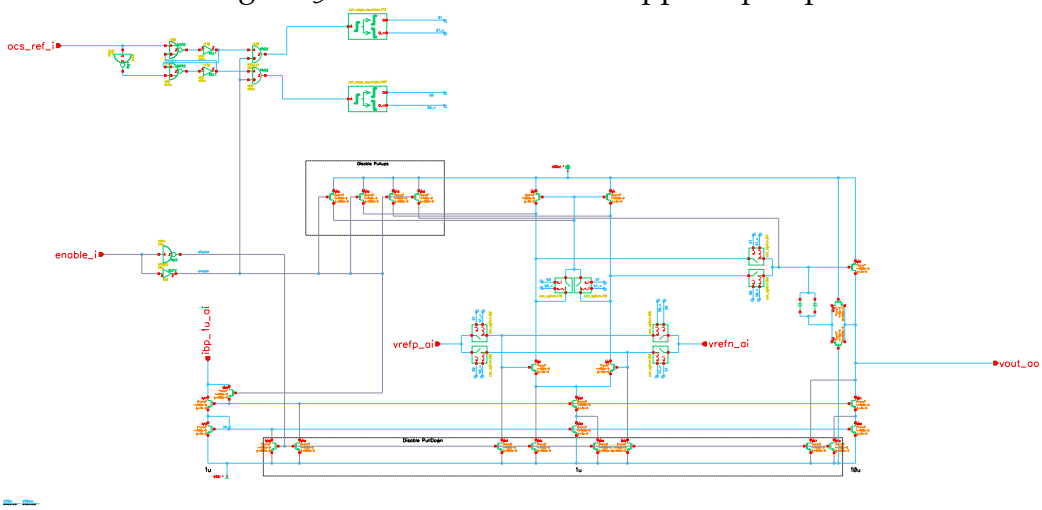
Figure 4: Schematic of the source follower.



6 Chopped Opamp

Figure 5 shows the chopped opamp. It is a miller opamp with chopped inputs and a chopped current mirror load. In the upper left corner you find the clock generation circuit that makes sure that the rising and falling edges of the two phases are properly aligned.

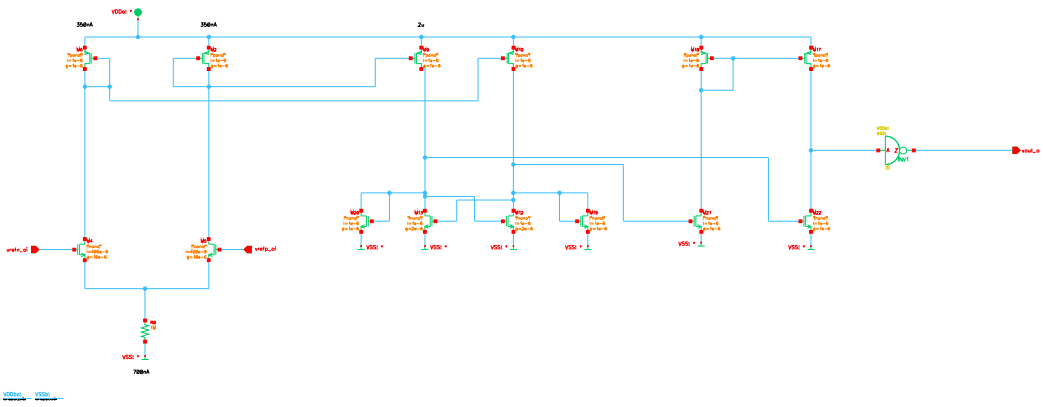
Figure 5: Schematic of the chopped opamp.



7 Over/Under Voltage Comparator

The over and under voltage comparators detect whether the supply voltage is higher or lower than a specific threshold. The implementation of one comparator can be seen in figure 6.

Figure 6: Schematic of the under voltage and overvoltage comparator.



The transfer curve is shown in figure 7. It shows a hysteresis of about 47.5 mV.

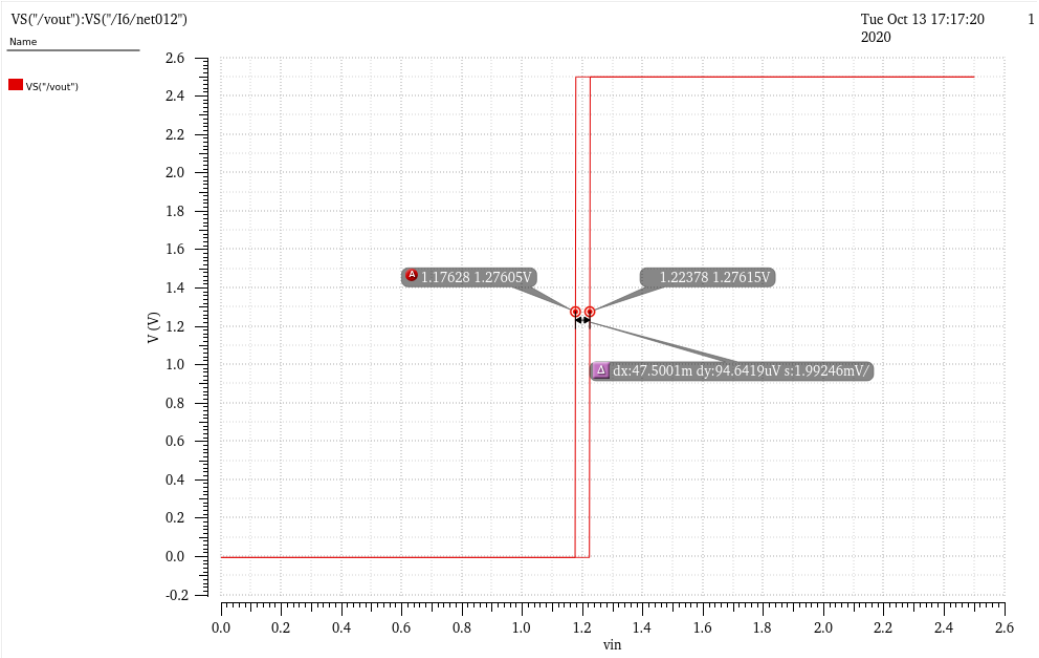


Figure 7: Transfer curve of the over/under voltage comparator.

If we sweep the power supply, we see the transfer curve of figure 8. Because the comparator creates very steep slopes, convergence issues might arise for DC and transient simulations.

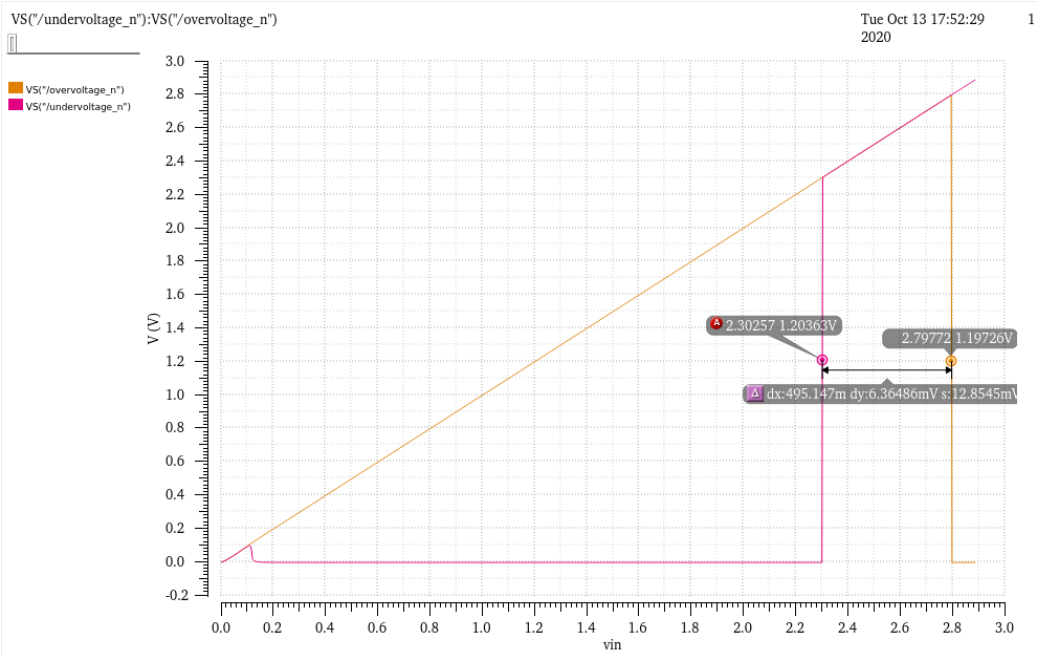


Figure 8: Transfer curve of over/under voltage detector when sweeping the power supply.

8 LDO Test

The test sequence is as follows:

1. Bootup
2. Undervoltage
3. Overvoltage
4. VDDA step down (in spec)
5. VDDA step up (in spec)
6. Disable
7. Vref step down
8. Vref step up
9. +5 mA step at the output (25 mA)
10. -5 mA step at the output (15 mA)

After each stimuli change the output voltage is probed and checked against the expected value. The simulation, as it can be seen in figure 9, shows the stability of the LDO under nominal conditions.

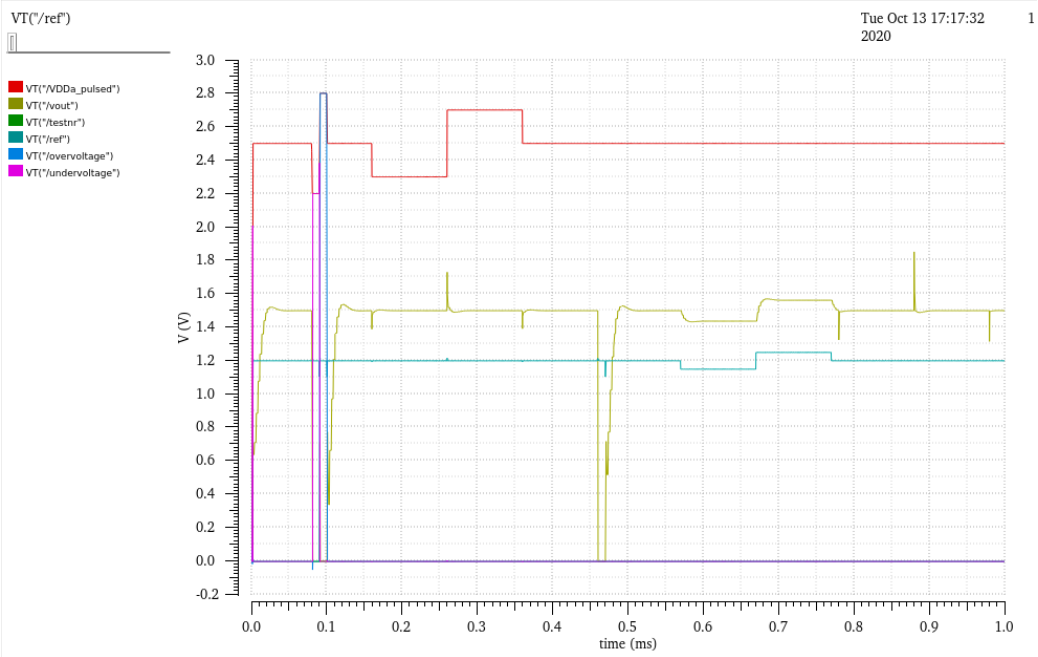


Figure 9: LDO test sequence.

9 Test IDs

The following test ids are output when an error occures:

Table 3: Test IDs of the LDO.

Test ID	Description
7	Output voltage in disabled state is violated
8	Output voltage is not within the expected limits
9	Output voltage has not settled
10	Under/over voltage has been triggered

The test id is 0 if everything is within the specification.