11 bit SAR ADC for the Evaluation of Analog Defect Simulation Tools

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Note:
The CMOS transistor models used, were freely available models downloaded from: http://ptm.asu.edu.
The bipolar transistor models are from: **The Development of Bipolar Log-Domain Filters in a Standard CMOS Process**, G. D. Duerden, G. W. Roberts, M. J. Deen, 2001

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Abstract:

This document introduces you to the schematic and the internal circuits of the delivered 11 bit SAR ADC. The purpose is to enable the reader to understand, run and extend the test benches of this circuit.

Audience: Tool evaluators

1 Overview

This document gives you the most important information about the 11 bit redundant SAR ADC that is used to test EDA software for Analog Fault Simulation. The circuit has been implemented in an 130 nm open source technology taken from http://ptm.asu.edu/. The top-level symbol of the SAR ADC is shown in figure 1.

Figure 1: Symbol of the top-level SAR ADC.

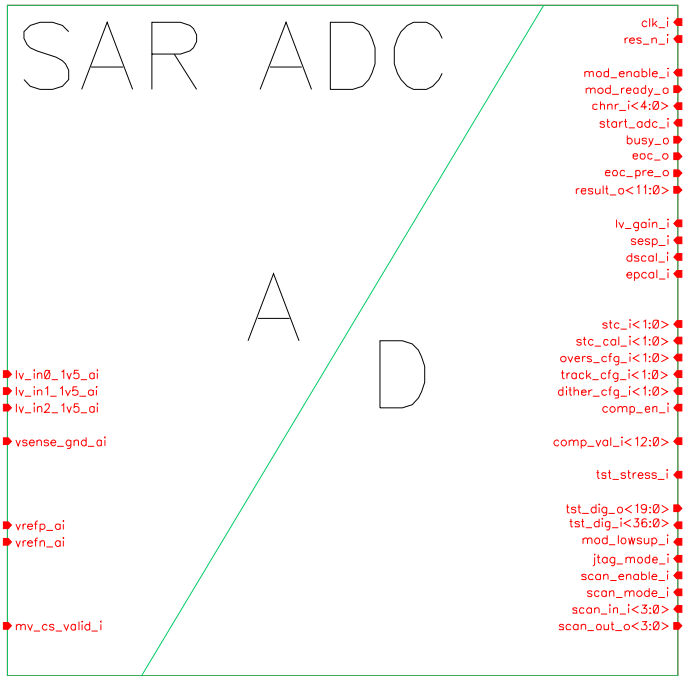

Table 1 shows the description of all pins.

Table 1: Pin list of the top-level SAR ADC.

Pin name	Direction	Min	Typ	Max	Unit	Description
vsense_gnd_ai	input	-	0	-	V	No internal connection
vrefp_ai	input		1.2		V	Bandgap reference voltage
vrefn_ai	input		0		V	Negative reference voltage

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Pin name	Direction	Min	Typ	Max	Unit	Description
tst_stress_i	input		0		V	Test mode stress: switches on all input switches and power module
track_cfg_i<1:0>	input		0,0		V	Tracking mode configuration
stc_i<1:0>	input		0,0		V	Sample time control
stc_cal_i<1:0>	input		0,0		V	Sample time control for calibration
start_adc_i	input	0		VDDC	V	Enable the ADC
sesp_i	input		0		V	Spreaded early sample point enable
scan_mode_i	input		0		V	Scan mode select signal
scan_in_i<3:0>	input		0,0,0		V	scan input to scan chains
res_n_i	input	0		VDDC	V	Reset of the ADC (must be VDD to enable ADC)
overs_cfg_i<1:0>	input		0,0		V	Oversampling configuration
mod_enable_i	input		VDDC		V	Module enable
lv_in2_1v5_ai	input	0	-	1.5	V	Input channel 2 (Max code is reachted at V_{refp})
lv_in1_1v5_ai	input	0	-	1.5	V	Input channel 1 (Max code is reachted at V_{refp})

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Pin name	Direction	Min	Typ	Max	Unit	Description
lv_ino_1v5_ai	input	0	-	1.5	V	Input channel 0 (Max code is reachted at V_{refp})
lv_gain_i	input		0		V	Low voltage gain selection
jtag_mode_i	input		0		V	JTAG MODE enable
epcal_i	input		0		V	Enable post-calibration
dscal_i	input		VDDC		V	Disable startup calibration
dither_cfg_i<1:0>	input		0,0		V	Dither configuration
comp_val_i<12:0>	input		0...0		V	Comparator value - redundant code
comp_en_i	input		0		V	Comparator mode enable
clk_i	input	0		VDDC	V	Input clock
chnr_i<4:0>	input	0		VDDC	V	Channel number: 0: 0b01001 1: 0b01010 2: 0b01011
tst_dig_0<19:0>	output	0		VDDC	V	Test digital output bits
scan_out_0<3:0>	output	0		VDDC	V	Scan output from scan chains

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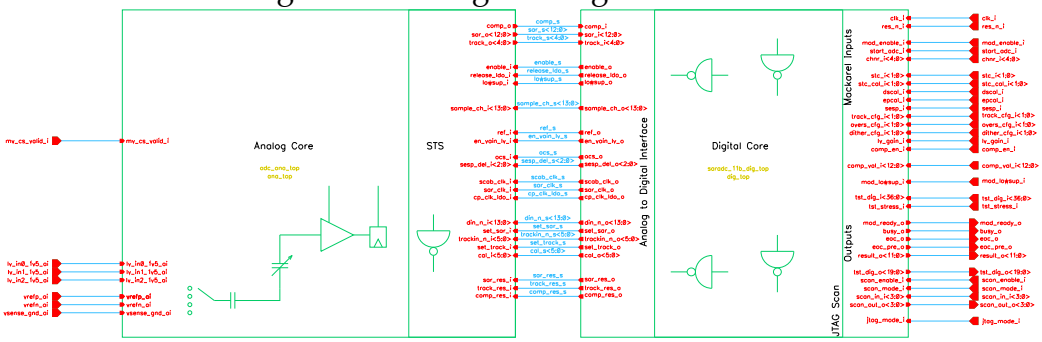
Pin name	Direction	Min	Typ	Max	Unit	Description
result_o<11:0>	output	0		VDDC	V	Result of A/D conversion (result_o<0> is not used! The 11 bit binary result is starting from result_o<1> and end at result_o<11>).
mod_ready_o	output	0		VDDC	V	Module ready signal
eoc_pre_o	output	0		VDDC	V	End of conversion pre-timed advanced eoc_o pulse
eoc_o	output	0		VDDC	V	End of conversion signal pulse flags end of conversion
busy_o	output	0		VDDC	V	Busy signal (high indicates running conversion/operation)
mv_cs_valid_i	input	0	VDDA	VDDA	V	Core supply valid - if high, all level shifters are released - if low, all level shifters are in isolation mode
scan_enable_i	input		0		V	Scan enable path
tst_dig_i<36:0>	input		0...0		V	Test mode digital input bits
mod_lowsup_i	input	0	VDDC	VDDC	V	Not implemented

Note:

- The 11 bit output of the result can be found in `result_o<11:1>`. The signal `result_o<0>` is inactive.
- Code ob11111111111 is reachted at $V_{\text{in}} = V_{\text{refp}} = 1.2\,\text{V}$

The digital SystemVerilog block is located in the first hierarchy as shown in figure 2. The right block has to be linked to the SystemVerilog module.

Figure 2: Analog and digital modules.



2 Electrical Characteristics

Table 2 shows the typical electrical characteristics of the ADC.

Table 2: Electrical characteristics of the SAR ADC.

Symbol	Min	Typ	Max	Unit	Description
VDDA	-	2.5	-	V	Supply voltage for the analog core
VDDC	-	1.5	-	V	Supply voltage for the digital core
f	-	28	-	MHz	Clock frequency
Vrefp	-	1.2	-	V	Bandgap reference voltage

3 Startup and Conversion

To start the ADC the following steps have to be done:

1. res_n_i = VDDC
2. Apply clock to clk_i
3. Wait for mod_ready_o signal from ADC
4. Start conversion by applying a pulse to start_adc_i (start_adc_i has to be high during a rising edge of clk_i)
5. Wait for eoc_o going high (then the result will be available on result_o)

Figure 3 shows the startup routine and figure 4 shows a zoom to one conversion.

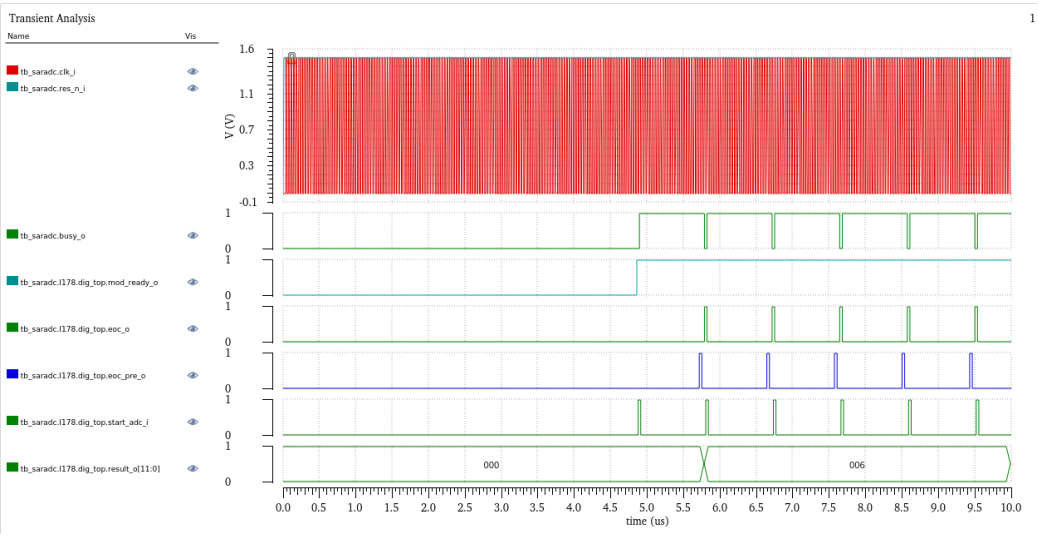


Figure 3: Startup of ADC.

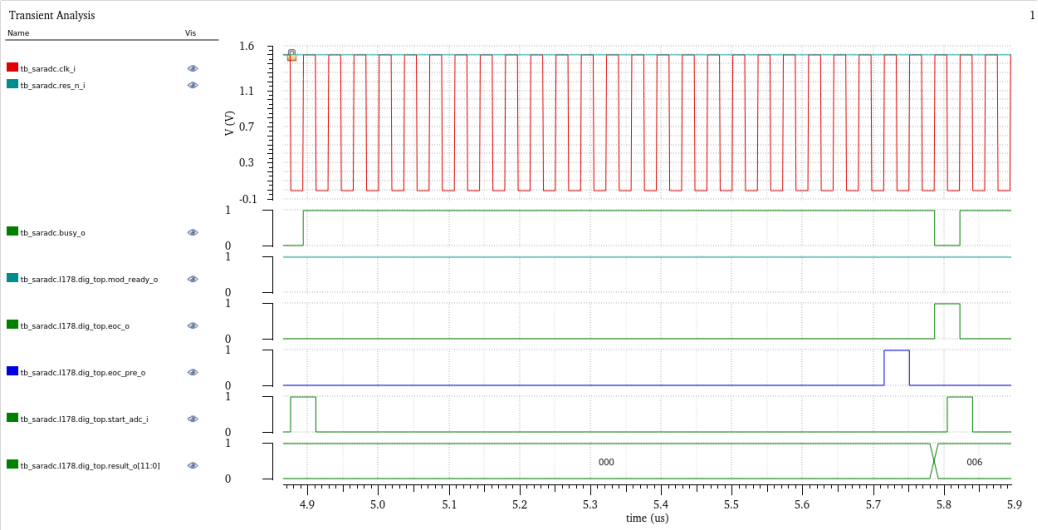


Figure 4: Zoom at single conversion.

The mod_ready_o signal signalizes the readiness of the analog circuitry and it is set after 4.85 µs for a 28 MHz clock. One conversion takes 25 clock cycles. With an input clock of 28 MHz one conversion takes about 900 ns.

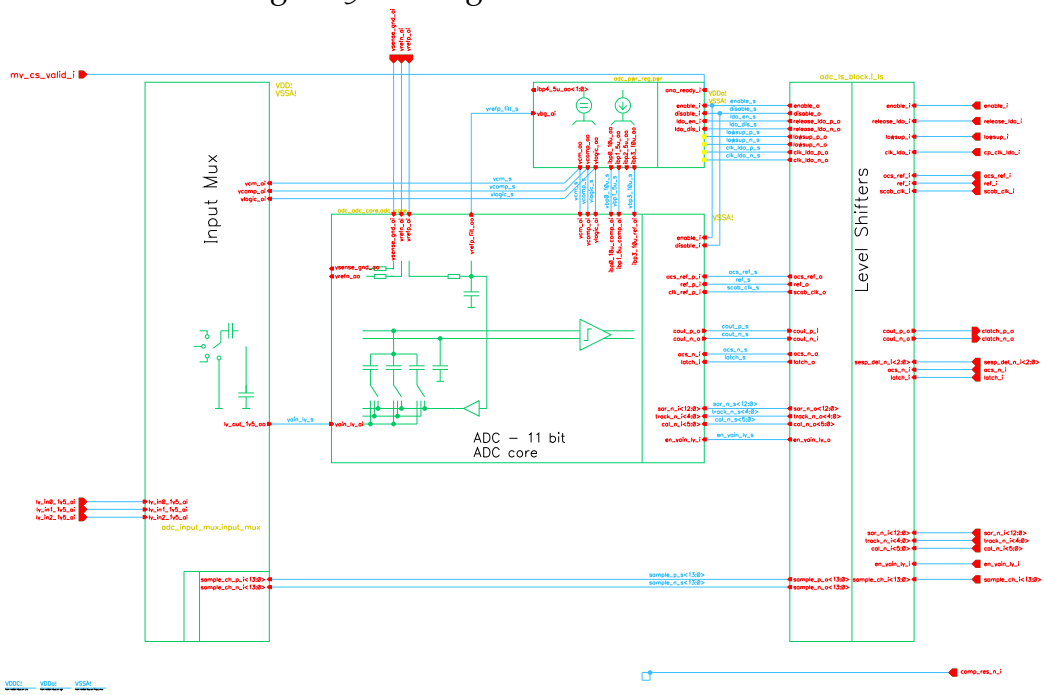
4 Analog Core

Figure 5 shows the analog core of the SAR ADC. On left, you see the input multiplexer for the input channels. On the right side, you see the level shifters, connecting the digital circuitry to the analog side. On the top, you will find the internal voltage regulators that produce the internal voltages:

- $V_{\text{cm}} \approx 0.9\,\text{V}$
- $V_{\text{comp}} = 1.5\,\text{V}$
- $V_{\text{logic}} = 1.5\,\text{V}$

and the required bias currents: 10 µA and 5 µA.

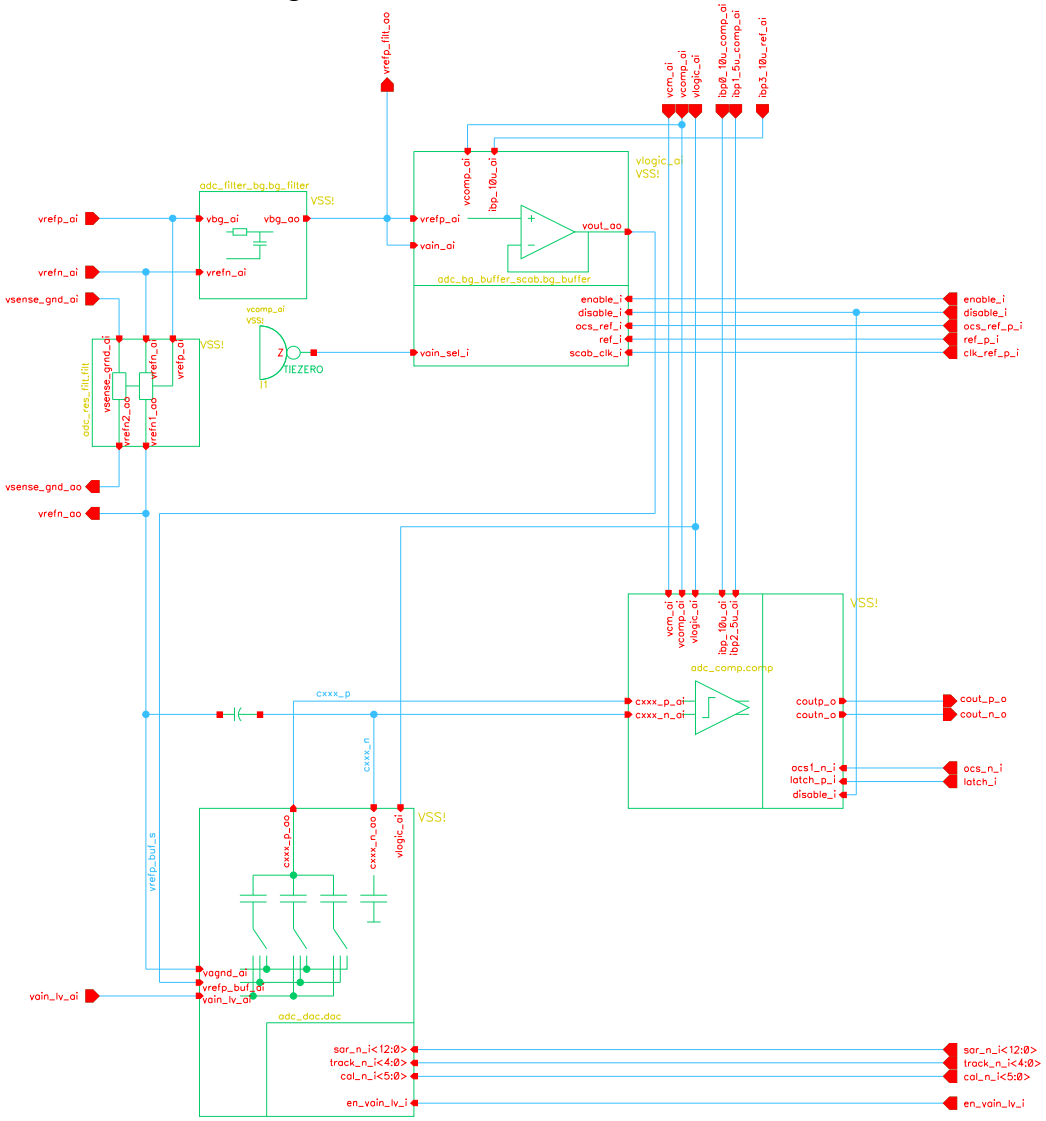
Figure 5: Analog core of the SAR ADC.



5 ADC Core

The ADC core is shown in figure 6. On the top, you see the buffer for the reference voltage together with a low pass filter on the input. On the right side, you see the comparator. On the bottom, you see the C-DAC.

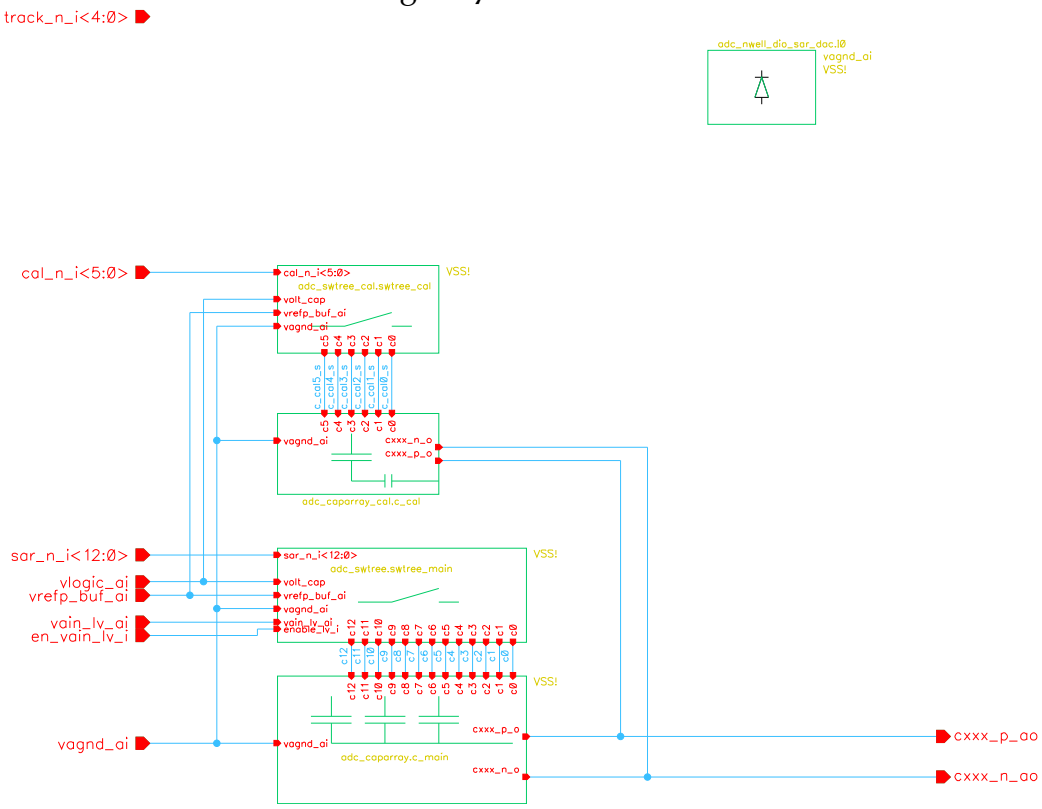
Figure 6: ADC core of the SAR ADC.



6 ADC DAC

The DAC of the ADC can be seen in figure 7. The capacitor array, which has a total capacitance of 512 fF, is shown in figure 8.

Figure 7: ADC DAC.



The calibration DAC is not used during the tests. The tracking DAC has been removed.

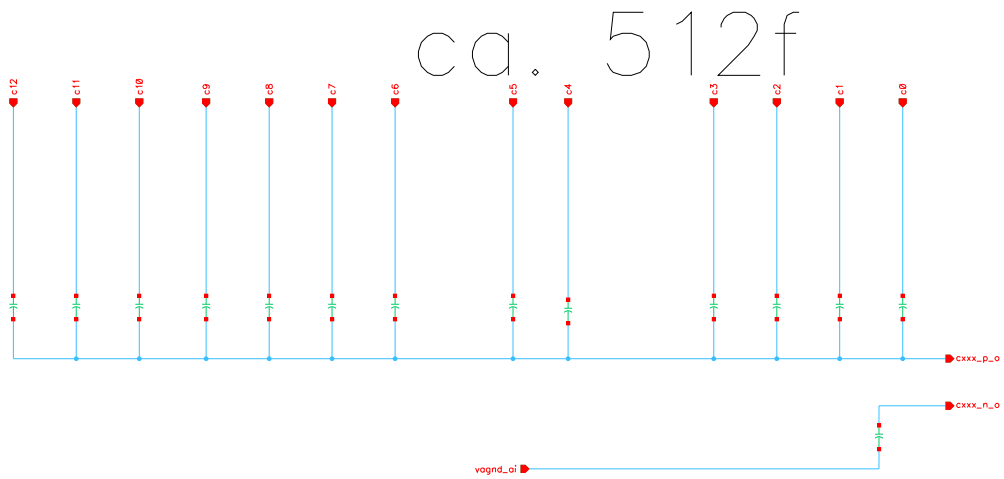
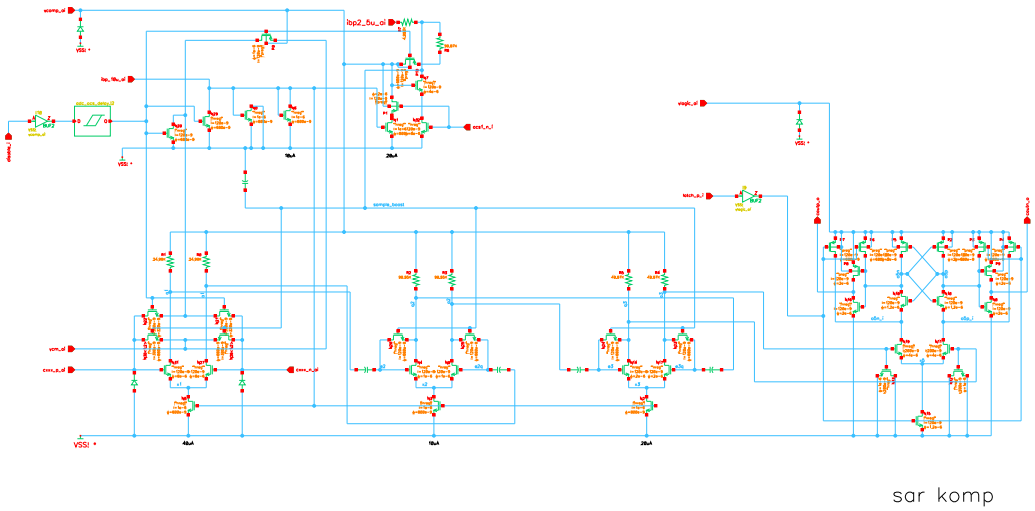


Figure 8: DAC capacitor array.

7 Comparator

Figure 9 shows the comparator. It consists out of 3 amplifier and one latching stage. The switches to precharge the inputs to V_{cm} are boosted by a current that originates from the 2.5 V voltage domain.

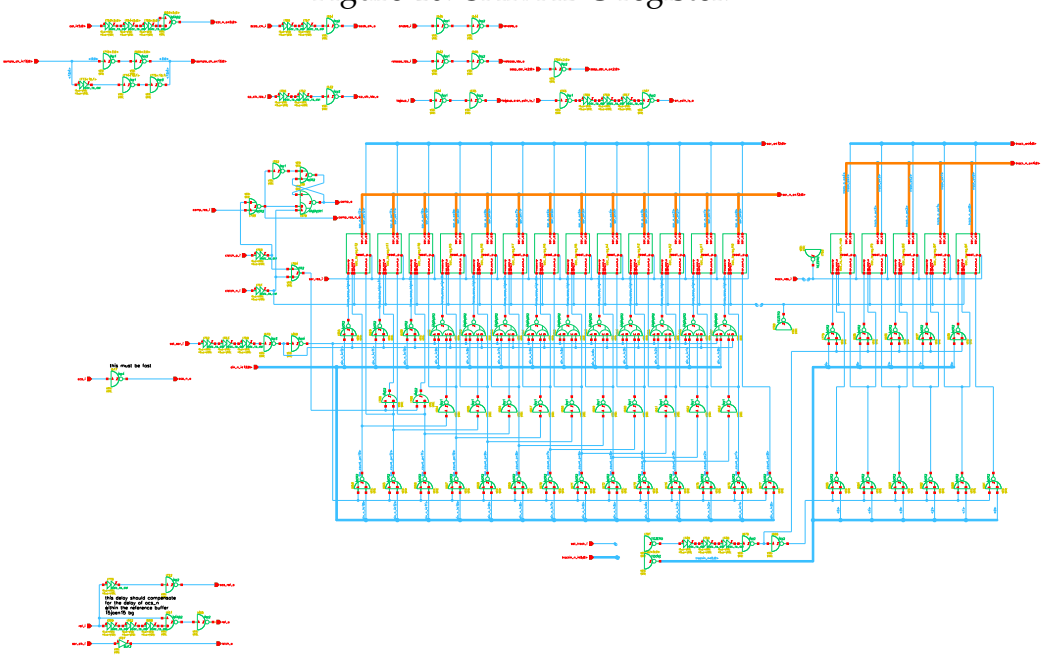
Figure 9: ADC Comparator.



8 SAR Register

The register that contains the results of each comparison is depicted in figure 10. The register of the tracking DAC is kept but not used. Any injected fault in this block cannot be detected.

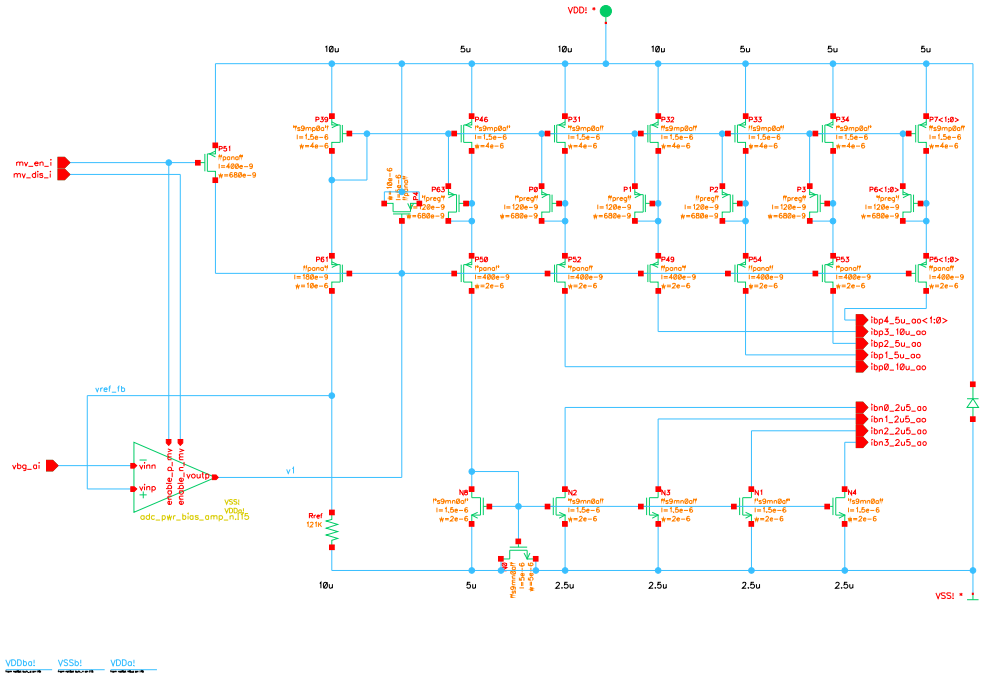
Figure 10: SAR ADC register.



9 Bias Current Generation

In contrast to the current sinks, all current sources are cascoded (see e.g. figure 11). If the cascode has a short between drain and source, then this error should most likely not be detectable.

Figure 11: Bias generation example.



10 Test IDs

The following test ids are output when an error occures:

Table 3: Test IDs of the SAR ADC.

Test ID	Description
4	DNL histogram test failed
5	INL histogram test failed
6	Catastrophic fault detected
11	DNL and INL histogram test failed

The test id is 0 if everything is within the specification.