Bandgap Circuit for the Evaluation of Analog Defect Simulation Tools

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Note:
The CMOS transistor models used, were freely available models downloaded from: http://ptm.asu.edu.
The bipolar transistor models are from: **The Development of Bipolar Log-Domain Filters in a Standard CMOS Process**, G. D. Duerden, G. W. Roberts, M. J. Deen, 2001

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Abstract:

This document describes the bandgap circuit and its test suite. It should enable the reader to perform defect simulations on the bandgap circuit and to adapt the test bench if needed.

Audience: Tool evaluators

1 Description of the bandgap circuit

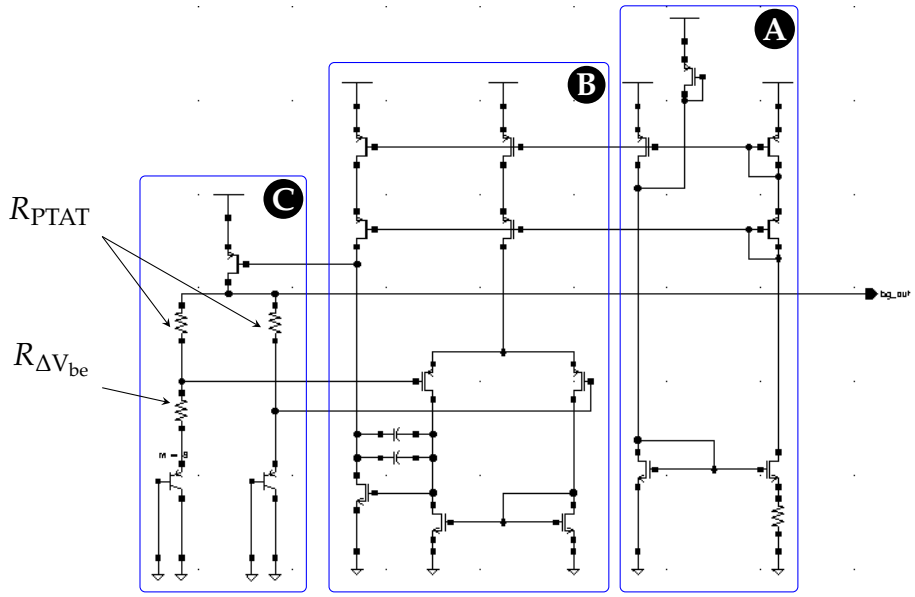

Figure 1: Bandgap schematic overview.

Figure 1 shows a simplified schematic of the bandgap. The block labelled A is an independent biasing for the bandgap circuit.

The block B is an operational amplifier that controls the current flowing into the transistors used to generate the PTAT (**P**roportional **t**o **a**bsolute **t**emperature) and CTAT (**C**omplementary **t**o **a**bsolute **t**emperature) voltages.

Block C is the core of the bandgap. This part of the circuit generates a ΔV_{be} voltage across resistor $R_{\Delta V_{be}}$ at the emitter of the left pnp-bjt, this results in a PTAT current flowing through the resistor.

Because the opamp insures that the voltages at its inputs are equal, it regulates the current through the bandgap core so that the voltage across the two R_{PTAT} resistors are equal, and as both resistors have equal values, the same PTAT current flows through both R_{PTAT} resistors.

The value of the R_{PTAT} resistors is chosen so that the voltage drop across them has the opposite temperature coefficient to that of the V_{be} of the right pnp-bjt, this results in a temperature independent voltage at the `bg_out` pin as this voltage is the sum of the V_{be} of the right pnp-bjt and the voltage across the right R_{PTAT} resistor.

Figure 2 shows the schematic of the bandgap circuit contained in the netlist.

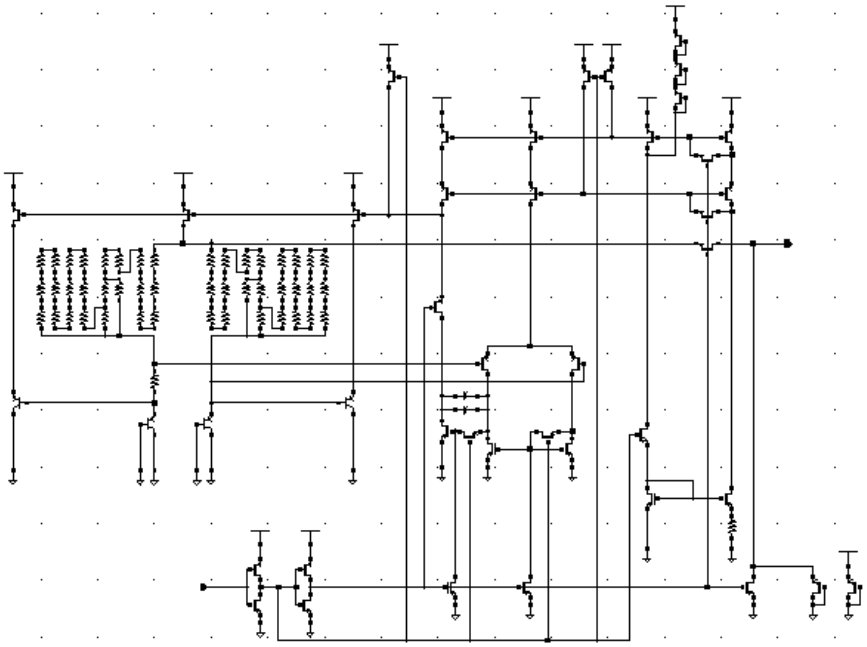

Figure 2: Bandgap full schematic.

Here, circuitry to disable the bandgap is included. The R_{PTAT} resistors consist of a series/parallel network using a unit resistor having the same value as the $R_{\Delta V_{be}}$ resistor. Base current compensation transistors have been added to the bandgap core. A reverse polarity protection has also been added.

Table 1: List of module signals.

Name	Type	Min.	Nom.	Max.	Unit
`VDDA!`	Power	2.25	2.5	2.75	V
`bg_out`	Output	1.395	1.4	1.405	V
`disable`	Input	0	2.5	`VDDA!`	V

Table 1 lists the signals needed to operate the bandgap. Please note that `disable` is high active. When high it disables the bandgap.

2 Description of the test bench

The test procedure is written in `VerilogA` and runs according to the following description:

1. After power up, the `disable` signal is asserted (Set to `VDDA!`), the first measurement of the voltage at pin `bg_out` is performed at 10 ms, this voltage should be below 10 mV in the fault free case. In your test bench, please make sure that the `disable` signal stays high for at least 10 ms.

2. The `disable` signal is then set to 0 V and at 50 ms the second measurement of `bg_out` takes place. This measurement checks the bandgap voltage, and is fault free if 1.395 V $<$`bg_out`$<$ 1.405 V

3. At time 100 ms, the `bg_out` voltage is measured again. This test ensures that the operational amplifier has settled and that there are no oscillations. To be fault free, the voltage measured during this this test should not differ from the voltage measured at time 50 ms by more than 7 mV.

The signals `fail` and `testnr` indicate respectively that a fault has been detected, and which fault triggered the fail.

A fault can be triggered by each of the measurements, meaning that the signal `fail` can flag a fault by rising to 1 V, but if the simulation continues, the `testnr` can still change value: *the* `testnr` *value is set by the latest detected fault*.

As an example, if you let the simulation run after an idle test fail, if now the bandgap voltage is outside of the limits, then `testnr` will have the value flagging that the bandgap voltage was out of the limits.

Table 2: List of tests and `testnr` values.

Name	Value	Time	`disable`	Fault cond	`testnr`	`fail`
Idle	$\texttt{val}_1$	10 ms	`VDDA!`	$\texttt{val}_1 > 10$ mV	1	1
Value	$\texttt{val}_1$	50 ms	0 V	$\lvert\texttt{val}_1 - 1.4\,\text{V}\rvert > 5$ mV	2	1
Settling	$\texttt{val}_2$	0.1 s	0 V	$\lvert\texttt{val}_2 - \texttt{val}_1\rvert > 7$ mV	3	1

Table 2 lists the sequence of tests, the conditions under which they should be performed as well as the conditions that lead to a test fail.