PHY for the Evaluation of Analog Defect Simulation Tools

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September 27, 2021

Note:
The CMOS transistor models used, were freely available models downloaded from: http://ptm.asu.edu.
The bipolar transistor models are from: **The Development of Bipolar Log-Domain Filters in a Standard CMOS Process**, G. D. Duerden, G. W. Roberts, M. J. Deen, 2001

Contents

List of Figures

List of Tables

Abstract:

This document introduces you to the schematic and the internal circuits of the delivered phy. The purpose is to enable the reader to understand, run and extend the test benches of this circuit.

Audience: Tool evaluators

1 Overview

This document gives you the most important information about the 16 bit, 1/2 Gprs phy that is used to test EDA software for Analog Fault Simulation. The circuit has been implemented in an 130 nm open source technology taken from http://ptm.asu.edu/. The top level symbol of the phy is shown in figure 2. Figure 1 shows the concept of the phy. It consists out of 4 identical data lanes and one clock lane which outputs a 90° shifted output signal. The phy has a 1 Gprs and a 2 Gprs mode. Each lane includes an high speed transmitter (HSTX) and a low power transmitter (LPTX).

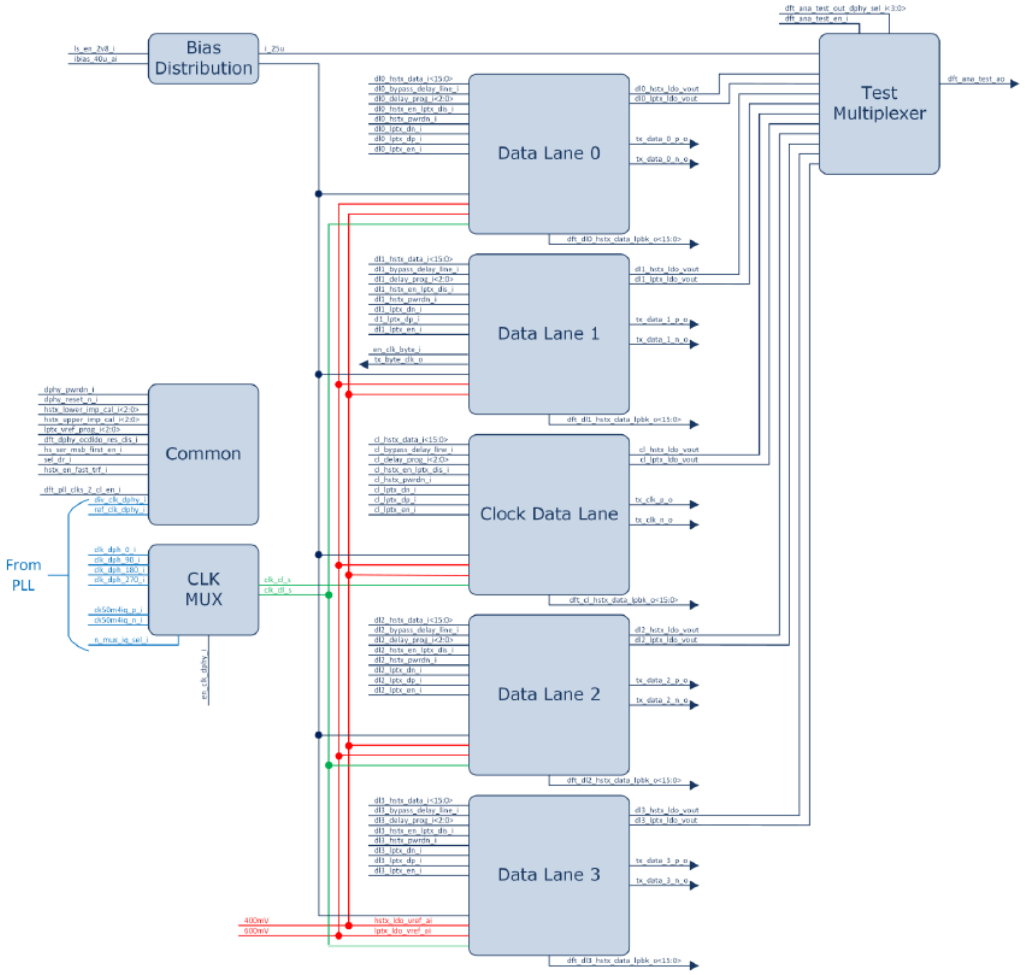

Figure 1: Concept overview of the phy.

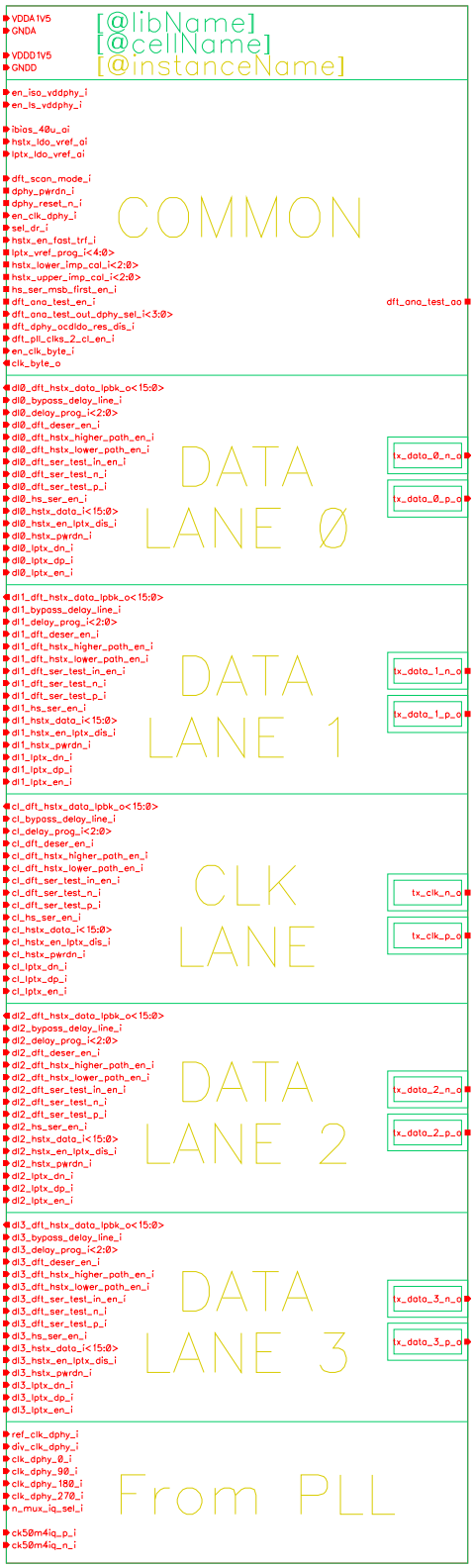

Figure 2: Top level symbol of the phy.

1.1 Lane

Each lane is build up identical. Figure 3 shows the structure. It consists out of a serializer that takes the 16 bit input word and outputs a bitstream. A deserializer can be used for dft purposes to check the correctness of the serializer. A configurable delay line follows the serializer and can be used to introduce an additional delay to the lane to counter act mismatches of PCB trace lengths. The next component is a pre-driver that can be configured in two modes: normal (1 Gbps) or fast mode (2 Gbps). The four output signals of the pre-driver control the gates of an H-bridge inside of the HSTX OCD. This H-bridge is fed by the internal HSTX LDO that produces a 400 mV. In LPTX mode, the HSTX output stages are disabled, giving the LPTX drivers the possibility to drive the pad outputs to either 1.2 V or GND. The 1.2 V voltage is generated by another internal LDO.

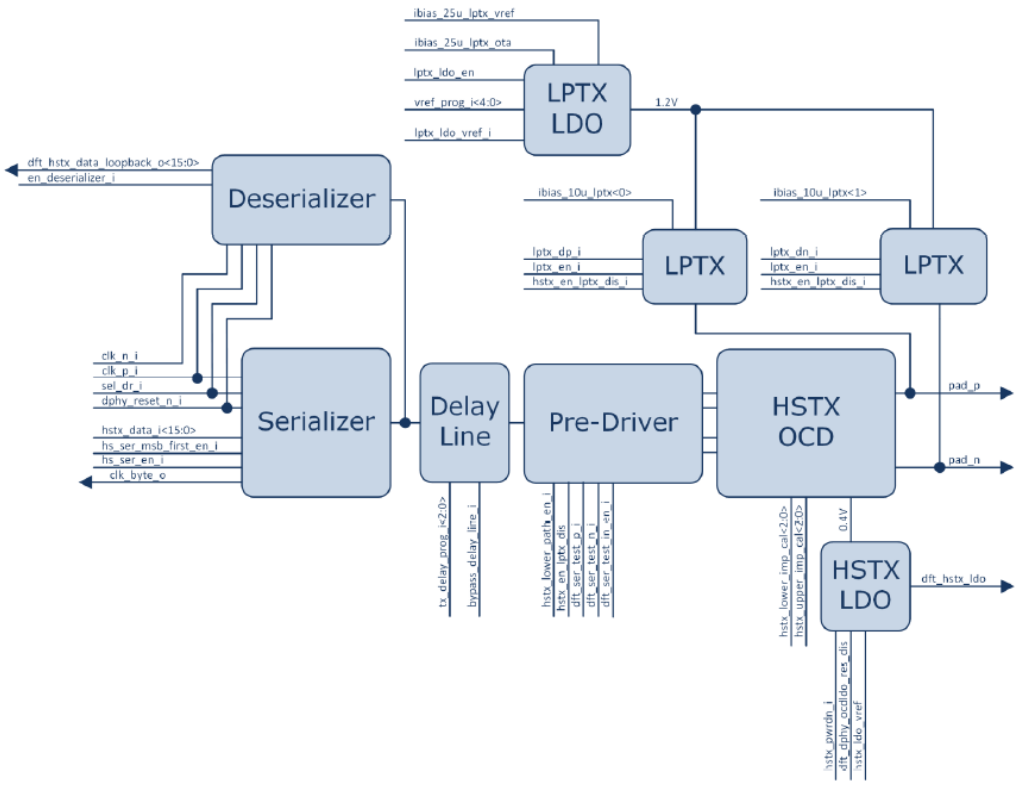

Figure 3: Internals of a lane.

1.2 Pin List

The phy offers many pins. The following list shows all of them.

Table 1: Pin list of the phy.

Terminal Name	Dir	Min	Typ	Max	Unit	Description
GNDA	input	0	0	0	V	Analog ground
GNDD	input	0	0	0	V	Digital ground
VDDA1V5	input	0	1.5	1.5	V	Analog supply
VDDD1V5	input	0	1.5	1.5	V	Digital supply
clk_dphy_0_i	input	0	-	1.5	V	Clock input from DLL (phase: 0°)
clk_dphy_90_i	input	0	-	1.5	V	Clock input from DLL (phase: 90°)
clk_dphy_180_i	input	0	-	1.5	V	Clock input from DLL (phase: 180°)
clk_dphy_270_i	input	0	-	1.5	V	Clock input from DLL (phase: 270°)
ck50m4iq_n_i	input	0	-	1.5	V	not used
ck50m4iq_p_i	input	0	-	1.5	V	not used
clk_byte_0	output	0	-	1.5	V	Output to synchronize the receiver for design for test (DfT) purposes
dft_ana_test_ao	output	0	-	1.5	V	Output of Analog DfT Testmux
dft_ana_test_en_i	input	0	-	1.5	V	
dft_ana_test_out_dphy_sel_i<3:0>	input	0	-	1.5	V	
dft_dphy_ocdldo_res_dis_i	input	0	-	1.5	V	
dft_pll_clks_2_cl_en_i	input	0	-	1.5	V	
dft_scan_mode_i	input	0	-	1.5	V	
div_clk_dphy_i	input	0	-	1.5	V	

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Terminal Name	Dir	Min	Typ	Max	Unit	Description
cl_bypass_delay_line_i	input	0	-	1.5	V	If 1 then bypass the delay line
cl_delay_prog_i<2:0>	input	0	-	1.5	V	Delay setting
cl_dft_deser_en_i	input	0	-	1.5	V	Enable the deserializer for DfT purposes
cl_dft_hstx_data_lpbk_o<15:0>	output	0	-	1.5	V	Output of the deserializer for DfT purposes
cl_dft_hstx_higher_path_en_i	input	0	-	1.5	V	Enable the HSTX pull up transistors
cl_dft_hstx_lower_path_en_i	input	0	-	1.5	V	Enable the HSTX pull down transistors
cl_dft_ser_test_in_en_i	input	0	-	1.5	V	
cl_dft_ser_test_n_i	input	0	-	1.5	V	
cl_dft_ser_test_p_i	input	0	-	1.5	V	
cl_hs_ser_en_i	input	0	-	1.5	V	
cl_hstx_data_i<15:0>	input	0	-	1.5	V	
cl_hstx_en_lptx_dis_i	input	0	-	1.5	V	
cl_hstx_pwrdn_i	input	0	-	1.5	V	
cl_lptx_dn_i	input	0	-	1.5	V	Input to the pull down transistors of the LPTX driver
cl_lptx_dp_i	input	0	-	1.5	V	Input to the pull up transistors of the LPTX driver
cl_lptx_en_i	input	0	-	1.5	V	Enable/Disable the LPTX driver
dlo_bypass_delay_line_i	input	0	-	1.5	V	All lanes have the same signals

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Terminal Name	Dir	Min	Typ	Max	Unit	Description
dlo_delay_prog_i<2:0>	input	0	-	1.5	V	
dlo_dft_deser_en_i	input	0	-	1.5	V	
dlo_dft_hstx_data _lpbk_o<15:0>	output	0	-	1.5	V	
dlo_dft_hstx_higher _path_en_i	input	0	-	1.5	V	
dlo_dft_hstx_lower _path_en_i	input	0	-	1.5	V	
dlo_dft_ser_test_in _en_i	input	0	-	1.5	V	
dlo_dft_ser_test_n_i	input	0	-	1.5	V	
dlo_dft_ser_test_p_i	input	0	-	1.5	V	
dlo_hs_ser_en_i	input	0	-	1.5	V	
dlo_hstx_data_i<15:0>	input	0	-	1.5	V	
dlo_hstx_en_lptx _dis_i	input	0	-	1.5	V	
dlo_hstx_pwrdn_i	input	0	-	1.5	V	
dlo_lptx_dn_i	input	0	-	1.5	V	
dlo_lptx_dp_i	input	0	-	1.5	V	
dlo_lptx_en_i	input	0	-	1.5	V	
dl1_bypass_delay_line _i	input	0	-	1.5	V	
dl1_delay_prog_i<2:0>	input	0	-	1.5	V	
dl1_dft_deser_en_i	input	0	-	1.5	V	
dl1_dft_hstx_data _lpbk_o<15:0>	output	0	-	1.5	V	
dl1_dft_hstx_higher _path_en_i	input	0	-	1.5	V	
dl1_dft_hstx_lower _path_en_i	input	0	-	1.5	V	
dl1_dft_ser_test_in _en_i	input	0	-	1.5	V	
dl1_dft_ser_test_n_i	input	0	-	1.5	V	
dl1_dft_ser_test_p_i	input	0	-	1.5	V	
dl1_hs_ser_en_i	input	0	-	1.5	V	
dl1_hstx_data_i<15:0>	input	0	-	1.5	V	
dl1_hstx_en_lptx _dis_i	input	0	-	1.5	V	

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Terminal Name	Dir	Min	Typ	Max	Unit	Description
dl1_hstx_pwrdn_i	input	0	-	1.5	V	
dl1_lptx_dn_i	input	0	-	1.5	V	
dl1_lptx_dp_i	input	0	-	1.5	V	
dl1_lptx_en_i	input	0	-	1.5	V	
dl2_bypass_delay_line_i	input	0	-	1.5	V	
dl2_delay_prog_i<2:0>	input	0	-	1.5	V	
dl2_dft_deser_en_i	input	0	-	1.5	V	
dl2_dft_hstx_data_lpbk_o<15:0>	output	0	-	1.5	V	
dl2_dft_hstx_higher_path_en_i	input	0	-	1.5	V	
dl2_dft_hstx_lower_path_en_i	input	0	-	1.5	V	
dl2_dft_ser_test_in_en_i	input	0	-	1.5	V	
dl2_dft_ser_test_n_i	input	0	-	1.5	V	
dl2_dft_ser_test_p_i	input	0	-	1.5	V	
dl2_hs_ser_en_i	input	0	-	1.5	V	
dl2_hstx_data_i<15:0>	input	0	-	1.5	V	
dl2_hstx_en_lptx_dis_i	input	0	-	1.5	V	
dl2_hstx_pwrdn_i	input	0	-	1.5	V	
dl2_lptx_dn_i	input	0	-	1.5	V	
dl2_lptx_dp_i	input	0	-	1.5	V	
dl2_lptx_en_i	input	0	-	1.5	V	
dl3_bypass_delay_line_i	input	0	-	1.5	V	
dl3_delay_prog_i<2:0>	input	0	-	1.5	V	
dl3_dft_deser_en_i	input	0	-	1.5	V	
dl3_dft_hstx_data_lpbk_o<15:0>	output	0	-	1.5	V	
dl3_dft_hstx_higher_path_en_i	input	0	-	1.5	V	
dl3_dft_hstx_lower_path_en_i	input	0	-	1.5	V	
dl3_dft_ser_test_in_en_i	input	0	-	1.5	V	

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Terminal Name	Dir	Min	Typ	Max	Unit	Description
dl3_dft_ser_test_n_i	input	0	-	1.5	V	
dl3_dft_ser_test_p_i	input	0	-	1.5	V	
dl3_hs_ser_en_i	input	0	-	1.5	V	
dl3_hstx_data_i<15:0>	input	0	-	1.5	V	
dl3_hstx_en_lptx _dis_i	input	0	-	1.5	V	
dl3_hstx_pwrdn_i	input	0	-	1.5	V	
dl3_lptx_dn_i	input	0	-	1.5	V	
dl3_lptx_dp_i	input	0	-	1.5	V	
dl3_lptx_en_i	input	0	-	1.5	V	
dphy_pwrdn_i	input	0	-	1.5	V	
dphy_reset_n_i	input	0	-	1.5	V	
en_clk_byte_i	input	0	-	1.5	V	
en_clk_dphy_i	input	0	-	1.5	V	
en_iso_vddphy_i	input	0	-	1.5	V	
en_ls_vddphy_i	input	0	-	1.5	V	
hs_ser_msb_first_en_i	input	0	-	1.5	V	
hstx_en_fast_trf_i	input	0	-	1.5	V	
hstx_ldo_vref_ai	input	0	0.4	0.6	V	
hstx_lower_imp_cal _i<2:0>	input	0	-	1.5	V	
hstx_upper_imp_cal _i<2:0>	input	0	-	1.5	V	
ibias_40u_ai	input	0	40	40	µA	
lptx_ldo_vref_ai	input	0	0.6	1	V	
lptx_vref_prog_i<4:0>	input	0	-	1.5	V	
n_mux_iq_sel_i	input	0	-	1.5	V	
ref_clk_dphy_i	input	0	-	1.5	V	
sel_dr_i	input	0	-	1.5	V	Select 1 Gbps or 2 Gbps mode
tx_clk_n_0	output	0	-	1.2	V	N-Output of clock lane
tx_clk_p_0	output	0	-	1.2	V	P-Output of clock lane
tx_data_0_n_0	output	0	-	1.2	V	N-Output of data lane 0

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Terminal Name	Dir	Min	Typ	Max	Unit	Description
tx_data_0_p_0	output	0	-	1.2	V	P-Output of data lane 0
tx_data_1_n_0	output	0	-	1.2	V	N-Output of data lane 1
tx_data_1_p_0	output	0	-	1.2	V	P-Output of data lane 1
tx_data_2_n_0	output	0	-	1.2	V	N-Output of data lane 2
tx_data_2_p_0	output	0	-	1.2	V	P-Output of data lane 2
tx_data_3_n_0	output	0	-	1.2	V	N-Output of data lane 3
tx_data_3_p_0	output	0	-	1.2	V	P-Output of data lane 3

1.3 Characteristics

Table 2 shows the typical electrical characteristics of the phy.

Table 2: Characteristics of the phy.

Symbol	Min	Typ	Max	Unit	Description
Number of lanes		5			Number of lanes
Bit width of one lane		16			Bit width of one lane
$f_{PLL,out} = f_{DLL,in}$	-	200	-	MHz	Output frequency of the PLL and input frequency of the DLL
$f_{DLL,out}$	-	1	-	GHz	Output frequency of the four phase clock generated by the DLL

1.4 Clock Source

The phy is powered by a DLL that generates the for phase clock from the output of a PLL. The DLL is shown in figure 4 and 5. The output frequency of the DLL is a four phase 1 GHz signal.

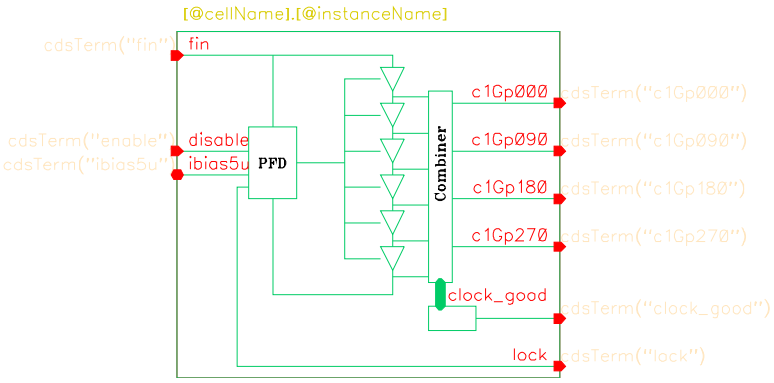

Figure 4: DLL symbol.

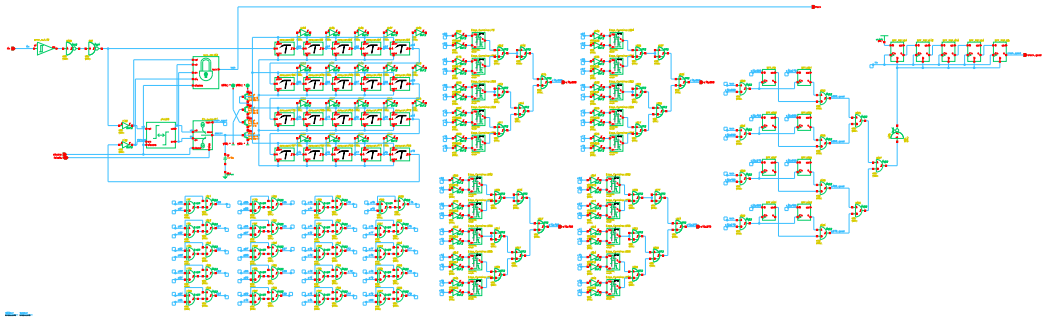

Figure 5: DLL schematic.

2 The Test Bench

The test bench consists out of the device under test (DUT) in the middle and the it is surrounded by the test program, see figure 6. Additionally, it includes a bandgap and bias circuit that produces the 40 µA bias current and the required 600 mV and 400 mV reference voltages. Furthermore, the test bench offers multiple measurement and stimuli blocks that have been implemented with Verilog-A or in schematic which should not be part of the fault injection.

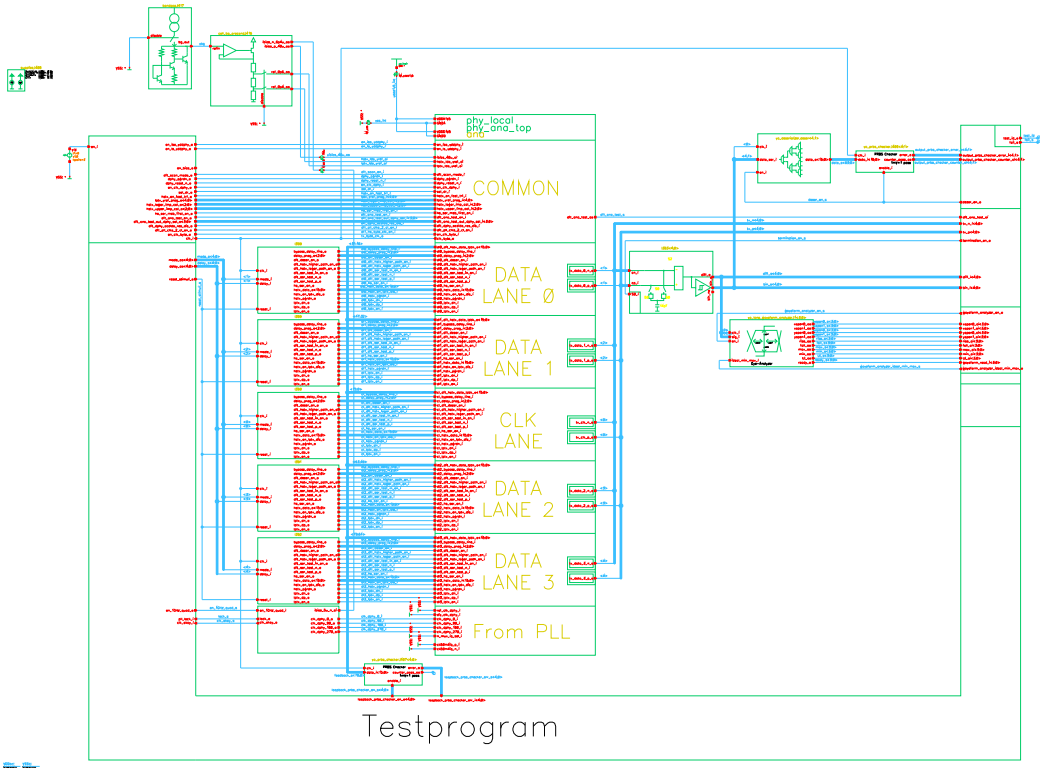

Figure 6: Test bench of the phy.

2.1 Tests

The following tests are performed sequentially:

- Ramp up: Enable the phy and wait till the internal LDOs settle.
- LDO checks: Test all HSTX LDOs and LPTX LDOs via the analog DfT bus.

- LPTX checks: Check the voltage levels and timing of the LPTX output stages.
- DC checks: Measure the output voltage levels for various loads (impedance measurement).
- Delay line checks: Go through all delay line settings and check the introduced delay.
- HSTX PRBS check: Finally, input a PRBS-9 bitstream to the input and check the received output words.

If one test fails, the simulation is stopped and an error is indicated by the test_id signal.