



Introduction to PSOC™ Edge

Customer training workshop

January 2026

public



Table of contents

1	Introduction to PSOC™ Edge	3
2	Overview of PSOC™ Edge features	10
3	Applications use-cases	47
4	Getting started with PSOC™ Edge	55

Table of contents

1	Introduction to PSOC™ Edge	3
2	Overview of PSOC™ Edge features	10
3	Applications use-cases	47
4	Getting started with PSOC™ Edge	55

What is PSOC™ Edge?

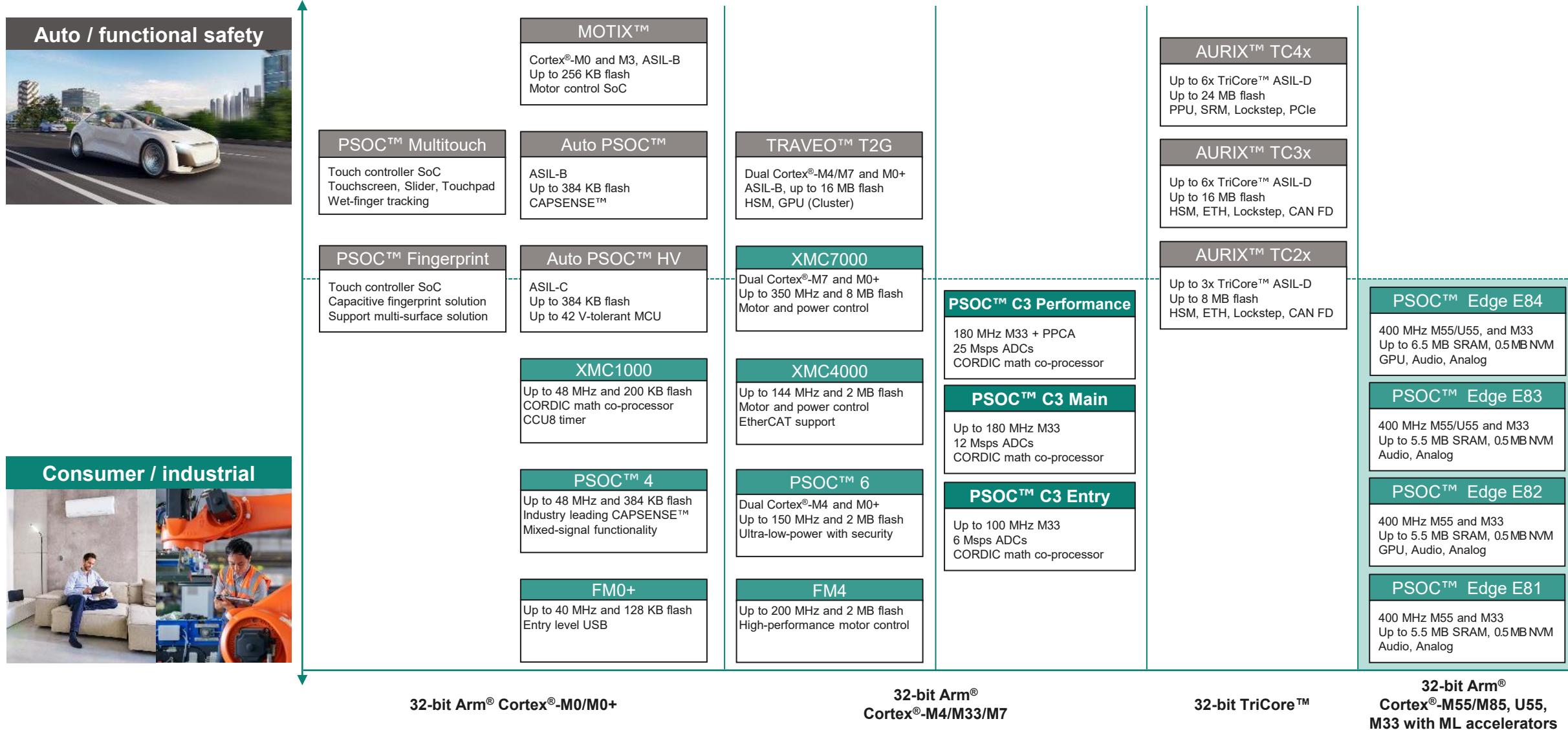
PSOC™ Edge is a microcontroller (MCU) designed for next-generation responsive compute systems, featuring hardware assisted machine learning (ML), artificial intelligence (AI), and sensor fusion capabilities on a power-efficient platform with robust security and advanced human interface capabilities for IoT, consumer, and industrial applications.

PSOC™ Edge is designed to support:

- Low-power applications
- Enhanced sensing, including battery monitoring
- Real-time control
- Communications
- Voice recognition
- Human-machine interface (HMI)
- Machine learning (ML)
- Security

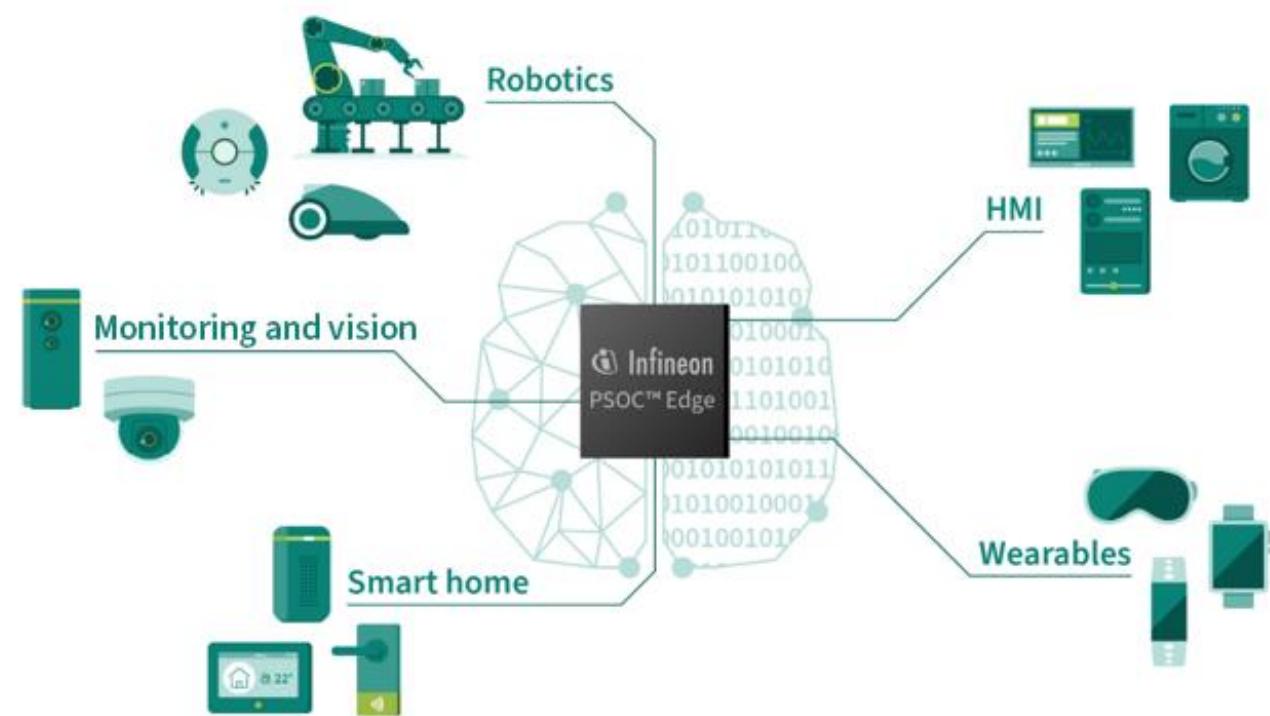


PSOC™ Edge – Infineon's next generation ML-enabled MCUs



PSOC™ Edge – Infineon's next generation ML-enabled MCUs (contd.)

- Arm® Cortex®-M55 based microcontrollers with up to 400 MHz
- Arm® Cortex®-M33 with up 200 MHz
- Arm® Ethos™-U55 and NNLite NPUs for next-generation Edge AI applications
- **Scalable and compatible portfolio** in features, packages, pinouts, memory, and performance
- **Comprehensive peripheral set** to optimize bill-of-materials (BOM) cost
- **Highest level of security** for microcontrollers with Infineon Edge Protect Category 4 (EPC4) and PSA Certified L3/L4 iSE



Key differentiators – Why choose PSOC™ Edge

High performance
Low power



Highest security



Machine learning
Artificial intelligence



Multi-modal HMI



Advanced audio



- Cortex®-M55 MCU core with Helium™ DSP up to 400 MHz
- Always-on, low-power domain Cortex®-M33 MCU core up to 200 MHz

- Infineon EPC4 with PSA Certified L3/L4 iSE
- Secure Enclave architecture
- Edge Protect Bootloader and TF-M Stack available in ModusToolbox™

- Ethos™-U55 NPU at up to 400 MHz
- Infineon's NNLite NPU – up to 200 MHz
- Enabled by DEEPCRAFT™ AI Suite

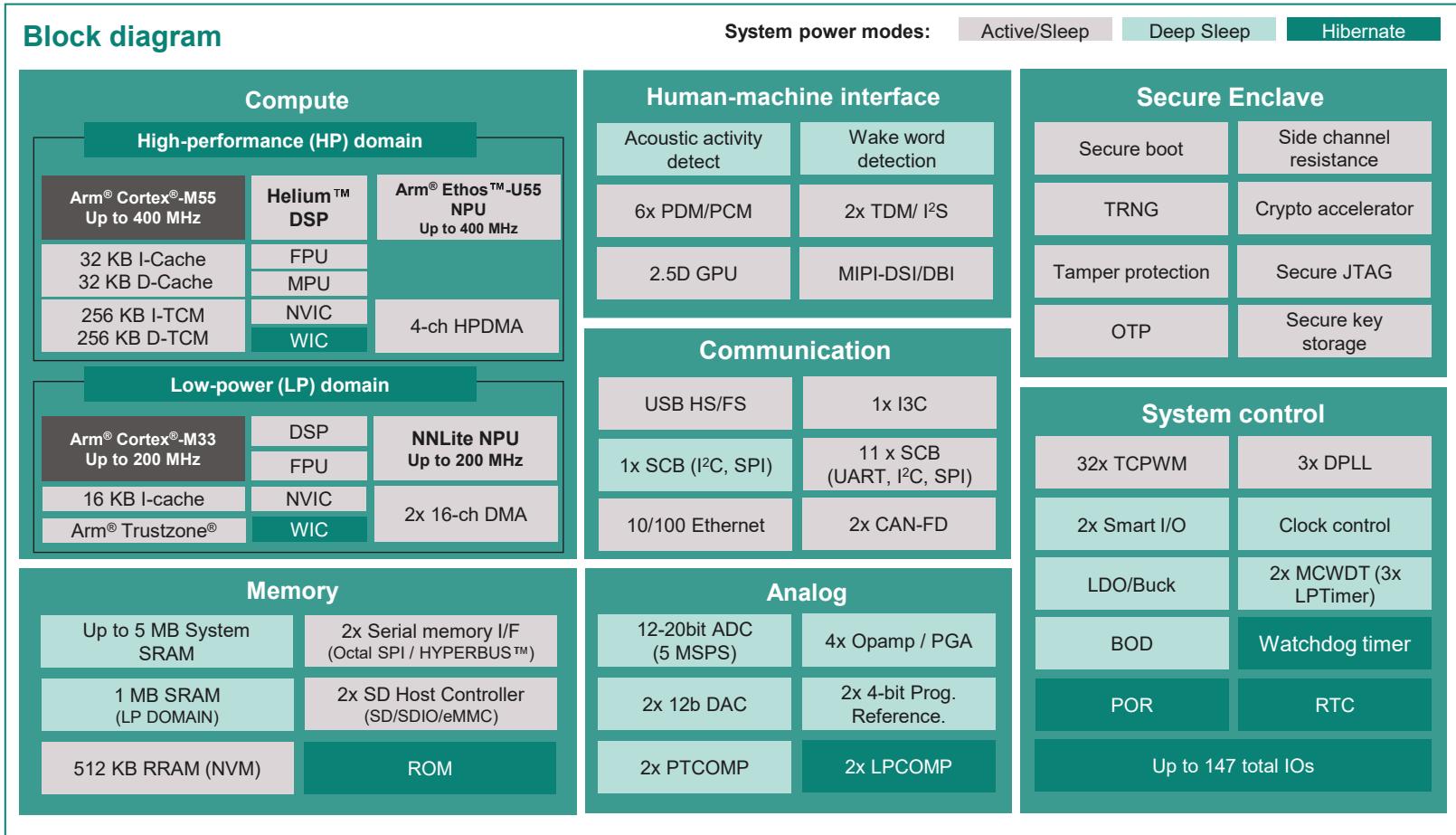
- Voice, Natural Language & Generative AI
- Accelerated multi-microphone audio
- Vision-based awareness and interaction
- Low-power graphics with 2.5D GPU – up to 400 MHz

- Audio enhancement: AI-driven noise suppression and echo cancellation for superior audio clarity
- Voice assistant: Advanced beamforming and scene analysis enable accurate, far-field voice recognition

PSOC™ Edge E84: Low-power advanced ML MCU with graphics



Block diagram



Status/availability

- Documentation available now
- Samples and Evaluation Kits available (PSOC™ Edge E84)
- Qualified samples available now

Packages

WLB154
(5.2 x 4.3 x 0.5 mm,
0.35 mm)

Operating range

-20 to 70°C Ta (Consumer), -40 to 105°C Ta (Industrial)

BGA220
(10 x 10 x 1.2 mm,
0.65 mm)

eWLB235
(7 x 7 x 0.7 mm,
0.4 mm)

Applications and target markets

- Smart home, appliances, residential AC, wearables, industrial HMI, smart speakers, and more

Product highlights

- High performance, real-time compute domain:**
 - Cortex®-M55 with Helium™ DSP and Ethos™-U55 NPU for ML
 - Up to 5 MB system SRAM, 256 KB I&D TCMs**
- Low-power, real-time compute domain:**
 - Cortex®-M33 and DSP with Infineon's NNLite for ML
 - 512 KB RRAM, 1 MB SRAM
- HMI:**
 - Traditional MCU HMI
 - Local voice, cloud voice
 - Vision for friction free interface & safety
 - Low-power graphics, up to 1024x768, MIPI-DSI/DBI**
- ML:** Advanced ML leveraging Ethos™-U55 and NNLite
- Peripherals and IO:**
 - USB, 10/100 Ethernet, CAN, SPI, UART, I2C, I3C, I2S
 - Ultra-low-power always-on analog
- Security:**
 - Secure Enclave at 25 JIL pts, Infineon Edge Protect Category 4 (EPC4) with PSA certified L3/L4 iSE
 - Edge Protect Bootloader and TF-M stack available in ModusToolbox™
- Operating range**
 - 20 to 70°C Ta (consumer), -40 to 105°C Ta (industrial)

PSOC™ Edge E8 MCU family overview

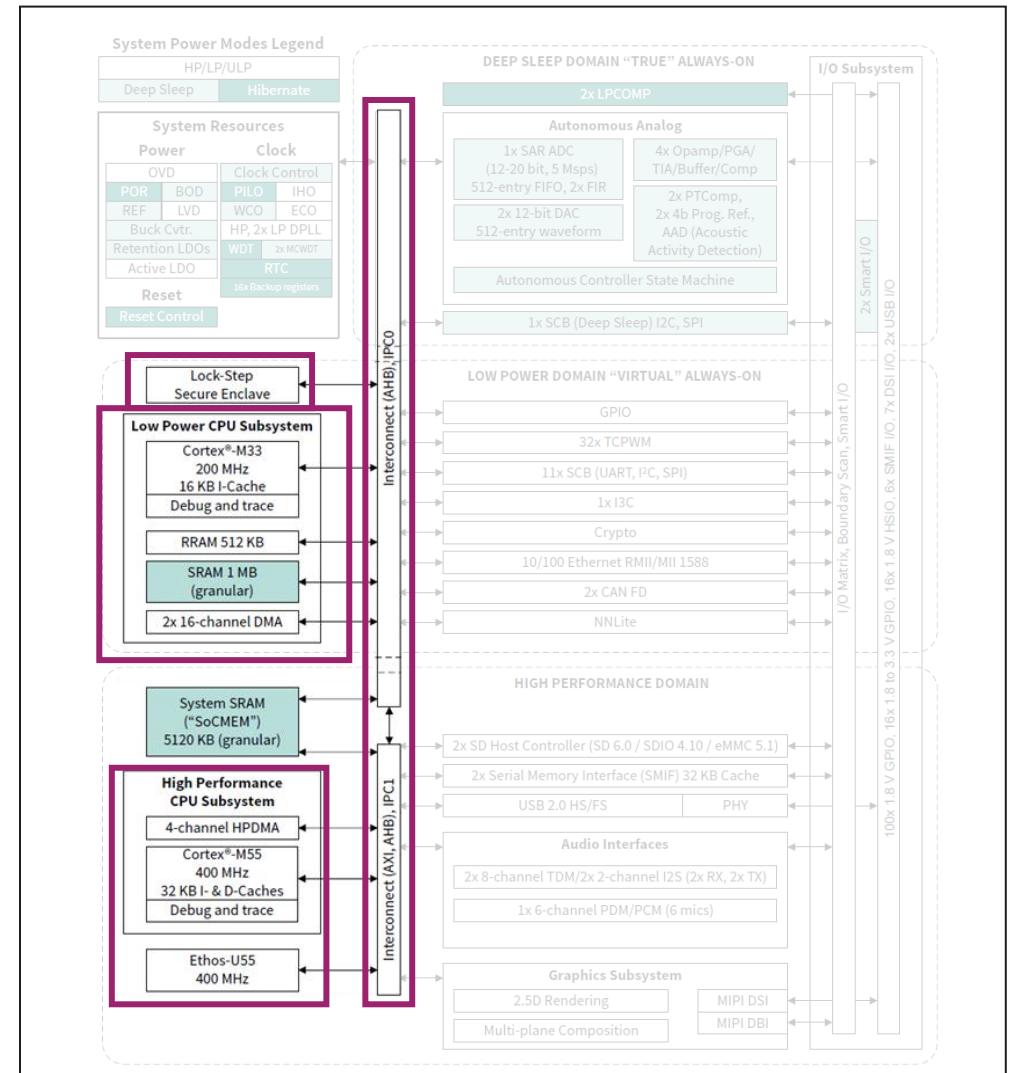
	PSOC™ Edge E81 Base	PSOC™ Edge E82 Base + GFX	PSOC™ Edge E83 Base + NPU + Vision	PSOC™ Edge E84 Base + NPU + Vision + GFX
Processor	Cortex®-M55 + DSP Cortex®-M33	Cortex®-M55 + DSP Cortex®-M33	Cortex®-M55 + DSP Cortex®-M33	Cortex®-M55 + DSP Cortex®-M33
Machine Learning	DSP NN accelerator, NNLite	DSP NN accelerator, NNLite	DSP NN accelerator, NNLite, U55-128	DSP NN accelerator, NNLite, U55-128
SRAM	Up to 4 MB (System RAM) Up to 1 MB (Low-power domain)	Up to 4 MB (System RAM) Up to 1 MB (Low-power domain)	Up to 4 MB (System RAM) Up to 1 MB (low-power domain)	Up to 5 MB (System RAM) Up to 1 MB (low-power domain)
RRAM / NVM	512 kB	512 kB	512 kB	512 kB
External Memory	2x SMIF, 2x SD Host Controller	2x SMIF, 2x SD Host Controller	2x SMIF, 2x SD Host Controller	2x SMIF, 2x SD Host Controller
Audio/Voice	ULP Always ON prog. analog for voice, audio, sensing 4x Analog mic, 6x Digital mic Acoustic activity detection & NNLite Wake Word	ULP Always ON prog. analog for voice, audio, sensing 4x Analog mic, 6x Digital mic Acoustic activity detection & NNLite Wake Word	ULP Always ON prog. analog for voice, audio, sensing 4x Analog mic, 6x Digital mic Acoustic activity detection & U55 ML-based Wake Word & Full voice inferencing	ULP Always ON prog. analog for voice, audio, sensing 4x Analog Mic, 6x Digital mic Acoustic activity detection & U55 ML-based Wake Word, & Full voice inferencing
Graphics	No	LP 2.5D GPU Up to 1024 x 768, MIPI-DSI/DBI formats	No	LP 2.5D GPU Up to 1024 x 768, MIPI-DSI/DBI formats
Vision	No	No	Position detection/Face recognition/Object detection (VGA) via USB	Position detection/Face recognition/Object detection (VGA) via USB
Peripherals & IO	USB, 10/100 Ethernet, CAN, SPI, UART, I2C, I3C, I2S	USB, 10/100 Ethernet, CAN, SPI, UART, I2C, I3C, I2S	USB, 10/100 Ethernet, CAN, SPI, UART, I2C, I3C, I2S	USB, 10/100 Ethernet, CAN, SPI, UART, I2C, I3C, I2S
Security	Infineon EPC4 with PSA Certified L3/L4 iSE Edge-Protect Bootloader and TF-M stack	Infineon EPC4 with PSA Certified L3/L4 iSE Edge-Protect Bootloader and TF-M stack	Infineon EPC4 with PSA Certified L3/L4 iSE Edge-Protect Bootloader and TF-M stack	Infineon EPC4 with PSA Certified L3/L4 iSE Edge-Protect Bootloader and TF-M stack
Packages	BGA-220, 10x10, 0.65p WLB-154, 4.3x5.3, 0.35p	BGA-220, 10x10, 0.65p WLB-154, 4.3x5.3, 0.35p	BGA-220, 10x10, 0.65p WLB-154, 4.3x5.3, 0.35p	BGA-220, 10x10, 0.65p eWLB-235, 7x7, 0.4p WLB-154, 4.3x5.3, 0.35p
Availability	Available now	Available now	Available now	Available now

Table of contents

1	Introduction to PSOC™ Edge	3
2	Overview of PSOC™ Edge features	10
3	Applications use-cases	47
4	Getting started with PSOC™ Edge	55

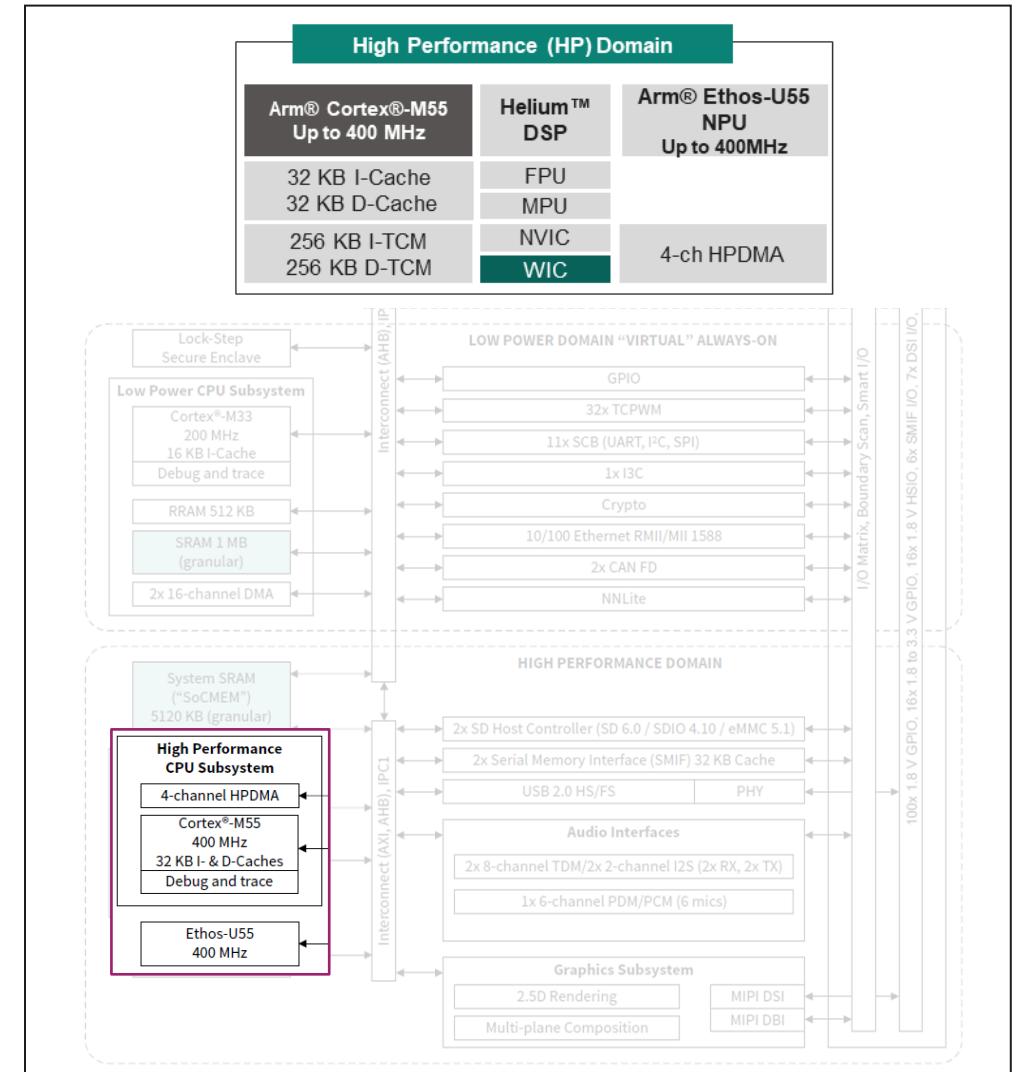
PSOC™ Edge E84: CPU subsystem architecture

- High performance CPU subsystem
 - Cortex®-M55 CPU
 - Arm® Ethos™-U55 NPU
- Low-power CPU subsystem
 - Cortex®-M33 CPU
- Lockstep Secure Enclave
- Inter-processor communication



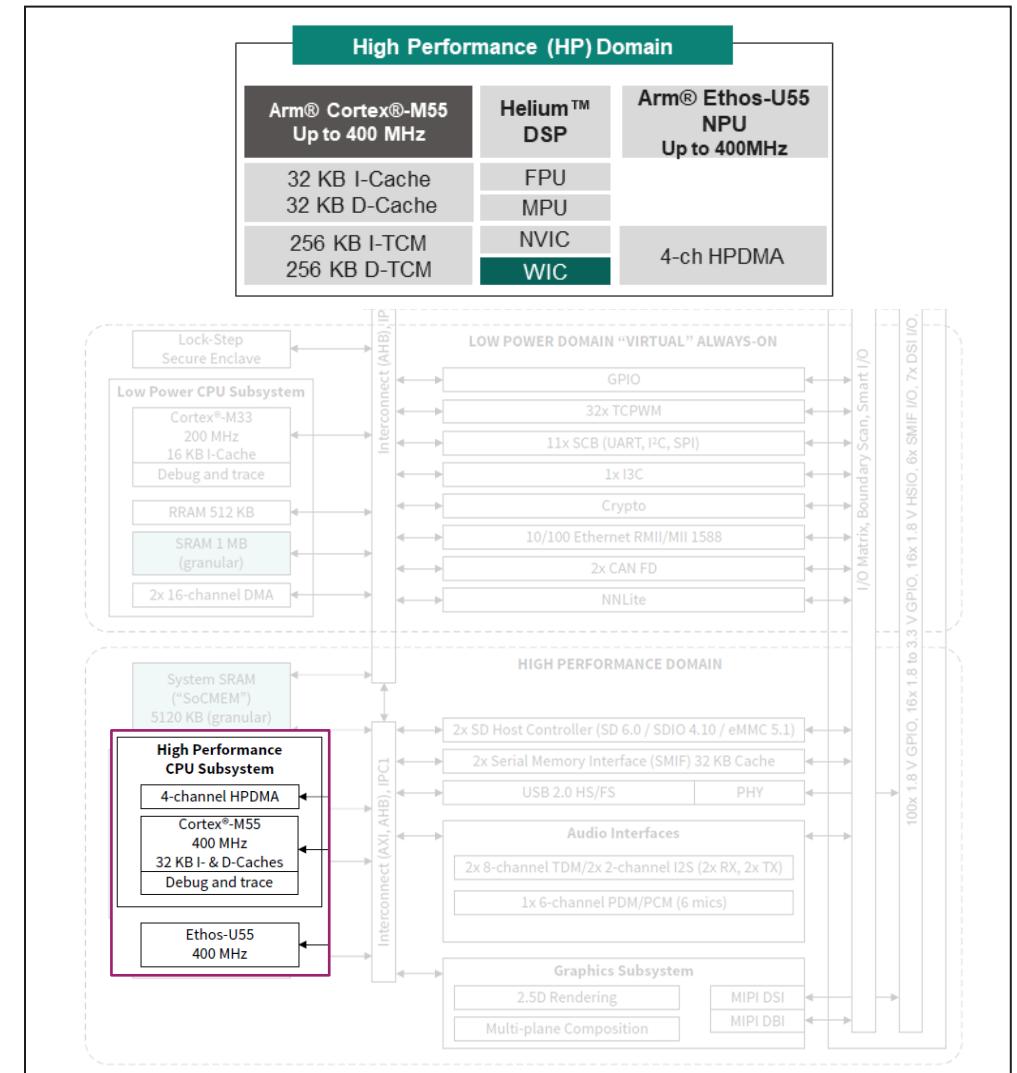
High-performance CPU subsystem: Cortex®-M55 CPU

- Runs at up to 400 MHz
- M-Profile Vector Extension (MVE), or Helium™, for DSP and ML applications
- Floating-point unit (FPU): half, single and double-precision operations
- Nested Vectored Interrupt Controller (NVIC)
 - 480 interrupts; configurable priority levels: 8 to 256
 - Non-Maskable Interrupt (NMI)
- Wake-up Interrupt Controller (WIC)
- Programming and debug support
 - SWD and JTAG, hardware and software breakpoints
 - Trace capability: 8-bit ITM, ETM interfaces with ETB and TPIU
- 32 KB each instruction and data caches
- 256 KB each instruction and data tightly coupled memories



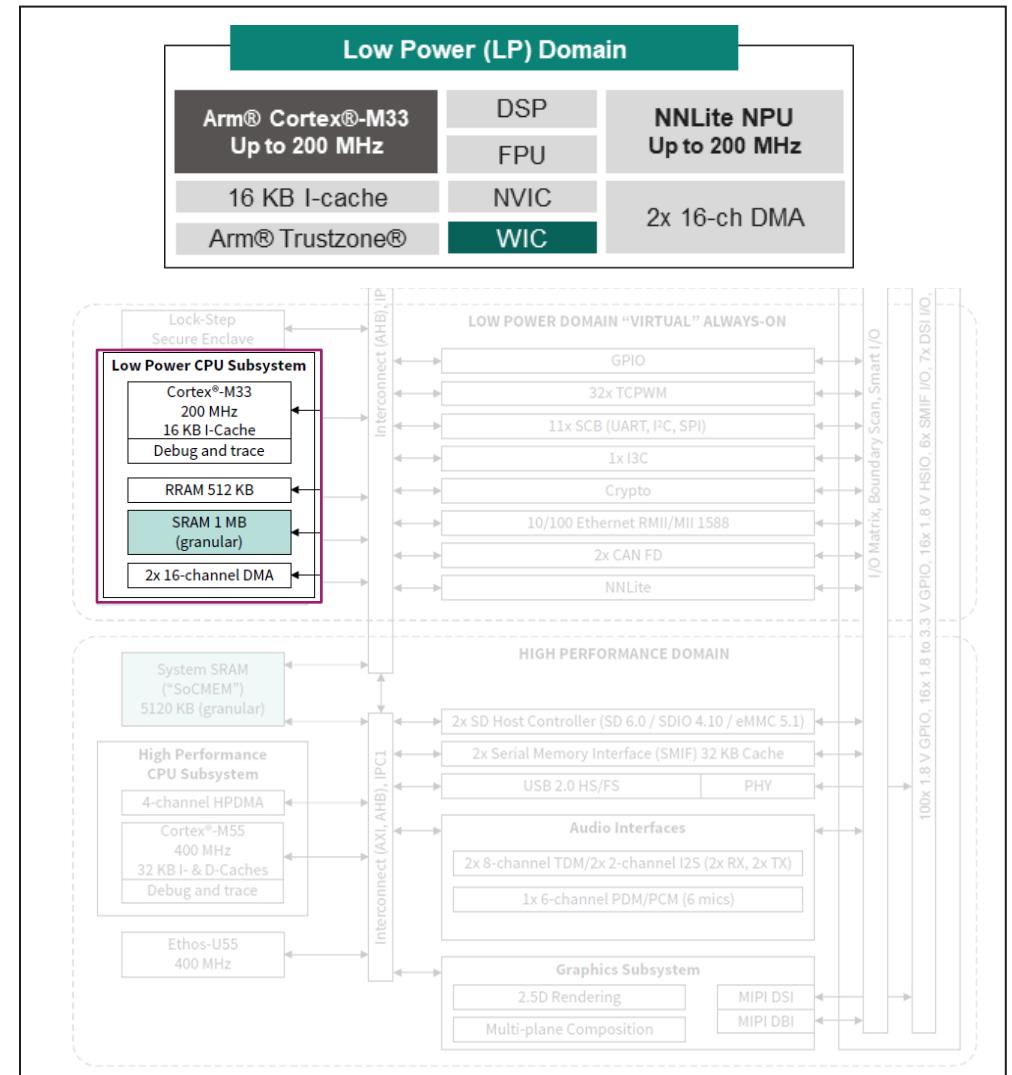
High-performance CPU subsystem: More features

- Arm® Ethos™-U55 NPU co-processor
 - Runs at same the frequency as Cortex®-M55
 - Supports 128 multiply and accumulate operations (MACs) per clock cycle
 - Used for processing voice input in speech recognition
 - Supports dense, convolutional, and recurrent neural networks
- High-performance Direct Memory Access (HPDMA) with four channels
- Multi-AXI high-bandwidth interconnect
- Inter-processor communication (IPC) is used for resource sharing and synchronization with another CPU subsystem
- Can access resources in the low-power domain via a bus bridge over the system interconnect



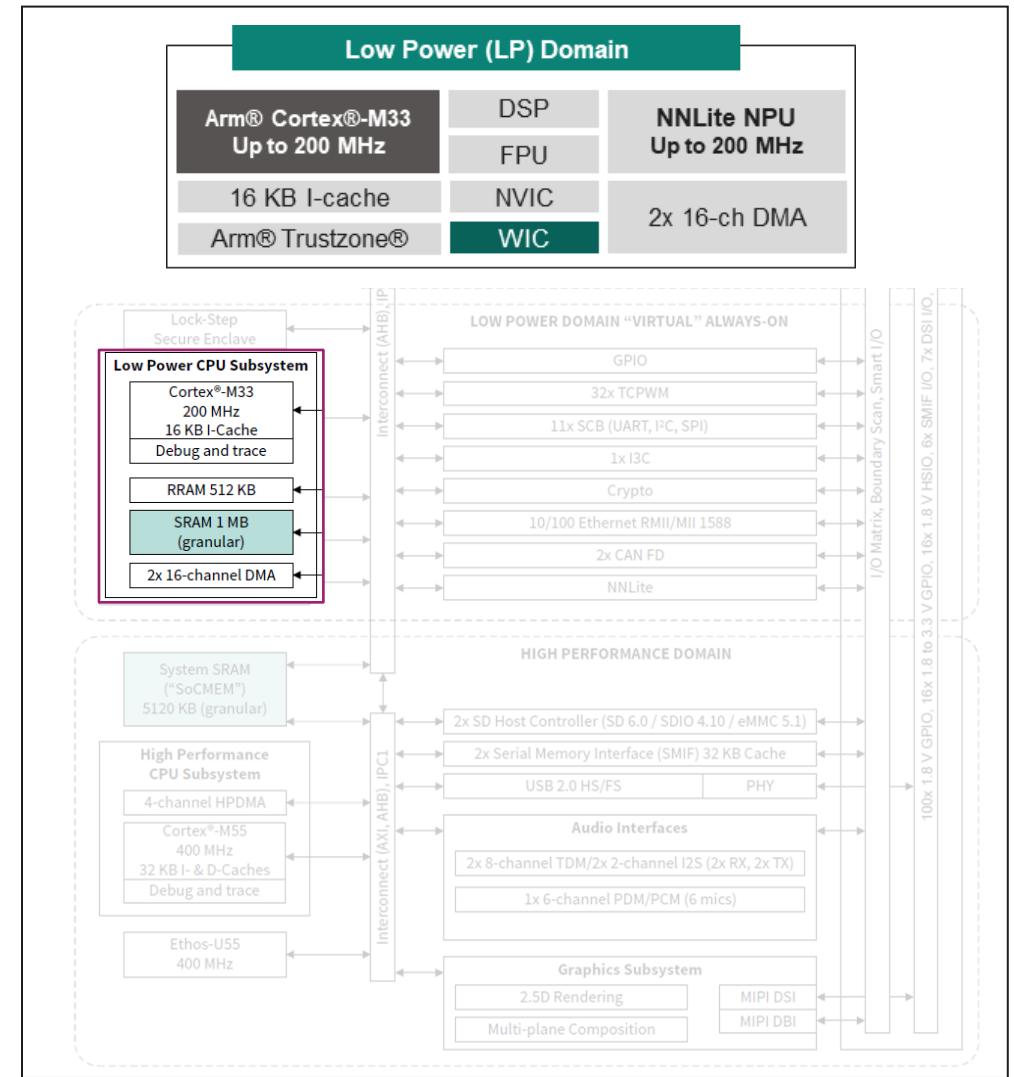
Low-power CPU subsystem: Cortex®-M33 CPU

- Runs at up to 200 MHz in system HP power mode
- Supports Arm® TrustZone®, and secure and non-secure processing environments (SPE, NSPE)
- Floating point unit (FPU), and DSP extension
- Nested Vectored Interrupt Controller (NVIC)
 - 480 interrupts; configurable priority levels: 8 to 256
 - Non-Maskable Interrupt (NMI)
- Wake-up Interrupt Controller (WIC)
- Programming and debug support
 - SWD and JTAG
 - Trace capability: 8-bit ITM, ETM interfaces with ETB and TPIU
 - Micro Trace Buffer (MTB) with 8-KB trace SRAM
- 16 KB I-cache
- Ultra-low-power consumption



Low-power CPU subsystem: More features

- NNLite co-processor running at the same frequency as Cortex®-M33
 - Optimized for machine learning model: wake-up word detect (WWD)
 - Supports 4 MACs per clock cycle
 - Supports dense/1D/2D convolutional neural networks
- 512 KB RRAM module for NVM
 - A portion can be used for EEPROM emulation
- 1 MB SRAM
 - 64 KB granularity for SRAM retention in System Deep Sleep power mode
- Two low-power DMA controllers with 16 channels each
 - A single transfer engine for all channels, that arbitrates for bus master access



System resources: Clocks

Two internal clock sources

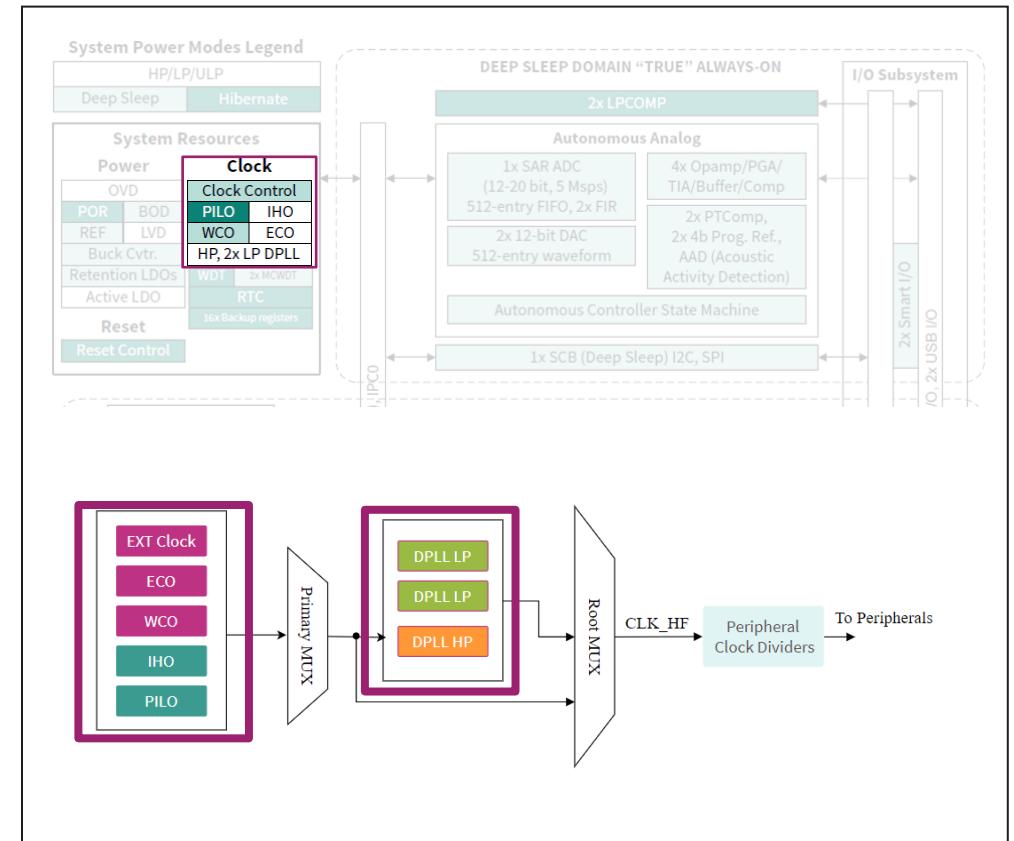
- Internal high-speed oscillator (IHO) at $50\text{ MHz} \pm 1\%$
- Precision internal low-speed oscillator (PILO):
 - $32.768\text{ kHz} \pm 250\text{ ppm}$ (with calibration)

Three external clock sources

- External crystal oscillator (ECO): 4-38 MHz
- Watch crystal oscillator (WCO): 32.768 kHz
- External clock input: up to 100 MHz

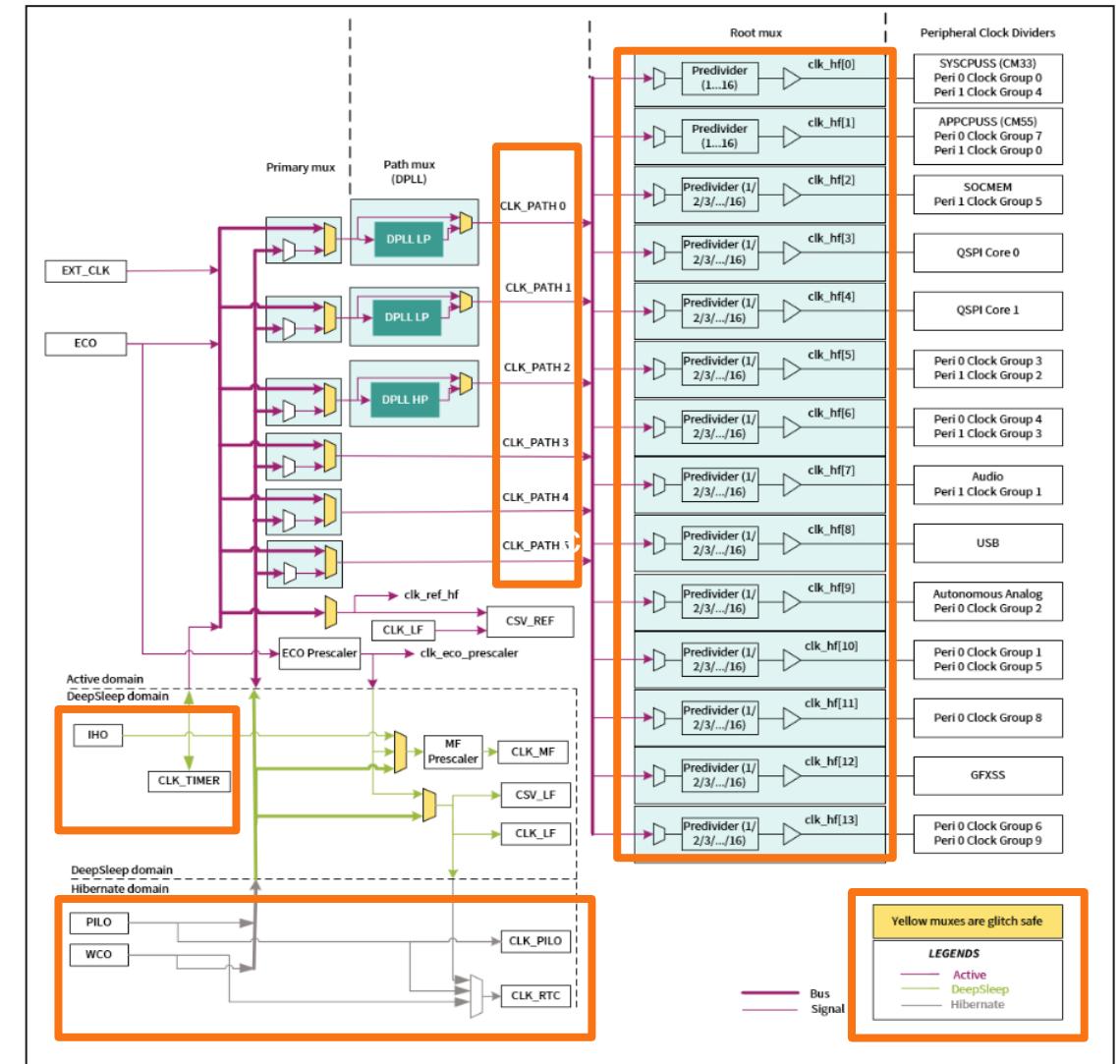
Three digital phase-locked loops (DPLL)

- Two lower-frequency low-power (DPLL LP) up to 500 MHz
- One high-frequency high-performance (DPLL HP) up to 500 MHz



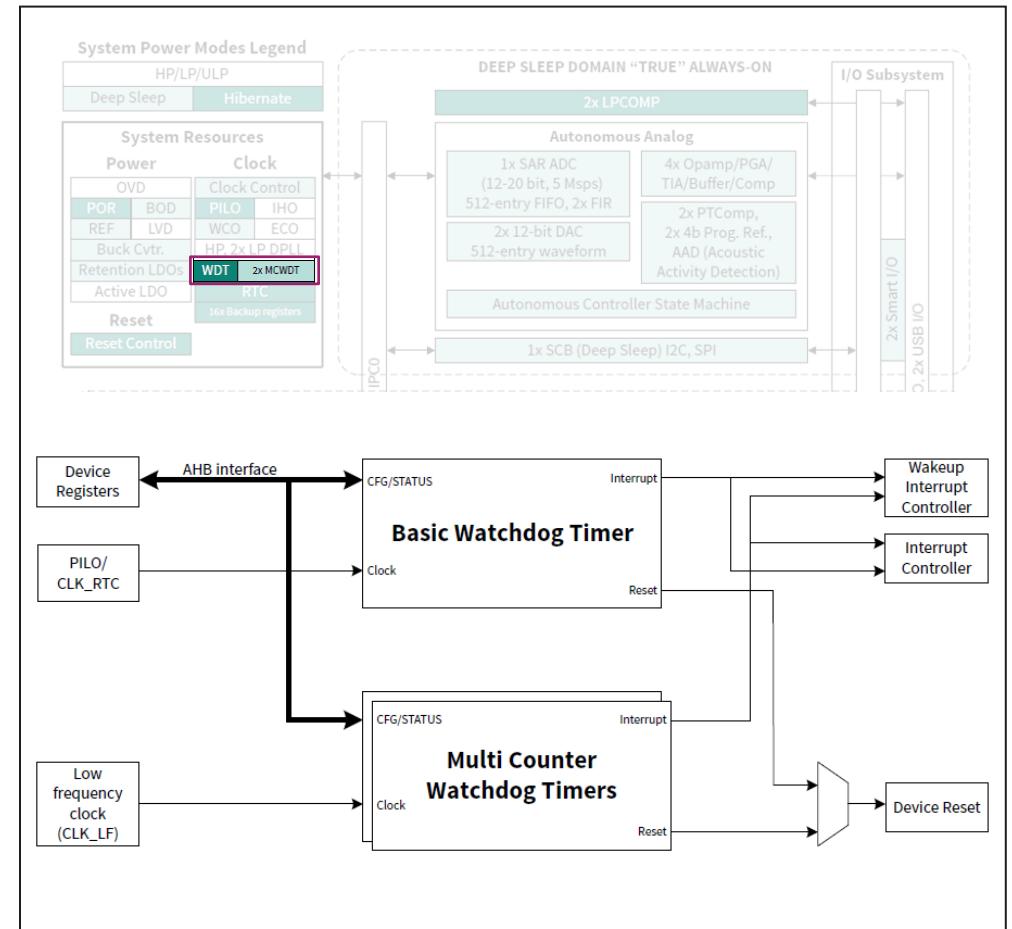
System resources: Clock tree

- Six path clocks
 - CLK_PATH0.... CLK_PATH5
- Fourteen high-frequency root clocks (CLK_HF)
 - CLK_HF0....CLK_HF13
- Low-frequency clock options
 - PILO, WCO
- Timer clock: fixed 1 MHz derived from IHO
- Peripheral clock dividers
 - Fourteen 8-bit integer
 - Five 16-bit integer
 - Six 16.5-bit fractional (16 integer bits, five fractional bits)
 - One 24.5-bit fractional (24 integer bits, five fractional bits)



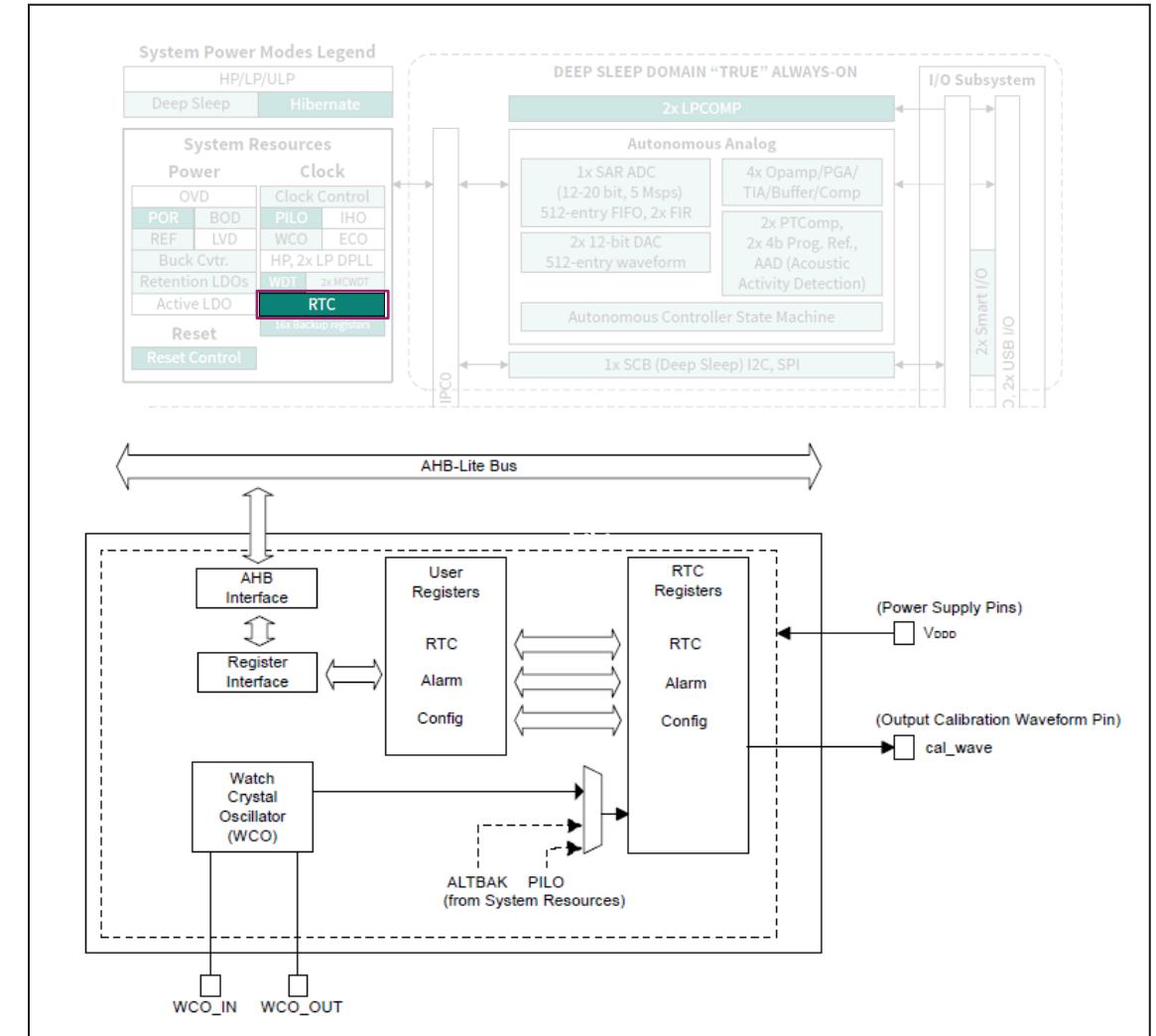
System resources: Watchdog timers

- Watchdog timers are used for:
 - Monitoring firmware execution or hardware issue, with device reset
 - Interrupt or wake-up source
- PSOC™ Edge has two types of watchdog timers:
 - 1x free-running WDT
 - Clocked by PILO or CLK_RTC (PILO/WCO)
 - Recommended for firmware monitoring
 - Can be used to generate periodic interrupts
 - 2x multi-counter WDT (MCWDT)
 - Clocked by CLK_LF (PILO/WCO/ECO)
 - Recommended for periodic interrupts or wakeups
 - Can be used for firmware protection



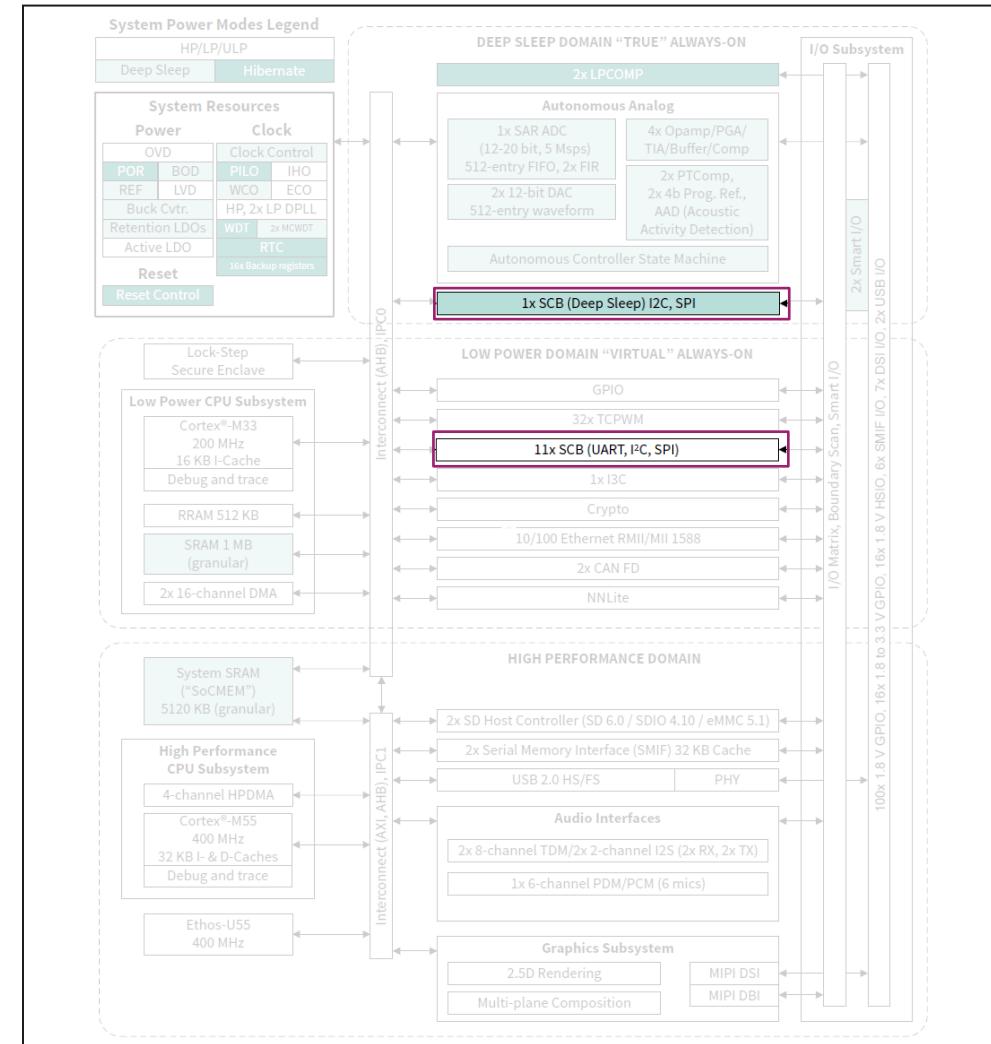
System resources: Real-time clock (RTC)

- Year, month, date, day-of-week, hour, minute, second
(integer fields only)
- 12-hour and 24-hour formats
- Automatic leap year correction
- Two alarms
 - Alarm on month, date, day-of-week, hour, minute, second
 - Generates wakeup interrupts
- Always on function, supplied by VDDD
- Clock source:
 - WCO
 - ALTBKA (CLK_LF)
 - PILO
- WCO calibration – absolute accuracy calibration



Serial communication block (SCB)

- 12 SCBs, three protocols: SPI, UART, I2C
- SCB0 supports only I2C slave and SPI slave mode in System Deep Sleep power mode
 - Wakeup on I2C slave address match or SPI slave selection
- Each SCB has a 256-byte FIFO for receive (Rx) and transmit (Tx)
- Trigger outputs for connection to DMA
- Multiple interrupt sources to indicate status of FIFOs and transfers
- Local loop-back control

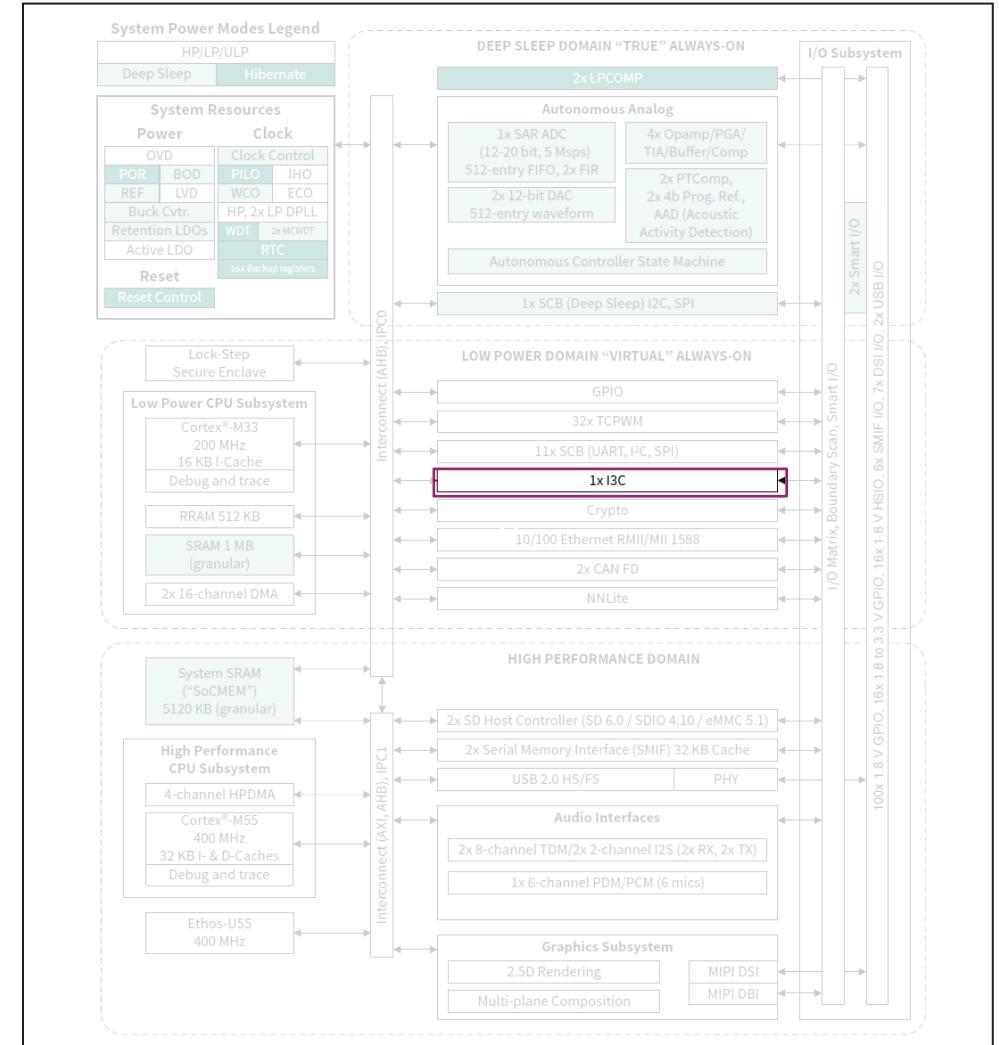


SCB protocols

UART	Serial peripheral interface (SPI)	Inter-Integrated Circuit (I2C)
<ul style="list-style-type: none"> - Standard UART - Multi-processor mode - Smart card (ISO7816) reader - IrDA - Local Interconnect Network (LIN) <ul style="list-style-type: none"> - Break detection - Baud rate detection - Collision detection - Data frame size: 4 to 16 bits - Programmable number of STOP bits - Parity support - Programmable oversampling - Start skipping - Hardware flow control 	<ul style="list-style-type: none"> - Master and slave - Three protocols: Motorola SPI, Texas Instruments SPI, National Semiconductor MicroWire - Up to four slave select lines (master) - Configurable polarity - Slave select can be programmed to stay active for a whole transfer, or just for each byte - Late sampling for better timing margin (master) - Continuous SPI clock (master) - Data frame size: 4 bits to 32 bits - Variable SELECT output signal timing (master) - Parity support - Interrupts or polling CPU interface - Programmable oversampling - MSB or LSB first - Median filter available for inputs - Supports FIFO mode, EZ mode (slave), and CMD_RESP mode (slave) - Deep Sleep wake-up on slave selection (SCB0 only) - Local loop-back control 	<ul style="list-style-type: none"> - Master, slave, and master-slave functionality - Standard mode (100 kHz), fast mode (400 kHz), and fast plus mode (1 MHz) - 7-bit and 10-bit addressing - Multi-master modes and bus arbitration - Clock stretching - Collision detection - Programmable oversampling of SCL - Auto ACK when RX FIFO not full, including address - General call address detection - FIFO Mode, EZ, and CMD_RESP modes - Deep Sleep wake-up on slave address match (SCB0 only)

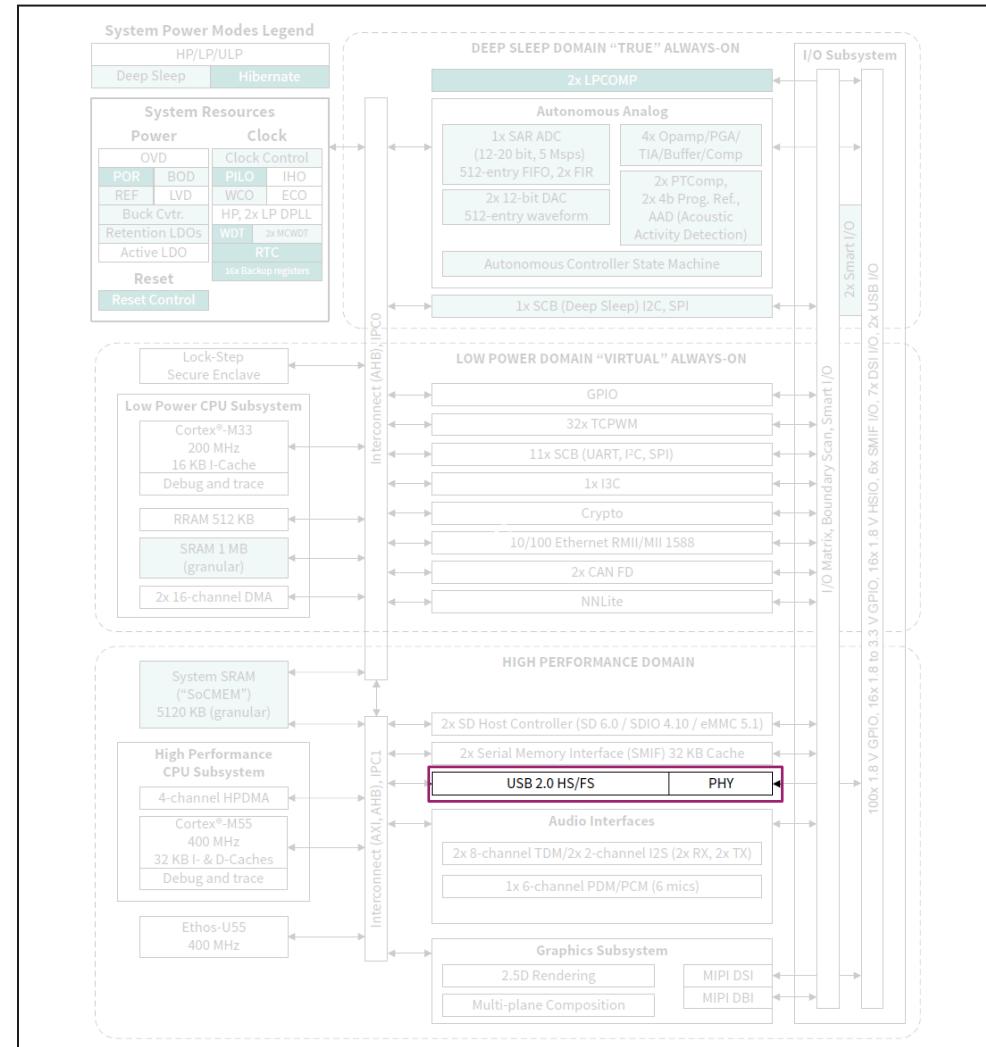
Improved Inter-Integrated Circuit (I3C)

- Designed to address limitation of I2C
- Provides low-cost, low-power, fast digital signals
- Supported modes:
 - Primary controller
 - Secondary controller
 - Target
- SCL frequency up to 12.5 MHz (SDR data rate 12.5 Mbps, HDR-DDR data rate at 25 Mbps)
- In-band interrupts (IBI)
- Dynamic address allocation (DAA)
- Hot-join capability
- Device characteristics register (DCR)
- Common command code (CCC)
- Controller mode allows addressing up to 11 target devices
- Error detection of CE0, CE2, CE3, and TE0 to TE5
- SRAM 1 KB (256x32-bit) for command/response queues and transmit/receive data buffers
- Backward compatible with I2C
 - Legacy I2C devices using FM or FM+ with 50-ns spike filter



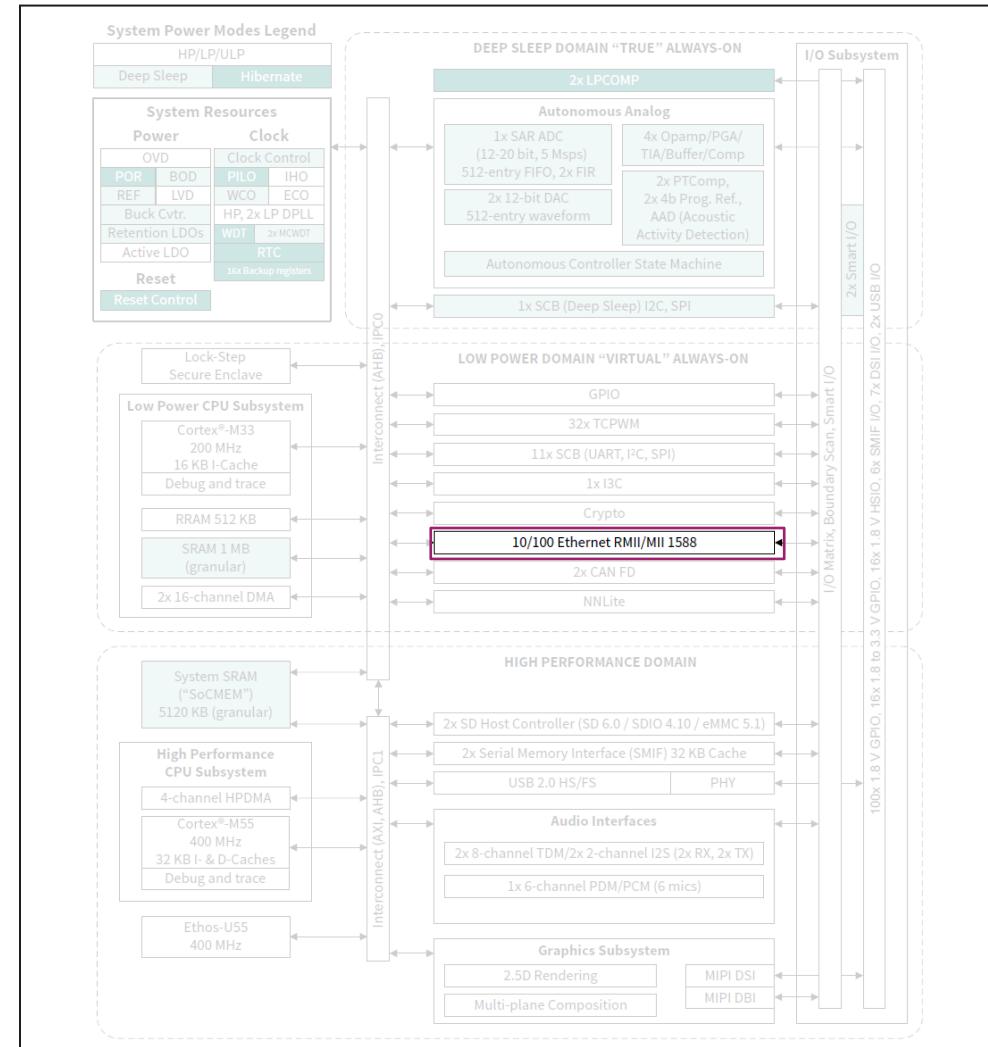
USB HS

- Complies with USB 2.0 specification
- Can be configured as USB host or USB device (one at a time)
- Supports the following speed modes:
 - High-Speed (HS): 480 Mbps
 - Full-Speed (FS): 12 Mbps
 - Low-Speed (LS): 1.5 Mbps (only as host)
- Supports up to 9 bidirectional endpoints, one control endpoint and eight data endpoints
- Supports up to 16 host channels
- Supports all four types of USB data transfers (control, bulk, isochronous, and interrupt)
- Includes a dedicated Scatter-Gather DMA interface to avoid using CPU for packet transfers
- Includes a 6912×35-KB SRAM buffer for both Host and Device mode operations
- Supports high-bandwidth multimedia, isochronous data transfers that can store up to 3*1 KB packet per endpoint
- Supports remote wakeup, host, or device-initiated resumes
- Supports Link Power Management (LPM) suspend and sleep modes



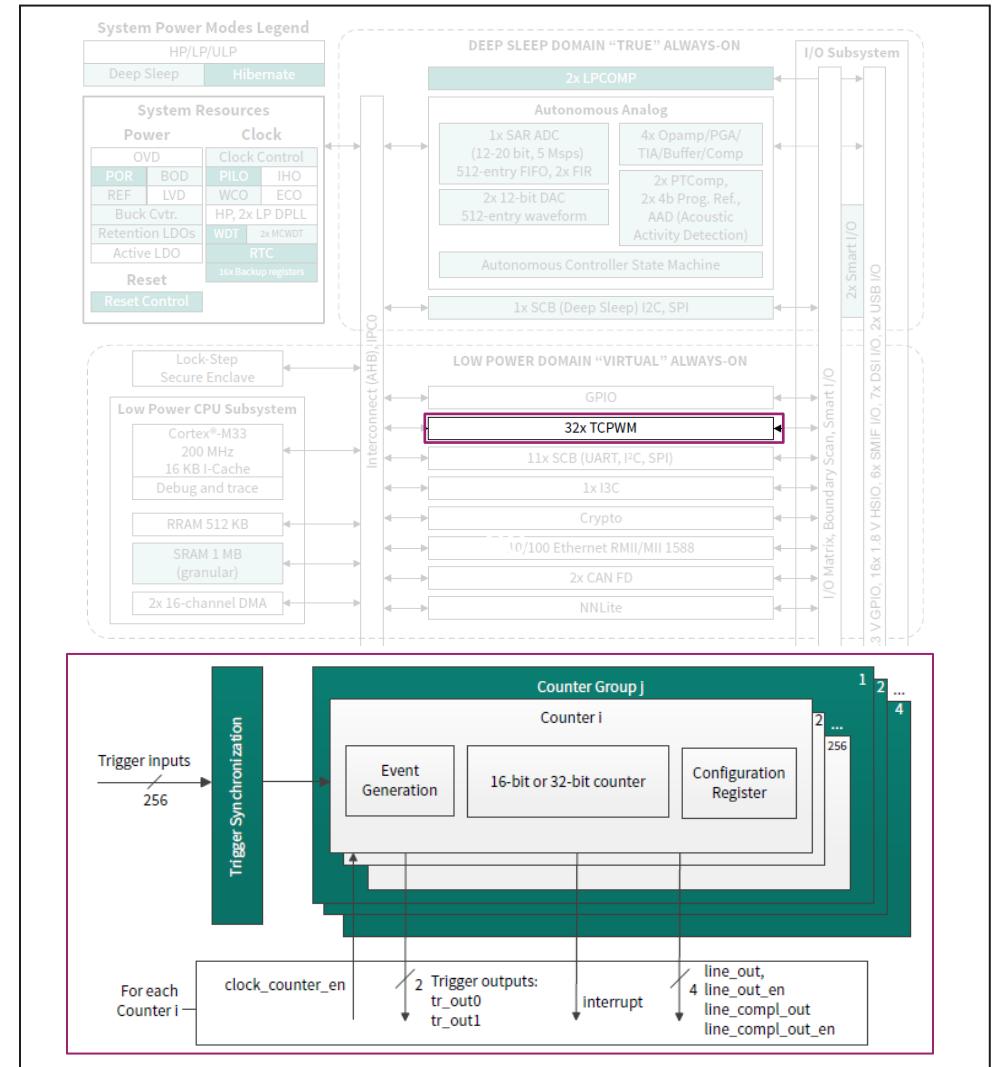
Ethernet

- 10 Mbps or 100 Mbps operation
- MII and RMII PHY interface modes
- Full store and forward modes
- 1536 bytes of maximum frame length
- 8 KB TX and 4 KB RX package buffer
- AHB DMA Master Interface
- MDIO interface for PHY management
- Automatic pad and CRC generation on transmitted frames
- Timing, prioritization, energy:
 - IEEE Std 802.1Qav
 - IEEE Std 802.1AS
 - IEEE Std 1588
 - IEEE Std 802.1Qbb
 - IEEE 802.3 Pause frame and MAC PFC priority-based pause frame support
 - Strict priority, DWRR, or enhanced transmission selection (ETS – 802.1Qaz) on transmit queues
 - 802.3az EEE



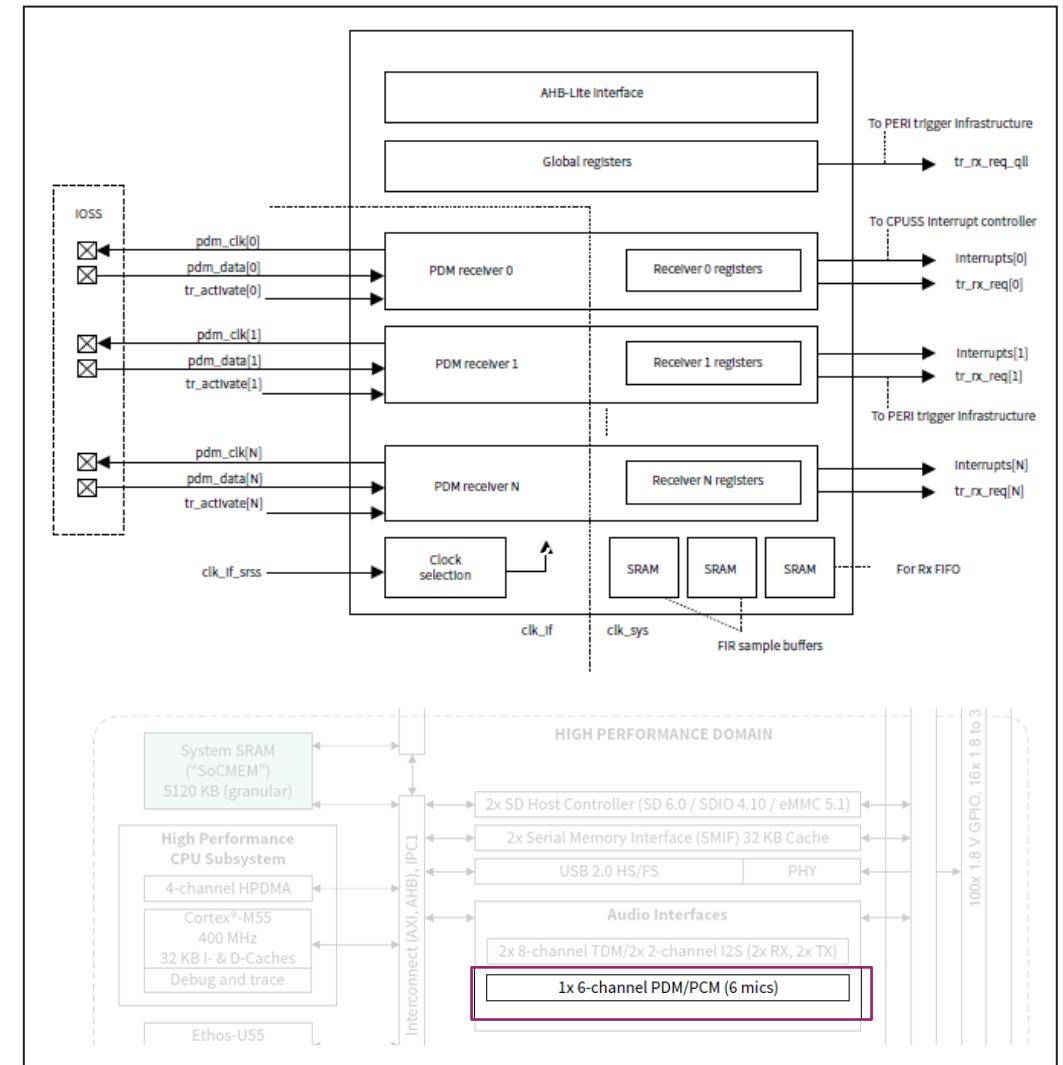
TCPWM

- 32 Timer, counter, and pulse width modulator (TCPWM) blocks.
 - Eight have 32-bit counters
 - 24 have 16-bit counters
- Modes:
 - Timer-counter with compare
 - Timer-counter with capture
 - Quadrature decoding
 - PWM / stepper motor control (SMC)
 - PWM with dead time / three-phase motor control (BLDC)
 - Pseudorandom PWM
 - Shift-register mode
- Up, down, and up/down counting modes
- Clock prescaling (division by 1, 2, ... 64, 128)
- Double-buffering of all compare/capture and period registers
- Each counter supports up to 28 synchronized input trigger signals
- Two type of input triggers for each counter:
 - General-purpose trigger used by all counters
 - One-to-one triggers for specific counters
- Synchronous operation of multiple counters



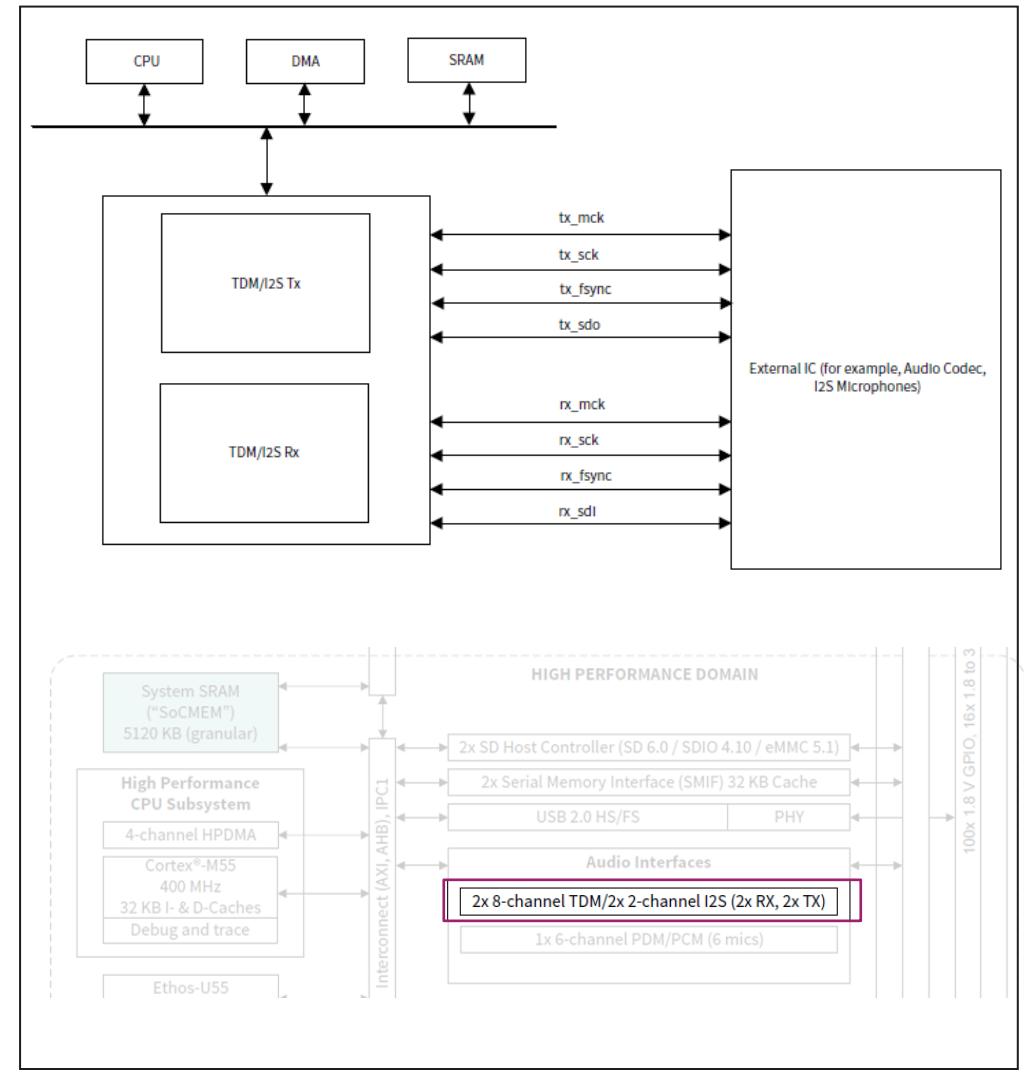
PDM-PCM converter

- Supports up to 6 PDM receivers in mono and stereo configurations
- Programmable filtering options including CIC filter, FIR filter, DC blocking
- Supports standard sampling rates: 8, 16, 32, 44.1, and 48 KHz
- Programmable PCM sample size 8, 10, 12, 14, 16, 18, 20, 24, and 32 bits
- Programmable sampling delay to cope with different master-slave-master round-trip delays
- 64-entry RX FIFO with interrupt and trigger support
- Common data path implementation with SRAM, FIR filter, and DC blocking filter logic shared by all PDM receivers
- Half-rate sampling to reduce system power consumption



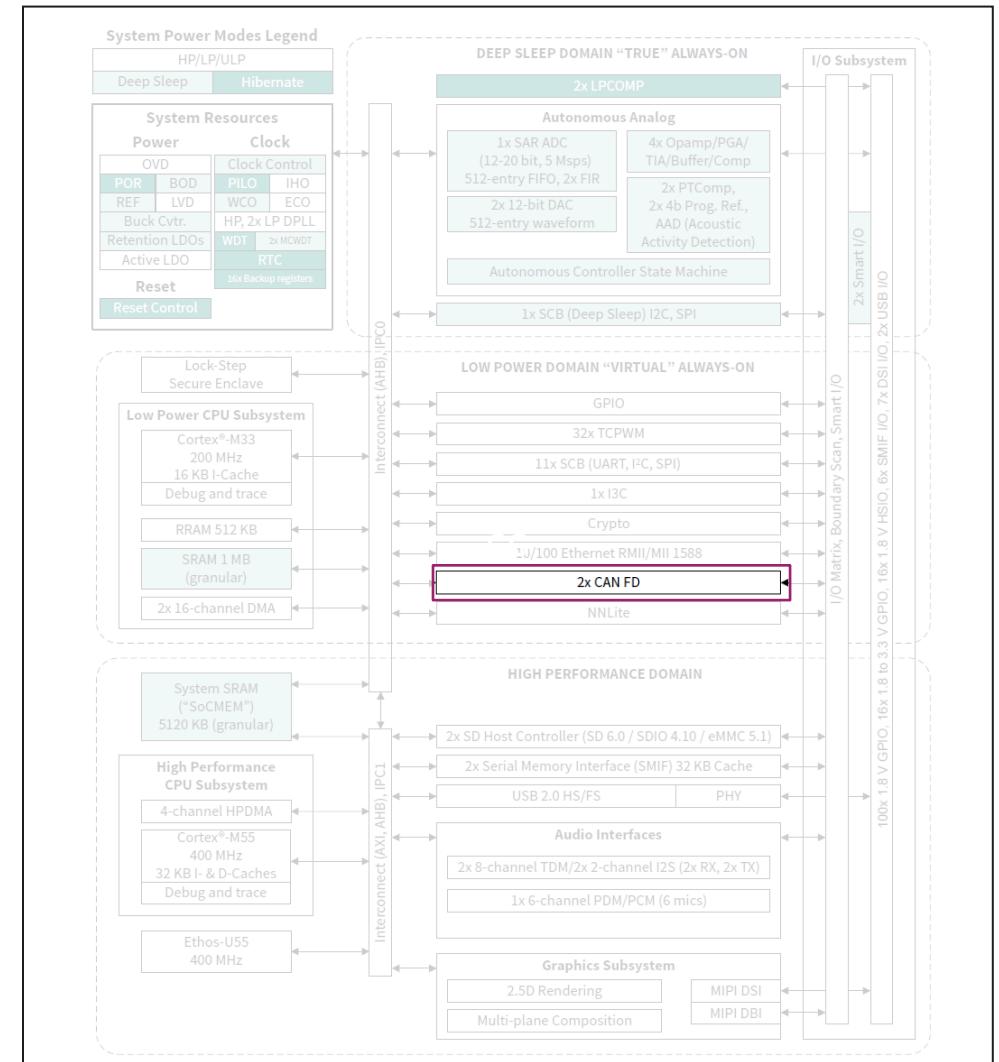
TDM/I2S

- Supports 8-channel TDM and standard Philips I2S digital audio interface formats
- Supports full-duplex and half-duplex transmitter and receiver operation
- Both transmitter and receiver support master and slave functionality
- Supports operating from an external master clock provided through an external IC such as audio codec
- Provides individual configurable clock dividers for transmitter and receiver to generate the required sample rates
- Programmable channel length of up to 32 bits
- Supports PCM sample length / PCM data word length of 8, 10, 12, 14, 16, 18, 20, 24, and 32 bits per channel
- Provides hardware FIFO buffers of 128 data words for the TX and RX blocks
- Supports all common sampling frequencies: 4, 8, 11.025, 12, 16, 20, 22.05, 24, 30, 32, 40, 44.1, 48, 60, and 96 kHz
- Supports transmitter to receiver loop back
- Supports both DMA- and CPU-based data transfers



CAN FD

- Flexible data-rate (FD) (ISO 11898-1: 2015)
 - Up to 64 data bytes per message
 - Supports maximum 8 Mbps
- Shared message 8-KB RAM
- Time-triggered (TT) communication on CAN (ISO 11898-4: 2004)
- AUTOSAR support
- Acceptance filtering
- Two channels, where each channel includes:
 - Up to 64 dedicated receive buffers per channel
 - Two configurable receive FIFOs (up to 64 buffers each) with acceptance filters
 - Up to 32 dedicated transmit buffers
 - Configurable transmit FIFO
 - Configurable transmit queue
 - Configurable transmit event FIFO
- Programmable loop-back test mode
- Power-down support
- Enables DMA access on the FIFO
- DMA for debug message and received FIFOs
- Shared-time stamp counter

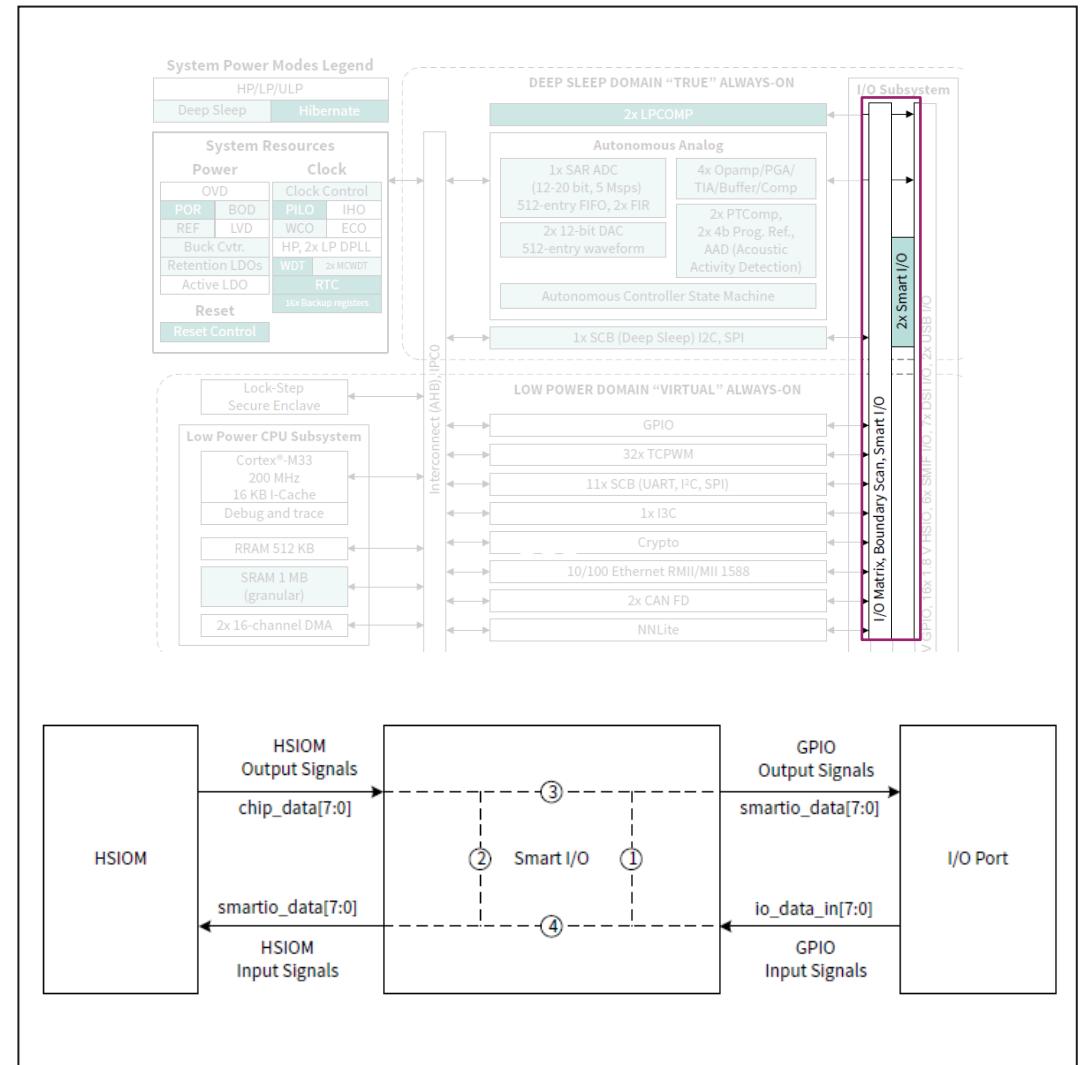


Smart I/O

Smart I/O is a component of the I/O subsystem that enhances I/O signal functionality, with following capabilities:

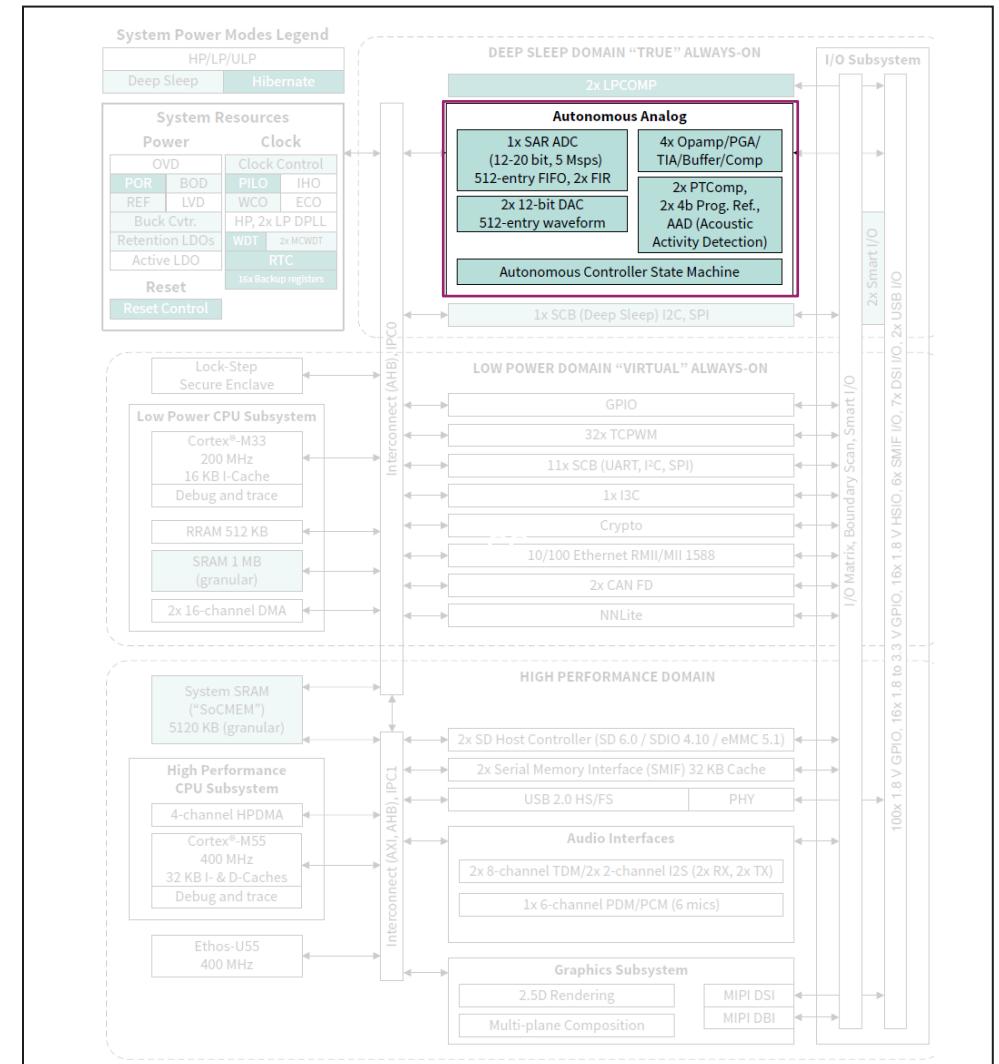
- Integrate board-level boolean logic functionality into a port
- Ability to preprocess HSIOM input signals from the GPIO port pins
- Ability to post-process HSIOM output signals to the GPIO port pins
- Support in all device power modes except Hibernate
- Integrate closely to the I/O pads, providing shortest signal paths with programmability
- Two dedicated ports equipped with Smart I/O

- Examples include:
 - Invert a GPIO
 - Ramping LED
 - Glitch filter
 - Mux/demux
 - Repeater, and so on



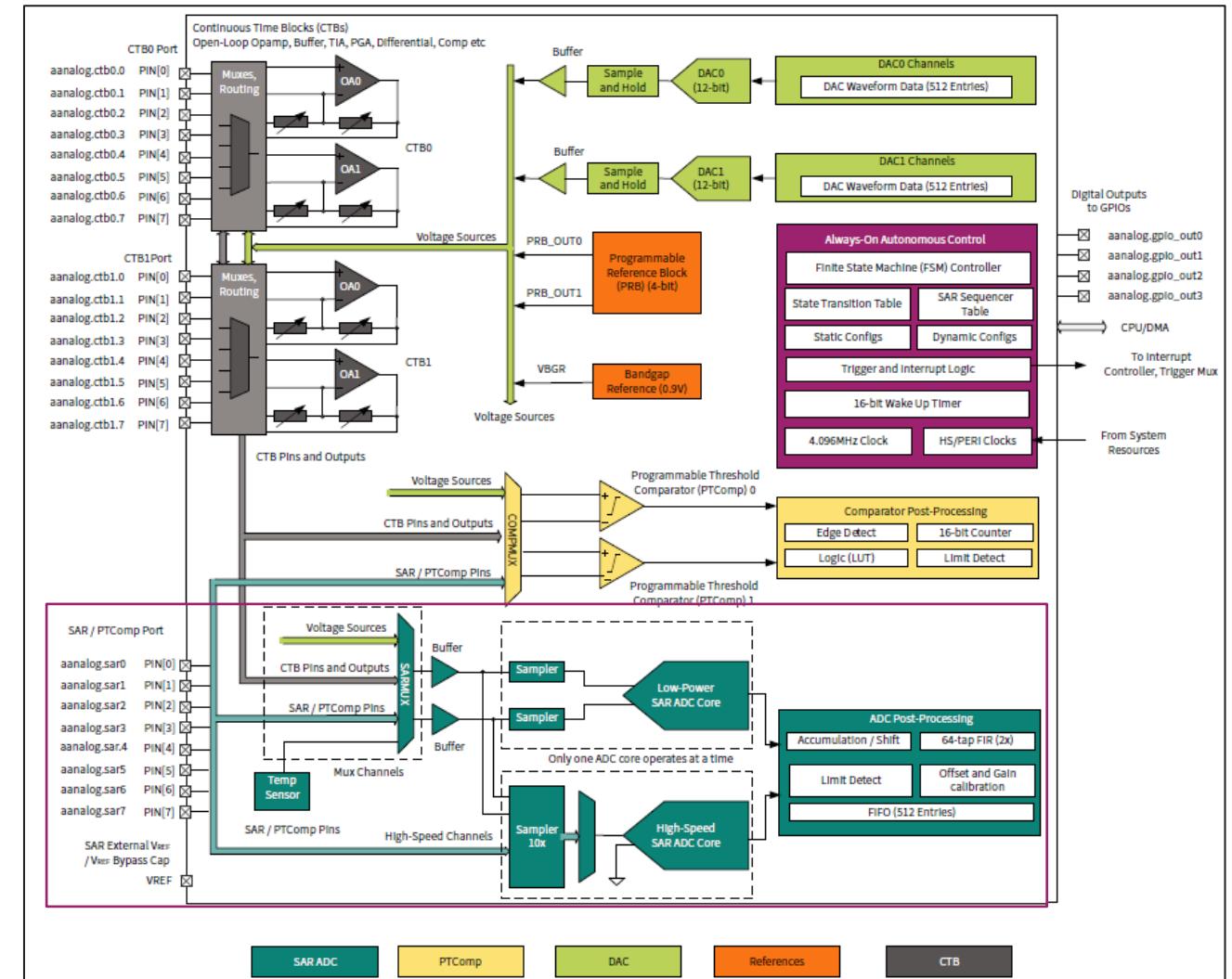
Autonomous analog

- Always-on (Deep Sleep capable) mixed-signal peripherals
- CPU-independent decision making
- The subsystem includes:
 - SAR ADC
 - CTB opamp circuits
 - ADC digital post processing
 - DACs with waveform generation
 - Programmable threshold comparators (PTComp)
 - Programmable reference blocks



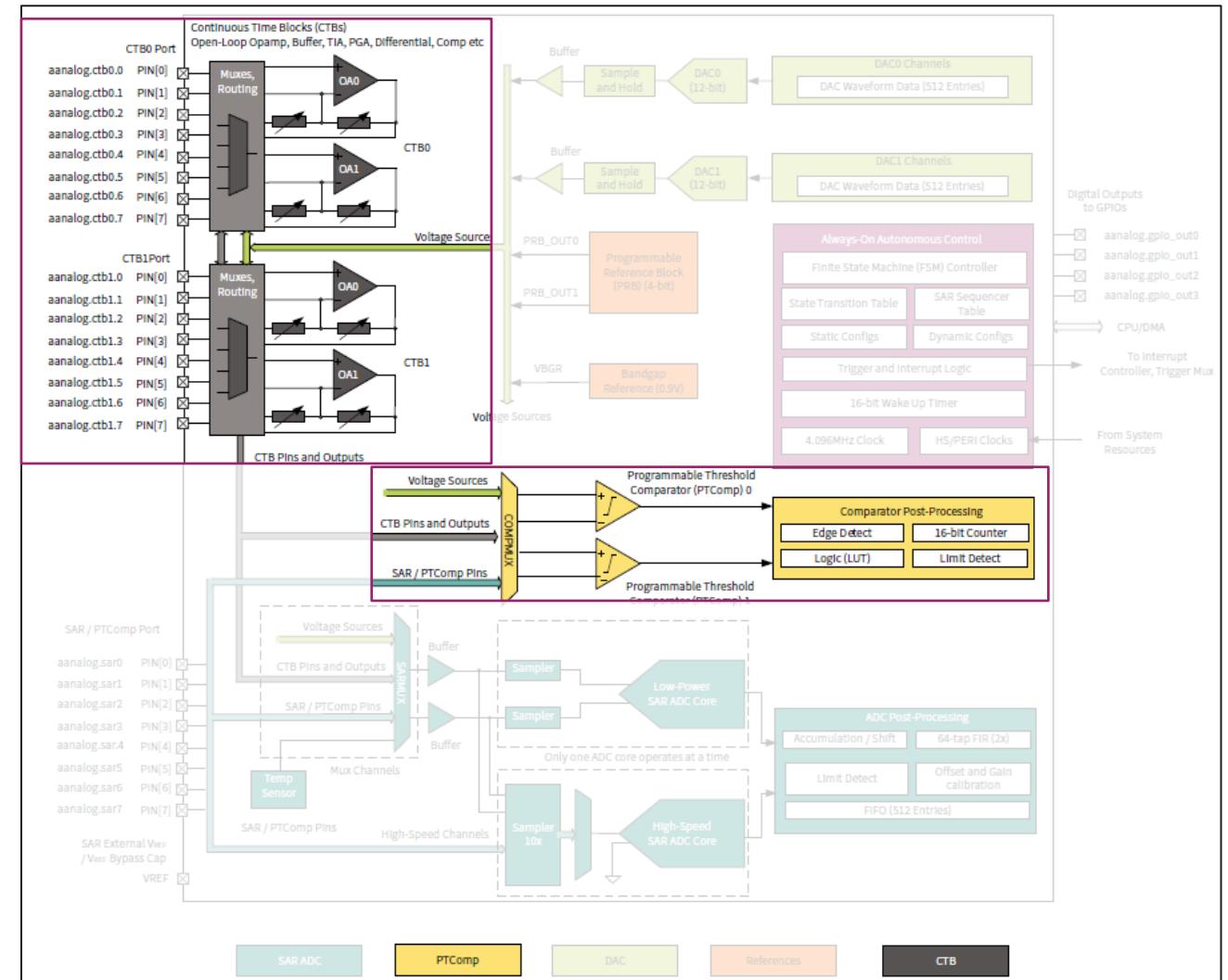
Autonomous analog: SAR ADC

- One SAR ADC with
 - 12- to 20-bit (with accumulation) results
 - 5-Msps sample rate at 12 bits or 250 ksps at 16 bits in System High Performance mode
 - 200-ksps sample rate at 12 bits or 12.5 ksps at 16 bits in System Deep Sleep mode
- Buffered Inputs
 - Inputs from 16 pins or 7 internal signals (from opamps, DACs, temperature sensor, and so on)
 - Simultaneous sampling of as many as 10 inputs
 - 32 logical channels
- Post processing and storage
 - Accumulation and averaging – 2x, 4x, 8x ... 256x
 - Two 64-tap FIR filters
 - A 512-entry FIFO that can be subdivided into 2, 4, or 8 FIFOs
 - Limit detection
 - Offset and gain calibration



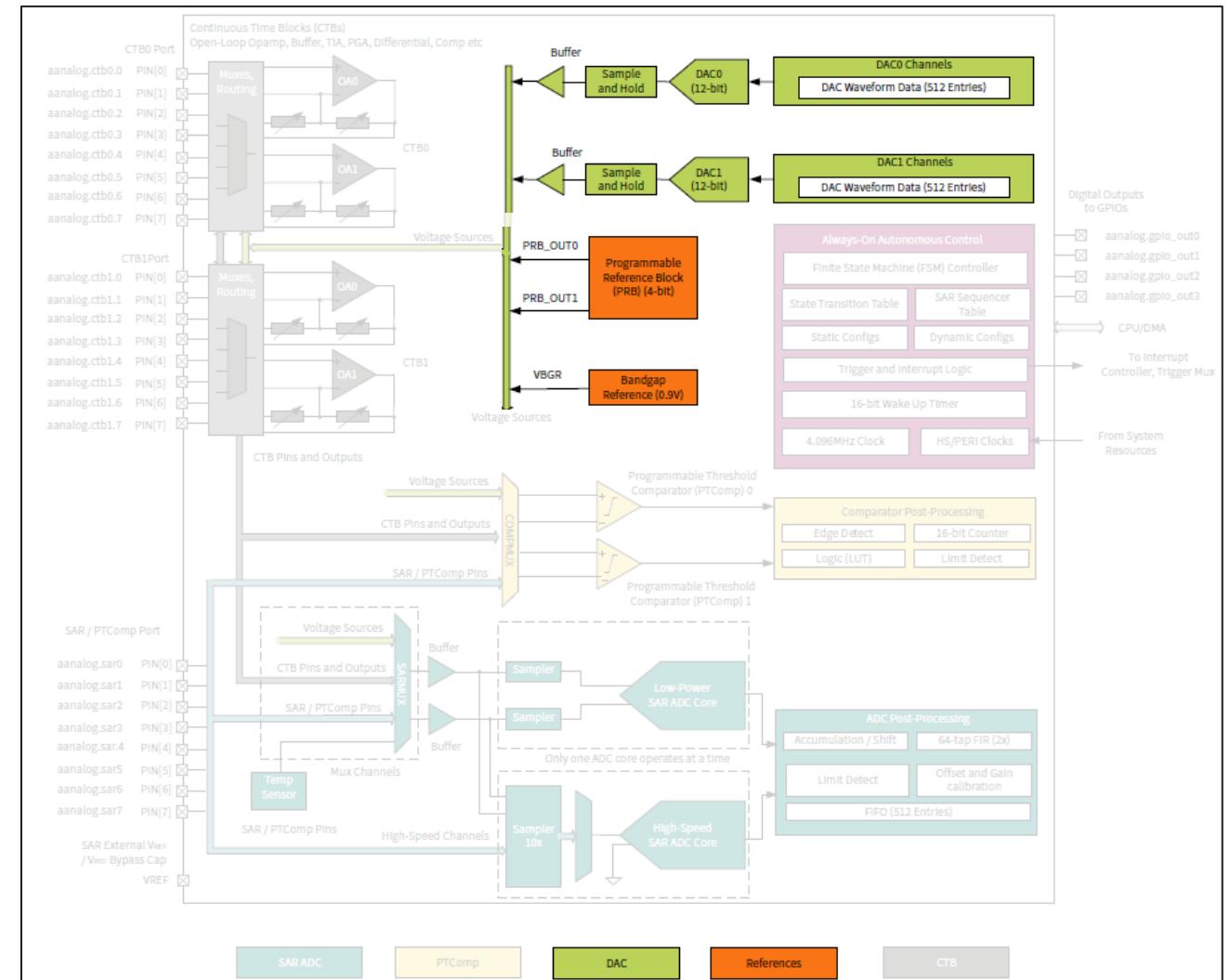
Autonomous analog: CTBs and PTComps

- Two 12-bit digital-to-analog converters (DACs) supporting:
 - 1- μ s refresh time
 - Buffered outputs (sample-and-hold capable)
 - A 512-entry waveform table
 - Automatic waveform generation
- Two 4-bit programmable reference blocks (PRB)
- Internal bandgap reference at 0.9 V



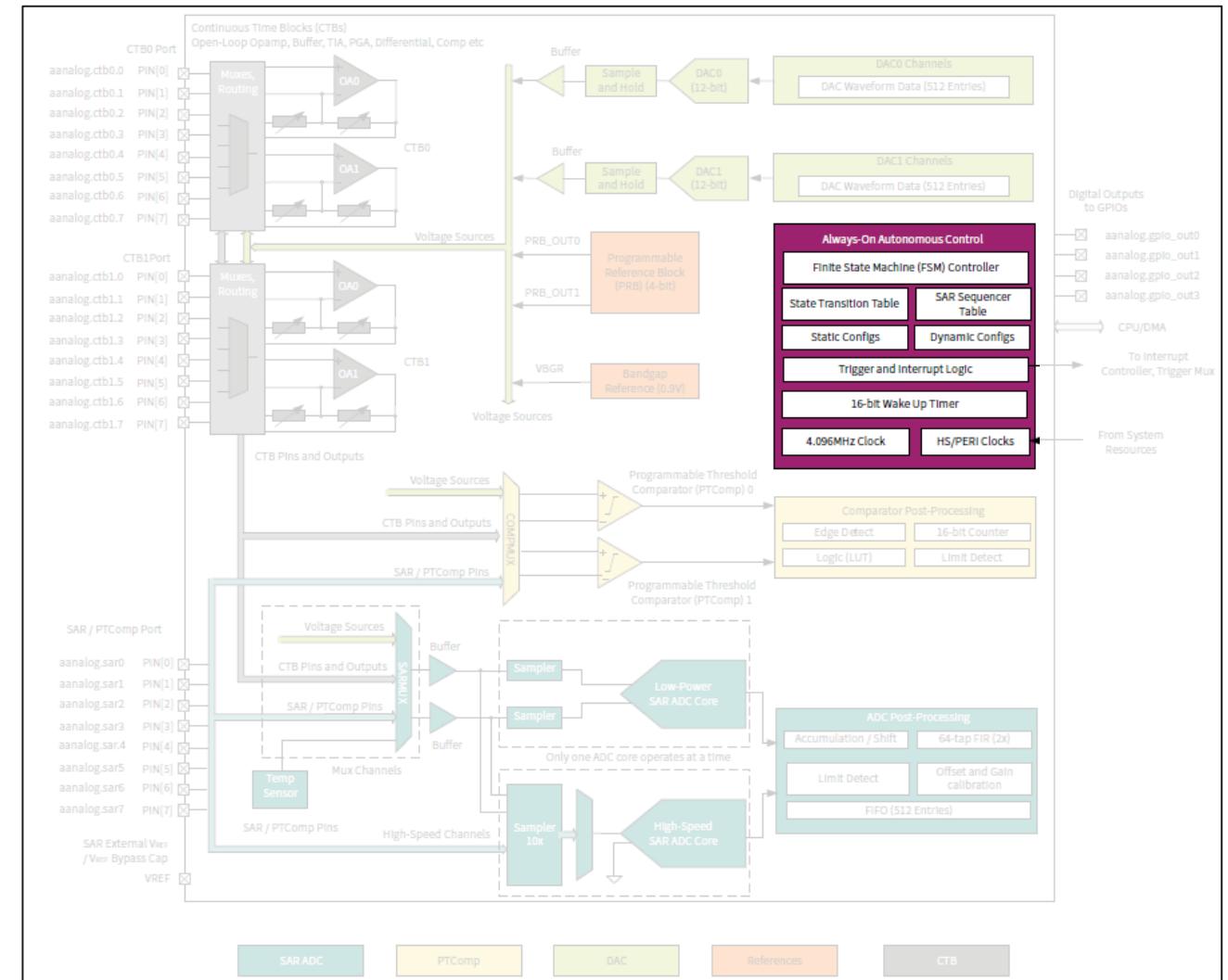
Autonomous analog: DACs and voltage references

- Two continuous-time blocks (CTBs), each consisting of two op-amp circuits that can perform analog front-end functions such as:
 - Programmable gain amplifier (PGA)
 - Transimpedance amplifier (TIA)
 - Pseudo-differential amplifier
 - Unity gain buffer (voltage follower)
 - Open loop opamp
 - Comparator
- Two programmable threshold comparators (PTComps)
 - With post-processing supporting audio activity detection (AAD) and motor control



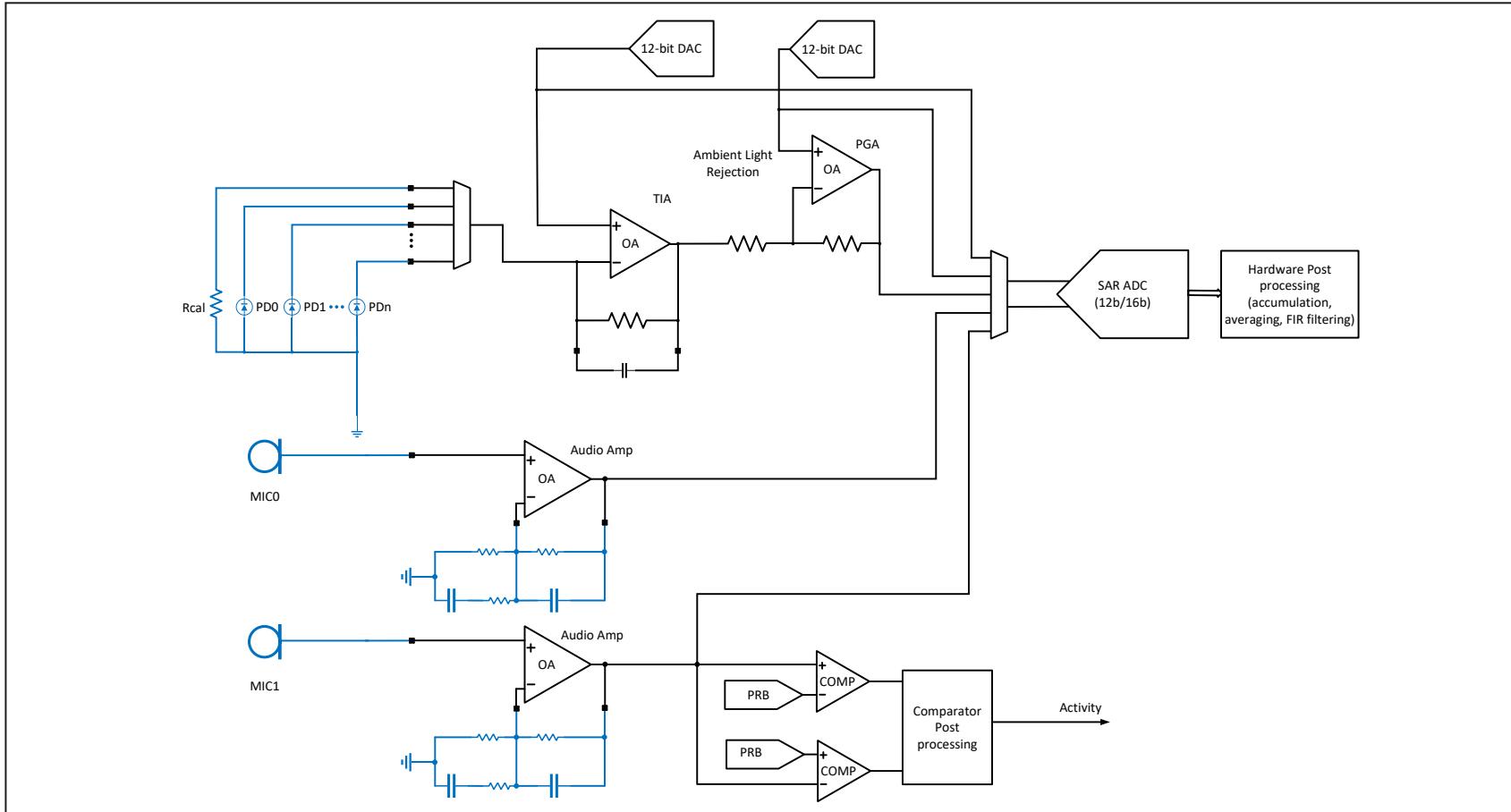
Autonomous analog: Autonomous controller

- A finite-state machine (FSM) sequencer called the autonomous controller that works with a 64-entry state transition table (STT), to transition appropriately through various pre-defined states, based on timer, and/or events
- Supports Deep Sleep mode
- Autonomous controller can perform:
 - Power cycling of individual blocks
 - Listen to/send triggers to individual blocks
 - Send triggers and/or interrupts to the CPU
 - Change the connections between blocks using dynamic configurations of individual blocks
 - Digital output to as many as four GPIOs



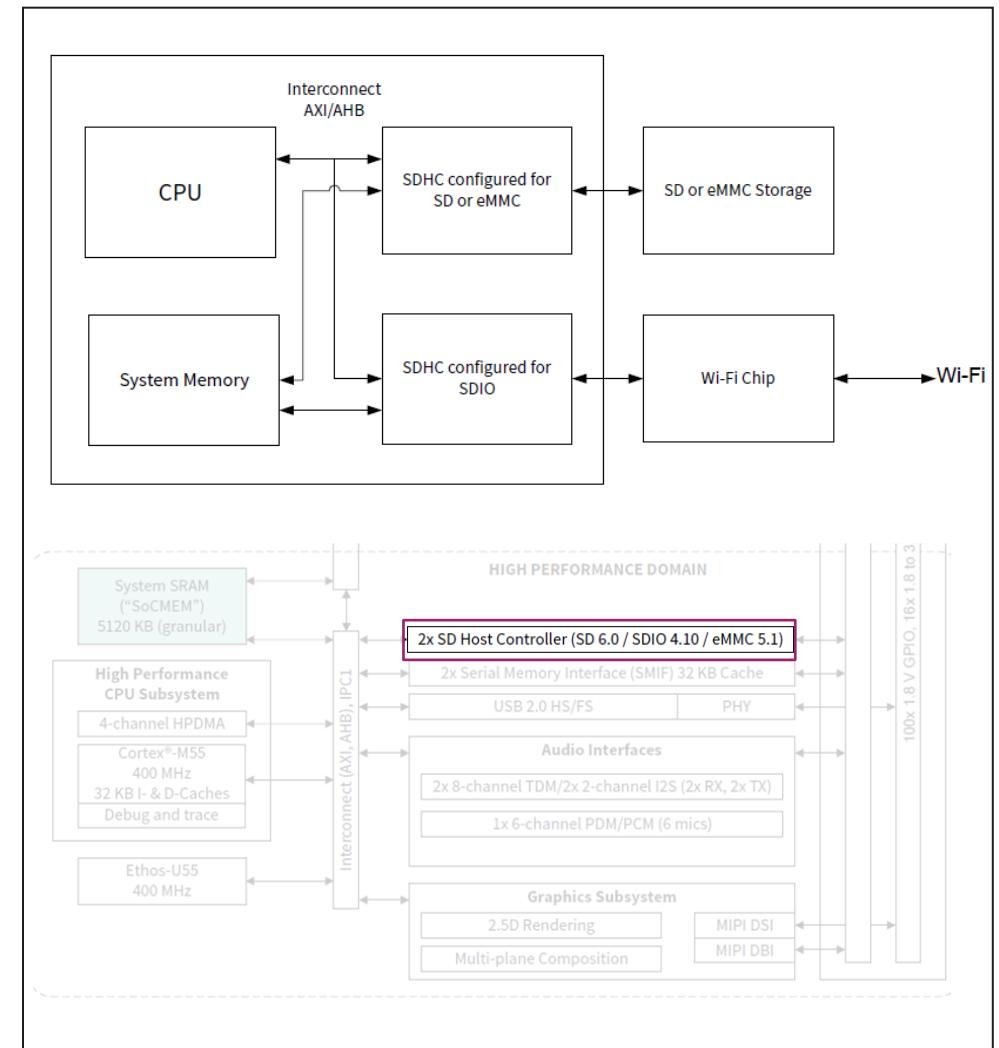
Autonomous analog: Autonomous controller application

The following is an application example for analog microphone interface with pulse detection.



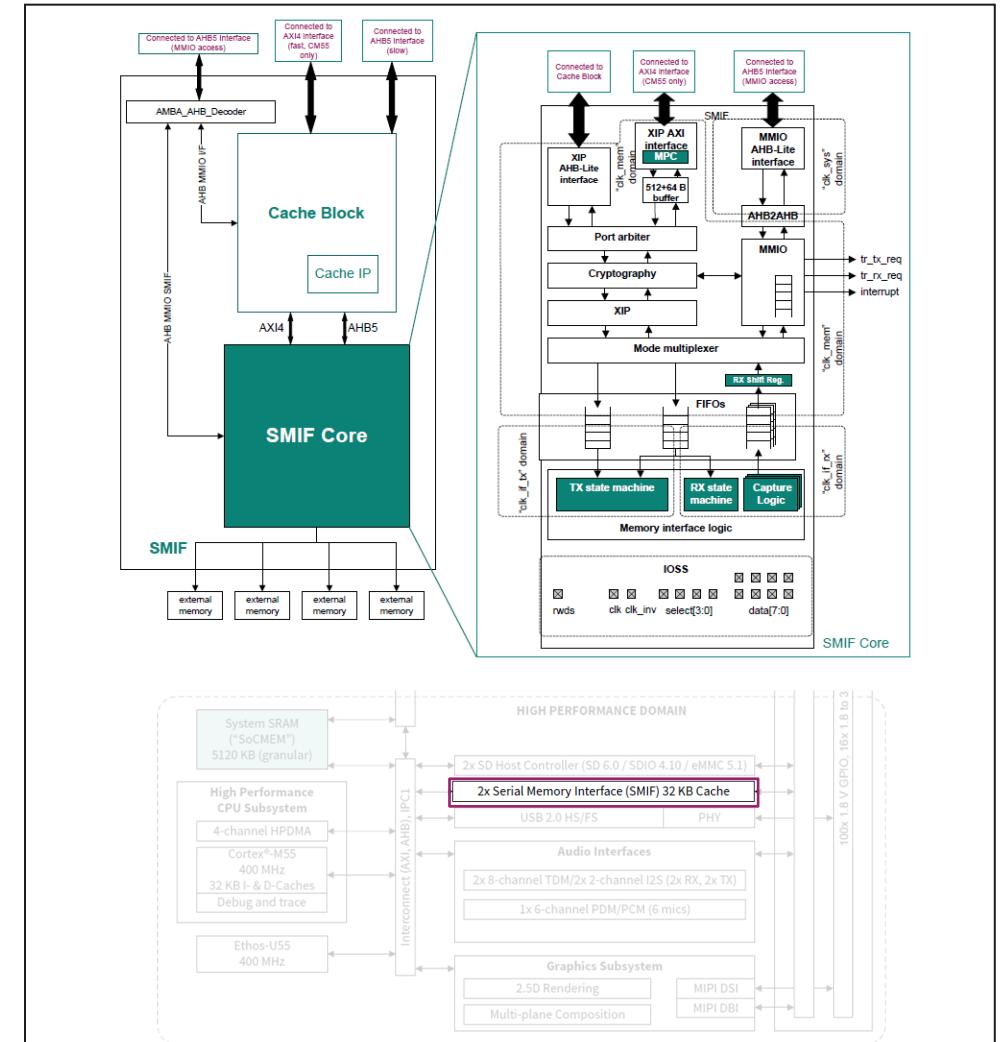
Secure Digital host controller (SDHC)

- Enables interfacing with embedded MultiMediaCards (eMMCs), Secure Digital (SD) cards, and Secure Digital Input Output (SDIO) components
- Complies with eMMC 5.1, SD 6.0, and SDIO 4.10 standards
- Supports host controller interface (HCI) 4.2 shared by eMMC and SD
- SD interface:
 - 1-bit and 4-bit bus interfaces
 - 3.3-V signal voltage: Default speed (12.5 MB/s at 25 MHz) and high-speed (25 MB/s at 50 MHz)
 - UHS-I modes using 1.8-V signal voltage : SDR12 (12.5 MB/s at 25 MHz), SDR25 (25 MB/s at 50 MHz), SDR50 (50 MB/s at 100 MHz), and DDR50 (50 MB/s at 50 MHz)
- eMMC interface:
 - 1-bit, 4-bit, and 8-bit bus interfaces
 - Legacy (26 MB/s at 26 MHz), high-speed SDR (52 MB/s at 52 MHz), and high-speed DDR (104 MB/s at 52 MHz)
- Supports three DMA modes – SDMA, ADMA2, and ADMA3
- Supports command queuing engine (CQE)
- Provides 2 KB SRAM for buffering up to two 1 KB blocks



External memories: Serial memory interface (SMIF)

- Two SMIF interfaces
- Supports four external memory devices per block
- SPI and HYPERBUS™ master functionality
- SPI
 - Single/dual/quad/octal
 - Single data rate (SDR) and dual data rate (DDR)
- Supports overall capacity in the range of 64 KB to 1 GB in power of two multiples
- Memory-mapped I/O (MMIO) operation mode
- Memory protection control (MPC) support on AXI XIP
- Execute-in-place (XIP) mode
 - Supports on-the-fly encryption/decryption
- 32 KB cache per SMIF instance
- Speeds
 - 166 MHz HYPERBUS™
 - 200 MHz Octal/xSPI DDR
 - 166 MHz SPI/xSPI SDR
 - 100 MHz SPI DDR
- Firmware update over the air (FOTA) support



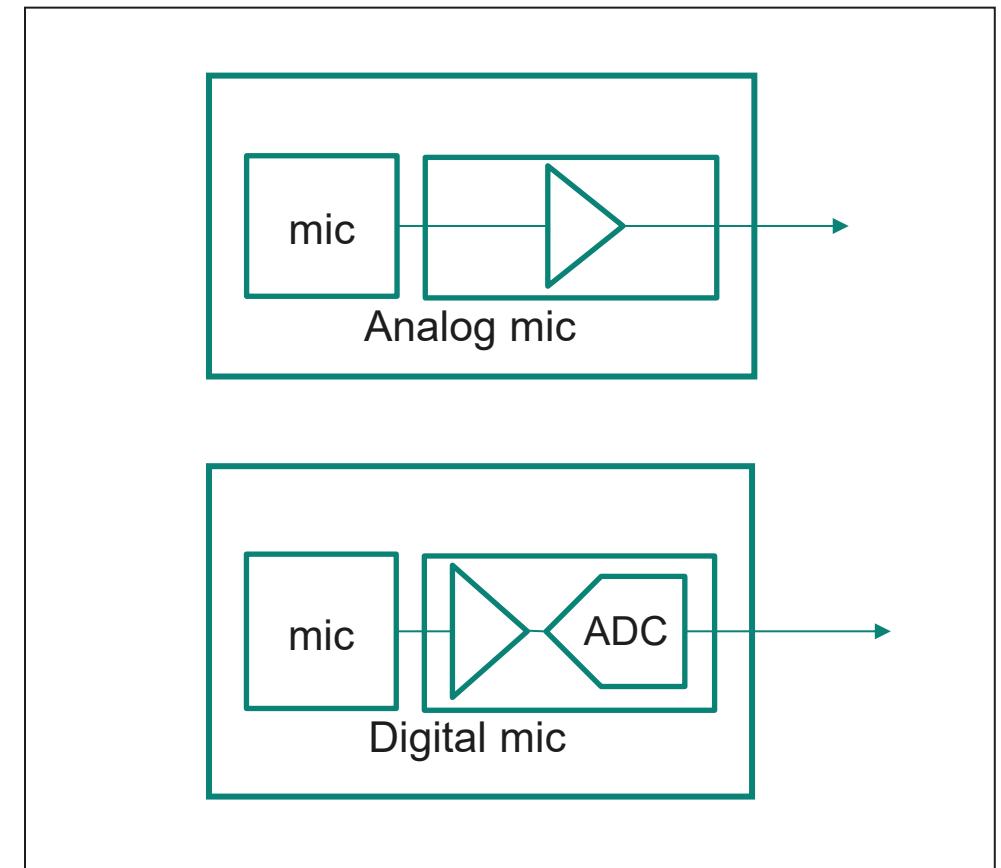
Human-machine interface: Audio

Analog mic

- Acoustic activity detect (AAD) uses low-power comparators that operate in the System Hibernate power mode
- Triggers the ADC if acoustic activity is detected
- AAD is followed by speech onset detect in the NNLite co-processor

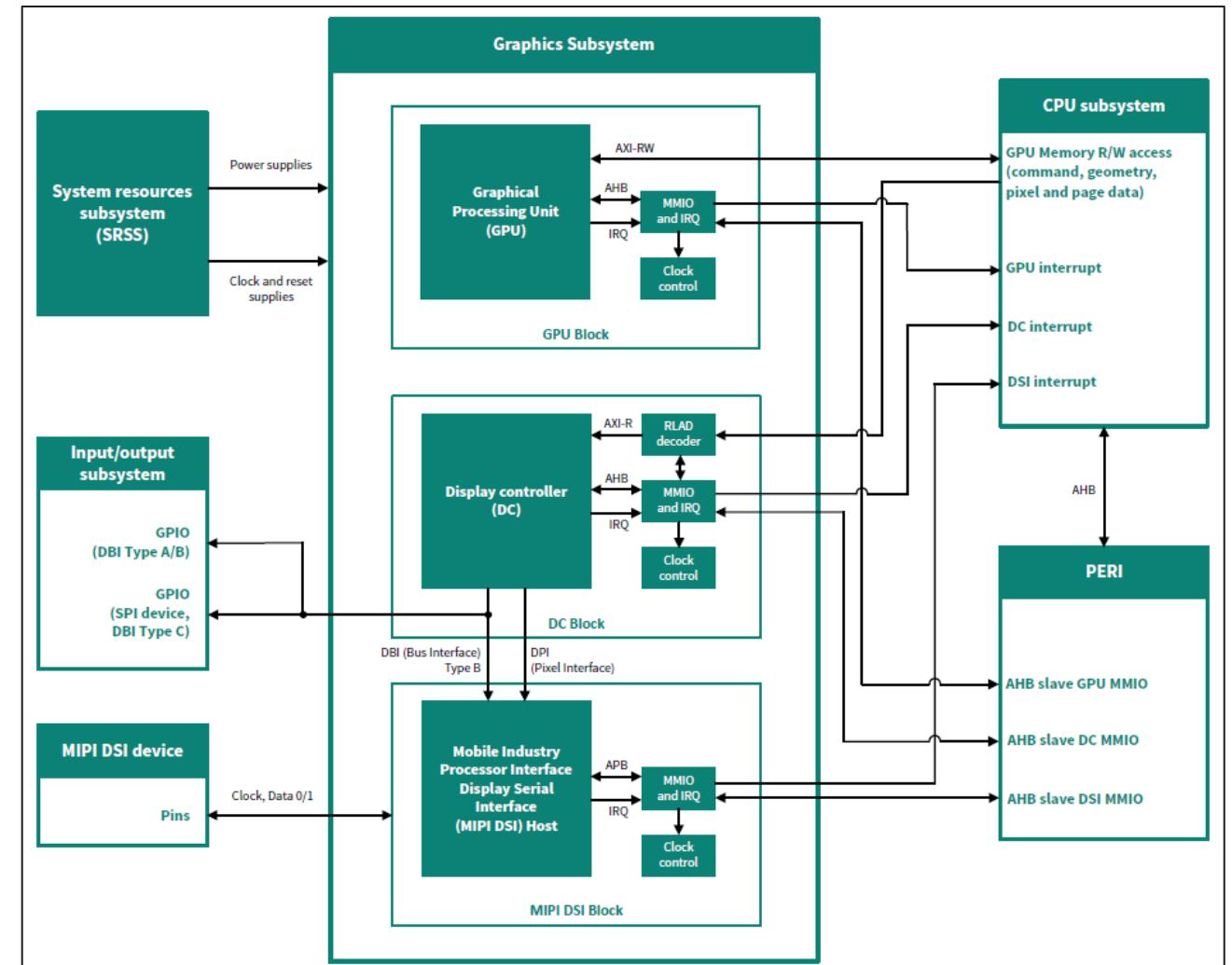
Digital mic

- Up to six microphones using PDM/PCM
- Low-power subsystem: Cortex®-M33 and NNLite
- High-performance subsystem: Cortex®-M55/Ethos™-U55



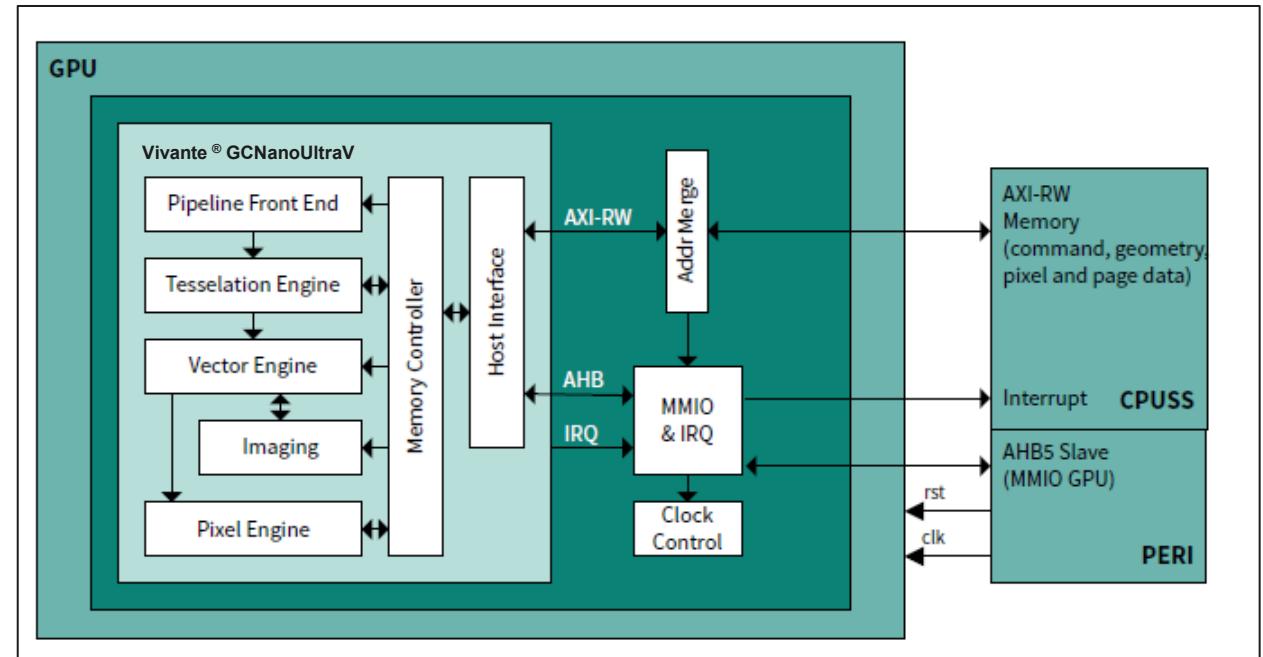
Human-machine interface: Graphics subsystem (GFXSS) overview

- Supports display sizes up to 1024×768 pixels at 60 Hz with 24-bit color resolution (all modes)
- DPI up to 64-MHz pixel clock, for example 1024×768 at 60 Hz (via MIPI-DSI)
- DBI up to 16 bits at 50 MHz (GPIO) or 37.5 MHz (MIPI-DSI)
- Independent GPU
- MIPI display compatibility
 - MIPI-DSI, D-PHY
 - MIPI Display Bus Interface (DBI) Type C, Type B
- The graphics subsystem consists of three blocks:
 - GPU block
 - Vivante® GCNanoUltraV
 - Display controller
 - Vivante® DC8000Nano
 - MIPI DSI host controller
 - Synopsys DWC MIPI DSI host controller
 - Integrated D-PHY



GPU

- Display list command processing
- 2D geometry processing with perspective correction and no depth coordinate (= 2.5D)
- Tessellation of line, quad, and Bezier curve primitives
- Vector graphics rasterization for linear and curved paths
- Textured, solid, and linear fill pattern
- Eight Porter-Duff blend modes
- Various ARGB formats for textures and destination buffers (8, 16, or 32 bpp)
- Color palette for textures (1, 2, 4, or 8 index bpp)
- Chroma sub-sampled destination buffers
(YUV 4:2:2 or 4:2:0 with 16 or 12 bpp)



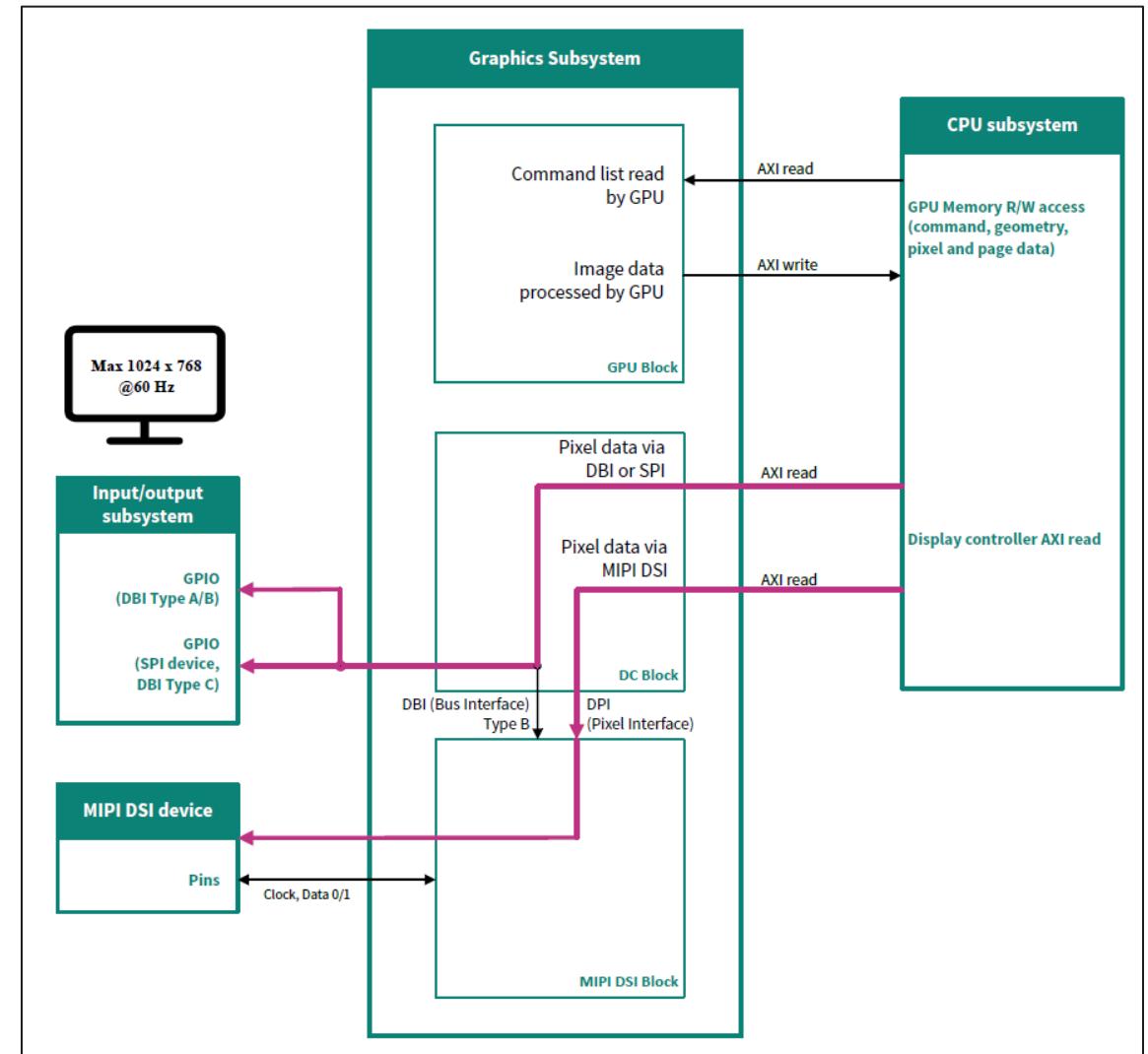
Display controller and MIPI DSI host controller

Display controller

- Fetches pixel data from memory
- Processes in pipeline
 - Cursor
 - Layering
 - Run length adaptive dithering (RLAD)
 - Outputs to different formats

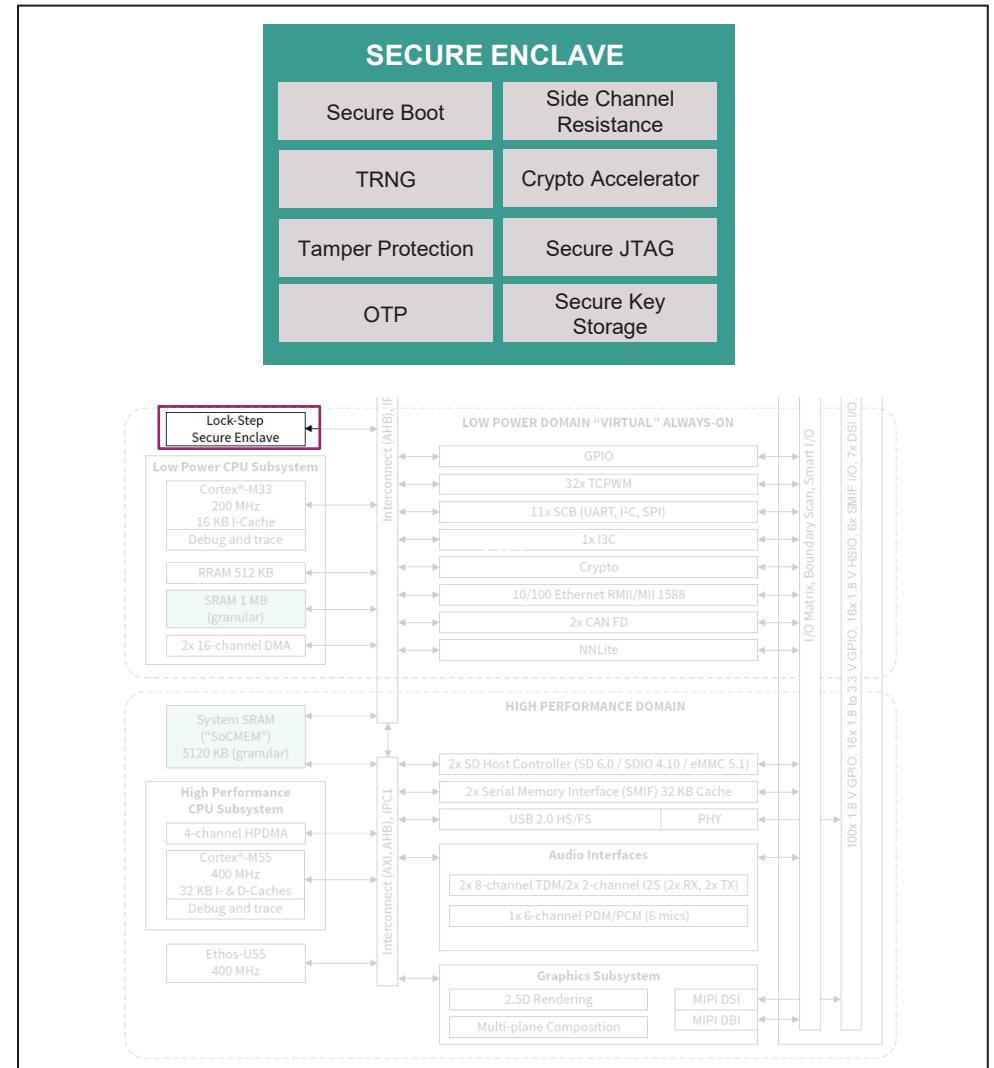
MIPI DSI host controller

- From display controller
 - DPI
 - DBI
- 2 lane MIPI DSI has dedicated pins for output

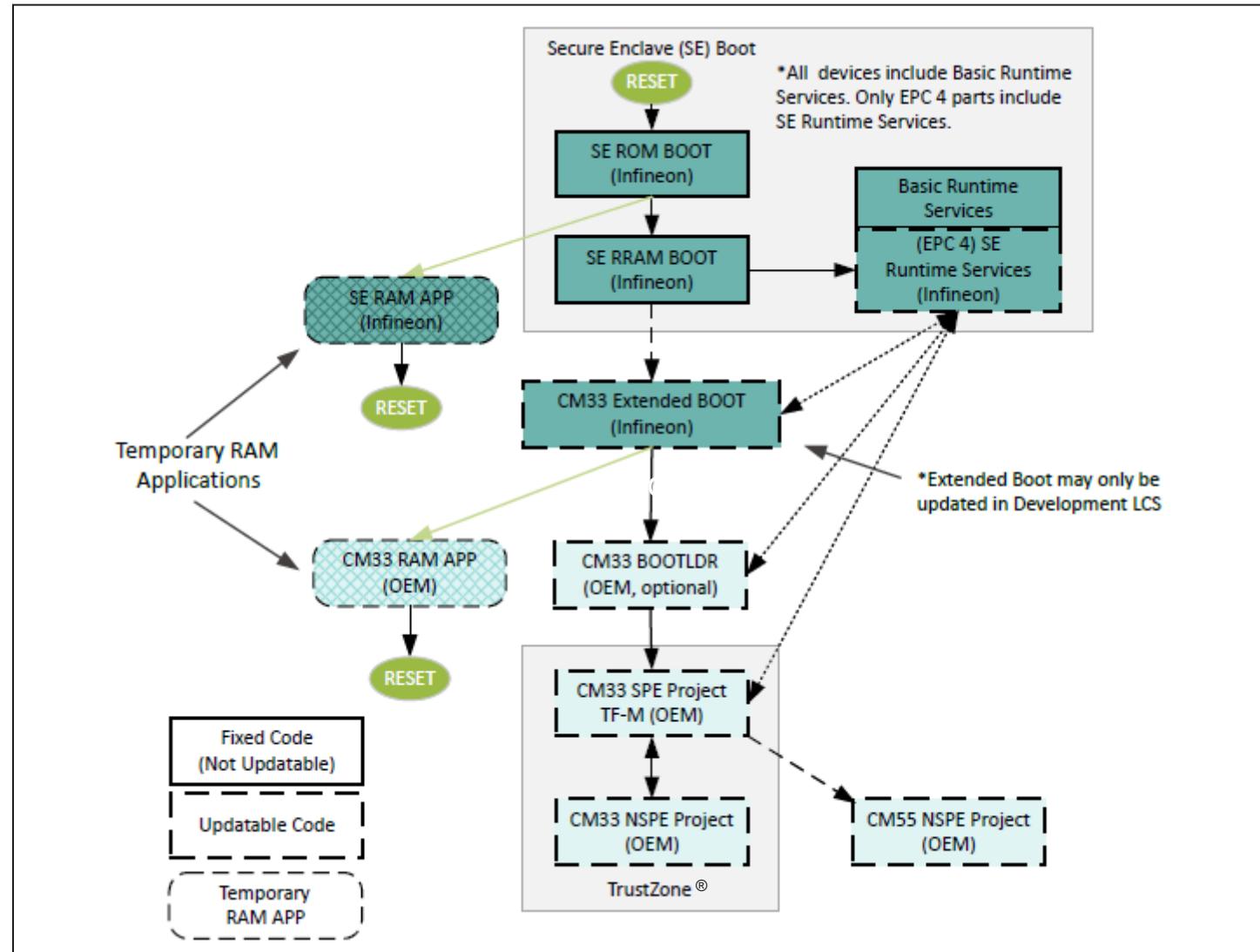


Security

- Up to Infineon Edge Protect Category 4 (EPC4)
- Lockstep Secure Enclave in low-power always-on domain
 - Secure Infineon RoT key storage; secure boot
 - Tamper detection, side channel attack (SCA) mitigation, and protection against fault injection attacks
 - On EPC4 part numbers only: Secure Enclave runtime services for Arm® Platform Security Architecture (PSA) compliant cryptography, key management, secure storage and attestation services
- Off-the-shelf Trusted Firmware-M enablement and Mbed-TLS for crypto operations
- Secure isolation of processing environments via Arm® TrustZone® with Root of Trust established at boot by Cortex®-M33 CPU
- Factory provisioned device unique keypair (DICE_DeviceID), Hardware Unique Key (HUK), Unique Device Secret (UDS), and Infineon device certificates
- Infineon proprietary protection units for memory and peripherals
- Secure firmware update; secure debug, secure RMA mode for field failure analysis

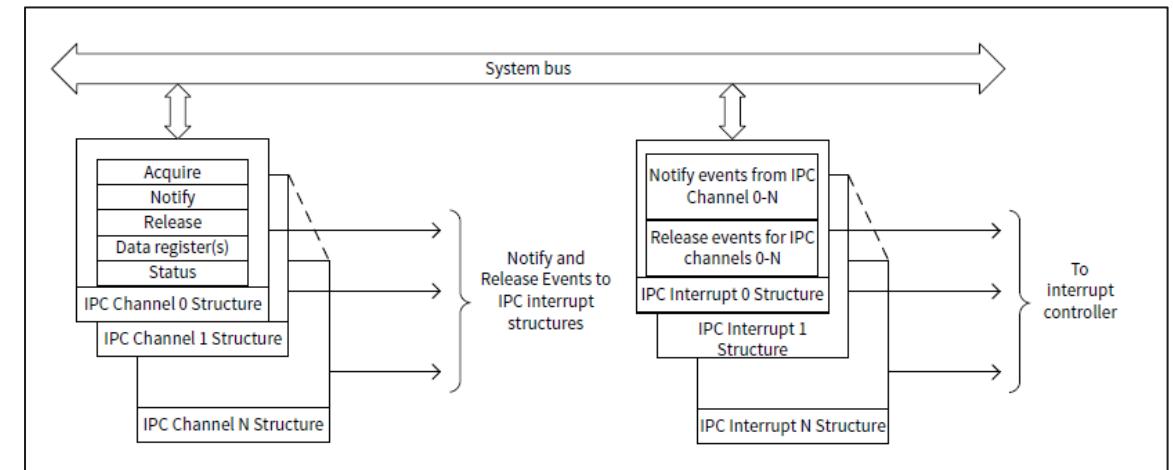


Security architecture



Inter-processor communication (IPC)

- Implements locks for mutual exclusion and synchronization between processors
- Allows sending messages between processors
- Supports up to 16 channels for communication
- Supports up to 8 interrupts, which can be triggered using notify or release events from the channels
- Inter-processor communication methods:
 - Half-duplex with shared event handling
 - Half-duplex with independent event handling
 - Full-duplex
- IPC is available in CPU Active power mode only



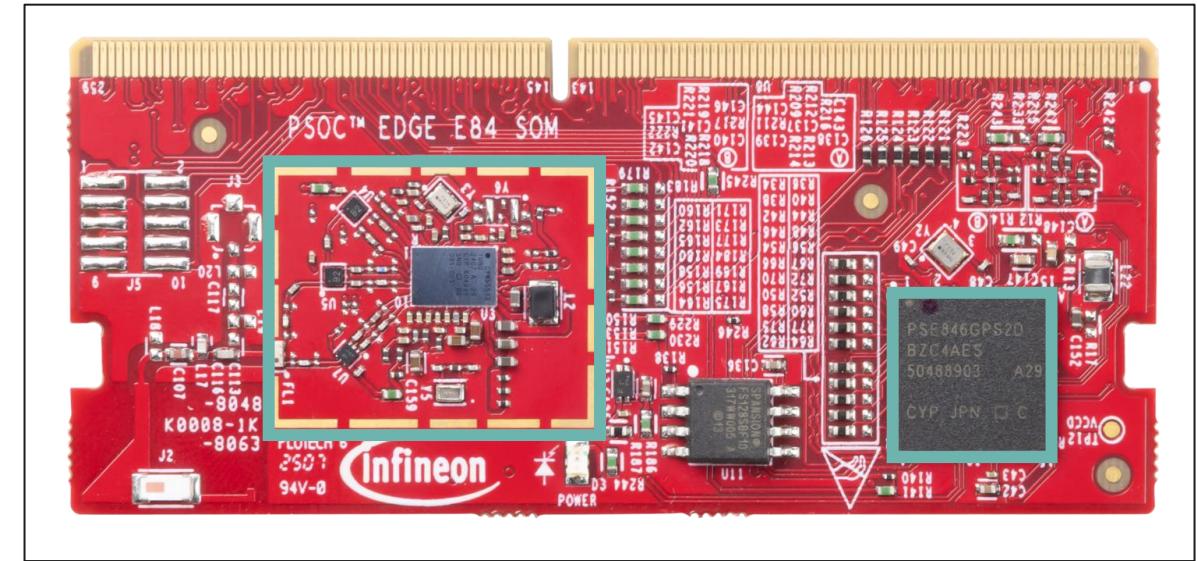
Device power modes

- Five system power modes
 - High-Performance (HP)
 - Low-Power (LP)
 - Ultra-Low-Power (ULP)
 - System Deep Sleep
 - Deep Sleep RAM and Deep Sleep Off
 - System Hibernate
- Three CPU power modes
 - CPU Active
 - CPU Sleep
 - CPU Deep Sleep
 - SRAM retention from 64 KB to 6.5 MB
 - SRAM granularity 64 KB

System power mode	CPU core voltage	Max frequency Cortex®-M33	Max frequency Cortex®-M55
System High-Performance (HP)	0.9 V	200 MHz	400 MHz
System Low-Power (LP)	0.8 V	70 MHz	140 MHz
System Ultra-Low-Power (ULP)	0.7 V	50 MHz	50 MHz
System Deep Sleep	0.7 V	Clock gated	Clock gated
System Hibernate	Off	Off	Off

Wireless connectivity

- PSOC™ Edge E84 can communicate with IoT combo chips using:
 - SDIO (for Wi-Fi)
 - UART (for Bluetooth® and Bluetooth® LE)
- Infineon AIROC™ has wide variety of IoT combo chips
 - SOM combines PSOC™ Edge E84 and CYW55513
- CYW55513 is a low-power combo chip
 - Tri-band, IEEE 802.11ax, Wi-Fi 6/6E,
 - Bluetooth® Low Energy 5.3



The Bluetooth® word mark and logos are registered trademarks owned by Bluetooth SIG, Inc., and any use of such marks by Infineon is under license.

Table of contents

1	Introduction to PSOC™ Edge	3
2	Overview of PSOC™ Edge features	10
3	Applications use-cases	47
4	Getting started with PSOC™ Edge	55

Industrial/consumer focus: Markets and applications

HMI



Smart homes



Wearables



Robotics



Monitoring and vision



Markets



- Appliances
- Industrial devices
- Factory automation



- Thermostats
- Speakers
- Door locks



- Fitness watches
- AR/MR/VR glasses and accessories
- Audio accessories



- Vacuum cleaners
- Vacuum robots
- Service robots
- Industrial robotics



- IP cameras
- Smart doorbells
- Security cameras and accessories

Advanced ML

Performance/Low-power

Integration

DEEPCRAFT™ AI Suite and ModusToolbox™

Infineon's next generation of ML-enabled MCUs

PSOC™ Edge E8

PSOC™ Edge – AI/ML at the Edge

Key benefits of Edge AI/ML

No internet connection required

Low latency and real-time response

Optimized power efficiency

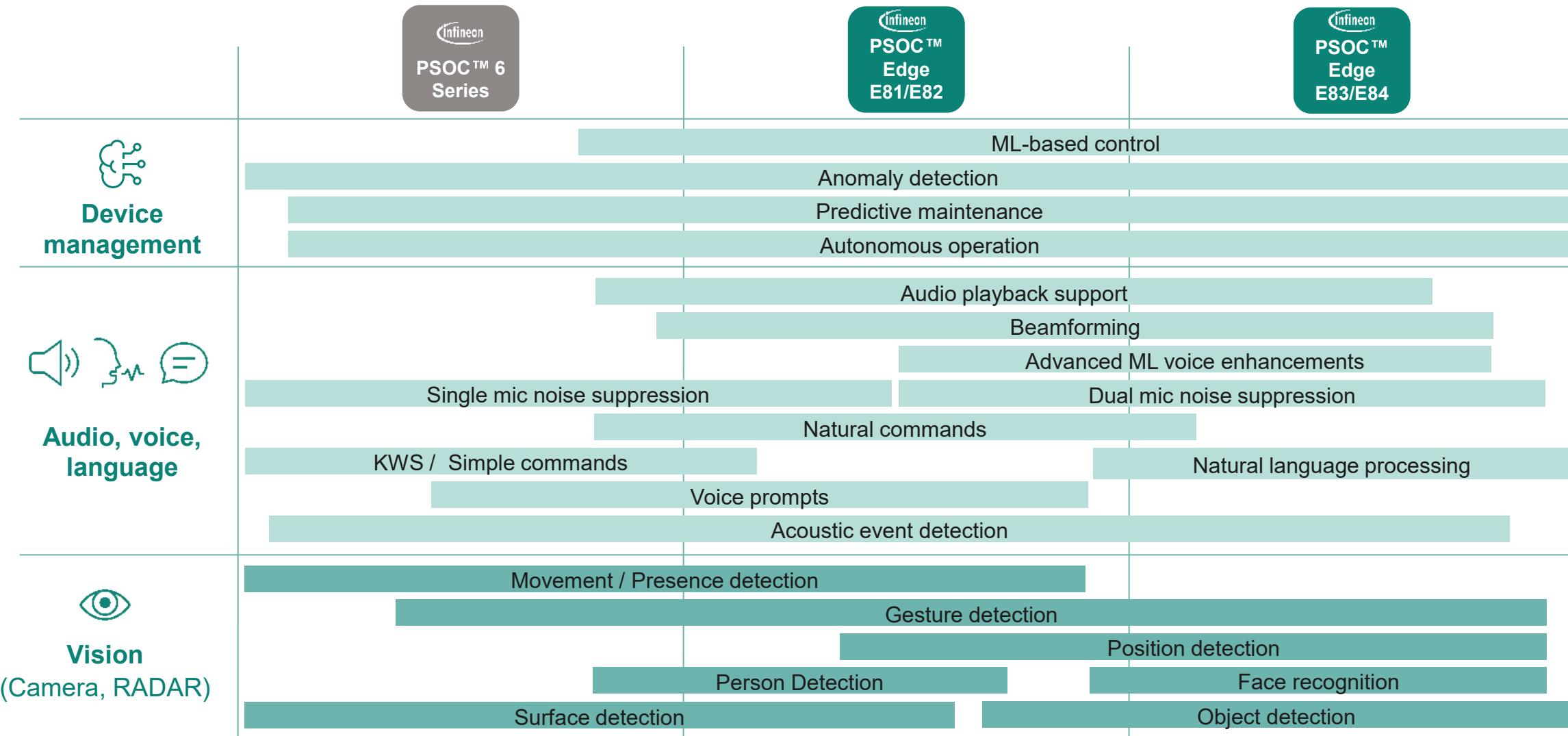
Improved security and data privacy

Reduced cost



Sense and inference at the edge

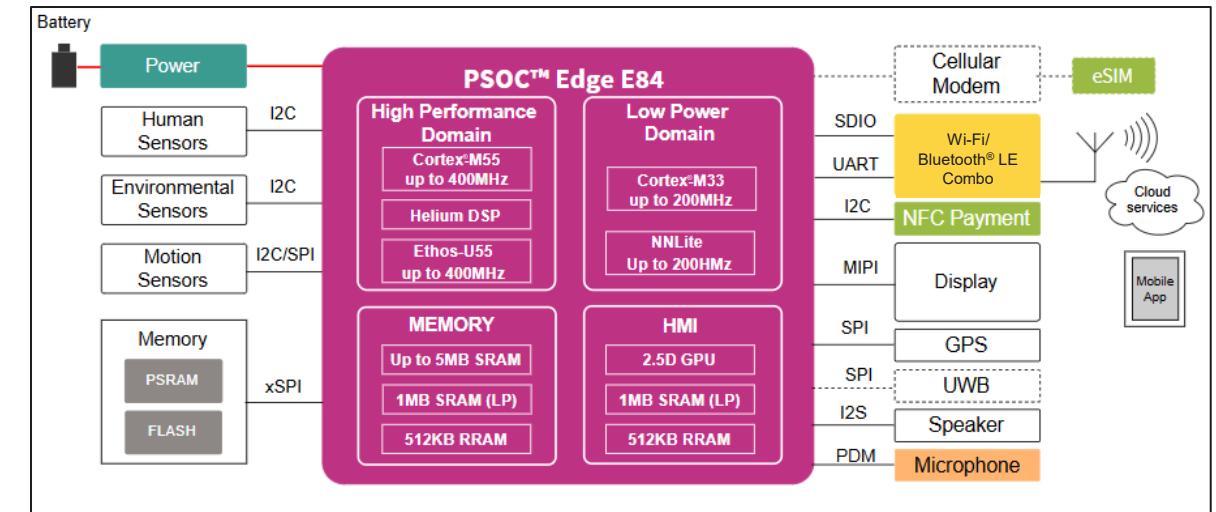
Expanding AI/ML horizons with PSOC™ Edge



PSOC™ Edge E84 application – Wearables

Why choose PSOC™ Edge?

- **Ultra-low-power consumption** to extend battery life and enable continuous sensing even in low-power modes
- **Advanced system architecture** with high-performance and always-on low-power domains
- **AI/ML acceleration and SW solutions** for sensor fusion processing
- **Helium™ DSP and Ethos™-U55** for advanced audio/voice processing for calls, voice commands and music playback
- **Advanced graphics** and **comprehensive HMI** features for high-resolution displays and enhanced experiences
- **Small form factor** with WLB154 package – $4.3 \times 5.3 \times 0.5$ mm



Target applications

- Wearables
- Smart watches
- EMG bands

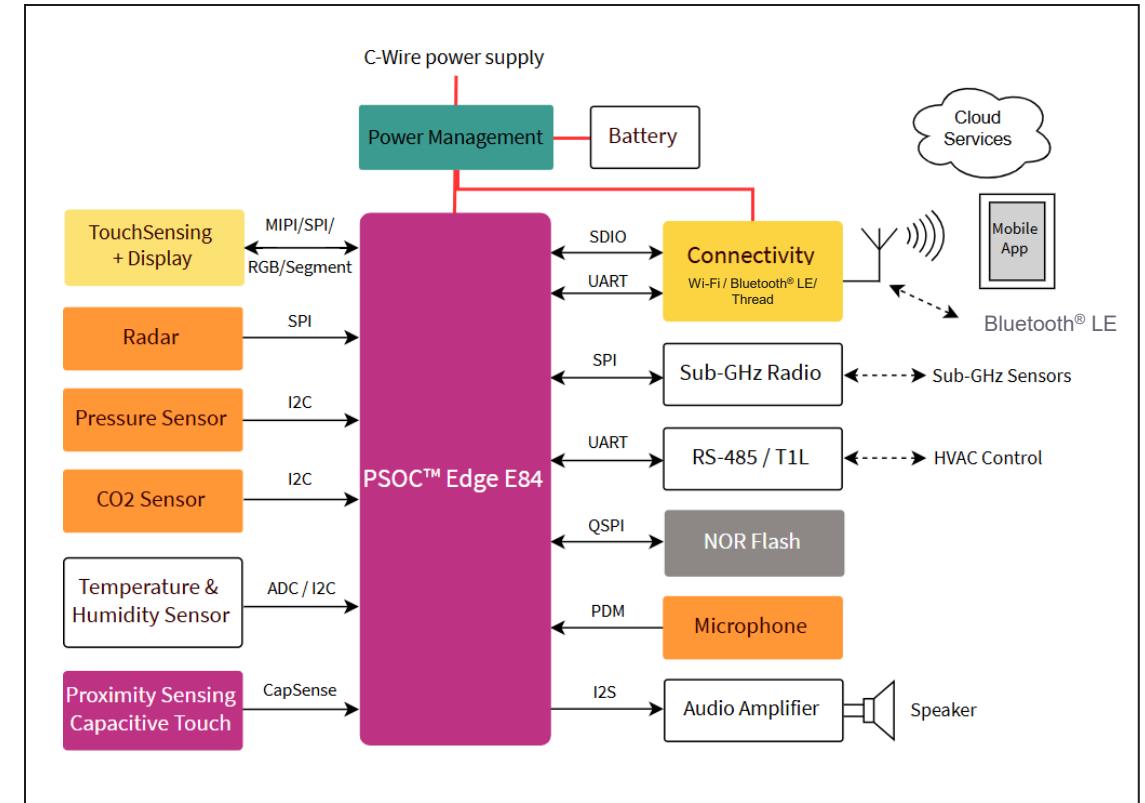
PSOC™ Edge E84 application – Smart home (thermostats)

Why choose PSOC™ Edge?

- **Dual-core architecture** with Cortex®-M55 and Cortex®- M33 cores for high-performance yet low-power energy efficient systems
- **Autonomous analog system for I/Os and peripherals** to monitor sensor inputs independently and always-on support
- **Multiple AI/ML accelerators** to provide multi-modal Edge AI experiences and increased comfort with features like wake word detection, speech recognition and voice commands
- **DEEPCRAFT™ Voice Assistant and DEEPCRAFT™ Audio Enhancement** best-in-class solutions for ease-of-use and accelerated time to market
- **Edge AI MCU** for smaller PCB footprint, lower BOM cost and simpler system design compared to the previous MPU approaches

Target applications

- Smart thermostats
- Home panels



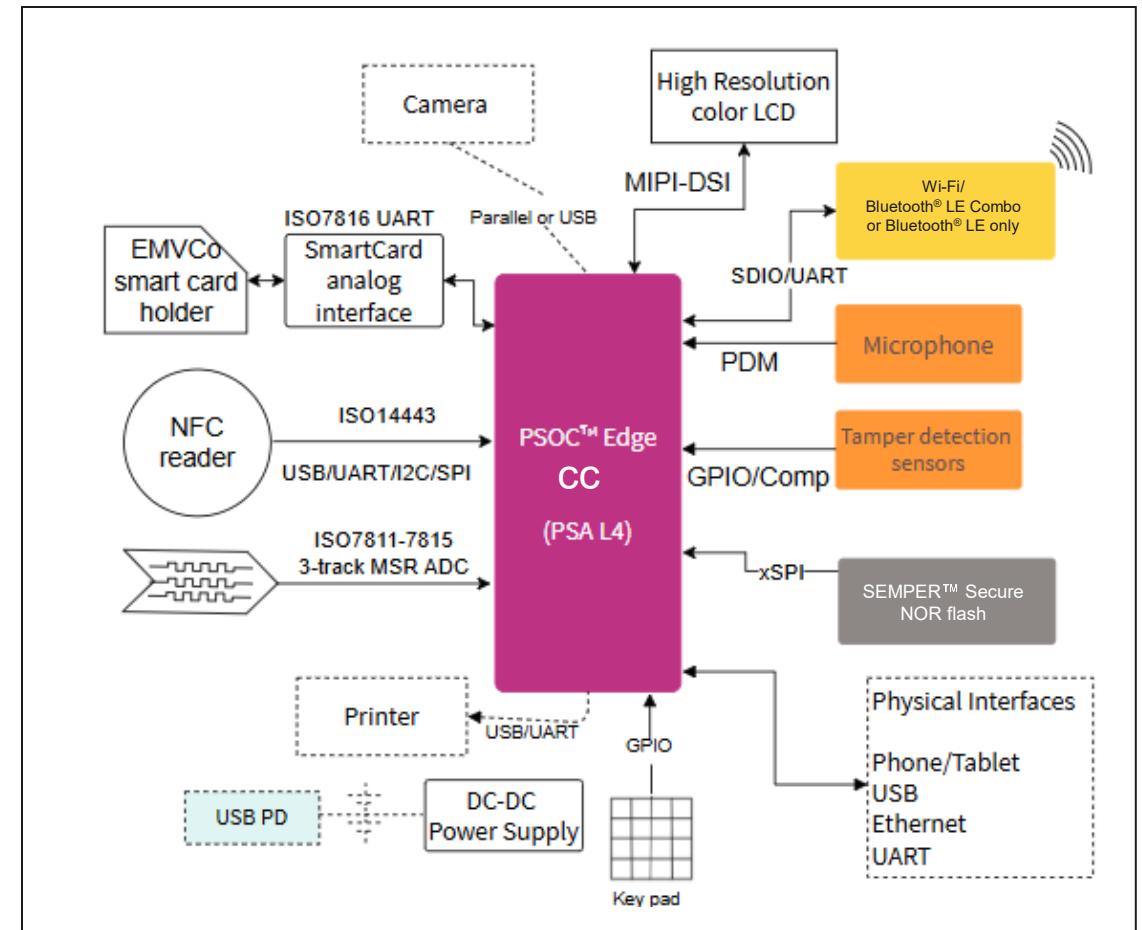
PSOC™ Edge E8 application – Point of sale (POS)

Why to choose PSOC™ Edge?

- Highest level of security certification with **PSA Level 4** security
- **PCI PTS v6.2** pre-certification for POS devices
- ISO7816 UART SmartCard support
- **Tamper detection** mechanisms
- **Ultra-low-power** on both static and dynamic
 - Hibernate mode with RTC, comparators, and GPIO resources is available
- Heterogenous **Cortex®-M55** and **Cortex®-M33** architecture
- Rich analog and digital peripheral sets for “secure world” implementation of MSR, NFC and EMVCo card readers

Target applications

- Mobile POS
- PINPAD terminals
- Portable POS with high-resolution color LCD
 - Authentication systems



PSOC™ Edge E8 application – Smart glasses

Why choose PSOC™ Edge?

- **Small form-factor** with WL154 package – $4.3 \times 5.3 \times 0.5$ mm
- **Ultra-low-power consumption** to extend battery life
- Heterogenous **Cortex®-M55** and **Cortex®-M33** architecture offering high energy efficiency
- **AI/ML acceleration** for voice assistant and/or ML-based sensor fusion capabilities
- **Multi-microphone support** for better user experience and voice command accuracy
- **DEEPCRAFT™ Voice Assistant** and **DEEPCRAFT™ Audio Enhancement** for accelerated time to market
- **Embedded state-of-the-art security** to help protect personal and sensitive information; ability to process everything at the edge for increased privacy

Target applications

- Smart glasses
- Augmented/virtual/mixed reality accessories

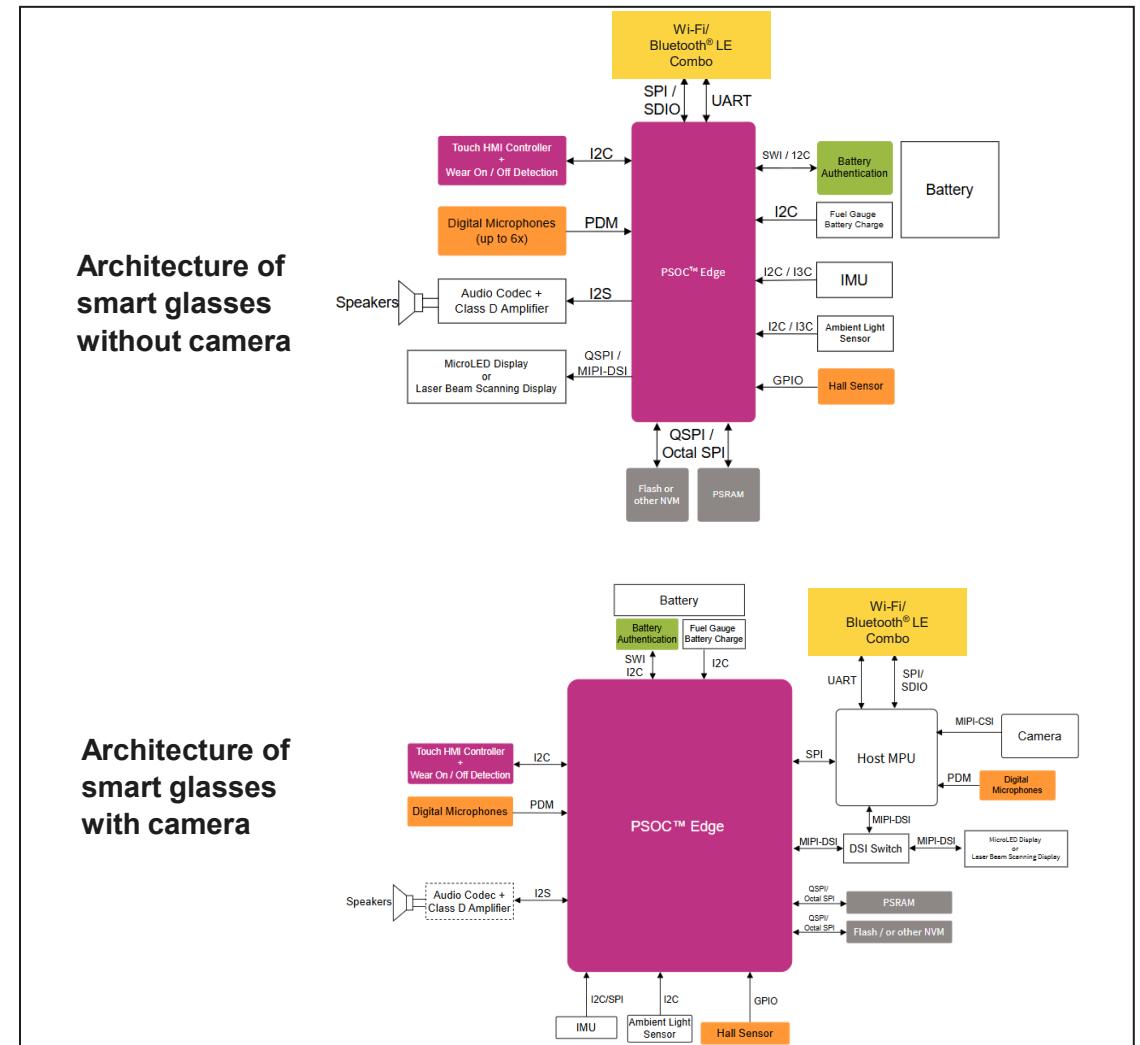
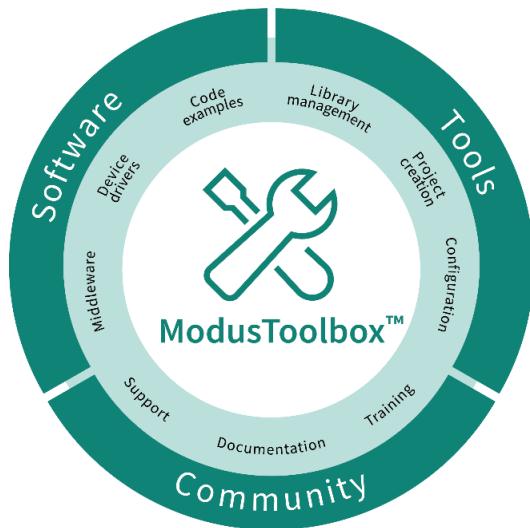


Table of contents

1	Introduction to PSOC™ Edge	3
2	Overview of PSOC™ Edge features	10
3	Applications use-cases	47
4	Getting started with PSOC™ Edge	55

PSOC™ Edge – Ecosystem for AI/ML applications

ModusToolbox™



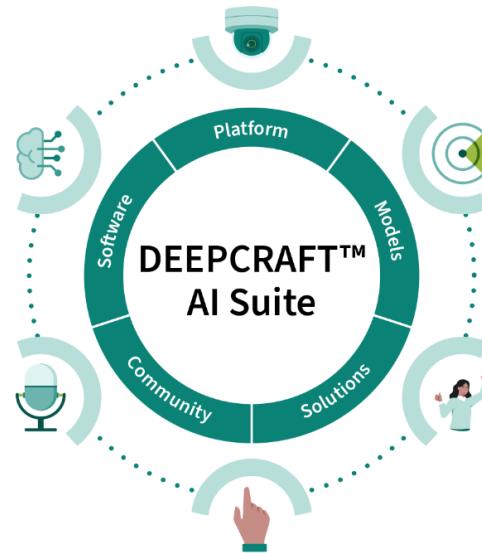
ModusToolbox™ – Comprehensive collection of resources

- Flexible development tools and resources
- Robust software, middleware, and security ecosystem



Comprehensive Zephyr RTOS enablement for
seamless integration and rapid development

DEEPCRAFT™ AI Suite



Accelerate Edge AI Innovation with DEEPCRAFT™ AI Suite

- Integrated platform and tools for end-to-end AI workflow
- Comprehensive AI solutions
- Centralized DEEPCRAFT™ AI Hub

PSOC™ Edge embedded development



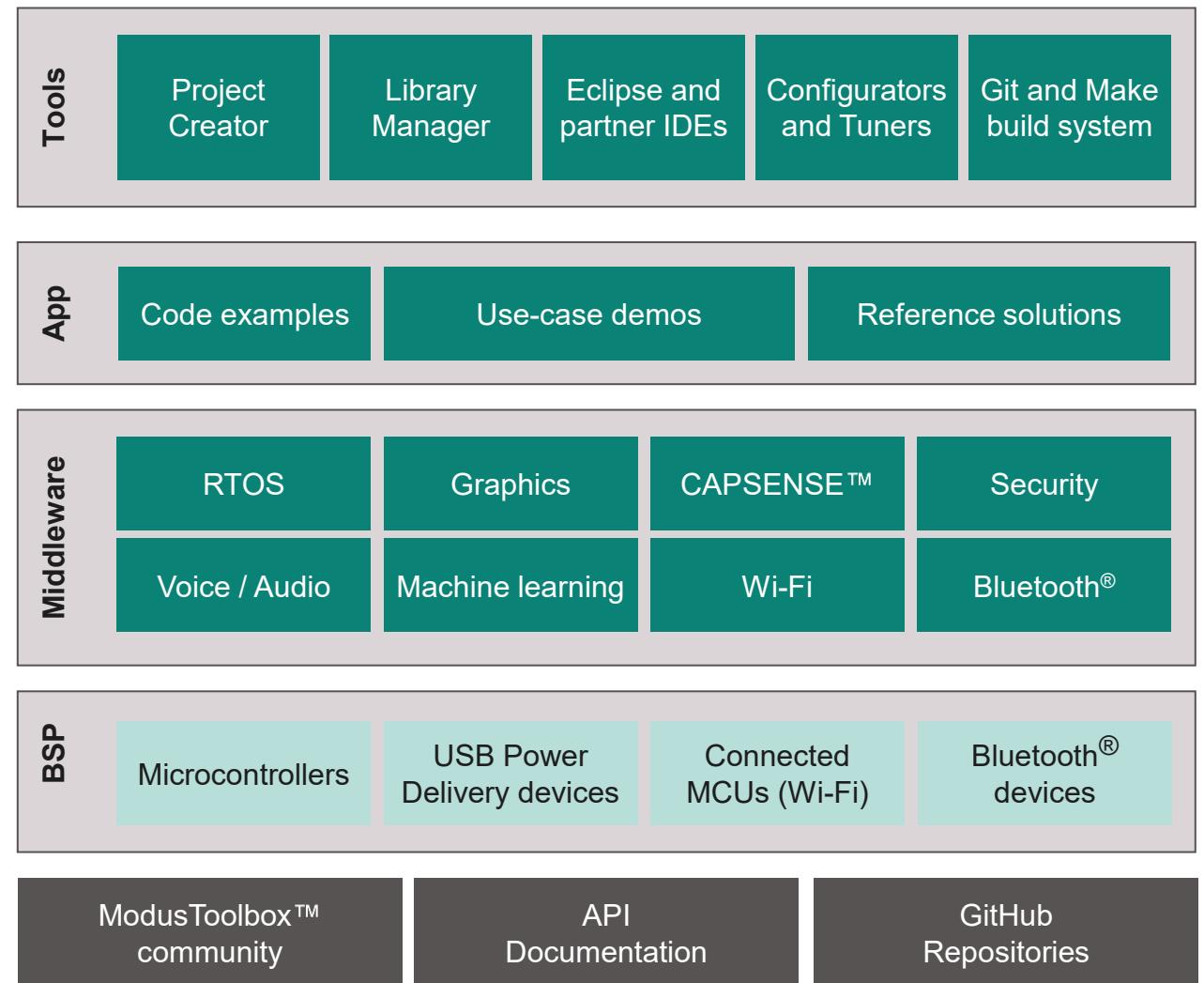
Development boards

- **PSOC™ Edge E84 Evaluation Kit:** PSOC™ Edge device functional evaluation
- **PSOC™ Edge E84 SOM:** PSOC™ Edge Minimal system-on-module
- **PSOC™ Edge E84 AI Kit:** Low-cost kit with multiple sensors for evaluation of AI capabilities and fast prototyping

ModusToolbox™ – Comprehensive collection of resources

Enablement throughout the application development process

- IDEs – [Eclipse](#) / [VS Code](#) / [IAR](#) / [Keil µVision](#)
(click to access hyperlinks)
 - Dedicated user guides for all IDEs available online
- Configurators and code Generation
 - Device Configurator (pins/clocks)
 - Edge Protect Configurator
 - QSPI Configurator
 - Smart I/O Configurator
- Additional ModusToolbox™ packages
 - Programming tools
 - Edge Protect Security Suite
 - Motor Suite
- Application development resources
- Middleware from Infineon and the ecosystem
- Board support packages/device packages



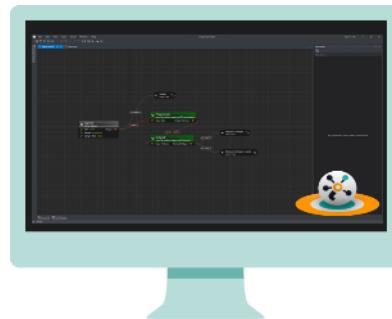
Accelerate Edge AI Innovation with DEEPCRAFT™ AI Suite

DEEPCRAFT™ products provide innovative, trustworthy, convenient and green **AI** software solutions.

Infineon offers **end-to-end Edge AI** and **best-in-class system performance in combination with Infineon hardware**.

Platform and tools

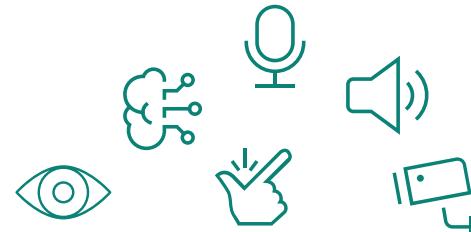
For data collection and pre-processing, model training, model conversion and deployment



DEEPCRAFT™ Studio
DEEPCRAFT™ Model Converter*

Solutions

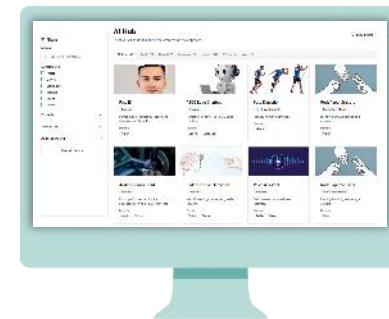
Collection of high value tools, models and configurators to add AI-based capabilities. Range across sensor and data types, from off-the-shelf to customizable solutions.



DEEPCRAFT™ Ready Models
DEEPCRAFT™ Audio Enhancement*
DEEPCRAFT™ Voice Assistant*
DEEPCRAFT™ Face ID*
Liquid level sensing

DEEPCRAFT™ AI Hub

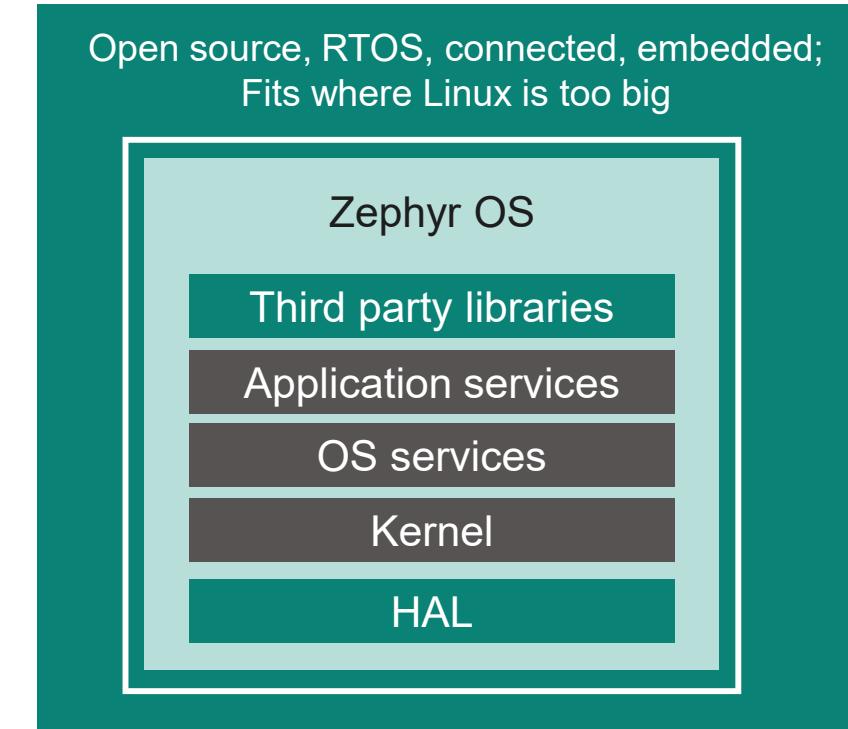
Find the DEEPCRAFT™ Studio platform, plus the models, demos, solutions, tools, and more that you need all in one centralized hub.



DEEPCRAFT™ Studio Accelerators,
open-source models, AI tools, and more;
Everything Edge AI in one place.
Visit [DEEPCRAFT™ AI Hub](#)

Zephyr – a proven RTOS ecosystem, by developers, for developers

- Open-source, real-time operating system
- Portable, secure, power-efficient
- Highly connected
 - Bluetooth® LE, Wi-Fi, Ethernet, USB / USB-C, CAN bus
- Complete developer environment
 - Toolchain and HAL management
 - Logging, tracing, debugging
 - Testing framework
- Infineon support for:
 - PSOC™ Edge E84
 - PSOC™ Control C3
 - AIROC™ CYW20829, and more



PSOC™ Edge E84 evaluation kit: KIT_PSE84_EVAL

Kit contents

- PSOC™ Edge E84 evaluation kit
- USB Type-C to Type-C cable
- 4.3-inch capacitive touch display and USB camera module

Highlights

- Hardware evaluation for rapid prototyping and development of applications based on PSOC™ Edge
- Provides easy access to all the devices interfaces and capabilities
- Evaluation kit consists of a base board routing out all the key interfaces of the device and a system-on-module featuring PSOC™ Edge E84

Featured components

- PSE846GPS2DBZC4 PSOC™ Edge E84 MCU
- PSOC™ 4000T/ CAPSENSE™ co-processor
- AIROC™ CY55513 Wi-Fi + Bluetooth® combo chip
- IM73A135V01 analog microphone
- IM73D122V01 digital microphone
- S25FS128SAGBHM203 16 MB flash memory
- S70KS1283GABHI020 16 MB PSRAM



Kit status

- Available now
- Order by visiting [KIT_PSE84_EVAL](#)

PSOC™ Edge E84 AI kit: KIT_PSE84_AI

Kit contents

- PSOC™ Edge E84 AI kit
- Camera module

Highlights

- Designed to support the creation of Edge AI-powered applications
- Optimized for rapid prototyping and development of embedded systems leveraging the versatile PSOC™ Edge E84 microcontroller
- Data collection enabled via radar, acoustic, pressure, and IMU sensors available in the kit
- Enables evaluation of Infineon's ML platform – DEEPCRAFT™ AI Suite

Featured components

- PSE846GPS2DBZC4 PSOC™ Edge E84 MCU
- AIROC™ CY55513 Wi-Fi + Bluetooth® combo chip
- BGT60TR13C 60 GHz radar
- IM73A135V01 analog microphone
- IM73D122V01 digital microphone
- DPS368 barometric pressure sensor
- S25FS128SAGBHM203 16 MB flash memory
- S70KS1283GABHI020 16 MB PSRAM



Kit status

- Available now
- Order by visiting [KIT_PSE84_AI](#)

Revision history

Document revision	Date	Description of change
**	2026-01-12	Initial release.

