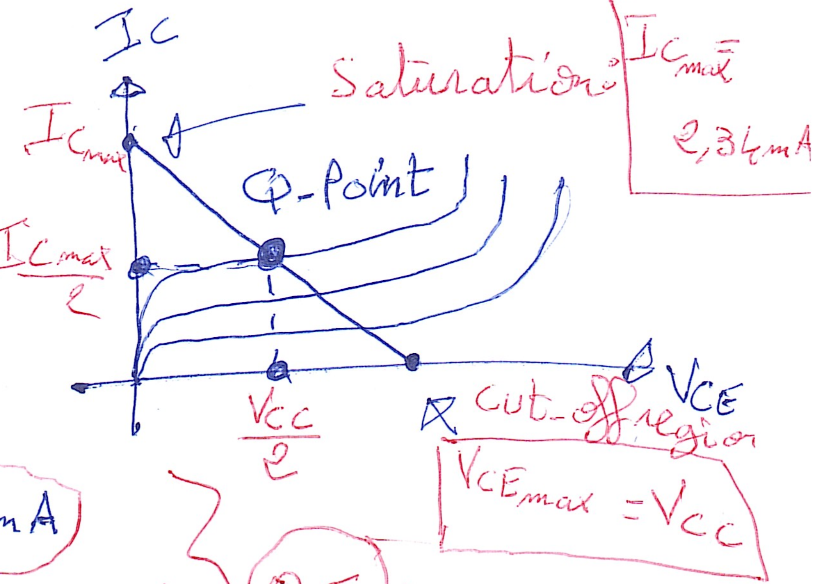
Solution of the Problem

Part 1: Design A

1) Here is the load line Q-point in the middle of the load line =>



$$I_{C_0} = \frac{I_{C_{max}}}{2} = 1{,}17\,mA$$

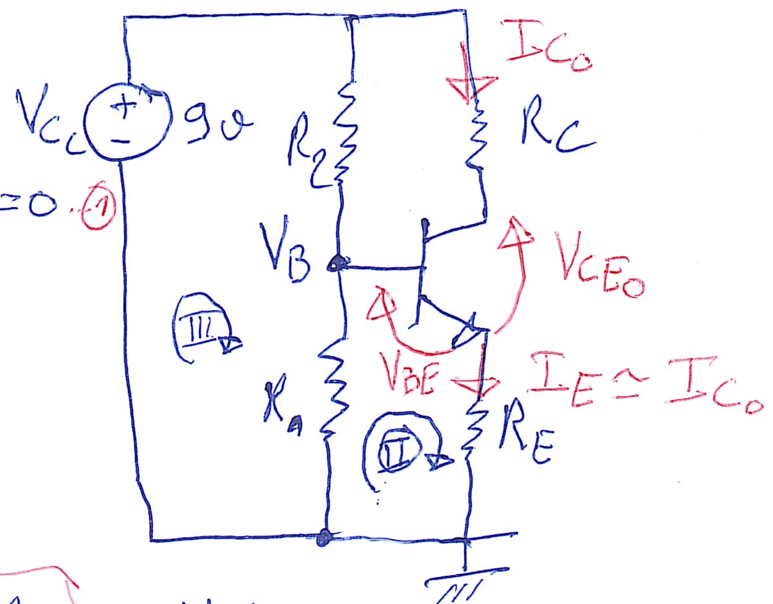
$$V_{CE_0} = \frac{V_{CC}}{2} = \frac{9}{2} = 4{,}5 \text{ volts}$$

0,5 P

* to calculate the values of R_1 and R_E we study the circuit in DC:

* Loop 1: (Big loop)

$$V_{CC} - (R_C + R_E) I_{C_0} - V_{CE_0} = 0 \quad \text{...(1)}$$



from (1) we have:

$$\frac{V_{CC} - V_{CE_0}}{I_{C_0}} = R_C + R_E$$

$$\Rightarrow R_E = \frac{V_{CC} - V_{CE_0}}{I_{C_0}} - R_C$$

0,5 P

NUMERICAL VALUES

$$R_E = \frac{9 - 4{,}5}{1{,}17\,10^{-3}} - 1{,}65\,10^{3}$$

$$R_E = 2{,}2\,k\Omega$$

* Loop 2 : $V_B - V_{BE} - R_E I_E = 0$ ... (2)

and using voltage divider (Assuming current $I > 10 I_b$) => $V_B = \frac{R_1}{R_1 + R_2} V_{CC}$ ... (3)

from (3) and (2) => $V_{BE} + R_E I_E = \frac{R_1}{R_1 + R_2} V_{CC}$

$$\frac{1}{V_{BE} + R_E I_E} = \left(1 + \frac{R_2}{R_1}\right) \cdot \frac{1}{V_{CC}}$$

$$\frac{R_2}{R_1} = \frac{V_{CC}}{V_{BE} + R_E I_E} - 1$$

$$R_1 = R_2 \cdot \frac{1}{\frac{V_{CC}}{V_{BE} + R_E I_E} - 1}$$

0,5 p

Numerical values : $R_1 = 2{,}7\,10^3 \cdot \frac{1}{\frac{9}{0{,}7 + 2{,}2 \cdot 10^3 \cdot 1{,}17 \cdot 10^{-3}} - 1}$

(Recall that 2N2222 is a Silicon NPN TRANSISTOR => $V_{BE} = 0{,}7\,V$

$R_1 = 1{,}54\,K\Omega$ 0,25 p

$I_E \simeq I_C = 1{,}17\,mA$

0,25 p

2) The name: voltage divider Biasing (it is a method of biasing with common emitter) 0,5p

3) The purpose: voltage Amplifier 0,5p

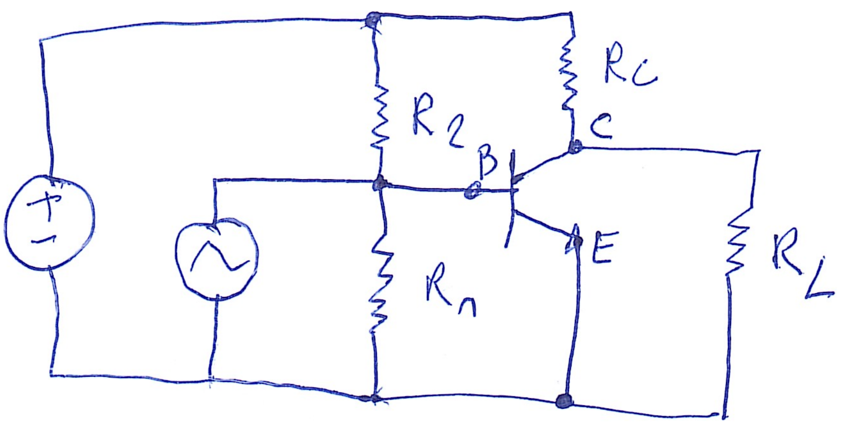
4) C_1 and C_2 are called coupling Capacitors 0,25p

C_3 is called by pass capacitor 0,25p

(Decoupling capacitor is accepted)

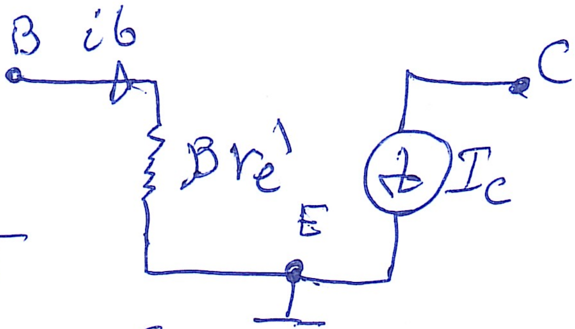
5) AC-EQUIVALENT CIRCUIT:

—||— are replaced by short circuits

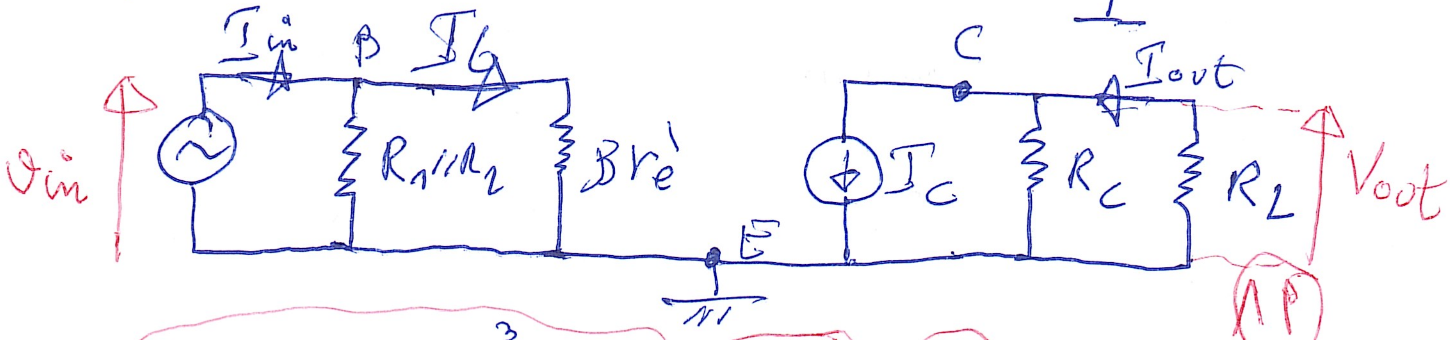


(3/5)

in (AC) V_{cc} goes to ground and the π-model of the Transistor is



(AC) EQUIVALENT CIRCUIT



(1p)

$$r_e' = \frac{25\cdot 10^{-3}}{1{,}17\,10^{-3}} = 21{,}37\,\Omega$$ (0,5p)

6) $G_V = \frac{V_{out}}{V_{in}}$ and we know that $v_{out} = -(R_C // R_L)\cdot I_C$

$V_{in} = \beta r_e' \cdot I_b$

$v_{out} = -\beta\,(R_C // R_L)\,I_b$

$$G_V = \frac{V_{out}}{V_{in}} = -\frac{\beta(R_C // R_L)\,I_b}{\beta r_e'\,I_b} = -\frac{(R_C // R_L)}{r_e'}$$ (0,5p)

NUMERICAL VALUES: $G_V = 75{,}96$ (0,5p)

7) $Z_{in} = \frac{v_{in}}{I_{in}} = (R_1 // R_2) // \beta r_e' = 806{,}4\,\Omega$ (0,5p)

$Z_{out} = \frac{V_{out}}{I_{out}} = R_C = 1{,}65\,k\Omega$ (0,5p)

Part 2: comparison

1) The name: Base Biasing (0,5 p)

2.a) The Q-Point will move slightly (Negligeable). Voltage-DIVIDER is very stable and The gain is independant from β_{DC} => $G_{V_{2N2222}} \simeq G_{V_{2N3904}}$ (0,5)

2.b) The Q-Point will change dramatically. The base biasing is not stable => (0,25)

$G_{V2N2222} \neq G_{V2N3904}$ (See calculation below)

3) The best design is Design A (0,5)
(Gv is independant from B)
Q-Point is very stable) 0,5

Calculation with 2N3904:

$V_{CC} - V_{BE} - (R_b + \beta_{DC} R_E) I_b = 0 \Rightarrow I_B = \frac{V_{CC} - V_{BE}}{R_b + \beta_{DC} R_E} = 6,06$

$I_{C_0} = \beta_{DC} \cdot I_B = 0,85 \, mA$ (0,75 p)

$V_{CE_0} = V_{CC} - (R_C + R_E) I_{E_0} = 5,9$ volts

$r_e'' = \frac{25 \, mV}{0,85 \, 10^{-3}} = 29,4 \, \Omega$

(5 / 5)

$G_V = \frac{-(R_C // R_L)}{r_e''} = -55,2 \, \Omega$