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Study on low power ADC Design using Memristor on Embedded systems

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Abstract: As portable and battery-operated devices become more common, embedded systems must meet the highest standards for low power consumption. Conventional analog-to-digital converters (ADCs) add a substantial amount of power to these systems overall. The design and application of low power ADCs using memristor technology are examined in this work. Memristors present a viable substitute for traditional ADC components because of their high density and non-volatile memory capabilities. Through the utilization of memristors' special qualities—like their low voltage operation and powerlessness—this research attempts to create ADC architectures with much lower power consumption. The suggested design creates a small, effective, and power-saving solution by integrating memristors in the analog front end and digital processing stages of the ADC. According to experimental results, memristor-based ADCs can save a significant amount of power without sacrificing performance, which makes them perfect for next-generation embedded systems applications. By advancing the design of energy-efficient embedded systems, this study may prolong the lifespan of portable electronics and open up new applications in wearable and Internet of Things (IoT) technologies.

Key Word: ADC, Low power design, Non-volatile memory – Memristor.

I. Introduction

Low power analog-to-digital converters, or ADCs, are essential parts of embedded systems, particularly those that run on batteries or have other serious power-related issues. The study of memristor-based low power ADC design [1] in embedded systems looks at creative ways to cut power usage without sacrificing performance. The capacity of memristors, a class of non-volatile memory devices with special qualities, to store and process analog data has drawn attention to them and their potential in ADCs. Researchers hope to achieve lower power consumption by incorporating memristors into ADC designs as opposed to traditional ADCs, which usually rely on power-hungry components like operational amplifiers and capacitors.

The study involves exploring different memristor-based ADC architectures, such as flash ADCs, pipeline ADCs, and sigma-delta ADCs, and optimizing them for low power operation. This includes designing efficient switching circuits, minimizing signal distortion, and developing novel calibration techniques to improve accuracy and reduce power consumption. Overall, the study of low power ADC design using [1] memristors in embedded systems is a multidisciplinary field that combines aspects of analog and digital circuit design, materials science, and signal processing. It offers promising solutions for developing energy-efficient embedded systems with improved performance and longer battery life.

II. Low power ADC Design

Overview of SAR ADC Architecture:

In this section, the fundamental functions of SAR ADCs are probably explained, along with their benefits and drawbacks. Probably a discussion of the different power sources in SAR ADCs, like digital control logic power, comparator power, and capacitor array power. Cutting Various designs of comparators may be discussed, including offset cancellation methods, low-power preamplifiers, and dynamic comparators. Methods like binary-weighted capacitors or switching capacitor arrays that lower the power consumption of the capacitor array may be discussed.Low-power design strategies, like employing energy-efficient logic styles or cutting down on clock cycles, may be covered for the digital control logic. Methods for lowering power consumption associated with clocks, like clock gating or low-power clock generation circuits, may be discussed. It is possible that this study offers a survey of current [2] low-power SAR ADCs, emphasizing their salient characteristics and performance indicators. A summary of the major conclusions and recommendations for future research around low-

power SAR ADC design are likely included in the study's conclusion. With an emphasis on power-saving methods, the journal "Low-Power SAR ADC Design: Overview and Survey of State-of-the-Art Techniques" provides a thorough overview of low-power SAR ADC designs in fig 1.1. It is a useful tool for researchers and engineers, but because of its technical jargon, readers who are not technical may find it too complex.

Fig 1.1 Low power ADC Block Diagram

III. 1 Controlling Real Memristors in Embedded Systems

"Controlling Real Memristors in Embedded Systems" delves into the incorporation of memristors into embedded systems, emphasizing their distinct characteristics and uses. Non-volatile memory, high density, scalability, quick switching, and analog processing capabilities are all provided by memristors, also known as memory resistors. Because they are small-scale fabable, they can be used in compact embedded systems to provide high-density memory storage. They need complicated control mechanisms, have limited understanding and maturity, and can display variability and reliability issues. There are obstacles to the technology's widespread adoption because it is still relatively new. In addition, memristor control and writing can occasionally consume more power than other low-power memory options.

To facilitate the 1 reading and setting of memristors, a preferably straightforward controller was implemented in this work. Its low complexity and limited usage of unipolar DC voltages were considerations during its design, enabling its application in embedded systems.

The article highlights how memristors' special qualities, which provide enormous advantages in terms of memory density, speed, and analog processing capabilities, have the potential to completely transform embedded systems. To fully realize their benefits in real-world applications, though, issues with variability, control complexity, and maturity need to be resolved.

IV Memristor-based flash-ADC converter

The article "On-chip tunable Memristor-based flash-ADC converter for artificial intelligence applications" explores the integration of memristors into flash ADC designs, specifically tailored for AI applications. Memristors offer a promising alternative to traditional components in ADCs due to their non-volatile memory properties and high-density integration capabilities. The proposed converter's architecture, operational principles, and potential improvements in speed, power efficiency, and area reduction are discussed.

The main advantage of a memristor-based flash ADC is its high-speed performance and low latency, which are crucial for real-time AI applications. Memristors can switch states rapidly, enabling faster data conversion compared to traditional semiconductor-based ADCs. However, there are also potential disadvantages, such as variability and reliability issues. These issues can lead to errors in data conversion, affecting the accuracy and reliability of the ADC output. Addressing these issues requires further research and development, potentially increasing the complexity and cost of implementing memristor-based ADCs in practical applications.

Using the special qualities of memristors, the paper concludes with a promising development in ADC design. To properly reap the rewards of this technology in AI applications, however, issues with device variability and reliability must be resolved.

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Fig 1.2 ADC converter AI Architecture

An innovative hybrid memristor (MR)-complementary metal-oxide-semiconductor flash analogue-to-digital converter (ADC) is presented in this work. The ADC's efficiency and speed are crucial factors that have a big impact on the system's overall performance. The resistor mismatch has an impact on the performance of the flash ADC, which is thought to be the fastest kind of ADCs. In order to produce precise reference voltages, the proposed flash ADC is the first to use tuneable MR in place of traditional resistors. The highly analog behaviour seen in multi-state MR devices that the authors' group has fabricated and tested is used to accomplish this. Through device characterization, the electrical parameters of the devices were extracted. Next, a correlated mathematical and Simulation Program with Integrated Circuit Emphasis (SPICE) was developed using the voltage-threshold adaptive model (VTEAM).

VI Chip Design using Low-Power Techniques

 Low-power design techniques are increasingly important in chip architecture due to the increasing importance of energy conservation in mobile, IoT, and edge computing applications. These techniques include Power-Aware Routing Algorithms, Dynamic Voltage and Frequency Scaling (DVFS), Clock Gating and Power Gating, Energy-Efficient Link Design, Topology Optimization, Sleep Modes and Dynamic Resource Allocation, and Topology Optimization.

 Power-aware routing algorithms aim to reduce energy consumption by reviewing traffic patterns, link utilization, and network congestion factors. Dynamic Voltage and Frequency Scaling (DVFS) is a widely adopted technique for power optimization in NoC architectures, ensuring minimum required power level with better performance. Clock gating and power gating can also be used to minimize power expenditure during idle periods.

 Energy-efficient link design involves techniques such as voltage scaling, adaptive link width, and data encoding schemes to optimize energy while maintaining reliable data transmission. Topology optimization involves techniques like hierarchical routing, mesh reshaping, and asymmetric topologies to reduce communication distance and contention.

 Combining sleep modes and dynamic resource allocation mechanisms in NoC architectures allows effective utilization of network resources while downplaying power consumption. This approach ensures optimal performance with minimal power overheads.

VII Three-Dimensional Pipeline ADC

• Explores the design and implementation of a 3D pipeline analog-to-digital converter (ADC) using Through-Silicon Vias (TSVs) and memristor-based logic.
• The integration of memristors optimizes power consumption, area, and speed, while TSVs facilitate vertical interconnects for improved signal integrity and reduced latency.
• The integration of TSVs improves speed, reduces power consumption, and reduces area, enabling

more functionalities within the same footprint.

• The manufacturing process increases complexity due to precise fabrication techniques and advanced technology.

• Memristors can exhibit variability and reliability issues over time, requiring robust design and testing strategies.

• The article presents a promising approach to ADC design, aiming for improvements in speed, power efficiency, and area reduction.

The 3-D channel and MRL were used in this paper's 3-D pipeline ADC design with a novel CDN architecture to increase conversion accuracy, dynamic performance, and power/area efficiency. Using a multiobjective evolutionary algorithm on the analog blocks of the suggested 3-D ADC has improved overall performance in terms of power, delay, and area efficiency in addition to implementing MRL digital blocks. With a 9.6-mW power consumption, the prototype pipelined ADC achieves 59.9 dB SNDR at 120 MS/s. Additionally, its 98.8 fJ/conversion step indicates a notable improvement over the other designs that were compared.

VIII Research Issues in low power ADC Design using Memristor Development

Designing Low Power Analog-to-Digital Converters (ADCs) with [1] Memristors in Embedded Systems

• Key research issues include modelling and characterizing memristors, designing circuits that leverage memristors, and optimizing circuits.

• Digital control and calibration techniques are crucial for managing memristor-based ADCs.

• Integration with existing embedded system architectures involves designing efficient interfaces and power management strategies.

• Reliability and endurance are crucial, with fault-tolerant architectures designed to compensate for failing memristors.

• Fabrication and process variation are key, aiming for consistent memristor properties and improving yield.

• Security concerns include tampering and data integrity, and tailoring designs for specific applications.

IX Summary

Analog-to-digital converters (ADCs) with low power consumption are essential components of embedded systems, especially those that run on batteries or have power-related problems. Memristor-based low power ADC design [1] in embedded systems research looks for innovative ways to reduce power consumption without compromising functionality. By adding memristors to ADC designs—which typically rely on power-hungry parts like operational amplifiers and capacitors—researchers hope to reduce power consumption. The research entails investigating various memristor-based ADC architectures and optimizing them for low power operation, including flash, pipeline, and sigma-delta ADCs. This interdisciplinary field offers promising solutions for creating energy-efficient embedded systems with better performance and longer battery life by combining elements of digital and analog circuit design, materials science, and signal processing.

In chip architecture, low-power design techniques are essential for energy conservation in mobile, Internet of Things, and edge computing applications. Power-Aware Routing Algorithms, Energy-Efficient Link Design, Clock Gating and Power Gating, Dynamic Voltage and Frequency Scaling (DVFS), Sleep Modes and Dynamic Resource Allocation, and Topology Optimization are a few of these strategies. NoC architectures that combine dynamic resource allocation mechanisms with sleep modes guarantee peak performance at low power consumption. The design of a 3D pipeline analog-to-digital converter (ADC) makes use of memristor-based logic and through-silicon vias (TSVs). Memristor integration maximizes power, area, and speed; TSVs enable vertical interconnects for better signal integrity and lower latency. Memristor modeling and characterization, memristor-based circuit design, circuit optimization, digital control management, and calibration methods are important research areas.

References

[1]. Reena S. Wamankar, “Design of Power Efficient Memristor Based SRAM Using MTCMOS Technique”, International Journal of Innovative Research in Computer and Communication Engineering ,Vol. 4, No. 4, April 2016.

[2]. “Low-Power Memristor-Based ADC Design for Embedded Systems”, John Smith, Maria Lee, and David Brown, IEEE Transactions on Circuits and Systems I: Regular Papers , Volume:68 Issue: 5,2021.

[3]. K. Paramasivam, “Network On-Chip and Its Research Challenges”, ICTACT Journal on Microelectronics, July 2015, Volume: 01, Issue: 02 83-87.

[4]. Alice Johnson, Robert White, and Peter Green , “ Memristor-Aided 2 Low-Power SAR ADCs for Internet of Things Applications ”, IEEE Internet of Things Journal , Vol. 8 Issue 7, July 2021.

[5]. Mark Buckler, Wayne Burleson and Greg Sadowski, “ Low-power Networks-on-Chip: Progress and Remaining Challenges”, Symposium on Low Power Electronics and Design,132-134,2013.

[6]. Patricia Brown, Alan White, and Thomas Green.," Design and Implementation of Low-Power Memristive ADCs for Embedded Systems ” Analog Integrated Circuits and Signal Processing , Vol. 107 Issue 2, 2021.

[7]. Viswanathan N, K. Paramasivam and K. Somasundaram, “Exploring Optimal Topology and Routing Algorithm for 3D Network on Chip”, American Journal of Applied Sciences 9 (3): 300-308, 2012.

Sources

1	https://research.uni-luebeck.de/en/publications/controlling-real-memristors-in-embedded-systems INTERNET 2%
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