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Design and Implementation of a High-Speed Non-Overlapping Mealy Sequence Detector for Digital Communication

Banothu Bapuji[1], Salivoju Laharika[2]
[1]*M. Tech I-Year, VLSI System Design, CVR College of Engineering, Hyderabad, Telangana, India.*
[2]*B. Tech III-Year, ECE, Scient Institute of Technology, Hyderabad, Telangana, India.*

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Abstract: *With the fast progressions in innovation, the improvement of proficient and speedier communication gadgets has gotten to be vital to play down wrong communication. This requires strong blunder discovery and rectification instruments in different areas, counting advanced communication, fawning communication, managing an account, and security applications. In this work, we display the plan of a Mealy-type non-overlapping grouping locator particularly for the grouping '01111110'. The non-overlapping plan was chosen due to its capacity to reset itself after recognizing the desired arrangement, improving its pertinence in real-world scenarios. The Coarse machine was chosen for its focal points in speed and less states compared to Moore machines. The plan was executed, synthesized, and recreated utilizing Xilinx ISE 14.7 on the ZYNQ FPGA stage. Our comes about illustrate that the optimized plan accomplishes noteworthy advancements in range productivity, control utilization, and delay, making it a exceedingly compelling arrangement for advanced communication frameworks.*

Key words: *Sequence Detector, Mealy Machine, Non-overlapping Design Digital Communication, Error Detection, Xilinx ISE, ZYNQ FPGA, Power Consumption, high speed operation.*

I.INTRODUCTION

Grouping finders are basic components in computerized frameworks, working as consecutive limited state machines that recognize and confirm particular bit designs inside information streams. Their essential part is to guarantee the astuteness and exactness of transmitted information, which is significant in a assortment of applications, especially in communication frameworks. Within the domain of advanced communications, arrangement locators play a crucial part in blunder location and adjustment, where they are utilized to screen approaching data [1][3] streams and distinguish predefined arrangements. This capability is especially noteworthy in remote information transmission and fawning communication, where information is transmitted through loud channels which will present blunders.

Computerized communication frameworks regularly utilize different balance strategies such as Twofold Sufficiency Move Keying (Loll), Double Stage Move Keying (BPSK), Quadrature Stage Move Keying (QPSK), and Twofold Recurrence Move Keying (BFSK). Amid these transmissions, the astuteness of the information can be compromised due to equipment defects, obstructions, or natural components, driving to inaccurate information being gotten. For occasion, a transmitted bit arrangement of '10101' may be changed to '10110' upon gathering, coming about in potential miscommunication. To moderate these issues, grouping locators are utilized to confirm the rightness of gotten bits, subsequently guaranteeing that the information transmitted matches the aiming data. They are especially vital in security applications, such as managing an account, where arrangement finders approve passwords by checking in case an entered arrangement matches the put away grouping within the framework.

In this work, we centre on the plan of a Mealy-type non-overlapping arrangement detector specifically for the arrangement '01111110'. The choice of this particular sequence is noteworthy, because it outlines the capabilities of grouping finders in recognizing particular designs which will be basic for different applications. The non-overlapping plan is advantageous because it resets its state to the beginning condition after effectively identifying the specified bits, upgrading proficiency compared [4] to covering grouping finders. Besides, the Coarse machine engineering is favoured due to its diminished number of states, which leads to speedier yield reactions compared to Moore machines.

The following fig shows the mealy machine block diagram.

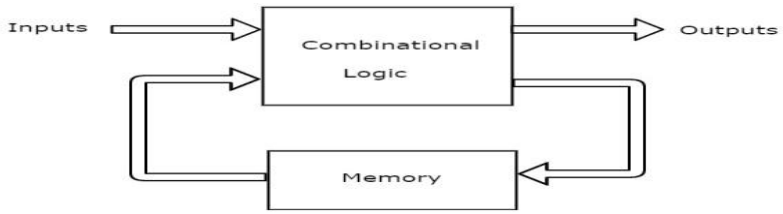

Fig-1: Block Diagram for Mealy machine

The usage of the arrangement finder was carried out utilizing Verilog HDL and confirmed utilizing the Xilinx ISE device on the Zynq board stage. This execution centres on accomplishing moo control utilization whereas keeping up high-speed execution, which is fundamental for advanced computerized frameworks that require productivity and unwavering quality. Comprehensive examinations were performed, counting appraisals of control utilization, delay, and region utilization, to guarantee that the plan meets the vital execution and asset imperatives for viable applications. By concentrating [2][5] on the arrangement '01111110', this work not as it were illustrating the usefulness of grouping locators but too highlights their basic part in keeping up information judgment in computerized communications, hence contributing to the unwavering quality and proficiency of advanced frameworks.

II.LITERATURE SURVEY

1. **Finite State Machine-Based Sequence Detectors in Communication Systems** This paper discusses the design of sequence detectors using FSMs in communication systems, focusing on their role in detecting specific patterns in digital bitstreams. It highlights the use of Mealy and Moore models for sequence detection and compares their efficiency, particularly in **error detection and correction**. The advantages of **Mealy machines** in terms of reduced state count and faster response times are emphasized, making them suitable for high-speed data transmission applications.
2. **Design and Implementation of Non-Overlapping Sequence Detectors on FPGA** This paper explores the implementation of **non-overlapping sequence detectors** on FPGA platforms. It reviews different design strategies for non-overlapping sequence detection and explains how such detectors are reset to the initial state after detecting a pattern. The paper highlights the application of these detectors in error detection during **digital communications** and **storage devices** like SSDs. It also discusses the advantages of Mealy-based designs in terms of **resource efficiency** and **timing** on FPGA platforms.
3. **Mealy vs. Moore Models: A Comparative Study for Digital Communication Applications** This survey examines the differences between Mealy and Moore FSM models in digital communication systems, focusing on their use in sequence detection. It provides an analysis of how Mealy machines, with their faster output response due to transition-based output, are better suited for high-speed **digital communication schemes** like **BPSK, QPSK**, and **BFSK**. The paper also touches on the use of sequence detectors in **error correction** and **signal processing**.
4. **Sequence Detectors for Data Integrity and Error Correction in Digital Storage** This paper focuses on the application of sequence detectors in maintaining **data integrity** and performing **error correction** in digital storage systems such as **HDDs and SSDs**. The paper surveys various error detection techniques, including sequence detection in data transmission, and discusses how FSM-based sequence detectors (especially Mealy machines) play a critical role in ensuring that data errors, caused by bit transitions, are identified and corrected.
5. **Applications of Sequence Detectors in Security and Encryption Systems** This survey reviews the use of sequence detectors in **security** and **encryption** applications, such as **password verification** and **secure communication protocols**. It highlights how non-overlapping sequence detectors can be used to verify data sequences, including passwords and authentication keys. The paper underscores the **Mealy machine's** efficiency in detecting correct sequences quickly, making it ideal for **security** and **banking systems** where response time is crucial.

III. PROPOSED ARCHITECTURE

The following fig shows the proposed architecture and the possible states of the mealy finite state machine sequence detector. The sequence detector consists of the 8 states those are S0, S1, S2, S3, S4, S5, S6, S7.
S0=000 is the initial state which detects -0
S1=001 is the first state which detects -1
S2=010 is the second state which detects -1
S3=011 is the third state which detects -1
S4=100 is the fourth state which detects -1
S5=101 is the fifth state which detects -1
S6=110 is the sixth state which detects -1
S7=111 is the seventh state which detects -0

After detection of the sequence, the output sets to high, and after that, it goes to the reset state and searches for the next sequence. The main advantage of the non-overlapping sequence detector is that it resets itself to the initial state after the sequence pattern detection, and it is mostly used rather than the overlapping sequence detectors.

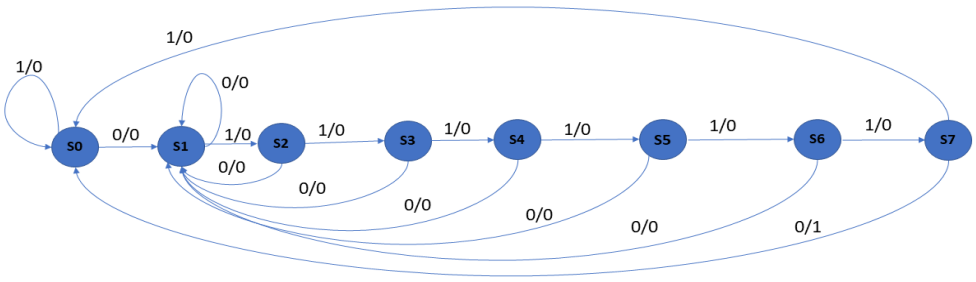

Fig-1: proposed architecture for the mealy type sequence detector "01111110".

The following table shows the input and output signals of the proposed mealy-type non-overlapping sequence detector.

S . No	Pin Name	Direction	Width	Description
1	Out	Output	1	Output Signal
2	In	Input	1	Input Signal
3	Rst	Input	1	Reset Signal
4	clk	Input	1	Clock Signal

Table-1: Input and output signals of the proposed non overlapping mealy type sequence detector.

IV.HDL IMPLEMENTATION

The proposed architecture is implemented using the behavioural modelling Verilog HDL language and simulated and synthesized using the Xilinx ISE 14.7 on the Zynq Board platform.

The following fig shows the schematic diagrams obtained during the synthesis of the proposed architecture in the Xilinx ISE 14.7 on the Zynq Board platform.

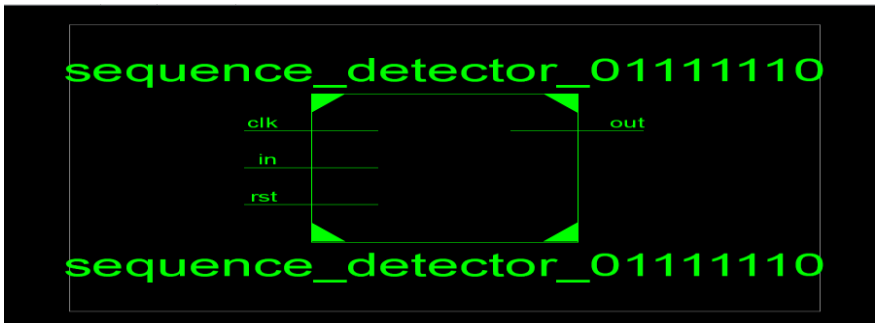

Fig-2: Block Diagram schematic of proposed sequence detector

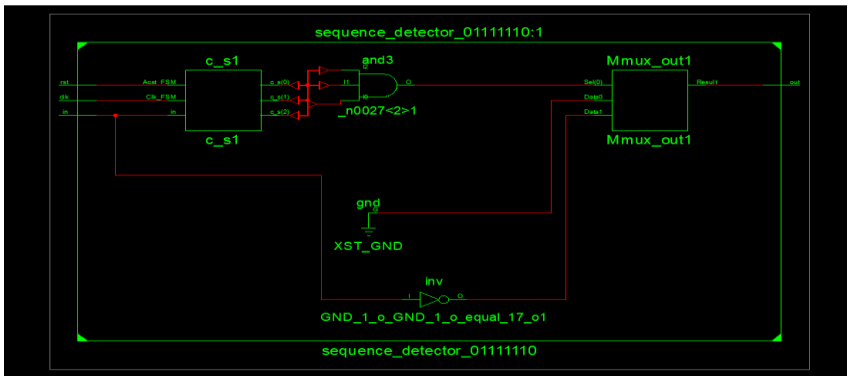

Fig-3: RTL Schematic of proposed sequence detector

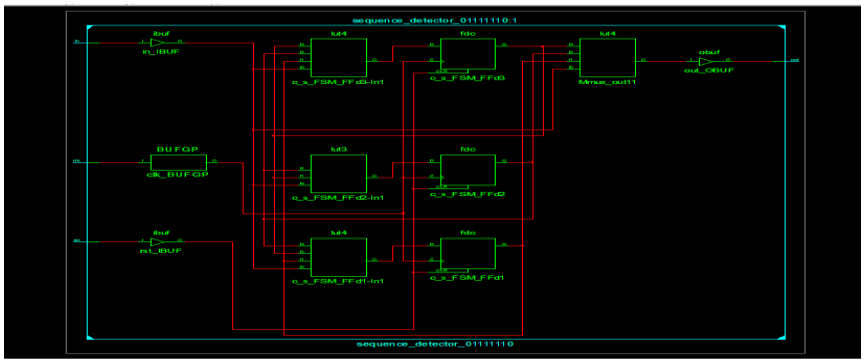

Fig-4: Technology schematic of proposed sequence detector

The above fig shows the RTL schematic and the technological schematic of the proposed mealy type non overlapping sequence detector.

V.RESULTS

The following fig shows the output waveform of the proposed sequence detector by giving a correct sequence.

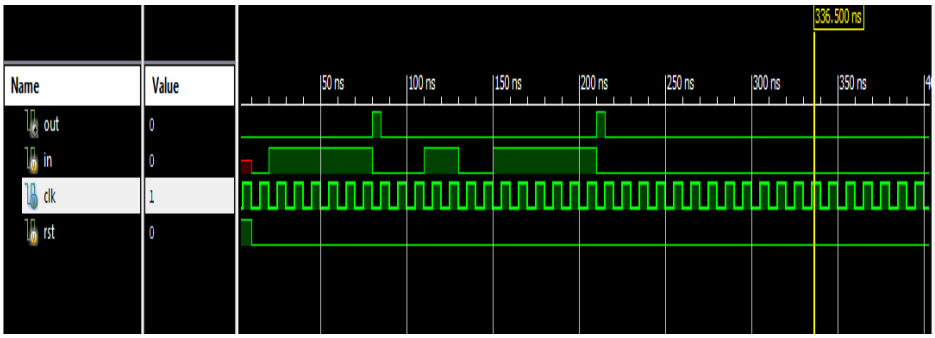

Fig-5: Output waveform for correct sequence-01111110.

In the above fig., the output sets to high after successful detection of the input sequence, and after that, it sets to reset state (initial state).

The following fig shows the output waveform of the proposed sequence detector by giving a random sequence.

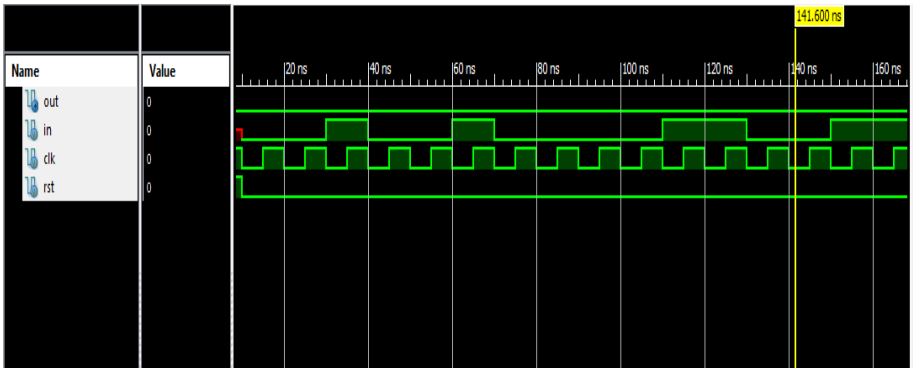

Fig-6: Output waveform for random sequence-001001000011.

The following fig shows the area utilization in the Zynq FPGA board by the proposed mealy type non-overlapping sequence detector.

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	3	35200	0%
Number of Slice LUTs	4	17600	0%
Number of fully used LUT-FF pairs	0	7	0%
Number of bonded IOBs	4	100	4%
Number of BUFG/BUFGCTRLs	1	32	3%

Fig-7:Area utilization by the proposed sequence detector on Zynq Board.

The following fig shows the power analysis results on the ZYNQ FPGA Board.

Device	
Family	Zynq-7000
Part	xc7z010
Package	clg400
Temp Grade	Commercial
Process	Typical
Speed Grade	-3

On-Chip	Power (W)	Used	Available	Utilization (%)
Clocks	0.000	1	---	---
Logic	0.000	4	17600	0
Signals	0.000	6	---	---
IOs	0.000	4	230	2
Leakage	0.100			
Total	0.100			

Fig-8: Power Consumption by the proposed sequence detector on Zynq Board.

The following fig shows the delay analysis results of the proposed sequence detector on the ZYNQ FPGA Board.

```
Data Path: in to out
                                   Gate     Net
  Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
  ----------------------------------------  ------------
   IBUF:I->O             4   0.000   0.470  in_IBUF (in_IBUF)
   LUT4:I0->O            1   0.043   0.279  Mmux_out11 (out_OBUF)
   OBUF:I->O                 0.000          out_OBUF (out)
  ----------------------------------------
  Total                      0.793ns (0.043ns logic, 0.750ns route)
                                     (5.4% logic, 94.6% route)
```

Fig-9: Delay obtained by the proposed sequence detector on Zynq Board.

VI.CONCLUSION

In conclusion, this work presents the design of a Mealy-type non-overlapping sequence detector for the sequence **'01111110'**. The design was successfully simulated and synthesized using Xilinx ISE 14.7 on the ZYNQ FPGA platform. We explored the critical role of sequence detectors in various applications, including digital communication, satellite communication, banking applications, and security/encryption systems. The results of our implementation demonstrate significant advantages, including low power consumption of **100 milli watts**, minimal area utilization, and high-speed operation with a delay of **0.793 ns**. By opting for a non-overlapping Mealy machine, we effectively reduced the number of states, thereby enhancing the efficiency of the detector. This non-overlapping design, which resets to the initial state after detecting the specified sequence, proves to be a versatile and practical solution for real-world applications, ensuring reliable performance in diverse scenarios.

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