

Low-Power Artificial Neural Network Implementation on Artix-7 FPGA Using Reversible Logic

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Abstract: This paper presents an energy-efficient hardware implementation of an Artificial Neural Network (ANN) using reversible logic gates. The proposed ANN design is implemented in Verilog HDL and tested on various FPGA platforms, including Zynq-7000, Virtex-7, Kintex-7, and Artix-7. The novelty of this work lies in leveraging reversible logic gates, such as the Peres gate, to construct fundamental arithmetic units like half adders, full adders, a 4-bit ripple carry adder (RCA), and a 4-bit array multiplier, ultimately forming the neuron structure. The power consumption analysis across different FPGA architectures highlights the efficiency of the proposed approach, with Artix-7 achieving the lowest power consumption at 0.077W. The results demonstrate significant power savings compared to conventional ANN implementations, making this design suitable for low-power AI/ML Applications.

Key words: Reversible Logic, Artificial Neural Network (ANN), FPGA, Low-Power Design, Verilog HDL, Peres Gates.

I. INTRODUCTION

With the rapid advancement of artificial intelligence (AI), hardware implementations of neural networks have gained significant attention due to their efficiency and real-time processing capabilities. However, conventional Artificial Neural Network (ANN) implementations on FPGA suffer from high power consumption due to irreversible logic computations. These traditional approaches lead to energy dissipation in the form of heat, which significantly affects the performance and longevity of FPGA-based systems.

To address this challenge, we explore the potential of reversible logic computing, an emerging paradigm that significantly reduces power consumption while ensuring data integrity. Reversible logic gates, such as the Peres gate, Fredkin gate, and Toffoli gate, have been widely studied in low-power VLSI design due to their ability to [1][2] prevent information loss, which is a primary source of energy dissipation in conventional CMOS circuits. According to Landauer's principle, erasing a single bit of information results in energy dissipation of at least $kT\ln(2)$ joules, where k is Boltzmann's constant and T is the operating temperature. By designing ANN architectures using reversible arithmetic circuits, we can drastically minimize energy loss, making them ideal for power-constrained AI/ML applications.

In this work, we propose an energy-efficient ANN architecture using reversible logic-based arithmetic units, implemented in Verilog HDL and synthesized on various FPGA platforms, including Zynq-7000, Virtex-6, Virtex-7, Kintex-7, and Artix-7. The experimental results demonstrate a significant reduction in power consumption, with Artix-7 achieving the lowest power consumption at 0.077W. This research establishes a foundation for the integration of reversible computing techniques in AI hardware, offering a sustainable solution for power-efficient machine learning applications.

II. LITERATURE REVIEW

Several works have explored low-power ANN designs on FPGA, focusing on optimization techniques like pipelining, approximate computing, and custom Datapath architectures. However, most of these approaches still rely on conventional CMOS-based logic, leading to inevitable energy dissipation. In contrast, reversible logic computing offers a promising alternative, significantly reducing power consumption while maintaining computational accuracy.

2.1 Existing Low-Power ANN Implementations

Research has focused on approximate computing techniques, where small reductions in accuracy result in significant power savings. However, this approach may not be suitable for all applications.

Pipelining and parallelism have been used to optimize [3][4] computation, but these methods often lead to increased area utilization.

Conventional FPGA-based ANN implementations still suffer from high power consumption due to irreversible logic gates.

2.2 Application of Reversible Logic in VLSI

Prior studies have demonstrated the use of reversible logic in arithmetic circuits such as adders and multipliers, but its application in ANN-based AI/ML models remains largely unexplored.

This paper presents the first implementation of a fully reversible ANN architecture on FPGA, demonstrating superior power efficiency.

III. PERES GATE

The **Peres Gate** is a **3×3 reversible logic gate** used in **quantum computing, low-power VLSI design, and arithmetic circuits**. It has three inputs and three outputs, ensuring **bijective mapping** for reversibility. This gate is highly efficient due to its **low quantum cost, minimal garbage output (only one), and reduced power consumption**. It is **universal**, meaning it can be used to [5] construct any Boolean function, making it a fundamental component in **reversible logic, nanotechnology, and optical computing**. Its **scalability and efficiency** make it ideal for designing energy-efficient circuits in advanced computing applications.

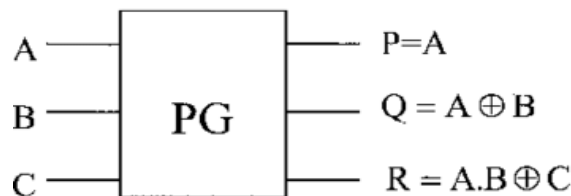


Fig-1: Block Diagram of the Peres Gate

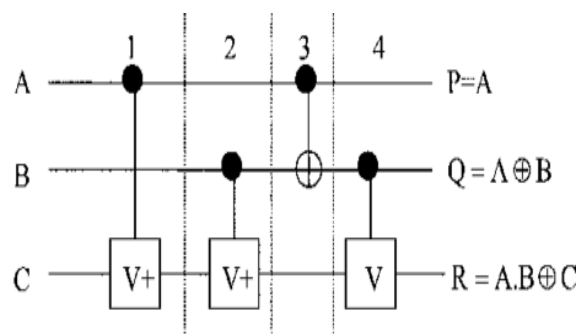


Fig-2: Quantum level Diagram of the Peres gate

IV. PROPOSED METHODOLOGY

4.1 Reversible Logic-Based ANN Design

The proposed ANN consists of the following key The proposed **Artificial Neural Network (ANN)** is designed using **reversible logic-based arithmetic units**, ensuring efficient computation with minimal power dissipation, making it highly suitable for FPGA-based implementations. The core components of this ANN include **Peres gate-based half adders and full adders**, which provide a low-power solution for arithmetic operations due to their reversibility and minimal quantum cost. These adders form the basis of a **4-bit Ripple Carry Adder (RCA)**, which enables multi-bit addition by cascading full adders, where the carry propagates sequentially through each stage. Additionally, a **4-bit Array Multiplier** is implemented to perform the essential multiplication operations required for weighted sum calculations in neural processing. This multiplier efficiently generates partial products and sums them using Peres gate-based adders, ensuring optimized power and delay performance. These arithmetic units collectively form the **Neuron Block**, which is responsible for computing the weighted sum of inputs, a fundamental operation in artificial neurons. The entire ANN design is implemented using **Verilog HDL**, optimized for FPGA synthesis, and verified through **RTL simulation and timing analysis** to ensure correctness, high speed, and efficient resource utilization. The use of **reversible logic** significantly reduces power consumption and enhances computational efficiency, making this ANN architecture well-suited for **hardware-accelerated AI applications, low-power VLSI designs, and real-time neural network processing on FPGA platforms**.

The following is the artificial neural network which I have designed

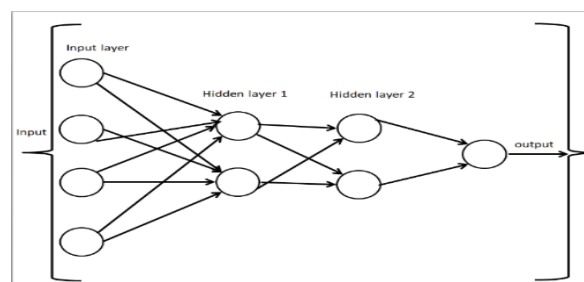


Fig-3: Proposed Artificial Neural Network

The following fig shows the Implementation block diagram of ANN

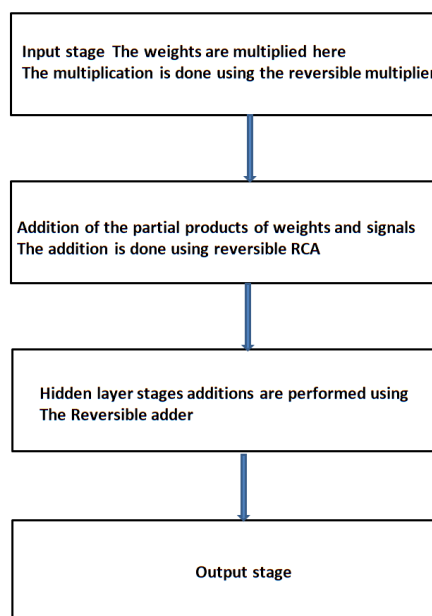


Fig-4: Block Diagram of the Proposed ANN

The following are the few formulas which I have implemented for the artificial neural network

V. HDL IMPLEMENTATION

The proposed Artificial Neural Network (ANN) architecture is designed and implemented in Verilog HDL, utilizing reversible logic-based arithmetic units to enhance computational efficiency while minimizing power consumption. The architecture is simulated using Xilinx ISE, ensuring precise validation and optimization for FPGA-based deployment. The key modules in this design include a Full Adder using Peres Gate, a 4-bit Ripple Carry Adder (RCA), a 4-bit Array Multiplier, and a Neuron Model Construction, each contributing to the overall efficiency and functionality of the ANN.

The Full Adder using Peres Gate forms the fundamental building block for arithmetic operations. Since Peres gates are reversible, they help in reducing power dissipation and quantum cost, making them highly efficient for low-power VLSI applications. The 4-bit Ripple Carry Adder (RCA) is built using multiple full adders, where the carry generated in one stage propagates to the next. This module is crucial for performing multi-bit addition operations, ensuring low-power arithmetic computation in neural processing.

The 4-bit Array Multiplier is another key component, responsible for performing weighted sum calculations in the neuron model. It generates partial products and sums them efficiently using Peres gate-based full adders, ensuring a balanced trade-off between power, area, and computation speed. The Neuron Model Construction integrates these arithmetic units to implement the fundamental computational operations of an artificial neuron. It performs the weighted summation of inputs, a crucial step in neural network processing, and prepares data for the activation function.

Each module undergoes extensive validation through RTL simulation, functional verification, and synthesis analysis in Xilinx ISE, ensuring accurate performance and hardware feasibility. The synthesis results confirm optimal power and area trade-offs, making this ANN architecture highly suitable for low-power AI applications, FPGA-based neural network accelerators, and advanced VLSI designs. The use of reversible logic-based arithmetic units further enhances the overall efficiency, making it a promising approach for next-generation hardware implementations of artificial intelligence.

VI. RESULTS AND DISCUSSION

6.1 RTL and Timing Analysis

The following fig shows the RTL schematic of the Reversible Peres gate

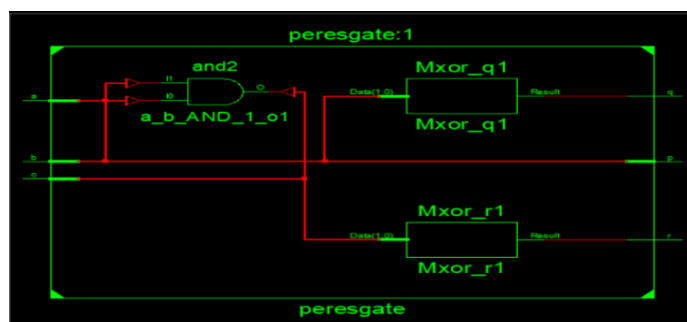


Fig-5: RTL schematic of the Reversible Peres gate

The following fig shows the RTL schematic of the Reversible 1 bit full adder

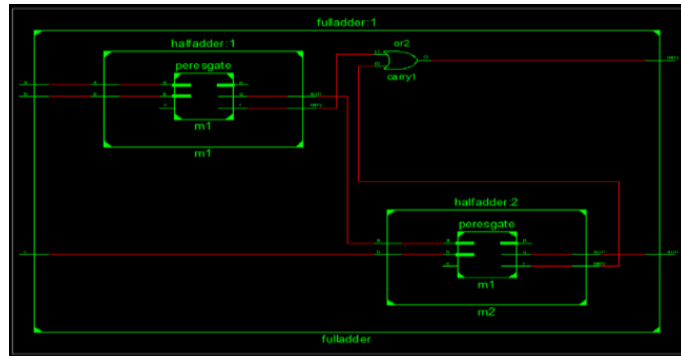


Fig-6: RTL schematic of the Reversible 1 bit full adder

The following fig shows the RTL schematic of the Reversible 4-bit RCA

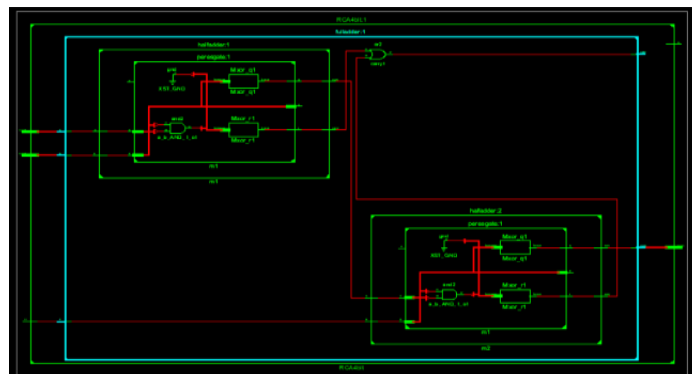


Fig-7: the RTL schematic of the Reversible 4-bit RCA

The following fig shows the RTL schematic of the Reversible 4-bit array multiplier

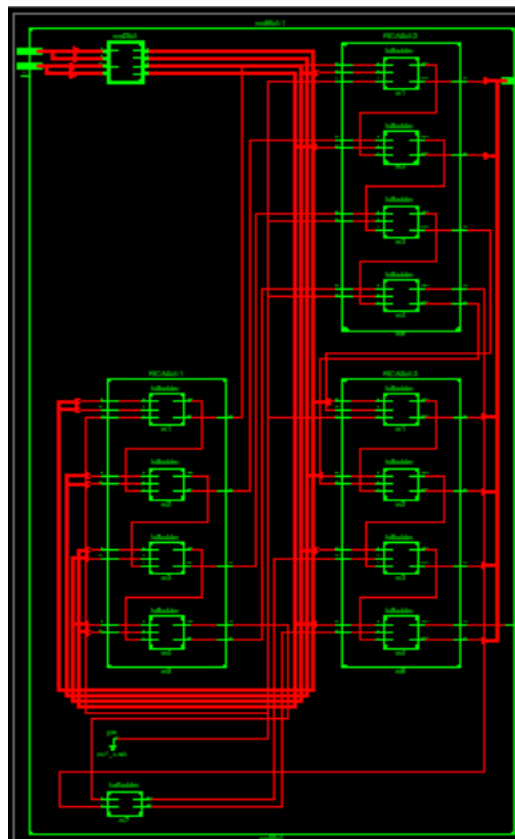


Fig-8: RTL schematic of the Reversible 4-bit array multiplier

The following fig shows the RTL schematic of the Reversible Artificial neural network with 4 input and 8 weights and 4 bias inputs

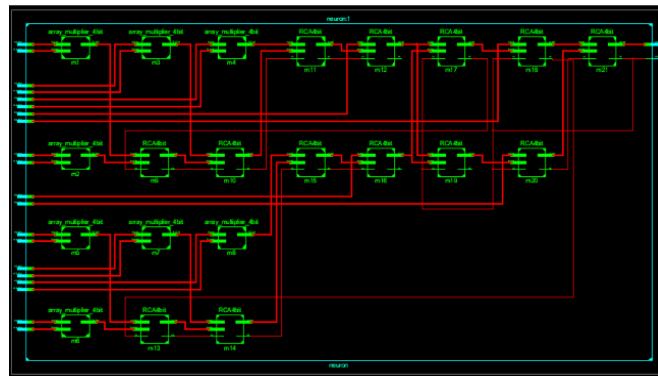


Fig-9 :RTL schematic of the Reversible Artificial neural network

The following fig shows the Technology schematic of the Reversible Artificial neural network with 4 input and 8 weights and 4 bias inputs

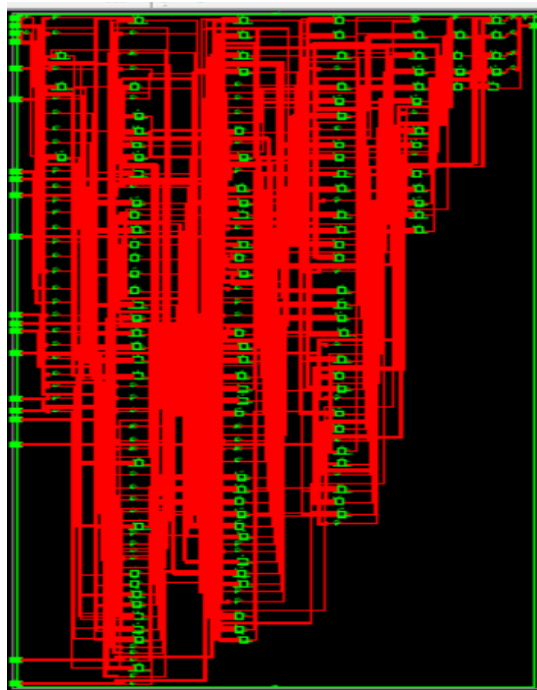


Fig-10: Technology schematic of the Reversible Artificial neural network

The following fig shows the Timing diagram of the Reversible Artificial neural network with 4 input and 8 weights and 4 bias inputs

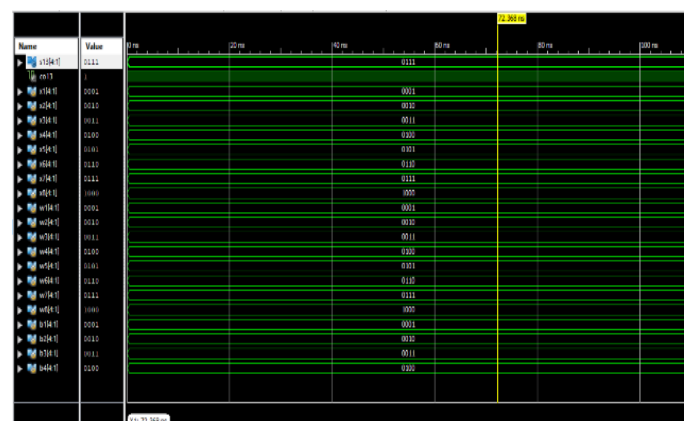


Fig-11 :Timing Diagram of the Reversible Artificial neural network

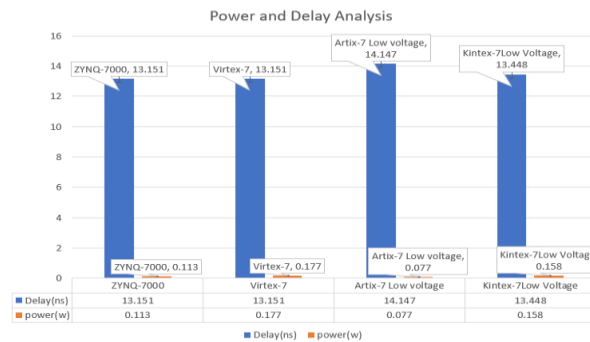


Fig-12 :Power and Delay Analysis Across FPGA Platforms

VII. CONCLUSION AND FUTURE WORK

This work presents a **low-power artificial neural network (ANN) architecture** leveraging **reversible logic-based arithmetic circuits**, including **Peres gate-based adders and multipliers**, to optimize power consumption and computational efficiency. The ANN is implemented in **Verilog HDL**, synthesized, and simulated using **Xilinx ISE** across various FPGA platforms, with **Artix-7 achieving the lowest power consumption at 0.077W**. The use of **reversible logic** significantly reduces **energy dissipation**, aligning with **Landauer's principle**, which states that information loss leads to power dissipation. By eliminating unnecessary power losses and reducing **quantum cost**, the proposed design ensures **efficient area utilization, lower heat generation, and improved performance**. The results demonstrate that **reversible ANN implementations offer a sustainable solution for AI/ML applications in power-constrained environments**. Future work includes extending this approach to **higher-bit architectures, optimizing quantum cost further, and exploring hybrid reversible-quantum computing models for neuromorphic hardware**.

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