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Three-Phase F-Type Inverter Topology for Grid Connected Inverter

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Abstract: *In renewable energy systems, efficient and stable integration with the electrical grid remains a pivotal challenge. This research paper investigates the implementation of a grid-connected three-level F-type inverter with dq frame control, specifically tailored for three-phase systems. Compared to traditional two-level inverters, the pro- posed inverter architecture leverages a three-level configuration to enhance output quality and reduce harmonic distortion. By employing dq frame control, the system achieves effective decoupling of active and reactive power, leading to improved dynamic performance and grid synchronization. The study presents a detailed analysis of the inverter's operational principles, control strategy, and performance metrics. Simulation results demonstrate the efficacy of the three-level F-type inverter in maintaining grid stability, minimizing total harmonic distortion, and ensuring reliable power delivery under varying load conditions. This research contributes to advancing inverter technology for renewable energy applications, offering a robust solution for efficient grid integration and enhanced power quality. The dq frame control technique is thoroughly examined, highlighting its advantages in simplifying the control algorithms and improving the system's overall stability. Key metrics such as efficiency, response time, and harmonic performance are analyzed, showcasing the benefits of the three-level configuration in mitigating common issues associated with lower-level inverters. Practical implementation aspects, including hardware considerations and potential challenges, are also discussed.*

Key Word: *Three-Phase F-Type Inverter; SPWM, dq frame, Condction Losses, Switching Losses*

I. INTRODUCTION

The design and control of power-conditioning circuits, particularly DC-AC converters (inverters), have been a longstanding focus of research in Power Electronics. The global imperative drives this ongoing interest to develop sustainable, Solar, wind, hydro, geothermal, and biomass power sources, with smart grids, energy storage, and electric vehicles. Inverters play a vital role in various critical applications, including high-voltage direct-current (HVDC) transmission systems [1], Flexible AC Transmission Systems (FACTS) are power electronics-based systems that provide control and flexibility to AC transmission systems, enabling efficient and reliable transmission of electrical power [2], renewable Energy Grid Integration refers to the process of connecting renewable energy sources, such as solar, wind, and hydro power, to the electrical grid, enabling the efficient and reliable transmission of clean energy to meet growing electricity demands [3], energy Storage Systems (ESS) are technologies that enable the storage of electrical energy for later use, helping to stabilize the grid, optimize energy consumption, and provide backup power during outages [4], railway and Vehicle Traction refers to the use of electric power to propel trains, trams, and other vehicles, providing efficient, reliable, and environmentally friendly transportation [5-7], marine propulsion refers to the systems and technologies used to propel ships, boats, and other watercraft through the water. Efficient and reliable marine propulsion systems are crucial for the safe and economic operation of vessels [8], Hydro-Pumped Storage (HPS) is a type of energy storage technology that stores excess energy by pumping water from a lower reservoir to an upper reservoir during off-peak hours.

During peak hours, the water is released back to the lower reservoir, generating electricity through hydroelectric turbines [9], grinding and Rolling Mills are machinery used in various industries, such as mining, cement, and steel, to process and transform raw materials into finished products [10], Compressors and Extruders are machinery used in various industries to process and transform materials [11] to mention a few. To facilitate these deployments, power electronics inverters must meet specific requirements, including a wide range of operational output responses. Currently, Multilevel Inverters (MLIs) are the most suitable devices for meeting these demands, offering superior performance, flexibility, and reliability [12].The inherent advantages and potentials of Multilevel Inverters (MLIs) have been widely recognized, particularly in industrial applications where they have demonstrated significant positive impacts. As a result, there has been a surge in the development and implementation of MLI configurations include NPC, T-Type, and F-Type, with control strategies like SVM, SPWM, and carrier-based PWM techniques [13-15].Crucial examination of recently developed Multilevel Inverter (MLI) topologies reveals that they are, in fact, variations or hybrids of conventional MLI configurations.he Cascaded H-Bridge (CHB) MLI stands out because it naturally supports higher-level output voltages by using separate DC sources for each H-bridge, thereby avoiding capacitor

voltage imbalance issues.On the other hand, Diode-Clamped (Neutral-Point Clamped) and Flying Capacitor MLIs struggle with increasing levels due to voltage imbalance in the capacitor banks. As the number of levels increases, maintaining equal voltage distribution across capacitors becomes increasingly difficult, leading to control complexity and instability. Advanced control strategies, such as balancing algorithms and active voltage regulation, have been explored, but they often add to the system's computational and implementation complexity.

Figures 1(a) and 1(b) pole structure of Multilevel Inverters (MLIs). The traditional diode-clamped topology, also known as the Neutral-Point-Clamped (NPC) inverter, is shown in Fig. 1(a). This configuration synthesizes 3-level output voltages using half-rated voltage switches.Contrast, the 3-level T-type inverter (3LT2I), depicted in Fig. 1(b), employs active clamping to regulate the output voltage. Although both configurations utilize the same number of active power switches, the 3LT2I compromises the voltage rating of two switches, which are now High-voltage blocking switches. However, the bidirectional switch retains its reduced voltage stress rating. Notably, the 3LT2I exhibits significantly lower conduction losses in different multilevel inverters (MLIs), the Diode-Clamped (Neutral-Point Clamped, NPC) Inverter, primarily due to the reduced number of semiconductors in series (only two) along the current path [16].The 3-level T-type inverter (3LT2I) also benefits from a simpler circuit design by eliminating the need for clamping diodes, reducing component count and overall system complexity compared to the Neutral-Point-Clamped (NPC) inverters: reduced component count.Additionally, both inverter topologies achieve lower total harmonic distortion (THD) and reduced electromagnetic interference (EMI), resulting in improved power quality and better performance in high-efficiency applications,making them attractive solutions for high-performance applications. Fig. 1(b) reveals that 50% of the power switches per leg in the 3-level T-type inverter (3LT2I) have a full dc-link reverse blocking voltage rating. However, the three-level F-type inverter (3LFTI) is an advanced topology designed to improve power conversion efficiency and reduce harmonics compared to conventional two-level inverters in the proposed the three-tevel F-type inverter (3LFTI) to has an unique topology where only one power switch per phase-leg is used. This differs from conventional neutral-point-clamped (NPC) or flying capacitor (FC) three-level inverters, which typically require two or more switches per phase-leg.This design modification presents opportunities for further optimization and cost reduction. Operationally, the proposed 3LFTI inverter, similar to the 3LT2I, features only two semiconductors in series within the current path decreases the voltage burden on the power switches, effectively reducing conduction losses significantly when compared to NPC and T-type inverters.

Furthermore, In the 3LFTI power circuit (Fig. 1c), the voltage stress on one of the power switches is reduced by half compared to the T-type inverter, enhancing overall efficiency, performance, and reliability, especially with the latest high-voltage power switch modules rated at 6.5 kV and 1200 A [17].

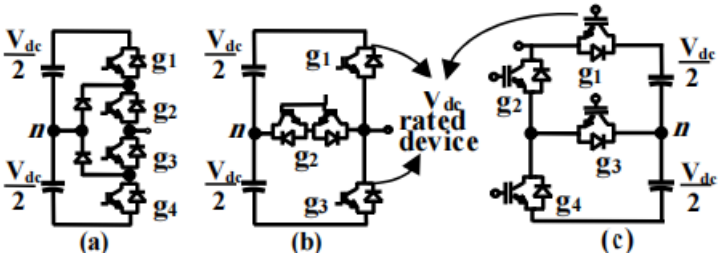

***Figure 1**.Phase-leg configurations of three-level multilevel inverter power circuits: (a) Neutral-Point-Clamped (NPC), (b) T-type, (c) F-type.*

The proposed 3-level F-type inverter's characteristic features make it a viable solution for deployment in specific Suitable for applications operating at low and medium voltage levels,offering advantages in terms of efficiency, reliability, and performance. The three-level MLI inverter configurations depicted in Fig. 1 exhibit equivalent operational characteristics.However, they share common challenges, including neutral-point voltage imbalance and low-frequency oscillations of the dc-link capacitor voltages during operation. To address these issues, various technical solutions have been proposed, primarily through the development of advanced Control techniques for Neutral-Point-Clamped (NPC) inverters include various modulation strategies.Two of the most widely the implemented modulation techniques include Space Vector Pulse-Width Modulation (SVPWM) [18-22] and (another technique, likely to be mentioned next, e.g., Sinusoidal Pulse-Width Modulation (SPWM)) [23-27]. The performance equivalence of Space Vector Pulse-Width Modulation (SVPWM) and Sinusoidal Pulse-Width Modulation (SPWM) has been extensively demonstrated and validated in the literature, confirming that both approaches can achieve similar performance characteristics in multilevel inverter applications [28-29].

The proposed F-type inverter generates three-level output voltage waveforms at each inverter leg terminal concerning the neutral point (n) while effectively reducing voltage stress on the switches. Significantly, only 25% of the power switches per phase-leg (one switch) need to withstand the full DC-link reverse-blocking voltage rating.This inherent topological advantage of the 3-level F-type inverter translates to reduced losses and cost, making it an attractive solution for low-voltage and certain medium-voltage applications.

II. MATERIAL AND METHODS

As previously stated, the proposed F-type power circuit differs from the conventional T-type configuration mainly in the blocking voltage rating of one switch, which directly impacts cost, power losses, and overall inverter performance and suitability. Leveraging its unique configuration, a tailored A switching scheme is designed and implemented, and the Sinusoidal Pulse-Width Modulation (SPWM) technique is employed to generate the switching signals. The control approach presented

in [30] is utilized to address two critical aspects: ensuring neutral voltage balancing and minimizing low-frequency oscillations in the DC-link capacitor voltages.

A.Three - Phase Three - Level F-type Inverter with R-load

Figure 1(c) presents the phase-leg power circuit of the F-type inverter, representing a topological enhancement of the T-type inverter design.Specifically, this design leverages the shared emitter junction of the bidirectional switch to achieve reduced voltage stress across the constituent power switches.The F-type inverter topology depicted in Fig. 1c, is engineered to minimize voltage stress on its power switches, it operates equivalently to its diode-free counterpart shown in Fig. 1(b).Consequently, it can synthesize three distinct output voltages relative to the neutral point (n): 0.5Vdc, 0, and -0.5Vdc. In Table 1 provides a comprehensive summary of the switching states of the power switches and the corresponding synthesized inverter output voltages. The notation used is as follows: P, O, and N represent the positive, zero, and negative voltage states of the inverter, respectively. Logic states 1 and 0 denote the on- and off-switching states of the power switches. The three-phase power circuit configuration is illustrated in Fig. 2.

Table 1 Switching states and corresponding synthesized output voltages of the 3LFTI

Inverter state	g 1	g 2	g 3	g 4	Output voltage
P	1	0	1	0	0.5 V dc
0	0	1	1	0	0
N	0	1	0	1	-Vdc

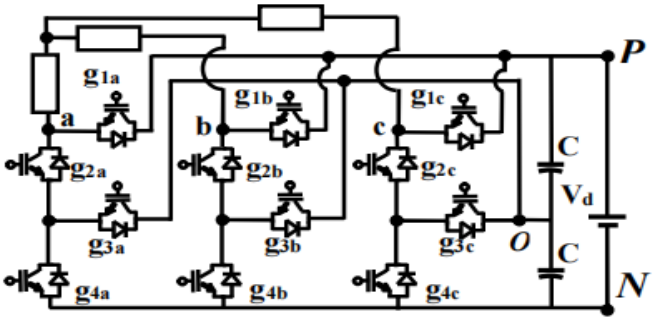

Figure 2. *Three-phase, three-level F-type inverter power circuit*

A review of Table 1 and Fig. 1(c) reveals that switch g1 is subjected to the maximum blocking voltage of Vdc, whereas switches g2, g3, and g4 have a reduced maximum blocking voltage of 0.5Vdc each. Furthermore, it is observed that the proposed F-type inverter, similar to its T-type counterpart, has two semiconductors in series along the current path.

Switching State Transition

Given that each inverter phase-leg's output node can connect to the positive (P), neutral (O), or negative (N) DC-link voltage level, as shown in Fig. 2, a crucial requirement is to ensure seamless switching transitions that operate independently of the load current direction. In essence, the phase current should naturally transition to the correct branch of the F-structured inverter phase-leg, without being influenced by the current direction.

Sinusoidal Pulse-Width Modulation (SPWM) scheme for the proposed F-type inverter

The Sinusoidal Pulse-Width Modulation (SPWM) technique operates on a phase-leg basis, generating gating signals through phase modulation. This method applies the same control strategy to each inverter phase, differing only in the phase angle shift.Consequently, extending SPWM to multi-phase, multilevel systems does not pose significant computational challenges in comparison to Space Vector Modulation (SVM).

However, a significant limitation of SPWM is the inefficient utilization of the DC-link voltage in power converters when employing pure sinusoidal reference signals in the modulation process.To overcome this limitation and expand the modulation index range in the linear modulation region beyond unity, an effective method is to introduce a zero-sequence component using the min-max function principle [28].

This concept was incorporated into the SPWM modulation strategy outlined in [23] and [25] for a three-phase, three-level NPC inverter.By incorporating voltage errors and analytically derived offset signals into the reference signals, effective capacitor bank voltage balancing was achieved, significantly minimizing low-frequency voltage oscillations at the neutral point.Notably, the modulation and control strategy used in the Neutral-Point Clamped (NPC) inverter is the same as that implemented in the

proposed 3LFTI.

The modulation method described in [25] is implemented in the proposed F-type inverter power circuit illustrated in Fig. 2. A brief summary of this technique is presented below.

Table 2. Phase-leg current transitions during switching transitions from P to 0 and 0 to P

g1	g2	g3	T1	D1	T2	D2	T3	D3	Vo	io
1	0	1	1	0	0	0	0	0	P	+
0	0	1	0	0	0	1	1	0	0	+
0	1	1	0	0	0	1	1	0	0	+
1	0	1	0	1	0	0	0	0	P	-
0	0	1	0	1	0	0	0	0	P	-
0	1	1	0	0	1	0	0	1	0	-
0	1	1	0	0	0	1	1	0	0	+
0	0	1	0	0	0	1	1	0	0	+
1	0	1	1	0	0	0	0	0	P	+
0	1	1	0	0	1	0	0	1	0	-
0	0	1	0	1	0	0	0	0	P	-
1	0	1	0	1	0	0	0	0	P	-

Table 3.Phase-leg current changes during switching transitions from N to 0 and 0 to N

g2	g3	g4	T2	D2	T3	D3	T4	D4	Vao	iao
1	0	1	1	0	0	0	1	0	N	-
1	0	0	1	0	0	1	0	0	0	-
1	1	0	1	0	0	1	0	0	0	-
1	0	1	0	1	0	0	0	1	N	+
1	0	0	0	1	0	0	0	0	N	+
1	1	0	0	1	1	0	0	0	0	+
1	1	0	1	0	0	1	0	0	0	-
1	0	0	1	0	0	1	0	0	0	-
1	0	1	1	0	0	0	1	0	N	-
1	1	0	0	1	1	0	0	0	0	+
1	0	0	0	1	0	0	0	1	N	+
1	0	1	0	1	0	0	0	1	N	+

B. 3-level, 3-phase F-type Inverter Grid Connected Power Circuit

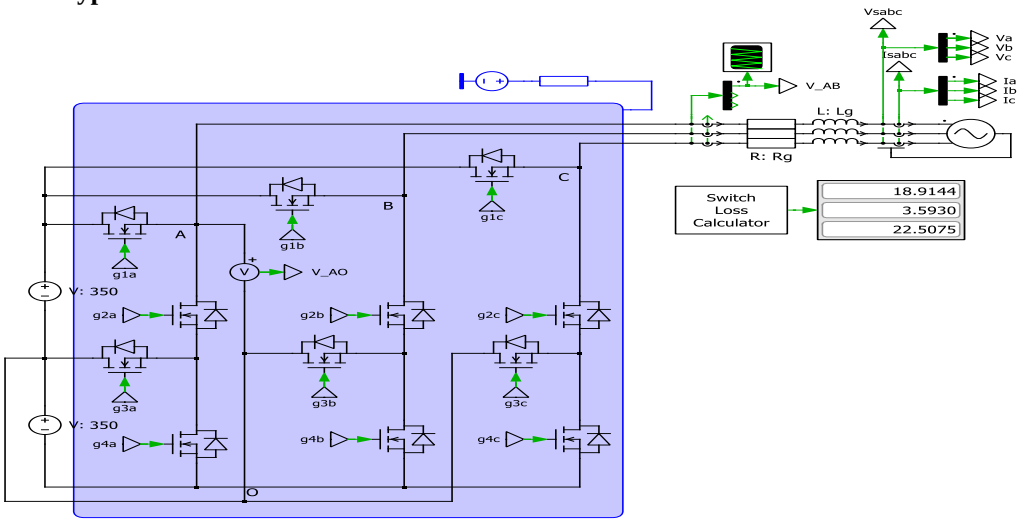

***Figure 3**. 3-PhaseF-Type Grid Connected Inverter*

The DC-Link is a crucial component in a power electronics system, particularly in a three-phase, three-level grid-connected inverter. Its primary function is to store energy from the DC source. In this specific case, the DC-Link voltage is 700V. This voltage level is typical for many industrial power electronics applications.

To synchronize the inverter output voltage with the grid voltage, A PLL is a control system that generates a signal that is synchronized with the grid voltage. The PLL uses a feedback loop to adjust the phase of the inverter output voltage to match the phase of the grid voltage

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Mathematical Model Analysis

Conduction Losses

Conduction loss occurs when the IGBT is in its "on" state and allows current to flow. This loss depends on the on- state voltage and the current flowing through the device.

The conduction loss Pcond, IGBT for an IGBT is calculated as

Pcond(IGBT)=Vceo * i + R0 * i^2

Pcond(Diode)=Vd0 * i +Rd0 * i^2

VCE0, On-state voltage threshold voltage, temperature-dependent

R0, On-state resistance, temperature-dependent

R0 =(Vce2-vce1)/(Ic2-Ic1)

Vce(sat)=Vceo + R0 * Ic

$$P_{cond\ (I)} = \left(\frac{1}{2\pi} + \frac{m * cos(\emptyset)}{8}\right) * V_{CEO} * I_{pk} + \left(\frac{1}{8} + \frac{m * cos(\emptyset)}{3\pi}\right) * R_0 * {I_{pk}}^2$$

$$P_{cond\ (D)} = \left(\frac{1}{2\pi} - \frac{m * cos(\emptyset)}{8}\right) * V_{CDO} * I_{pk} + \left(\frac{1}{8} - \frac{m * cos(\emptyset)}{3\pi}\right) * R_{D0} * {I_{pk}}^2$$

Switching Losses

Switching loss occurs when the IGBT transitions between its "on" and "off" states. During these transitions, the overlap of voltage and current causes energy dissipation.

The switching loss Psw, IGBT per cycle is:

$$P_{SW} = (E_{ON} + E_{OFF}) * F_{SW}$$

$$P_{DIODE} = (E_{REC}) * F_{SW}$$

$$P_{SW} = (E_{ON} + E_{OFF}) * \frac{F_{SW}}{\pi} * \frac{I_{pk}}{I_{nom}} * \frac{V_{dc\ link}}{V_{nom}}$$

$$P_{SW\ DIODE} = (E_{REC}) * \frac{F_{SW}}{\pi} * \frac{I_{pk}}{I_{nom}} * \frac{V_{dc\ link}}{V_{nom}}$$

Fsw = Switching Frequency

Ipk = Peak Collector Current

Inom = Nominal Rated current of Device

V dc link = DC Link Voltage

V nom = Datasheet Dynamic V line

E on = Turn on Energy Losses @ I pk

E off = Turn off Energy Losses @ I pk

E rec = Diode Reverse Recovery Energy Loss @ Ipk

Parameter Ratings of the System

S.No	Parameter	Value
1	SiC MOSFET module	UJ4C075018K4S
2	IGBT Module with diode module	DIM900MIH 12-PG500
3	Grid voltage	415 V
4	Frequency	10 kHZ
5	Resistance	0.01 Ohm
6	Inductance	4 m H
7	DC Link voltage	700V

S=√3 VL IL

Peak Grid Voltage is 338.8 (415 sqrt 2/3)

s= apparent power (kv) = 10KVA

10 KVA=√3*415 I_L

$I_{L=\frac{10000}{\sqrt{3}*415}} = \frac{10000}{1.732*415} = \frac{10000}{718.78}$ =13.912 A

I_L=13.912 A

$I_L = I_M$ *sqrt 2 = 19.61 A

Peak value of grid current 19.6 A

RMS Value I_rms = 19.6/√2 =13.8613 A

Si IGBT

η= Output Power/Output Power +Losses

=1.732∗415∗13.8613/1.732∗415∗13.8613+36.6510

= 99.63 %

SiC MOSFET

η= Output Power/Output Power +Losses =

=1.732∗415∗13.8613/1.732∗415∗13.8613+22.5075

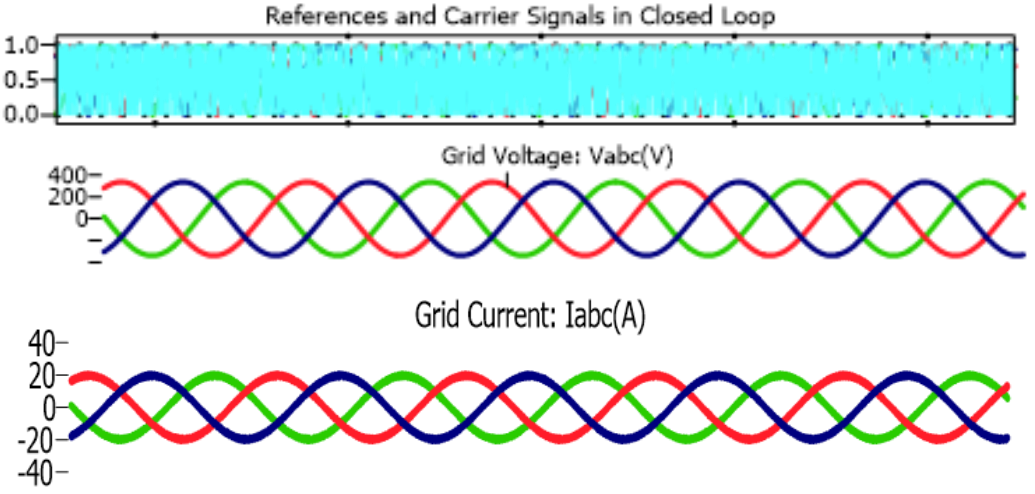
III. PLECS SIMULATION RESULTS

Two carrier signals are typically used per phase for a three-level inverter, forming a multi-carrier PWM strategy,this closed-loop approach enhances the inverter's dynamic response, improves power quality, and ensures compliance with grid requirements by effectively compensating for disturbances and variations in grid conditions.three-phase, three-level F-Type grid-connected inverter, these waveforms could represent phase voltages (Va, Vb, Vc) or phase currents (Ia, Ib, Ic). The sinusoidal nature of these signals indicates that the inverter is operating in a well-regulated manner, likely using Pulse-Width Modulation (PWM) to generate a nearly sinusoidal output after passing through an LC filter.This waveform ensures balanced power delivery to the grid or load, minimizing harmonic distortion and improving power quality. If this represents the output current, the alignment with the voltage waveforms would indicate unity power factor operation, which is ideal for grid-connected inverters. Three-phase, three-level F-Type grid-connected inverter, this waveform could represent line-to-line voltage (Vab) and phase voltage (VaO), or reference and actual waveforms in a closed-loop control system. The waveform, with a higher amplitude, may correspond to the inverter's output voltage. In contrast, the waveform, with a lower amplitude, could indicate the reference signal or a filtered response.When this waveform is passed through an LC filter, it smooths into a sinusoidal AC waveform, ensuring that the inverter can efficiently transfer power to the grid with minimal harmonic distortion. The multilevel structure helps reduce Total Harmonic Distortion (THD) and improve power quality, making it suitable for grid-connected applications.

IV. DISCUSSION

This description provides a detailed overview of a three-phase, three-level F-Type grid-connected inverter using Si (Silicon) and SiC (Silicon Carbide) semiconductor devices. The system is designed and simulated in PLCES software, leveraging manufacturer datasheet parameters for accurate modeling. The inverter, rated at 10 kVA, undergoes real-time simulation to evaluate performance aspects such as voltage, current, active power (P), and reactive power (Q) waveforms. In a three-level inverter, the phase output voltage can switch between +Vdc/2, 0, and -Vdc/2, forming a stepped waveform that resembles a sinusoidal AC signal when filtered through an LC filter. Sinusoidal pulse-width modulation (SPWM) is employed to achieve efficient operation and reduced harmonic distortion. This technique regulates the switching of IGBTs or MOSFETs, optimizing efficiency and ensuring grid compliance. Integrating Si and SiC devices improves overall system performance by reducing switching losses and enhancing thermal stability.

The switching losses in the three-phase, three-level F-Type grid-connected inverter are calculated to be 29.1788 W, while the conduction losses amount to 7.4722 W. This results in total power losses of 36.6510 W, as determined using the module's calculation tool. These losses are influenced by the semiconductor devices (Si and SiC), the switching frequency, and the modulation strategy. Minimizing these losses is essential for improving inverter efficiency and thermal performance.



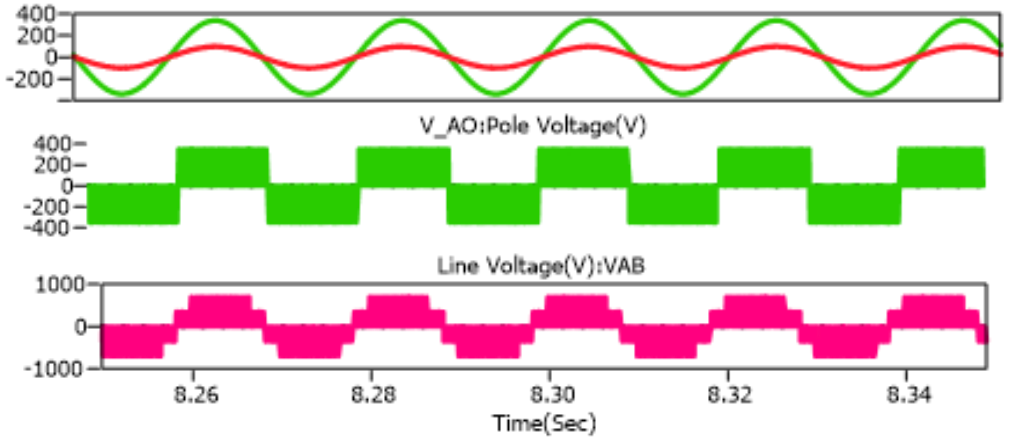


Figure 4. *3-Phase 3L F-Type Inverter Grid Connected Wave-forms*

V.CONCLUSION

Si IGBT and SiC MOSFET Device

The switching losses in the three-phase, three-level F-Type grid-connected inverter are calculated to be 29.1788 W, while the conduction losses amount to 7.4722 W. This results in total power losses of 36.6510 W, as determined using the module's calculation tool. These losses are influenced by the semiconductor devices (Si and SiC), the switching frequency, and the modulation strategy. Minimizing these losses is essential for improving inverter efficiency and thermal performance.

The switching losses in the three-phase, three-level F-Type grid-connected inverter are calculated to be 3.5930 W, while the conduction losses amount to 18.9144 W. As determined using the module's calculation tool, as shown in Figure 1, this results in total power losses of 22.5075 W.

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