

FPGA Implementation of Highway Accident Prevention Traffic Control System Using FSM

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Abstract: Road accidents on national highways and expressways at junctions can be dramatically reduced with an effective traffic control system. In this work, we propose a better traffic control system. The proposed method was designed using the Moore Model FSM in Verilog HDL. The performance of the design is evaluated using various FPGAs to develop a low-power, high-speed architecture.

Key words: FSM-Finite State Machine, FPGA-Field Programmable Gate Array.

I. INTRODUCTION

In India, on national highways and expressways, road accidents are considerably high. Some of the contributing factors to road accidents include improper traffic control at junctions, such as Highway Road and Country Road. The traffic control system is used to control the traffic [1][2] and prevent accidents by giving the proper signal based on crowd detection. The sensors present on the traffic signal will detect the vehicles and give different signals for the different roads. In this work, we have designed a dynamic traffic control system using Moore Model FSM in Verilog HDL, and this work is synthesized and simulated using the XILINX ISE 14.7 software environment.

II. PROPOSED METHOD

The following fig. shows the Moore model finite state machine state diagram of the proposed method for traffic light control systems.

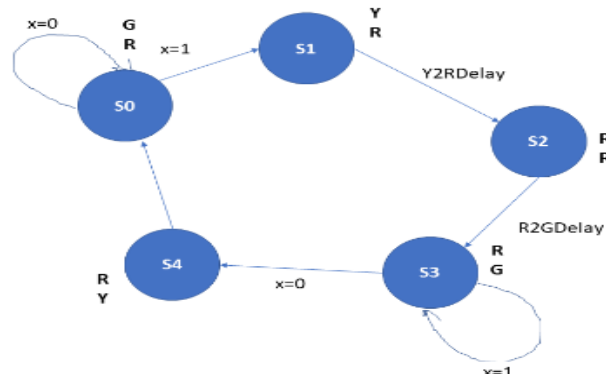


Fig 1: State Diagram of Traffic Light Control System

The above-proposed method shows that the FSM diagram of the traffic light [3][4] control system, in which it consists of five states for both highway roads and country roads.

The following are the states and signals of the traffic light control system:

States	Highway Road	Country Road
S0	Green	Red
S1	Yellow	Red
S2	Red	Red
S3	Red	Green
S4	Red	Yellow

The X value in Fig. 1 indicates the sensor at the country side road.

If X = 0, no vehicles are present on the country side road.

If X = 1, vehicles are present on the country side road.

Initially, the priority is given to the highway side green signal; when the X value [5] at the country side goes to Logic HIGH, then the priority is changed to Country Side Road.

In this system, the delay for red to green and yellow to red is provided, which is from states s1–s3.

III.HDL IMPLEMENTATION

The traffic light control system has been implemented using the Verilog HDL in behaviour modelling, and we have done the power and delay analysis on different FPGS's in the XILINX ISE 14.7 environment.

The following are the RTL schematic, technology schematic, and simulation waveform.

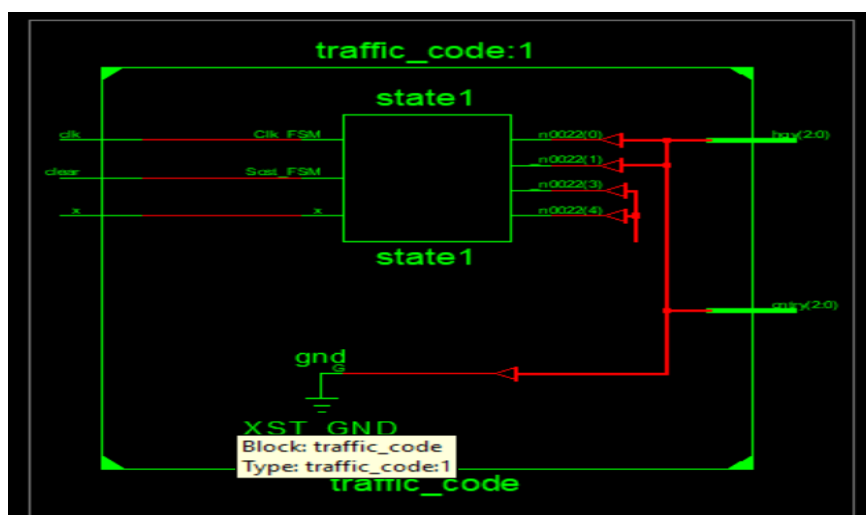


Fig 2: RTL Schematic of traffic light control system

The above fig. shows the RTL schematic of the traffic light control system

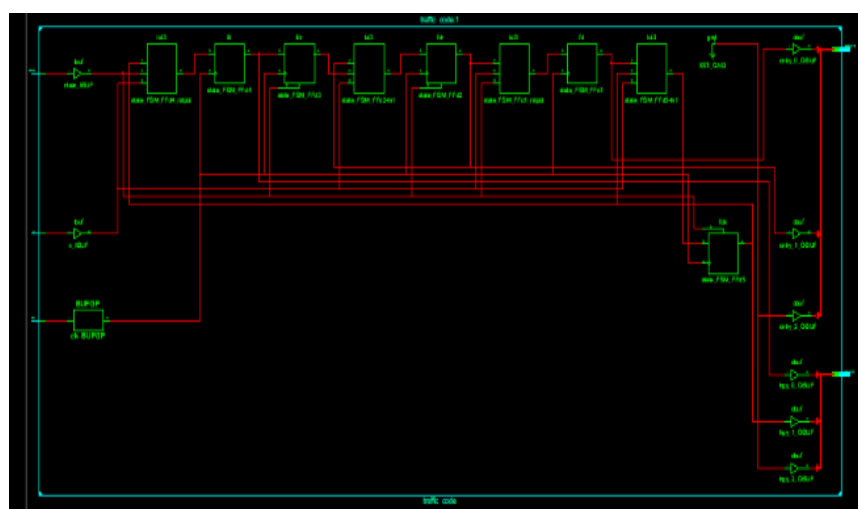


Fig 3 Technology schematic of traffic control system

The above figure shows the technology schematic of the traffic light control system.

IV.RESULT

The below fig. shows the simulation waveform of the traffic light control system.

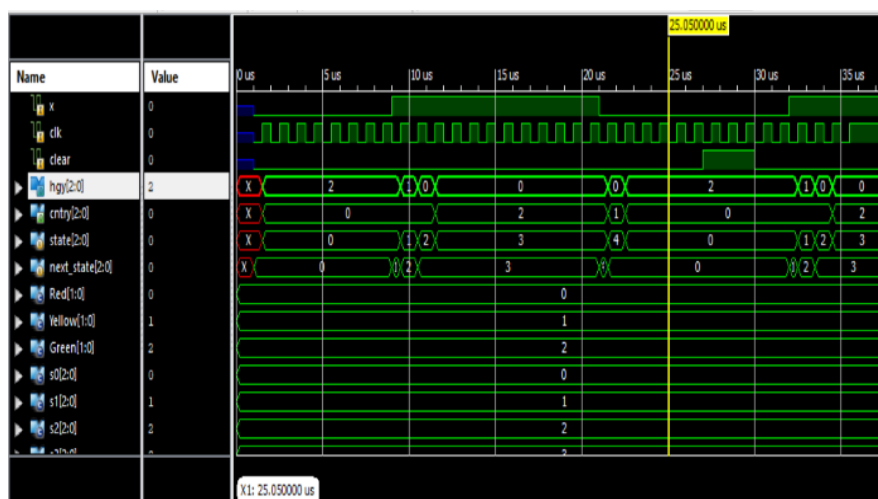


Fig 4 waveform of traffic light control system

The following figure shows a power analysis graph.

The power analysis is done on the various FPGAs, and the values are noted down as shown in the below bar graph.

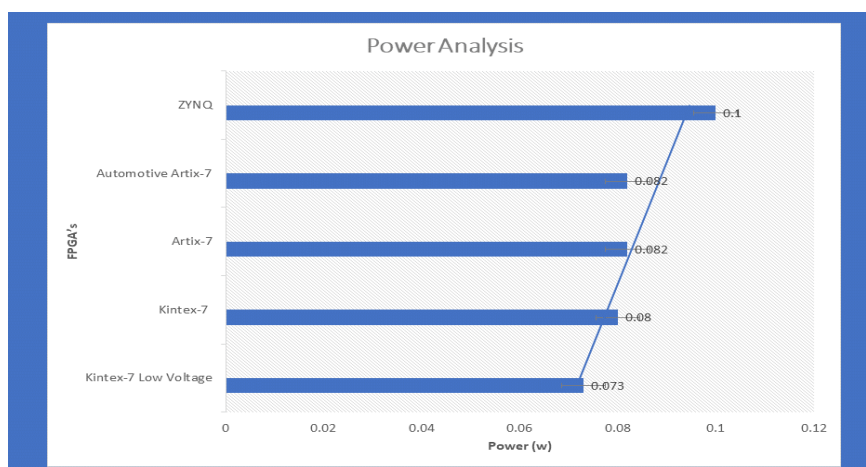


Fig 5: power analysis of traffic light control system

The following figure shows the delay analysis of the traffic light control system. The delay analysis is done on the various FPGAs, and the values are noted down as shown in the below bar graph.

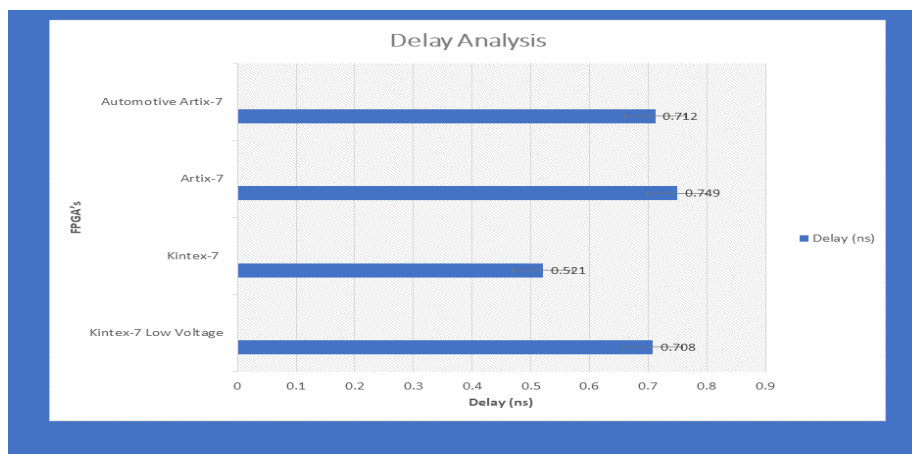


Fig 6: Delay analysis of traffic light control system

V. CONCLUSION

The proposed method assures a better solution for reducing accidents on highways and expressways at junctions on Country Road and Highway Road. Are meeting.

The performance of the proposed method was evaluated on various FPGAs, and we found the following:

- a. The proposed method can be implemented with high speed and performance using the Kintex-7 FPGA.
- b. The proposed method can be implemented with low power consumption using a Kintex-7 low-voltage FPGA.

The proposed method can be easily adopted for any other dynamic traffic control application.

REFERENCES

1. L. F. P. Oliveira, L. T. Manera and P. D. G. Luz, "Smart Traffic Light Controller System," 2019 Sixth International Conference on Internet of Things: Systems, Management and Security (IOTSMS), Granada, Spain, 2019, pp. 155-160, doi: 10.1109/IOTSMS48152.2019.8939239. keywords: {Sensors;Internet of Things;Electronic circuits;Wireless sensor networks;Communication system security;Wireless communication;Microcontrollers;Smart traffic light;smart city;smart mobility}
2. David Beymer, Philip McLachlan, Benn Coifman, and Jitendra Malik, —A real-time computer vision system for measuring traffic parameters, \ IEEE Conf. on Computer Vision and Pattern Recognition, (1997).
3. B. Coifman, D. Beymer, P. McLauchlan, and J. Malik, "A real-time computer vision system for vehicle tracking and traffic surveillance," *Transportation Research Part C*, vol. 6, pp. 271-288, 1998.
4. R. Cucchiara, C. Grana, M. Piccardi, A. Prati, and S. Sirotti, "Improving shadow suppression in moving object detection with HSV color information," in *Proc. IEEE Int. Conf. Intell. Transport. Syst.*, Aug. 2001, pp. 334-339.