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Simulation and FPGA based Implementation of PI and Fuzzy Controllers for Cascaded Asymmetric Multilevel Inverter

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Abstract: *The main objective of this work is to improve the performance of Multilevel Inverter by using the novel LS-PD- PWM and controlling technique instead of the existing approach. The proposed work focus on closed loop controller such as existing PI and Fuzzy Logic Controller for resistive load with Multilevel Inverter. The proposed Asymmetric fifteen level Inverter offers less THD and high frequency than the Asymmetric nine level inverter. Asymmetric multilevel inverter is used to reduce the switching losses and THD. In thiswork is the generation and implementation of Pulse WidthModulation (PWM) techniques using Field Programmable Gate Array (FPGA) for Multilevel Inverter. PWM can be generated via Microprocessors, Microcontroller, FPGA and DSP Processors. Higher density Programmable Logic Devices (PLD) such as FPGAs can be used to amalgamate large amounts of logic into a single Integrated. Pulse width modulation (PWM) is generally used in power converter control. To generate LS-PD- PWM by using FPGA, this occupies less memory capacity and accurate than conventional one. An efficient PWM generation technique is performed using FPGA for lower frequency applications. Simulation and synthesis is done by ModelSim6.3c and Xilinx10.1. Further, theImplementation is carried out by FPGA Spartan3 Xc3s50.*

Key Word: *PWM, FPGA, PLD (Programmable LogicDevices), LS-PD-PWM*

I.INTRODUCTION

In recent years, the field of power converters has seen a considerable growth especially in the field of multilevel inverters. Additionally, these advances in semiconductor industrial technology have greatly enabled the processing capacity of voltage and current and the switching speed of the power semiconductor devices to practice the converter forming many applications. While industries face many difficulties in the variable voltage fixed voltage transforms. Therefore, a conversion process DC to DC is obtained from conventional methods[1-11], such as divider potentiometer voltage set a voltage lower than output power, in this case, itresults in power losses.

The proposed circuit is capable of producing 15 level outputvoltage using asymmetric voltage source configuration (binary progression). Also, the comparison table shows that the proposed circuit uses minimum number of components when compared to other conventional circuits. To minimize the Total harmonic distortion, several different techniques such as PWM, LS PWM, LS-PD PWM modulation techniques were adopted for proposed MLI. Results demonstrate that the proposed circuit exhibits better THD by using Multicarrier Level shifting Phase Disposition Pulse Width Modulation technique (MC-LS-PD-PWM). This modulation technique moderately reduced the THD. Further, the research work is extended to compare the performanceof the proposed circuit using PI and Fuzzy Logic Controller (FLC). From the simulation results, it is seen that the output of the FLC has minimum THD when compared to the PI controller. Hence, it is concluded that the FLC is more reliable than the PI controller based 15 level inverter fed Induction motor system. Also in this work, the experimental prototype for Three Phase 15 level Multicell Multilevel Inverter was developed using Spartan 3E FPGA board. Further, the LS-PD PWM method was coded forSpartan 3E board using VHDL programming to drive powerswitches (MOSFET's) of Three Phase 15 level Multicell Multilevel Inverter. Also, the output voltage levels of the Three Phase 15 level Multicell Multilevel Inverter were acquired and stored using digital signal oscillator. The obtained results for Three Phase Multicell MultilevelInverter were presented in this chapter. Further, the simulation results have been validated with results obtained from developed experimental prototype.

II.15 LEVEL CASCADED MULTI CELL INVERTER

In the proposed 15 level inverter we have three cells connected in cascaded fashion. Here we use asymmetric dc voltages whose voltage levels are given as V for cell 1, 2V for cell 2, 4V for cell 3 etc. Each cell consist of two switches and one isolated DC voltage source.

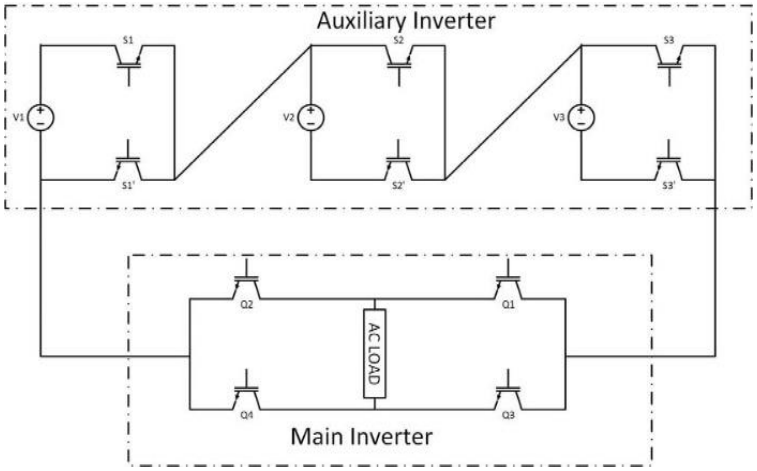
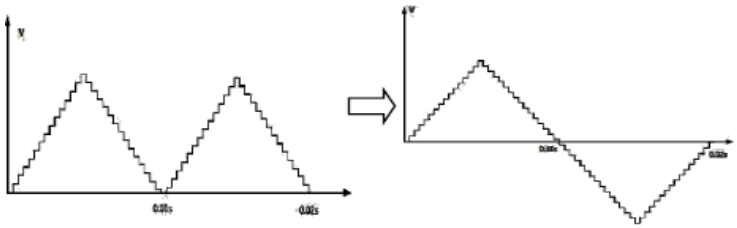


Fig. 2.1 Structure of Proposed Cascaded H-Bridge multi cell 15 level inverter

The output voltages of each cell are added in order to produce multilevel output at the inverters. Their peak to peak voltage available is the addition of all the voltagesources. In our case the peak to peak voltage is 7V. Here, we used voltage of about 40V. So we produce the output voltage of about 280V.

The proposed fifteen -level cascaded multi cell converter, requires three cells which are connected in series as shownin the Figure 3.6. The switching pattern to produce 15 voltage levels is shown in the Figure 3.7.



Output of Auxiliary inverter Output of Main inverter

Fig.2.2 Sample outputs of the proposed inverter

Table I

Switching Table for 15 Level Asymmetrical Cascaded Multi cell Converter

Output voltage levels	Main Switches		Auxiliary Switches					
	Q1 & Q4	Q2 & Q3	S_1	S_2	S_3	S_1'	S_2'	S_3'
7V	1	0	1	1	1	0	0	0
6V	1	0	1	1	0	0	0	1
5V	1	0	1	0	1	0	1	0
4V	1	0	1	0	0	0	1	1
3V	1	0	0	1	1	1	0	0
2V	1	0	0	1	0	1	0	1
1V	1	0	0	0	1	1	1	0
0	0	0	0	0	0	0	0	0
-1V	0	1	1	1	0	0	0	1
-2V	0	1	1	0	1	0	1	0
-3V	0	1	1	0	0	0	1	1
-4V	0	1	0	1	1	1	0	0
-5V	0	1	0	1	0	1	0	1
-6V	0	1	0	0	1	1	1	0
-7V	0	1	0	0	0	1	1	1

A. Modulation techniques and control strategy

The persistence of the modulation technique is to have a smooth transition between the conductive and the nonconductive state. The smooth transition also includes thereduction of the intermediate time (or not). Various modulation techniques have established to reduce harmonics and minimize conduction losses depending on the switching frequency.

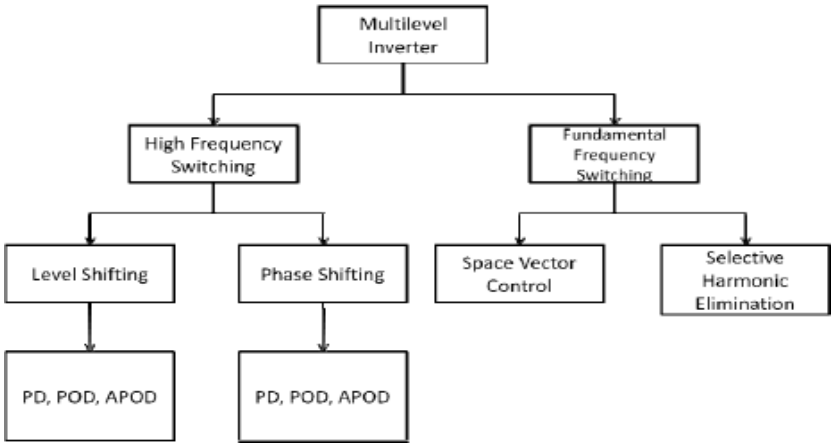


Fig.2.3 Modulation Types using switching frequency

B. Multicarrier Pulse Width Modulation

In particular for multi-level inverter PWM multi-carriers itis easy to create on and off signals to the switches and the output waveform appears next sinus.

There are off two types.

1. Phase Shifting PWM
2. Level shifting PWM

In Phase Shifted topology all the carriers are phase shiftedwith respect to each other. The phase shifting occurs in bothpositive and negative regions of the reference waveforms.The carriers must have same frequency and amplitude. In Level Shifting topology, all the carriers have differentbiasing levels with same peak to peak measures and same frequency. The phase of the carrier plays a major role forfurther classification of LS-PWM

a. Level shifted PWM Method

The LSPWM is further classified into three types dependingupon the phase of the multicarrier.

- Phase arrangement (PD), all the carriers are arranged in-phase with each other.
- Anti-phase arrangement (POD), all the carrier waveforms above the biasing level are in-phase with each other were as the carriers below thebiasing level contains the phase difference of 180 degrees with respect to each other .
- Alternate Phase Disposition (APOD), each carrier waveform is in phase with the adjacent carrier by 180 degrees.

b. Phase Disposition (PD)

In this work the step of applying on the carrier base the PWM system of the arranging is used. As a rule, the reference and the carrier waveforms are compared to produce the circuitry signals of the proposed inverter.

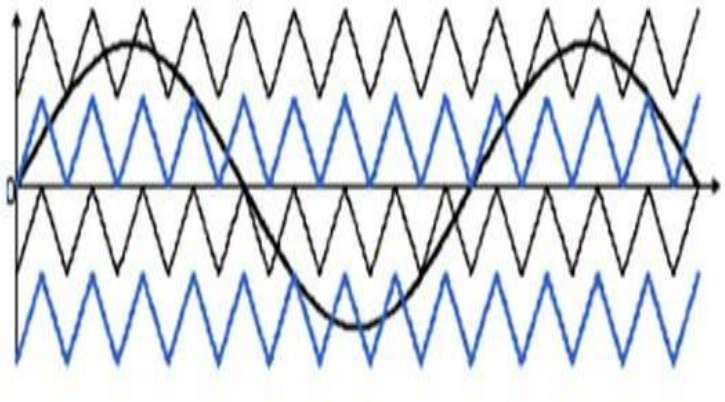


Fig.2.4 Phase Disposition (LS-PD-PWM)

Similarly, the inverters with N levels, requires the (N-1) triangular signals as carriers. Positive switches S1 and S4use the over-zero bias to generate output voltages Vs / 2 andVs and the negative switches S2 and S3 uses the subcarriers below the zero division to generate the output voltages, -Vs /2 and - vs.

C. Design of Conventional Controllers

The PI controller is one of the most reasonable key for alarge portion of the mechanical applications. It is theessential controller which utilizes the input component todeliver the controller impact. It figures the mistake between the real esteem and the reference esteem and that blunder ishandled through relative and vital pick up to deliver itsoutput. It is prominent as a result of its basic structure andcan be effortlessly executed. The control activity law of a PIcontroller is characterized by the accompanying condition. The PI controller output equation is

$$u(t) = K_p e(t) + K_i \int_0^t e(t)dt$$

Where
e (t) is the computed error
Kp represents the gain value of the proportional controller
Ki represents the gain value of the integral controller.

The proportional gain factor represents the present value of the error. On the off chance that the error is little and negative then the controller output will likewise be little andnegative. The vital pick up manages the past estimations of the blunder. In the event that the present value of the controller result is not strong enough in order to optimizethe system output then the fundamental error will gather for some particular period, also the integral activity of the controller takes place to produce the optimized system output.

Table II.

Effects of Proportional and Integral Gain

Parameter	Rise Time	Overshoot	Settling time	Steady-state Error	Stability
K_p	Decrease	Increase	Small Change	Decrease	Degrade
K_i	Decrease	Increase	Increase	Eliminate	Degrade

D. Design of Fuzzy logic Controllers

A Fuzzy Logic Controller (FLC) purely depends upon the information from its sources and by processing the given information depends upon the set of rules specified by the trainer the essential outputs are produced, and also outlining each of its four fundamental parts: Fuzzification, lead –base, derivation component and defuzzification.Fundamentally Fuzzy Logic is a controller in view of scientific framework which utilizes the simple signs to breakdown the qualities as far as computerized factors as 1 and 0 rely on the rationale of the fuzzy guidelines. The fuzzytenets 49 depend on the mistake between the genuine and the reference esteem. The rationale relies on upon the error signal.
To implement fuzzy logic technique to a real application requires the Following three steps:

1. **Fuzzification** – change over established information or fresh information into fuzzy information which are represented universally as Membership Functions (MFs)
2. **Process** – consolidate enrollment capacities and views to regulate the fuzzy output
3. **Defuzzification** – utilize diverse techniques in order to ascertain each related output and build a set of values depending upon the information. (Fuzzy table) The Variables error and the change of error are chosen as the information factors to produce the duty cycle of the inverter.The output is used to produce the reference signal of the LS-PD-PWM. Triangular enrollment capacities are chosen for all these procedure. Fuzzy affiliated memory for theproposed framework is referred in the table

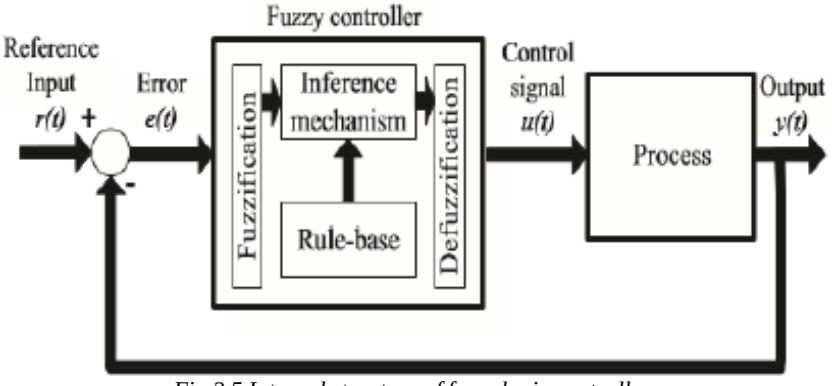


Fig.2.5 Internal structure of fuzzy logic controller

Table III.

Fuzzy Rule Base

ce / e	NB	NM	NS	ZE	PS	PM	PB
NB	NB	NB	NB	NB	NM	NS	ZE
NM	NB	NB	NB	NM	NS	ZE	PS
NS	NB	NB	NM	NS	ZE	PS	PM
ZE	NB	NM	NS	ZE	PS	PM	PB
PS	NM	NS	ZE	PS	PM	PB	PB
PM	NS	ZE	PS	PM	PB	PB	PB
PB	ZE	PS	PM	PB	PB	PB	PB

III.MODULE SIMULATION RESULTS OF SINGLE PHASEMULTICELL MULTILEVEL INVERTER

A. Single phase Multi cell Multilevel Inverter

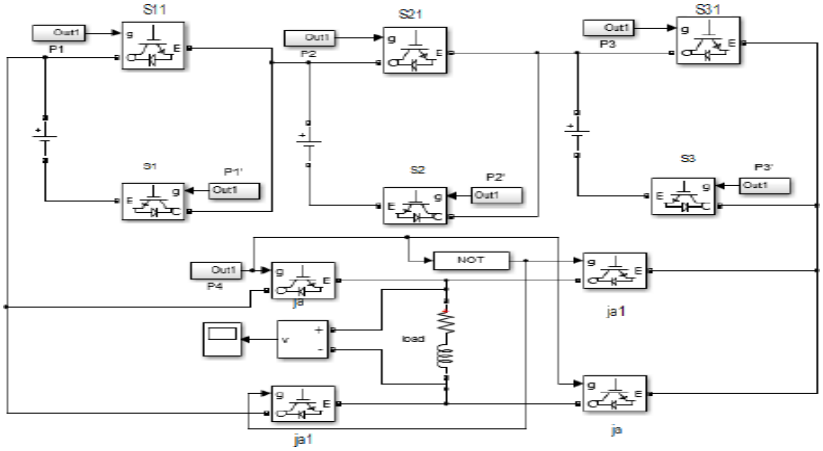


Fig. 3.1 Simulink diagram of Single Phase Multi cell Multilevel Inverter

B. Control strategy of 15 level multi cell multilevel inverterusing LS-PD PWM method

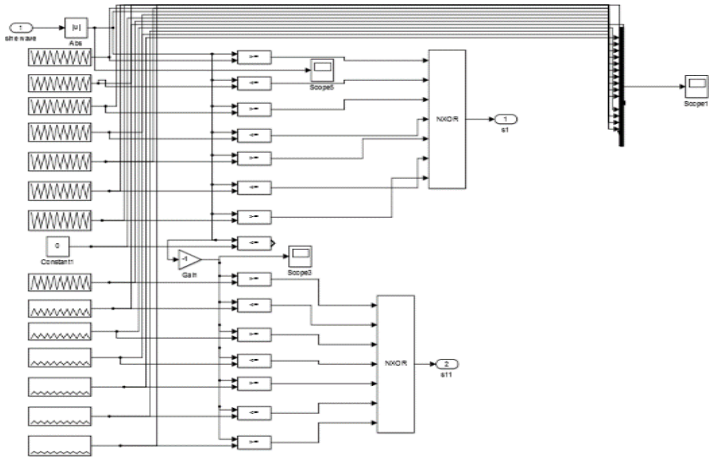


Fig.3.2 Control Strategy using LS-PD-PWM method

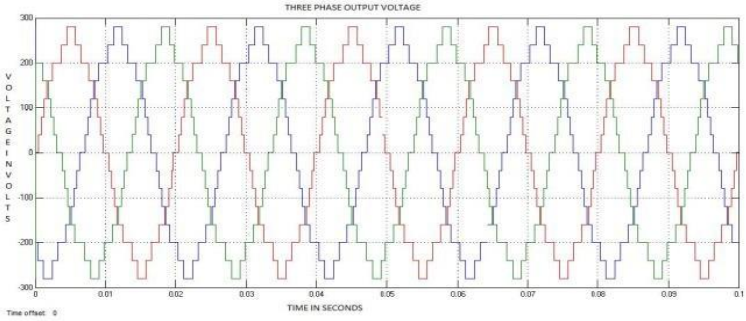


Fig.3.3 Single Phase 15 level Output Voltage using LS-PD-PWM method

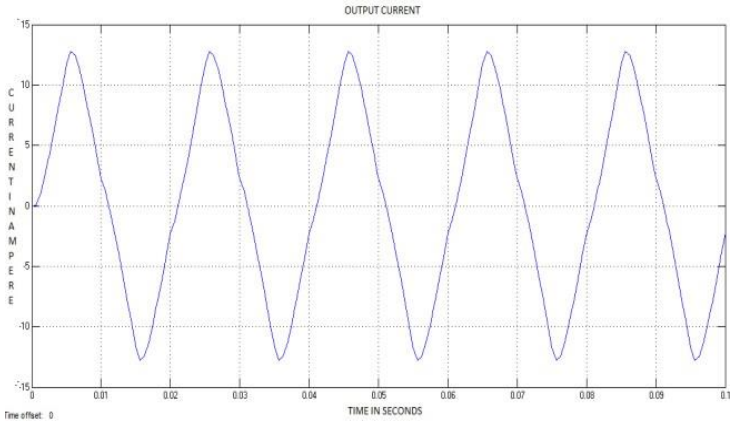


Fig.3.4 Single phase 15 level Output Current using LS-PD-PWM method

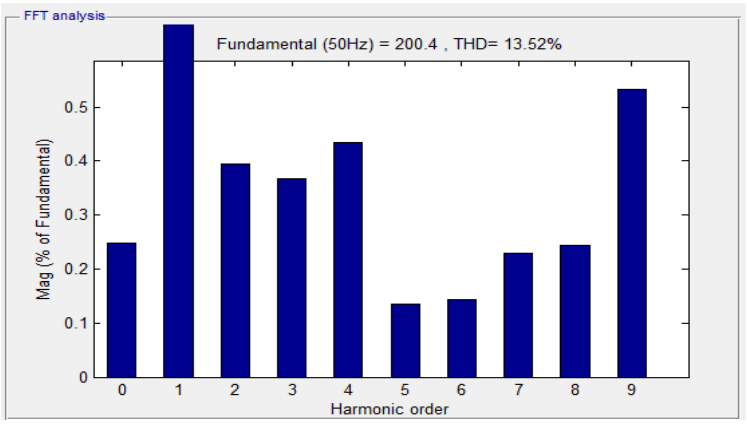


Fig.3.5 THD of Single Phase 15 level Output Voltage using LS-PD-PWMMethod

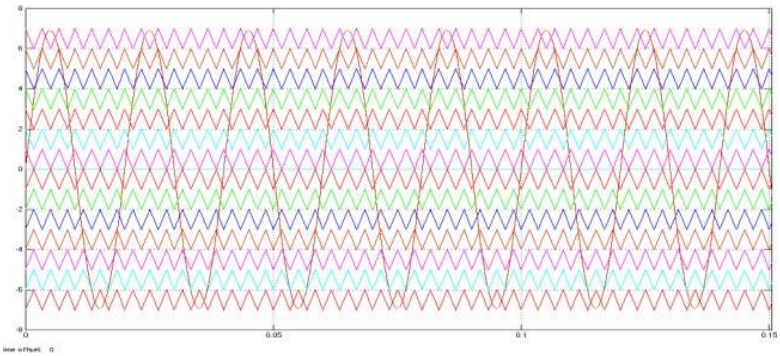


Fig.3.6 Carrier arrangement using LS-PD-PWM method

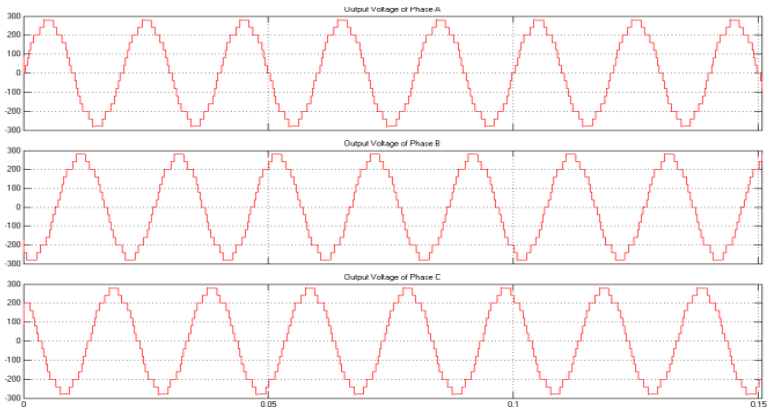


Fig.3.7 Three Phase 15 level Output Voltage using LS-PD-PWM method

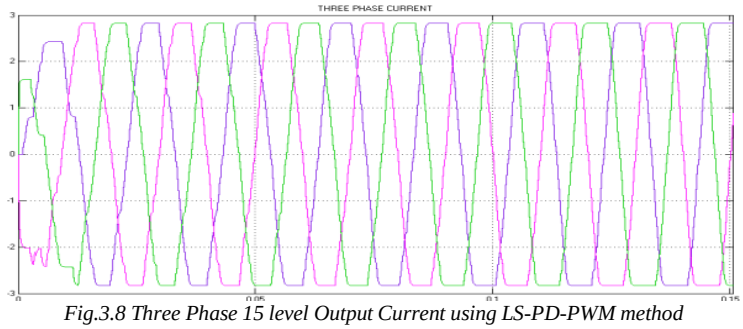


Fig.3.8 Three Phase 15 level Output Current using LS-PD-PWM method

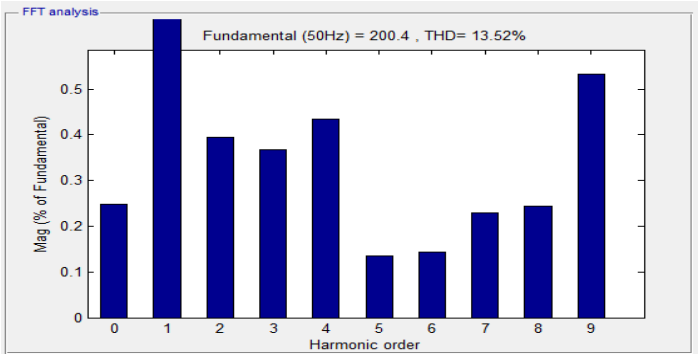


Fig.3.9 THD of Three Phase 15 level Output Voltage using LS-PD-PWMMethod

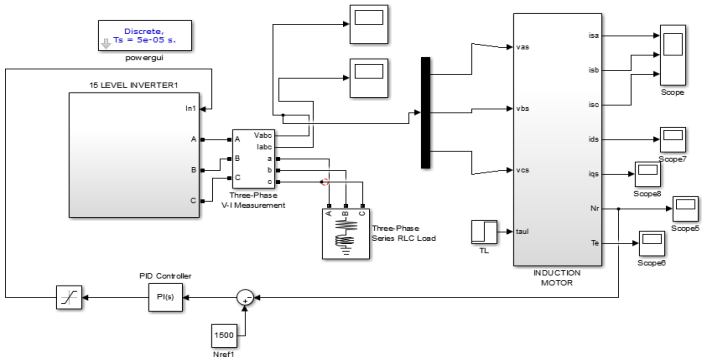


Fig.3.10 Simulink diagram of Three Phase 15 Level Multi cell MultilevelInverter using PI Controller with LS-PD-PWM method

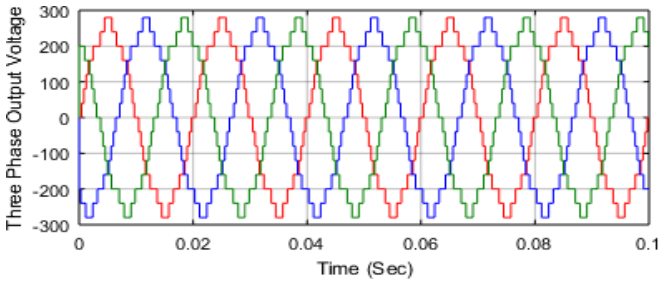


Fig3.11 Output Voltage of Three Phase 15 Level Multi cell MultilevelInverter using PI Controller with LS-PD-PWM method

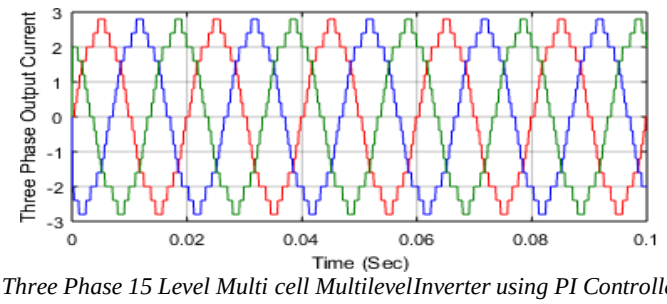


Fig.3.12 Output Current of Three Phase 15 Level Multi cell MultilevelInverter using PI Controller with LS-PD-PWM method

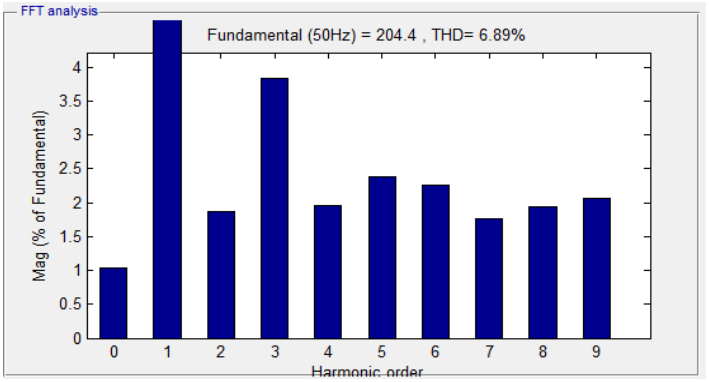


Fig.3.13 THD of Three Phase 15 level Output Voltage using PI controller with LS-PD-PWM method

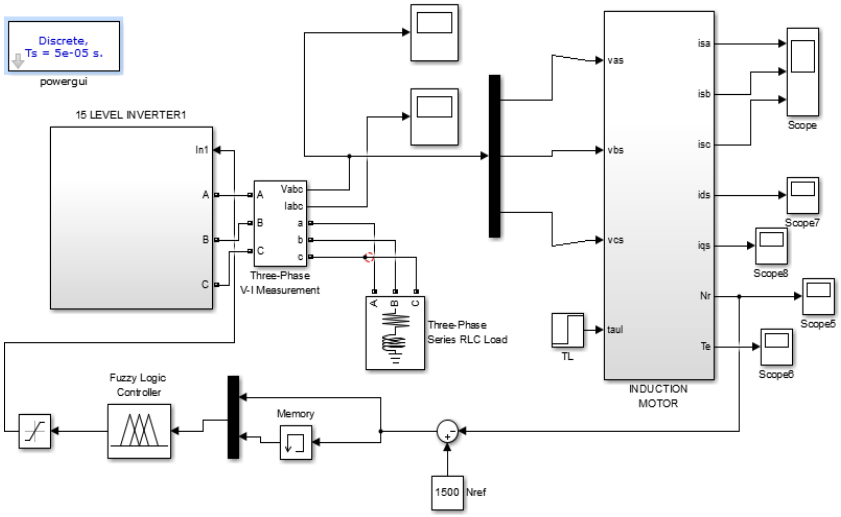


Fig.3.14 Simulink diagram of Three Phase 15 Level Multicell Multilevel Inverter using Fuzzy Controller with LS-PD-PWM method

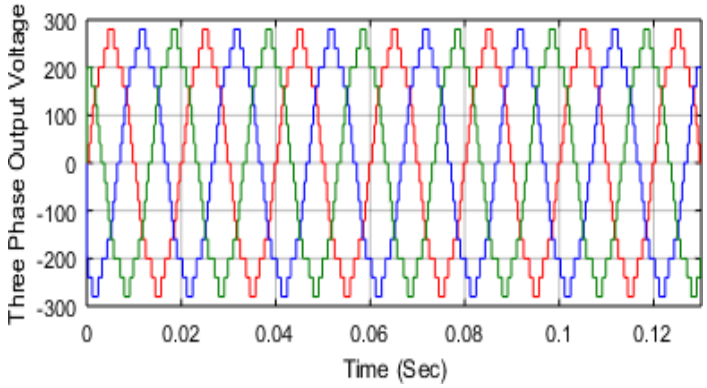


Fig3.15 Output Voltage of Three Phase 15 Level Multicell Multilevel Inverter using Fuzzy Controller with LS-PD-PWM method

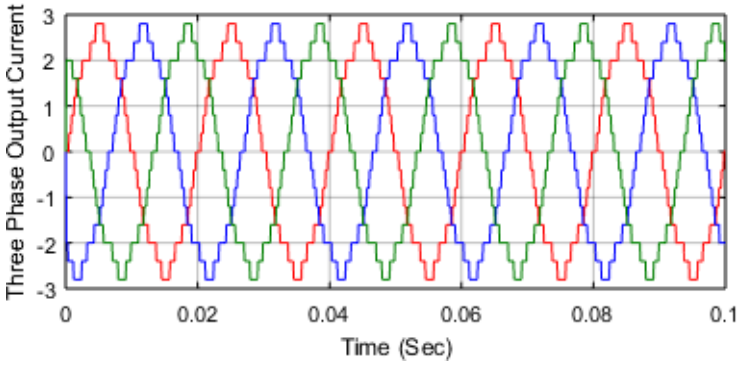


Fig.3.16 Output Current of Three Phase 15 Level Multicell Multilevel Inverter using Fuzzy Controller with LS-PD-PWM method

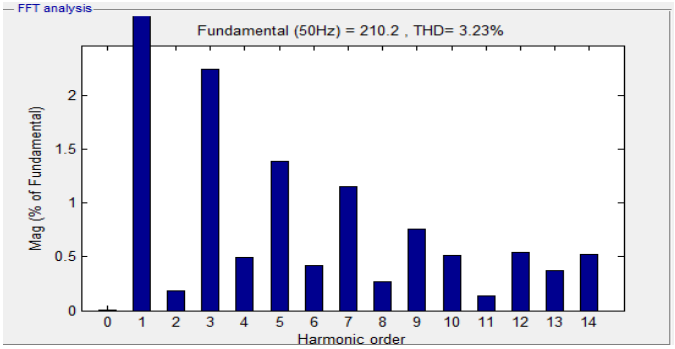


Fig.3.17 THD of Three Phase 15 level Output Voltage using Fuzzycontroller with LS-PD-PWM method

C. Comparison of THD with different controllers

The Asymmetrical 15 level cascaded H bridge inverter usingPWM technique got the total harmonic distortion value is 19.28% and given to the proposed LS PD PWM pulse instead of PWM pulse, the total harmonic distortion value reduced to 13.52%.It is concluded that the LS PD PWM pulse is suitable for reducing the THD value in multilevel inverter. The research work extended to controller section,an Asymmetrical 15 level cascaded H bridge inverter using LS-PD PWM pulse with closed loop PI controller gives6.89% total harmonic distortion value. The same configuration inverter using fuzzy controller drastically reduced harmonics in the value of 3.23% is shown in the Figure 5.27.

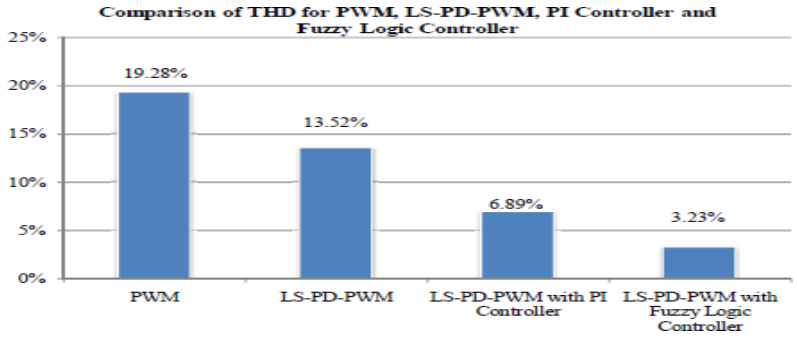


Fig.3.18 Comparison of THD with different controllers

IV. FIELD PROGRAMMABLE GATE ARRAY (FPGA)

The greatest and widely recognized FPGA making comprises of a variety of configurable rationale squares (CLBs), Input/output pieces and reconfigurable network of interconnects CLBs are utilized for acknowledgment of primary rationale in FPGA. It regularly comprises of 4-information Lookup Tables (LUT), multiplexors and flip- flops. LUT is utilized for acknowledgment of combinational rationale. It is a 16-bit configurable memory which is able tounderstand every one of the 4-input 23 mix intelligent capacities. The yield of the LUT can be enrolled to acknowledge consecutive capacities.

In present day FPGAs are likewise CLBs with more than 4 inputs incorporated. Multiplexors in CLB canbe additionally utilized for acknowledgment of rationale capacity with more than 4 inputs, they permits join yields of LUTs CLBs are utilized for acknowledgment of primary rationale in FPGA. It normally comprises of 4-information Lookup Tables (LUT), multiplexers and flip-flops.

LUT is utilized for acknowledgment ofcombinational rationale. It is a 16-bit configurable memory which is proficient to understand every one of the 4-input mix intelligent capacities. The yield of the LUT can beenrolled to acknowledge consecutive capacities. In current FPGAs there are additionally CLBs with more than 4 inputs incorporated. Multiplexors in CLB can be likewise utilized for acknowledgment of rationale capacity with more than 4 inputs, they permit stacked to the SRAM before the begin ofthe FPGA work. It builds boot-time and power utilization.

Nonvolatile FPGAs utilize anti fuses or some sortof nonvolatile memory (FLASH, EEPROM). This arrangement gives the upsides of lower power utilization and higher imperviousness to radiation. Close to essential pieces portrayed above, there are likewise some others square incorporated in a large portion of the FPGAs. Delay- Locked Loops are utilized for clock flag era. Theysynchronize check motion in entire FPGA a can be likewise utilized as clock divider or multiplier. In some application isimportant to utilize a considerable measure of memory.

In these cases, there are Block RAMs coordinated in FPGA. Square RAM is normally a double port RAM withfree control signals for each port. Since FPGAs is broadly utilized for DSP applications, there are multipliers, adders with Carry chain engineering, MAC units and so on incorporated in some FPGAs to expand speed of calculation.The principle preferred

standpoint of DSP processor in examination with FPGA is a basic usage. DSP processor canbe program in constructing agent or C dialect. Then againthe calculation execution is as yet constrained by the design of DSP processor and program acknowledgment.

V.EXPERIMENTAL RESULTS

The output results obtained from experimental prototype of Three Phase 15 Level Multi cell Multilevel Inverter using PI and Fuzzy Controllers with LS-PD-PWM method is shown in figure 4.1. Fig.4.2 shows the Experimental Output Voltages Three Phase 15 Level Multi cell Multilevel Inverterusing PI Controller with LS-PD-PWM Method. Fig.4.3 shows the Experimental Output Voltages Three Phase 15 Level Multi cell Multilevel Inverter using Fuzzy Controller with LS-PD-PWM Method. Fig.4.4 shows the SwitchingWaveforms of single leg 15 Level Multi cell Multi levelInverter (a) Switch S1 & S2 (b) Switch S3 & S4 (c) Switch S5 & S6. Fig.4.5 shows the THD of Three Phase 15 level Multi cell Multilevel Inverter using PI Controller with LS- PD-PWM method. Fig.4.6 shows the THD of Three Phase 15 level Multi cell Multilevel Inverter using FUZZY Controller with LS-PD-PWM method. It is seen that the THD values of developed prototype of Three Phase 15 Level Multi cell Multilevel Inverter is highly correlated withobtained simulation results.

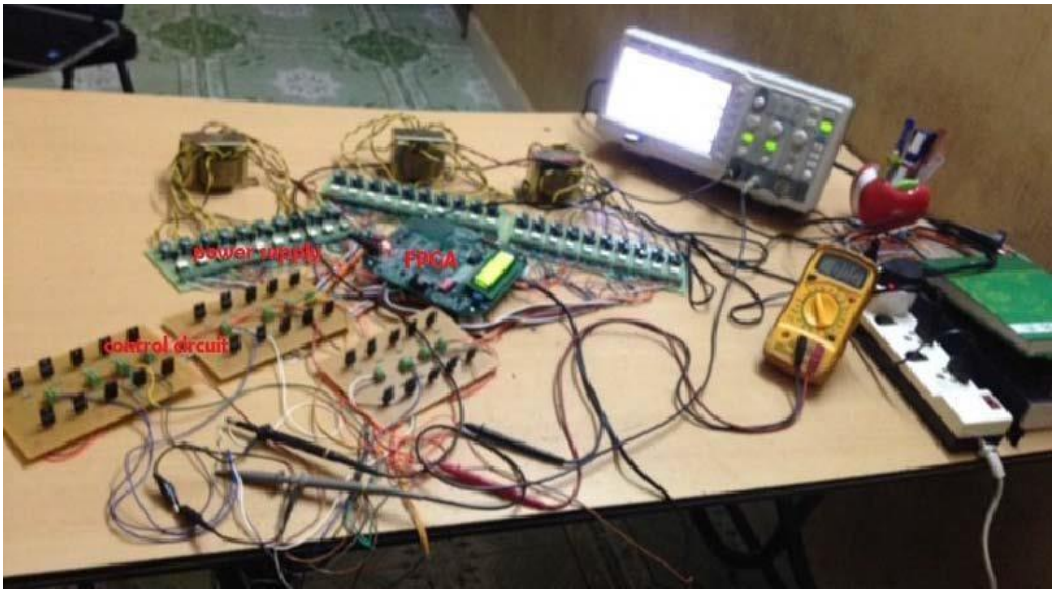


Fig. 4.1 Experimental Setup Three Phase 15 Level Multi cell MultilevelInverter using PI and Fuzzy Controller with LS-PD-PWM Method

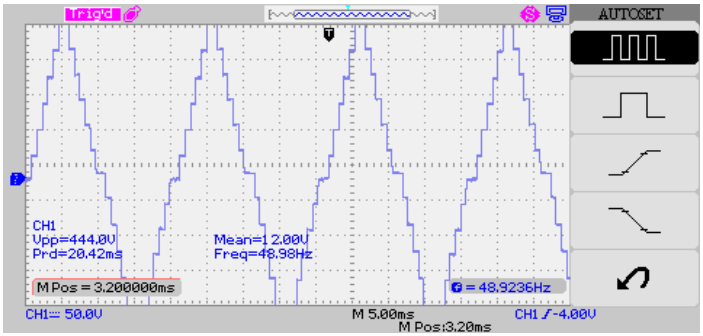


Fig.4.2. Experimental Output Voltages Three Phase 15 Level MulticellMultilevel Inverter using PI Controller with LS-PD-PWM Method

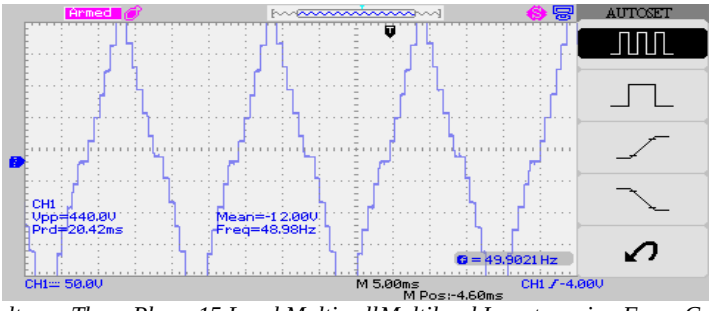
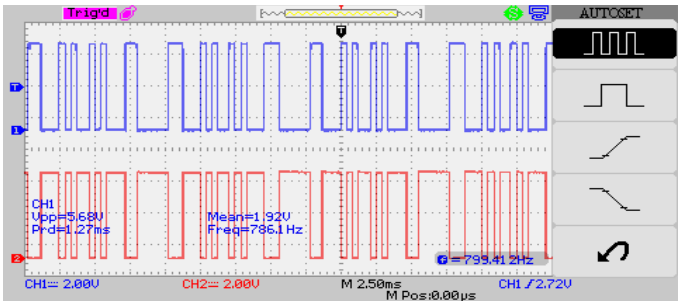
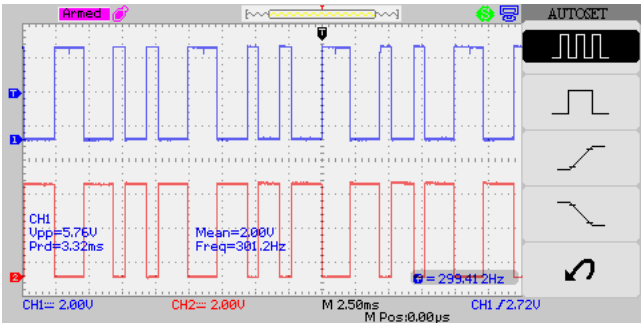


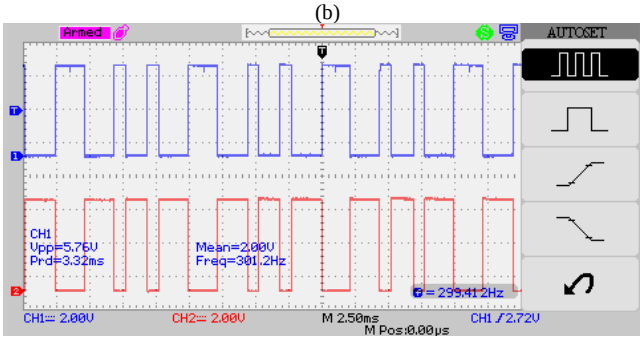
Fig.4.3 Experimental Output Voltages Three Phase 15 Level Multi cellMultilevel Inverter using Fuzzy Controller with LS-PD-PWM Method



(a)



(b)



(c)

Fig. 4.4 Switching Waveforms of single leg 15 Level Multicell Multi levelInverter (a) Switch S1 & S2 (b) Switch S3 & S4 (c) Switch S5 & S6

Fig.4.5 THD of Three Phase 15 level Multi cell Multilevel Inverter usingPI Controller with LS-PD-PWM metho

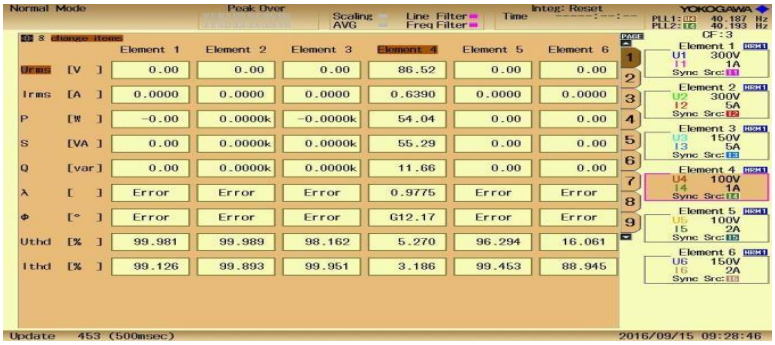


Fig.4.6 THD of Three Phase 15 level Multicell Multilevel Inverter usingFUZZY Controller with LS-PD-PWM method

V. CONCLUSION

The scope of this work is to design a circuit with reducednumber of semiconductor devices. Further, the total of 10 switches for single phase was built. The proposed circuit is capable of producing 15 level output voltage using asymmetric voltage source configuration (binary progression). Also, the comparison table shows that the proposed circuit uses minimum number of components when compared to other conventional circuits. To minimize the total harmonic distortion, several different techniques such as PWM, LS PWM, LS-PD PWM modulation techniques were adopted for proposed MLI. Results demonstrate that the proposed circuit exhibits better THD byusing Multicarrier Level shifting Phase Disposition Pulse Width Modulation technique (MC-LS-PD-PWM). Thismodulation technique moderately reduced the THD. Further,in this work is extended to compare the performance of the proposed circuit using PI and Fuzzy Logic Controller (FLC) by simulation and FPGA based implementation. From the simulation and FPGA based implementation results, it is seen that the output of the FLC has minimum THD when compared to the PI controller. Hence, it is concluded that theFLC is more reliable than the PI controller based 15 level inverter system.

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