**Efficient 1-Bit Full Adder Design Using 9 Transistors for Low Power and Energy-Efficient VLSI Systems**

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| ***Abstract:***In the modern cutting-edge era the VLSI design have been mainly concentrating on the low power ,area efficient and high overall performance gadgets , so the great manner to meet the all the constraints we need to lessen the transistor count number , in this work we've designed the 9 transistor CMOS full adder with a purpose to consume the less power and occupy the much less place in the chip, the adders are the essential circuits inside the mathematics circuits the overall performance of the ALU is rely on the adders , right here the comparison of adder is curious about the previous present fashions and in particular compared with the 10 transistor primarily based CMOS full adder to the 9 transistor full adder , the average power intake thing for the 9 transistor version is improved 94 % compared with the ten transistor version ,here the design is used the 90 nm technology node for the improvement , the paintings is designed and demonstrated with the aid of the use of the microwind DSCH and cadence virtuoso EDA  ***Key Word****:*EDA, ALU, full adder, Transistor remember, power intake, power performance, CMOS common sense, VLSI design, area optimization |

# **I. Introduction**

Fuller adders play a important function in digital circuits. They're just like the fundamental additives that appreciably impact the performance of arithmetic circuits. These circuits, much like multipliers and subtractors, are ordinarily composed of adders inside them. And due to the fact they're a critical thing of mathematics common sense units (ALUs), their overall performance without delay affects how those gadgets characteristic, you recognize? Presently, the primary recognition in designing very large scale integration (VLSI) systems is to beautify power efficiency and reduce strength intake. That's why we're really targeted on improving full adder architectures. Our have a look at tested a 1-bit full adder with 9 transistors and discovered that it consumes strength extra efficaciously compared to older fashions including the 28T, 14T, and 10T ones. This revised design not best reduces the dimensions of the circuit, but it additionally prevents overheating through employing fewer transistors. Essentially, we examined numerous transistor-primarily based full adders and decided which one conserves the most energy and power in the long run.

**II. Literature Survey**

Dr., Md., Masood, Ahmad., D., Anitha. (2022). In this paper The paper provides CMOS full adders with 10, 13, and 15 transistors, reducing the traditional 28-transistor layout through over 50% the use of Cadence equipment for leakage energy analysis.

Zarin, Tabassum., Meem, Shahrin., Aniqa, Ibnat., Tawfiq, Amin. (2018). In this paper The paper compares CMOS full adders with distinct common sense patterns. The 14-transistor full adder has the bottom transistor depend most of the analyzed designs.

**III. existing architectures**

Within the realm of virtual electronics, distinctive architectures have been created for the full adder circuit, with each layout counting on a specific range of transistors. The main goal of this examine is to examine a few decided on architectures and determine their overall performance stages, in the end identifying the only that offers the maximum green operation

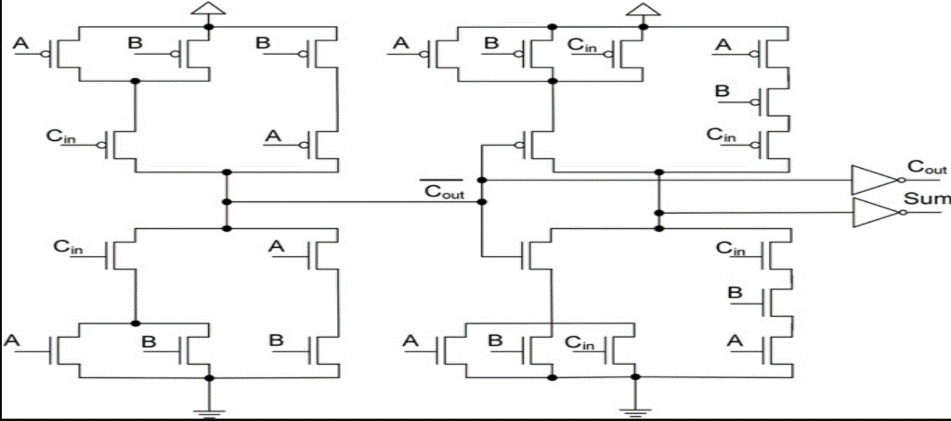


Fig -1 28 transistor full adder schematic.

The instance furnished above depicts a 28-transistor CMOS-primarily based full adder proposing both Nmos and Pmos transistors, with a distribution of 14 Pmos and 14 Nmos transistors. This configuration ends in multiplied energy intake due to the presence of 28 transistors, resulting in higher warmness dissipation and a bigger circuit size, necessitating a further discount inside the wide variety of transistors used for optimization functions.

The under determine indicates the timing diagram of the 28-transistor, 1-bit full-adder circuit.

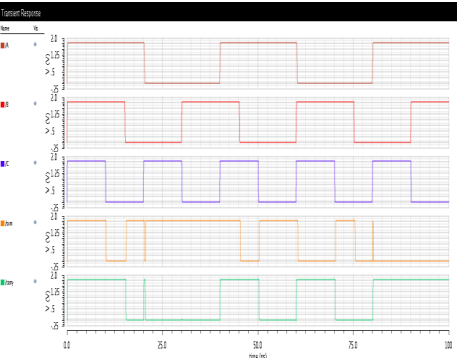


Fig-2 timing diagram of the 28 transistor full adder

The following fig the 14 transistor CMOS full adder.

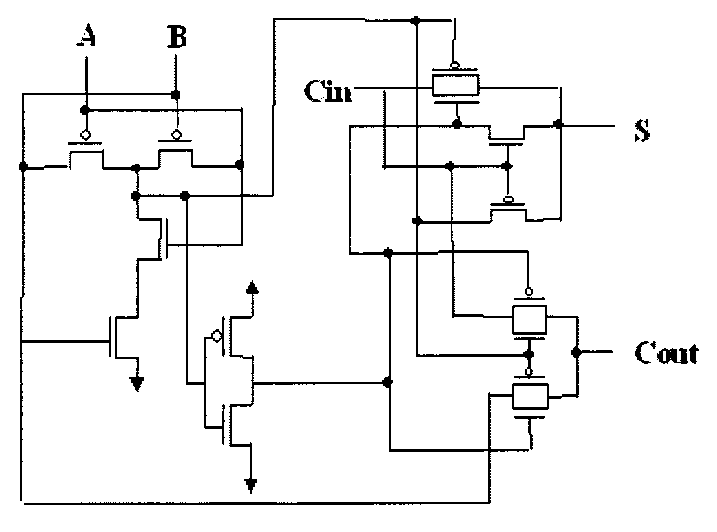


Fig-3 14 transistor full adder

The diagram above illustrates the 14-transistor full adder, constructed by using integrating both MOS transistor logic and transmission gate common sense. The main benefit lies within the decreased power dissipation accomplished by the transmission gate, improving operational performance. But, a large disadvantage arises from the larger region footprint demanded by means of the transmission gate, therefore main to an increase in chip size. Moreover, the complementary operation required by using the transmission gate in addition complicates the layout, in the end resulting in a higher transistor count number.

The beneath fig. Indicates the timing diagram of the 14-transistor, 1-bit full-adder circuit.

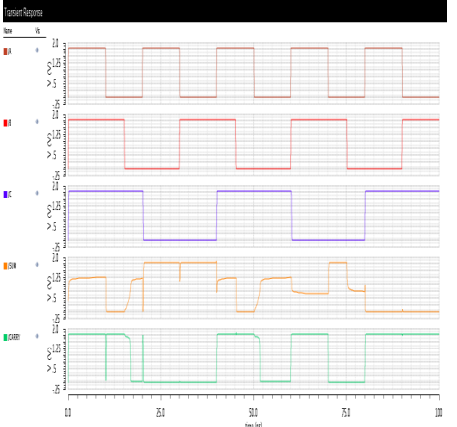


Fig-4 outppputtt waveform of 14 transistor full adder.

The following fig shows the 10 transistor full adder.

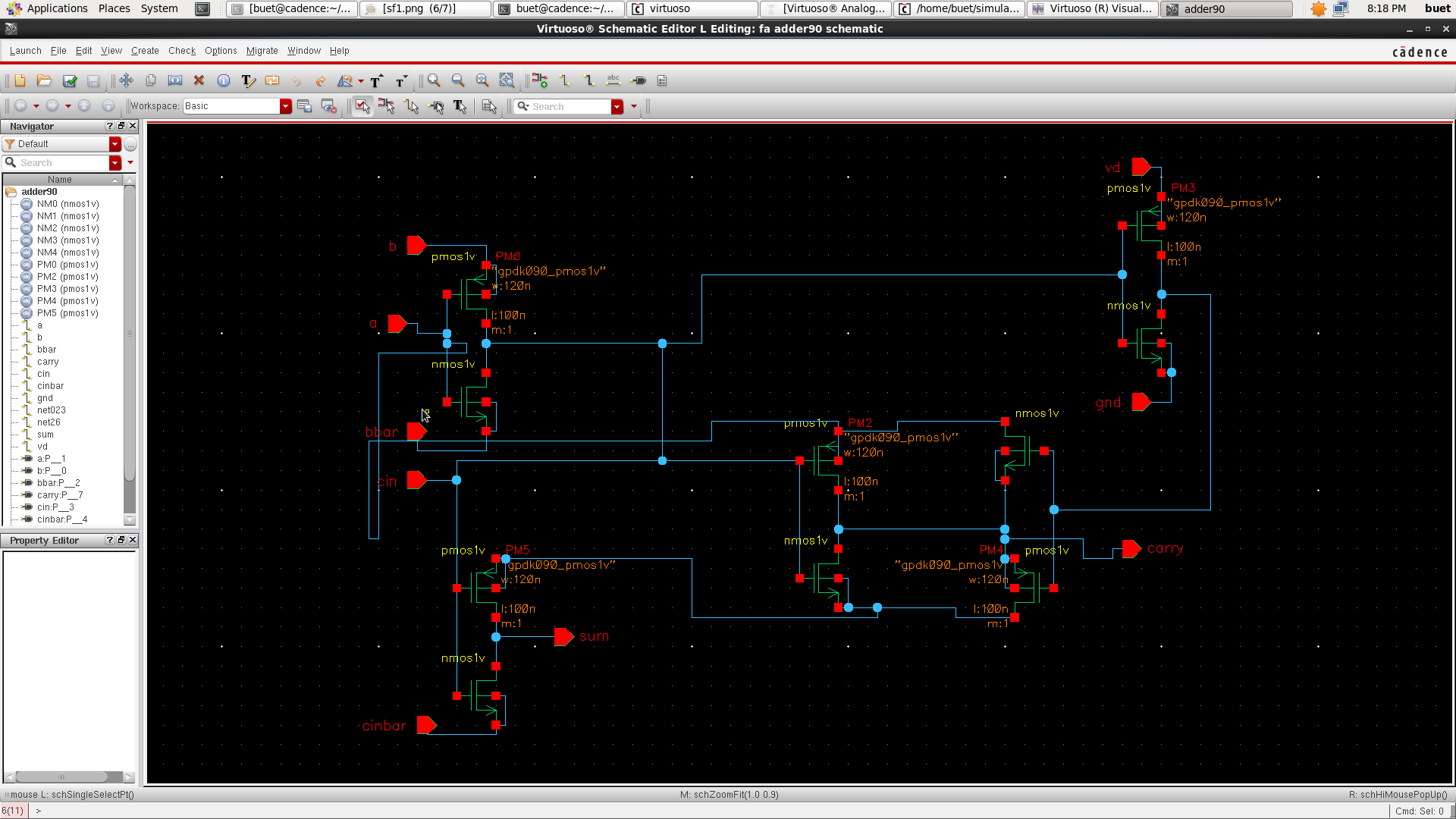


Fig-5 10 transistor based full adder

Within the illustration above, the diagram depicts a ten transistor-primarily based full adder presenting a mixture of five nmos and 5 pmos transistors. This unique design became subjected to rigorous testing making use of EDA gear tailored for the 90nm era node. However, the analysis found out that the modern version is characterized by way of a better power consumption charge. As a VLSI circuit developer, our number one objective is to reduce energy consumption, lessen silicon region occupation, and enhance standard performance metrics. Those standards are deemed important in VLSI layout. Therefore, my research efforts have centered on crafting a 1-bit full adder using a 9-transistor version, which is predicted to exhibit decrease power intake degrees as compared to its predecessors even as also occupying a smaller bodily footprint.

The subsequent discern shows the temporary reaction of the 10-transistor full adder.

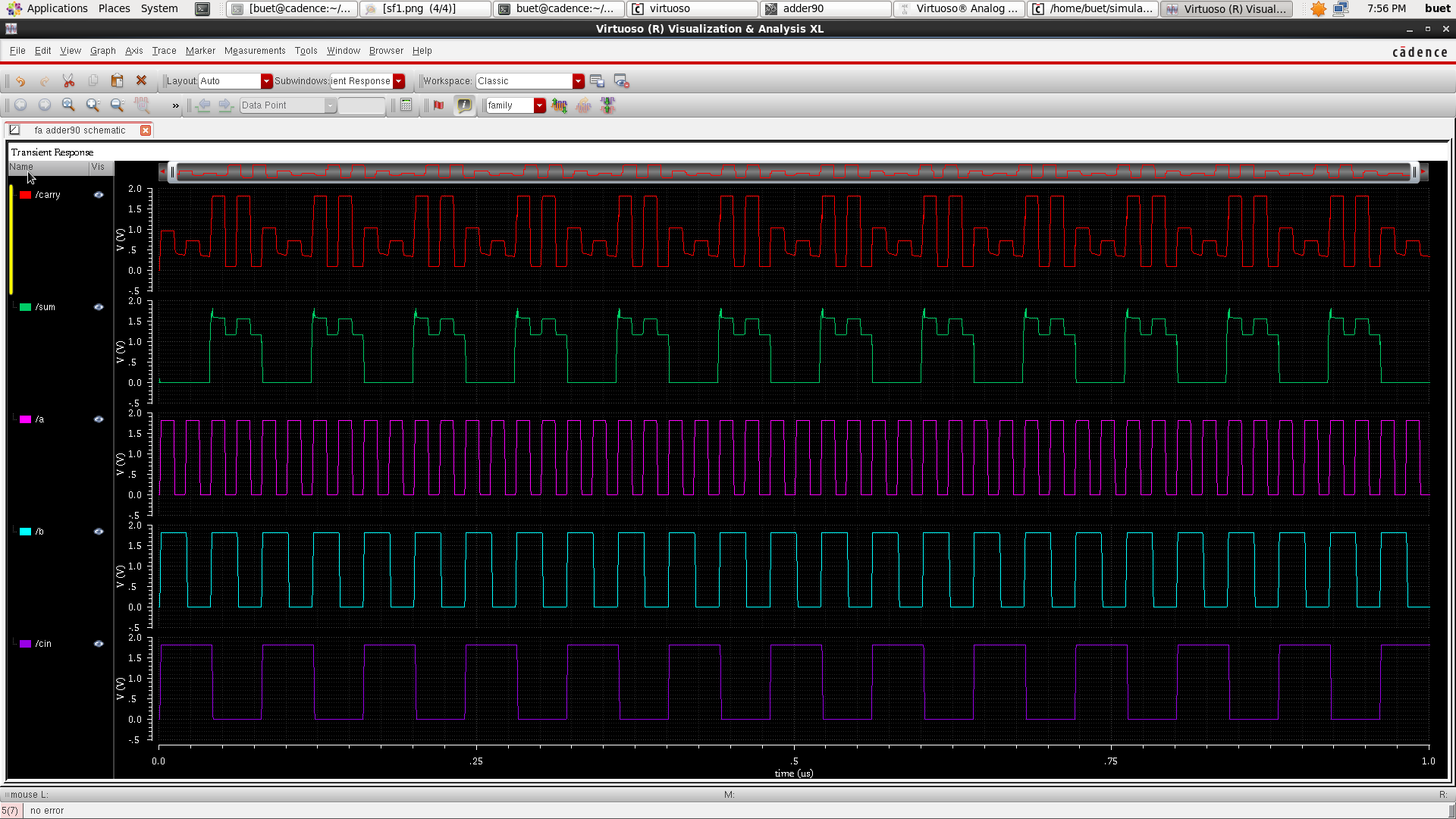


Fig-6 10 Transistor full adder simulation waveform

**IV. proposed architecture**

In my work, the 1 bit full adder is advanced the use of 9 transistors, wherein there are 4 pmos and 5 nmos transistors. Right here, right here we reduced the transitor depend to 9, so this could occupy much less region and consume less power as compared to the above-cited architectures.

The subsequent fig shows the architecture of a 9-transistor-primarily based CMOS full Adder.

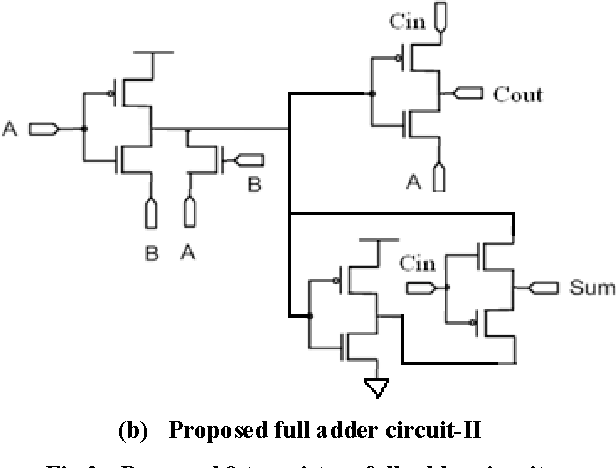


Fig-7 Proposed 9 transistor based CMOS 1 bit full adder

**V. outcome obtained**

The following figures show the consequences received for the proposed architecture and also the assessment effects of the distinctive adders.

The below fig shows the virtual schematic of the proposed structure the usage of the 9 transistor CMOS-primarily based full adder with a 90 nm era node, which has been

demonstrated inside the microwind virtual schematic (DSCH).

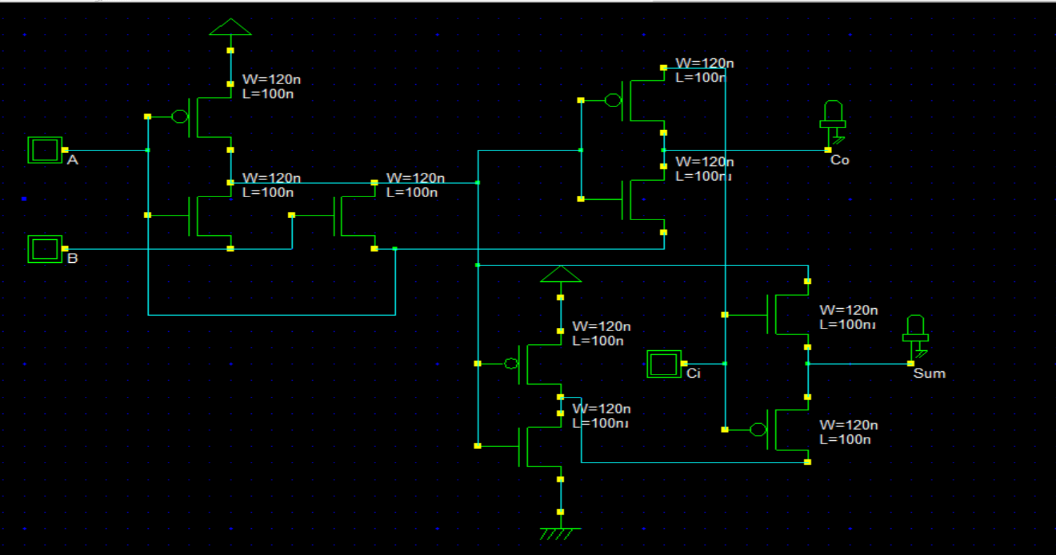


Fig. 8: Digital Schematic of the 9-transistor Full Adder

The subsequent fig shows the timing diagram of the 9-transistor full adder using the microwind EDA tool

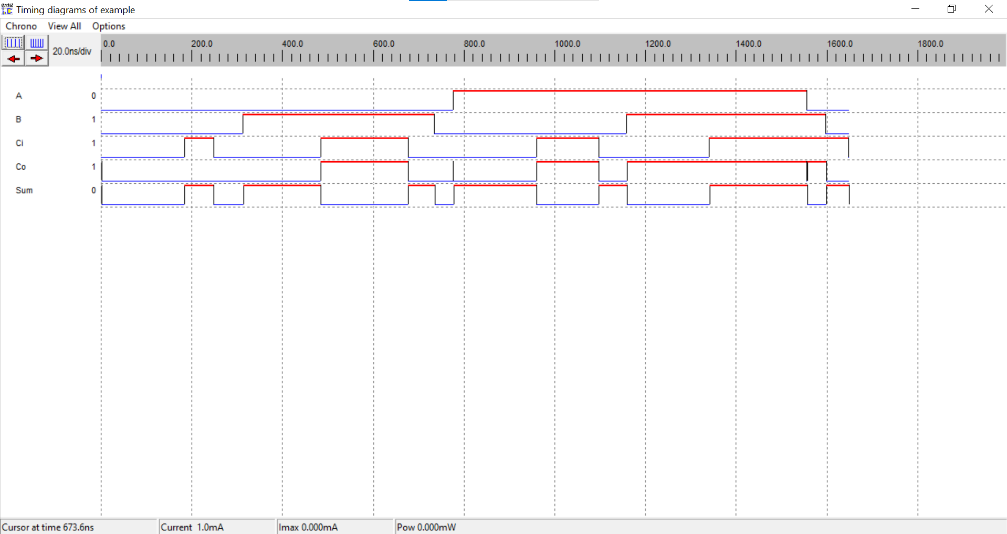


Fig-9 Timing diagram of the 9 transistor full adder.

The subsequent fig shows the energy evaluation of a 90 nm 10 transistor-based CMOS 1 bit full adder the use of the Cadence Virtuoso tool.

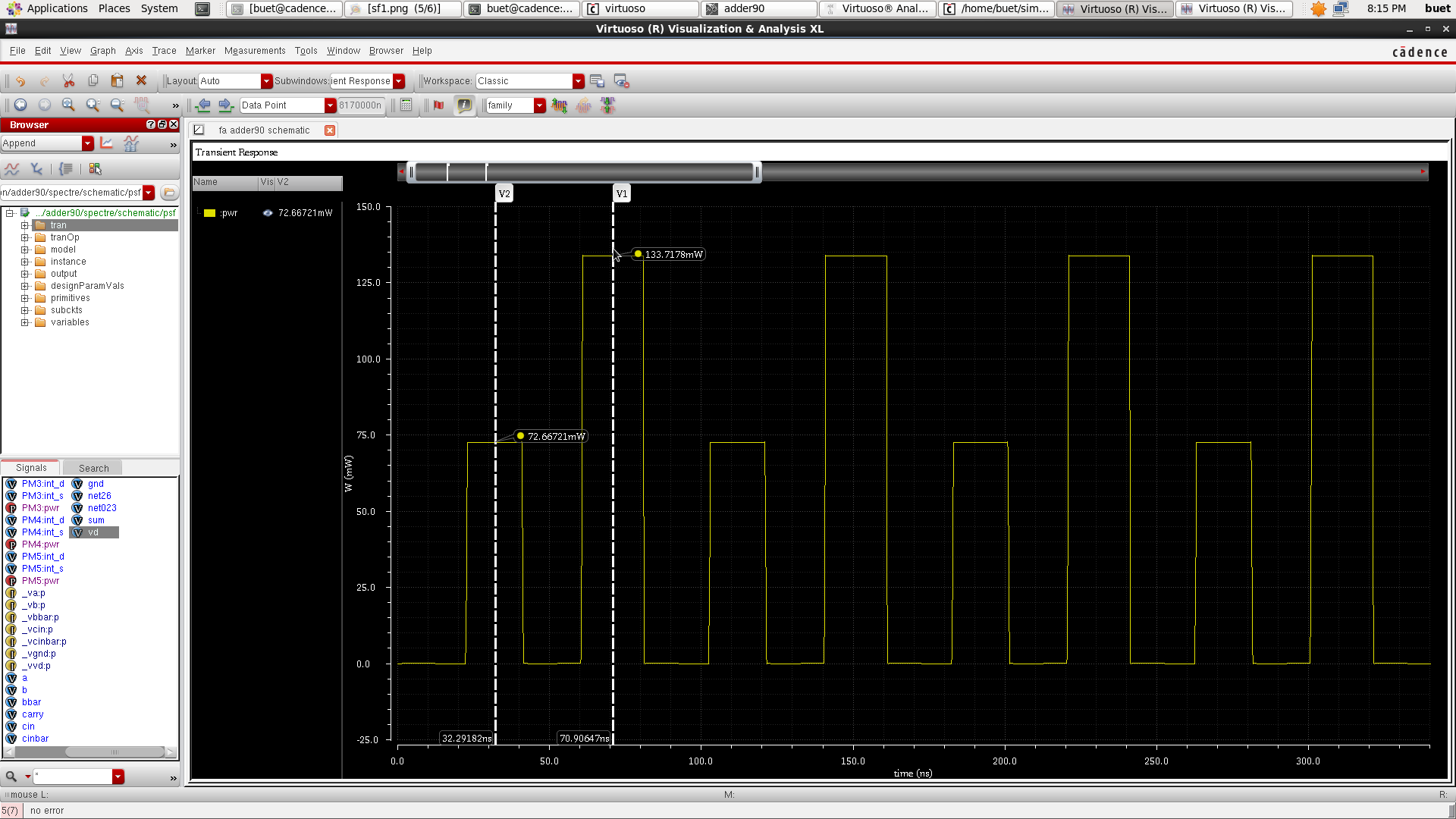
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Fig-10 suggests the total strength analysis of the ten t full adder using a 90 nm tech node.

The subsequent parent shows the average strength consumption of the 10-transistor full adder.

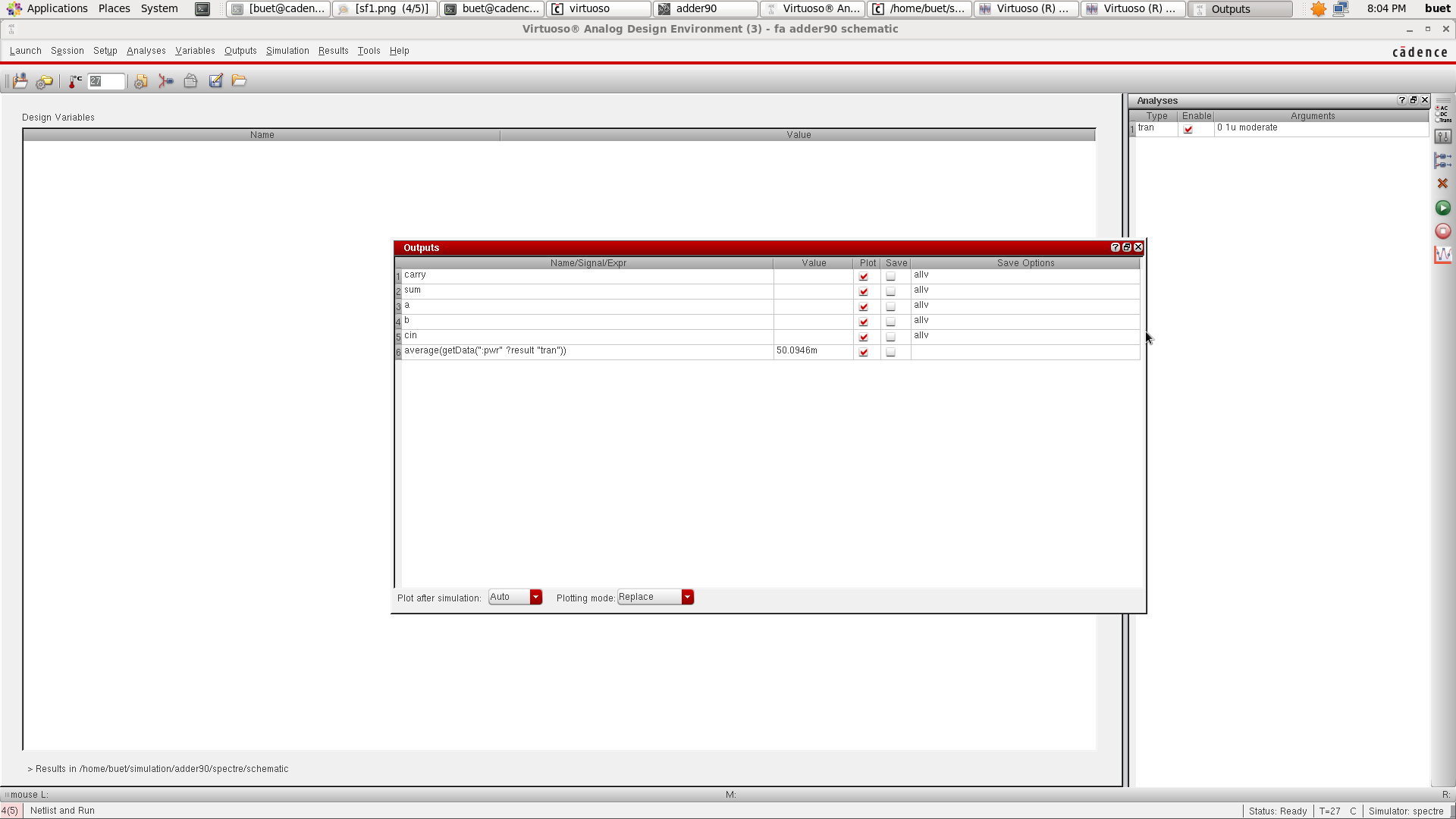
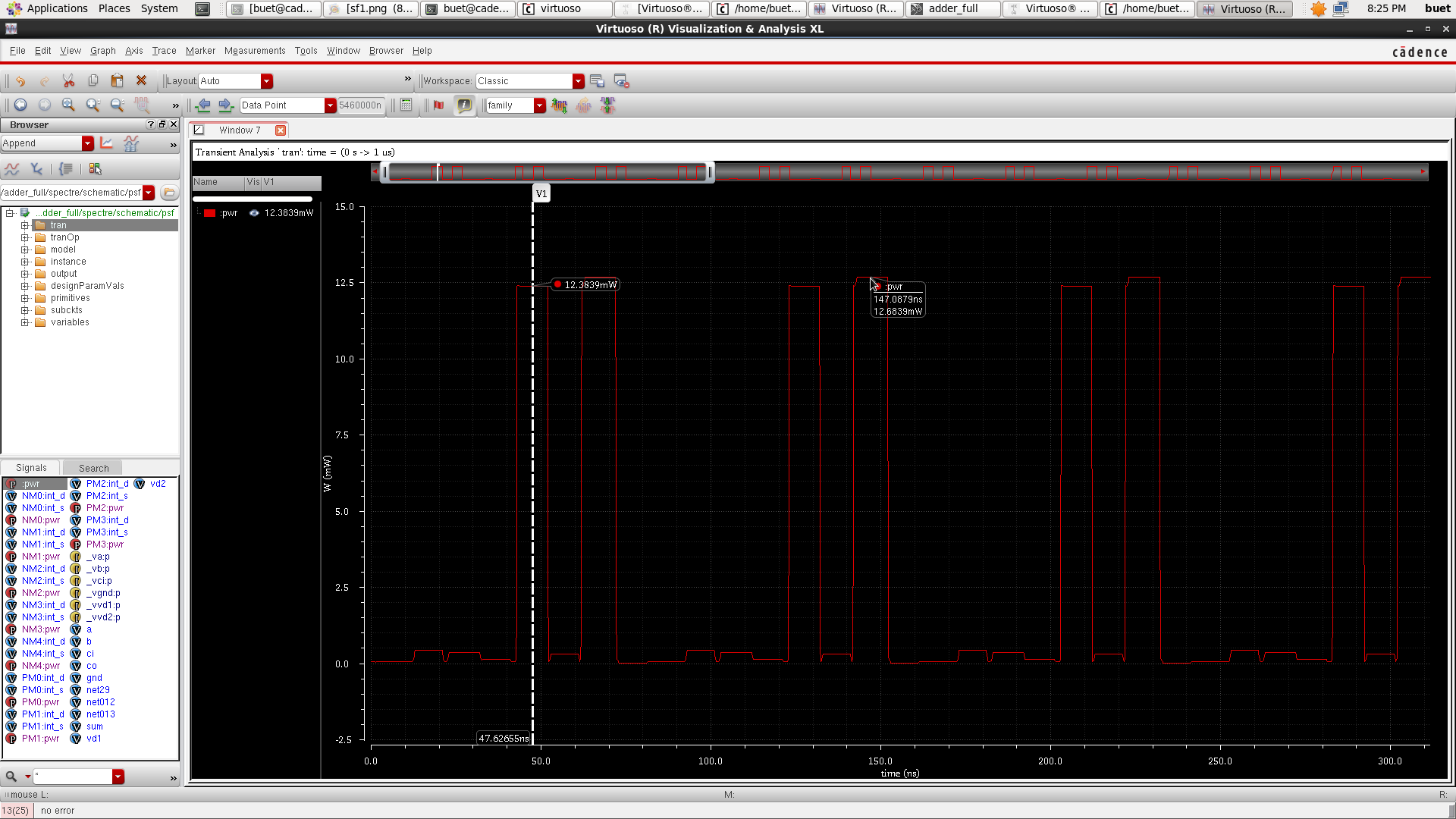
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Fig-11 shows the average power consumption of the 10 transistor full adder on the 90 nm technology node.

The following fig suggests the energy evaluation of the proposed structure, i.e., a 9-transistor full adder on **the 90 nm technology node.**

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**Fig-12: Total power analysis of the 9 T full adder using a 90 nm tech node.**

The subsequent fig suggests the average power intake by the 9-transistor full adder at the 90nm generation node.

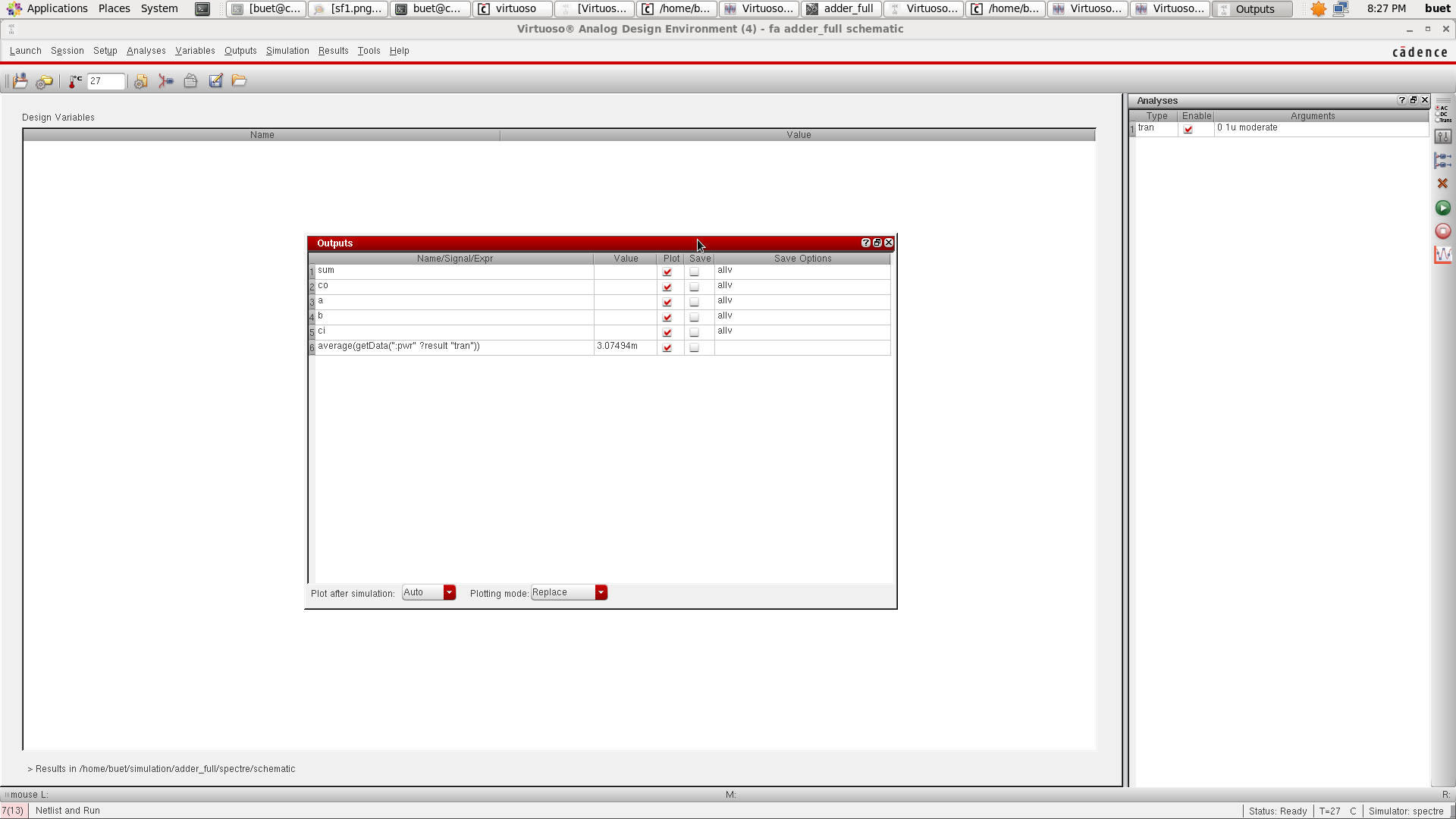
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Fig-13 average power consumption by the 9 transistor full adder using 90 nm technology.

**Comparison of the power of the 90 nm 10 transistor full adder and the 9 transistor full adder.**

Fig-11 comparison of power consumption by both 10 transistor and 9 transistor model.

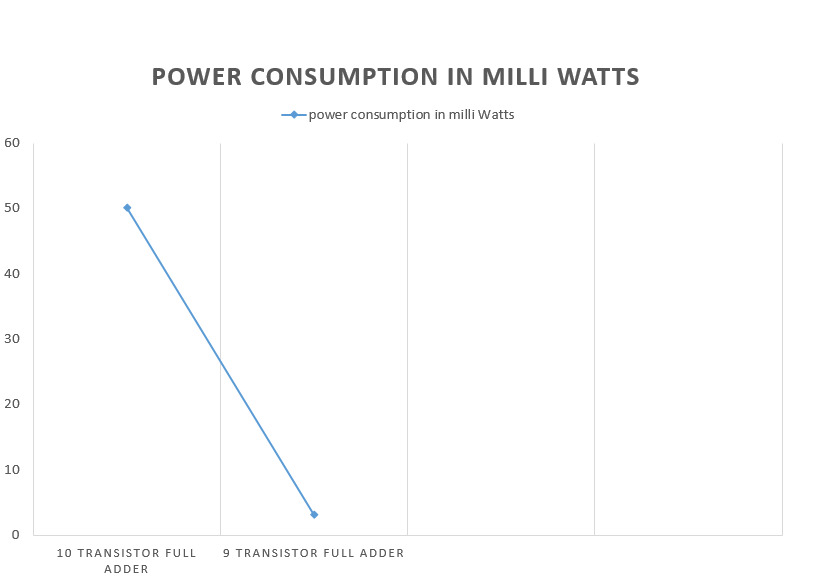
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Fig-11 comparison of power consumption by both 10 transistor and 9 transistor model.

**VI. conclusion**

This paper introduces a power- and power-efficient 1-bit full adder layout that calls for simplest 9 transistors (4 pmos and 5 nmos) in 90nm technology. The advised architectural layout is compared to current designs such as the 28-transistor, 14-transistor, and 10-transistor full adders. The findings imply that the 9-transistor full adder calls for less strength and occupies a smaller physical area compared to the opposite architectures. The digital schematic and timing diagram of the proposed layout are tested using EDA tools. Energy analysis suggests that the 9-transistor full adder consumes much less total and common power in comparison to the 10-transistor design in 90nm technology. The 9-transistor version complements the average energy with the aid of 94% compared to the preceding 10-transistor model.

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