**Comparative Analysis of 7nm and 5nm Semiconductor Technologies**

1Pinnoji Srujana, 2Poloju Mahesh3Pandi Deepika, 4Bhuvan Srinived,5Bandi Keerthana

*1PG Student, Department of ECE, Scient institute of technology, Hyderabad, India Jawaharlal Nehru Technological University Hyderabad*

*2,3,4,5UG Student, Department of ECE, Jawaharlal Nehru Technological University Hyderabad, India.*

***Abstract:***

*This FinFET devices are evolved such that promises a substitute of a bulk of CMOS(complementary metal oxide semiconductor) based device on the nanotechnology. 5nm technology node was very efficient campared to previous nodes. Here MOSFET gate length nothing but size of transistor is 5 nm so it is termed as 5nm technology. This is process is the MOSFET technology node that follows the 7 nm node. In the year of 2020 samsung and TSMC will began production of 5nm process chips. These 5nm process node is a groundbreaking semiconductor manufacturing technology that packs 30 billion transistors into a tiny chip. This results in faster processing speeds, with up to a 15% increase in clock speed, and lower power consumption, with up to a 30% reduction in power usage. Additionally, the technology allows for increased transistor density, with up to 80% more transistors per area. These advancements enable improved performance and efficiency in various applications, including artificial intelligence, high-performance computing, mobile devices, Internet of Things devices, and automotive and industrial applications.*

**Keyword:** *FinFET, 5nm technology, 5nm process, 5nm nanoscaling, MOSFET 5nm process, nanometer technology, nanometer process node, semiconductor nodes.*

**I.Introduction**

The semiconductor industry has long been driven by the insatiable demand for smaller, faster, and more efficient electronics. The advent of 5nm technology represents a major breakthrough in this pursuit, pushing the boundaries of what is possible in semiconductor manufacturing. With transistors measuring just 5 nanometers in size, this cutting-edge process node enables the creation of chips that are not only more powerful and efficient but also more compact and cost-effective. As the successor to 7nm and 10nm technologies, 5nm technology is poised to revolutionize the way we design, build, and interact with electronic devices, from smartphones and laptops to servers, data centers, and artificial intelligence systems. By packing more transistors into a smaller area, 5nm technology unlocks new possibilities for innovation and growth, enabling the development of smarter, more connected, and more sustainable technologies that will shape the future of our increasingly digital world.

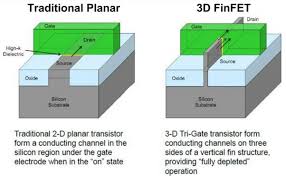
**II. Literature survey**

Srinivasan Natarajan, Mike Agostinelli, Sriram Balakrishnan, An Steegen, and Shriram Shivaram(2014).This paper presents the development of 5nm FinFET technology, featuring a Fin pitch of 24nm, Fin width of 5nm, and gate length of 15nm. The technology demonstrates improved performance, power, and area (PPA) benefits, with a 30% increase in drive current and a 50% reduction in power consumption compared to the previous generation.

Yanzhen Wang, Juntao Liang, and James F. Buckwalter in the Year 2013. This paper presents the design and fabrication of III-V FinFETs for low-power applications. The devices feature a novel InGaAs/InP FinFET structure with a Fin width of 15nm and a gate length of 30nm. The results demonstrate improved subthreshold slope, reduced leakage current, and enhanced drive current compared to traditional silicon FinFETs.

**III. Developing of FinFET**

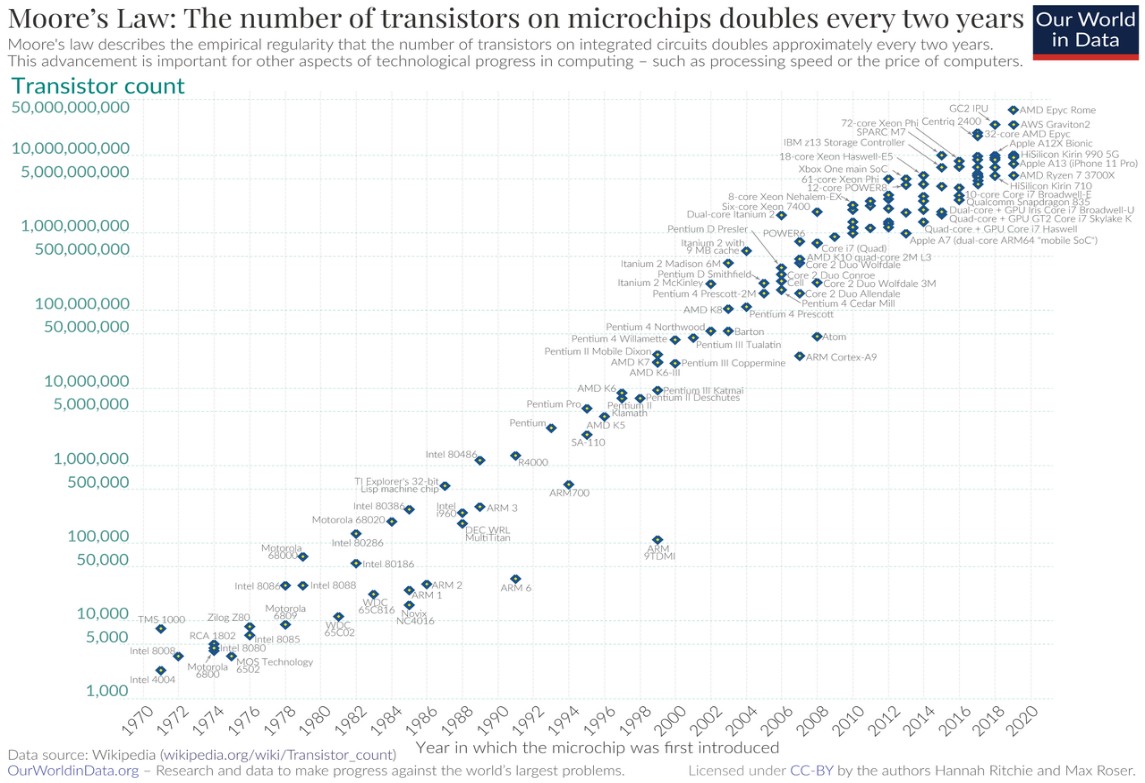
fin field effect transistor(FinFET) it is a type of multi gate MOSFET . In the name fin means channel between source and drain it can have two or more fin in same structure.FinFETs are made from MOSFETs by altering the structure to include a three-dimensional "fin" that protrudes from the silicon substrate. The process begins with a standard planar MOSFET layout, followed by etching narrow, vertical fins into the silicon. These fins act as the transistor channels. A gate structure is then formed to wrap around the fin, providing better control over the channel by influencing it from multiple sides. Finally, source and drain regions are created at the ends of the fins, completing the FinFET. This design enhances performance and power efficiency compared to traditional planar MOSFETs due to improved electrostatic control of the channel.FinFET design further increases the density and the many transistors packed in the same area. [1][2] When compare to traditional planar it is more better in many factors.



**Fig1:** From MOSFET to FINFET

**IV. Moore’s Law**

Goordon Moore, his is the cofounder of the of INTEL corporation he established the term “MOORE’S LAW’in 1965. This law explains that how the number of transistors on intregrated circuits is increasing exponentially, which boosts the computing capability with lower prices. It is the prediction that the number of the transistors on an integrated circuits will doubled for every two years.

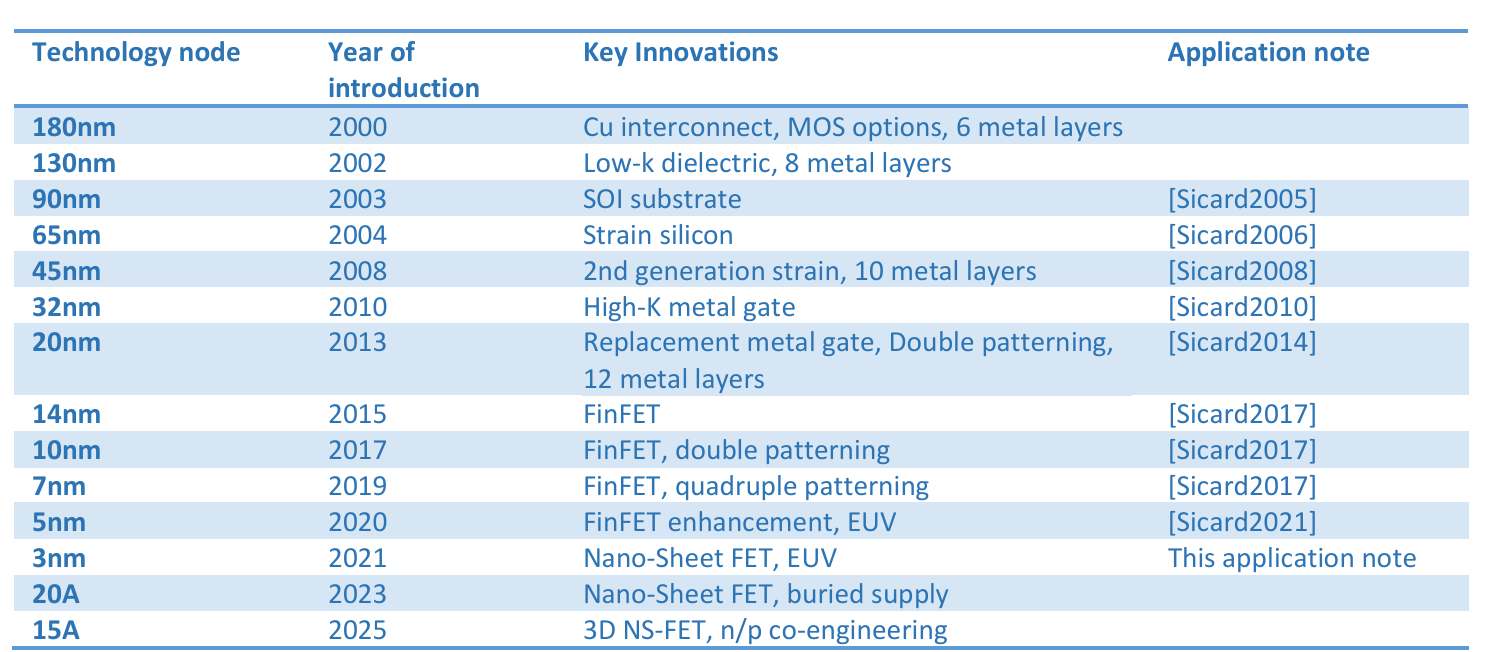


**fig2**: Moore’s law graph

**V. Nanotechnology**

Nanotechnology as the name itself as suggested that it is a path for a technological development that concerns the management of the materials at the nanoscale. The nanometer technology represents a measurement of the transistor nothing but the size of the transistor simply in nanotechnology. Gate length decides the type of the node like 5nm and also other measurements of devices on the microchip or nm technology refers to the measurement of the transistor size.

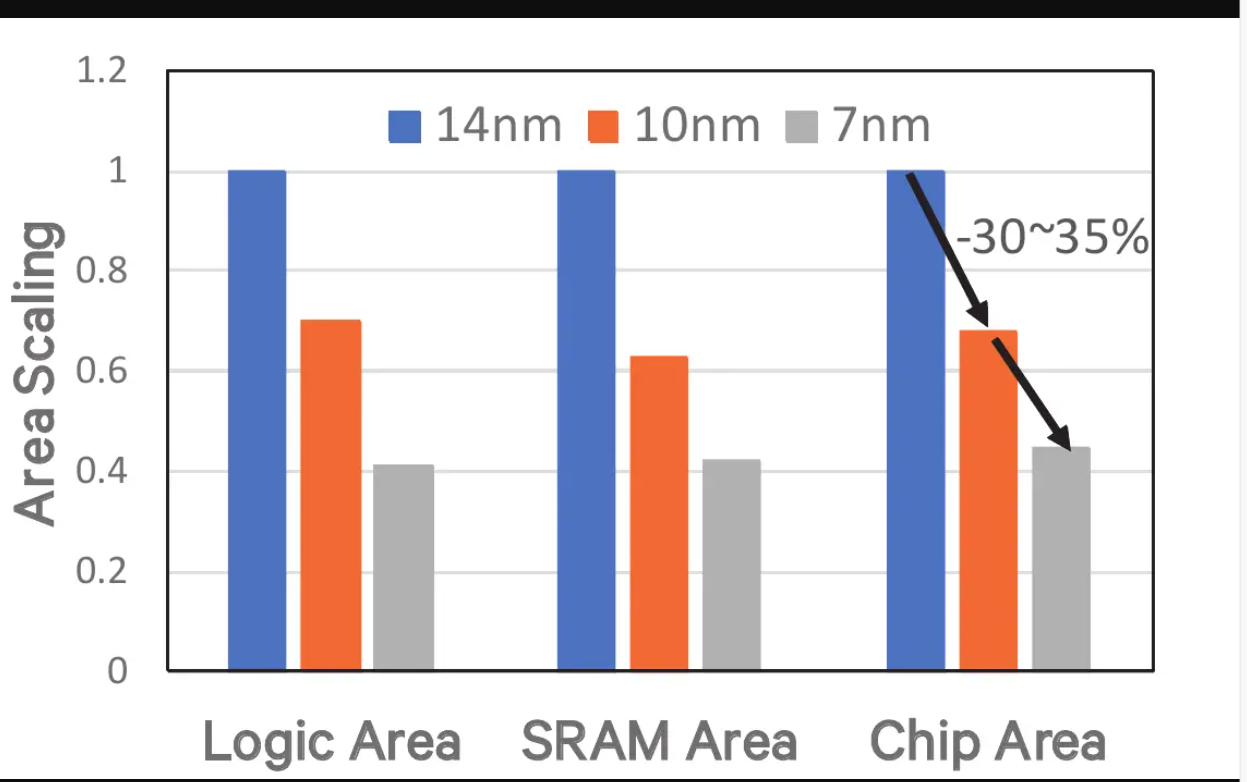
When the dimensions of the MOSFET are scaled down then the both voltage level and gate oxide thickness will be reduced. The dimensions of the MOSFET is directly proportional to the voltage levels and gate oxide thickness. Since the thermal voltage of the electron is constant for a room temperature electronics. The gate oxide has scaled to a thickness of only a few atom layers, where the quantum mechanical tunnneling is rise to sharp the gate leakage currents.



**Table 1:** Technology nodes over past 20years

**VI. 7nm technology**

In these 7nm technology the size on a chip is 7nanometers, it allows to for greater transistor density, improved performance and it consumes less power when compare to before technologies .it is very upgrading technology. It employes the advanced techniques called Extreme ultraviolet (EUV) lithography to achieve the precise patterning required for these small features.

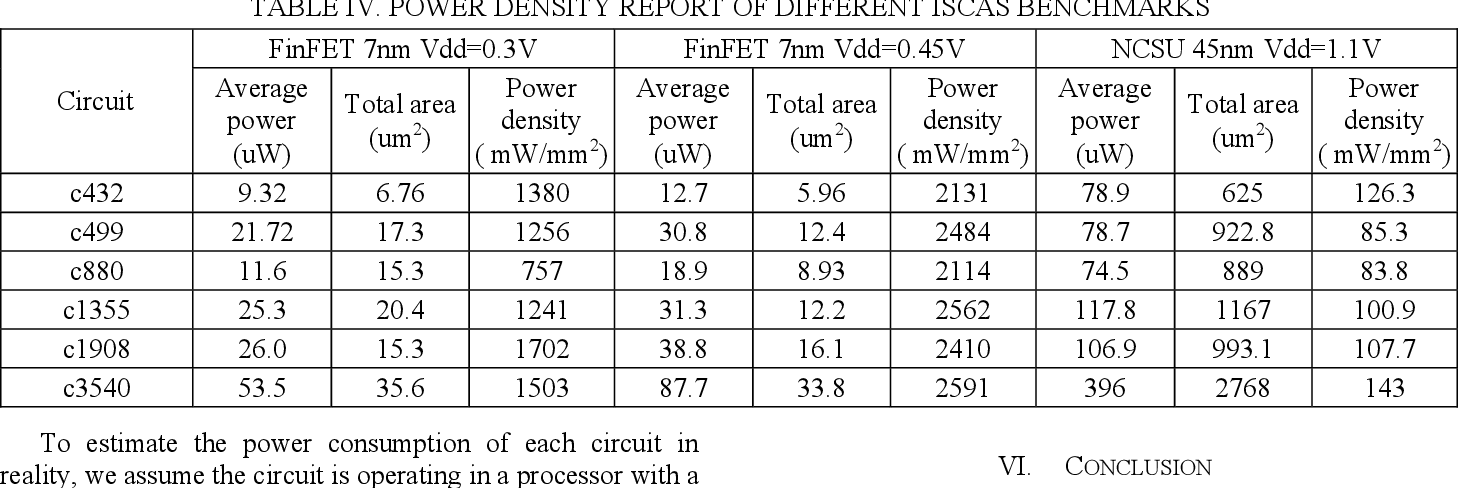


**Fig 3**: comparision between different technologies

To predict the power values in 7nm technology .we have to synthesize the various ISCAS benchmark circuits using the developed FinFET technology.to find the average power consumption in various circuits can be calculated using:

Paverage =Pleakage+α.Pdynamic .D.f

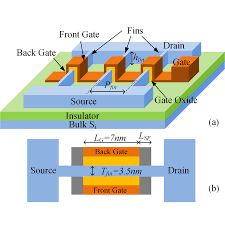
In power report we can find the Pleakage , pdynamic and D where D is the circuit delay and the α value is set to be 0.2 an the power density analysis as shown in the below figure.



**Table 2:** power density analysis for 7nm FinFET

**VII. 5nm TECHNOLGY**

The purpose of these 5nm technology is to decrease transistor size when compare to 7nm technology the parameters like power,area, , and more efficient devices, driving innovation in fields like artificial intelligence, 5G, IoT, and autonomous vehicles. With 5nm technology, devices can have increased storage capacity, display resolution, and camera quality, while also supporting emerging technologies like edge computing and cloud computing.[3][4] Furthermore, it enhances hardware-based security features, protecting against emerging threats. Overall, 5nm technology plays a crucial role in shaping the future of electronics, meeting the growing demand for smaller, faster, and more efficient devices, and enabling new applications and use cases across various industries.



**Fig 4** : structure of FinFETfet

As shown in the figure FinFET it consists very thin silicon body with the thickness of Tfin which is wrapped by the electrodes. The height of the fin is twice of the gate length Lg In these structure each fin essentially the parallel connection of the front gate controlled FET and the back gate controlled FET both width is equal to the fin height hfin.

When the supply voltage is reduced then the dynamic energy consumption also reduced that results in a leakage energy consumption, [5] which is a product of leakage currents and circuit delay increases, because of reduction of the leakage power which is a linear relationship versus vdd due to the circuit delay which is the exponential relationship versus vdd.

In every technology reduced the the power in three specific ways they are

1.smaller dimentions that typically do not travel large distances so less capacitance to charge.

2.nanosheets are pack more efficiently than their FinFETs, so less transistor capacitance and more drive capability of the transistors

3.in 5nm technology could translate the 75℅ power saving than the previous nodes.

4.these transistors are 40℅ faster than the previous FinFETs.

The 5nm technology involves several factors, including:

**1. Transistor density**: Higher transistor density enables more functionality and improved performance.

**2. FinFET and GAA transistors:** 3D transistor structures for better current control and reduced leakage.

**3. EUV lithography:** Enables precise patterning and smaller transistors.

**4. Atomic Layer Deposition (ALD):** Precise material control for thin layers.

**5. Self-Aligned Quadruple Patterning (SAQP):** Enables precise patterning and smaller transistors.

**6. Voltage and frequency scaling:** Reduces power consumption and improves performance.

**7. Leakage reduction:** Minimizes unwanted current and reduces power consumption.

**8. Advanced materials:** New materials with improved electrical properties.

**9. Design optimization:** Optimizes circuit design for performance, power, and area.

**10. Manufacturing process innovations:** Improvements in wafer processing, etching, and deposition.

**12. Thermal management:** Manages heat dissipation to prevent thermal throttling.

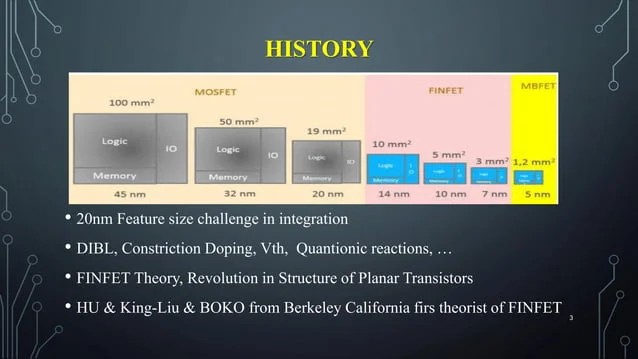
**13. Power management:** Optimizes power consumption and delivery

**15. Electromagnetic compatibility**: Minimizes electromagnetic interference.

These factors contribute to the development of the 5nm technology, enabling improved performance, power efficiency, and functionality in semiconductor devices.

|  |  |  |
| --- | --- | --- |
| Process name | 7nm | 5nm |
| SRAMbit cell size | 0.027 | 0.020 |
| Transistor gate pitch | 48 | 42 |
| Interconnect pitch | 28 | 24 |
| Transistor density | 100miilion transistors per square millimeter | 170-200 transistors per square millimeter |

**Table 2:** comparision analysis of 7nm and 5nm



**Fig 5:** Reduced Nanotechnologies

As shown in the above figure, transistor size has been reduced over the past few years. Now in these generation 5nm technology is widely used and major companies like Apple, Samsung etc uses these 5nm technology

**VIII. Conclusion**

The 5nm technology achieves unprecedented transistor density, revolutionizing semiconductor manufacturing. It enables smaller, faster, and more efficient devices, transforming the electronics landscape. With 5nm, breakthroughs in AI and ML are fueled, and IoT innovation is unlocked. Performance meets efficiency, driving future technological advancements and ushering in a new era of innovation. Transistor density increases by 30%, power consumption is reduced by 20%, and faster switching speeds and improved processing power are achieved. Devices show enhanced performance, increased storage capacity, faster data transfer rates, and improved energy efficiency, with reduced heat generation. Ultimately, 5nm paves the way for 3nm and beyond, shaping the future of technology.

**IX.Future scope**

The 5nm technology is poised for widespread adoption, becoming the new standard for smartphones, laptops, and servers. It will enable more powerful AI and ML processors, leading to breakthroughs in areas like natural language processing and computer vision. The Internet of Things (IoT) will also benefit, with 5nm powering more efficient and compact devices that connect even more aspects of our lives. Next-generation technologies on the horizon include 3nm and 2nm semiconductors, Quantum Computing, Neuromorphic Computing, DNA Computing, and Graphene-based Electronics. Additionally, researchers are exploring Nanotechnology, Artificial General Intelligence (AGI), and Brain-Computer Interfaces (BCIs). These emerging technologies have the potential to revolutionize various fields and transform our lives

**X. References**

[1] . C., Horowitz, M., Schlachter, S., Thompson, S., & Gregory, R. (2010). “Performance and scaling of FinFETs”. IEEE Transactions on Electron Devices, 57(6), 1342-1350. Doi:10.1109/TED.2010.2046725

[2]. Hisamoto, D., Kaga, T., Nakamura, Y., & Shimizu, T. (2000). “FinFET: A self-aligned double-gate MOSFET scalable to 20 nm” "5nm FinFET Technology" by Natarajan et al. (2014) - Presented the development of 5nm FinFET technology.

[3]. "5nm FinFET Technology" by Natarajan (2014) - Presented the development of 5nm FinFET technology.

[4]. "FinFET-Based Low-Power and High-Performance Circuit Design" by Y. Wang et al. (2019)

[5]. "5nm FinFET Standard Cell Library Optimization" by J. Li et al. (2018)