Design of standard cells: Inverter, NAND, NOR

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***Abstract*—This document shows the design of NAND, NOR and NOT gates on 180nm CMOS technology. Static and Dynamic design are considered in development. Then, this gates with its parameter, such as K_p, V_{th},λ, frequency, W and L, are simulated in LTSpice. Finally, a brief conclusion and results are shown.**

***Index Terms*—NAND, NOR, NOT, 180nm CMOS, Static design, Dynamic design.**

I. Introduction

Complementary CMOS gates inherit all the nice properties of the basic CMOS inverter, for that reason, the inverter is truly the nucleus of all digital designs. Once its operation and properties are clearly understood, designing more intricate structures such as NAND gates, adders, multipliers, and microprocessors is greatly simplified. The electrical behavior of these complex circuits can be almost completely derived by extrapolating the results obtained for inverters. The analysis of inverters can be extended to explain the behavior of more complex gates such as NAND, NOR, or XOR, which in turn form the building blocks for modules such as multipliers and processors.[1]

A. The Static CMOS Design

Figure 1 shows the circuit diagram of a static CMOS inverter. Operation of CMOS inverter is described as follow: When V_{in} is high and equal to VDD, the NMOS transistor is on, while the PMOS is off. A direct path exists between V_{out} and the ground node, resulting in a steady-state value of 0V. On the other hand, when the input voltage is low (0V), NMOS and PMOS transistors are off and on, respectively, a path exists between VDD and V_{out} yielding a high output voltage.[1]

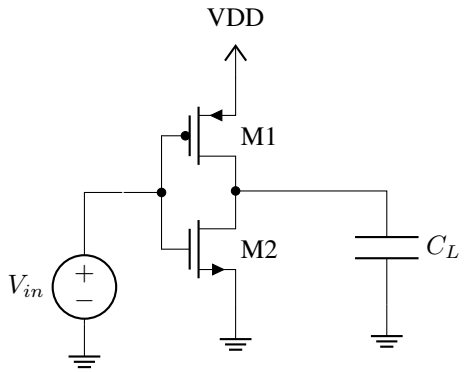

Fig. 1. Inverter in CMOS Technology

Operation regions and the modes of each transistor are plotted in 2. The switching threshold voltage V_t is defined as the point where $V_{in} = V_{out}$. Its value can be obtained graphically from 2 with the line given by $V_{in} = V_{out}$. In this region both PMOS and NMOS are always saturated, since $V_{DS} = V_{GS}$. An analytical expression for V_t is given by 1.

$$V_t = \frac{\gamma}{1+\gamma} VDD \tag{1}$$

Where:

$$\gamma = \sqrt{\frac{K_p \frac{W_P}{L_P}}{K_n \frac{W_N}{L_N}}} \tag{2}$$

An ideal scenario, and which we are seeking, is $V_t = \frac{VDD}{2}$. This is for $\gamma = 1$. Equation 1 does not consider modulation channel.

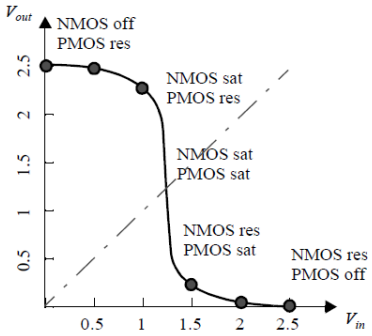

Fig. 2. Input voltage vs Output voltage and CMOS regions

B. The Dynamic CMOS Design

The propagation delay of the CMOS inverter is determined by the time it takes to charge and discharge the load capacitor C_L through the PMOS and NMOS transistors, respectively. This observation suggests that getting C_L as small as possible is crucial to the realization of high-performance CMOS circuits.[1] A digital circuit often is modeled as First-Order RC network, Figure 3, and the propagation delay of such a network is thus of considerable interest.

When applying a step input (with V_{in} going from 0 to V) the transient response of this circuit is known to be an exponential function, and is given by the following expression (where $\tau = R_{eq}C_L$, the time constant of the network):

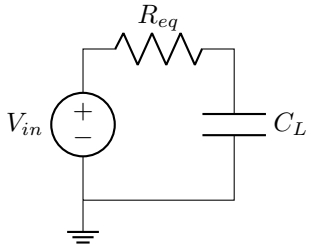

Fig. 3. First order RC network

$$V_{out}(t) = \left(1 - e^{-t/\tau}\right) \tag{3}$$

The time to reach the 50% point is easily computed as:

$$t = ln(2)\tau = 0.69\tau = 0.69R_{eq}C_L \tag{4}$$

To reach 90%:

$$t = ln(9)\tau = 2.2\tau = 2.2R_{eq}C_L \tag{5}$$

Using RC network approximation to describe time of propagation in CMOS inverter, Figure 1, and considering 90% of final value, we get:

$$t_{PHL} = ln(9)R_{eqN}C_L = 2.2R_{eqN}C_L \tag{6}$$

$$t_{PLH} = ln(9)R_{eqP}C_L = 2.2R_{eqP}C_L \tag{7}$$

where:

$$R_{eqN} = \frac{1}{VDD/2}\int_{Vdd/2}^{VDD}\frac{V(t)dt}{I_{sat}} = \frac{3VDD}{4I_{sat}} \tag{8}$$

and:

$$I_{dsat} \approx K_n\frac{W}{L}(V_{DD} - V_{th})V_{dsat} - \frac{V_{dsat}^2}{2} \qquad V_{dsat} \approx \frac{V_{DD}}{2} \tag{9}$$

To obtain frequency, which relates transition from Low to High (t_{PLH}) and transition High to Low (t_{PHL}), we have:

$$f_{max} = \frac{1}{t_p} = \frac{t_{PLH} + t_{PHL}}{2} \tag{10}$$

Using R_{eqN} and I_{sat} defined previously:

$$t_{PHL} = 2.2\frac{3C_LV_{DD}}{4I_{dsat}N} \approx 1.64\frac{C_L}{W/LK_nV_{dsatn}} \tag{11}$$

1) NAND & NOR gates: The last part, before development, is to know CMOS configuration for NAND and NOR gates, NAND is presented in Figure 4, while NOR is in Figure 5

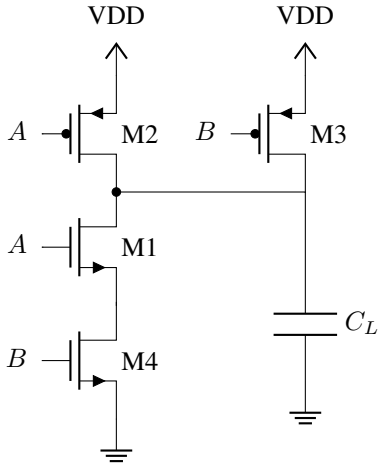

Fig. 4. NAND in CMOS Technology

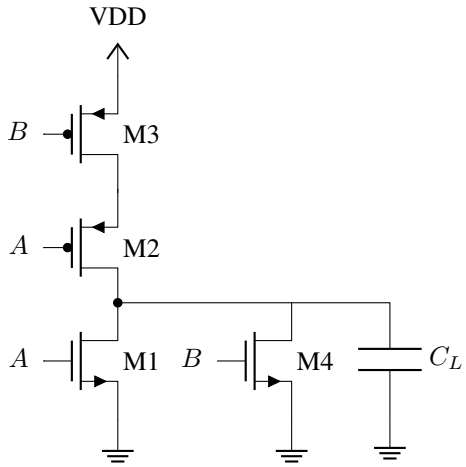

Fig. 5. NOR in CMOS Technology

II. Development

In this section we design Inverter, NAND and NOR gates with the following parameters:

- $F_{max} = 1GHz$
- $C_L = 300fF$
- $K_N = 263\mu A/V^2$
- $K_P = 95\mu A/V^2$
- $V_{DD} = 1.8V$
- $V_{thn} = 0.5V$
- $V_{thp} = -0.5V$
- $V_t = 0.9V$

From equation 2 and doing some math, we get equation 12, which help us to determine relationship between sizes and manufacture process gains:

$$W_P/L_P = \frac{1}{\frac{K_p}{K_n}}W_N/L_N \tag{12}$$

Evaluating with parameters:

$$W_P/L_P = 2.768W_N/L_N \tag{13}$$

Then, using equation 11 in dynamic design section and solving for W_N/L_N:

$$\frac{W_N}{L_N} = 1.64\frac{C_L}{t_{PHL}K_nV_{dsatn}} \tag{14}$$

Using equations 13 and 14, and setting $L_N = L_P = 180nm$ we can code a script in Python, figure 6, to automate this design process and get W and L of PMOS and NMOS transistors.

```
fmax = 1e9  #Frequency max
CL = 300e-15 #Load capacitance
tp = 1 / fmax #Time propagation
thl = tp / 2 #Time propagation from High to Low
vdd = 1.8 #Supply voltaje
vth = 0.5 #Threshold voltage
kn = 263e-6 #Manufacture process gain
vdsat = vdd/2 - vth #Velocity voltage
WLN = 3.3* (CL) / (thl * kn * vdsat)
#WLN=1.64* (CL) / (thl * kn * vdsat) #To reach 90% of final value
#WLN =0.52 * (CL) / (thl * kn * vdsat) #To reach 50% of final value
WLP = 2.768 * WLN #Relación W/L del PMOS con Vm = VDD/2
WN = WLN * 0.18  #W of NMOS = 180nm
WP = WLP * 0.18  #W of PMOS = 180nm

print(f"PMOS:\n W/L= {WLP}\n W={WP}um \n L=180nm")
print(f"NMOS:\n W/L= {WLN}\n W={WN}um \n L=180nm")
```

Fig. 6. Script to determine Width and Length of PMOS and NMOS

Inserting the parameters defined previously in the script, we get Table I. It is important to consider critical stages in NAND and NOR due to its truth tables. In NAND,Figure 4, when $A = 1 = 1.8V$ and $B = 1 = 1.8V$, then $R_{eq} = 2 * R_{eqN}$, since M1 and M4 are both in saturation and capacitor's path to discharge is through two resistor. In the same way, NOR gate, Figure 5, when $A = 1 = 1.8V$ and $B = 1 = 1.8V$, then $R_{eq} = 2 * R_{eqP}$ because Current passes through two resistors to charge capacitive load.

	W_P	L_P	W_N	L_N
Inverter	$4.6\mu m$	180nm	$1.6\mu m$	180nm
NAND	$4.5\mu m$	180nm	$3.5\mu m$	180nm
NOR	$9.3\mu m$	180nm	$1.5\mu m$	180nm

TABLE I
WIDTH AND LENGTH OF CMOS GATES

LTSpice simulations are shown in figures 7, 8, 9.

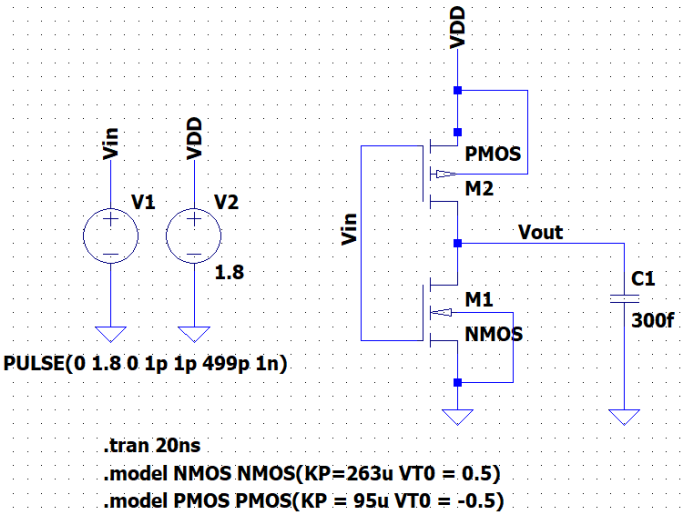

Fig. 7. CMOS inverter in LTSpice

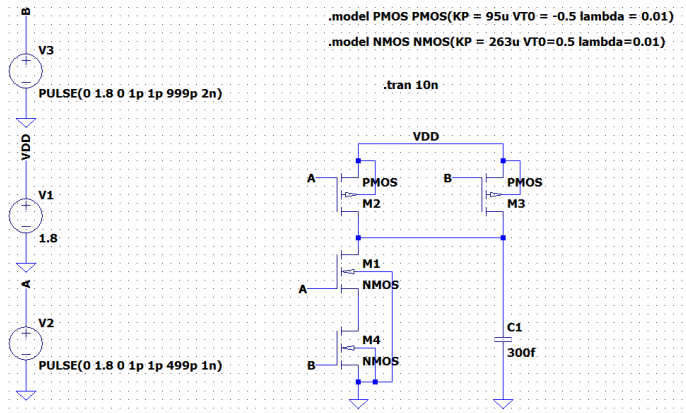

Fig. 8. CMOS NAND in LTSpice

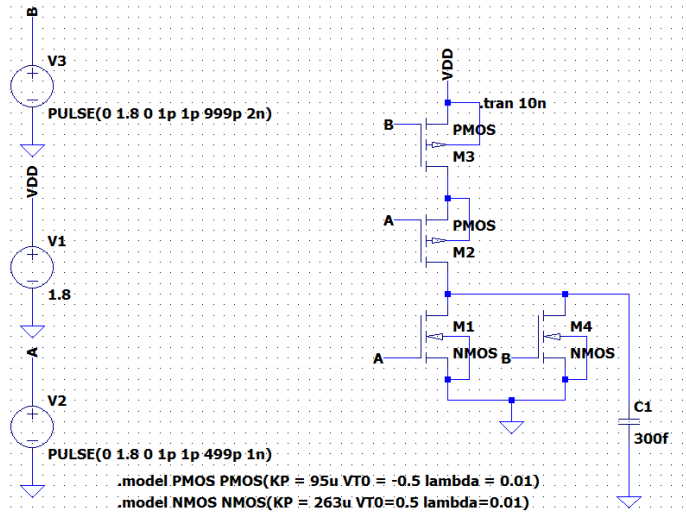

Fig. 9. CMOS NOR in LTSpice

III. Results and conclusions

Figures 10, 11 and 12 shows transient analysis in which we can see that output value reach its final value in time requested, 1GHz with capacitive load of 300f F, this means that our consideration of $R_{eq} = 2R_{eq_n}$ in critical stages, in NAND and NOR gates was correct.

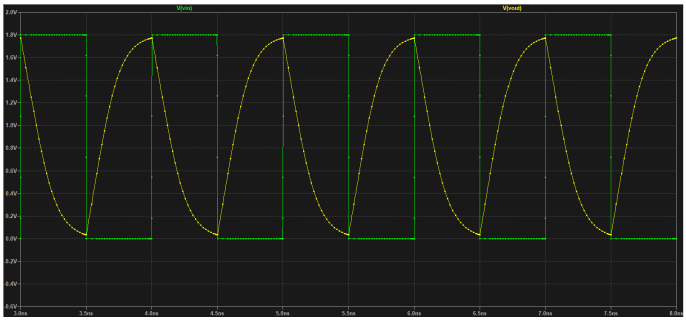

Fig. 10. Transient analysis of CMOS inverter

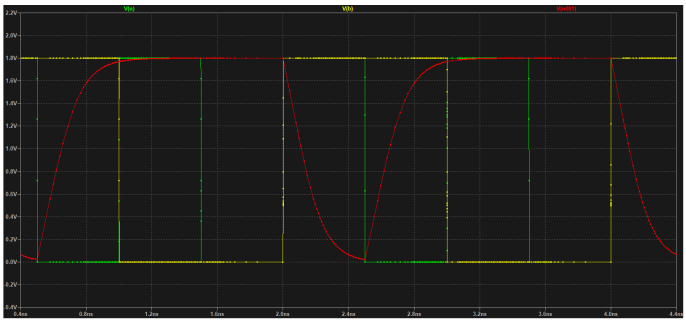

Fig. 11. Transient analysis of CMOS NAND

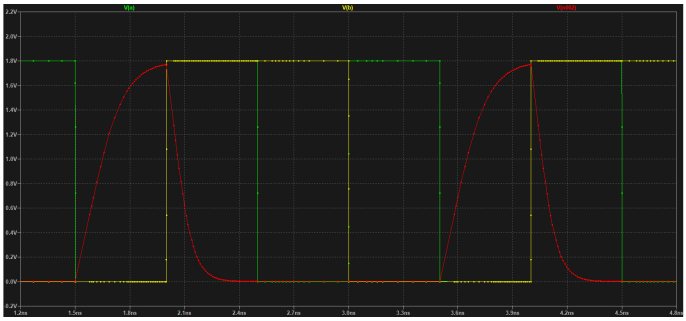

Fig. 12. Transient analysis of CMOS NOR

References

[1] M. Rabaey, Digital Integrated Circuits, 2nd ed.: Prentice Hall, 2003, ISNB: 9788120322578