X1520

IoT Application Processor

Data Sheet

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Data Sheet

Disclaimer

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1 Overview

X1520 is a low power consumption, high performance and high integrated application processor focus on IoT devices like bar-code scanner devices and square-code scanner devices. X1520 provides high-speed CPU computing power and excellent image signal process. And it can match the requirements of many other embedded products.

The CPU (Central Processing Unit) core, equipped with 32kB instruction and 32kB data level 1 cache, and 128kB level 2 cache, operating at 1.2GHz, and full feature MMU function performs OS related tasks. At the heart of the CPU core is XBurst® processor engine. XBurst® is an industry leading microprocessor core which delivers superior high performance and best-in-class low power consumption. A hardware floating-point unit which compatible with IEEE754 is also included. The MXU2.0(SIMD128) instruction set has been implemented by XBurst® engine, and is one part of the CPU.

With the powerful CPU, X1520 supports various computer vision applications, such as face detection, human detection, gesture recognition, and etc. Also people can develop new computer vision application using the MXU2.0 to accelerate it.

The ISP (Image signal processor) core supports excellent image process with the image coming from raw sensors. It supports DVP interface. With the functions, such as 3A, 2D and 3D denoise, WDR/HDR, lens shading, it can supply maximum resolution 2048x1536 resolution image for view or encoding to store or transfer.

For more quickly and easily to use X1520, one 32Mbit DDR2 is integrated.

On-chip modules such as audio CODEC, multi-channel SAR-ADC controller and camera interfaces offer designers a economical suite of peripherals for scanner application. WLAN, Bluetooth and expansion options are supported through high-speed SPI and MMC/SD/SDIO host controllers. Other peripherals such as USB OTG, UART and SPI as well as general system resources provide enough computing and connectivity capability for many applications.

1.1 Block Diagram

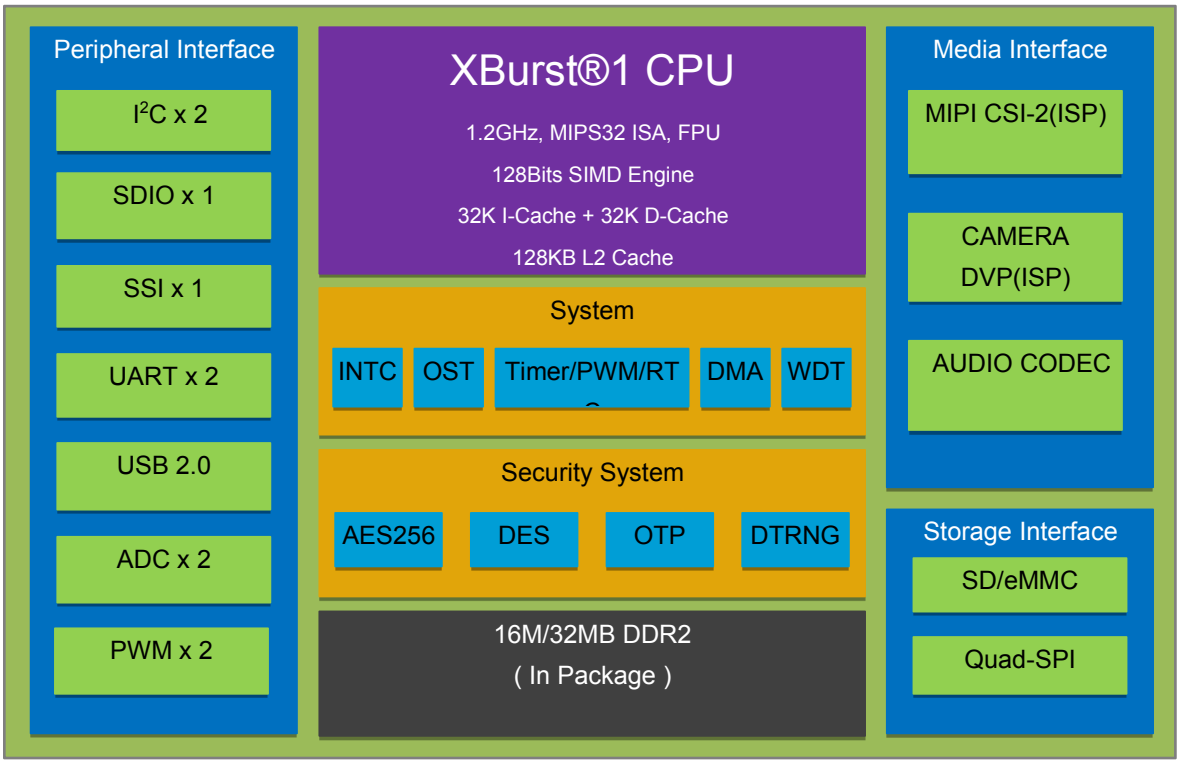


Figure 1- 1 X1520 Diagram

1.2 Features

1.2.1 CPU

- XBurst®-1 core
  - XBurst® RISC instruction set
  - XBurst® SIMD128 instruction set
  - XBurst® FPU instruction set supporting both single and double floating point format which are IEEE754 compatible
  - XBurst® 9-stage pipeline micro-architecture, the operating frequency is 1.2GHz
- MMU
  - 32-entry joint-TLB
  - 8-entry Instruction TLB
  - 8-entry data TLB
- L1 Cache
  - 32KB instruction cache
  - 32KB data cache
- Hardware debug support
- 16KB tight coupled memory
- L2 Cache
  - 128KB unified cache

1.2.2 ISP

- Max input resolution 2048x1536 @30fps, 1080p @45fps,720p @60fps.
- Input image up to 12bit RAW or Up to 24bit RGB. Both RGB and YCbCr are supported from sensor.
- Up to 2 output channel. Image crop and downscaler.
- 2-D and 3-D noise reduction filter lead to high levels of noise reduction with minimal effect on edges and textures.
- Single frame and multi frame WDR/HDR provide high dynamic range in both still and video capture modes.
- Advanced demosaic, colour processing, lens shading, defog, glare, static/dynamic defect pixel and other modules provide high image quality.
- 3A supported.
- Flash timer

1.2.3 Image post processor(IPU)

- AXI Bus for data transaction
- Input data format:
  - ARGB, RGB, NV12/NV21
- Output data format:
  - ARGB, RGB
  - NV12/NV21
  - HSV
- Color conversion feature: input and output format can be chosen freely from input and output data format.
- Minimum input image size (pixel): 4x4
- Maximum input image size (pixel): 2047x2047
- Minimum output image size (pixel): 4x4
- Maximum output image size (pixel): 2047x2047
- Background channel OSD function:
  - Support 4 layers OSD
  - Support whole background picture into OSD process and partial picture into OSD process
  - Support 12 port-duff OSD modes
  - Support 5 input format in background channel: ARGB8888, ARGB1555, RGB888, NV12, NV21. RGB can be in following sequence: RGB, RBG, BRG, BGR, GRB, GBR. Specifically, RGB888 format data occupy 4 bytes when stored in memory, RGB occupy three bytes, and the forth byte can be any value, as it will never be used in IPU.
  - Output picture format must be the same with the input picture format of separated background channel.

1.2.4 Camera interfaces

- DVP input
  - DVP Input data format: YUV422, RGB565, RGB555, RAW8, RAW10, RAW12.

- MIPI CSI2 2-lane input
  - MIPI CSI-2 input format: RAW8, RAW10, RAW12, RGB555, RGB565, RGB666, RGB888, YUV422

1.2.5 Audio

- Integrated Audio codec.
  - 24 bits DAC with 93dB SNR
  - 24 bits ADC with 92dB SNR
  - Support signal-ended and differential microphone input and line input
  - Automatic Level Control (ALC) for smooth audio recording
  - Pure logic process: no need for mixed signal layers and less mask cost
  - Programmable input and output analog gains
  - Digital interpolation and decimation filter integrated
  - Sampling rate 8K/12K/16K/24K/32/44.1K/48K/96K

1.2.6 Memory Interface

- Integrated 32Mbits DDR2

1.2.7 System Functions

- Clock generation and power management
  - On-chip 12/24/48MHZ oscillator circuit
  - External 32.768KHZ input
  - One three-chip phase-locked loops (PLL) with programmable multiplier
  - CCLK, HHCLK, H2CLK, PCLK, H0CLK, DDR_CLK, HELIX_CLK frequency can be changed separately for software by setting registers
  - SSI clock supports 50M clock
  - MSC clock supports 100M clock
  - Functional-unit clock gating
- Timer and counter unit with PWM output and/or input edge counter
  - Provide four separate channels, two of them have input signal transition edge counter
  - 16-bit A counter and 16-bit B counter with auto-reload function every channel
  - Support interrupt generation when the A counter underflows
  - Three clock sources: RTCLK (real time clock), EXCLK (external clock input), PCLK (APB Bus clock) selected with 1, 4, 16, 64, 256 and 1024 clock dividing selected
  - Every channel has PWM output
- OS timer
  - 64-bit counter and 32-bit compare register
  - Support interrupt generation when the counter matches the compare register
  - Two clock sources: RTCLK (real time clock), HCLK (system bus clock) selected with 1, 4, 16, 64, 256 and 1024 clock dividing selected
- Interrupt controller
  - Total 64 interrupt sources
  - Each interrupt source can be independently enabled

  - Priority mechanism to indicate highest priority interrupt
  - All the registers are accessed by CPU
  - Unmasked interrupts can wake up the chip in sleep mode
  - Another set of source, mask and pending registers to serve for PDMA
- Watchdog timer
  - Generates WDT reset
  - A 16-bit Data register and a 16-bit counter
  - Counter clock uses the input clock selected by software
- PCLK, EXTAL and RTCCLK can be used as the clock for counter
- The division ratio of the clock can be set to 1, 4, 16, 64, 256 and 1024 by software
- Direct memory access controllers
  - Support up to 32 independent DMA channels
  - Descriptor or No-Descriptor Transfer mode compatible with previous JZ SOC
  - Transfer data units: 1-byte, 2-byte, 4-byte, 16-byte, 32-byte, 64-byte, 128-byte
  - Transfer number of data unit: 1 ~ 2^{24} - 1
  - Independent source and destination port width: 8-bit, 16-bit, 32-bit
  - Fixed three priorities of channel groups: 0~3, highest; 4~11: mid; 12~31: lowest
  - An extra INTC IRQ can be bound to one programmable DMA channel
- SAR A/D Controller
  - 2 Channels
  - Resolution: 10-bit
  - Integral nonlinearity: ±2 LSB
  - Differential nonlinearity: ±1 LSB
  - Resolution/speed: up to 1Msps
  - Max Clock Frequency: 24MHz
  - Low power dissipation: 1.5mW(worst)
  - Support two auxiliary input (Through pin ADC_AIN0 to AIN1)
  - Pin Description
- RTC (Real Time Clock)
  - Need external 32768Hz oscillator for 32k clock generation
  - 32-bits second counter
  - Programmable and adjustable counter to generate accurate 1 Hz clock
  - Alarm interrupt, 1Hz interrupt

1.2.8 Peripherals

- General-Purpose I/O ports
  - Each port can be configured as an input, an output or an alternate function port
  - Each port can be configured as an interrupt source of low/high level or rising/falling edge triggering. Every interrupt source can be masked independently
  - Each port has an internal pull-up or pull-down resistor connected. The pull-up/down resistor can be disabled
  - GPIO output 3 interrupts, each interrupt corresponds to the group, to INTC
- SMB Controller

- Two-wire SMB serial interface – consists of a serial data line (SDA) and a serial clock (SCL)
- Two speeds
  - Standard mode (100 Kb/s)
  - Fast mode (400 Kb/s)
- Device clock is identical with pclk
- Programmable SCL generator
- Master or slave SMB operation
- 7-bit addressing/10-bit addressing
- 16-level transmit and receive FIFOs
- Interrupt operation
- The number of devices that you can connect to the same SMB-bus is limited only by the maximum bus capacitance of 400pF
- APB interface
- 2 independent SMB channels (SMB0, SMB1)

- One High Speed Synchronous serial interfaces (SFC0)
  - 3 protocols support: National's Microwire, TI's SSP, and Motorola's SPI
  - transmit-only or receive-only operation
  - MSB first for command and data transfer, and LSB first for address transfer
  - 64 entries x 32 bits wide data FIFO
  - one device select
  - Configurable sampling point for reception
  - Configurable timing parameters: tSLCH, tCHSH and tSHSL
  - Configurable flash address wide are supported
  - 7 transfer formats: Standard SPI, Dual-Output/Dual-Input SPI, Quad-Output/Quad-Input SPI, Dual-I/O SPI, Quad-I/O SPI, Full Dual-I/O SPI, Full Quad-I/O SPI
  - two data transfer mode: slave mode and DMA mode
  - Configurable 6 phases for software flow
- One Normal Speed Synchronous serial interfaces (SSI0)
  - 3 protocols support: National's Microwire, TI's SSP, and Motorola's SPI
  - Full-duplex or transmit-only or receive-only operation
  - Programmable transfer order: MSB first or LSB first
  - 128 entries deep x 32 bits wide transmit and receive data FIFOs
  - Configurable normal transfer mode or Interval transfer mode
  - Programmable clock phase and polarity for Motorola's SSI format
  - Back-to-back character transmission/reception mode
- Two Universal Asynchronous Receiver/Transmitter interfaces (UART0, UART1)
  - Full-duplex operation
  - 5-, 6-, 7- or 8-bit characters with optional no parity or even or odd parity and with 1, 1½, or 2 stop bits
  - 64x8 bit transmit FIFO and 64x11bit receive FIFO
  - Independently controlled transmit, receive (data ready or timeout), line status interrupts
  - Internal diagnostic capability Loopback control and break, parity, overrun and

framing-error is provided
- Separate DMA requests for transmit and receive data services in FIFO mode
- Supports modem flow control by software or hardware
- Slow infrared asynchronous interface that conforms to IrDA specification

- One MMC/SD/SDIO controllers (MSC1)
  - Fully compatible with the MMC System Specification version 4.2
  - Support SD Specification 3.0
  - Support SD I/O Specification 1.0 with 1 command channel and 4 data channels
  - Consumer Electronics Advanced Transport Architecture (CE-ATA – version 1.1)
  - Maximum data rate is 50MBps
  - Support MMC data width 1bit and 4bit
  - Built-in programmable frequency divider for MMC/SD bus
  - Built-in Special Descriptor DMA
  - Maskable hardware interrupt for SDIO interrupt, internal status and FIFO status
  - 128 x 32 built-in data FIFO
  - Multi-SD function support including multiple I/O and combined I/O and memory
  - IRQ supported enable card to interrupt MMC/SD controller
  - Single or multi block access to the card including erase operation
  - Stream access to the MMC card
  - Supports SDIO read wait, interrupt detection during 1-bit or 4-bit access
  - Supports CE-ATA digital protocol commands
  - Support Command Completion Signal and interrupt to CPU
  - Command Completion Signal disable feature
  - The maximum block length is 4096bytes
- USB 2.0 interface
  - Complies with the USB 2.0 standard for high-speed (480 Mbps) functions and with the On-The-Go supplement to the USB 2.0 specification
  - Operates either as the function controller of a high- /full-speed USB peripheral or as the host/peripheral in point-to-point or multi-point communications with other USB functions
  - Supports Session Request Protocol (SRP) and Host Negotiation Protocol (HNP)
  - UTMI+ Level 3 Transceiver Interface
  - Soft connect/disconnect
  - 16 Endpoints:
  - Dedicate FIFO
  - Supports control, interrupt, ISO and bulk transfer
- Digital True Random Number Generator（DTRNG）
  - Pure digital logic circuits
  - True random number
  - Interrupt mode and no interrupt mode

1.2.9 Bootrom

16kB Boot ROM memory

1.3 Characteristic

Item	Characteristic
Process Technology	40nm CMOS low power
Power supply voltage	General purpose I/O: 3.0~3.6V DVP I/O: 1.6~3.6V DDR I/O for DDR2: 1.8V ± 0.1V EFUSE programming: 2.5V ± 10% Analog power supply 1: 2.5V ± 10% Analog power supply 2: 3.3V ± 10% Core: 1.1V ± 0.1V
Package	BGA104 6mm x 8mm x 1.27mm, 0.65mm pitch
Operating frequency	1.2 GHz

2 Packaging and Pinout Information

2.1 Overview

X1520 processor is offered in 104-pin LFBGA package, which is 6mm x 8mm x 1.27mm outline, 9 x 12 matrix ball grid array and 0.65mm ball pitch, show in Figure 2-1. The X1520 pin to ball assignment is show in Figure 2-2. The detailed pin description is listed in Table 2-1~Table 2-16.

2.2 Solder Process

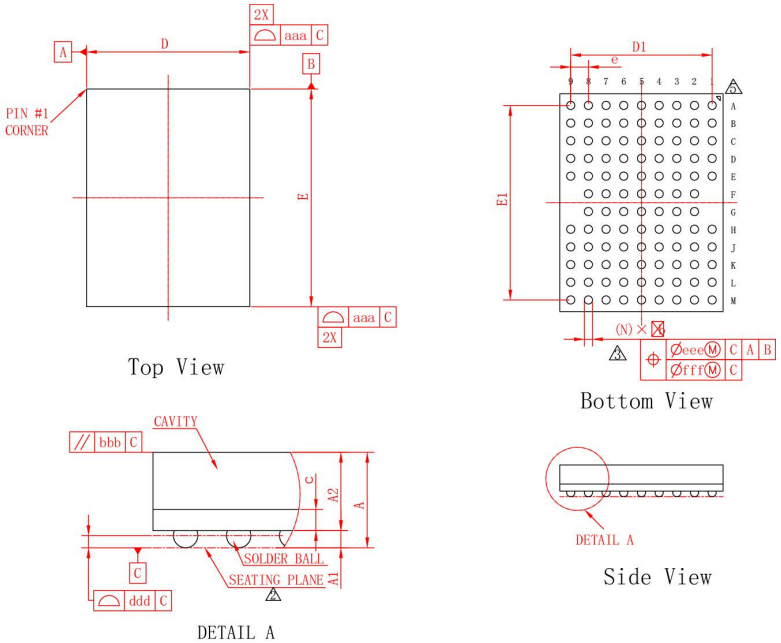
X1520 package is lead-free. It's reflow profile follows the IPC/JEDEC lead-free reflow profile as contained in J-STD-020E.

2.3 Moisture Sensitivity Level

X1520 package moisture sensitivity is level 3.

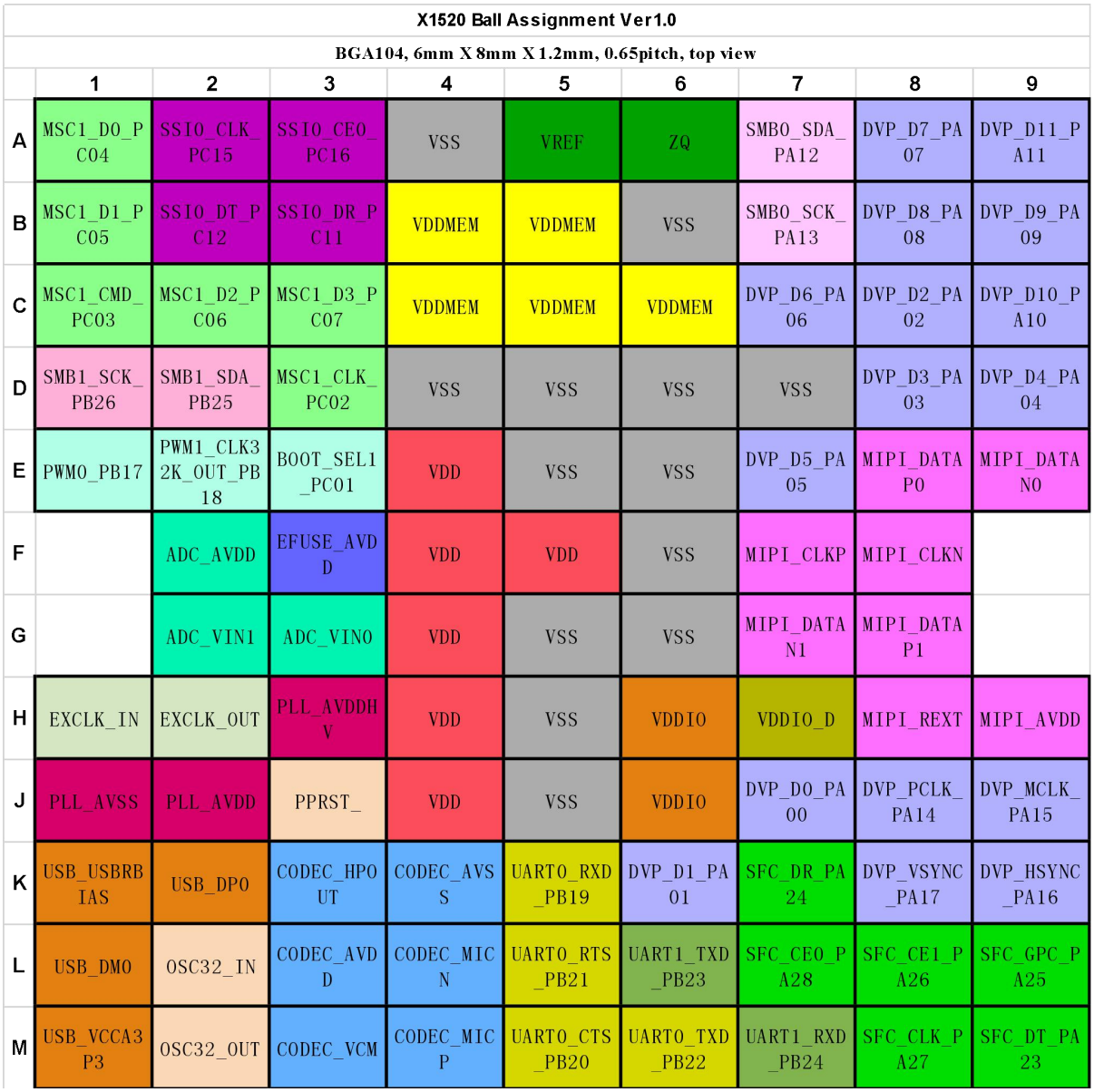
2.4 X1520 Package

symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.270	---	---	0.050
A1	0.160	0.210	0.260	0.006	0.008	0.010
A2	0.910	0.960	1.010	0.036	0.038	0.040
c	0.220	0.260	0.300	0.009	0.010	0.012
D	5.900	6.000	13.100	0.232	0.236	0.516
E	5.900	8.000	13.100	0.232	0.315	0.516
D1	---	5.200	---	---	0.205	---
E1	---	7.150	---	---	0.281	---
e	---	0.650	---	---	0.026	---
b	0.250	0.300	0.350	0.010	0.012	0.014
aaa	0.100			0.004		
bbb	0.100			0.004		
ddd	0.100			0.004		
eee	0.150			0.006		
fff	0.080			0.003		
Ball Diam	0.300			0.012		
N	104			104		
MD/ME	9/12			9/12		



TECHNOLOGY SPECIFICATION[技术要求]
1. BALL PAD OPENING: 0.27m; [球形防焊开口: 0.27mm;]
⚠PRIMARY DATUM C AND SEATING PLANE ARE THE SOLDER BALLS;
[主要基准C和底面是锡球;]
⚠DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C; [尺寸b是测量最大锡球直径, 平行于主要基准C;]
4. SPECIAL CHARACTERISTICS C CLASS: bbb, ddd; [特殊特性C类: bbb, ddd;]
⚠THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY;
[PIN 1 标识仅供参考;]
6. BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES;
[禁止使用一级环境管理物质;]

Figure 2-1 X1520 package outline drawing



	1	2	3	4	5	6	7	8	9
A	MSC1_D0_PC04	SSI0_CLK_PC15	SSI0_CE0_PC16	VSS	VREF	ZQ	SMB0_SDA_PA12	DVP_D7_PA07	DVP_D11_PA11
B	MSC1_D1_PC05	SSI0_DT_PC12	SSI0_DR_PC11	VDDMEM	VDDMEM	VSS	SMB0_SCK_PA13	DVP_D8_PA08	DVP_D9_PA09
C	MSC1_CMD_PC03	MSC1_D2_PC06	MSC1_D3_PC07	VDDMEM	VDDMEM	VDDMEM	DVP_D6_PA06	DVP_D2_PA02	DVP_D10_PA10
D	SMB1_SCK_PB26	SMB1_SDA_PB25	MSC1_CLK_PC02	VSS	VSS	VSS	VSS	DVP_D3_PA03	DVP_D4_PA04
E	PWM0_PB17	PWM1_CLK32K_OUT_PB18	BOOT_SEL1_PC01	VDD	VSS	VSS	DVP_D5_PA05	MIPI_DATAP0	MIPI_DATAN0
F		ADC_AVDD	EFUSE_AVDD	VDD	VDD	VSS	MIPI_CLKP	MIPI_CLKN	
G		ADC_VIN1	ADC_VIN0	VDD	VSS	VSS	MIPI_DATAN1	MIPI_DATAP1	
H	EXCLK_IN	EXCLK_OUT	PLL_AVDDHV	VDD	VSS	VDDIO	VDDIO_D	MIPI_REXT	MIPI_AVDD
J	PLL_AVSS	PLL_AVDD	PPRST_	VDD	VSS	VDDIO	DVP_D0_PA00	DVP_PCLK_PA14	DVP_MCLK_PA15
K	USB_USBRBIAS	USB_DP0	CODEC_HPOUT	CODEC_AVSS	UART0_RXD_PB19	DVP_D1_PA01	SFC_DR_PA24	DVP_VSYNC_PA17	DVP_HSYNC_PA16
L	USB_DM0	OSC32_IN	CODEC_AVDD	CODEC_MICN	UART0_RTS_PB21	UART1_TXD_PB23	SFC_CE0_PA28	SFC_CE1_PA26	SFC_GPC_PA25
M	USB_VCCA3P3	OSC32_OUT	CODEC_VCM	CODEC_MICP	UART0_CTS_PB20	UART0_TXD_PB22	UART1_RXD_PB24	SFC_CLK_PA27	SFC_DT_PA23

Figure 2-2 X1520 pin to ball assignment

2.5 Pin Description [1][2]

2.5.1 DDR

Table 2-1 DDR2 Pins (2)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
VREF	AI	A5		VREF: DDR2 input reference voltage	VDDMEM/2
ZQ	AIO	A6		ZQ: DDR2 External reference which is connected to a 240ohm resister to VSS	

2.5.2 I2C1

Table 2-2 I2C0/I2C1 Pins(4)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
SMB0_SDA PA12	IO IO	A7	8mA pullup-pe rst-pe	SMB0_SDA: I2C 0 serial data PA12: GPIO group A bit 12	VDDIO_D
SMB0_SCL PA13	IO IO	B7	8mA pullup-pe rst-pe	SMB0_SCL: I2C 0 serial clock PA13: GPIO group A bit 13	VDDIO_D
SMB1_SDA PB25	IO IO	D2	8mA pullup-pe rst-pe	SMB1_SDA: I2C 1 serial data PB25: GPIO group B bit 25	VDDIO
SMB1_SCL PB26	IO IO	D1	8mA pullup-pe rst-pe	SMB1_SCL: I2C 1 serial clock PB26: GPIO group B bit 26	VDDIO

2.5.3 DVP

Table 2-3 DVP Pins (16)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
DVP_D0 PA00	I IO	J7	8mA pullup-pe	DVP_D0: DVP data bit 0 PA00: GPIO group A bit 00	VDDIO_D
DVP_D1 PA01	I IO	K6	8mA pullup-pe	DVP_D1: DVP data bit 1 PA01: GPIO group A bit 01	VDDIO_D
DVP_D2 PA02	I IO	C8	8mA pullup-pe	DVP_D2: DVP data bit 2 PA02: GPIO group A bit 02	VDDIO_D
DVP_D3 PA03	I IO	D8	8mA pullup-pe	DVP_D3: DVP data bit 3 PA03: GPIO group A bit 03	VDDIO_D
DVP_D4 PA04	I IO	C9	8mA pullup-pe	DVP_D4: DVP data bit 4 PA04: GPIO group A bit 04	VDDIO_D
DVP_D5 PA05	I IO	E7	8mA pullup-pe	DVP_D5: DVP data bit 5 PA05: GPIO group A bit 05	VDDIO_D
DVP_D6 PA06	I IO	C7	8mA pullup-pe	DVP_D6: DVP data bit 6 PA06: GPIO group A bit 06	VDDIO_D
DVP_D7 PA07	I IO	A8	8mA pullup-pe	DVP_D07: DVP data bit 7 PA07: GPIO group A bit 07	VDDIO_D
DVP_D8 PA08	I IO	B8	8mA pullup-pe	DVP_D08: DVP data bit 8 PA08: GPIO group A bit 08	VDDIO_D
DVP_D9 PA09	I IO	B9	8mA pullup-pe	DVP_D09: DVP data bit 9 PA09: GPIO group A bit 09	VDDIO_D
DVP_D10 PA10	I IO	C9	8mA pullup-pe	DVP_D10: DVP data bit 10 PA10: GPIO group A bit 10	VDDIO_D
DVP_D11 PA11	I IO	A9	8mA pulldown-pe	DVP_D11: DVP data bit 11 PA11: GPIO group A bit 11	VDDIO_D
DVP_PCLK PA14	I IO	J8	8mA pullup-pe rst-pe	DVP_PCLK: DVP pixel clock input PA14: GPIO group A bit 14	VDDIO_D

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
DVP_MCLKP A15	O IO	J9	8mA pullup-pe rst-pe	DVP_MCLK: DVP master clock output PA15: GPIO group A bit 15	VDDIO_D
DVP_HSYNC PA16	I IO	K9	8mA pulldown-pe rst-pe	DVP_HSYNC: DVP line horizonal sync input PA16: GPIO group A bit 16	VDDIO_D
DVP_VSYNC PA17	I IO	K8	8mA pullup-pe rst-pe	DVP_VSYNC: DVP vertical sync input PA17: GPIO group A bit 17	VDDIO_D

2.5.4 MSC1

Table 2-4 MSC0/MSC1 Pins (6)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
MSC1_CLK PC02	O IO	D3	8mA pullup-pe	MSC1_CLK: MSC (MMC/SD) 1 clock output PC02: GPIO group C bit 02	VDDIO
MSC1_CMD PC03	IO IO	C1	8mA pullup-pe	MSC1_CMD: MSC (MMC/SD) 1 command PC03: GPIO group C bit 03	VDDIO
MSC1_D0 PC04	IO IO	A1	8mA pullup-pe	MSC1_D0: MSC (MMC/SD) 1 data bit 0 PC04: GPIO group C bit 04	VDDIO
MSC1_D1 PC05	IO IO	A2	8mA pullup-pe	MSC1_D1: MSC (MMC/SD) 1 data bit 1 PC05: GPIO group C bit 05	VDDIO
MSC1_D2 PC06	IO IO	C2	8mA pullup-pe	MSC1_D2: MSC (MMC/SD) 1 data bit 2 PC06: GPIO group C bit 06	VDDIO
MSC1_D3 PC07	IO IO	C3	8mA pullup-pe	MSC1_D3: MSC (MMC/SD) 1 data bit 3 PC07: GPIO group C bit 07	VDDIO

2.5.5 PWM

Table 2-5 PWM Pins (2)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
PWM0 PB17	IO IO	E1	8mA pulldown-pe rst_pe	PWM0: PWM output or pulse input 0 PB17: GPIO group B bit 17.	VDDIO
PWM1 CLK32K_OUT PB18	IO O IO	E2	8mA pulldown-pe rst_pe	PWM1: PWM output or pulse input 1 CLK32K_OUT: 32.768K clock out PB18: GPIO group B bit 18.	VDDIO

2.5.6 UART

Table 2-6 UART Pins (6)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
UART0_RXD PB19	I IO	K5	8mA pullup-pe	UART0_RXD: uart 0 receive data PB19: GPIO group B bit 19	VDDIO

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
UART0_CTS PB20	I IO	M5	8mA pullup-pe	UART0_CTS: uart 0 clear to send input PB20: GPIO group B bit 20	VDDIO
UART0_RTS PB21	O IO	L5	8mA pullup-pe	UART0_RTS:uart 0 request to send PB21: GPIO group B bit 21	VDDIO
UART0_TXD PB22	O IO	M6	8mA pullup-pe	UART0_TXD: UART 0 transmit data PB22: GPIO group B bit 22	VDDIO
UART1_TXD PB23	O IO	L6	8mA pullup-pe	UART1_TXD: UART 1 transmit data PB23: GPIO group B bit 23	VDDIO
UART1_RXD PB24	I IO	M7	8mA pullup-pe rst-pe	UART1_RXD: UART 1 receive data PB24: GPIO group B bit 24	VDDIO

2.5.7 SFC/SSI0

Table 2-7 SFC/SSI0 Pins (12)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
SFC_DT PA23	IO IO	M9	8mA pullup-pe rst_pe	SFC_DT: high speed ssi transmit data PA23: GPIO group A bit 23	VDDIO
SFC_DR PA24	IO IO	K7	8mA pullup-pe rst_pe	SFC_DR: high speed ssi receive data PA24: GPIO group A bit 24	VDDIO
SFC_GPC PA25	IO IO	L9	8mA pullup-pe rst-pe	SFC_GPC: high speed ssi general-purpose control PA25: GPIO group A bit 25	VDDIO
SFC_CE1 PA26	IO IO	L8	8mA pulldown-pe rst-pe	SFC_CE1: high speed ssi chip 1 select PA26: GPIO group A bit 26	VDDIO
SFC_CLK PA27	IO IO	M8	8mA pullup-pe rst-pe	SFC_CLK: high speed ssi clock PA27: GPIO group A bit 27	VDDIO
SFC_CE0 PA28	IO IO	L7	8mA pullup-pe rst-pe	SFC_CE0: high speed ssi chip 0 select PA28: GPIO group A bit 28	VDDIO
SSI0_DR PC11	IO IO	B3	8mA pullup-pe	SSI0_DR: normal speed ssi 0 receive data PC11: GPIO group C bit 11	VDDIO
SSI0_DT PC12	IO IO	B2	8mA pullup-pe	SSI0_DT: normal speed ssi 0 transmit data PC12: GPIO group C bit 12	VDDIO
SSI0_CLK PC15	IO IO	A2	8mA pullup-pe	SSI0_CLK: normal speed ssi 0 clock PC15: GPIO group C bit 15	VDDIO
SSI0_CE0 PC16	IO IO	A3	8mA pulldown-pe rst-pe	SSI0_CE0: normal speed ssi 0 chip 0 select PC16: GPIO group C bit 16	VDDIO

2.5.8 System

Table 2-8 System Pins(1)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
PC01 (BOOT_SEL1)	IO I	E3	8mA pullup-pe	PC01: GPIO group C bit 01 It is taken as BOOT select bit 1 by Boot ROM code	VDDIO

2.5.9 Digital power/ground

Table 2-9 IO/Core power supplies for FBGA (30)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
VDDMEM	P	B4,B5,C4, C5,C6		VDDMEM: IO digital power for DDR PHY, 1.8V ± 0.1V	-
VDDIO_D	P	H7		VDDIO_D: IO digital power for DVP power domain, 1.8V~3.3V	-
VDDIO	P	H6,J6		VDDIO: IO digital power for none DRAM/NAND, 3.3V	-
VSS	P	A4,B6,D4, D5,D6,D7, E5,E6,F6,G 5,G6,H5,J5		VSS: Digital ground, 0V	-
VDD	P	E4,F4,F5,G 4,H4,J4		VDD: CORE digital power, 1.1V	-

2.5.10 Analog - USB

Table 2-10 USB 2.0 (4)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
USB_DP0	AIO	K2		USB_DP0: OTG data plus	USB_VCCA3P3
USB_DM0	AIO	M1		USB_DM0: OTG data minus	USB_VCCA3P3
USB_USBRBIAS	AIO	K1		USB_USBRBIAS: Transmitter resister tune. It connects to an external resistor of 270Ω with 1% tolerance to ground VSS, that adjusts the OTG 2.0 high-speed source impedance	USB_VCCA3P3
USB_VCCA3P3	P	L1		USB_VCCA3P3: OTG 2.0 host & OTG analog power, 3.3V	-

2.5.11 Analog - SAR ADC

Table 2-11 SAR ADC Pins (3)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
ADC_VIN0	AI	J3		ADC_AIN0: ADC general purpose input 0	ADC_AVDD

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
ADC_VIN1	AI	J2		ADC_AIN1: ADC general purpose input 1	ADC_AVDD
ADC_AVDD	P	F2		ADC_AVDD: ADC analog power, 3.3 V	-

2.5.12 Analog - CODEC

Table 2-12 CODEC Pins (6)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
CODEC_MICP	AI	M4		CODEC_MICP: differential microphone input	CODEC_AVDD
CODEC_MICN	AI	L4		CODEC_MICN: differential microphone input	CODEC_AVDD
CODEC_VCM	AO	M3		CODEC_VCM: Reference voltage output	CODEC_AVDD
CODEC_HPOUT	AO	K3		CODEC_HPOUT: headphone output	CODEC_AVDD
CODEC_AVDD	P	L3		CODEC_AVDD:3.3v analog supply	-
CODEC_AVSS	P	K4		CODEC_AVSS: Analog ground	-

2.5.13 Analog - MIPI-CSI

Table 2-13 MIPI CSI(8)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
MIPI_CLKP	AIO	F7		Positive DPHY differential clock line transceiver output	MIPI_AVDD
MIPI_CLKN	AIO	F8		Negative DPHY differential clock line transceiver output	MIPI_AVDD
MIPI_DATAP0	AIO	E8		Positive DPHY differential data line transceiver output,lane0	MIPI_AVDD
MIPI_DATAN0	AIO	E9		Negative DPHY differential data line transceiver output,lane0	MIPI_AVDD
MIPI_DATAP1	AIO	G8		Positive DPHY differential data line transceiver output,lane1	MIPI_AVDD
MIPI_DATAN1	AIO	G7		Negative DPHY differential data line transceiver output,lane1	MIPI_AVDD
MIPI_REXT	AIO	H8		Analog Probing Pin. It connects to an external resistor of 6.04KΩ with 1% tolerance to ground VSS	MIPI_AVDD
MIPI_AVDD	P	H9		MIPI_AVDD: mipi phy analog power, 2.5V	-

2.5.14 Analog - EFUSE

Table 2-14 EFUSE Pins for Two EFUSE (1)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
EFUSE_AVDD	P	F3		AVDEFUSE: EFUSE programming power, 0V/2.5V	-

2.5.15 Analog - CPM

Table 2-15 CPM Pins (5)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
EXCLK_IN	AI	H1	2~30 MHz Oscillator, OSC on/off	EXCLK_XIN: OSC input or 24MHz clock input	VDDIO
EXCLK_OUT	AO	H2		EXCLK_XOUT: OSC output	VDDIO
PLL_AVDDHV	P	H3		PLL_AVDDHV: PLL analog power, 1.8V	-
PLL_AVDD	P	J2		PLL_AVDD: PLL analog power, 1.1V	-
PLL_AVSS	P	J1		AVSPLL: PLL analog ground	-

2.5.16 Analog - RTC

Table 2-16 RTC Pins (3)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
OSC32_IN	AI	L2	32768Hz Oscillator	OSC32_IN: 32768 clock input or OSC input	VDDIO
OSC32_OUT	AO	M2		OSC32_OUT: OSC output	VDDIO
PPRST_	I	J3	Schmitt	PPRST_: RTC power on reset and RESET-KEY reset input	VDDIO

NOTES:

1 The meaning of phases in IO cell characteristics are:

- pull-up: The IO cell contains a pull-up resistor and the pull-up resistor cannot be enabled or disabled by setting corresponding register.
- pull-down: The IO cell contains a pull-down resistor and the pull-down resistor cannot be enabled or disabled by setting corresponding register.
- pullup-pe: The IO cell contains a pull-up resistor and the pull-up resistor can be enabled or disabled by setting corresponding register.
- pulldown-pe: The IO cell contains a pull-down resistor and the pull-down resistor can be enabled or disabled by setting corresponding register.
- rst-pe: these pins are initialed (during reset and after reset) to IO internal pull (up or down) enabled. Otherwise, the pins are initialed to pull disabled
- Schmitt: The IO cell is Schmitt trigger input.

2 All GPIO shared pins are reset to GPIO input.

3 Electrical Specifications

3.1 Absolute Maximum Ratings

The absolute maximum ratings for the processors are listed in Table 3-1. Do not exceed these parameters or the part may be damaged permanently. Operation at absolute maximum ratings is not guaranteed.

Table 3-1 Absolute Maximum Ratings

Parameter	Min	Max	Unit
Storage Temperature	-65	150	°C
Operation Temperature	-40	125	°C
VDDMEM DDR PHY and SDRAM power supplies voltage	-0.5	1.98	V
VDDIO power supplies voltage	-0.5	3.6	V
VDDIO_D power supplies voltage	-0.5	3.6	V
VDD power supplies voltage	-0.2	1.21	V
PLL_AVDD power supplies voltage	-0.2	1.21	V
PLL_AVDDHV power supplied voltage	-0.5	3.6	V
EFUSE_AVDD power supplies voltage	-0.5	2.75	V
USB_VCCA3P3 power supplies voltage	-0.5	3.63	V
ADC_AVDD power supplies voltage	-0.5	3.63	V
CODEC_AVDD power supplies voltage	-0.5	3.63	V
MIPI_AVDD power supplies voltage	-0.1	2.75	V
Maximum ESD stress voltage, Human Body Model; Any pin to any supply pin, either polarity, or Any pin to all non-supply pins together, either polarity. Three stresses maximum.	-	2000	V

3.2 Recommended operating conditions

Table 3-2 Recommended operating conditions for power supplies

Symbol	Description	Min	Typical	Max	Unit
VDDMEM	VDDMEM voltage for SSTL18 (DDR2)	1.7	1.8	1.9	V
VDDIO	VDDIO voltage	3	3.3	3.6	V
VDDIO_D	VDDIO_D voltage	1.62	1.8	3.6	V
VDD	VDD core voltage	0.99	1.1	1.21	V
PLL_AVDD	AVDPLL analog voltage	1.08	1.1	1.21	V
PLL_AVDDHV	AVDPLL analog IO voltage	1.62	1.8	3.63	V
EFUSE_AVDD	AVDEFUSE voltage	2.25	2.5	2.75	V
USB_VCCA3P3	AVDUSB33 voltage	3.0	3.3	3.6	V

ADC_AVDD	AVDAD voltage	3.0	3.3	3.6	V
CODEC_AVDD	CODEC_AVDD voltage	2.97	3.3	3.63	V
MIPI_AVDD	MIPI voltage	2.25	2.5	2.75	V

Table 3-3 Recommended operating conditions for VDDIO/VDDIO_D supplied pins

Symbol	Parameter	Min	Typical	Max	Unit
V_{IH18}	Input high voltage for 1.8V I/O application	1.17		3.6	V
V_{IL18}	Input low voltage for 1.8V I/O application	–0.3		0.63	V
V_{IH25}	Input high voltage for 2.5V I/O application	1.7		3.6	V
V_{IL25}	Input low voltage for 2.5V I/O application	–0.3		0.7	V
V_{IH33}	Input high voltage for 3.3V I/O application	2		3.6	V
V_{IL33}	Input low voltage for 3.3V I/O application	–0.3		0.8	V

Table 3-4 Recommended operating conditions for others

Symbol	Description	Min	Typical	Max	Unit
T_A	Ambient temperature	–20		85	°C

Table 3-5 Recommended operating conditions for ADC pins

Symbol	Description	Min	Typical	Max	Unit
V_{IADC}	ADC_AIN0/ADC_AIN1 input voltage range	0		AVD_{AD}	V

3.3 DC Specifications

The DC characteristics for each pin include input-sense levels and output-drive levels and currents. These parameters can be used to determine maximum DC loading, and also to determine maximum transition times for a given load. All DC specification values are valid for the entire temperature range of the device.

Table 3-6 DC characteristics for V_{REFMEM} and V_{TT}

Symbol	Parameter	Min	Typical	Max	Unit
VREFM	Reference voltage supply	0.49	0.5	0.51	VMEM
VTT	Terminal Voltage	VREFM – 0.4	VREFM	VREFM + 0.4	V

Table 3-7 DC characteristics for VDDIO_D supplied pins for 1.8V application

Symbol	Parameter	Min	Typical	Max	Unit
V_T	Threshold point	0.77	0.84	0.92	V
V_{T+}	Schmitt trig low to high threshold point	0.99	1.1	1.19	V
V_{T-}	Schmitt trig high to low threshold point	0.62	0.73	0.82	V

V_{TPU}	Threshold point with pull-up resistor enabled		0.77	0.84	0.91	V
V_{TPD}	Threshold point with pull-down resistor enabled		0.77	0.85	0.92	V
V_{TPU+}	Schmitt trig low to high threshold point with pull-up resistor enabled		0.99	1.1	1.19	V
V_{TPU-}	Schmitt trig high to low threshold point with pull-down resistor enabled		0.62	0.73	0.81	V
V_{TPD+}	Schmitt trig low to high threshold point with pull-down resistor enabled		0.99	1.1	1.2	V
V_{TPD-}	Schmitt trig high to low threshold point with pull-up resistor enabled		0.62	0.73	0.82	V
I_L	Input Leakage Current @ V_I=1.8V or 0V				±10	μA
I_{OZ}	Tri-State output leakage current @ V_I=1.8V or 0V				±10	μA
R_{PU}	Pull-up Resistor		79	129	218	kΩ
R_{PD}	Pull-down Resistor		73	127	233	kΩ
V_{OL}	Output low voltage				0.45	V
V_{OH}	Output high voltage		1.35			V
I_{OL}	Low level output current @ V_{OL}(max)	8mA	6.9	12.5	20.1	mA
		16mA	11.5	20.8	33.5	mA
I_{OH}	High level output current @ V_{OH}(min)	8mA	4.9	11.6	22.6	mA
		16mA	8.4	19.9	38.8	mA

Table 3-8 DC characteristics for VDDIO_D supplied pins for 2.5V application

Symbol	Parameter	Min	Typical	Max	Unit
V_T	Threshold point	1.03	1.13	1.23	V
V_{T+}	Schmitt trig low to high threshold point	1.32	1.45	1.56	V
V_{T-}	Schmitt trig high to low threshold point	0.92	1.01	1.12	V
V_{TPU}	Threshold point with pull-up resistor enabled	1.03	1.13	1.23	V
V_{TPD}	Threshold point with pull-down resistor enabled	1.05	1.14	1.23	V
V_{TPU+}	Schmitt trig low to high threshold point with pull-up resistor enabled	1.32	1.45	1.55	V
V_{TPU-}	Schmitt trig high to low threshold point with pull-down resistor enabled	0.91	1	1.12	V
V_{TPD+}	Schmitt trig low to high threshold point with pull-down resistor enabled	1.33	1.46	1.56	V
V_{TPD-}	Schmitt trig high to low threshold point with pull-up resistor enabled	0.92	1.01	1.13	V
I_L	Input Leakage Current @ V_I=1.8V or 0V			±10	μA
I_{OZ}	Tri-State output leakage current @ V_I=1.8V or 0V			±10	μA
R_{PU}	Pull-up Resistor	53	82	132	kΩ
R_{PD}	Pull-down Resistor	51	82	143	kΩ

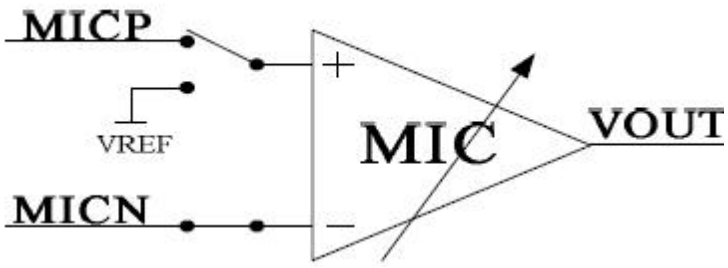
V_{OL}	Output low voltage				0.7	V
V_{OH}	Output high voltage		1.7			V
I_{OL}	Low level output current @ V_{OL}(max)	8mA	15.1	25.3	37.3	mA
		16mA	25.1	42.2	62.2	mA
I_{OH}	High level output current @ V_{OH}(min)	8mA	13.3	26.6	46.4	mA
		16mA	22.8	45.7	79.6	mA

Table 3-9 DC characteristics for VDDIO/VDDIO_D supplied pins for 3.3V application

Symbol	Parameter		Min	Typical	Max	Unit
V_T	Threshold point		1.34	1.46	1.6	V
V_{T+}	Schmitt trig low to high threshold point		1.69	1.83	1.96	V
V_{T-}	Schmitt trig high to low threshold point		1.21	1.32	1.46	V
V_{TPU}	Threshold point with pull-up resistor enabled		1.33	1.44	1.59	V
V_{TPD}	Threshold point with pull-down resistor enabled		1.36	1.47	1.6	V
V_{TPU+}	Schmitt trig low to high threshold point with pull-up resistor enabled		1.69	1.82	1.94	V
V_{TPU-}	Schmitt trig high to low threshold point with pull-down resistor enabled		1.2	1.31	1.45	V
V_{TPD+}	Schmitt trig low to high threshold point with pull-down resistor enabled		1.71	1.84	1.97	V
V_{TPD-}	Schmitt trig high to low threshold point with pull-up resistor enabled		1.23	1.33	1.46	V
I_L	Input Leakage Current @ V_I=1.8V or 0V				±10	μA
I_{OZ}	Tri-State output leakage current @ V_I=1.8V or 0V				±10	μA
R_{PU}	Pull-up Resistor		41	60	92	kΩ
R_{PD}	Pull-down Resistor		43	64	104	kΩ
V_{OL}	Output low voltage				0.4	V
V_{OH}	Output high voltage		2.4			V
I_{OL}	Low level output current @ V_{OL}(max)	8mA	13.1	20.2	27.4	mA
		16mA	21.9	33.8	45.7	mA
I_{OH}	High level output current @ V_{OH}(min)	8mA	19.3	38.2	64.5	mA
		16mA	33.1	65.4	110.5	mA

3.4 Audio codec

3.4.1 Microphone input



There are two microphone input channels, MICR and MICN. They can be configured as either single-ended input or differential inputs by the microphone PGA(MIC).

In single-ended mode., MICN is input to MIC, respectively. In differential mode, MICP is also input to MIC to form a differential input pair with MICN.

Microphone PGA has two gains to amplify the input signal, that is, 0dB and +20dB.

3.4.2 ALC

Automatic Level Control (ALC) function is included to adjust the signal level, which is input into ADC. ALC will measure the signal magnitude and compare it to defined threshold. Then it will adjust the ALC controlled PAG (ALC) gain according to the comparison result.

The programmable gain range of ALC controlled PAG is from -18dB to +28.5dB. The tuning step is 1.5dB.

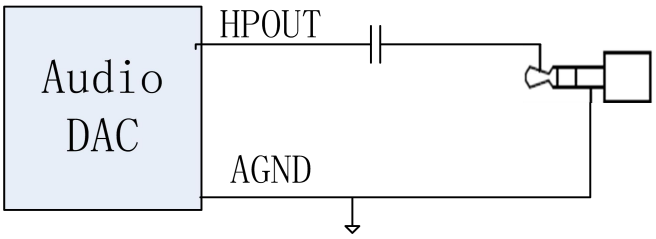
3.4.3 Headphone output

DAC output can drive 16 Ohm or 32 Ohm headphone load through DC-blocking capacitor.

In the configuration using DC-blocking capacitor, shown in following figure, the headphone ground is connected to the real ground. The capacitance and the load resistance determine the lower cut-off frequency. For instance, if 16 Ohm headphone and 100uF DC-blocking capacitor are used, the lower cut-off frequency is

$$f = \frac{1}{2\pi RC} = \frac{1}{2\pi \times 16 \times 100 \times 10^{-6}} = 99.5Hz$$

The DC-blocking capacitor can be increased to lower the cut-off frequency for better bass response.



The headphone driver chooses DAC output as input. It has a gain rang from -39dB to +6dB with a tuning step of 1.5dB..

3.5 Power On, Reset and BOOT

3.5.1 Power-On Timing

The external voltage regulator and other power-on devices must provide the X1520 processor with a specific sequence of power and resets to ensure proper operation. Figure 3-1 shows this sequence and Table 3-10 gives the timing parameters. Following are the name of the power.

- AVDAUD: CODEC_AVDD
- VDD11: all 1.1V power supplies, include VDD, PLL_AVDD
- VDDIO: all other digital IO, include DDR power supplies: VDDMEM, VDDIO, VDDIO_D
- AVD: all other analog power supplies: ADC_AVDD, USB_VCCA3P3, MIPI_AVDD, PLL_AVDDHV
- EFUSE_AVDD

Table 3-10 Power-On Timing Parameters

Symbol	Parameter	Min	Max	Unit
t_{R_VDDIO}	VDDIO rise time[1]	0	5	ms
t_{R_VDD11}	VDD11 rise time[1]	0	5	ms
t_{D_VDD11}	Delay between VDDIO arriving 50% (or 90%) to VDD11 arriving 50% (or 90%)	–1	1	ms
t_{R_AVDAUD}	AVDAUD rise time[1]	0	5	ms
t_{D_AVDAUD}	Delay between VDD11 arriving 50% (or 90%) to AVDAUD arriving 50% (or 90%)	0	1	ms
t_{R_AVD}	AVD rise time[1]	0	5	ms
t_{D_AVDA}	Delay between VDDIO arriving 50% to AVD arriving 50%	-1	1	ms
$t_{D\_PPRST\_}$	Delay between VDDAUD stable and PPRST_ deasserted	TBD[3]	–	ms[2]
$t_{D\_VPEFUSE}$	Delay between PPRST_ finished and E-fuse programming power apply	0	–	ms

NOTES:

- The power rise time is defined as 10% to 90%.

- The PPRST_ must be kept at least 100us. After PPRST_ is deasserted, the corresponding chip reset will be extended at least 40ms.
- It must make sure the EXCLK is stable and all power(except AVDEFUSE) is stable.

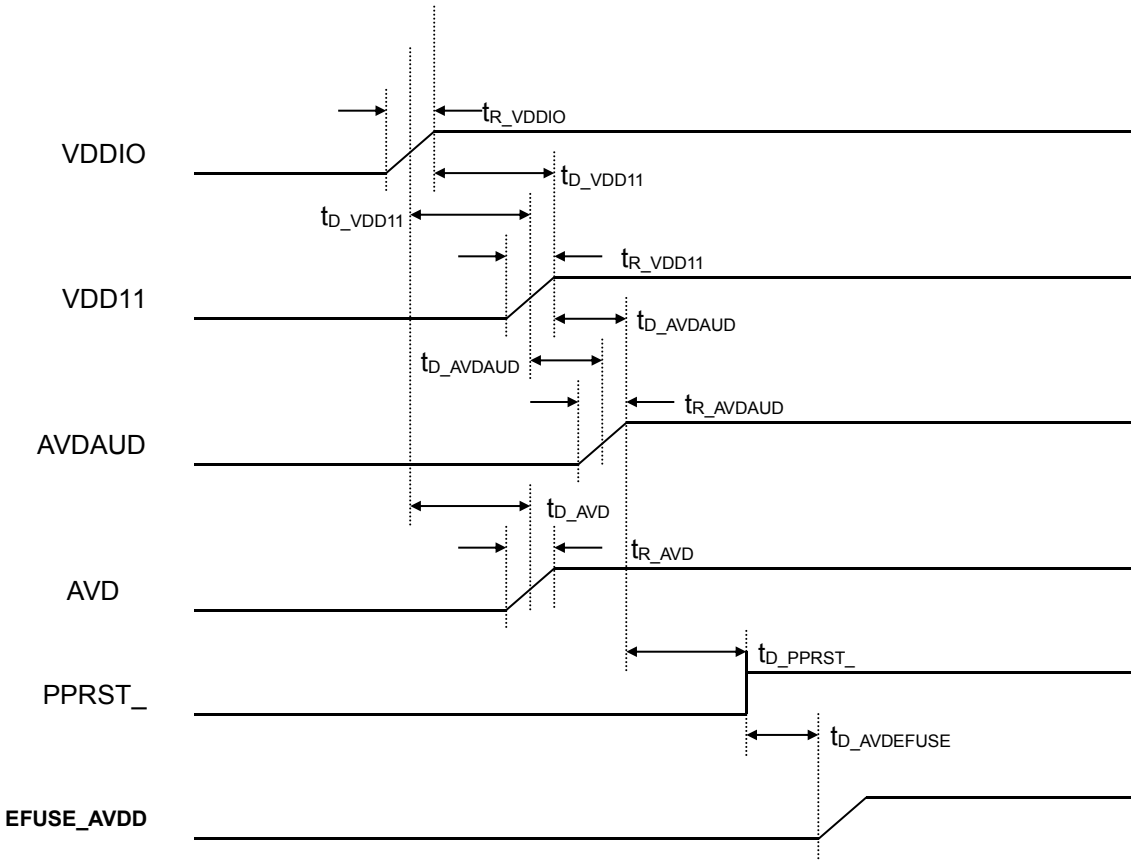


Figure 3-1 Power-On Timing Diagram

3.5.2 Reset procedure

There 2 reset sources: 1 PPRST_ pin reset; 2 WDT timeout reset. After reset, program start from boot.

- PPRST_ pin reset.
  This reset is trigged when PPRST_ pin is put to logic 0. It happens in power on RTC power and RESET-KEY pressed to reset the chip from unknown dead state. The reset end time is about 1M EXCLK cycles after rising edge of PPRST_.
- WDT reset.
  This reset happens in case of WDT timeout. The reset keeps for about a few RTCLK cycles.

After reset, all GPIO shared pins are put to GPIO input function and most of their internal pull-up/down resistor are set to on, see “2.5Pin Description [1][2]” for details. 1. The oscillators are on. The USB 2.0 OTG PHY and USB 1.1 PHY, the audio CODEC DAC/ADC, the SAR-ADCs is put in suspend mode.

3.5.3 BOOT

The boot sequence of the X1520 is controlled by boot_sel1. The configuration is shown as follow:

Table 3-11 Boot Configuration of X1520

boot_sel1	Boot method
0	SFC boot @ CS4 (SPI boot)
1	USB boot @ USB 2.0 device, EXTCLK=24MHz

The boot procedure is showed in the following flow chart:

As shown in Figure 3-2 boot sequence Block Diagram, after reset, the boot program on the internal boot ROM executes as follows:

1 Disable all interrupts and read boot_sel1 to determine the boot method.

2 There 26KB backup reading failed, the 26KB backup at 128th, 256th , …, and finally 1024th page will be tried in consecutive order.

3 If it is boot from USB, a block of code will be received through USB cable connected with host PC and be stored in cache. Then branch to this area in cache.

4 If it is boot from SPI nor/nand at SFC, its function pins SFC_CLK,SFC_CE, SFC_DR,SFC_DT, SFC_WP,SFC_HOLD are initialized,the boot program loads the 12kB code from SPI NAND/NOR flash to cache and jump to it.

When SFC boot start failure, the program in bootrom will go into USB boot.

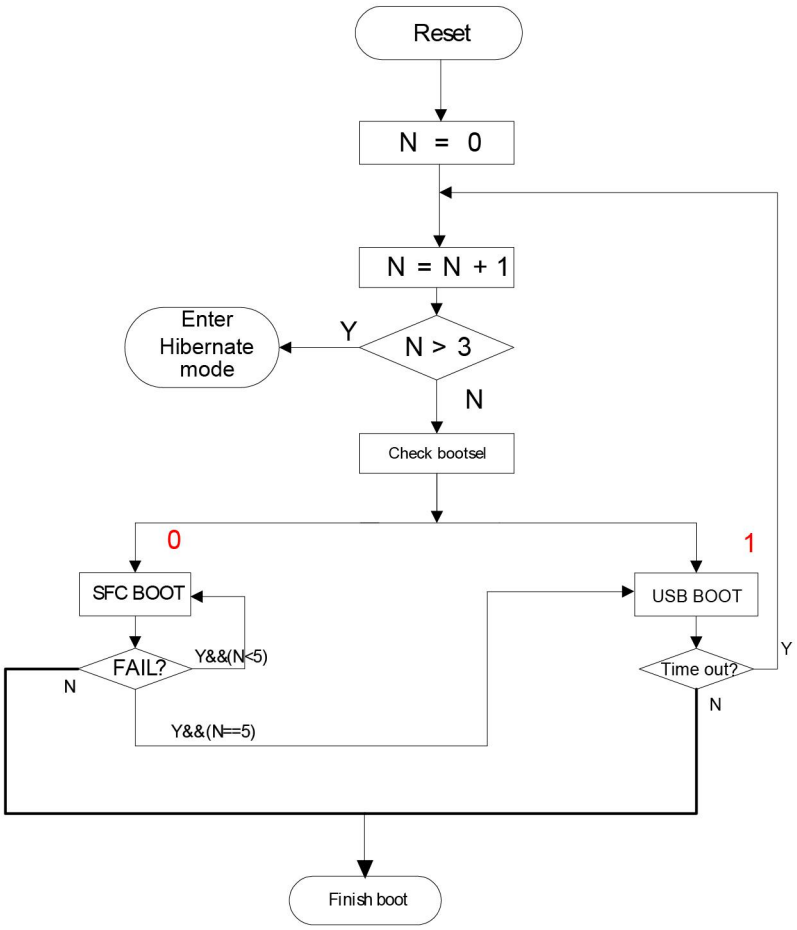


Figure 3-2 Boot sequence diagram of X1520