Ingenic®

X2670 AIoT Application Processor

Data Sheet

Revision:2.0

Date:Aug.2023

北京君正集成电路股份有限公司
Ingenic Semiconductor Co.,Ltd.

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Release history

Date	Revision	Change
Aug.2023	2.0	Modify RISC-V D-Cache and I-Cache size Add DDR3L VDDMEM
May.2023	1.0	First release

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1 Overview

X2670 is a low power consumption, high performance and high integrated application processor featuring a Xburst® 2 Dual-Core and a RISC-V Core. Based on Xburst® 2 dual-core, it integrates H264 decoder, JPEG Codec, 2D graphics engine, RGB/MIPI-DSI/LVDS display, security system and other usefull peripherals.

For more quickly and easily to use X2670, DDR KGD is integrated on chip.

NAME	SIP DDR	VDDMEM(V)
X2670M	64MB DDR2	1.8
X2670	128MB DDR3(L)	1.5/1.35

1.1 Block Diagram

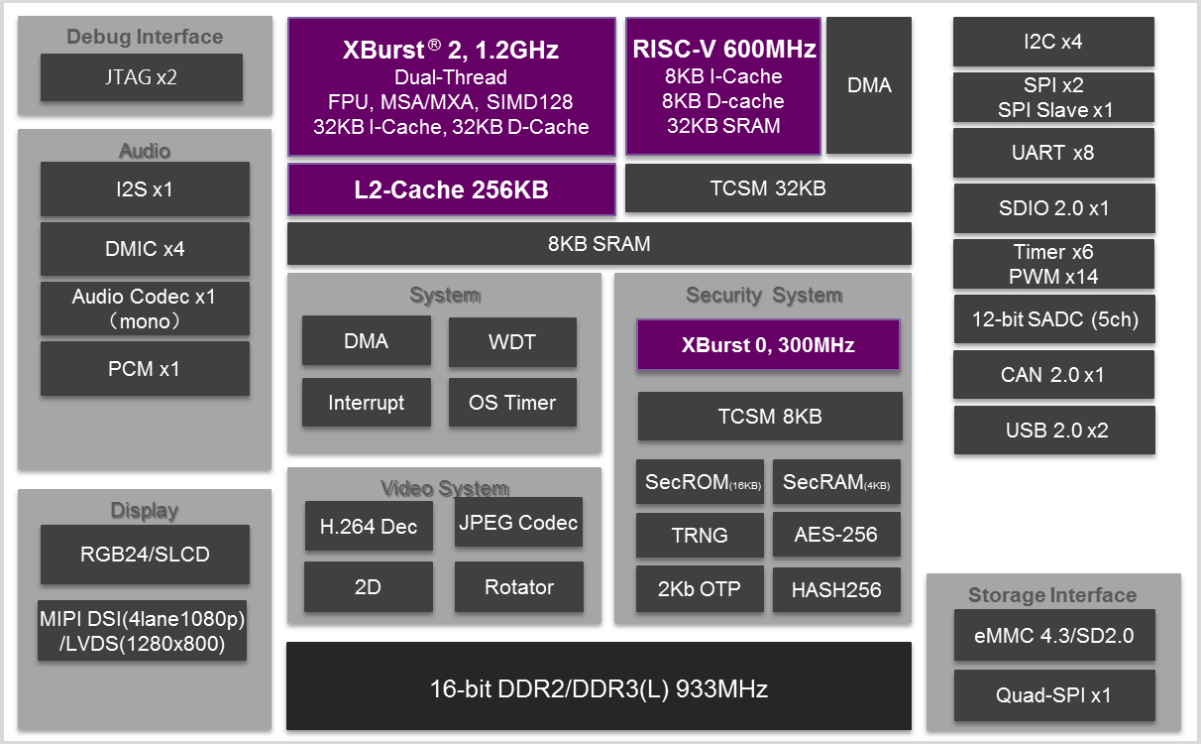


Figure 1-1 X2670 Diagram

1.2 Features

1.2.1 CPU

- XBurst® 2, Signal Core, Dual-thread, 1.2Ghz
  - 32KB L1 I-Cache, 32KB L1 D-Cache, 256 KB L2-Cache, 8KB SRAM
  - High-performance Floating-point Unit and SIMD Engine: FSE
    - ◆ 32 x 128-bit register set, 128-bit loads/stores to/from SIMD unit
    - ◆ IEEE-754 2008 compliant
  - MIPS32 ISA R2 plus MIPS SIMD instruction set architecture:128bit MSA
  - Ingenic SIMD instruction set architecture: 128bit MXA
  - Support JTAG

- RISC-V(LEP) 600Mhz
  - 8KB L1 D-cache +8K L1 I-cache, 32KB SRAM
  - Support JTAG

1.2.2 Memory Interface

- DDR2/DDR3(L) inside

1.2.3 Video Process

- H.264 Decoder
  - Maximum resolution: 2560x2048
  - Decoding capabilities: 1920x1080@60fps
  - Output data format: NV12
- JPEG Decoder
  - Baseline DCT decoder according to JPEG ITU-T T.81 | ISO/IEC 10918-1 standard
  - Unlimited image size (specification up to 64Kx64K)
  - Decoding capabilities: 1920x1080@160fps(ARGB)
  - Input data format：ARGB, NV12, NV21, YUV422, RGB888, YUV444
- JPEG Encoder
  - Baseline DCT compression according to JPEG ITU-T T.81 | ISO/IEC 10918-1.
  - Unlimited image size (specification up to 64Kx64K)
  - Encoding capabilities：1920x1080@110fps(4:2:0 subsampling)
  - Output data format：ARGB, NV12, NV21, YUV422, RGB888, YUV444
- 2D Graphics Engine
  - LineDraw
  - Rectangle Fill
  - BitBLt
  - Color Space Conversion
  - Clipping
  - Alpha Blending
  - Rotation
  - Mirror
  - Scale

1.2.4 Display & Camera

- Display Controller
  - input：ARGB8888, RGB565, RGB555, ARGB1555, NV12, NV21, YUV422
  - output
    - ◆ MIPI DSI interface
      - Support 2-lane, 4-lane
      - 1.5Gbps maximum data transfer rate per lane
      - Capabilities: 1920x1080@60Hz, 24BPP
    - ◆ LVDS interface

        - Single channel 8 bit
        - Display size up to 1280x800@60Hz, 24BPP
    - RGB interface
        - Support 24bit/pixel(R:8bit, G:8bit, B:8bit)
        - Support 18bit/pixel(R:6bit, G:6bit, B:6bit)
        - Support 16bit/pixel(R:5bit, G:6bit, B:5bit)
        - Capabilities: 1280x720@60Hz, 24BPP
    - 60/80-Type MCU Interface
        - Support 6800, 8080
        - Support 8/9/16/18/24-bit bus
        - Capabilities: 640x480@60Hz, 24BPP
    - 3/4 wire SPI interface
        - Support Serial data transfer interface, 3/4line-spi
        - Support 8/12/16/24-bit bus
- Maximum resolution: 2047x2047

1.2.5 Audio

- AIC Controller
    - Sample bit support: 24, 20, 18, 16 and 8 bit
    - Sample rate support: 8, 12, 16, 32, 44.1, 48, 96 Khz
    - Support I2S and MSB-Justified format
    - Support Master and Slave mode
- PCM Controller
    - Sample bit support: 16 and 8 bit
    - Sample rate support: 8, 12, 16, 32, 44.1, 48, 96 Khz
    - Support Master and Slave mode
- Internal Audio Codec
    - 24bit DAC with 90db SNR
    - 24bit ADC with 90db SNR
    - Sample bit support: 16, 20 and 24 bit
    - Sample rate support: 8, 12, 16, 32, 44.1, 48, 96 Khz
    - Automatic Level Control (ALC) for smooth audio recording
    - Mono Differential input/output
    - Support loopback
- DMIC Controller
    - Support 1/2/3/4 channel digital MIC
    - SNR: 90dB, THD: -90dB @ FS-20dB
    - Sample bit support: 16 and 24 bit
    - Sample rate support: 8, 12, 16, 48, 96 Khz
    - Support DMIC clock frequency 2.4MHz and 3.072MHz
    - Support enable DMIC and AIC at the same time

1.2.6 System Functions

- WatchDog0/1
  - WDT0 generate full reset signal
  - WDT1 generate full interrupt
  - Each WDT has a half interrupt
  - Only EXCLK/512 can be used as the clock for counter
- OS timer
  - One 64bit global timer for system time
  - One 32bit event timer for one logical core
  - Only EXCLK can be used as the clock for counter
- Power On Reset(POR)
  - Monitor 1.8V supply for PLL and 0.9V for core

1.2.7 Security System

- XBurst® 0 MIPS-Based, 300Mhz
- 16KB Secret ROM
- 4KB Secret RAM
- True Random Number Generator
- MD5, SHA, SHA2
- AES 256/192/128-bit key size
- 2Kb OTP(EFUSE)
- Support secure boot

1.2.8 Storage Interface

- High Speed Synchronous serial interfaces (SFC)
  - SPI protocol support: Standard, Dual, Quad SPI
  - 7 transfer formats：Standard SPI, Dual-Input/Dual-Output SPI, Dual-I/O SPI, Full Dual I/O SPI, Quad-Input/Quad-Output SPI, Quad I/O SPI, Full Quad I/O SPI
  - Maximum IO clock frequency of 80MHz
- SD/MMC/SDIO interface(MSC0/1)
  - Support SD 2.0/eMMC 4.3/SDIO 2.0
  - Support 1/4bit
  - Maximum IO clock frequency of 50Mhz

1.2.9 Peripherals

- General-Purpose I/O ports
  - Each port can be configured as an input, an output or an alternate function port
  - Each port can be configured as an interrupt source triggered by high/low level or rising / falling edge or dual edge
  - Support shadow
- I2C x4
  - Three speeds：

  - ◆ Standard Mode(100Kb/s)
  - ◆ Fast Mode(400Kb/s)
  - ◆ High Mode(3.4Mb/s)
- Master or slave I2C operation
- 7/10-bit addressing

- SPI x2, SPI Slave x1
  - 3 protocols support: National's Microwire, TI's SSP, and Motorola's SPI
  - Full-duplex or transmit-only or receive-only operation
  - Programmable transfer order: MSB first or LSB first
- UART x8
  - 5-, 6-, 7- or 8-bit characters
  - no parity or even or odd parity
  - 1, 1½, or 2 stop bits
  - Supports modem flow control by software or hardware
  - Slow infrared asynchronous interface that conforms to IrDA1.1 specification
  - Maximum 3M baud rate
  - Support DMA mode
- TCU x2
  - 8 channels each channel has two pins
  - Support posedge / negedge / dualedge clock counting
  - Support gate counting(only count for gating signal)
  - Support direction counting(add / sub because of input signal)
  - Support quadrature counting
  - Support capture counting, output signal high-level time and total cycle time
  - Support exclk / gpio two clock source
- PWM x1
  - 14 channels, output signal ~50MHz, signal precision ~500MHz
  - Cpu / dma mode to update config
- TPC x1
  - One print head control unit, SFT_CLKx1, SFT_DATAx8, LAT_x1, DSTx8
  - Support one 8-channel stepper motor control unit, or two 4-channel stepper motor control unit
  - Support one watchdog timer(WDT) unit
  - output signal ~50MHz, signal precision ~500MHz
- SAR A/D Converter x1
  - Contains 5 input channels and outputs 12-bit conversion data. Up to 2MS/s sampling rate.
  - DNL < 1.5LSB, INL < 3LSB
  - Support three conversion sequences.
  - Support two conversion modes：
    - ◆ Scan conversion mode: Convert multiple analog channels one by one, and the delay time can be configured.
    - ◆ Continuous conversion mode:The sequence restarts automatically after all conversions are completed, and the restart interval can be configured.

- Support three trigger modes: Register trigger, TCU trigger and GPIO trigger.
- Setting the priority of the conversion sequences according to requirements can adjust the preemption strategy.
- Support analog watchdog, interrupt is set if the analog voltage converted is below a low threshold or above a high threshold.
- Support DMA transfers.

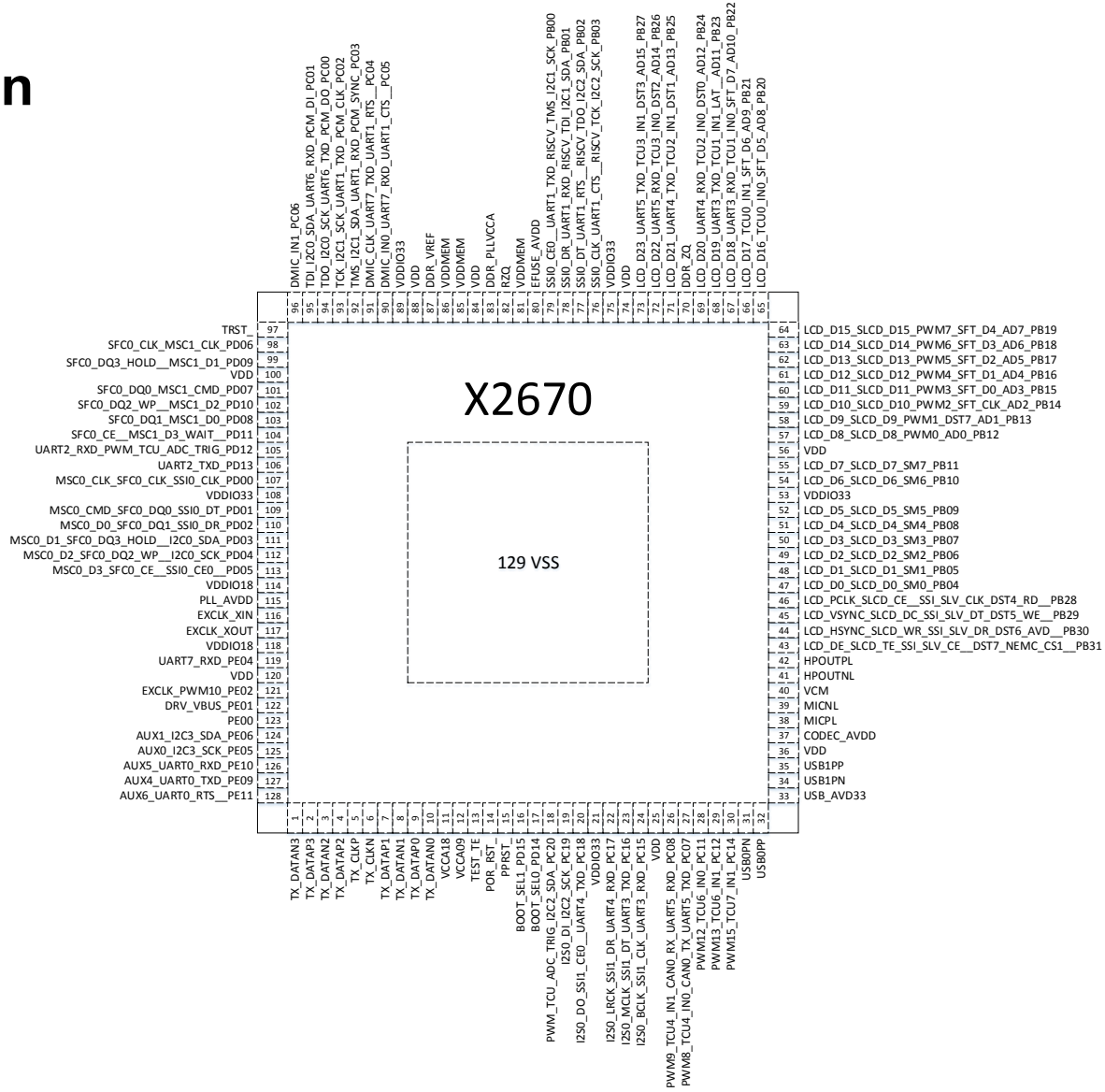
- CAN2.0 x1
  - Support CAN 2.0B protocol in ISO-11898-1:2003
  - Arbitration Bit Rate up to 1Mbps
  - Support DMA transfers
- USB2.0 x2
  - Do not support OTG, but support Device/Host by configuration
  - Fully compliant with USB specifications Rev2.0
    - high-spped(480Mbps)
    - full-speed(12Mbps)
    - low-speed (1.5Mbps)host only
  - soft connect/disconnect
  - 16 Endpoints
  - Supports control, interrupt, ISO and bulk transfer
  - Support wakeup, remote-wakeup

1.2.10 Bootrom

- 24KB Boot ROM

2 PAD Information

2.1 Pin Map



2.2 Pin Description

2.2.1 GPIO Group B

Ball No.	Ball Name	DS	Pull	Slew Rate	Schmitt	GPIO	Func0	Func1	Func2	Func3	Power
79	SSI0_CE0__UART1_TXD_RISCV_TMS_I2C1_SCK_PB00	8mA	Hiz	fast	No	GPB [0]	SSI0_CE0_	UART1_TXD	RISCV_TMS	I2C1_SCK	VDDIO33
78	SSI0_DR_UART1_RXD_RISCV_TDI_I2C1_SDA_PB01	8mA	Hiz	fast	No	GPB [1]	SSI0_DR	UART1_RXD	RISCV_TDI	I2C1_SDA	VDDIO33
77	SSI0_DT_UART1_RTS__RISCV_TDO_I2C2_SDA_PB02	8mA	Hiz	fast	No	GPB [2]	SSI0_DT	UART1_RTS_	RISCV_TDO	I2C2_SDA	VDDIO33
76	SSI0_CLK_UART1_CTS__RISCV_TCK_I2C2_SCK_PB03	8mA	Hiz	fast	No	GPB [3]	SSI0_CLK	UART1_CTS_	RISCV_TCK	I2C2_SCK	VDDIO33
47	LCD_D0_SLCD_D0_SM0_PB04	8mA	Hiz	fast	No	GPB [4]	LCD_D0	SLCD_D0		SM0	VDDIO33
48	LCD_D1_SLCD_D1_SM1_PB05	8mA	Hiz	fast	No	GPB [5]	LCD_D1	SLCD_D1		SM1	VDDIO33
49	LCD_D2_SLCD_D2_SM2_PB06	8mA	Hiz	fast	No	GPB [6]	LCD_D2	SLCD_D2		SM2	VDDIO33
50	LCD_D3_SLCD_D3_SM3_PB07	8mA	Hiz	fast	No	GPB [7]	LCD_D3	SLCD_D3		SM3	VDDIO33
51	LCD_D4_SLCD_D4_SM4_PB08	8mA	Hiz	fast	No	GPB [8]	LCD_D4	SLCD_D4		SM4	VDDIO33
52	LCD_D5_SLCD_D5_SM5_PB09	8mA	Hiz	fast	No	GPB [9]	LCD_D5	SLCD_D5		SM5	VDDIO33
54	LCD_D6_SLCD_D6_SM6_PB10	8mA	Hiz	fast	No	GPB [10]	LCD_D6	SLCD_D6		SM6	VDDIO33
55	LCD_D7_SLCD_D7_SM7_PB11	8mA	Hiz	fast	No	GPB [11]	LCD_D7	SLCD_D7		SM7	VDDIO33
57	LCD_D8_SLCD_D8_PWM0_AD0_PB12	8mA	Hiz	fast	No	GPB [12]	LCD_D8	SLCD_D8	PWM0	AD0	VDDIO33
58	LCD_D9_SLCD_D9_PWM1_DST7_AD1_PB13	8mA	Hiz	fast	No	GPB [13]	LCD_D9	SLCD_D9	PWM1	DST7/AD1	VDDIO33
59	LCD_D10_SLCD_D10_PWM2_SFT_CLK_AD2_PB14	8mA	Hiz	fast	No	GPB [14]	LCD_D10	SLCD_D10	PWM2	SFT_CLK/AD2	VDDIO33
60	LCD_D11_SLCD_D11_PWM3_SFT_D0_AD3_PB15	8mA	Hiz	fast	No	GPB [15]	LCD_D11	SLCD_D11	PWM3	SFT_D0/AD3	VDDIO33
61	LCD_D12_SLCD_D12_PWM4_SFT_D1_AD4_PB16	8mA	Hiz	fast	No	GPB [16]	LCD_D12	SLCD_D12	PWM4	SFT_D1/AD4	VDDIO33

62	LCD_D13_SLCD_D13_PWM5_SFT_D2_AD5_PB17	8mA	Hiz	fast	No	GPB [17]	LCD_D13	SLCD_D13	PWM5	SFT_D2/AD5	VDDIO33
63	LCD_D14_SLCD_D14_PWM6_SFT_D3_AD6_PB18	8mA	Hiz	fast	No	GPB [18]	LCD_D14	SLCD_D14	PWM6	SFT_D3/AD6	VDDIO33
64	LCD_D15_SLCD_D15_PWM7_SFT_D4_AD7_PB19	8mA	Hiz	fast	No	GPB [19]	LCD_D15	SLCD_D15	PWM7	SFT_D4/AD7	VDDIO33
65	LCD_D16_TCU0_IN0_SFT_D5_AD8_PB20	8mA	Hiz	fast	No	GPB [20]	LCD_D16	SLCD_RD	TCU0_IN0	SFT_D5/AD8	VDDIO33
66	LCD_D17_TCU0_IN1_SFT_D6_AD9_PB21	8mA	Hiz	fast	No	GPB [21]	LCD_D17		TCU0_IN1	SFT_D6/AD9	VDDIO33
67	LCD_D18_UART3_RXD_TCU1_IN0_SFT_D7_AD10_PB22	8mA	Hiz	fast	No	GPB [22]	LCD_D18	UART3_RXD	TCU1_IN0	SFT_D7/AD10	VDDIO33
68	LCD_D19_UART3_TXD_TCU1_IN1_LAT__AD11_PB23	8mA	Hiz	fast	No	GPB [23]	LCD_D19	UART3_TXD	TCU1_IN1	LAT_/AD11	VDDIO33
69	LCD_D20_UART4_RXD_TCU2_IN0_DST0_AD12_PB24	8mA	Hiz	fast	No	GPB [24]	LCD_D20	UART4_RXD	TCU2_IN0	DST0/AD12	VDDIO33
71	LCD_D21_UART4_TXD_TCU2_IN1_DST1_AD13_PB25	8mA	Hiz	fast	No	GPB [25]	LCD_D21	UART4_TXD	TCU2_IN1	DST1/AD13	VDDIO33
72	LCD_D22_UART5_RXD_TCU3_IN0_DST2_AD14_PB26	8mA	Hiz	fast	No	GPB [26]	LCD_D22	UART5_RXD	TCU3_IN0	DST2/AD14	VDDIO33
73	LCD_D23_UART5_TXD_TCU3_IN1_DST3_AD15_PB27	8mA	Hiz	fast	No	GPB [27]	LCD_D23	UART5_TXD	TCU3_IN1	DST3/AD15	VDDIO33
46	LCD_PCLK_SLCD_CE__SSI_SLV_CLK_DST4_RD__PB28	8mA	Hiz	fast	No	GPB [28]	LCD_PCLK	SLCD_CE_	SSI_SLV_CLK	DST4/RD_	VDDIO33
45	LCD_VSYNC_SLCD_DC_SSI_SLV_DT_DST5_WE__PB29	8mA	Hiz	fast	No	GPB [29]	LCD_VSYNC	SLCD_DC	SSI_SLV_DT	DST5/WE_	VDDIO33
44	LCD_HSYNC_SLCD_WR_SSI_SLV_DR_DST6_AVD__PB30	8mA	Hiz	fast	No	GPB [30]	LCD_HSYNC	SLCD_WR	SSI_SLV_DR	DST6/AVD_	VDDIO33
43	LCD_DE_SLCD_TE_SSI_SLV_CE__DST7_NEMC_CS1__PB31	8mA	Hiz	fast	No	GPB [31]	LCD_DE	SLCD_TE	SSI_SLV_CE_	DST7/NEMC_CS1_	VDDIO33

2.2.2 GPIO Group C

Ball No.	Ball Name	DS	Pull	Slew Rate	Sch mitt	GPIO	Func0	Func1	Func2	Func3	Power
94	TDO_I2C0_SCK_UART6_TXD_PCM_DO_PC00	8mA	Hiz	fast	No	GPC [0]	TDO	I2C0_SCK	UART6_TXD	PCM_DO	VDDIO33
95	TDI_I2C0_SDA_UART6_RXD_PCM_DI_PC01	8mA	PU	fast	No	GPC [1]	TDI	I2C0_SDA	UART6_RXD	PCM_DI	VDDIO33
93	TCK_I2C1_SCK_UART1_TXD_PCM_CLK_PC02	8mA	PU	fast	No	GPC [2]	TCK	I2C1_SCK	UART1_TXD	PCM_CLK	VDDIO33
92	TMS_I2C1_SDA_UART1_RXD_PCM_SYNC_PC03	8mA	PU	fast	No	GPC [3]	TMS	I2C1_SDA	UART1_RXD	PCM_SYNC	VDDIO33
91	DMIC_CLK_UART7_TXD_UART1_RTS__PC04	8mA	Hiz	fast	No	GPC [4]	DMIC_CLK	UART7_TXD	UART1_RTS_		VDDIO33
90	DMIC_IN0_UART7_RXD_UART1_CTS__PC05	8mA	Hiz	fast	No	GPC [5]	DMIC_IN0	UART7_RXD	UART1_CTS_		VDDIO33
96	DMIC_IN1_PC06	8mA	Hiz	fast	No	GPC [6]	DMIC_IN1				VDDIO33
27	PWM8_TCU4_IN0_CAN0_TX_UART5_TXD_PC07	8mA	Hiz	fast	No	GPC [7]	PWM8	TCU4_IN0	CAN0_TX	UART5_TXD	VDDIO33
26	PWM9_TCU4_IN1_CAN0_RX_UART5_RXD_PC08	8mA	Hiz	fast	No	GPC [8]	PWM9	TCU4_IN1	CAN0_RX	UART5_RXD	VDDIO33
28	PWM12_TCU6_IN0_PC11	8mA	Hiz	fast	No	GPC [11]	PWM12	TCU6_IN0			VDDIO33
29	PWM13_TCU6_IN1_PC12	8mA	Hiz	fast	No	GPC [12]	PWM13	TCU6_IN1			VDDIO33
30	PWM15_TCU7_IN1_PC14	8mA	PD	fast	No	GPC [14]	PWM15	TCU7_IN1			VDDIO33
24	I2S0_BCLK_SSI1_CLK_UART3_RXD_PC15	8mA	Hiz	fast	No	GPC [15]		I2S0_BCLK	SSI1_CLK	UART3_RXD	VDDIO33
23	I2S0_MCLK_SSI1_DT_UART3_TXD_PC16	8mA	Hiz	fast	No	GPC [16]		I2S0_MCLK	SSI1_DT	UART3_TXD	VDDIO33
22	I2S0_LRCK_SSI1_DR_UART4_RXD_PC17	8mA	Hiz	fast	No	GPC [17]		I2S0_LRCK	SSI1_DR	UART4_RXD	VDDIO33
20	I2S0_DO_SSI1_CE0__UART4_TXD_PC18	8mA	Hiz	fast	No	GPC [18]		I2S0_DO	SSI1_CE0_	UART4_TXD	VDDIO33
19	I2S0_DI_I2C2_SCK_PC19	8mA	Hiz	fast	No	GPC [19]		I2S0_DI	I2C2_SCK		VDDIO33

18	PWM_TCU_ADC_TRIG_I2C2_SDA_PC20	8mA	Hiz	fast	No	GPC [20]		PWM_TCU_ADC_TRIG	I2C2_SDA		VDDIO33

2.2.3 GPIO Group D

Ball No.	Ball Name	DS	Pull	Slew Rate	Schmitt	GPIO	Func0	Func1	Func2	Func3	Power
107	MSC0_CLK_SFC0_CLK_SSI0_CLK_PD00	26pF	PU	fast	No	GPD [0]	MSC0_CLK	SFC0_CLK	SSI0_CLK		VDDIO33
109	MSC0_CMD_SFC0_DQ0_SSI0_DT_PD01	26pF	PU	fast	No	GPD [1]	MSC0_CMD	SFC0_DQ0	SSI0_DT		VDDIO33
110	MSC0_D0_SFC0_DQ1_SSI0_DR_PD02	26pF	PU	fast	No	GPD [2]	MSC0_D0	SFC0_DQ1	SSI0_DR		VDDIO33
111	MSC0_D1_SFC0_DQ3_HOLD__I2C0_SDA_PD03	26pF	PU	fast	No	GPD [3]	MSC0_D1	SFC0_DQ3/HOLD_	I2C0_SDA		VDDIO33
112	MSC0_D2_SFC0_DQ2_WP__I2C0_SCK_PD04	26pF	PU	fast	No	GPD [4]	MSC0_D2	SFC0_DQ2/WP_	I2C0_SCK		VDDIO33
113	MSC0_D3_SFC0_CE__SSI0_CE0__PD05	26pF	PU	fast	No	GPD [5]	MSC0_D3	SFC0_CE_	SSI0_CE0_		VDDIO33
98	SFC0_CLK_MSC1_CLK_PD06	8mA	PU	fast	No	GPD [6]	SFC0_CLK	MSC1_CLK			VDDIO33
101	SFC0_DQ0_MSC1_CMD_PD07	8mA	PU	fast	No	GPD [7]	SFC0_DQ0	MSC1_CMD			VDDIO33
103	SFC0_DQ1_MSC1_D0_PD08	8mA	PU	fast	No	GPD [8]	SFC0_DQ1	MSC1_D0			VDDIO33
99	SFC0_DQ3_HOLD__MSC1_D1_PD09	8mA	PU	fast	No	GPD [9]	SFC0_DQ3/HOLD_	MSC1_D1			VDDIO33
102	SFC0_DQ2_WP__MSC1_D2_PD10	8mA	PU	fast	No	GPD [10]	SFC0_DQ2/WP_	MSC1_D2			VDDIO33
104	SFC0_CE__MSC1_D3_WAIT__PD11	8mA	PU	fast	No	GPD [11]	SFC0_CE_	MSC1_D3		WAIT_	VDDIO33
105	UART2_RXD_PWM_TCU_ADC_TRIG_PD12	8mA	PU	fast	No	GPD [12]	UART2_RXD	PWM_TCU_ADC_TRIG			VDDIO33
106	UART2_TXD_PD13	8mA	Hiz	fast	No	GPD [13]	UART2_TXD				VDDIO33

17	BOOT_SEL0_PD14	8mA	Hiz	fast	Yes	GPD [14]	BOOT_SEL0					VDDIO33
16	BOOT_SEL1_PD15	8mA	Hiz	fast	Yes	GPD [15]	BOOT_SEL1					VDDIO33

2.2.4 GPIO Group E

Ball No.	Ball Name	DS	Pull	Slew Rate	Schmitt	GPIO	Func0	Func1	Func2	Func3	Power
123	PE00	12mA	PD	dis	No	GPE [0]					VDDIO18
122	DRV_VBUS_PE01	12mA	Hiz	dis	No	GPE [1]		DRV_VBUS			VDDIO18
121	EXCLK_PWM10_PE02	12mA	Hiz	dis	No	GPE [2]		EXCLK	PWM10		VDDIO18
119	UART7_RXD_PE04	12mA	Hiz	dis	No	GPE [4]		UART7_RXD			VDDIO18
125	AUX0_I2C3_SCK_PE05	12mA	Hiz	dis	No	GPE [5]	AUX0	I2C3_SCK			VCCA18
124	AUX1_I2C3_SDA_PE06	12mA	Hiz	dis	No	GPE [6]	AUX1	I2C3_SDA			VCCA18
127	AUX4_UART0_TXD_PE09	12mA	Hiz	dis	No	GPE [9]	AUX4	UART0_TXD			VCCA18
126	AUX5_UART0_RXD_PE10	12mA	Hiz	dis	No	GPE [10]	AUX5	UART0_RXD			VCCA18
128	AUX6_UART0_RTS__PE11	12mA	Hiz	dis	No	GPE [11]	AUX6	UART0_RTS			VCCA18

2.3 Analog PAD Description

Ball No.	Pin Names	IO	Power	Pin Description
Memory				
83	DDRPLL_VCCA	P	-	DDR PHY PLL Supply 1.8V
82	RZQ	I	VDDMEM	For DDR, external reference resistor for output calibrating
70	DDR_ZQ	I	VDDMEM	For DDR, external reference resistor for output calibrating
87	DDR_VREF	P	-	Reference voltage supply of DDR , typical 0.5*VDDMEM
Power and Ground				
129	VSS	P		Ground

81	VDDMEM	P	-	DDR PHY IO Supply, 1.5V for DDR3, 1.35 for DDR3L, 1.8V for DDR2
85	VDDMEM	P	-	DDR PHY IO Supply, 1.5V for DDR3, 1.35 for DDR3L, 1.8V for DDR2
86	VDDMEM	P	-	DDR PHY IO Supply, 1.5V for DDR3, 1.35 for DDR3L, 1.8V for DDR2
21	VDDIO33	P	-	IO digital power for GPIO Port B&C&D, 3.3V
53	VDDIO33	P	-	IO digital power for GPIO Port B&C&D, 3.3V
75	VDDIO33	P	-	IO digital power for GPIO Port B&C&D, 3.3V
89	VDDIO33	P	-	IO digital power for GPIO Port B&C&D, 3.3V
108	VDDIO33	P	-	IO digital power for GPIO Port B&C&D, 3.3V
114	VDDIO18	P	-	IO digital power for GPIO Port E, 1.8V
118	VDDIO18	P		IO digital power for GPIO Port E, 1.8V
25	VDD	P	-	CORE digital power, 0.9V
36	VDD	P	-	CORE digital power, 0.9V
56	VDD	P	-	CORE digital power, 0.9V
74	VDD	P	-	CORE digital power, 0.9V
84	VDD	P	-	CORE digital power, 0.9V
88	VDD	P	-	CORE digital power, 0.9V
100	VDD	P	-	CORE digital power, 0.9V
120	VDD	P	-	CORE digital power, 0.9V
11	VCCA18	P	-	Analog IO Supply 1.8V
12	VCCA09	P	-	Analog Core Supply 0.9V
DSI-TX				
10	TX_DATAN0	AIO	VCCA18	Lane0 negative end
9	TX_DATAP0	AIO	VCCA18	Lane0 positive end
8	TX_DATAN1	AI	VCCA18	Lane1 negative end
7	TX_DATAP1	AI	VCCA18	Lane1 positive end
3	TX_DATAN2	AI	VCCA18	Lane2 negative end
4	TX_DATAP2	AI	VCCA18	Lane2 positive end
1	TX_DATAN3	AI	VCCA18	Lane3 negative end
2	TX_DATAP3	AI	VCCA18	Lane3 positive end
6	TX_CLKN	AI	VCCA18	CLK lane negative end
5	TX_CLKP	AI	VCCA18	CLK lane positive end

Audio Codec				
37	CODEC_AVDD	P	-	Codec Analog Supply 1.8V
40	VCM	AO	CODEC_AVDD	Reference voltage output
38	MICPL	AI	CODEC_AVDD	ADC channel input
39	MICNL	AI	CODEC_AVDD	ADC channel input
41	HPOUTNL	AO	CODEC_AVDD	DAC channel output
42	HPOUTPL	AO	CODEC_AVDD	DAC channel output
USB OTG				
33	USB_AVD33	P	-	USB Analog Supply.3.3V
31	USB0PN	AIO	USB_AVD33	USB0 data negative
32	USB0PP	AIO	USB_AVD33	USB0 data positive
34	USB1PN	AIO	USB_AVD33	USB1 data negative
35	USB1PP	AIO	USB_AVD33	USB1 data positive
EFUSE				
80	EFUSE_AVDD	P	-	EFUSE programming power, 1.8V
SARADC				
125	AUX0	AI	VCCA18	SARADC input channel 0
124	AUX1	AI	VCCA18	SARADC input channel 1
127	AUX4	AI	VCCA18	SARADC input channel 4
126	AUX5	AI	VCCA18	SARADC input channel 5
128	AUX6	AI	VCCA18	SARADC input channel 6
CPM				
116	EXCLK_XIN	AI	VDDIO18	EXCLK OSC Input
117	EXCLK_XOUT	AO	VDDIO18	EXCLK OSC Output
115	PLL_AVDD	P	-	PLL Analog Supply 1.8V

2.4 Digital PAD Description

Ball No.	Pin Names	IO	Power	Pin Description
System Control				
15	PPRST_	I	VDDIO33	power on reset and RESET-KEY reset input
97	TRST_	I	VDDIO33	JTAG reset
13	TEST_TE	I	VDDIO33	Manufacture test enable, program readable
14	POR_RST_	O	VDDIO33	POR Reset Output

Pin Names	IO	Pin Description
LCD		
LCD_PCLK	O	LCD pixel clock
LCD_VSYNC	O	LCD frame sync
LCD_HSYNC	O	LCD line sync
LCD_DE	O	LCD data enable
LCD_D<n>	O	LCD data output bit n (0-23)
SLCD(60/80-Type MCU)		
SLCD_WR	O	Smart LCD write signal
SLCD_CE_	O	Smart LCD chip select signal
SLCD_TE	I	Smart LCD tearing effect signal
SLCD_DC	O	Smart LCD data/command select signal
SLCD_D<n>	O	Smart LCD data output bit n (0-15)
I2S		
I2S0_MCLK	O	I2S master clock output
I2S0_BCLK	IO	I2S bit clock
I2S0_LRCK	IO	I2S LR clock
I2S0_DO	O	I2S data output
I2S0_DI	I	I2S data input

DMIC		
DMIC_CLK	O	Digital MIC clock output
DMIC_IN0	I	DMIC data in for DMIC 0/1
DMIC_IN1	I	DMIC data in for DMIC 2/3
PCM		
PCM_CLK	IO	PCM clock
PCM_SYNC	IO	PCM sync
PCM_DO	O	PCM data out
PCM_DI	I	PCM data in
SFC		
SFC0_CLK	O	Serial Flash clock output
SFC0_CE_	O	Serial Flash chip enable
SFC0_DQ0	IO	Serial Flash data
SFC0_DQ1	IO	Serial Flash data
SFC0_DQ2/WP_	IO	Serial Flash write protect signal
SFC0_DQ3/HOLD_	IO	Serial Flash hold signal
MSC		
MSC<n>_CLK	O	MSC(MMC/SD) n clock output
MSC<n>_CMD	IO	MSC(MMC/SD) n command
MSC<n>_D<m>	IO	MSC(MMC/SD) n data bit m (0-3)
PWM		
PWM<n>	O	PWM n data output
PWM_TCU_TRIG	I	Use to save PWM counter
TCU		
TCU<n>_IN0	I	TCU n data input
TCU<n>_IN1	I	TCU n data input
PWM_TCU_ADC_TRIG	I	Use to save TCU counter
UART		
UART<n>_RXD	I	UART n receiving data
UART<n>_TXD	O	UART n transmitting data

UART<n>_CTS_	I	UART n Clear to send control
UART<n>_RTS_	O	UART n Request to send control
I2C		
I2C<n>_SCK	IO	I2C n serial clock
I2C<n>_SDA	IO	I2C n serial data
SSI		
SSI0_CLK	O	SSI clock output
SSI0_CE0_	O	SSI chip enable 0
SSI0_DT	O	SSI data output
SSI0_DR	I	SSI data input
SSI_Slave		
SSI_SLV_CLK	I	SSI Slave clock
SSI_SLV_CE0_	I	SSI Slave chip enable
SSI_SLV_DT	O	SSI Slave data output
SSI_SLV_DR	I	SSI Slave data input
NEMC(LocalBus)		
NEMC_CS1_	O	NEMC chip select1
AVD_	O	Address Valid ouput
RD_	O	NEMC read enable, low active
WE_	O	NEMC write enable, low active
ADn	IO	Address[15:0], Data[15:0] in muxed mode
WAIT_	I	External wait state request signal
CAN		
CAN<n>_TX	O	CAN n TX output to CAN transceiver
CAN<n>_RX	I	CAN n RX input from CAN transceiver
TPC		
SFT_CLK	O	Thermal Print Head data clock
SFT_D<n>	O	Thermal Print Head data channel n(0-7)
LAT_	O	Thermal Print Head latch pin
DST<n>	O	Thermal Print Head heating channel n(0-7)

SM<n>	O	Stepper Motor unit channel n(0-7)
DEBUG		
TDO	O	JTAG serial data output
TDI	I	JTAG serial data input
TCK	I	JTAG clock
TMS	I	JTAG mode select
RISCV_TDO	O	JTAG serial data output for RISC-V
RISCV_TDI	I	JTAG serial data input for RISC-V
RISCV_TCK	I	JTAG clock for RISC-V
RISCV_TMS	I	JTAG mode select for RISC-V

NOTES:

1 The meaning of phases in IO cell characteristics are:
   a DS: default output drive strength
   b Pull: default driver state, PD(pull-up), PU(pull-down) , HIZ
   c SlewRate: slew-rate function select fast mode by default
   d Schmitt: The IO cell is Schmitt trigger input by default
   e I: Digtal Input
   f O: Digtal Output
   g IO: Digtal Input and Output
   h AI: Analog Input
   i AO: Analog Output
   j AIO: Analog Input and Output
2 All GPIO shared pins are reset to GPIO input except PC00-03 is function 0

3 Electrical Specifications

3.1 Absolute Maximum Ratings

The absolute maximum ratings for the processors are listed in Table 3-1. Do not exceed these parameters or the part may be damaged permanently. Operation at absolute maximum ratings is not guaranteed.

Table 3-1 Absolute Maximum Rating

Parameter	Min	Max	Unit
Storage Temperature	-65	150	°C
Operation Temperature	-40	85	°C
VDD core power supplies voltage	-0.5	1.05	V
VDDMEM power supplies voltage (1.5V for DDR3)	-0.4	1.8	V
VDDMEM power supplies voltage (1.35V for DDR3L)	-0.4	1.8	V
VDDMEM power supplies voltage (1.8V for DDR2)	-0.5	2.3	V
DDR_PLLVCCA power supplies voltage	-0.5	1.98	V
PLL_AVDD power supplies voltage	-0.5	1.98	V
VDDIO18 power supplies voltage	-0.5	1.98	V
VDDIO33 power supplies voltage	-0.5	3.63	V
VCCA18	-0.1	1.98	V
VCCA09	-0.1	0.99	V
CODEC_AVDD	-0.1	1.98	V
USB_AVD33 power supplies voltage	-0.1	3.63	V
EFUSE_AVDD power supplies voltage	-0.1	1.98	V
IO voltage to VDDMEM (1.5V for DDR3) supplied non-supply pins	-0.4	1.8	V
IO voltage to VDDMEM (1.35V for DDR3) supplied non-supply pins	-0.4	1.8	V
IO voltage to VDDMEM (1.8V for DDR2) supplied non-supply pins	-0.5	2.3	V
IO voltage to VDDIO18 supplied non-supply pins	-0.3	2.28	V
IO voltage to VDDIO33 supplied non-supply pins	-0.5	3.93	V
IO voltage to CODEC_AVDD supplied non-supply pins	-0.1	1.98	V
IO voltage to USB_AVD33 supplied non-supply pins	-0.1	3.63	V
Maximum ESD stress voltage, Human Body Model; Any pin to any supply pin, either polarity, or Any pin to all non-supply pins together, either polarity. Three stresses maximum.	-	2000	V

3.2 Recommended operating conditions

Table 3-2 Recommended operating conditions for power supplies

Symbol	Description	Min	Typical	Max	Unit
VCORE	VDD core voltage	0.9	0.9	0.99	V
VMEM(1.5V)	VDDMEM voltage for DDR3	1.425	1.5	1.575	V
VMEM(1.35V)	VDDMEM voltage for DDR3L	1.283	1.35	1.45	V
VMEM(1.8V)	VDDMEM voltage for DDR2	1.71	1.8	1.89	V
VDDRPLL	DDR_PLLVCCA voltage	1.62	1.8	1.98	V
VIO18	VDDIO18 voltage	1.62	1.8	1.98	V
VIO33	VDDIO33 voltage	2.97	3.3	3.63	V
VDSI18	VCCA18 voltage	1.62	1.8	1.98	V
VDSI09	VCCA09 voltage	0.9	0.9	0.99	V
VCDC	CODEC_AVDD voltage	1.62	1.8	1.98	V

VUSB33	USB_AVD33 voltage	3.0	3.3	3.6	V
VEFUSE	EFUSE_AVDD voltage	1.71	1.8	1.98	V

Table 3-3 Recommended operating conditions for SARADC pins

Symbol	Description	Min	Typical	Max	Unit
SADC_VREFP	VCCA18 and VSS are used as reference for SADC	-	1.8	VADC	V
V_{IADC}	AUX0-1,4-6 input voltage range	0		VADC	V

Table 3-4 Recommended operating conditions for others

Symbol	Description	Min	Typical	Max	Unit
TA	Ambient temperature	–40		85	°C

3.3 DC Specifications

The DC characteristics for each pin include input-sense levels and output-drive levels and currents. These parameters can be used to determine maximum DC loading, and also to determine maximum transition times for a given load. All DC specification values are valid for the entire temperature range of the device

Table 3-5 DC characteristics for VREF

Symbol	Parameter	Min	Typical	Max	Unit
DDR_VREF(DC)	Reference voltage supply of DDR	0.49* VMEM	0.5* VMEM	0.51* VMEM	V

NOTE: The ac peak noise on VREF may not allow VREF to deviate from VREF(DC) by more than +/- 1% VMEM.

Table 3-6 DC characteristics for VDDIO33 supplied pins

Symbol	Parameter		Min	Typical	Max	Unit
V_{DVDD}	I/O supply voltage		2.97	3.3	3.63	V
V_{PAD}	Voltage at IO		-0.3		V_{DVDD}+0.3	V
V_{IL}	Input Low Voltage		-0.3		0.8	V
V_{IH}	Input High Voltage		2		V_{DVDD}+0.3	V
V_{T+}	Schmitt trig low to high threshold point		0.9		2.1	V
V_{T-}	Schmitt trig high to low threshold point		0.7		1.9	V
R_{PU}	Pull-up Resistor		36	57	100	kΩ
R_{PD}	Pull-down Resistor		35	57	103	kΩ
V_{OL}	Output low voltage				0.23	V
V_{OH}	Output high voltage		2.69			V
I_{OL}	Low level output current	2mA	3.5	6.0	8.8	mA
		4mA	8.1	13.0	20.5	mA
		8mA	13.8	23.8	35.2	mA
		12mA	18.4	31.7	46.9	mA
I_{OH}	High level output current	2mA	3.4	5.3	7.5	mA
		4mA	6.9	10.7	14.9	mA

		8mA	12.7	19.7	27.5	mA
		12mA	16.1	25.0	35.0	mA

Table 3-7 DC characteristics for VDDIO18 supplied pins

Symbol	Parameter		Min	Typical	Max	Unit
VDDIO	I/O supply voltage		1.62	1.8	1.98	V
V_{IL}	Input Low Voltage		-0.3		0.35* VDDIO	V
V_{IH}	Input High Voltage		0.65* VDDIO		VDDIO +0.3	V
V_T	Threshold point		0.83	0.91	1	V
V_{T+}	Schmitt trig low to high threshold point		0.95	1.03	1.12	V
V_{T-}	Schmitt trig high to low threshold point		0.73	0.8	0.9	V
V_{TPU}	Threshold point with pull-up resistor enabled		0.82	0.9	1	V
V_{TPD}	Threshold point with pull-down resistor enabled		0.84	0.92	1	V
V_{TPU+}	Schmitt trig low to high threshold point with pull-up resistor enabled		0.94	1.02	1.11	V
V_{TPU-}	Schmitt trig high to low threshold point with pull-down resistor enabled		0.72	0.79	0.89	V
V_{TPD+}	Schmitt trig low to high threshold point with pull-down resistor enabled		0.96	1.05	1.12	V
V_{TPD-}	Schmitt trig high to low threshold point with pull-up resistor enabled		0.74	0.81	0.91	V
I_L	Input Leakage Current @ V_I=1.8V or 0V				±10	μA
I_{OZ}	Tri-State output leakage current @ V_I=1.8V or 0V				±10	μA
R_{PU}	Pull-up Resistor		55	79	122	kΩ
R_{PD}	Pull-down Resistor		51	87	169	kΩ
V_{OL}	Output low voltage				0.45	V
V_{OH}	Output high voltage		VDDIO -0.45			V
I_{OL}	Low level output current	(DS1,DS0) = 00	7.7	12.8	17.8	mA
		(DS1,DS0) = 01	15.3	25.4	35.2	mA
		(DS1,DS0) = 10	22.8	37.6	51.7	mA
		(DS1,DS0) = 11	30.2	49.2	67.1	mA
I_{OH}	High level output current	(DS1,DS0) = 00	4.8	10.9	18.9	mA
		(DS1,DS0) = 01	9.6	21.5	37.4	mA
		(DS1,DS0) = 10	14.4	32.3	56.0	mA
		(DS1,DS0) = 11	19.1	42.8	74.2	mA

3.4 SARADC Electrical Characteristics

Table 3-8 SARADC Performance

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Operating Condition						
Analog Supply	AVDD	-	1.62	1.8	1.98	V
SARADC Performance						
Resolution	-	-	-	12	-	bit
Effective Number of Bit	ENOB	-	10-	11	-	bit

Differential Nonlinearity	DNL	-	-1.5	-	+1.5	LSB
Integral Nonlinearity	INL	-	-3	-	+3	LSB
Reference voltage	VREFP		-	1.8	-	V
Input Capacitance	C_{IN}	-	-	16	-	pF
Sampling Rate	f_S	-	-	-	2	MS/s
Spurious Free Dynamic Range	SFDR	f_S=2MS/s f_{OUT}=1.17KHz	-	70	-	dB
Signal to Noise and Harmonic Ratio	SNDR	-	-	68	-	dB
Power Consumption						
Analog Supply Current	IAVDD	f_S=2MS/s	-	1.9	-	mA
		Power Down	-	1	-	uA
Digital Supply Current	IVDD	f_S=2MS/s	-	0.1	-	mA
		Power Down	-	1	-	uA

3.5 Power On, Reset and BOOT

3.5.1 Power-On Timing

The external voltage regulator and other power-on devices must provide the X2670 processor with a specific sequence of power and resets to ensure proper operation. Following are the name of the power：

- VDD09: all 0.9V power supplies, VDD, VCCA09
- VMEM: VDDMEM
- VDDIO18: all 1.8V power supplies, VDDIO18, DDR_PLLVCCA, VCCA18, CODEC_AVDD, EFUSE_AVDD
- CODEC_AVDD, USB_AVD18
- VDDIO33: all 3.3V power supplies, VDDIO33, USB_AVD33

Table 3-9 Power-On Timing Parameters

Symbol	Parameter	Min	Max	Unit
t_{D_VMEM}	Delay between VDD09 arriving 90% to VMEM arriving 50%	0	–	ms
$t_{D\_VDDIO18}$	Delay between VDD09 arriving 90% to VDD18 arriving 50%	0	–	ms
$t_{D\_AVDIO33}$	Delay between VDDIO18 arriving 90% to VDDIO33 to be turned on	100	–	us
$t_{D\_PPRST\_}$	Delay between all power rails get stable and power-on reset PPRST_ de-asserted	1	–	ms[2]

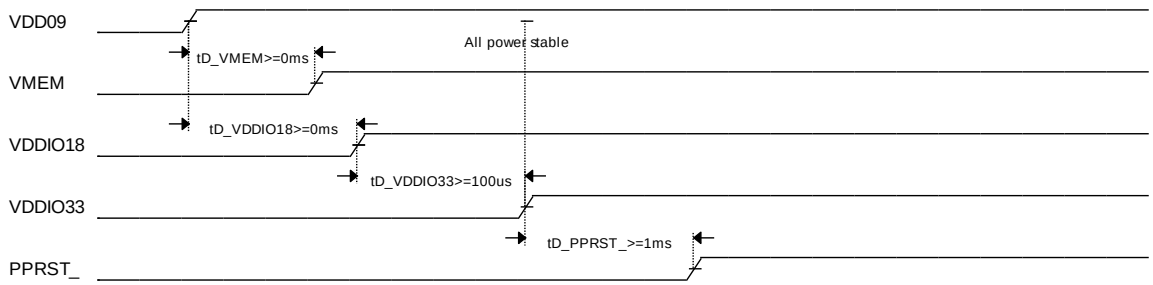


Figure 3-1 Power-On Timing Diagram

3.5.2 Power On Reset(POR)

X2670 has an internal POR circuit, and compares PLL_AVDD,VDD with the reference voltage to generate a signal which is open-drain output.

Table 3-10 POR

Symbol	Parameter	Min	Typical	Max	Unit
V_{tha+}	Power up threshold on PLL_AVDD supply[1]	1.3	1.35	1.4	V
V_{tha-}	Power down threshold on PLL_AVDD supply[1]	1.2	1.25	1.3	V
V_{thd+}	Power up threshold on VDD supply[1]	0.55	0.6	0.65	V
V_{thd-}	Power down threshold on VDD supply[1]	0.45	0.5	0.55	V
V_{hysa}	POR hysteresis on PLL_AVDD supply[1]	-	0.1	-	V
V_{hysd}	POR hysteresis on VDD supply[1]	-	0.1	-	V
T_{dr}	Debounce delay time for POR rising edge	-	120	-	us
T_{df}	Debounce delay time for POR falling edge	-	4	-	us
T_{D_POR}	Extend delay time for POR rising edge[2]		15		ms

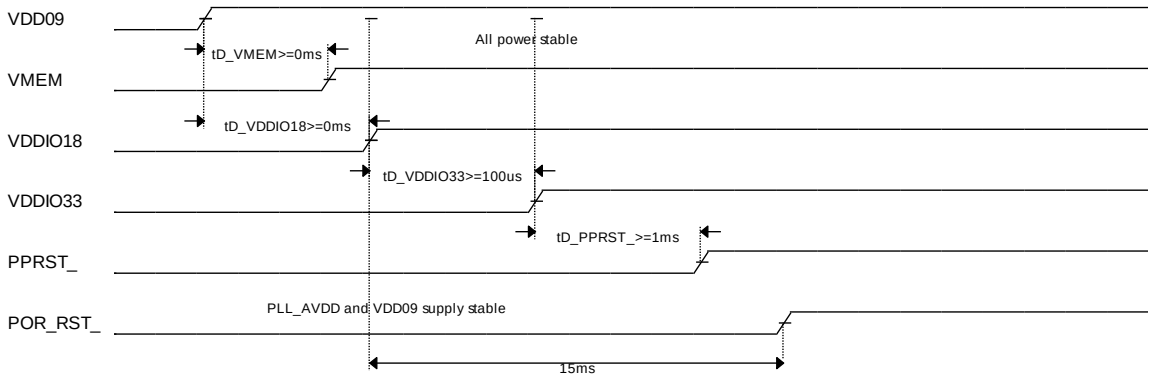


Figure 3-2 POR_RST_ Timing Diagram

Note:

1 In order to use the POR circuit to reset X2670, follow the circuit design below to connect the POR_RST_ to PPRST_.

2 After PLL_AVDD and VDD supply stable, the POR_RST_ output will be extended 15ms then release.

Following figure shows the sequence where PLL_AVDD rises first and VDD drops first.

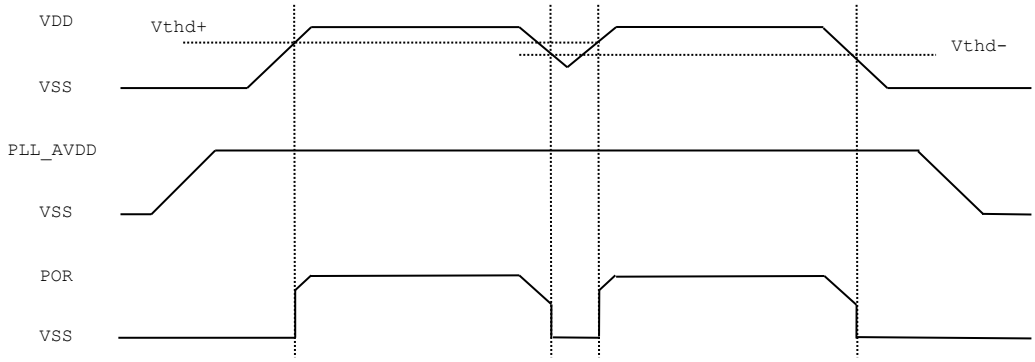


Figure 3-3 POR TIMING 1

Following figure shows the sequence where VDD rises first and PLL_AVDD drops first.

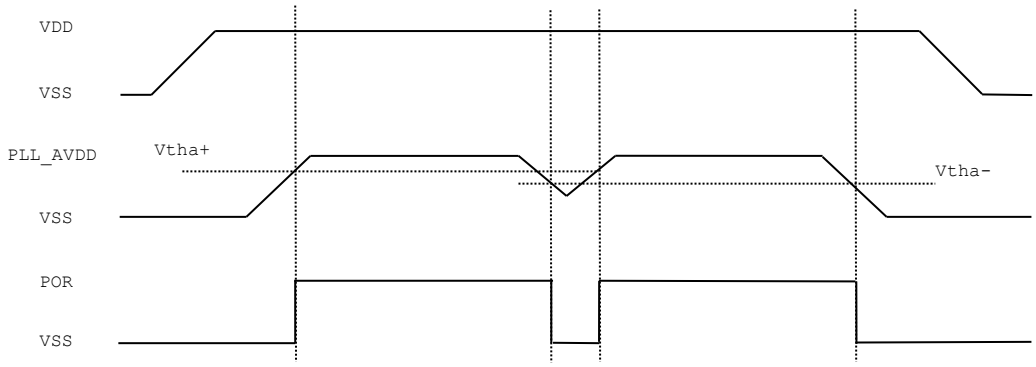


Figure 3-4 POR TIMING 2

3.5.3 Reset Procedure

In addition, X2670 also supports 2 reset sources: 1 PPRST_ pin reset; 2 WDT timeout reset. After reset, program start from boot.

1 PPRST_ pin reset

This reset is trigged when PPRST_ pin is put to logic 0. It happens in power on all power stable and RESET-KEY pressed to reset the chip from unknown dead state.

2 WDT timeout reset

This reset happens in case of WDT timeout. The reset keeps for about a few EXCLK/512 cycles.

After reset, all GPIO shared pins are put to GPIO input function, except JTAG relate TCK/ TMS/ TDI/TDO which reset to function mode. The oscillators are on.

3.5.4 BOOT

The boot sequence of the X2670 is controlled by boot_sel [1:0].

Table 3-11 Boot configuration of X2670

boot_sel[1]	boot_sel[0]	Boot configuration	Error jump
0	0	MSC0(PD0)_3.3V	SFC(PD0)_3.3V
0	1	SFC(PD6)_3.3V	MSC1(PD6)_3.3V
1	0	SFC(PD0)_3.3V	USB
1	1	USB	

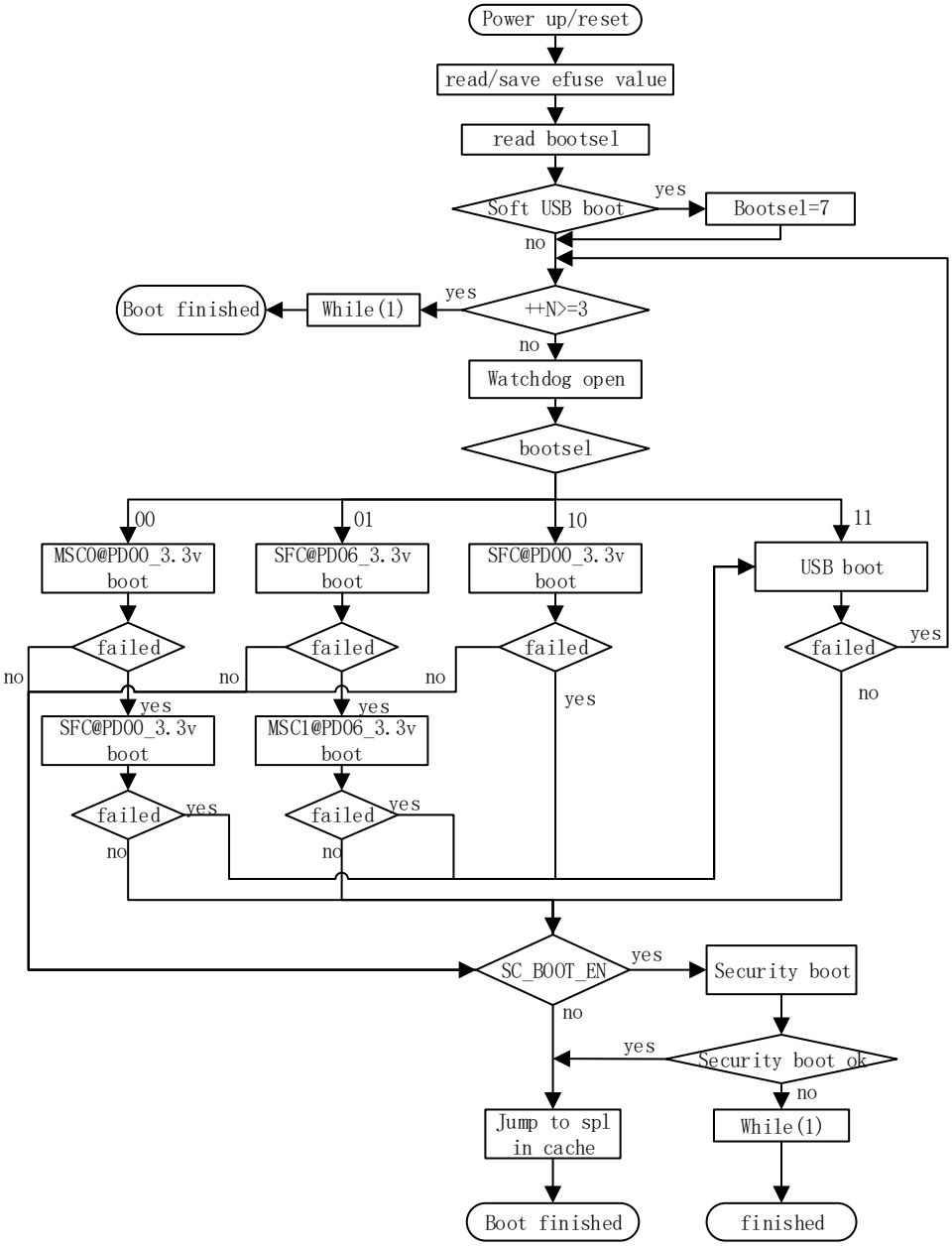


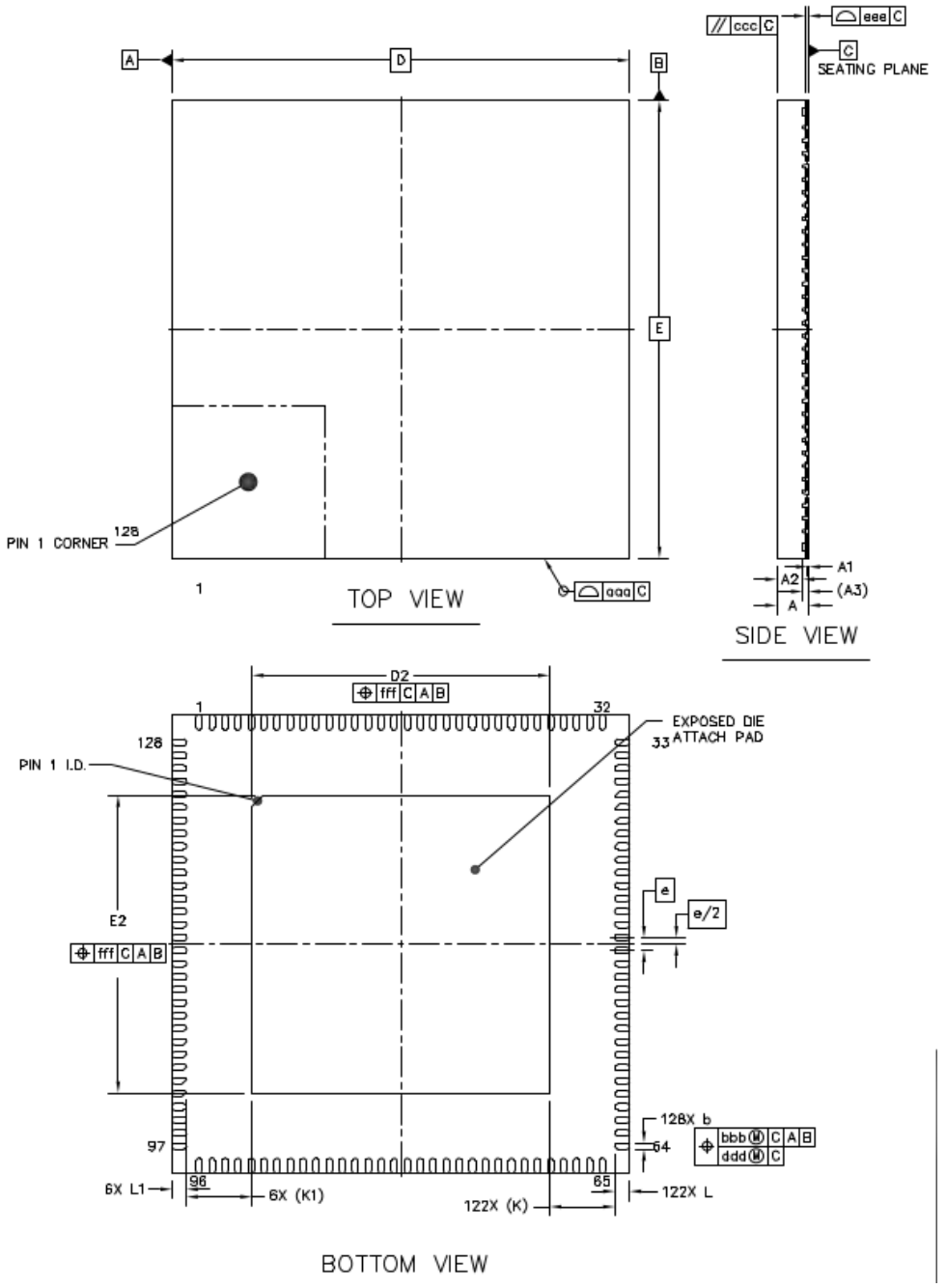
Figure 3-5 Boot sequence diagram of X2670

4 Packaging Information

4.1 Overview

X2670 processor is offered in 128 QFN package, the size is 12.3mm x 12.3mm x 0.85mm, 0.35mm pin space.

4.2 Device Dimensions



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.7	---
L/F THICKNESS		A3		0.152 REF	
LEAD WIDTH		b	0.12	0.17	0.22
BODY SIZE	X	D		12.3 BSC	
	Y	E		12.3 BSC	
LEAD PITCH		e		0.35 BSC	
EP SIZE	X	D2	7.9	8	8.1
	Y	E2	7.9	8	8.1
LEAD LENGTH		L	0.3	0.4	0.5
		L1	0.29	0.39	0.49
LEAD TIP TO EXPOSED PAD EDGE		K		1.75 REF	
		K1		1.76 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.07	
		ddd		0.05	
EXPOSED PAD OFFSET		fff		0.1	

Figure 4-1 X2670 package outline drawing

Notes:

1. REFER TO JEDEC MO-220;
2. COPLANARITY APPLES TO LEADS,CORNER LEADS AND DIE ATTACH PAD;
3. BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES OF JCET PRESCRIBING;
4. FINISH:Cu/EP • Sn8~20s

4.3 Moisture Sensitivity Level

X2670 package moisture sensitivity is level 3.