Ingenic® X2000

Hardware Design Guide

Revision: 1.1
Data: 2021.7

北京君正集成电路股份有限公司
Ingenic Semiconductor Co., Ltd.

Ingenic X2000

Hardware Design Guide

Release history

Date	Revision	Change
2021.07	1.1	Correct some mistakes
2021.05	1.0.1	Correct some mistakes
2021.04	1.0	First release

Disclaimer

Ingenic Semiconductor Co., Ltd.

Ingenic Headquarters, East Bldg. 14, Courtyard #10,
Xibeiwang East Road, Haidian Dist., Beijing 100193, China
Tel: 86-10-56345000
Fax: 86-10-56345001
http: //www.ingenic.com

CONTENTS

1 Overview 1
1.1 Abbreviation description 1
1.2 X2000 block diagram 2
1.3 X2000 features 3
1.4 Applications 3
2 Hardware Design Checkpoints 4
2.1 Minimum System 4
2.1.1 Power Design 4
2.1.2 Clock Design 7
2.1.3 Watchdog and Reset 7
2.1.4 Boot and Security Boot 8
2.1.5 Build-in DDR 9
2.2 Peripheral Interfaces 10
2.2.1 Ethernet 10
2.2.2 Display 11
2.2.3 Camera 12
2.2.4 USB OTG 14
2.2.5 Audio 16
2.2.6 Memories 18
2.2.7 WIFI & Bluetooth 20
2.3 PCB Design 22
2.3.1 PCB Layout 22
2.3.2 PCB stack and impedance 23
2.3.2.1 PCB Layer Stacking 23
2.3.2.2 Signal Traces Impedance 23
2.3.3 Return Path Guidelines 24
2.3.4 Clock Layout Guidelines 25
2.3.5 X2000 RGMII Layout Guidelines 25
2.3.6 MIPI signals Layout Guidelines 25
2.3.7 Analog Signals Layout Guidelines 26
2.4 GPIO Notice 27

1 Overview

X2000 hardware design manual is used to help users quickly master the development and design based on the processor X2000. The manual divides the design points according to X2000 functional modules, and provides reference design for interfaces to help users develop their own functional modules. The manual also provides users with the necessary inspection items of X2000 design and the PCB layout rules. Ensure the successful start of the first prototype developed by users, reduce the risk of software and hardware development and shorten the time to market.

This manual helps users get started quickly and develop their own products by using the existing software and hardware resources of the Halley5 platform development kit provided by Ingenic team. Your participation and suggestions are our greatest encouragement and support.

X2000 is a high-performance and highly integrated comprehensive application processor product launched by Ingenic. It adopts XBurst® 2 dual core 1.2GHz main frequency and XBurst® 240MHz small core architecture. It has low power consumption and is mainly oriented to the field of intelligent Internet of things and data control. It integrates a large number of system equipment, including lpddr3 (128MB SIP lpddr3), high-performance audio codec, LCD controller, camera sensor interface, SSI controller, SD / MMC controller, I2C controller, etc., supports USB OTG, UART interface, OTP, and has multiple flexible GPIO interfaces.

1.1 Abbreviation description

RMII: Reduced Media Independent Interface
RGMII: Reduced Gigabit Media Independent Interface
eMMC: Embedded Multi-Media Card
SDIO: Secure Digital Input and Output
OTG: On The Go
PCM: Pulse Code Modulation
Quad SPI: Quad Serial Peripheral Interface
Octal SPI: Octal Serial Peripheral Interface
I2C: Inter-Integrated Circuit
UART: Universal Asynchronous Receiver/Transmitter
SPDIF: Sony/Philips Digital Interface
I2S: Inter-IC Sound
DMIC: Digital Micro Phone
MIPI: Mobile Industry Processor Interface
MIPI CSI: MIPI Camera Serial interface
MIPI DSI: MIPI Display Serial interface
CIM: Camera Interface Module

1.2 X2000 block diagram

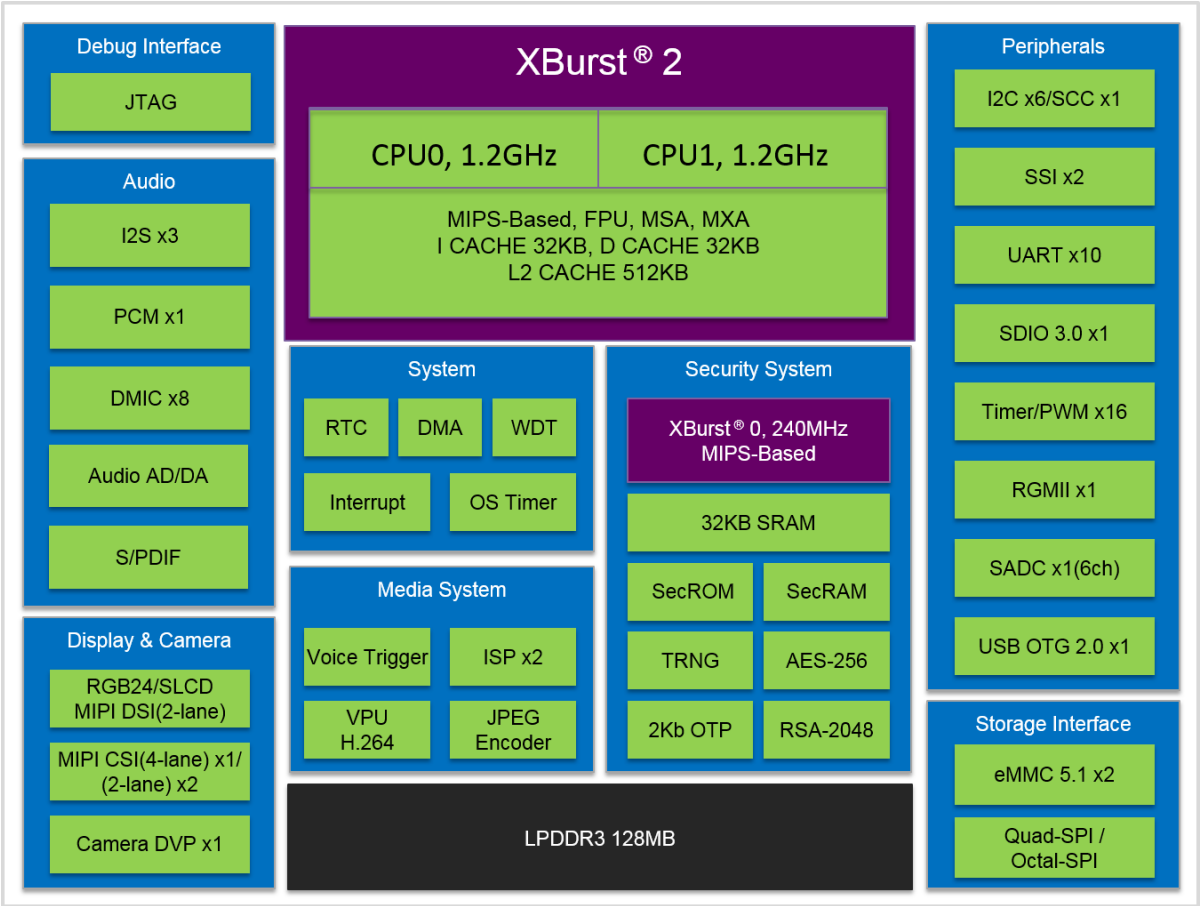

Figure 1.2.1 X2000 Functional Block Diagram

1.3 X2000 features

- One minor CPU core which is good at real time control, MIPS based, run at 240MHz
- One Video Processing Unit consisting of H.264 encoder/decoder and JPEG encoder / decoder
- Two Image Processing Units (ISP) and Camera Interfaces connecting up to 3 cameras at the same time
- LPDDR3 128MBytes memory on chip
- Audio CODEC including ADC and DAC on chip together with three I2S ports, PCM interface and S/PDIF
- MIPI-DSI with the resolution up to 1920x1080@40Hz
- SLCD display interface with the resolution up to 640x480@60Hz, 24BPP
- RGB display interface, with the resolution up to 1280x720@60Hz, 24BPP
- External memory interface for SPI Flash
- Interrupt controller up to 64 sources
- A/D converter on chip with a resolution of 10bit, 6 channels
- Real time clock
- GPIO, I2C x6, SSI x2, TCU x8 / PWM x16 and UART x10
- EMMC / SD / SDIO x3
- USB 2.0 OTG
- Gigabit Media Access Controller (RGMII), in compliance with IEEE 1588-2002
- Security subsystem with true random number generator and AES-256 / RSA-2048 / MD5 / SHA / SHA2 engines
- BGA270 package, 12mm x 12mm x 1.2mm, 0.65mm pitch

1.4 Applications

- Smart Audio: Smart Speakers, Smart Toys
- Image Recognition: QR Code Readers, Plate Recognition, Facial Recognition and Finger Print Recognition
- Smart Appliances: Smart Air-conditioners, Smart Refrigerators, Smart Small Appliances
- Smart Home: Smart Gateways, Smart Lights
- Smart Office: Cloud Printers, Data Transfer Units

2 Hardware Design Checkpoints

2.1 Minimum System

2.1.1 Power Design

X2000 has certain timing requirements for power up sequence, wrong timing sequence may lead to the following situations:

- GPIO is not in HIZ state during power up
- Fail to start up
- High current impulse during power up

VDDIORTC: VDDIORTC
VDDRTC: VDDRTC
VDDIO18: all other 1.8V power supplies, include: VDDIO, VDDIO18, PLLAVDD, DDRPLL, DDR_VDD1, VDDIO18_CIM, CSI_AVD18, DSI_AVD18, USB_AVD18, CODEC_AVDD and SADC_AVDD
VMEM: VDDMEM
VDDIO33: all 3.3V power supplies include: VDDIO33, VDDIO33_CIM, VDDIO33_SD and AVDUSB33
VDD: all other 0.9V power suppliers include: VDD, PLLVDD, DSI_AVD09, CSI_AVD09 and USB_AVD09
AVDEFUSE: AVDEFUSE

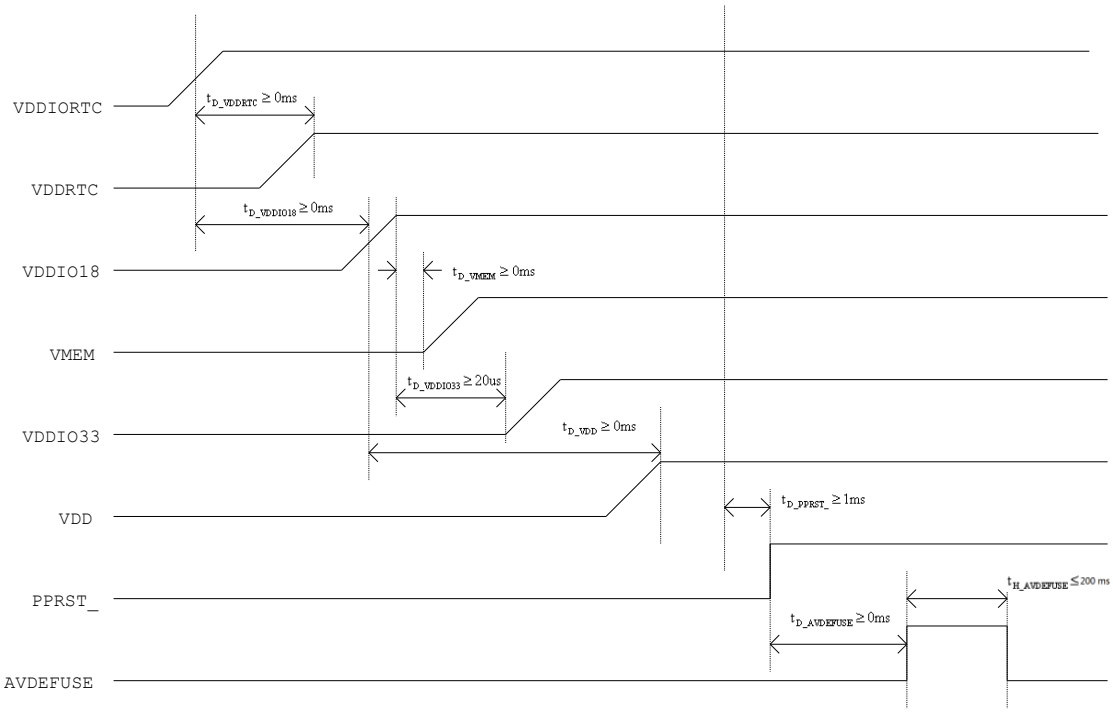

Figure 2.1.1 X2000 Power on Sequence

Table 2.1.1 Power on Sequence Timing

Symbol	Parameter	Min	Max	Unit
t_{D_VDDRTC}	Delay between VDDIORTC arriving 50% to VDDRTC arriving 90%[1]	0	–	ms
$t_{D\_VDDIO18}$	Delay between VDDIORTC arriving 50% to VDDIO18 arriving 50%[1]	0	–	ms
t_{D_VMEM}	Delay between VDDIO18 arriving 90% to VMEM to be turned on	0	–	ms
$t_{D\_VDDIO33}$	Delay between VDDIO18 arriving 90% to VDDIO33 to be turned on	20	–	us
t_{D_VDD}	Delay between VDDIO18 arriving 50% to VDD arriving 90%[1]	0	–	ms
$t_{D\_PPRST\_}$	Delay between all power rails get stable and power-on reset PPRST_ de-asserted[2]	TBD[3]	–	ms[2]
$t_{D\_AVDEFUSE}$	Delay between PPRST_ finished and E-fuse programming power apply	0	–	ms
$t_{H\_AVDEFUSE}$	E-fuse programming time	–	200	ms

NOTES:

1 The power rails have same skew.

2 The PPRST_ must be kept at least 1ms. If mechanical jitter of keys is toke into account, 10ms is recommended.

3 It must make sure the EXCLK is stable and all power (except AVDEFUSE) is stable.

Figure 2.1.2 shows the typical power design of X2000, and it supports 2 kinds of power saving schemes, hibernate and deep sleep (deep sleep is also called fast boot in some documents and designs). The difference is the existences of DDR_VDD1 and VMEM.

Case 1: X2000 enters hibernate mode and outputs the PWRON signal low to shut down power supplies except VDDIORTC and VDDRTC. Which means only RTC module of X2000 still work, and users can trigger WAKUP key to wake up the system.

Case 2: X2000 enters deep sleep mode and outputs the PWRON signal low to shut down power supplies except VDDIORTC, VDDRTC, VDDMEM and DDR_VDD1. Which means RTC module of X2000 still work as well as DDR, users also can trigger WAKUP key to wake up the system. But compared with recovering from hibernation, recovering from deep sleep can start more quickly, and the time is less than 1s.

Implementation of Case 1: R143 is no connection, R144 is 0 Ω. The power interface J34 input 5V, and then through the U10 over-voltage and over-current protection chip OVP, as the system's total power supply VSYS. VSYS supplies power to U7 to output VDDIORTC, and VDDIORTC supplies power to U6 to output VDDRTC. When the RTC module of X2000 is powered on, the signal PWRON will assert high to enable 1V8P output, then 1V8P enable other DC-DC bucks to supply power 1V2P, 3V3P and 0V9P to X2000.

Implementation of Case 2: R143 is 0 Ω, R144 is no connection. The power interface J34 input 5V, and then through the U10 over-voltage and over-current protection chip OVP, as the

system's total power supply VSYS. VSYS supplies power to U7 to output VDDIORTC, and VDDIORTC supplies power to U6 to output VDDRTC. However, VDDIORTC also supplies power to DDR_VDD1 at the same time, so PMIC BUCK2 outputs 1V2P to supply power to VDDMEM. When the RTC module of X2000 is powered on, the signal PWRON will assert high to enable 1V8P output, then 1V8P enable other DC-DC bucks to supply power 3V3P and 0V9P to X2000.

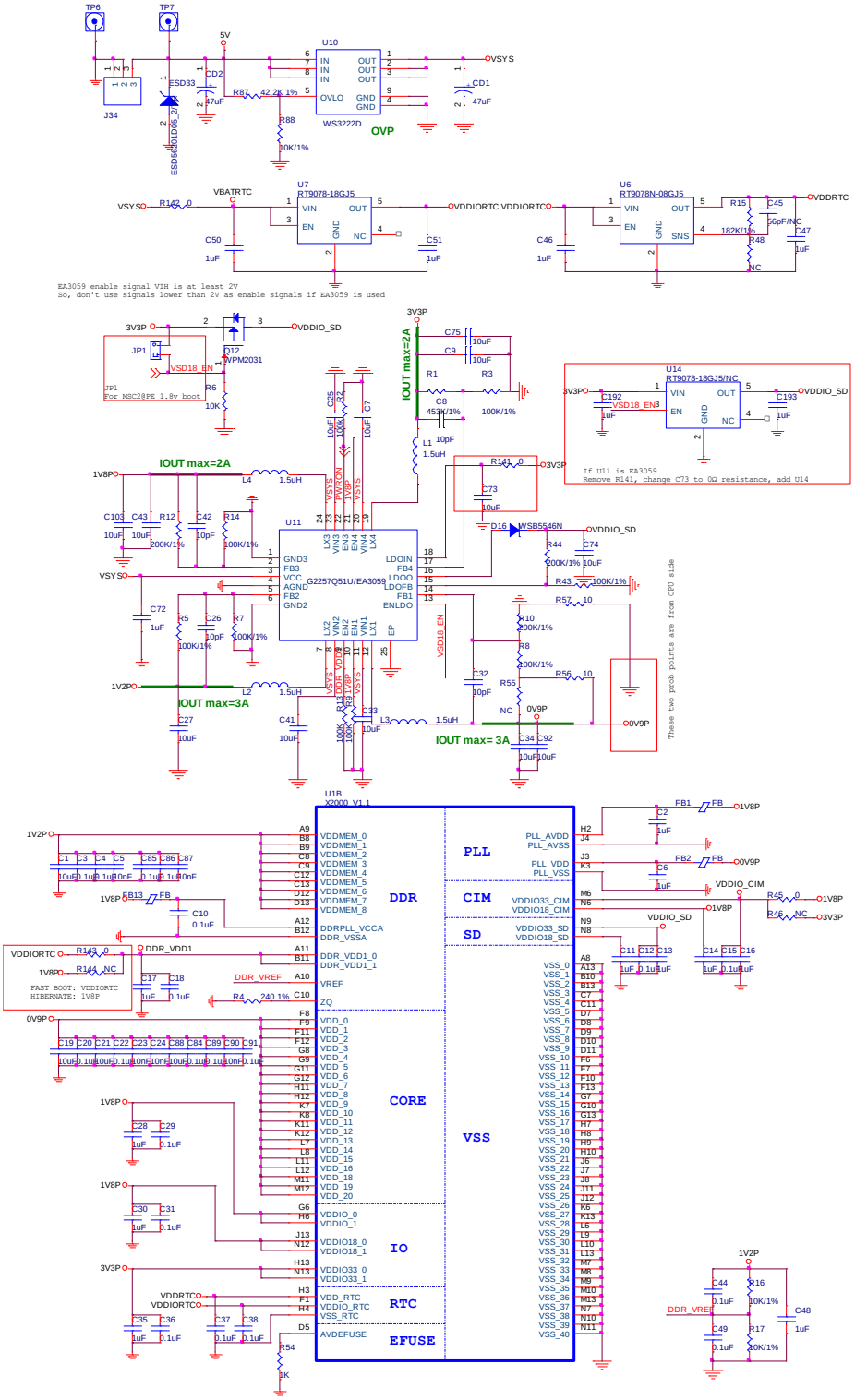

Figure 2.1.2 X2000 Power Reference Design

2.1.2 Clock Design

X2000 has an on-chip oscillator circuit which can support external 24MHz crystal. As working master clock of X2000, the frequency deviation of the crystal is required not more than 20ppm, and the effective resistance of the crystal is less than 40 Ω. The designer can chose the crystal according to these conditions, and adjust the capacitance and resistance according to the reference circuit in the figure below. Or use a 1.8V oscillator to output a 24MHz ± 20ppm clock source to the J1 pin EXCLK_ XI, left J2 floating. Figure 2.1.3 shows a typical connection for a crystal resonator circuit. The load capacitor values vary with the crystal vendors, check with the vendor for the recommended loads.

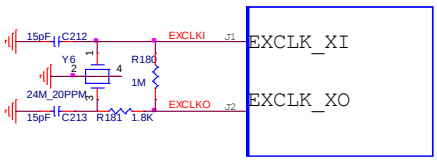

Figure 2.1.3 X2000 24MHz Working Clock Design

X2000 also has an on-chip oscillator circuit which can support external 32.768 KHz crystal. But it's necessary to parallel a 10M Ω resistor as shown in the figure below Figure 2.1.4, otherwise it will not vibrate. Or use a 32.768 KHz independent clock source to connect to pin G2, and left pin G1 floating. In addition, X2000 is able to boot up without an external RTC clock source, so designers don't have to design an RTC clock if the RTC clock isn't necessary.

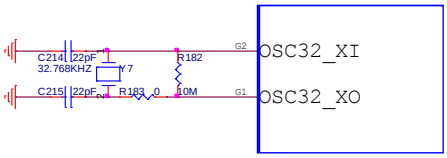

Figure 2.1.4 X2000 RTC Clock Design

2.1.3 Watchdog and Reset

X2000 is able to support internal watchdog timer function, and this function is controlled by a set of X2000's registers and is used to resume the processor whenever it is disturbed by malfunctions. But, if an external hardware watchdog and reset are required, please refer to the Figure 2.1.5 and note the difference between the voltage of input and output signals. It's suggested that use a reset chip with an open drain output for X2000's PPRST_N.

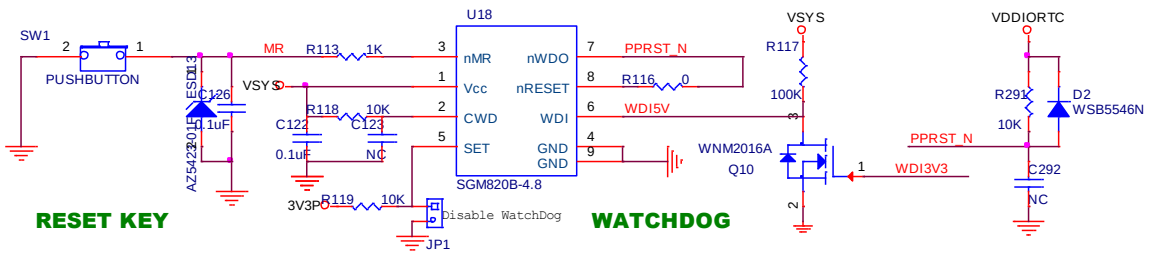

Figure 2.1.5 Watchdog Reference Design

2.1.4 Boot and Security Boot

X2000 uses 3 functional pins as strap options to place the device into boot modes, and the values of these pins are sampled at reset. And X2000 has a boot ROM inside, after reset, the boot program in the internal boot ROM will read boot_sel[2:0] to determine the boot method, the supported boot mode please refer to the Table 2.1.2.

Table 2.1.2 X2000 Boot Mode Configuration

boot_sel[2]	boot_sel[1]	boot_sel[0]	Boot configuration
0	0	0	SFC0@PE 3.3v
0	0	1	MSC2@PE 3.3v
X	1	0	USB
0	1	1	Nor flash
1	0	0	SFC0@PD 1.8v
1	0	1	MSC0@PD 1.8v
1	1	1	MSC2@PE 1.8v

NOTE: X means "DON'T CARE", and it is not recommended to use these 3 pins for GPIOs if there are other GPIOs left.

Booting from USB mode means that users update firmware through a USB cable connected with a host PC. Actually, Ingenic provide a programming tool USBCloner, and this burning tool can be installed on the PC with any one of followed OS, Windows XP, Windows 7, Ubuntu12.04 etc. Please find more detailed instructions for using the burning tool (USBCloner) from the USBCloner guide.

If security boot is enabled in the OTP EFUSE, X2000 will enter security boot flow. Therefore, the boot program will need users' key and NKU to start up. Actually those keys are burn in the OTP EFUSE of X2000 by USBCloner. So the OTP EFUSE has two work modes, one specific mode is the read mode, and the other is the mode for program. The difference of the two modes is the voltage of AVDEFUSE which is the power supply of OTP EFUSE, if the voltage is 0, then the OTP EFUSE is under the read mode. And if the developers need to program the OTP EFUSE, they can control the voltage to 1.8V ± 5% through software, then the OTP EFUSE will enter the program mode. And please note that the programming time MUST be less than 200ms. The control design of OTP EFUSE please refer to the Figure 2.1.6.

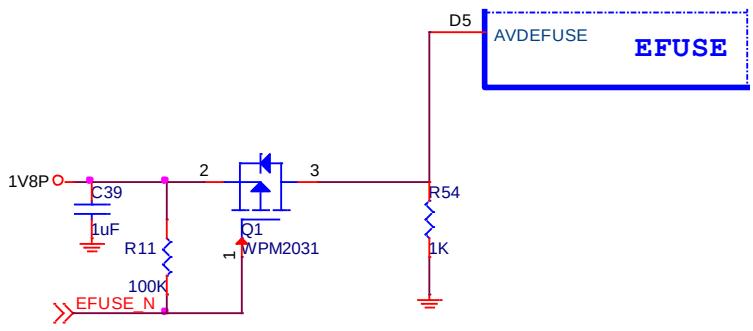

Figure 2.1.6 OTP EFUSE Reference Design

2.1.5 Build-in DDR

X2000 has a build-in LPDDR3 memory in package, therefore, a 240Ω 1% ZQ calibration resistor must be externally connected to the ball of X2000 C10. And the VREF is the reference voltage of DDR signals, and it is ought to half voltage of VMEM, the tolerance is less than 2% VREFDC. The reference design is as shown in the Figure 2.1.2.

2.2 Peripheral Interfaces

2.2.1 Ethernet

The X2000 processor contains one Gigabit Ethernet media access controller (GMAC), supports transmission speed of 10 / 100 / 1000 Mbps, supports RMII and RGMII interfaces, supports full duplex and configurable half duplex operation. The reference schematic diagram of X2000 with Gigabit Ethernet PHY chip is shown in the Figure 2.2.1.

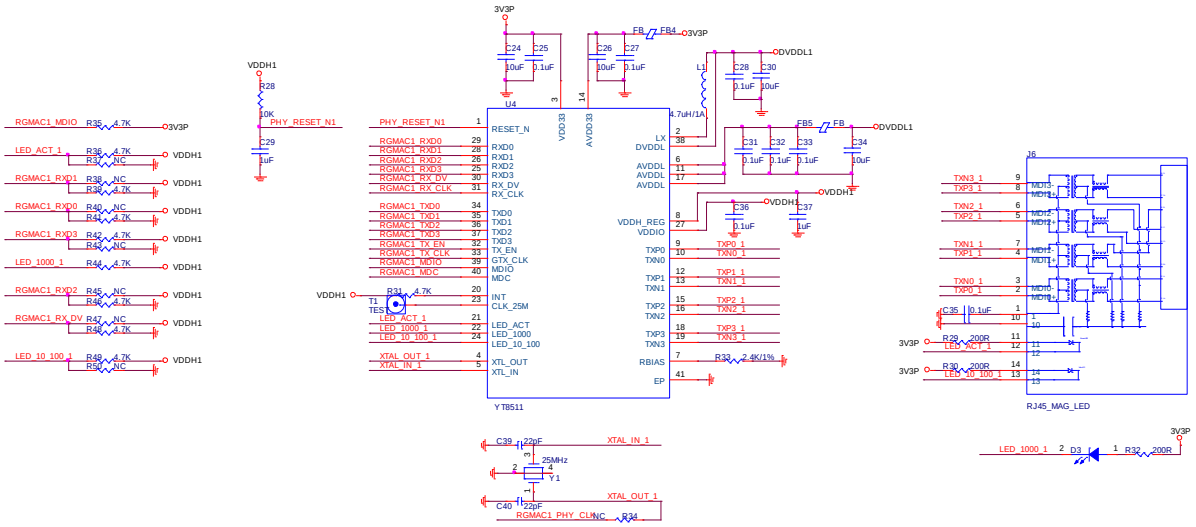

Figure 2.2.1 Gigabit Ethernet Design

As shown in the figure 2.2.1 and figure 2.2.2, The GMAC provides the interface between the host application and the PHY layer through RMII or RGMII. And the PHY layer device is external to the processor X2000. So the communication between controller and PHY chip is realized through RMII or RGMII interface. When using RGMII interface for the communication, the working clock of PHY chip can be provided by an external crystal or by the RGMAC of X2000, as shown in the Figure 2.2.1 RGMAC1_ PHY_ CLK is 25M Hz from X2000 pin and configured as the working clock of PHY chip.

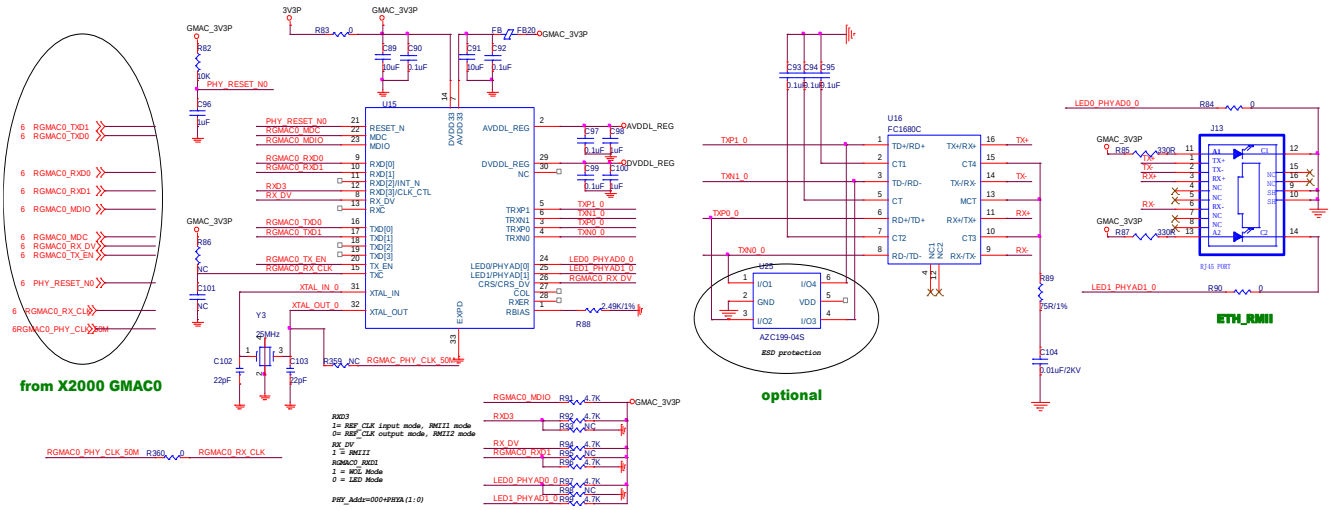

Figure 2.2.2 10/100M Ethernet Design

If using RMII interface for the communication, RGMAC0_RX_CLK is the reference clock input to X2000. And RGMAC0_ PHY_ CLK_50M is 50M Hz from X2000 pin and configured as the working clock of PHY chip as well as the reference clock as shown in the Figure 2.2.2.

2.2.2 Display

X2000 supports SMART LCD interface, RGB interface and MIPI-DSI interface. SMART LCD interface can be connected to an 8 / 9 / 16-bit smart LCD, and image size is 640x480@60Hz; RGB interface can be connected to an 8 / 16 / 18 / 24-bit TFT, and it supports ARGB8888, ARGB1555, RGB888, RGB565, RGB555, YUV422 and YUV420 input format, display image size is up to 1280x720@60Hz; MIPI-DSI interface can be connected to a 1 / 2-lane MIPI LCD, and the image size is up to 1920x1080@40Hz, 24bbp. Halley5 development kit equip with a 2-lane MIPI OLED panel, and it's reference design as followed Figure 2.2.3, and it's required that the impedance of MIPI differential signals is about 100 Ω.

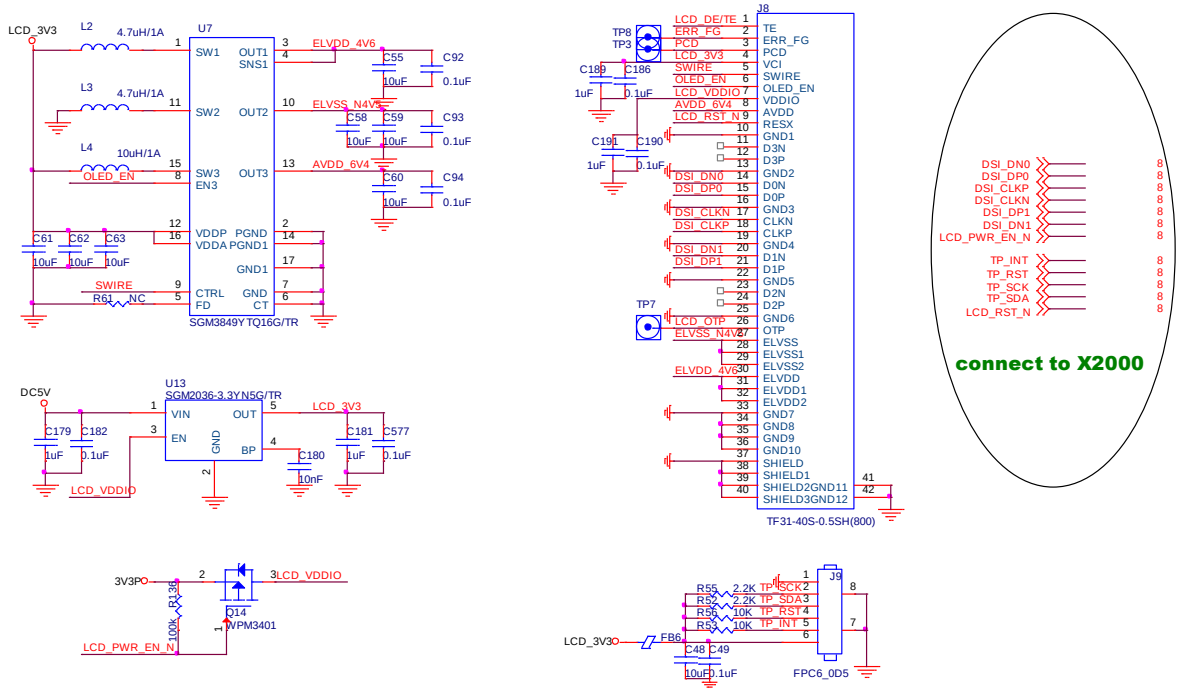

Figure 2.2.3 MIPI Display Interface

Figure 2.2.4 is for RGB 24-bit TFT application.

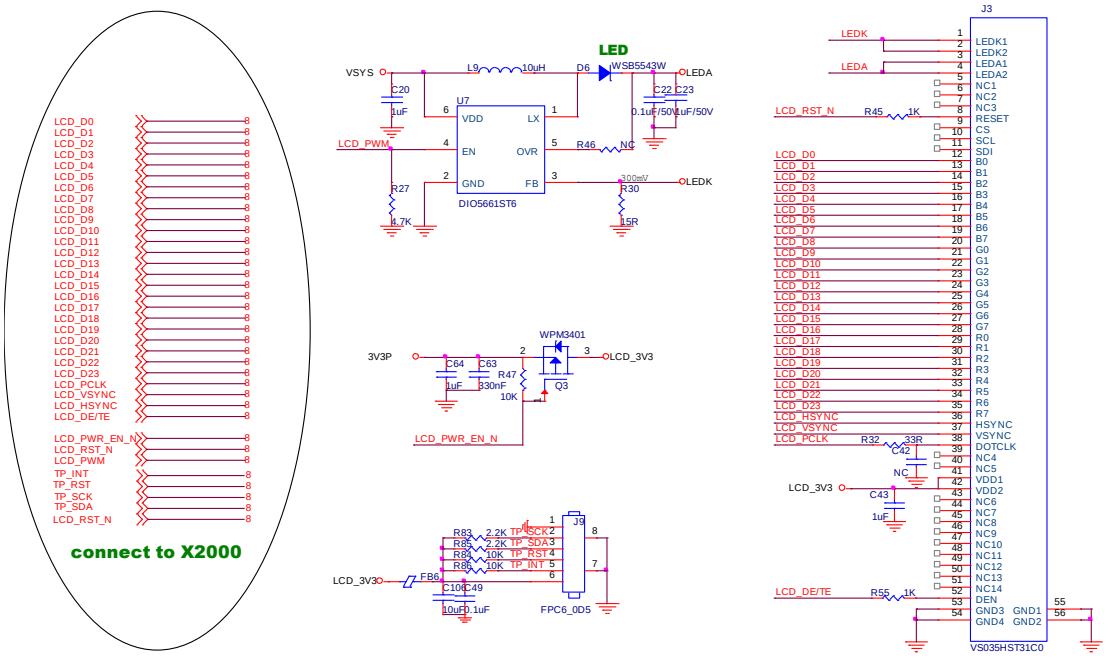

Figure 2.2.4 RGB Display Interface

2.2.3 Camera

X2000 processor has a CIM (camera interface module) and a Video Interface Control (VIC).

CIM supports 8 bits DVP and MIPI CSI(1 / 2-lane) data in ITU656, YCbCr 4:2:2, RGB888, RGB565 or MONO(8) format, and its resolution is up to 1080P@30fps. CIM also supports Snapshot and exposure control.

VIC input data from the DVP interface and the MIPI Camera Serial Interface (CSI). The DVP interface supports raw8 / 10 / 12 / YUV422 (Serial 8bit) format, and the image size up to 1080P@30fps. The MIPI-CSI supports RAW8, RAW10, RAW12(1 / 2 / 4-lane) format, and the image size is up to 1080P@120fps. VIC also supports two Image Signal Processors (ISP) which supports dual-camera sync, 2-D noise reduction filter, auto exposure, auto white balance, advanced demosaic, color processing, lens shading, sharpen, static/dynamic defect pixel correction etc.

X2000 supports single camera, dual cameras or three cameras application. In addition, two of the three cameras can process data through ISP because X2000 has two ISPs. For example, the X2000 development board Halley5 reserves an external camera interface to connect three cameras. Single camera application supports 8 / 10 / 12-bit DVP and 1 / 2 / 4-lane MIPI. Dual cameras application supports 8 / 10 / 12-bit DVP + 1 / 2 / 4-lane MIPI and dual 2-lane MIPI cameras. Please note that if two ISPs are used in DVP + MIPI application, MIPI camera should be connected to the clock1, lane2, lane3 signals as the followed Figure 2.2.5.

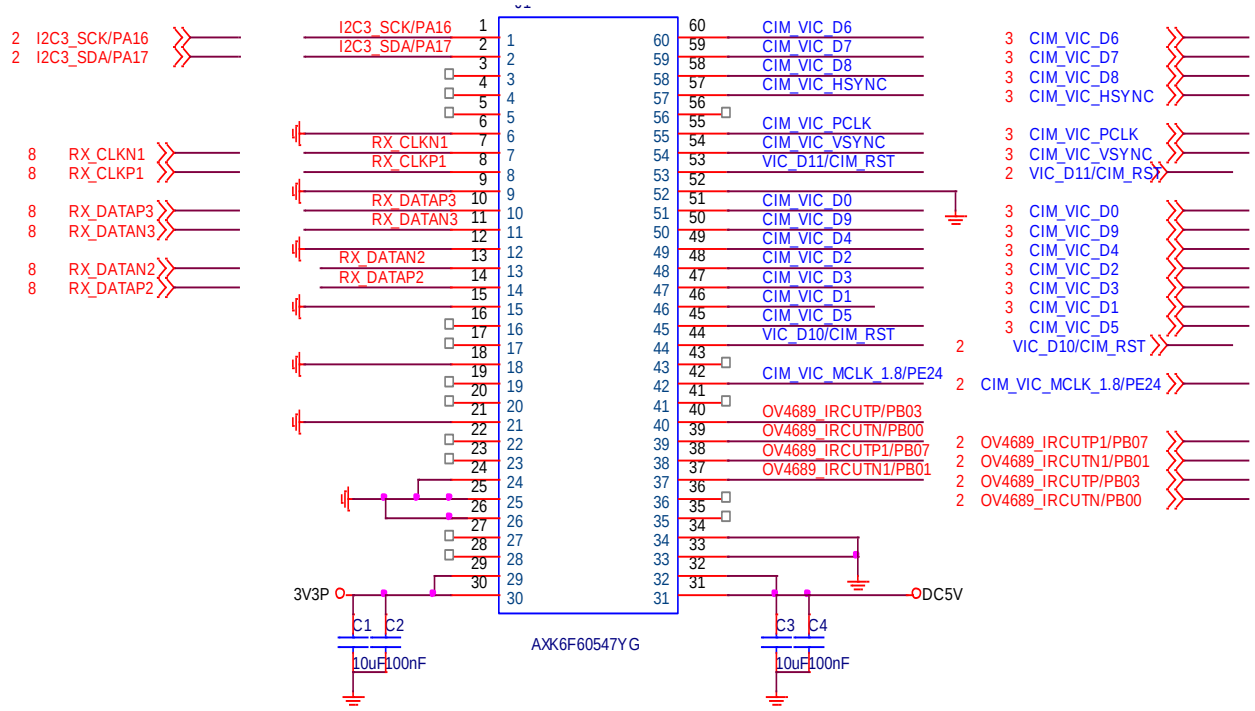

Figure 2.2.5 10-bit DVP+2-lane MIPI Dual CAMERA

A 4-lane MIPI camera interface is as the followed Figure 2.2.6.

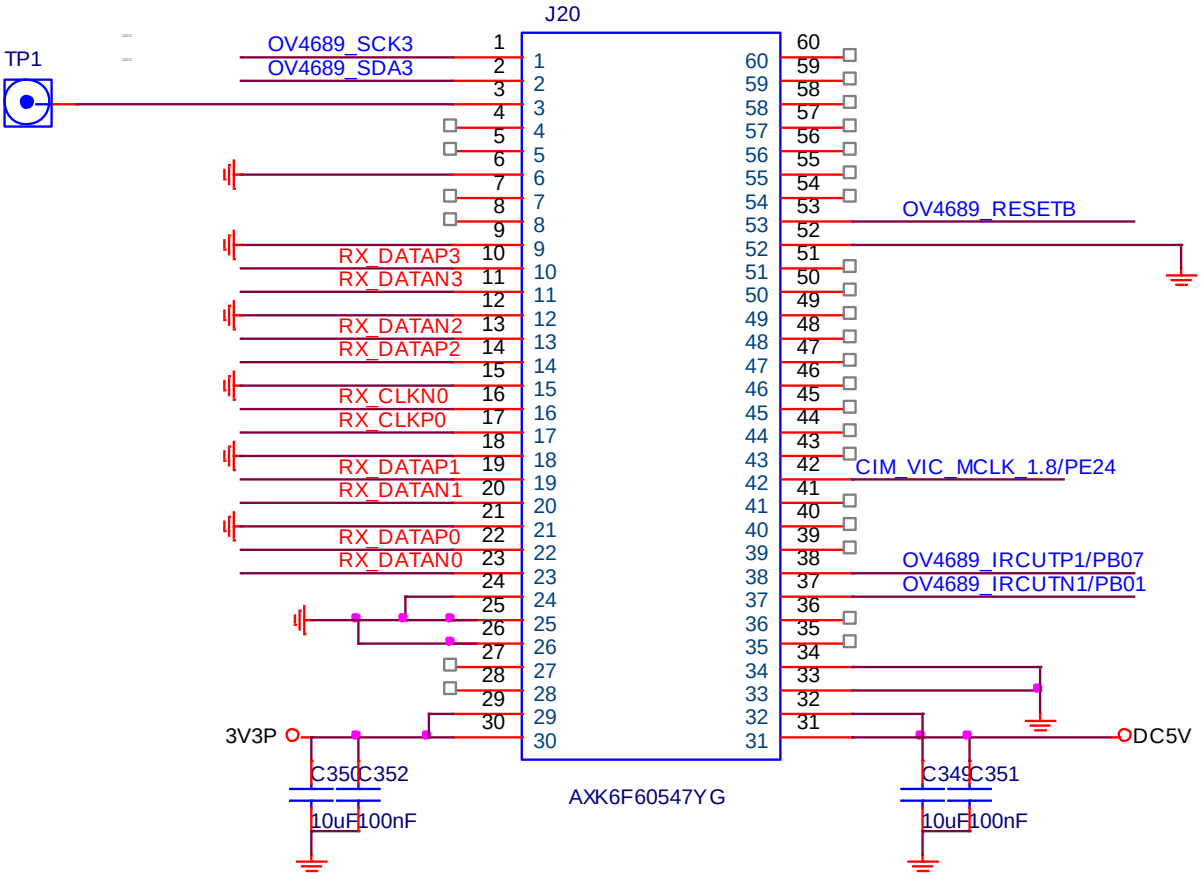

Figure 2.2.6 4-lane MIPI CAMERA

2.2.4 USB OTG

X2000 has a USB2.0 interface which can support OTG, host only and device only functions. Figure 2.2.7 shows the USB interface of processor X2000, it includes OTG_DM, OTG_DP, USB_VBUS, USB_ID etc. if X2000 is configured as OTG function, and left USB_ID floating, X2000 is USB device by default. But as long as USB_ID connect to GND (the impedance between USB_ID and GND is less than 10Ω), X2000 will work as USB host automatically. Meanwhile, X2000 monitors the power supply voltage of USB device through USB_VBUS, and the required voltage range is 5.25V ~ 4.75V. X2000 will shut down the OTG function automatically if the power supply voltage of USB device drop to 4.6V around caused by the USB device trouble. In addition, VBUS must be divided to 3/5 off chip to avoid overvoltage.

What's more, there's a pin of OTG_TXR_RKL connected with an external resistor of 135Ω with 10% tolerance to the ground, it's for the reference of USB 2.0 high-speed impedance.

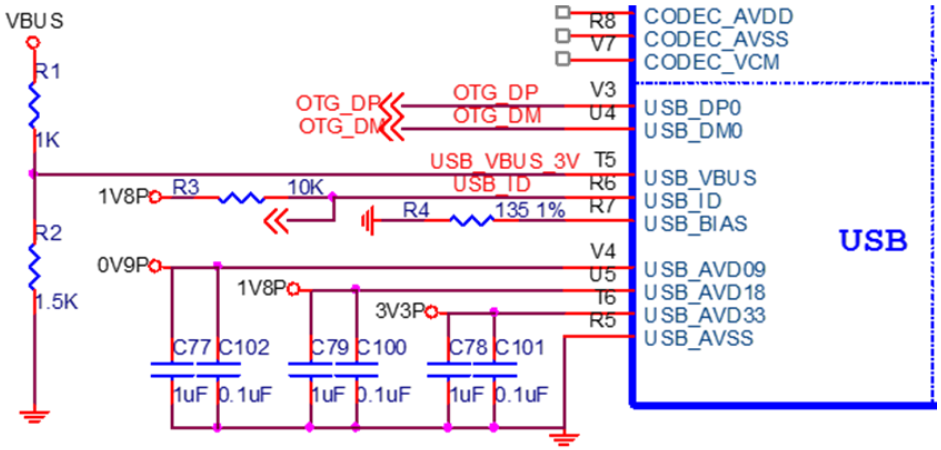

Figure 2.2.7 X2000 USB Interface

The USB interface of X2000 is not only an interface to expand USB devices, but also is the firmware downloading port as well as ADB debug port. The followed Figure 2.2.8 shows X2000 with a USB 4G module application. The differential signals OTG_DM and OTG_DP are from X2000 USB interface, and then they are connected to the USB SWITCH chip which has two paths. One path is to the USB HUB chip which is connected to USB 4G module and other USB devices. The other is to the firmware downloading port as well as ADB debug port. In this application X2000 works as host by default, but once a USB cable connected to PC is plugged in the downloading port, the USB switch chip will switch the path to the firmware downloading port automatically, and X2000 will work as device.

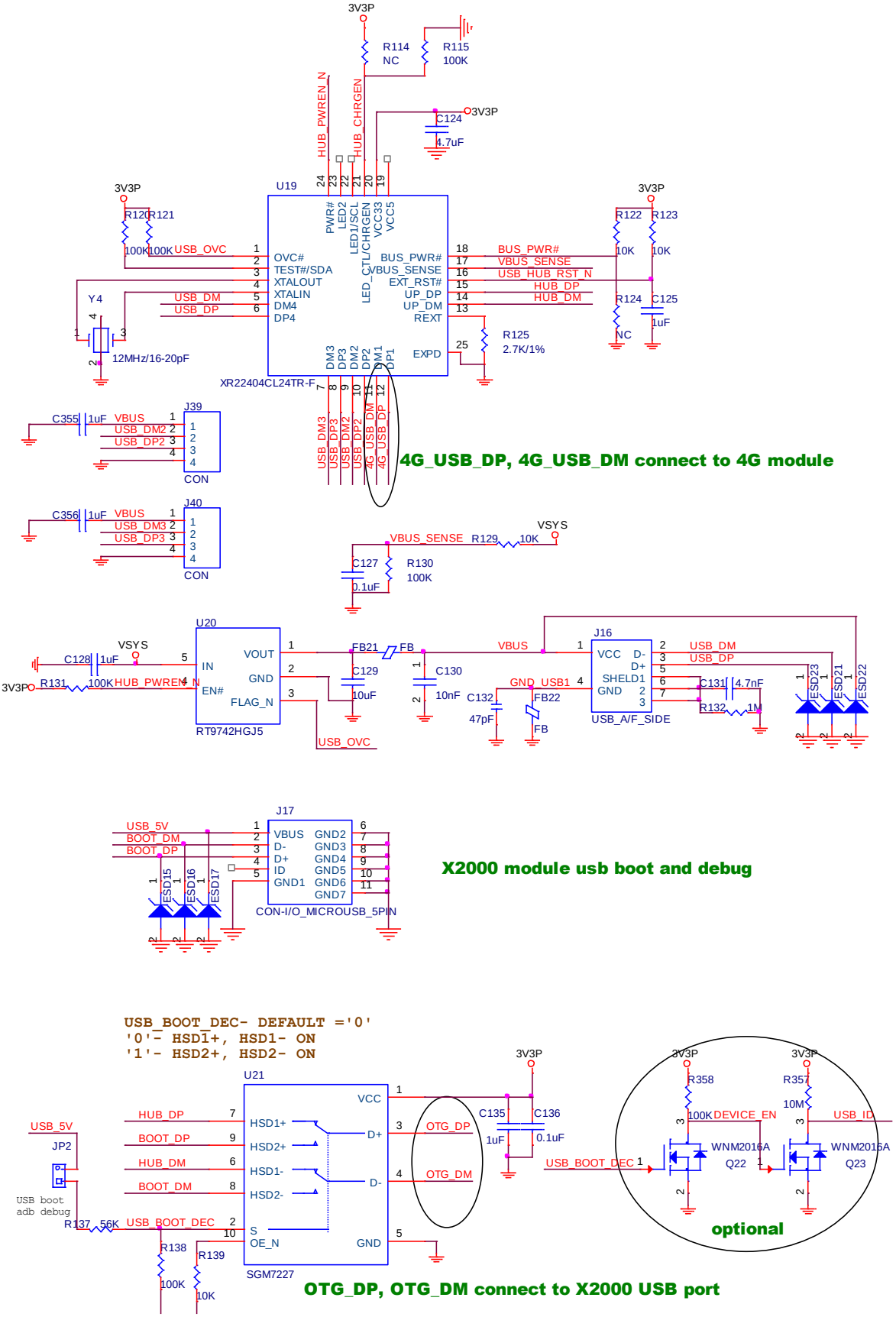

Figure 2.2.8 X2000 with USB 4G module Application

2.2.5 Audio

X2000 has rich audio interface resources, which can support 4-channel digital microphone, SPDIF input and output interface, PCM, internal codec and 3 I2S interfaces. Among them, I2S0 can support asynchronous recording and playback, I2S1 only supports recording and I2S3 only supports playback.

1. Digital microphone

   The digital mic channel of X2000 can support voice trigger to wake X2000 from sleep state. Users can also refer to the example in the Figure 2.2.9 below, which supports 8 digital microphone array. The figure below shows the connection of one digital microphone channel to two silicon microphones. The LR pins of the two microphones are connected high and low to distinguish whether the digital microphone channel samples at the rising edge or the falling edge of the signal CLK.

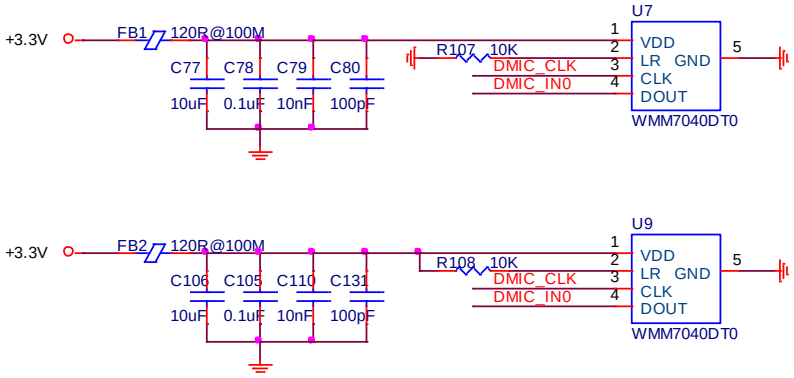

Figure 2.2.9 X2000 Digital MIC Application

2. X2000 supports SPDIF input interface as well as SPDIF output interface, which is compatible with IEC 60958-3.
3. X2000 supports PCM interface, which can be configured as master or slave. And X2000 supports DSP NORMAL / LEFT MODE, PCM NORMAL / LEFT MODE. The PCM interface is widely used in Bluetooth audio transmission.
4. Internal Codec

   X2000 integrates an internal CODEC which can implement differential audio signals sampling and playing. The followed Figure 2.2.10 shows there are 4.7uF and 0.1uF decupling capacitors connected to the VCM pin for high quality audio of internal codec.

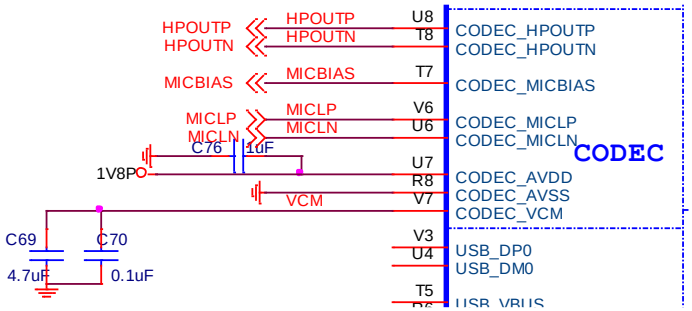

Figure 2.2.10 X2000 Internal CODEC

a) Analog MIC input

The values of those resistors as the Figure 2.2.11 shown R491 and R119 depend on the selected EC microphone. And MICBIAS is the bias voltage of the EC microphone provided by X2000, in other case, the bias voltage is supplied by a 0.9V power source instead of X2000.The C285 1nF decoupling capacitor at MICBIAS is used to eliminate the high frequency noise. The voltage of MICBIAS can configured from 0.9V to1.53V, and the max current of MICBIAS is 3mA.

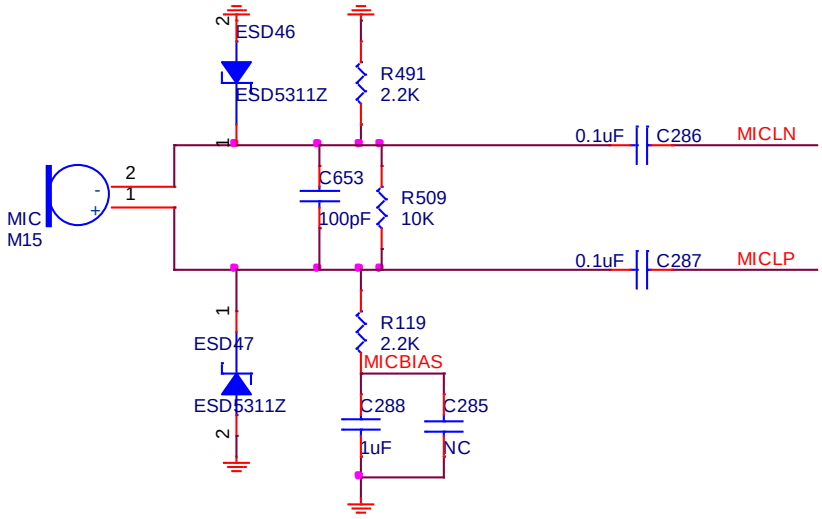

Figure 2.2.11 X2000 Analog Microphone Application

b) Analog audio signal output

Differential signals HPOUTP and HPOUTN are output analog audio signals. There's necessary to connect a power amplifier for a speaker application, and the reference circuit please refer to the followed Figure 2.2.12.

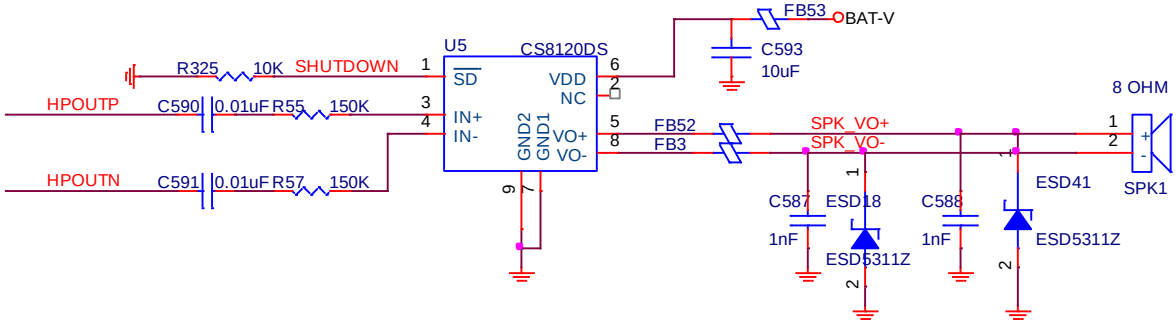

Figure 2.2.12 X2000 Analog Audio Signals Output Application

5. Digital audio interface I2S

Developers can using the I2S interface to extend an external CODEC to get a better performance of the audio. There are 3 I2S interfaces for external codec application.

a) X2000 I2S1 supports asynchronous bidirectional transmission, recording and playing.

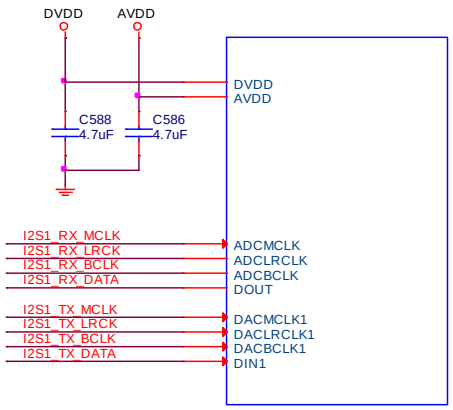

Figure 2.2.13 X2000 I2S1 Interface Application Diagram

b) X2000 I2S2 supports recording only.

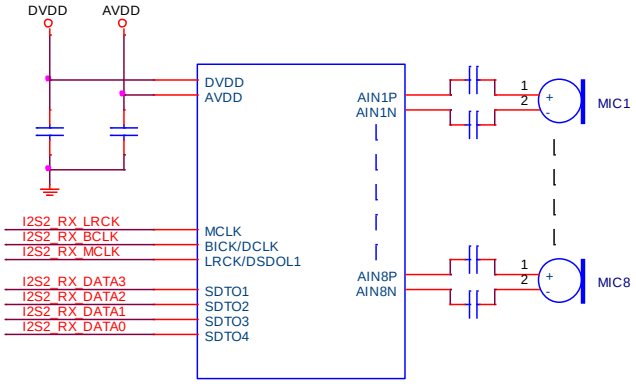

Figure 2.2.14 X2000 I2S2 Interface Application Diagram

c) X2000 I2S3 supports playing only.

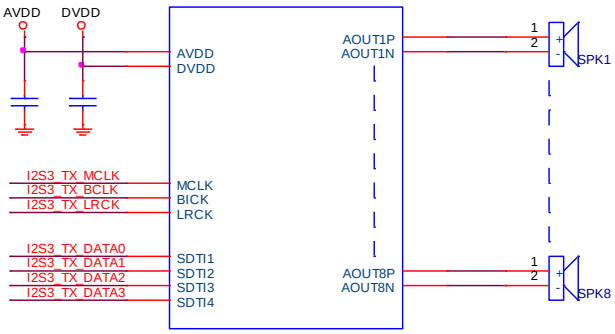

Figure 2.2.15 X2000 I2S3 Interface Application Diagram

2.2.6 Memories

X2000 not only has a 128 Mbytes built-in LPDDR3 memory in the package, but also supports a lot kinds of external memories, such as Quad / Octal SPI NAND / NOR flash, SD / TF card and eMMC flash, NEMC(SRAM) etc.

1. SFC

X2000 has a SFC controller, which can support standard, dual, quad, octal SPI. According to the Table 2.1.2 X2000 Boot Mode Configuration, X2000 will boot from SFC in GPIO

group PE if BOOT_SEL[0:2] are 000 during reset. Halley5 take a 2Gbits SPI NAND Flash as the program storage. Please refer to the followed Figure 2.2.16 as reference design, in addition, this design is compatible with SPI NOR Flash.

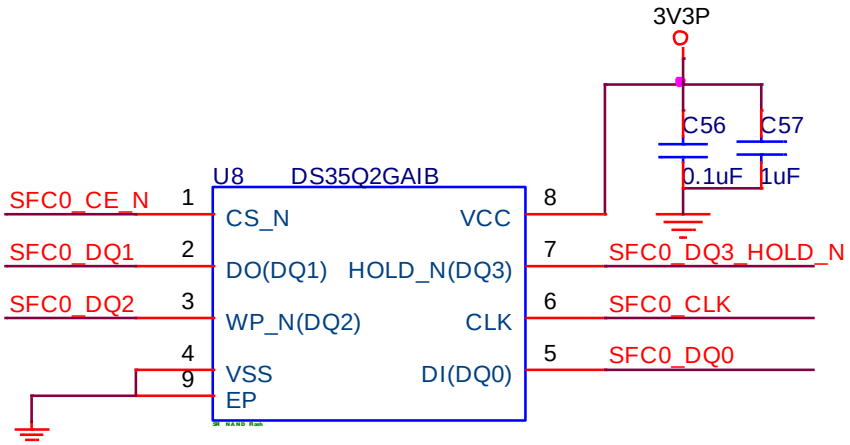

Figure 2.2.16 SPI FLASH Design

2. SD/SDIO/EMMC

X2000 has 3 SD/SDIO/EMMC controller (MSC0, MSC2, SDIO), which can support eMMC5.1, SD4.0, SDIO3.0 high speed mode, and the speed of clock is up to 187MHz. The SDIO interface is usually for communication with WIFI devices. The voltage of MSC2 signals can be 1.8V or 3.3V, so MSC2 is suitable for TF card and SD card interface. Compared with the other two interfaces, MSC0 not only supports 1 / 4 / 8 bits transmission, which is mostly used to connect with high-speed EMMC NAND flash. The X2000 development board halley5 is equipped with a TF card slot as shown in the Figure 2.2.17 below, and combined with the power design in the figure 2.1.2, VDDIO_SD will dynamically switch to 1.8V from 3.3V if X2000 identifies the high-speed card during initialization.

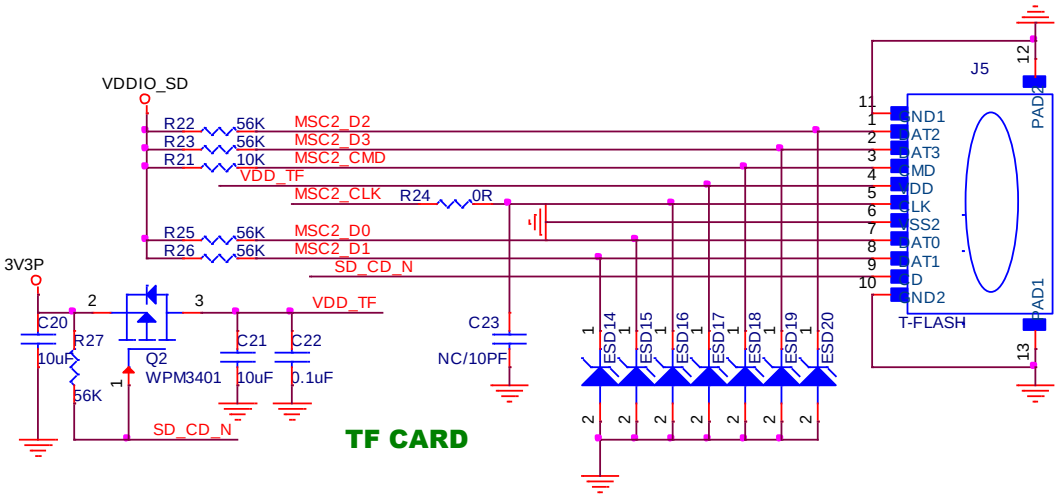

Figure 2.2.17 TF Card Slot

If the eMMC NAND is used as the storage of the boot code, the hardware reset of EMMC should be linked with the system reset signal PPRST_N in case of the system boot failure caused by the EMMC error. The reference design in the Figure 2.2.18 below shows that MSC0 is used as the eMMC interface. If MSC2 is used, please change the IO power of eMMC from 1.8V to the voltage of MSC2 signals.

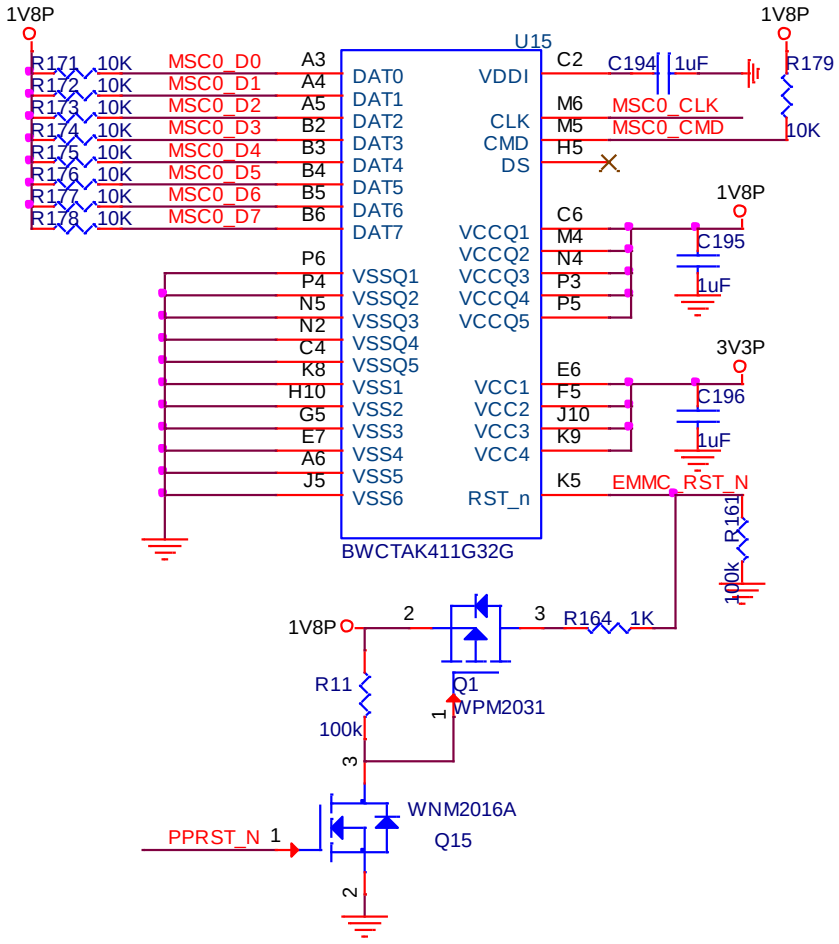

Figure 2.2.18 eMMC Flash Application

3. NEMC(SRAM)

X2000 processor also supports NEMC (SRAM) parallel interface. The address width of external NEMC interface can reach 12 bits and the data width can reach 16 bits, the interface also supports two chip select signals. In some cases, this interface is used to connect a FPGA. It should be noted that this interface and parallel LCD interface are multiplexed IO, so if using NEMC interface, the function of parallel LCD is no longer available.

2.2.7 WIFI & Bluetooth

X2000 processor has abundant interface resources, including UART, SSI, I2C, PWM, TCU, etc. in addition to the audio and video interface, RGMII, SDIO interface and PCM interface mentioned in the previous sections. So X2000 processor has powerful interconnection function.

For instance, X2000 communicates with a Wi-Fi / BT module through SDIO interface, PCM interface and UART interface. The figure 2.2.19 below shows the application design of Wi-Fi & BT module AP6256 on the X2000 development board Halley5. The module supports dual band Wi-Fi 802.11 b / g / n / ac, Bluetooth 5.0 with BLE. The antenna working frequency is 2.4GHz and 5GHz, and the layout of antenna circuit needs to match 50 Ω impedance to get a better performance. It should be noted that if CLK32K in the figure below is provided by X2000, G1 and G2 pins of X2000 must be connected with a RTC crystal or a 1.8V 32K clock source, and the RTC reference design of X2000 is shown in the Figure 2.2.19.

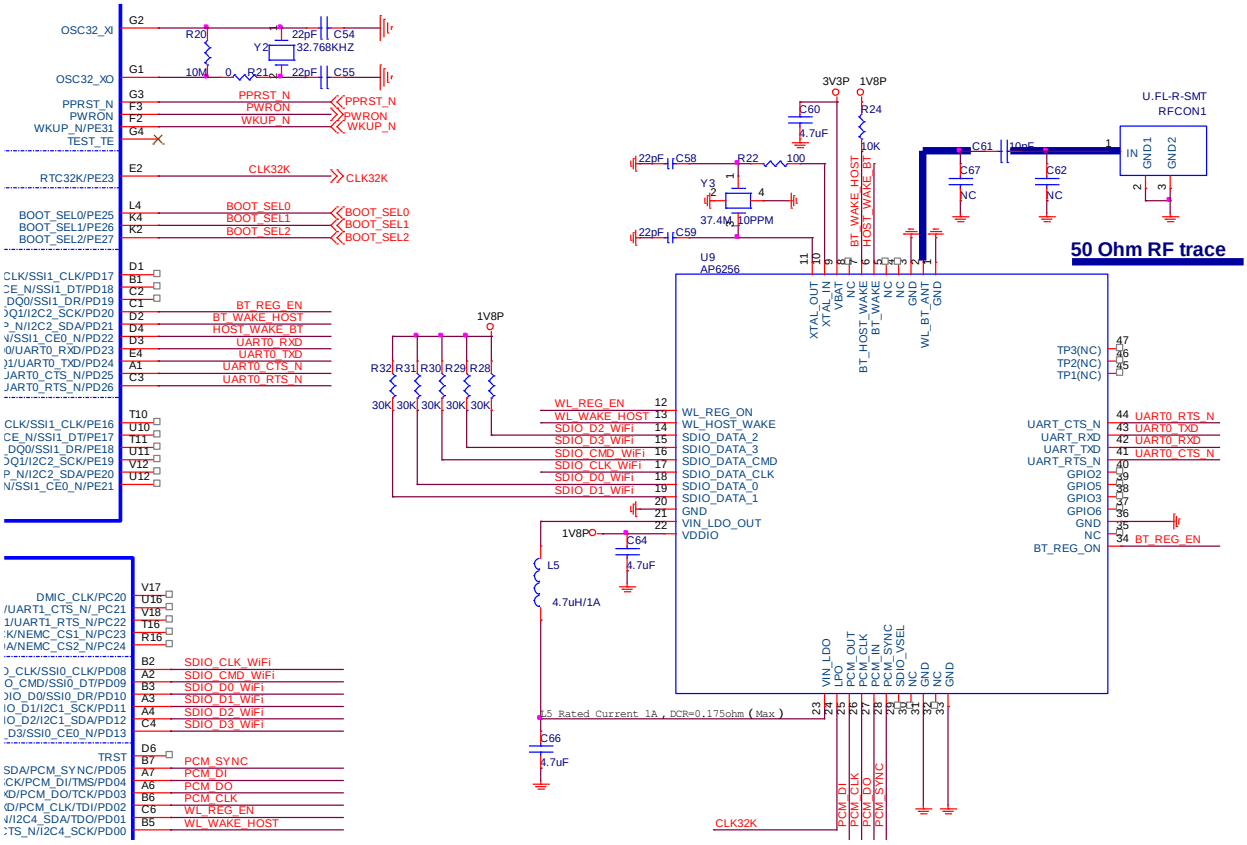

Figure 2.2.19 WIFI & BT Reference Design

2.3 PCB Design

2.3.1 PCB Layout

1. The capacitors of VDD, VDDMEM, PLL_AVDD, PLL_VDD, DDRPLL_VCCA and VREF should be placed near to those balls of CPU.
2. The placement priority of power supply decoupling capacitors:
   a) First class: PLLAVDD, PLLDVDD, DDRPLL_VCCA, VDD, VDDMEM, CODEC_VCM, VREF, DDR_VDD1.
   b) Second class: CSI_AVD09, DSI_AVD09, CSI_AVD18, DSI_AVD8, CODEC_AVDD, USB_AVD09, USB_AVD18, USB_AVD33, SADC_AVDD, VDDIO, VDDIO18, VDDIO33, VDDIO18_CIM, VDDIO33_CIM, VDDIO18_SD, VDDIO33_SD.
   c) Third class: VDDRTC, VDDIO_RTC, AVDEFUSE.
3. The potentiometer circuit of VREF should be close to X2000, and the trace should be as shorter as possible, the recommended width is 20mil, the recommended spacing is 3W.
4. It's suggested that VDD and VDDMEM have their own planes power at the power layer, in other words, please use the cooper instead of the trace.
5. It's suggested that there are enough VIAs to stitch the planes of different layers.
6. It's necessary to guarantee the integrity and continuity of plane under the CPU, so as to provide a good signal return path. Breaks in return path beneath the signal traces should be avoided at all cost. Signals crossing a plane split may cause unpredictable return path currents and would likely impact signal quality as well, potentially creating EMI problems.
7. Please pay attention to the position of power IC (DC to DC convertor and LDO) input and output capacitors. It's suggested that the input and output capacitors are placed as close to the pin of power IC as possible.

The reference layout of X2000 development board is as followed Figure 2.3.1:

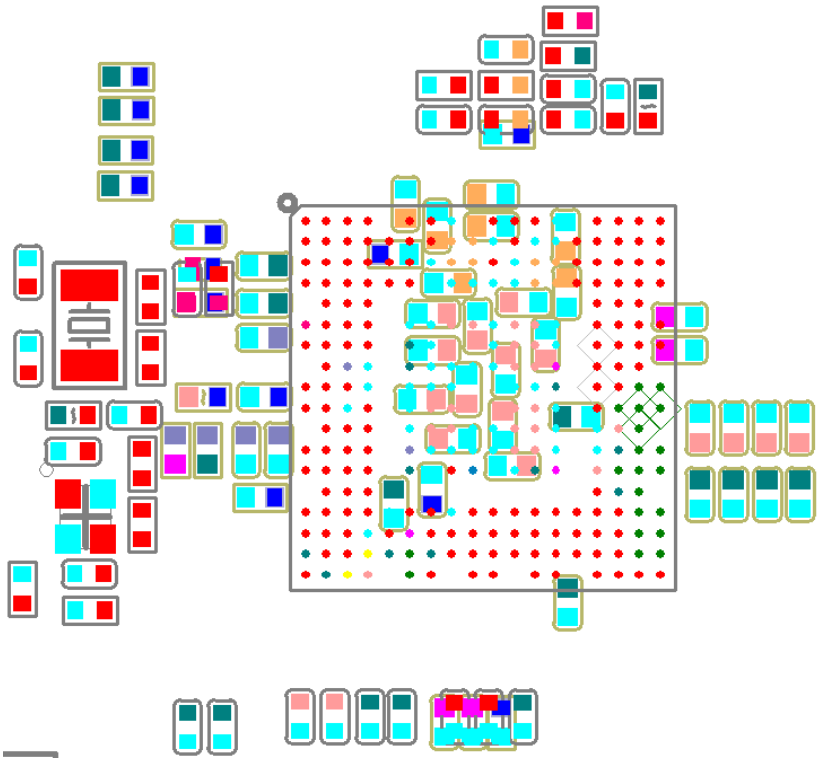

Figure 2.3.1 X2000 Power Supply Decoupling Capacitor Layout

2.3.2 PCB stack and impedance

2.3.2.1 PCB Layer Stacking

To meet signal integrity and performance requirements, at minimum a 4-layer (TOP - GND - POWER – BOTTOM) PCB should be used. See Figure 2.3.2 for the recommended layer stack ups for 4 layers boards.

Stack layer	
TOP	==================================
	PP
L2	==================================
	Core
L3	==================================
	PP
BOT	==================================

Figure 2.3.2 Recommended Layer Stack Up

2.3.2.2 Signal Traces Impedance

1. Unless mentioned otherwise, all signal traces should be 50Ω ± 10%, single ended impedance, especially antenna.

2. The differential impedance of USB signals should be set to 90Ω ±10%, and the mutation of inner and outer traces' impedance should be less than 20Ω ±10%. Within the

differential pairs, the trace lengths must run parallel to each other and matched in length. Matched lengths minimize delay differences, avoiding an increase in common-mode noise and increased EMI.

3. The differential traces audio related (includes analog mic differential signal input and analog audio differential signal output) has no requirements about impedance

4. Other differential pairs (Include MIPI_CSI, MIPI_DSI, and differential routing between Ethernet PHY chip and the transformer) should be 50Ω single-ended and 100Ω differential. Take care that the impedance is constant throughout. Impedance discontinuities cause reflections leading to EMI & signal integrity problems. Stubs must be avoided on all signal traces, especially the differential signal pairs.

2.3.3 Return Path Guidelines

1. A general best practice is to have a solid return path beneath all signal traces. This return path can be a continuous ground or DC power plane. Reducing the width of the return path width can potentially affect the impedance of the signal trace. This effect is more prominent when the width of the return path is comparable to the width of the signal trace.

2. All grounding pads should be connected to the GND layer through VIAs nearby, and have their own VIAs to connect to the ground layer, and the distance between the VIAs and pads should be as close as possible.

3. All metal pours which are not signals or power should be tied to ground. There should be no floating metal on the system. There should be no metal between the differential traces.

4. Ideally, there should be no crossover or via on the signal paths. Vias present impedance discontinuities and should be minimized. Route an entire trace pair on a single layer if possible.

   The layout of the power ground on Halley5 development board are as below.

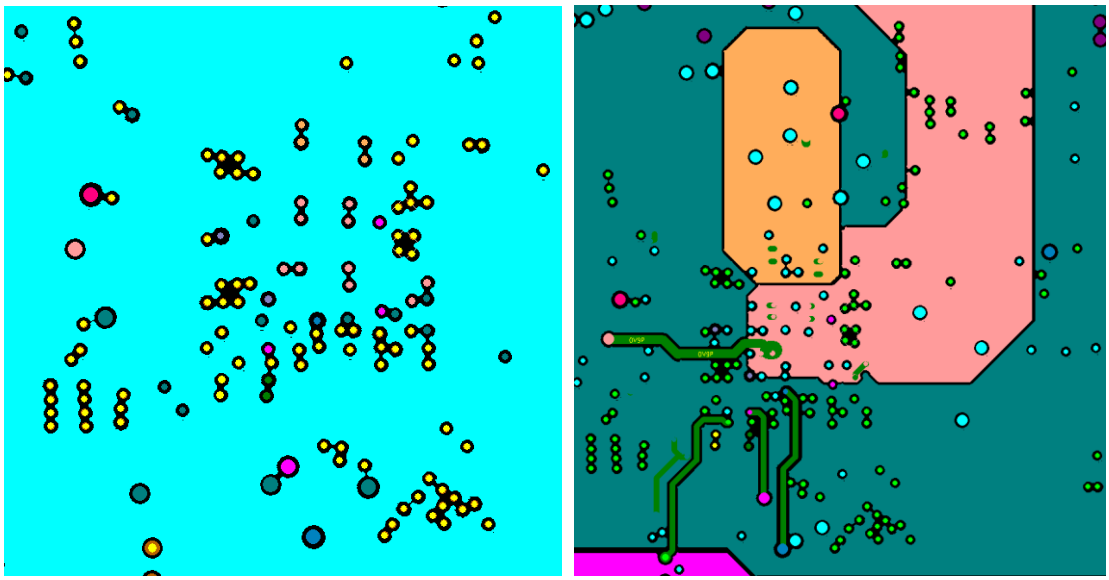

Figure 2.3.3 Diagram of Power and Ground

2.3.4 Clock Layout Guidelines

1. 24MHz and 32.768KHz crystals are recommended to be placed on the same layer as X2000, and copper is forbidden on the surface layer beneath the crystals

2. EXCLK_XI / XO and OSC32_XI / XO of X2000 are directly connected to the crystal at the surface layer. And please keep a distance from other adjacent traces by the 3W rules. The ground pad of the crystal should be connected directly to the ground layer. Do not connect with other ground on the surface layer.

3. There should be a solid metal layer running beneath the traces EXCLK_XI / XO and OSC32_XI / XO to ensure a continuous return path.

The reference layout of the clock is as below.

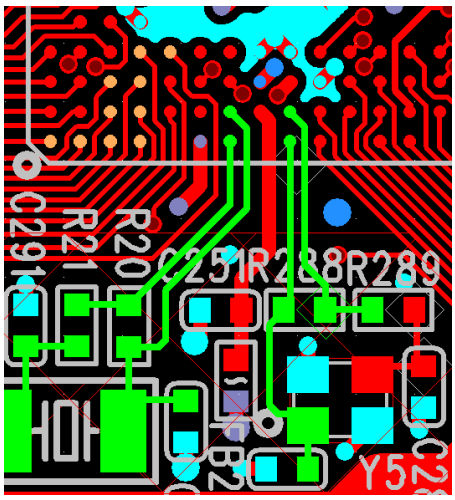

Figure 2.3.4 Layout of Clock

2.3.5 X2000 RGMII Layout Guidelines

1. RGMII signals are single-ended signals, so the traces must be routed with impedance of 50 Ω to ground.

2. Keep trace lengths as short as possible; Less than 2 inches is recommended with less than 6 inches as maximum length.

3. All Transmit signal trace lengths must match to each other and all Receive signal trace lengths must match to each other.

4. The length difference between RGMII_TXD[3:0] lines should be less than 100 mil. The length difference between RGMII_RXD[3:0] lines should be less than 100 mil. The length difference values vary with the PHY chip vendors, so check with the vendor for the recommended values.

5. All Transmit signal trace should keep 20 mil distance from all Receive signal trace.

2.3.6 MIPI signals Layout Guidelines

MIPI signals includes DSI_CLKP / N, DSI_DP0 / DN0, DSI_DP1 / DN1, RX_CLKP0 / N0,

RX_DATAP0 / N0, RX_DATAP1 / N1, RX_CLKP1 /N1, RX_DATAP2 / N2 and RX_DATAP3 / N3. MIPI DSI and MIPI CSI signals are differential signals pairs, so the differential pairs must be routed with differential impedance of 100Ω. Take care that the impedance is constant throughout. Impedance discontinuities cause reflections leading to EMI & signal integrity problems. Stubs must be avoided on all differential signal pairs.

2.3.7 Analog Signals Layout Guidelines

1. USB signals USB_DP0 and USB_DM0 are differential signal pairs, so recommends routing the differential pairs with impedance of 90Ω and a contiguous digital ground plane on the next layer. Shield the differential signal pairs with GND.
2. HPOUTP / HPOUTN, MICP / MICN are differential signal pairs, please shield the differential signal pairs with GND.

2.4 GPIO Notice

General Purpose I/O Ports (GPIO) of X2000 is used in generating and capturing application specific input and output signals. Each port can be programmed as an output, an input or function port that serves certain peripheral. As for the details of those function ports, please see the chapter 2.2 of X2000 datasheet.

Each port has internal pull up / down default state as input after reset, and the pull up / down can be enabled / disabled for the port. However, an external resistor is necessary if the control signal of peripherals outside needs a low / high state during initialization, because the pull up / down is not valid before the power of core VDD power up.

Each and the port also can be configured as level or edge tripped interrupt source to wake up X2000 from sleep mode, and every interrupt source can be masked independently. Please note that the pin of X2000 WKUP_PE31 is not a GPIO pad. There only be used the function of the PE31 for WKUP special pad, and the pin of X2000 WKUP_PE31 uses GPIO's logic to realize wakeup interrupt function with RTC module. That means WKUP_PE31 only can be input to wake up X2000 from sleep or hibernate mode. What is more, it needs an external resistor pull up to VDDIO_RTC.