

X1021

IoT Application Processor

Data Sheet

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北京君正集成电路股份有限公司
Ingenic Semiconductor Co.,Ltd.

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Data Sheet

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Ingenic Semiconductor Co., Ltd.

**Ingenic Headquarters, Zhongguancun Software Park,
Dongbeiwang West Road, Haidian District, Beijing, China,**

Tel: 86-10-56345000

Fax: 86-10-56345001

Http: [//www.ingenic.com](http://www.ingenic.com)

CONTENTS

| | | |
|----------|--|-----------|
| 1 | Overview..... | 1 |
| 1.1 | Block Diagram..... | 1 |
| 1.2 | Features..... | 1 |
| 1.2.1 | CPU | 1 |
| 1.2.2 | ISP | 2 |
| 1.2.3 | Image post processor(IPU) | 2 |
| 1.2.4 | Display(LCD) | 3 |
| 1.2.5 | Video input..... | 3 |
| 1.2.6 | Audio | 3 |
| 1.2.7 | Memory Interface | 4 |
| 1.2.8 | System Functions..... | 4 |
| 1.2.9 | Peripherals | 6 |
| 1.2.10 | Bootrom..... | 9 |
| 1.3 | Characteristic | 9 |
| 2 | Packaging and Pinout Information..... | 10 |
| 2.1 | Overview | 10 |
| 2.2 | Solder Process..... | 10 |
| 2.3 | Moisture Sensitivity Level | 10 |
| 2.4 | X1021 Package..... | 10 |
| 2.5 | Pin Description..... | 11 |
| 2.5.1 | Static Memory/DVP/I2C0..... | 11 |
| 2.5.2 | SFC | 13 |
| 2.5.3 | MSC0/GMAC/PWMx/UARTx/I2C1/JTAG/SLCD | 13 |
| 2.5.4 | MSC1/SSIO/PWMx/I2C1/GMAC/UART2/CAMERA/SLCD | 15 |
| 2.5.5 | GPIO..... | 16 |
| 2.5.6 | System..... | 17 |
| 2.5.7 | Digital IO/core power/ground..... | 17 |
| 2.5.8 | DDR power/ground..... | 18 |
| 2.5.9 | Analog - USB..... | 18 |
| 2.5.10 | Analog - SARADC | 19 |
| 2.5.11 | Analog - CODEC | 19 |
| 2.5.12 | Analog - MAC-PHY | 19 |
| 2.5.13 | Analog - EFUSE | 20 |
| 2.5.14 | Analog - CLOCK/PLL | 20 |
| 2.5.15 | Analog - RTC..... | 20 |
| 3 | Electrical Specifications | 22 |
| 3.1 | Absolute Maximum Ratings | 22 |
| 3.2 | Recommended operating conditions | 22 |
| 3.3 | Audio codec | 24 |

| | | |
|-------|--------------------------------|----|
| 3.3.1 | Microphone input | 24 |
| 3.3.2 | ALC | 24 |
| 3.3.3 | Headphone output | 25 |
| 3.3.4 | Microphone bias | 25 |
| 3.4 | MAC PHY | 25 |
| 3.5 | Power On, Reset and BOOT | 26 |
| 3.5.1 | Power-On Timing | 26 |
| 3.5.2 | Reset procedure | 28 |
| 3.5.3 | BOOT | 28 |

1 Overview

X1021 is a high performance and high integrated application processor, the application is focus on IoT devices. And it can match the requirements of many other embedded products.

1.1 Block Diagram

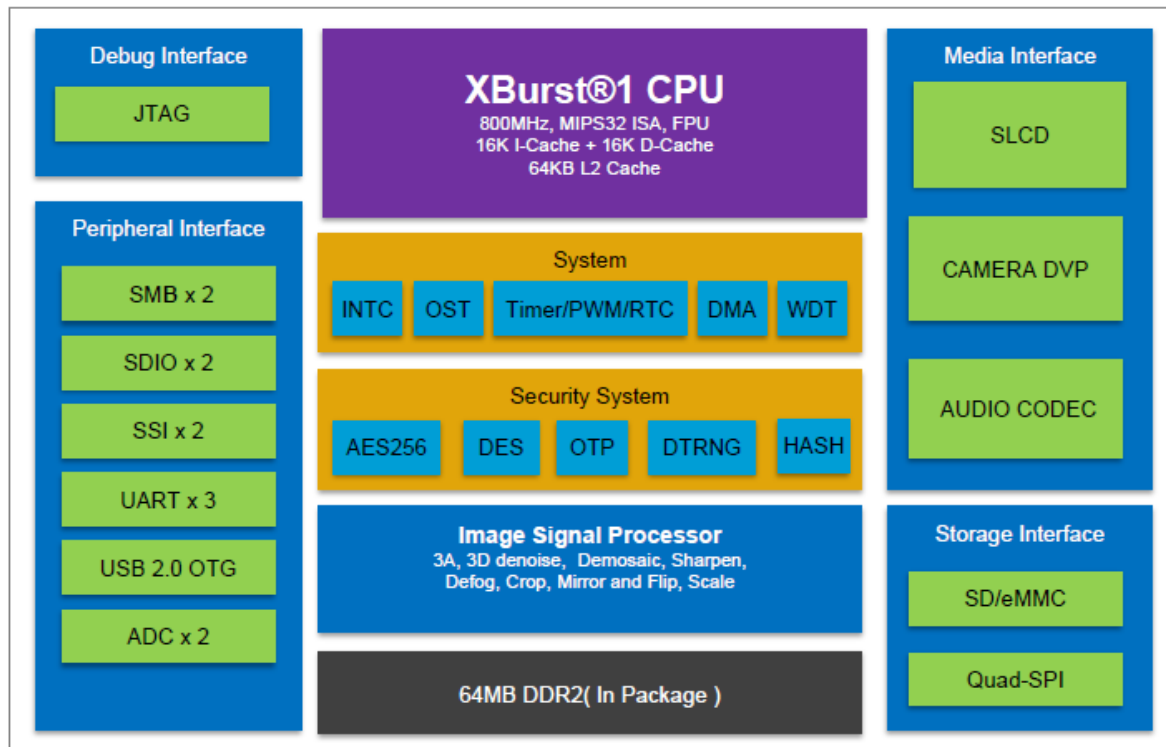


Figure 1-1 X1021 Diagram

1.2 Features

1.2.1 CPU

- XBurst®-1 core
 - XBurst® FPU instruction set supporting both single and double floating point format which are IEEE754 compatible
 - XBurst® 9-stage pipeline micro-architecture, the operating frequency is 800MHz
- MMU
 - 32-entry joint-TLB
 - 8 entry instruction TLB
 - 8 entry data TLB
- L1 Cache
 - 16kB instruction cache

- 16kB data cache
- Hardware debug support
- 16kB tight coupled memory
- L2 Cache
 - 64kB unify cache

1.2.2 ISP

- Dynamic/Static Defect Pixel Correction
- Green Equalization
- Black Level Correction
- Lens Shading Correction
- 3A(Auto Exposure/Auto White Balance/Auto Focus)
- Support Statistical Information Output(3A)
- Adaptive Dynamic Range Compression
- Demosaic
- Sharpen
- Bayer Denoise
- 2D/3D Denoise
- Color Noise Suppression
- Lens Distortion Correction
- 2D Color Correction
- 3D Color Correction
- Gamma Correction
- Defog
- 3 Independent Image Scaler and Output
- Crop, Mirror and Flip
- Support Maximum Resolution:2048x2048
- Flash timer

1.2.3 Image post processor(IPU)

- AXI Bus for data transaction
- Input data format:
 - NV12
- Output data format:
 - ARGB, RGB
 - NV12/NV21
 - HSV
- Color conversion feature: input and output format can be chosen freely from input and output data format.
- Minimum input image size (pixel): 4x4
- Maximum input image size (pixel): 2048x2048
- Minimum output image size (pixel): 4x4

- Maximum output image size (pixel): 2048x2048
- Background channel OSD function:
 - Support 4 layers OSD
 - Support whole background picture into OSD process and partial picture into OSD process
 - Support 12 port-duff OSD modes
 - Support 1 input format in background channel: NV12
 - Output picture format must be NV12

1.2.4 Display(LCD)

- Basic Features
 - Display size up to 800x600@60Hz,24BPP
 - SLCD interface 6800(type A) and 8080(type B)
- Colors Supports
 - Support up to 16,777,216 (16M) colors
- Panel Supports
 - transmit 565 by one cycle via SLCD 16bit data interface
 - transmit 666 by two cycle via SLCD 9bit data interface
 - transmit 565 by two cycle via SLCD 8bit data interface
 - transmit 888 by three cycle via SLCD 8bit data interface
 - Supports different size of display panel
 - Supports internal DMA operation and direct write register operation

1.2.5 Video input

- Support 8/10/12 bit RGB Bayer input
- Support maximum: 2688x2048 @20fps, 1080p @60fps,720p @120fps
- Support single-sensor input
- Support DVP/BT1120(serial mode)/BT656/BT601

1.2.6 Audio

- Integrated Audio codec.
 - 24 bits DAC with 93dB SNR
 - 24 bits ADC with 92dB SNR
 - Support signal-ended and differential microphone input and line input
 - Automatic Level Control (ALC) for smooth audio recording
 - Pure logic process: no need for mixed signal layers and less mask cost
 - Programmable input and output analog gains
 - Digital interpolation and decimation filter integrated
 - Sampling rate 8K/12K/16K/24K/32/44.1K/48K/96K

1.2.7 Memory Interface

- Integrated DDR on chip
- Static memory interface
 - Support 6 external chip selection CS6~1#. Each bank can be configured separately
 - The size and base address of static memory banks are programmable
 - Direct interface to 8-bit bus width external memory interface devices or external static memory to each bank. Read/Write strobe setup time and hold time periods can be programmed and inserted in an access cycle to enable connection to low-speed memory
 - Wait insertion by WAIT pin
 - Automatic wait cycle insertion to prevent data bus collisions in case of consecutive memory accesses to different banks, or a read access followed by a write access to the same bank

1.2.8 System Functions

- Clock generation and power management
 - On-chip 12/24/48MHZ oscillator circuit
 - External 32.768KHZ input
 - One three-chip phase-locked loops (PLL) with programmable multiplier
 - CCLK, HHCLK, H2CLK, PCLK, H0CLK, DDR_CLK, frequency can be changed separately for software by setting registers
 - SSI clock supports 50M clock
 - MSC clock supports 100M clock
 - Functional-unit clock gating
 - Shut down power supply for P0, ISP, IPU
- Timer and counter unit with PWM output and/or input edge counter
 - Provide eight separate channels, six of them have input signal transition edge counter
 - 16-bit A counter and 16-bit B counter with auto-reload function every channel
 - Support interrupt generation when the A counter underflows
 - Three clock sources: RTCLK (real time clock), EXCLK (external clock input), PCLK (APB Bus clock) selected with 1, 4, 16, 64, 256 and 1024 clock dividing selected
 - Every channel has PWM output
- OS timer
 - 64-bit counter and 32-bit compare register
 - Support interrupt generation when the counter matches the compare register
 - Two clock sources: RTCLK (real time clock), HCLK (system bus clock) selected with 1, 4, 16, 64, 256 and 1024 clock dividing selected
- Interrupt controller
 - Total 64 interrupt sources
 - Each interrupt source can be independently enabled
 - Priority mechanism to indicate highest priority interrupt
 - All the registers are accessed by CPU
 - Unmasked interrupts can wake up the chip in sleep mode

- Another set of source, mask and pending registers to serve for PDMA
- Watchdog timer
 - Generates WDT reset
 - A 16-bit Data register and a 16-bit counter
 - Counter clock uses the input clock selected by software
- PCLK, EXTAL and RTCCLK can be used as the clock for counter
- The division ratio of the clock can be set to 1, 4, 16, 64, 256 and 1024 by software
- Direct memory access controllers
 - Support up to 32 independent DMA channels
 - Descriptor or No-Descriptor Transfer mode compatible with previous JZ SoC
 - Transfer data units: 1-byte, 2-byte, 4-byte, 16-byte, 32-byte, 64-byte, 128-byte
 - Transfer number of data unit: $1 \sim 2^{24} - 1$
 - Independent source and destination port width: 8-bit, 16-bit, 32-bit
 - Fixed three priorities of channel groups: 0~3, highest; 4~11: mid; 12~31: lowest
 - An extra INTC IRQ can be bound to one programmable DMA channel
- SAR A/D Controller
 - 2 Channels
 - Resolution: 10-bit
 - Integral nonlinearity: ± 1 LSB
 - Differential nonlinearity: ± 0.5 LSB
 - Resolution/speed: up to 2MSPS
 - Max Frequency: 24MHz
 - Low power dissipation: 1.5mW(worst)
 - Support multi-touch detect
 - Support write control command by software
 - Single-end and Differential Conversion Mode
 - Support external touch screen controller
 - Pin Description
- RTC (Real Time Clock)
 - Need external 32768Hz oscillator for 32k clock generation
 - 32-bits second counter
 - Programmable and adjustable counter to generate accurate 1 Hz clock
 - Alarm interrupt, 1Hz interrupt
 - Stand alone power supply, work in hibernating mode
 - Power down controller
 - Alarm wakeup
 - External pin wakeup with up to 2s glitch filter
- OTP Slave Interface
 - Total 2048 bits. Lower 192bits are read only, other higher bits are read-able and write-able

1.2.9 Peripherals

- General-Purpose I/O ports
 - Each port can be configured as an input, an output or an alternate function port
 - Each port can be configured as an interrupt source of low/high level or rising/falling edge triggering. Every interrupt source can be masked independently
 - Each port has an internal pull-up or pull-down resistor connected. The pull-up/down resistor can be disabled
 - GPIO output 3 interrupts, each interrupt corresponds to the group, to INTC
- SMB Controller
 - Two-wire SMB serial interface – consists of a serial data line (SDA) and a serial clock (SCL)
 - Two speeds
 - Standard mode (100 Kb/s)
 - Fast mode (400 Kb/s)
 - Device clock is identical with pclk
 - Programmable SCL generator
 - Master or slave SMB operation
 - 7-bit addressing/10-bit addressing
 - 16-level transmit and receive FIFOs
 - Interrupt operation
 - The number of devices that you can connect to the same SMB-bus is limited only by the maximum bus capacitance of 400pF
 - APB interface
 - 2 independent SMB channels (SMB0, SMB1)
- One High Speed Synchronous serial interfaces (SFC)
 - 3 protocols support: National's Microwire, TI's SSP, and Motorola's SPI
 - transmit-only or receive-only operation
 - MSB first for command and data transfer, and LSB first for address transfer
 - 64 entries x 32 bits wide data FIFO
 - one device select
 - Configurable sampling point for reception
 - Configurable timing parameters: tSLCH, tCHSH and tSHSL
 - Configurable flash address wide are supported
 - 7 transfer formats: Standard SPI, Dual-Output/Dual-Input SPI, Quad-Output/Quad-Input SPI, Dual-I/O SPI, Quad-I/O SPI, Full Dual-I/O SPI, Full Quad-I/O SPI
 - two data transfer mode: slave mode and DMA mode
 - Configurable 6 phases for software flow
- Two Normal Speed Synchronous serial interfaces (SSI0, SSI1)
 - 3 protocols support: National's Microwire, TI's SSP, and Motorola's SPI
 - Full-duplex or transmit-only or receive-only operation

- Programmable transfer order: MSB first or LSB first
- 128 entries deep x 32 bits wide transmit and receive data FIFOs
- Configurable normal transfer mode or Interval transfer mode
- Programmable clock phase and polarity for Motorola's SSI format
- Two slave select signal (SSI_CE_ / SSI_CE2_) supporting up to 2 slave devices
- Back-to-back character transmission/reception mode
- Loop back mode for testing
- Three UARTs (UART0, UART1, UART2)
 - Full-duplex operation
 - 5-, 6-, 7- or 8-bit characters with optional no parity or even or odd parity and with 1, 1½, or 2 stop bits
 - 64x8 bit transmit FIFO and 64x11bit receive FIFO
 - Independently controlled transmit, receive (data ready or timeout), line status interrupts
 - Internal diagnostic capability Loopback control and break, parity, overrun and framing-error is provided
 - Separate DMA requests for transmit and receive data services in FIFO mode
 - Supports modem flow control by software or hardware
 - Slow infrared asynchronous interface that conforms to IrDA specification
- Two MMC/SD/SDIO controllers (MSC0, MSC1)
 - Fully compatible with the MMC System Specification version 4.2
 - Support SD Specification 3.0
 - Support SD I/O Specification 1.0 with 1 command channel and 4 data channels
 - Consumer Electronics Advanced Transport Architecture (CE-ATA – version 1.1)
 - Maximum data rate is 50MBps
 - Support MMC data width 1bit ,4bit and 8bit
 - Built-in programmable frequency divider for MMC/SD bus
 - Built-in Special Descriptor DMA
 - Maskable hardware interrupt for SDIO interrupt, internal status and FIFO status
 - 128 x 32 built-in data FIFO
 - Multi-SD function support including multiple I/O and combined I/O and memory
 - IRQ supported enable card to interrupt MMC/SD controller
 - Single or multi block access to the card including erase operation
 - Stream access to the MMC card
 - Supports SDIO read wait, interrupt detection during 1-bit or 4-bit access
 - Supports CE-ATA digital protocol commands
 - Support Command Completion Signal and interrupt to CPU
 - Command Completion Signal disable feature
 - The maximum block length is 4096bytes
- USB 2.0 OTG interface
 - Complies with the USB 2.0 standard for high-speed (480 Mbps) functions and with the

- On-The-Go supplement to the USB 2.0 specification
 - Operates either as the function controller of a high- /full-speed USB peripheral or as the host/peripheral in point-to-point or multi-point communications with other USB functions
 - Supports Session Request Protocol (SRP) and Host Negotiation Protocol (HNP)
 - UTMI+ Level 3 Transceiver Interface
 - Soft connect/disconnect
 - 16 Endpoints
 - Dedicate FIFO
 - Supports control, interrupt, ISO and bulk transfer
- Ethernet Media Access controller and interface
 - 10, 100Mbps data transfer rates with the following PHY interfaces:
 - RMII interface to communicate with an external Fast Ethernet PHY
 - RMII PHY integrated
 - Full-duplex operation:
 - IEEE 802.3x flow control automatic transmission of zero-quantum Pause frame on flow control input de-assertion
 - forwarding of received Pause frames to the user application
 - Half-duplex operation:
 - CSMA/CD Protocol support
 - Frame bursting and frame extension in 100 Mbps half-duplex operation
 - Preamble and start of frame data (SFD) insertion in Transmit path
 - Preamble and SFD deletion in the Receive path
 - Automatic CRC and pad generation controllable on a per-frame basis
 - Automatic Pad and CRC Stripping options for receive frames
 - Flexible address filtering modes, such as:
 - Up to 31 additional 48-bit perfect (DA) address filters with masks for each byte
 - 64-bit Hash filter for multicast and unicast (DA) addresses
 - Option to pass all multicast addressed frames
 - Promiscuous mode to pass all frames without any filtering for network monitoring
 - Pass all incoming packets (as per filter) with a status report
 - Support Standard or Jumbo Ethernet frames with up to 2 KB of size
 - IEEE 802.1Q VLAN tag detection for reception frames
 - MDIO master interface for PHY device configuration and management
 - CRC replacement, Source Address field insertion or replacement, and VLAN insertion, replacement, and deletion in transmitted frames with per-frame control
 - Programmable watchdog timeout limit in the receive path
 - Detect remote wake-up frames and AMD magic packets
- Digital True Random Number Generator (DTRNG)
 - Pure digital logic circuits
 - True random number
 - Interrupt mode and no interrupt mode

1.2.10 Bootrom

32kB Boot ROM memory

1.3 Characteristic

| Item | Characteristic |
|----------------------|--|
| Process Technology | 28nm CMOS low power |
| Power supply voltage | General purpose I/O: 1.5~3.6V DDR I/O: DDR2 $\pm 0.1V$ RTC I/O: 1.5V~3.6V EFUSE programming: 1.5V $\pm 10\%$ Analog power supply 1: 1.8V $\pm 10\%$ Analog power supply 2: 3.3V $\pm 10\%$ Core: 1.0V $\pm 0.1V$ |
| Package | BGA152 9mm x 9mm x 1.22mm, 0.65mm pitch |
| Operating frequency | 800MHz |

2 Packaging and Pinout Information

2.1 Overview

X1021 processor is offered in 152-pin BGA package, which is 9mm x 9mm x 1.22mm outline, 10 x 10 matrix ball grid array and 0.65mm ball pitch, show in Figure 2-1. The X1021 pin to ball assignment is show in Figure 2-2. The detailed pin description is listed in Table 2-1 ~ Table 2-16.

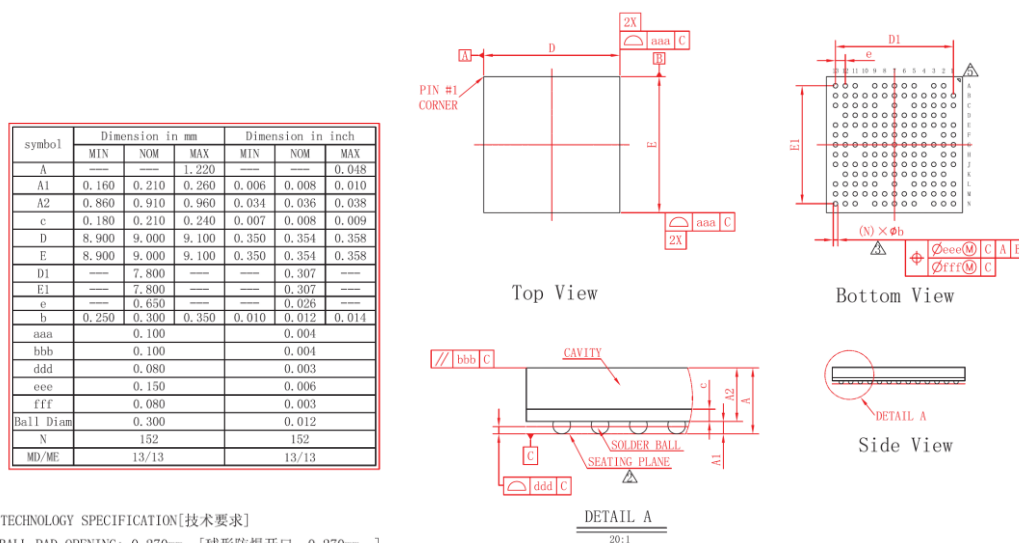
2.2 Solder Process

X1021 package is lead-free. It's reflow profile follows the IPC/JEDEC lead-free reflow profile as contained in [J-STD-020C](#).

2.3 Moisture Sensitivity Level

X1021 package moisture sensitivity is level 3.

2.4 X1021 Package



TECHNOLOGY SPECIFICATION[技术要求]

1. BALL PAD OPENING: 0.270mm; [球形防焊开口: 0.270mm;]

△ PRIMARY DATUM C AND SEATING PLANE ARE THE SOLDER BALLS;

[主要基准C和底面是锡球;]

△ DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C; [尺寸b是测量最大锡球直径, 平行于主要基准C;]

4. SPECIAL CHARACTERISTICS C CLASS: bbb, ddd; [特殊特性C类: bbb, ddd;]

△ THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY;

[PIN 1 标识仅供参考;]

6. BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES OF JCET PRESCRIBING;

[禁止使用长电科技规定的一级环境管理物质;]


| | | | | | | | | | | |
|--|--------|------|--------------------------|--|---|--|----------------|---------|----------------|--|
| | | | PROJECTION | |  | | SIGNATURE AREA | DESIGN | | |
| | | | | | | | | CHECK | | |
| TITLE: PACKAGE OUTLINE DRAWING (7-68-04-0010) | | | DRAWING NO. | | REV. | | | A00 | DESIGN APPROVE | |
| BGA-(9x9)-152 (PD. 65 T1.22) | | | DPO-AA-990-0152-00-00 | | | | | | PROCESS | |
| | | | GGP3.508.XXXXXX | | | | | | | |
| SIZE | PAGE | UNIT | DIMENSION AND TOLERANCES | | | | SCALE | STAND. | | |
| A3 | 1 OF 1 | MM | ASME Y14.5M | | | | 5:1 | APPROVE | | |

Figure 2-1 X1021 package outline drawing

| X1021 Ball Assignment Ver1.4 | | | | | | | | | | | | | | |
|------------------------------|--|-------------------|---|--|--|---|--|--|--|--|--|---|---|---|
| | BGA152, 9mm X 9mm X1.22mm, 0.65pitch, top view | | | | | | | | | | | | | |
| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | |
| A | | MSC0_D0_P B00 | UART0_RXD _TDI_PB19 | | UART1_RXD _TMS_PB24 | SMB1_SDA _PB25 | DDR_PLLVC CD | SSIO_CE0_P WM5_UART 2_RXD_PC1 4 | SSIO_CE1_U ART2_RXD _SMB1_SCK _SLCD_CS_P C09 | | MSC1_D3_M AC_LED_RX _SLCD_D5 _PC07 | MSC1_CLK MAC_LED_S PEED100_S LCD_D0_PC 02 | MSC1_D1_M AC_LED_DU PLEX_SLCD _D3_PC05 | A |
| B | MSC0_D3_P B03 | MSC0_CLK _PB04 | MSC0_D1_P B01 | UART0_CTS _PB20 | UART1_TXD _TCK_PB23 | SMB1_SCK _PB26 | DDR_PLLVC CA | SSIO_CLK_P WM4_UART 2_TXD_PC1 3 | SSIO_DR_P WM2_UART 2_CTS_PC1 1 | SSIO_GPC UART2_TXD _SMB1_SDA _SLCD_DC _PC08 | MSC1_CMD MAC_LED _TX_SLCD_D 1_PC03 | SFC_GPC_P A25 | SFC_CLK_P A27 | B |
| C | BOOT_SEL1 _PC01 | MSC0_D2_P B02 | MSC0_CMD _PB05 | UART0_TXD _TDO_PB22 | UART0_RTS _PB21 | | VREF | | SSIO_DT_P WM3_UART 2_RTS_PC1 2 | MSC1_D2_M AC_LED_LIN K_SLCD_D4 _PC06 | MSC1_D0_M AC_LED_SP EED10_SLC D_D2_PC04 | SFC_DT_PA 23 | SFC_CE1_P A26 | C |
| D | | PLL_VDDA | BOOT_SEL0 _PC00 | TRST | VDDMEM | VDDMEM | VDDMEM | VDDMEM | CLK32K_OU T_PWM7_SL CD_TE_PC1 6 | PWM6_SLC D_WR_PC1 5 | SFC_DR_PA 24 | SFC_CE0_P A28 | | D |
| E | EXCLK_XI | EXCLK_XO | RTC_VDD | RST_DELAY | DDRVD | DDRVD | DDRVD | DDRVD | PWM1_FL SH_OUT_UA RT2_RTS_S LCD_D7_PC 18 | PWM0_FL SH_STORB E_IN_UART 2_CTS_SLC D_D6_PC17 | WAIT_PA22 | GPIO_PA18 | RD_SMB0_S CK_PA13 | E |
| F | OSC32_XI | OSC32_XO | | AVDEFUSE | VSSMEM | VSSMEM | VSSMEM | VSSMEM | VSSMEM | VDDIO2 | | CS2_SMB0 _SDA_PA12 | DVP_VSYNC _PA17 | F |
| G | RTC_VDDIO | PPRST_ | AUX0 | TEST_TE | DDRVS | DDRVS | DDRVS | DDRVS | DDRVS | VDDIO2 | DVP_MCLK _PA15 | DVP_HSYN C_PA16 | DVP_PCLK _PA14 | G |
| H | AUX1 | SADC_VREF P | | WKUP_PA30 | VSS | VSS | VSS | VSS | VSS | VDDIO0 | | SA2_DVP_D 10_PA10 | CS1_DVP_D 11_PA11 | H |
| J | SADC_AV D | USB0PN | USB0PP | VSS | VSS | VDD | VDD | VDD | VDD | VDDIO0 | SD7_DVP_D 7_PA07 | SA0_DVP_D 8_PA08 | SA1_DVP_D 9_PA09 | J |
| K | | USB_VCC33 | USB_VCC18 | VSS | VDD | VDD | VDD | VDD | VDDIO1 | VDDIO1 | SD5_DVP_D 5_PA05 | SD6_DVP_D 6_PA06 | | K |
| L | USB_VCC10 | MICN | MICBIAS | GMAC_MDC K_SS11_CLK _LINK_SLCD _D4_PB10 | GMAC_RXD 0_MAC_LED _LINK_SLCD _WR_PB15 | | SLCD_RDY_ PB28 | | MAC_TXN | MAC_RXN | MAC_VDDA | SD3_DVP_D 3_PA03 | SD4_DVP_D 4_PA04 | L |
| M | MICP | VCM | DRV_VBUS _PB27 | GMAC_RXD V_SS11_DR _SLCD_D3_P B09 | GMAC_RXD 1_MAC_LED _RX_SLCD_ TE_PB16 | GMAC_PHY _CLK_MAC_ LED_TX_SL CD_D1_PB7 | GMAC_TXD 1_SS11_CE1 _MAC_LED_ DUPLEX_SL CD_D7_PB1 4 | PWM0_SLC D_CS_PB17 | MAC_TXP | MAC_RXP | MAC_EXTR ES | SD1_DVP_D 1_PA01 | SD2_DVP_D 2_PA02 | M |
| N | HPOUT | CODEC_AV DD | GMAC_MDI O_SS11_CE0 _SLCD_D5_ PB11 | | GMAC_TXC LK_MAC_LE D_SPEED10 0_SLCD_D0 _PB06 | GMAC_TXD 0_SS11_GPC _MAC_LED_ SPEED10_S LCD_D6_PB 12 | GMAC_TXE N_SS11_DT _SLCD_D2_P B08 | PWM1_SLC D_DC_PB18 | GPIO_PB31 | | MAC_TEST_ ATP | MAC_VDDH V | SD0_DVP_D 0_PA00 | N |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | |

Figure 2-2 X1021 pin to ball assignment

2.5 Pin Description

2.5.1 Static Memory/DVP/I2C0

Table 2-1 Static Memory/DVP/I2C0 Pins(19)

| Pin Names | IO | Loc | IO Cell Char. | Pin Description | Power |
|-----------------------|---------------|-----|---------------|---|--------|
| SD0 DVP_D0 PA00 | IO I IO | N13 | 8mA | SD0: Static memory data bus bit 0 DVP_D0:DVP data bit 0 PA00: GPIO group A bit 00 | VDDIO0 |

| Pin Names | IO | Loc | IO Cell Char. | Pin Description | Power |
|-------------------------|---------------|-----|----------------------------------|---|--------|
| SD1 DVP_D1 PA01 | IO I IO | M12 | 8mA | SD1: Static memory data bus bit 1 DVP_D1:DVP data bit 1 PA01: GPIO group A bit 01 | VDDIO0 |
| SD2 DVP_D2 PA02 | IO I IO | M13 | 8mA | SD2: Static memory data bus bit 2 DVP_D2:DVP data bit 2 PA02: GPIO group A bit 02 | VDDIO0 |
| SD3 DVP_D3 PA03 | IO I IO | L12 | 8mA | SD3: Static memory data bus bit 3 DVP_D3:DVP data bit 3 PA03: GPIO group A bit 03 | VDDIO0 |
| SD4 DVP_D4 PA04 | IO I IO | L13 | 8mA | SD4: Static memory data bus bit 4 DVP_D4:DVP data bit 4 PA04: GPIO group A bit 04 | VDDIO0 |
| SD5 DVP_D5 PA05 | IO I IO | K11 | 8mA | SD5: Static memory data bus bit 5 DVP_D5:DVP data bit 5 PA05: GPIO group A bit 05 | VDDIO0 |
| SD6 DVP_D6 PA06 | IO I IO | K12 | 8mA | SD6: Static memory data bus bit 6 DVP_D6:DVP data bit 6 PA06: GPIO group A bit 06 | VDDIO0 |
| SD7 DVP_D7 PA07 | IO I IO | J11 | 8mA | SD7: Static memory data bus bit 7 DVP_D7:DVP data bit 7 PA07: GPIO group A bit 07 | VDDIO0 |
| SA0 DVP_D8 PA08 | O I IO | J12 | 8mA | SA0: Static memory address bus bit 0 DVP_D8:DVP data bit 8 PA08: GPIO group A bit 08 | VDDIO0 |
| SA1 DVP_D9 PA09 | O I IO | J13 | 8mA | SA1: Static memory address bus bit 1 DVP_D9: DVP data bit 9 PA09: GPIO group A bit 09 | VDDIO0 |
| SA2 DVP_D10 PA10 | O I IO | H12 | 8mA | SA2: Static memory address bus bit 2 DVP_D10: DVP data bit 10 PA10: GPIO group A bit 10 | VDDIO0 |
| CS1 DVP_D11 PA11 | O I IO | H13 | 8mA Pullup-rst | CS1: Static memory chip 1 select DVP_D11: DVP data bit 11 PA11: GPIO group A bit 11 | VDDIO0 |
| CS2 SMB0_SDA PA12 | O IO IO | F12 | 8mA Pullup-rst | CS2: Static memory chip 2 select SMB0_SDA: I2C 0 serial data PA12: GPIO group A bit 12 | VDDIO0 |
| RD SMB0_SCK PA13 | O IO IO | E13 | 8mA Pullup-rst | RD: Static memory read signal SMB0_SCK: I2C 0 serial clock PA13: GPIO group A bit 13 | VDDIO0 |
| DVP_PCLK PA14 | I IO | G13 | 8mA | DVP_PCLK: camera sensor pixel clock input PA14: GPIO group A bit 14 | VDDIO0 |
| DVP_MCLK PA15 | O IO | G11 | 8mA Slew-rate-rst | DVP_MCLK: DVP main clock output PA15: GPIO group A bit 15 | VDDIO0 |
| DVP_HSYNC PA16 | I IO | G12 | 8mA | DVP_HSYNC: DVP horizontal sync PA16: GPIO group A bit 16 | VDDIO0 |
| DVP_VSYNC PA17 | I IO | F13 | 8mA | DVP_VSYNC: DVP vertical sync PA17: GPIO group A bit 17 | VDDIO0 |
| WAIT PA22 | O IO | E11 | 8mA Pullup-rst Schmitt-rst | WAIT: Slow static memory/device wait signal PA22: GPIO group A bit 22 | VDDIO0 |

2.5.2 SFC

Table 2-2 SFC Pins(6)

| Pin Names | IO | Loc | IO Cell Char. | Pin Description | Power |
|-----------------|----------|-----|-------------------|--|--------|
| SFC_DT PA23 | IO IO | C12 | 8mA Pullup-rst | SFC_DT: high speed ssi transmit data PA23: GPIO group A bit 23 | VDDIO1 |
| SFC_DR PA24 | IO IO | D11 | 8mA Pullup-rst | SFC_DR: high speed ssi receive data PA24: GPIO group A bit 24 | VDDIO1 |
| SFC_GPC PA25 | IO IO | B12 | 8mA Pullup-rst | SFC_GPC: high speed ssi general-purpose control PA25: GPIO group A bit 25 | VDDIO1 |
| SFC_CE1 PA26 | IO IO | C13 | 8mA Pullup-rst | SFC_CE1: high speed ssi chip 1 select PA26: GPIO group A bit 26 | VDDIO1 |
| SFC_CLK PA27 | O IO | B13 | 8mA Pullup-rst | SFC_CLK: high speed ssi clock PA27: GPIO group A bit 27 | VDDIO1 |
| SFC_CE0 PA28 | O IO | D12 | 8mA Pullup-rst | SFC_CE0: high speed ssi chip 0 select PA28: GPIO group A bit 28 | VDDIO1 |

2.5.3 MSC0/GMAC/PWMx/UARTx/I2C1/JTAG/SLCD

Table 2-3 MSC0/GMAC/PWMx/UARTx/I2C1/JTAG/SLCD (28)

| Pin Names | IO | Loc | IO Cell Char. | Pin Description | Power |
|---|-------------------|-----|---------------|---|--------|
| MSC0_D0 PB00 | IO IO | A2 | 8mA | MSC0_D0: MSC (MMC/SD) 0 data bit 0 PB00: GPIO group B bit 00 | VDDIO1 |
| MSC0_D1 PB01 | IO IO | B3 | 8mA | MSC0_D1: MSC (MMC/SD) 0 data bit 1 PB01: GPIO group B bit 01 | VDDIO1 |
| MSC0_D2 PB02 | IO IO | C2 | 8mA | MSC0_D2: MSC (MMC/SD) 0 data bit 2 PB02: GPIO group B bit 02 | VDDIO1 |
| MSC0_D3 PB03 | IO IO | B1 | 8mA | MSC0_D3: MSC (MMC/SD) 0 data bit 3 PB03: GPIO group B bit 03 | VDDIO1 |
| MSC0_CLK PB04 | O IO | B2 | 8mA | MSC0_CLK: MSC (MMC/SD) 0 clock output PB04: GPIO group B bit 04 | VDDIO1 |
| MSC0_CMD PB05 | IO IO | C3 | 8mA | MSC0_CMD: MSC (MMC/SD) 0 command PB05: GPIO group B bit 05 | VDDIO1 |
| GMAC_TXCLK MAC_LED_SPEE D100 SLCD_D0 PB06 | I O O IO | N5 | 8mA | GMAC_TXCLK: gmac transmitting clock MAC_LED_SPEED100: speed100 indication SLCD_D0: smart lcd data output bit 0 PB06: GPIO group B bit 06 | VDDIO1 |
| GMAC_PHY_CLK MAC_LED_TX SLCD_D1 PB07 | O O O IO | M6 | 8mA | GMAC_PHY_CLK: gmac phy clock MAC_LED_TX: TX activity indication SLCD_D1: smart lcd data output bit 1 PB07: GPIO group B bit 07 | VDDIO1 |
| GMAC_TXEN SSI1_DT SLCD_D2 PB08 | O O O IO | N7 | 8mA | GMAC_TXEN: gmac transmitting enable SSI1_DT: normal speed ssi 1 transmit data SLCD_D2: smart lcd data output bit 2 PB08: GPIO group B bit 08 | VDDIO1 |
| GMAC_RXDV SSI1_DR | I I | M4 | 8mA | GMAC_RXDV: gmac receive data valid SSI1_DR: normal speed ssi 1 receive data | VDDIO1 |

| Pin Names | IO | Loc | IO Cell Char. | Pin Description | Power |
|---|-----------------------------|-----|---------------------|--|--------|
| SLCD_D3 PB09 | O IO | | | SLCD_D3: smart lcd data output bit 3 PB09: GPIO group B bit 09. | |
| GMAC_MDCK SSI1_CLK SLCD_D4 PB10 | O O O IO | L4 | 8mA Pulldown-rst | GMAC_MDCK: gmac manage data clock SSI1_CLK: normal speed ssi 1 clock SLCD_D4: smart lcd data output bit 4 PB10: GPIO group B bit 10. | VDDIO1 |
| GMAC_MDIO SSI1_CE0 SLCD_D5 PB11 | IO O O IO | N3 | 8mA Pullup-rst | GMAC_MDIO: gmac MDIO which is clocked by MDC SSI1_CE0: normal speed ssi 1 chip 0 select SLCD_D5: smart lcd data output bit 5 PB11: GPIO group B bit 11. | VDDIO1 |
| GMAC_TXD0 SSI1_GPC MAC_LED_SPEE D10 SLCD_D6 PB13 | O O O O O IO | N6 | 8mA | GMAC_TXD0: gmac transmit data bit 0 SSI1_GPC: normal speed ssi 1 general-purpose control MAC_LED_SPEED10: PHY speed10 indication SLCD_D6: smart lcd data output bit 6 PB13: GPIO group B bit 13. | VDDIO1 |
| GMAC_TXD1 SSI1_CE1 MAC_LED_DUPL EX SLCD_D7 PB14 | O O O O O IO | M7 | 8mA Pullup-rst | GMAC_TXD1: gmac transmit data bit 1 SSI1_CE1: normal speed ssi 1 chip 1 select MAC_LED_DUPLEX: PHY duplex indication SLCD_D7: smart lcd data output bit 7 PB14: GPIO group B bit 14. | VDDIO1 |
| GMAC_RXD0 MAC_LED_LINK SLCD_WR PB15 | I O O O IO | L5 | 8mA | GMAC_RXD0: gmac receive data bit 0 MAC_LED_LINK: PHY link ON indication SLCD_WR: smart lcd write data control PB15: GPIO group B bit 15. | VDDIO1 |
| GMAC_RXD1 MAC_LED_RX SLCD_TE PB16 | I O I IO | M5 | 8mA | GMAC_RXD1: gmac receive data bit 1 MAC_LED_RX: PHY RX activity indication SLCD_TE: smart lcd crack control PB16: GPIO group B bit 16. | VDDIO1 |
| PWM0 SLCD_CS PB17 | O O O IO | M8 | 8mA Pullup-rst | PWM0: PWM channel 0 output SLCD_CS: smart lcd chip select PB17: GPIO group B bit 17. | VDDIO1 |
| PWM1 SLCD_DC PB18 | O O O IO | N8 | 8mA Pulldown-rst | PWM1: PWM channel 1 output SLCD_DC: smart lcd cmd/data identify PB18: GPIO group B bit 18. | VDDIO1 |
| UART0_RXD TDI PB19 | I I IO | A3 | 8mA Pullup-rst | UART0_RXD: UART 0 receive data TDI: JTAG data input PB19: GPIO group B bit 19 | VDDIO1 |
| UART0_CTS PB20 | I IO | B4 | 8mA | UART0_CTS: UART 0 clear-to-send handshaking PB20: GPIO group B bit 20 | VDDIO1 |
| UART0_RTS PB21 | O IO | C5 | 8mA | UART0_RTS: UART 0 request-to-send handshaking PB21: GPIO group B bit 21 | VDDIO1 |
| UART0_TXD TDO PB22 | O O IO | C4 | 8mA | UART0_TXD: UART 0 transmit data TDO: JTAG data output PB22: GPIO group B bit 22 | VDDIO1 |
| UART1_TXD | O | B5 | 8mA | UART1_TXD: UART 1 transmit data | VDDIO1 |

| Pin Names | IO | Loc | IO Cell Char. | Pin Description | Power |
|--------------------------|--------------|-----|--------------------|--|--------|
| TCK PB23 | I IO | | | TCK: JTAG clock input PB23: GPIO group B bit 23 | |
| UART1_RXD TMS PB24 | I I IO | A5 | 8mA Pullup-rst | UART1_RXD: UART 1 receive data TMS: JTAG mode select PB24: GPIO group B bit 24 | VDDIO1 |
| SMB1_SDA PB25 | IO IO | A6 | 8mA Pullup-rst | SMB1_SDA: I2C 1 serial data PB25: GPIO group B bit 25 | VDDIO1 |
| SMB1_SCK PB26 | IO IO | B6 | 8mA Pullup-rst | SMB1_SCK: I2C 1 serial clock PB26: GPIO group B bit 26 | VDDIO1 |
| DRV_VBUS PB27 | O IO | M3 | 8mA Schmitt-rst | DRV_VBUS: USB-5V control PB27: GPIO group B bit 27 | VDDIO1 |
| SLCD_RDY PB28 | I IO | L7 | 8mA Schmitt-rst | SLCD_RDY: smart lcd work status PB28: GPIO group B bit 28 | VDDIO1 |

2.5.4 MSC1/SSIO/PWMx/I2C1/GMAC/UART2/CAMERA/SLCD

Table 2-4 MSC1/SSIO/PWMx/I2C1/GMAC/UART2/CAMERA/SLCD Pins (16)

| Pin Names | IO | Loc | IO Cell Char. | Pin Description | Power |
|---|--------------------|-----|---------------|---|--------|
| MSC1_CLK MAC_LED_SPE ED100 SLCD_D0 PC02 | O O O IO | A12 | 8mA | MSC1_CLK: MSC (MMC/SD) 1 clock output MAC_LED_SPEED100: speed100 indication SLCD_D0: smart lcd data output bit 0 PC02: GPIO group C bit 02 | VDDIO2 |
| MSC1_CMD MAC_LED_TX SLCD_D1 PC03 | IO O O IO | B11 | 8mA | MSC1_CMD: MSC (MMC/SD) 1 command MAC_LED_TX: TX activity indication SLCD_D1: smart lcd data output bit 1 PC03: GPIO group C bit 03 | VDDIO2 |
| MSC1_D0 MAC_LED_SPE ED10 SLCD_D2 PC04 | IO O O IO | C11 | 8mA | MSC1_D0: MSC (MMC/SD) 1 data bit 0 MAC_LED_SPEED10: speed10 indication SLCD_D2: smart lcd data output bit 2 PC04: GPIO group C bit 04 | VDDIO2 |
| MSC1_D1 MAC_LED_DUP LEX SLCD_D3 PC05 | IO O O IO | A13 | 8mA | MSC1_D1: MSC (MMC/SD) 1 data bit 1 MAC_LED_DUPLEX: duplex indication SLCD_D3: smart lcd data output bit 3 PC05: GPIO group C bit 05 | VDDIO2 |
| MSC1_D2 MAC_LED_LINK SLCD_D4 PC06 | IO O O IO | C10 | 8mA | MSC1_D2: MSC (MMC/SD) 1 data bit 2 MAC_LED_LINK: link ON indication SLCD_D4: smart lcd data output bit 4 PC06: GPIO group C bit 06 | VDDIO2 |
| MSC1_D3 MAC_LED_RX SLCD_D5 PC07 | IO O O IO | A11 | 8mA | MSC1_D3: MSC (MMC/SD) 1 data bit 3 MAC_LED_RX: RX activity indication SLCD_D5: smart lcd data output bit 5 PC07: GPIO group C bit 07 | VDDIO2 |

| Pin Names | IO | Loc | IO Cell Char. | Pin Description | Power |
|---|-------------------------|-----|------------------------------------|--|--------|
| SSI0_GPC UART2_TXD SMB1_SDA SLCD_DC PC08 | O I IO O IO | B10 | 8mA Pullup-rst | SSI0_GPC: ssi 0 general-purpose control UART2_TXD: UART 2 transmit data SMB1_SDA: I2C 1 serial data SLCD_DC: smart lcd cmd/data identify PC08: GPIO group C bit 08. | VDDIO2 |
| SSI0_CE1 UART2_RXD SMB1_SCK SLCD_CS PC09 | O I IO O IO | A9 | 8mA Pullup-rst | SSI0_CE1: ssi 0 chip 1 select UART2_RXD: UART 2 receive data SMB1_SCK: I2C 1 serial clock SLCD_CS: smart lcd chip select PC09: GPIO group C bit 09. | VDDIO2 |
| SSI0_DR PWM2 UART2_CTS PC11 | I O I IO | B9 | 8mA | SSI0_DR: ssi 0 receive data PWM2: PWM channel 2 output UART2_CTS: UART 2 Clear-to-Send handshaking PC11: GPIO group C bit 11. | VDDIO2 |
| SSI0_DT PWM3 UART2_RTS PC12 | O O O IO | C9 | 8mA | SSI0_DT: ssi 0 transmit data PWM3: PWM channel 3 output UART2_RTS: UART 2 Request-to-Send handshaking PC12: GPIO group C bit 12. | VDDIO2 |
| SSI0_CLK PWM4 UART2_TXD PC13 | O O O IO | B8 | 8mA | SSI0_CLK: ssi 0 clock PWM4: PWM channel 4 output UART2_TXD: UART 2 transmit data PC13: GPIO group C bit 13. | VDDIO2 |
| SSI0_CE0 PWM5 UART2_RXD PC14 | O O I IO | A8 | 8mA Pullup-rst | SSI0_CE0: ssi 0 chip 0 select PWM5: PWM channel 5 output UART2_RXD: UART 2 receive data PC14: GPIO group C bit 14. | VDDIO2 |
| PWM6 SLCD_WR PC15 | O I IO | D10 | 8mA Pulldown-rst Schmitt-rst | PWM6: PWM channel 6 output SLCD_WR: smart lcd write data control PC15: GPIO group C bit 15. | VDDIO2 |
| CLK32K_OUT PWM7 SLCD_TE PC16 | O O I IO | D9 | 8mA Pulldown-rst Schmitt-rst | CLK32K_OUT: 32.768K clock output PWM7: PWM channel 7 output SLCD_TE: smart lcd crack control PC16: GPIO group C bit 16. | VDDIO2 |
| PWM0 FLASH_STORB E_IN UART2_CTS SLCD_D6 PC17 | O I I O IO | E10 | 8mA Pulldown-rst Schmitt-rst | PWM0: PWM channel 0 output FLASH_STORB_IN: camera flash store input UART2_CTS: UART 2 clear-to-send handshaking SLCD_D6: smart lcd data output bit 6 PC17: GPIO group C bit 17. | VDDIO2 |
| PWM1 FLASH_OUT UART2_RTS SLCD_D7 PC18 | O O O O IO | E9 | 8mA Pulldown-rst Schmitt-rst | PWM1: PWM channel 1 output FLASH_OUT: camera flash out UART2_RTS: UART 2 request-to-send handshaking SLCD_D7: smart lcd data output bit 7 PC18: GPIO group C bit 18. | VDDIO2 |

2.5.5 GPIO

Table 2-5 GPIO Pins (2)

| Pin Names | IO | Loc | IO Cell Char. | Pin Description | Power |
|-----------|----|-----|---------------------|---------------------------|--------|
| PA18 | IO | E12 | 8mA | PA18: GPIO group A bit 18 | VDDIO0 |
| PB31 | IO | N9 | 8mA Pulldown-rst | PB31: GPIO group B bit 31 | VDDIO1 |

2.5.6 System

Table 2-6 System Control Pins(6)

| Pin Names | IO | Loc | IO Cell Char. | Pin Description | Power |
|------------|----|-----|-----------------------------|---|---------------|
| TRST | I | D4 | 8mA Schmitt pull-down | TRST: JTAG reset | VDDIO1 |
| RST_DELAY | I | E4 | 8mA | RST_DELAY: system reset delay time control | VDDIO1 |
| WKUP_PA30* | I | H4 | 8mA Schmitt | WKUP_PA30: Wakeup signal after main power down | RTC_VD DIO |
| PPRST_ | I | G2 | 8mA Schmitt | PPRST_: RTC power on reset and RESET-KEY reset input | RTC_VD DIO |
| TEST_TE | I | G4 | 8mA Schmitt pull-down | TEST_TE: Manufacture test enable, program readable | RTC_VD DIO |

Table 2-7 Boot Select Pins(2)

| Pin Names | IO | Loc | IO Cell Char. | Pin Description | Power |
|---------------------|---------|-----|---------------------|---|--------|
| (BOOT_SEL0) PC00 | I IO | D2 | 8mA Pullup-rst | PC00: GPIO group C bit 00 It is taken as BOOT select bit 0 by Boot ROM code | VDDIO1 |
| (BOOT_SEL1) PC01 | I IO | D3 | 8mA Pulldown-rst | PC01: GPIO group C bit 01 It is taken as BOOT select bit 1 by Boot ROM code | VDDIO1 |

2.5.7 Digital IO/core power/ground

Table 2-8 IO/Core power supplies Pins (22)

| Pin Names | IO | Loc | IO Cell Char. | Pin Description | Power |
|-----------|----|-----------------------------|---------------|--|-------|
| VDDIO0 | P | H10,J10 | - | VDDIO0: IO digital power for DVP power domain, 1.8/3.3V | - |
| VDDIO1 | P | K9,K10 | - | VDDIO1: IO digital power for normal function Pad power domain, 3.3V | - |
| VDDIO2 | P | F10,G10 | - | VDDIO2: IO digital power for low leakage power domain, 1.8/3.3V | - |
| VDD | P | J6,J7,J8,J9,K5 ,K6,K7,K8 | - | VDD: CORE digital power, 1.0V | - |

| Pin Names | IO | Loc | IO Cell Char. | Pin Description | Power |
|-----------|----|-----------------------------|---------------|--|-------|
| VSS | P | H5,H6,H7,H8, H9,J4,J5,K4 | - | VSS: IO digital ground for none DRAM and CORE digital ground, 0V | - |

2.5.8 DDR power/ground

Table 2-9 DDR power/ground supplies Pins (21)

| Pin Names | IO | Loc | IO Cell Char. | Pin Description | Power |
|-------------|----|--------------------|---------------|--|-------|
| VREF | P | C7 | - | VREF: DDR reference voltage, (VREF = VDDMEM/2) | - |
| VDDMEM | P | D5,D6,D7,D8 | - | VDDMEM: DDR IO supply(1.8V for DDR2) | - |
| VSSMEM | P | F5,F6,F7,F8,F 9 | - | VSSMEM: DDR IO ground | - |
| DDRVDD | P | E5,D6,D7,D8 | - | DDRVDD: DDR PHY 1.8V supply | - |
| DDRVSS | P | G5,G6,G7,G8, G9 | - | DDRVSS: DDR PHY ground | - |
| DDR_PLLVCCD | P | A7 | - | DDR_PLLVCCD: DDR PLL power supply for digital | - |
| DDR_PLLVCCA | P | B7 | - | DDR_PLLVCCA: DDR PLL power supply for analog | - |

2.5.9 Analog - USB

Table 2-10 USB 2.0 OTG (5)

| Pin Names | IO | Loc | IO Cell Char. | Pin Description | Power |
|-----------|-----|-----|---------------|---|-----------|
| USB0PP | AIO | J3 | - | USB0PP: USB data-positive | USB_VCC33 |
| USB0PN | AIO | J2 | - | USB0PN: USB data-negative | USB_VCC33 |
| USB_VCC33 | P | K2 | - | USB_VCC33: This is the analog supply that is used to support 3.3V signaling. This supply has both integrated IO pads and associated ESD. The expectation is that this supply is unique to the USB PHY. The PHY provides two pins for this power supply, but they can often be bonded out to a single package pin if the parasitic are low enough to support the current draw. | - |
| USB_VCC18 | P | K3 | - | USB_VCC18: This is the analog supply that is used to support 1.8V signaling. This supply has both integrated IO pads. | - |
| USB_VCC10 | P | L1 | - | USB_VCC10: This is the analog supply that is used to support 1.0V circuits within the PHY. This supply has both integrated IO pads and associated ESD. As this includes power supplied to the PLL and HS driver, the supply needs to be fairly quiet. The PHY provides | - |

| Pin Names | IO | Loc | IO Cell Char. | Pin Description | Power |
|-----------|----|-----|---------------|---|-------|
| | | | | two pins for this power supply, but they can often be bonded out to a single pin if the parasitic are low enough to support the current draw. | |

2.5.10 Analog - SARADC

Table 2-11 SARADC Pins (4)

| Pin Names | IO | Loc | IO Cell Char. | Pin Description | Power |
|------------|----|-----|---------------|---|-----------|
| AUX0 | AI | G3 | - | AUX0: SARADC channel 0 input | SADC_AVDD |
| AUX1 | AI | H1 | - | AUX1: SARADC channel 1 input | SADC_AVDD |
| SADC_AVDD | P | J1 | - | SADC_AVDD: SARADC analog power, 1.8 V | - |
| SADC_VREFP | P | H2 | - | SADC_VREFP: Voltage reference input, 0.5* SADC_AVDD~0.99* SADC_AVDD | - |

2.5.11 Analog - CODEC

Table 2-12 CODEC Pins (6)

| Pin Names | IO | Loc | IO Cell Char. | Pin Description | Power |
|------------|----|-----|---------------|-------------------------------------|------------|
| MICP | AI | M1 | - | MICP: differential microphone input | CODEC_AVDD |
| MICN | AI | L2 | - | MICN: differential microphone input | CODEC_AVDD |
| VCM | AO | M2 | - | VCM: Reference voltage output | CODEC_AVDD |
| MICBIAS | AO | L3 | - | MICBIAS: Microphone bias output | CODEC_AVDD |
| HPOUT | AO | N1 | - | HPOUT: headphone output | CODEC_AVDD |
| CODEC_AVDD | P | N2 | - | CODEC_AVDD:1.8V analog supply | - |

2.5.12 Analog - MAC-PHY

Table 2-13 MAC-PHY Pins(8)

| Pin Names | IO | Loc | IO Cell Char. | Pin Description | Power |
|--------------|-----|-----|---------------|--|----------|
| MAC_TXN | AO | L9 | - | MAC_TXN: PHY transmit data-negative | MAC_VDDA |
| MAC_TXP | AO | M9 | - | MAC_TXP: PHY transmit data-positive | MAC_VDDA |
| MAC_RXN | AI | L10 | - | MAC_RXN: PHY receive data-negative | MAC_VDDA |
| MAC_RXP | AI | M10 | - | MAC_RXP: PHY receive data-positive | MAC_VDDA |
| MAC_EXTRES | AIO | M11 | - | MAC_EXTRES: PHY connection to reference resistor NOTES: 6.5KΩ should be connected externally on board. | MAC_VDDA |
| MAC_TEST_ATP | AIO | N11 | - | MAC_TEST_ATP: PHY analog test point NOTES: Resistance < 1Ω; inductance < | - |

| Pin Names | IO | Loc | IO Cell Char. | Pin Description | Power |
|-----------|----|-----|---------------|--|-------|
| | | | | 5nH | |
| MAC_VDDHV | P | N12 | - | MAC_VDDHV: PHY 1.8V analog power supply for central bias | - |
| MAC_VDDA | P | L11 | - | MAC_VDDA: PHY 1.0V analog power supply for RX and TX | - |

2.5.13 Analog - EFUSE

Table 2-14 EFUSE Pins (1)

| Pin Names | IO | Loc | IO Cell Char. | Pin Description | Power |
|-----------|----|-----|---------------|--|-------|
| AVDEFUSE | P | F4 | - | AVDEFUSE: EFUSE programming power, 0V/1.5V | - |

2.5.14 Analog - CLOCK/PLL

Table 2-15 CLOCK/PLL Pins (6)

| Pin Names | IO | Loc | IO Cell Char. | Pin Description | Power |
|-----------|----|-----|---------------------------------|---|-----------|
| EXCLK_XI | AI | E1 | 2~30 MHz Oscillator, OSC on/off | EXCLK_XI: external oscillator clock input or external 24MHz clock input | RTC_VDDIO |
| EXCLK_XO | AO | E2 | | EXCLK_XO: external oscillator clock output | RTC_VDDIO |
| PLL_VDDA | P | D2 | - | PLL_VDDA: PLL analog power, 1.8V | - |

2.5.15 Analog - RTC

Table 2-16 RTC Pins (4)

| Pin Names | IO | Loc | IO Cell Char. | Pin Description | Power |
|-----------|----|-----|----------------------|---------------------------------|-----------|
| OSC32_XI | AI | F1 | 32.768KHz Oscillator | osc32_XI: 32.768KHz clock input | RTC_VDDIO |
| OSC32_XO | AO | F2 | | osc32_XO: Reserved | RTC_VDDIO |
| RTC_VDD | P | E3 | - | RTC_VDD: 1.0V power for RTC | - |
| RTC_VDDIO | P | G1 | - | RTC_VDDIO: 3.3V power for RTC | - |

NOTES:

- All GPIO are programmable with multi-voltage (1.8V, 2.5V, 2.8V, 3.0V, 3.3V) general purpose, bi-directional I/O buffer with a selectable LVCMOS input or LVCMOS Schmitt trigger input and programmable pull-up / pull-down. In the full-drive mode, this buffer can operate in excess of 100MHz frequency with 15pF external load and 125 MHz with 10pF load, but actual frequency is load and system dependent. A maximum of 200 MHz can be achieved under small capacitive loads.
- The meaning of phases in IO cell characteristics are:
 - 8/16mA out: The IO cell's output driving strength is about 8/16mA.

- Pull-up: The IO cell contains a pull-up resistor and fixed pull up.
 - Pull-down: The IO cell contains a pull-down resistor and fixed pull down.
 - Pullup-rst: The IO cell during reset and after the pull up function is enabled.
 - Pulldown-rst: The IO cell during reset and after the pull down function is enabled.
 - Schmitt: The IO cell is Schmitt trigger input and fixed.
 - Schmitt-rst: The IO cell during reset and after the Schmitt trigger input function is enabled.
 - Slew-rate-rst: The IO cell during reset and after the slew-rate function select fast mode.
- 3 *: This pin has GPIO function as group A bit 30, but only input/interrupt function.

3 Electrical Specifications

3.1 Absolute Maximum Ratings

The absolute maximum ratings for the processors are listed in Table 3-1. Do not exceed these parameters or the part may be damaged permanently. Operation at absolute maximum ratings is not guaranteed.

Table 3-1 Absolute Maximum Ratings

| Parameter | Min | Max | Unit |
|--|------|-------|------|
| Storage Temperature | -65 | 150 | °C |
| Operation Temperature | -20 | 70 | °C |
| VDDMEM power supplies voltage | -0.1 | 1.98 | V |
| DDRVDD power supplies voltage | -0.1 | 1.98 | V |
| DDR_PLLVCCD power supplies voltage | -0.1 | 1.1 | V |
| DDR_PLLVCCA power supplies voltage | -0.1 | 1.98 | V |
| VDDIO0 power supplies voltage | -0.5 | 1.98 | V |
| VDDIO1 power supplies voltage | -0.5 | 3.63 | V |
| VDDIO2 power supplies voltage | -0.5 | 3.63 | V |
| VDD power supplies voltage | -0.2 | 1.1 | V |
| PLL_VDDA power supplies voltage | -0.1 | 1.98 | V |
| AVDEFUSE power supplies voltage | -0.1 | 1.65 | V |
| RTC_VDD power supplies voltage | -0.5 | 1.155 | V |
| RTC_VDDIO power supplies voltage | -0.5 | 3.63 | V |
| USB_VCC33 power supplies voltage | -0.1 | 3.63 | V |
| USB_VCC18 power supplies voltage | -0.1 | 1.98 | V |
| USB_VCC10 power supplies voltage | -0.1 | 1.1 | V |
| SADC_AVDD power supplies voltage | -0.1 | 1.98 | V |
| CODEC_AVDD power supplies voltage | -0.1 | 1.98 | V |
| MAC_VDDA power supplies voltage | -0.1 | 1.1 | V |
| MAC_VDDHV power supplies voltage | -0.1 | 1.98 | V |
| Maximum ESD stress voltage, Human Body Model; Any pin to any supply pin, either polarity, or Any pin to all non-supply pins together, either polarity. Three stresses maximum. | - | 2000 | V |

3.2 Recommended operating conditions

Table 3-2 Recommended operating conditions for power supplies

| Symbol | Description | Min | Typical | Max | Unit |
|--------|----------------------------------|------|---------|------|------|
| VDDMEM | VDDMEM voltage for SSTL18 (DDR2) | 1.62 | 1.8 | 1.98 | V |

| | | | | | |
|-------------|--------------------------------------|------|-----|-------|---|
| DDRVDD | DDR PHY power supplies voltage | 1.62 | 1.8 | 1.98 | V |
| DDR_PLLVCCD | DDR PLL power supplies voltage | 0.9 | 1.0 | 1.1 | V |
| DDR_PLLVCCA | DDR PLL power supplies voltage | 1.62 | 1.8 | 1.98 | V |
| VDDIO0 | GPIO power domain 0 supplies voltage | 1.62 | 1.8 | 1.98 | V |
| VDDIO1 | GPIO power domain 1 supplies voltage | 1.5 | 3.3 | 3.63 | V |
| VDDIO2 | GPIO power domain 2 supplies voltage | 1.5 | 3.3 | 3.63 | V |
| VDD | VDD core supplies voltage | 0.9 | 1.0 | 1.1 | V |
| PLL_VDDA | APLL, MPLL and VPLL analog voltage | 1.62 | 1.8 | 1.98 | V |
| AVDEFUSE | EFUSE program supplies voltage | 1.35 | 1.5 | 1.65 | V |
| RTC_VDD | RTC core supplies voltage | 0.72 | 1.0 | 1.155 | V |
| RTC_VDDIO | RTC IO supplies voltage | 1.35 | 3.3 | 3.63 | V |
| USB_VCC33 | USB PHY VCCA3P3 analog voltage | 3.0 | 3.3 | 3.6 | V |
| USB_VCC18 | USB PHY VCC18 analog voltage | 1.62 | 1.8 | 1.98 | V |
| USB_VCC10 | USB PHY VCCCORE1P0 voltage | 0.9 | 1.0 | 1.1 | V |
| SADC_AVDD | SAR-ADC analog voltage | 1.62 | 1.8 | 1.98 | V |
| CODEC_AVDD | CODEC analog voltage | 1.62 | 1.8 | 1.98 | V |
| MAC_VDDA | MAC PHY analog voltage | 0.9 | 1.0 | 1.1 | V |
| MAC_VDDHV | MAC PHY analog voltage | 1.62 | 1.8 | 1.98 | V |

Table 3-3 Recommended operating conditions for VDDIO/VDDIO_D/RTC_VDDIO supplied pins

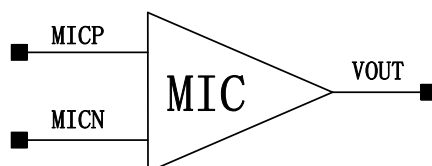
| Symbol | Parameter | Min | Typical | Max | Unit |
|-------------------|---|-------|---------|-------|------|
| V _{IH18} | Input high voltage for 1.8V I/O application | *0.65 | - | +0.3 | V |
| V _{IL18} | Input low voltage for 1.8V I/O application | -0.3 | - | *0.35 | V |
| V _{IH25} | Input high voltage for 2.5V I/O application | 1.7 | - | +0.3 | V |
| V _{IL25} | Input low voltage for 2.5V I/O application | -0.3 | - | 0.7 | V |
| V _{IH33} | Input high voltage for 3.3V I/O application | 2 | - | +0.3 | V |
| V _{IL33} | Input low voltage for 3.3V I/O application | -0.3 | - | 0.8 | V |

Table 3-4 Recommended operating conditions for others

| Symbol | Description | Min | Typical | Max | Unit |
|----------------|---------------------|-----|---------|------|------|
| T _A | Ambient temperature | -40 | 25 | +125 | °C |

3.3 Audio codec

3.3.1 Microphone input

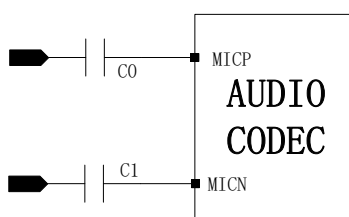


There are two microphone input channels, MICP and MICN. They can be configured as differential inputs by the microphone PGA(MIC).

The signal of microphone output should be input to AUDIO CODEC through DC-blocking capacitor, as shown in following figure. The capacitance and input resistance form a high pass filter. For example, when the gain of the MIC module is 20dB, the input resistance is 45K Ω and 0.1 μ F DC-blocking capacitor is used, the lower cut-off frequency is:

$$f = \frac{1}{2\pi RC} = \frac{1}{2\pi \times 45 \times 10^3 \times 0.1 \times 10^{-6}} = 35.4Hz$$

The capacitance of the DC-blocking capacitor should be determined by the minimum input impedance and application requirements.



If the output of microphone is single-ended, the AUDIO ADC input should be connected as following figure.



Microphone PGA has four gains to amplify the input signal, that is, 0dB, 20dB, 30dB and 40dB.

3.3.2 ALC

Automatic Level Control (ALC) function is included to adjust the signal level, which is input into ADC. ALC will measure the signal magnitude and compare it to defined threshold. Then it will adjust the ALC

controlled PAG (ALC) gain according to the comparison result.

The programmable gain range of ALC controlled PAG is from -18dB to +28.5dB. The tuning step is 1.5dB.

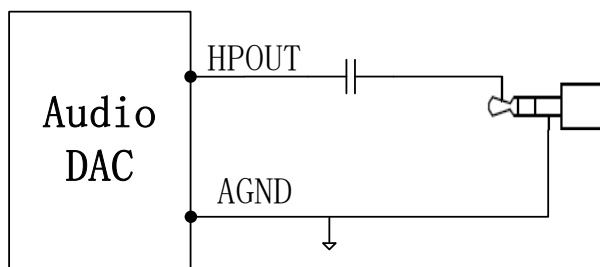
3.3.3 Headphone output

Audio codec DAC output can drive 16 Ω or 32 Ω headphone load through DC-blocking capacitor.

In the configuration using DC-blocking capacitor, shown in following figure, the headphone ground is connected to the real ground. The capacitance and the load resistance determine the lower cut-off frequency. For instance, if 16 Ω headphone and 100uF DC-blocking capacitor are used, the lower cut-off frequency is

$$f = \frac{1}{2\pi RC} = \frac{1}{2\pi \times 16 \times 100 \times 10^{-6}} = 99.5Hz$$

The DC-blocking capacitor can be increased to lower the cut-off frequency for better bass response.



The headphone driver chooses DAC output as input. It has a gain rang from -39dB to +6dB with a tuning step of 1.5dB.

3.3.4 Microphone bias

Microphone bias output is used to bias external microphones. The bias voltage can varies from 0.8*CODEC_AVDD to 0.975* CODEC_AVDD with a step of 0.025* CODEC_AVDD.

3.4 MAC PHY

The transmitter is implemented using a Class-A current steering architecture. The transmitter drives a scrambled MLT3 data into the 100 Ω impedance. The transmitter implements a 6b DAC.

For the 100BaseT receive function, the MLT-3 from the cable is fed into PHY through a low-pass-filter, and a 6b AD samples the incoming data. A programmable gain is implemented in the ADC. Baseline wander is corrected using a small DAC.

The receiver receives the encoded stream from the cable, and the analog signal is filtered and checked using a squelch circuit. The receiver recovers the clock and data to recreate the NRZI stream

after confirming that the data is valid encoded data. Polarity is identified and corrected as necessary (observable through register interface). Then stream is deserialized ascent to the MAC interface at 2.5MHz.

The recommendations board circuit design is as shown below.

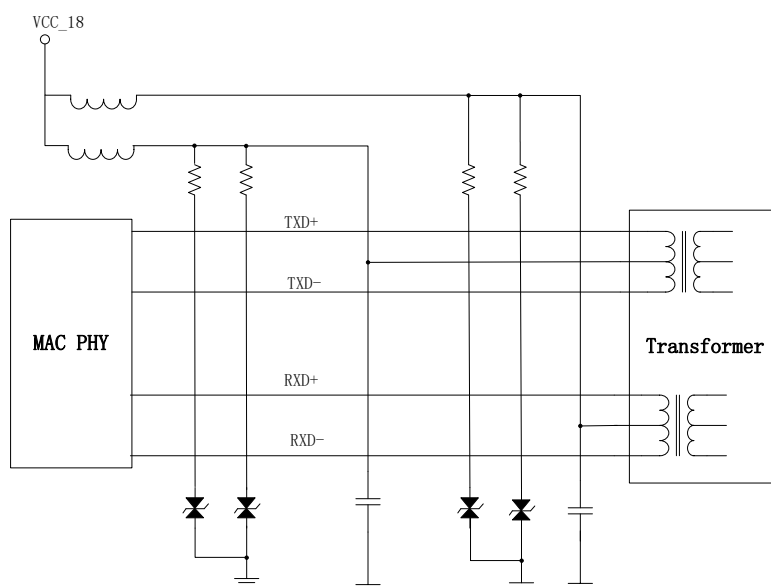


Figure 3-1 Typical Product board circuit Design

3.5 Power On, Reset and BOOT

3.5.1 Power-On Timing

The external voltage regulator and other power-on devices must provide the X1021 processor with a specific sequence of power and resets to ensure proper operation. Figure 3-2 shows this sequence and Table 3-5 gives the timing parameters. Following are the name of the power.

- VDDRTC: RTC_VDDIO, RTC_VDD
- AVDAUD: CODEC_AVDD
- VDD10: all 1.0V power supplies, include VDD
- VDD: all other digital IO, include DDR power supplies: VDDMEM, VDDIO0, VDDIO1, VDDIO2
- AVD: all other analog power supplies: SADC_AVDD, USB_VCC33, USB_VCC18, USB_VCC10, PLL_VDDA, MAC_VDDA, MAC_VDDHV

Table 3-5 Power-On Timing Parameters

| Symbol | Parameter | Min | Max | Unit |
|-----------------|---------------------------------|-----|-----|------|
| t_{R_VDDRTC} | VDDRTC rise time ^[1] | 0 | 5 | ms |

| | | | | |
|------------------|---|--------------------|---|-------------------|
| t_{R_VDD} | VDD rise time ^[1] | 0 | 5 | ms |
| t_{D_VDD} | Delay between VDDRTC arriving 50% (or 90%) to VDD33 arriving 50% (or 90%) | 0 | – | ms |
| t_{R_VDD10} | VDD10 rise time ^[1] | 0 | 5 | ms |
| t_{D_VDD10} | Delay between VDD arriving 50% (or 90%) to VDD10 arriving 50% (or 90%) | –1 | 1 | ms |
| t_{R_AVDAUD} | AVDAUD rise time ^[1] | 0 | 5 | ms |
| t_{D_AVDAUD} | Delay between VDD10 arriving 50% (or 90%) to AVDAUD arriving 50% (or 90%) | 0.01 | 1 | ms |
| t_{R_AVD} | AVD rise time ^[1] | 0 | 5 | ms |
| t_{D_AVDA} | Delay between VDD arriving 50% to AVD arriving 50% | -1 | 1 | ms |
| $t_{D_PPRST_}$ | Delay between VDDAUD stable and PPRST_ deasserted | TBD ^[3] | – | ms ^[2] |

NOTES:

- The power rise time is defined as 10% to 90%.
- The PPRST_ must be kept at least 100us. After PPRST_ is deasserted, the corresponding chip reset will be extended at least 40ms.

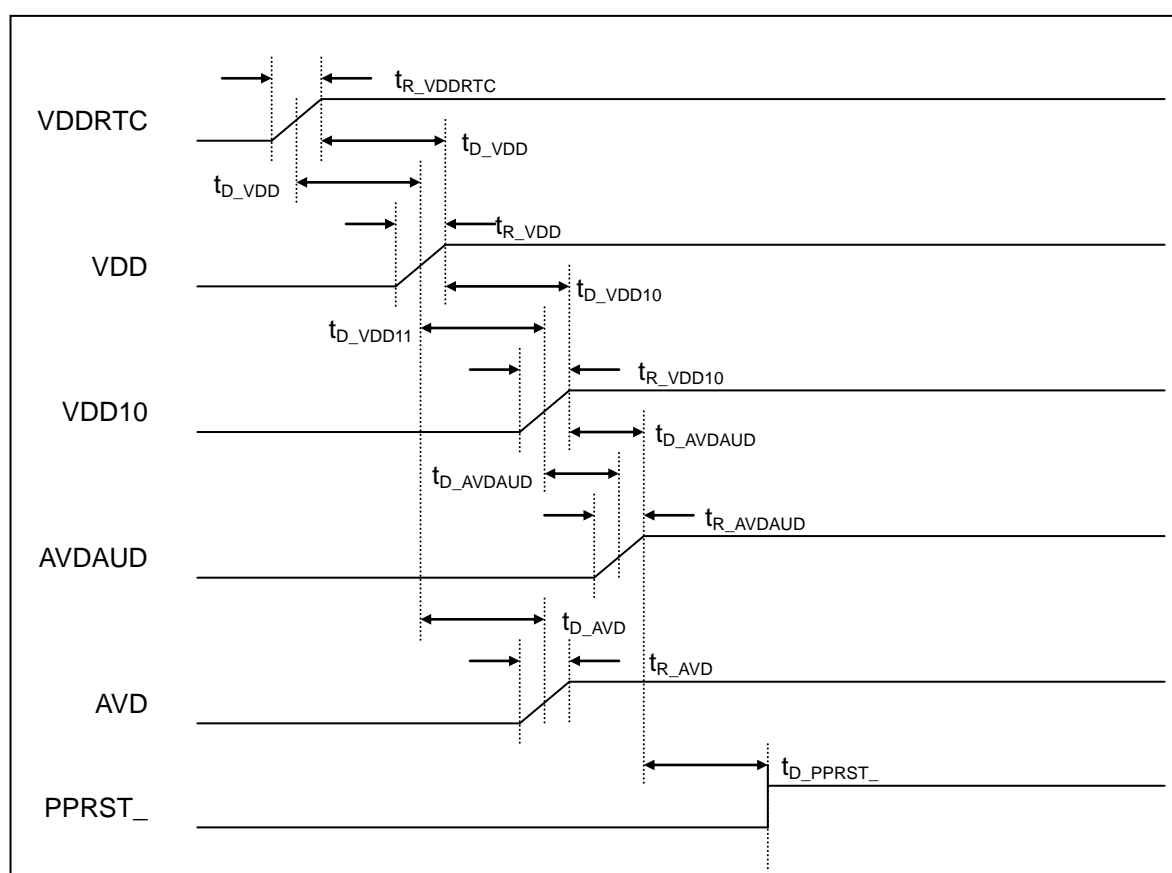


Figure 3-2 Power-On Timing Diagram

3.5.2 Reset procedure

There are 3 reset sources: 1. PPRST_ pin reset; 2. WDT timeout reset; and 3. hibernating reset when exiting hibernating mode. After reset, program start from boot.

- PPRST_ pin reset.
This reset is trigged when PPRST_ pin is put to logic 0. It happens in power on RTC power and RESET-KEY pressed to reset the chip from unknown dead state. The reset end time is about 1M EXCLK cycles after rising edge of PPRST_.
- WDT reset.
This reset happens in case of WDT timeout. The reset keeps for about a few RTCLK cycles.
- Hibernating reset.
This reset happens in case of wakeup the main power from power down. The reset keeps for about 1ms ~ 125ms programable, plus 1M EXCLK cycles, start after WKUP_ signal is recognized.

After reset, all GPIO shared pins are put to GPIO input function and most of their internal pull-up/down resistor are set to on, see “2.5Pin Description” for details. The PWRON is output 1. The oscillators are on. The USB 2.0 OTG PHY and USB 1.1 PHY, the audio CODEC DAC/ADC, the SAR-ADCs is put in suspend mode.

3.5.3 BOOT

The boot sequence of the X1021 is controlled by boot_sel[1:0]. The configuration is shown as follow:

Table 3-6 Boot Configuration of X1021

| boot_sel[1:0] | Boot method |
|---------------|--|
| 00 | MMC/SD boot @ MSC0 (MMC/SD use GPIO Port B. MSC1 use GPIO Port C) |
| 01 | SFC boot @ CS4 (SPI boot) |
| 10 | NOR boot @ CS2 (just for FPGA testing) |
| 11 | USB boot @ USB 2.0 device, EXTCLK=24MHz |

The boot procedure is showed in the following flow chart:

As shown in Figure 3-3, boot sequence Block Diagram. After reset, the boot program on the internal boot ROM executes as follows:

- 1 Disable all interrupts and read boot_sel[1:0] to determine the boot method.
- 2 There 26KB backup reading failed, the 26KB backup at 128th, 256 th , ..., and finally 1024th page will be tried in consecutive order.
- 3 If it is boot from MMC/SD card at MSC0, its function pins MSC0_D0, MSC0_CLK, MSC0_CMD are initialized, the boot program loads the 26KB code from MMC/SD card to cache and jump to it. Only one data bus which is MSC0_D0 is used.

- 4 If it is boot from USB, a block of code will be received through USB cable connected with host PC and be stored in cache. Then branch to this area in cache.
- 5 If it is boot from SPI nor/nand at SFC, its function pins SFC_CLK, SFC_CE, SFC_DR, SFC_DT, SFC_WP, SFC_HOLD are initialized, the boot program loads the 12kB code from SPI NAND/NOR flash to cache and jump to it.
- 6 If it is boot from NOR Flash, the boot program jump to nor and run directory.

When SFC boot start failure, the program in bootrom will go into MSC0 boot.

When MSC0 boot start failure, the program in bootrom will go into MSC1 boot. If it is boot from MMC/SD card at MSC1, its function pins MSC1_D0, MSC1_CLK, MSC1_CMD are initialized, the boot program loads the 26KB code from MMC/SD card to cache and jump to it. Only one data bus which is MSC1_D0 is used. If MSC1 boot start failure, jump to USB boot.

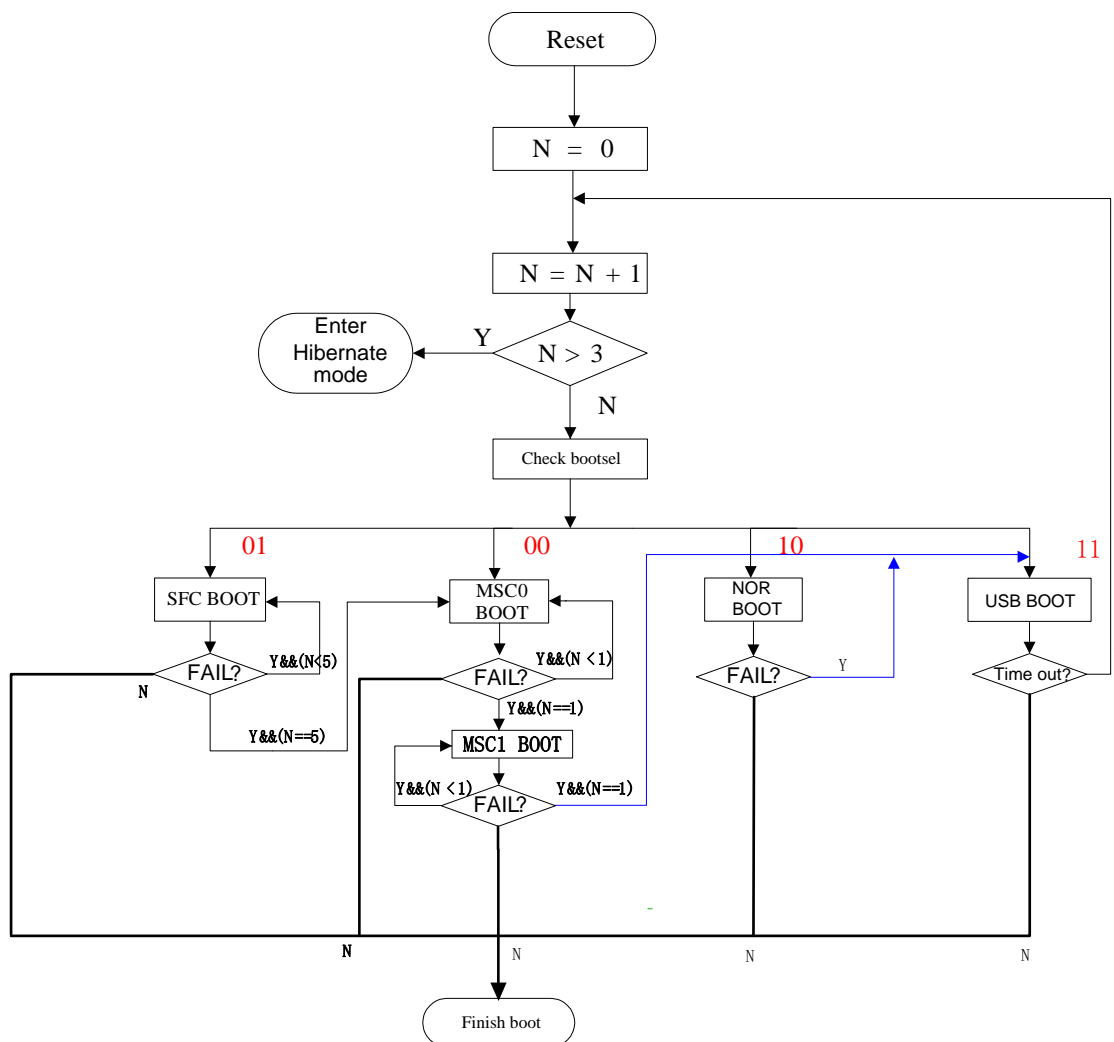


Figure 3-3 Boot sequence diagram of X1021