X1600

IoT Application Processor

Programming Manual

Release Date: Aug. 06, 2021

北京君正集成电路股份有限公司
Ingenic Semiconductor Co.,Ltd.

X1600 IoT Application Processor

Programming Manual

Copyright © 2005-2021 Ingenic Semiconductor Co. Ltd. All rights reserved.

Disclaimer

This documentation is provided for use with Ingenic products. No license to Ingenic property rights is granted. Ingenic assumes no liability, provides no warranty either expressed or implied relating to the usage, or intellectual property right infringement except as provided for by Ingenic Terms and Conditions of Sale.

Ingenic products are not designed for and should not be used in any medical or life sustaining or supporting equipment.

All information in this document should be treated as preliminary. Ingenic may make changes to this document without notice. Anyone relying on this documentation should contact Ingenic for the current documentation and errata.

Ingenic Semiconductor Co., Ltd.

Ingenic Headquarters, East Bldg. 14, Courtyard #10,
XIbeiwang East Road, Haidian District, Beijing 100193, China,
Tel: 86-10-56345000
Fax: 86-10-56345001
Http: //www.ingenic.com

CONTENTS

CONTENTS iii
TABLES ii
FIGURES 1
OVERVIEW 1
1 Overview 2
1.1 Block Diagram 2
1.2 Featrue 2
1.2.1 CPU Core 2
1.2.2 Memory Interface 3
1.2.3 Media Interface 3
1.2.4 System Functions 4
1.2.5 Peripherals 5
1.2.6 Bootrom 8
1.3 IO Devices Physical Memory Map 8
CORE FUNCTION 10
2 CPU 11
2.1 Overview 11
2.2 PRID of X1600-CPU 11
2.3 Interrupt Mapping 11
MEMORY INTERFACE 12
3 DDR Controller 13
3.1 Overview 13
3.2 Features 13
3.3 Supported DDR SDRAM Types 13
3.4 Block Diagram 13
3.5 DDR Controller Register Description 14
3.5.1 Register Memory Map 14
3.5.2 Register and Fields Description 17
3.6 DDR PHY Register Description 46
3.6.1 Register Memory Map 46
3.6.2 Register and Fields Description 48
3.7 Functional Description 89
3.7.1 DDRC and DDR2 Memory Initialization Sequence 89
3.8 Change Clock Frequency 91

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

3.8.1 Manually SELF-REFRESH Mode 91
3.8.2 CPM driven SELF-REFRESH Mode 91
3.8.3 DLL bypass mode 91
3.9 Data Endian 91
3.10 Retention Flow 92
3.10.1 Enter Retention mode 92
3.10.2 Exit Retention mode 93
3.11 DDR Connection Diagrams 95
3.11.1 Connection to one 512Mb x16 DDR2 devic 96
3.11.2 Connection to two 512Mb x16 DDR2 devices 97

4 External Memory Controller 98

4.1 Overview 98
4.2 Features 98
4.3 Pin Description 98
4.4 Physical Address Space Map 98
4.5 Example of Connection 100
4.6 Timing Setting 102
4.6.1 Normal Memory 102
4.6.2 Burst ROM 105
4.6.3 Address/Data Multiplexed Memory 106
4.7 Register Description 107
4.7.1 Register Memory Map 108
4.7.2 Register and Fields Description 108

5 SPI Flash Controller(SFC) 116

5.1 Overview 116
5.2 Features 116
5.3 Block Diagram 117
5.4 Functional Description 117
5.4.1 Bus function 117
5.4.2 AHB Slave Interface 117
5.4.3 AHB Master Interface 117
5.4.4 Configurable Timing parameter 118
5.5 Pin Description 118
5.6 Date Format Description 119
5.6.1 Transfer format 119
5.6.2 Endian Description 120
5.7 Registers Description 120
5.7.1 Instructions 120
5.7.2 Map 121
5.7.3 Registers 122
5.8 Software Guideline 136

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

5.8.1 CDT Description ... 136
5.8.2 DMA Descriptor ... 137
5.8.3 Phase Description ... 138
5.8.4 Multi phases flow ... 139
5.8.5 One phase flow ... 139
5.8.6 Meters of DMA operation need attention ... 140
5.8.7 Meters of slave mode operation need attention ... 140
5.8.8 Example (NAND flash write with multi phases in DMA mode) ... 140
5.8.9 Example (NAND flash write with multi phases in DMA descriptor mode) ... 141
5.8.10 Example (NAND flash write with multi phases in CDT mode) ... 143
5.8.11 Example (NAND flash write with single phase in REG mode) ... 143
5.9 Index ... 144

CAMERA/AUDIO/DISPLAY ... 146

6 MIPI_CSI Interface ... 147

6.1 Overview ... 147
6.1.1 Features ... 147
6.2 Register Descriptions ... 147
6.2.1 Register Mapping ... 147
6.2.2 VERSION ... 148
6.2.3 N_LANES ... 148
6.2.4 PHY_SHUTDOWNZ ... 149
6.2.5 DPHY_RSTZ ... 149
6.2.6 CSI2_RESETN ... 150
6.2.7 PHY_STATE ... 150
6.2.8 DATA_IDS ... 151
6.2.9 ERR1 ... 151
6.2.10 ERR2 ... 152
6.2.11 MASK1 ... 153
6.2.12 MASK2 ... 155
6.2.13 PHY_TST_CRTL0 ... 156
6.2.14 PHY_TST_CRTL1 ... 156
6.3 Operation ... 156

7 MIPI D-PHY Receiver ... 158

7.1 Overview ... 158
7.2 Functional Blocks ... 159
7.3 Registers Description ... 160
7.3.1 Instructions ... 160
7.3.2 Map ... 160
7.3.3 Configure ... 162
7.4 Operation Guide ... 173
7.4.1 Logic PHY-Protocol Interface ... 173

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

8 Camera Interface Module (CIM) 174
8.1 Overview 174
8.2 Feature 174
8.3 Function Description 175
8.3.1 Mode 175
8.4 Data Format Description 175
8.4.1 Input Data(DVP Interface) 175
8.4.2 Output Data(memory) 176
8.4.3 Timing 176
8.4.4 Others 176
8.5 Pins Description 177
8.6 Architecture map 177
8.7 Descriptor define 177
8.8 Registers Description 180
8.8.1 Instructions 180
8.8.2 Map 181
8.8.3 Registers 182
8.9 Operation guide 194
8.9.1 Configure flow 194
8.9.2 Interlace scan mode 195
8.9.3 Area Luminance 195
9 Audio Interface Controller (AIC) 196
9.1 Overview 196
9.2 Features 196
9.3 Block Diagram 197
9.4 Signal Descriptions 197
9.5 Interface Diagram 198
9.6 Data Format Description 200
9.6.1 I2S and MSB-justified serial audio format 200
9.6.2 Audio sample data placement in DAC_SDATA/ADC_SDATA 202
9.7 Register Description 203
9.7.1 Register Memory Map 203
9.7.2 Register and Fields Description 204
9.8 Operation Flow 215
9.8.1 Initialization 216
9.8.2 External CODEC Registers Access Operation 216
9.8.3 Audio Replay 216
9.8.4 Audio Record 217
9.8.5 FIFOs operation 218
9.8.6 Data Flow Control 220
9.8.7 Audio Samples format 221
9.8.8 Serial Audio Clocks and Sampling Frequencies 223

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

9.8.9 Interrupts 227

10 Display Controller 228

10.1 Features 228
10.2 Architecture map 228
10.3 Data Format Description 228
10.3.1 Source data define (the format of source data in DDR memory) 228
10.3.2 SLCD output pin define 229
10.3.3 GPIO Pads relation 230
10.4 Descriptor definition 230
10.5 Registers Description 231
10.5.1 Instructions 231
10.5.2 Map 232
10.5.3 Basic configure 233
10.5.4 Display interfaces configure 239
10.6 Operation guide 250
10.6.1 Simple read dma(SRD) operation 250
10.6.2 TFT operation 250
10.6.3 SLCD operation 251
10.6.4 Insert new descriptor into current chain 251
10.6.5 Interrupt control 251
10.7 Software Notes 251

SYSTEM FUNCTIONS 252

11 Clock Reset and Power Controller 253

11.1 Overview 253
11.1.1 CGU Block Diagram 254
11.1.2 CGU Registers 255
11.1.3 PLL Operation 286
11.1.4 Main Clock Division Change Sequence 287
11.2 Power Manager 287
11.2.1 Low-Power Modes and Function 287
11.2.2 Register Description 288
11.2.3 IDLE Mode 298
11.2.4 SLEEP Mode 299
11.3 Reset Control Module 299
11.3.1 Register Description 299
11.3.2 Power On Reset 300
11.3.3 WDT Reset 301

12 Timer/Counter Unit 302

12.1 Overview 302
12.2 Features 302

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

12.3 Pin Description 302
12.4 Register Description 302
12.4.1 Register Memory Map 303
12.4.2 Register and Fields Description 304
12.5 Operation Guide 323
12.5.1 Operation in TCU Mode 323
12.5.2 Operation in TCU Function 329

13 Pulse Modulator Module 331

13.1 Overview 331
13.2 Features 331
13.3 Block Diagram 331
13.4 Register description 331
13.4.1 PWM Counter Enable Register (PWMEN, PWMENS, PWMENC) 333
13.4.2 PWM Update Register (PWMUPT) 334
13.4.3 PWM Update Process Busy Status Register (PWMBSY) 334
13.4.4 PWM Channel Mode Select Register (PWMMS) 335
13.4.5 PWM INIT LEVEL Register (PWMINL) 335
13.4.6 PWM IDLE LEVEL Register (PWMIDL) 336
13.4.7 PWM Counter Configure Register (PWMCCn) 336
13.4.8 PWM Waveform Configuration(PWMWCn) 336
13.4.9 PWM DMA Channel Data Register (PWMDRn) 337
13.4.10 PWM DMA Channel FiFo Number Register (PWMDFNn) 338
13.4.11 PWM DMA Request Trigger Number Register (PWMDRTNn) 338
13.4.12 PWM DMA Request enable Register(PWMDRE) 338
13.4.13 PWM DMA Request Status Register(PWMDRS) 338
13.4.14 PWM DMA FiFo Under Run Interrupt enable Register(PWMDFIE) 339
13.4.15 PWM DMA Channel FiFo Status Register(PWMDFS) 339
13.4.16 PWM DMA Async FiFo Flush(PWMDAFF) 339
13.4.17 PWM DMA Channel FiFo Flush(PWMDCFF) 340
13.4.18 PWM Store Status Register(PWMSS) 340
13.4.19 PWM Store Interrupt Enable Register(PWMSIE) 340
13.4.20 PWM Store Control Register(PWMSCn) 341
13.4.21 PWM Store Number(PWMSNn) 341
13.4.22 PWM Output Number(PWMONn) 342
13.5 Basic Operation 342
13.5.1 Register update mode 342
13.5.2 DMA mode 343

14 Operating System Timer 345

14.1 overview 345
14.2 feature 345
14.3 register description 345

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

14.3.1 Registers Memory Map 346
14.3.2 Register and Fields Description 346
14.4 Operation 352
14.4.1 Basic Operation in channel1 352
14.4.2 Stop Operation in channel1 352
14.4.3 modify the pre-scale in channel1 352

15 Watchdog Timer 353

15.1 Overview 353
15.2 Features 353
15.3 Register Description 353
15.3.1 Register Memory Map 353
15.3.2 Register and Fields Description 354
15.4 Watchdog Timer Function 356

16 Real Time Clock 357

16.1 Overview 357
16.2 Features 357
16.3 Block Diagram 357
16.4 Pins Description 358
16.5 Registers Description 358
16.5.1 RTC Control Register (RTCCR) 360
16.5.2 RTC Second Register (RTCSR) 361
16.5.3 RTC Second Alarm Register (RTCSAR) 362
16.5.4 RTC Regulator Register (RTCGR) 362
16.5.5 Hibernate Control Register (HCR) 363
16.5.6 HIBERNATE mode Wakeup Filter Counter Register (HWFCR) 363
16.5.7 Hibernate Reset Counter Register (HRCR) 364
16.5.8 HIBERNATE Wakeup Control Register (HWCR) 364
16.5.9 HIBERNATE Wakeup Status Register (HWRSR) 365
16.5.10 Hibernate Scratch Pattern Register (HSPR) 366
16.5.11 Write Enable Pattern Register (WENR) 367
16.5.12 WKUP_PIN_RST control register (WKUPPINCR) 367
16.6 Operation Flow 368
16.6.1 Registers Access 368
16.6.2 Normal Mode 369
16.6.3 HIBERNATE Mode 369
16.6.4 Time Regulation 370
16.6.5 Clock select 371

17 Interrupt Controller 372

17.1 Overview 372
17.2 Register Description 372
17.2.1 Interrupt Controller Source Register (ICSR0) 373

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

17.2.2 Interrupt Controller Source Register (ICSR1) 374
17.2.3 Interrupt Controller Mask Register (ICMR0) 374
17.2.4 Interrupt Controller Mask Register (ICMR1) 374
17.2.5 Interrupt Controller Mask Set Register (ICMSR0) 375
17.2.6 Interrupt Controller Mask Set Register (ICMSR1) 375
17.2.7 Interrupt Controller Mask Clear Register (ICMCR0) 376
17.2.8 Interrupt Controller Mask Clear Register (ICMCR1) 376
17.2.9 Interrupt Controller Pending Register (ICPR0) 376
17.2.10 Interrupt Controller Pending Register (ICPR1) 377
17.2.11 Interrupt Source Register0 for PDMA (DSR0) 377
17.2.12 Interrupt Mask Register0 for PDMA (DMR0) 378
17.2.13 Interrupt Pending Register0 for PDMA (DPR0) 378
17.2.14 Interrupt Source Register1 to PDMA (DSR1) 379
17.2.15 Interrupt Mask Register1 for PDMA (DMR1) 379
17.2.16 Interrupt Pending Register1 for PDMA (DPR1) 380
17.3 Software Considerations 380

18 PDMA Controller 381

18.1 Overview 381
18.2 Features 381
18.3 Block Diagram 381
18.4 Memory Mapped Register Descriptions 382
18.4.1 DMA Channel Registers 382
18.4.2 Global Control Registers 383
18.5 DMA Channel Register Definition 383
18.5.1 DMA Source Address (DSAn, n = 0 ~ 31) 383
18.5.2 DMA Target Address (DTAn, n = 0 ~ 31) 384
18.5.3 DMA Transfer Count (DTCn, n = 0 ~ 31) 384
18.5.4 DMA Request Types (DRTn, n = 0 ~ 31) 384
18.5.5 DMA Channel Control/Status (DCSn, n = 0 ~ 31) 386
18.5.6 DMA Channel Command (DCMn, n = 0 ~ 31) 387
18.5.7 DMA Descriptor Address (DDAn, n = 0 ~ 31) 392
18.5.8 DMA Stride Difference (DSDn, n = 0 ~ 31) 392
18.6 DMA Global Register Definition 393
18.6.1 DMA Control 393
18.6.2 DMA Interrupt Pending (DIRQP) 394
18.6.3 DMA Doorbell (DDB) 394
18.6.4 DMA Doorbell Set (DDS) 395
18.6.5 Descriptor Interrupt Pending (DIP) 395
18.6.6 Descriptor Interrupt Clear (DIC) 395
18.6.7 DMA Channel Programmable (DMACP) 396
18.6.8 DMA Soft IRQ Pending (DSIRQP) 396
18.6.9 DMA Soft IRQ Mask (DSIRQM) 396

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

18.6.10 DMA Channel IRQ Pending to MCU (DCIRQP) 397
18.6.11 DMA Channel IRQ to MCU Mask (DCIRQM) 397
18.6.12 DMA Channel Source Address Compare INDEX 0 (SACIDX0) 398
18.6.13 DMA Channel Source Address Compare INDEX 1 (SACIDX1) 398
18.6.14 DMA Channel Destination Address Compare INDEX 0(DACIDX0) 398
18.6.15 DMA Channel Destination Address Compare INDEX 1(DACIDX1) 399
18.7 MCU 399
18.7.1 MCU Control & Status 399
18.7.2 MCU Normal MailBox 400
18.7.3 MCU Security MailBox 400
18.7.4 MCU Interrupt 401
18.7.5 Multiple Bank Tightly Coupled Sharing Memory 401
18.7.6 CP0 Registers of MCU 401
18.7.7 Normal Exceptions Accepted by MCU 402
18.7.8 How to Boot MCU Up 402
18.8 DMA manipulation 403
18.8.1 Descriptor Transfer Mode 403
18.8.2 No-Descriptor Transfer Mode 406
18.8.3 Descriptor Transfer Interrupt/Stop control 407
18.9 DMA Requests 408
18.9.1 Auto Request 408
18.9.2 On-Chip Peripheral Request 408
18.10 How to Use Programmable DMA Channel 408

19 SAR A/D Controller 409

19.1 Overview 409
19.2 Features 409
19.3 Block Diagram 409
19.4 Pins Description 409
19.5 Register Description 410
19.5.1 Register Memory Map 410
19.5.2 Register and Fields Description 411
19.6 SAR A/D Controller Guide 416
19.6.1 Power Down Mode 416
19.6.2 AUX Sample Operation 416

20 EFUSE Slave Interface (EFUSE) 417

20.1 Overview 417
20.2 Registers 417
20.2.1 Registers Memory Map 418
20.2.2 Registers and Fields Description 418
20.3 Flow 422
20.3.1 Program EFUSE Flow 422

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

20.3.2 Program Security Key Flow 422
20.3.3 Read EFUSE Flow 423
20.3.4 Read Security Key/Random Number Flow 423

PERIPHERALS 424

21 General-Purpose I/O Ports(GPIO) 425

21.1 Overview 425
21.2 Features 425
21.3 About GPIO Port Summary Table 425
21.3.1 GPIO Port A Summary 426
21.3.2 GPIO Port B Summary 428
21.3.3 GPIO Port C Summary 429
21.3.4 GPIO Port D Summary 430
21.3.5 GPIO Port Z-Shadow Group 431
21.4 Registers Description 431
21.4.1 Register Memory Map 432
21.4.2 Register and Fields Description 435
21.5 Program Guide 448
21.5.1 Port Function Guide 448
21.5.2 Configure without 3rd-unexpected state 448
21.5.3 Dual-edge Interrupt Configure Guide 449

22 I2C Controller 450

22.1 Overview 450
22.1.1 Features 450
22.1.2 Pin Description 450
22.2 Registers 451
22.2.1 Registers Memory Map 451
22.2.2 Registers and Fields Description 452
22.3 Operating Flow 481
22.3.1 I2C Behavior 481
22.3.2 Master Mode Operation 482
22.3.3 Slave Mode Operation 484
22.3.4 Disabling I2C 487
22.3.5 Summary the condition could flush TX FIFO 488
22.3.6 The condition could generate START, STOP and RESTART 488

23 Synchronous Serial Interface(SSI) 492

23.1 Overview 492
23.2 Features 492
23.3 Block Diagram 493
23.4 Functional Description 493
23.5 Pin Description 494

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

23.6 Data Formats 494
23.6.1 Motorola's SPI Format Details 495
23.6.2 TI's SSP Format Details 498
23.6.3 National Microwire Format Details 499
23.7 Register Description 501
23.7.1 Registers Mapping 502
23.7.2 Register and Fields Description 502
23.8 Software Guideline 511
23.8.1 Common flow 511
23.8.2 Interrupt Operation 512

24 Synchronous Serial Slave Interface(SSI_SLV) 513

24.1 Overview 513
24.2 Features 513
24.3 Block Diagram 514
24.4 Functional Description 514
24.5 Pin Description 515
24.6 Data Formats 515
24.6.1 Motorola's SPI Format Details 516
24.6.2 TI's SSP Format Details 518
24.6.3 National Microwire Format Details 519
24.7 Register Description 520
24.7.1 Register and Field Descriptions 521
24.8 Software Guideline 535
24.8.1 Configure Flow 535

25 Universal Asynchronous Receiver/Transmitter (UART) 537

25.1 Overview 537
25.2 Features 537
25.3 Block Diagram 537
25.4 Functional Description 538
25.4.1 Full-duplex operation 538
25.4.2 The meaning of all bits 538
25.4.3 RFIFO and TFIFO 538
25.4.4 Transmission, reception and line status Independently 538
25.4.5 Slow infrared asynchronous interface 538
25.5 Pins Description 539
25.6 Data Format Description 539
25.7 Register Description 539
25.7.1 Register Memory Map 540
25.7.2 Register and Fields Description 540
25.8 Operation Flow 555
25.8.1 UART Configuration 555

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

25.8.2 Data Transmission 556
25.8.3 Data Reception 556
25.8.4 Receive Error Handling 556
25.8.5 Modem Transfer 557
25.8.6 DMA Transfer 557
25.8.7 Slow IrDA Asynchronous Interface 557
25.8.8 For any frequency clock to use the UART 558

26 MMC/SD CE-ATA Controller(MSC) 560

26.1 Overview 560
26.2 Features 560
26.3 Block Diagram 561
26.4 Functional Description 561
26.4.1 MSC Reset 562
26.4.2 Voltage Validation 562
26.4.3 Card Registry 562
26.4.4 Card Access 563
26.4.5 Card Status 569
26.4.6 SD Status 572
26.4.7 SDIO 573
26.5 Pins Description 575
26.6 Data Format Description 576
26.7 Register Description 576
26.7.1 Register Memory Map 577
26.7.2 Register and Fields Description 577
26.8 Operation Flow 598
26.8.1 Data FIFOs 598
26.8.2 DMA and Program I/O 599
26.8.3 Start and Stop clock 601
26.8.4 Software Reset 601
26.8.5 Voltage Validation and Card Registry 602
26.8.6 Single Data Block Write 604
26.8.7 Single Block Read 605
26.8.8 Multiple Block Write 605
26.8.9 Multiple Block Read 606
26.8.10 Stream Write (MMC) 607
26.8.11 Stream Read (MMC) 608
26.8.12 Erase, Select/Deselect and Stop 608
26.8.13 SDIO Suspend/Resume 609
26.8.14 SDIO Read Wait 609
26.8.15 Operation and Interrupt 610
26.9 Index 610

27 ON-THE-GO Controller(OTG) 612

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

27.1 Overview 612
27.2 Features 612
27.3 Functional Description 612
27.4 Pins Description 612
27.5 Data Format Description 612
27.6 Register Desciption 613
27.6.1 Register Memory Map 613
27.6.2 Register and Fields Description 615
27.6.3 PHY Register Memory Map 699
27.6.4 PHY Register and Fields Description 699
27.7 PHY VBUS attention 709

28 SC_HASH HDL 710

28.1 Overview 710
28.2 Feature 710
28.3 Registers 710
28.3.1 Register Memory Map 711
28.3.2 Hash Ctrl Register (HSCR) 711
28.3.3 Hash Status Register (HSSR) 712
28.3.4 Hash Interrupt Mask Register (HSINTM) 713
28.3.5 Hash DMA Source Address (HSSA) 713
28.3.6 Hash Transfer Count (HSTC) 713
28.3.7 Hash Data Input Register (HSDI) 714
28.3.8 Hash Data Output Register (HSDO) 714
28.4 Software User Guide 715
28.4.1 HASH running flow 715
28.4.2 Example of MD5 716
28.4.3 Example of SHA1 717
28.4.4 Test Vectors 717
28.5 AHB Interface 717
28.5.1 AHB Slave Interface 717
28.5.2 AHB Master Interface 718

29 AES 722

29.1 Overview 722
29.2 AES engine 722
29.3 Registers 724
29.3.1 Register Memory Map 724
29.3.2 AES Control Register (ASCR) 725
29.3.3 AES Status Register (ASSR) 726
29.3.4 AES Interrupt Mask Register (ASINTM) 726
29.3.5 AES DMA Source Address (ASSA) 727
29.3.6 AES DMA Destination Address (ASDA) 727

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

29.3.7 AES Transfer Count (ASTC) 727
29.3.8 AES Data Input Register (ASDI) 728
29.3.9 AES Data Output Register (ASDO) 728
29.3.10 AES KEY FIFO (ASKY) 729
29.3.11 AES IV FIFO (ASIV) 729
29.4 Software User Guide 730

30 Digital True Random Number Generator（DTRNG） 732

30.1 Overview 732
30.2 Features 732
30.3 Block Diagram 732
30.4 Register Description 732
30.4.1 Register Memory Map 733
30.4.2 Register and Fields Description 733
30.5 Operation Flow 735

31 Fast Ethernet Media Access Controller (MAC) 737

31.1 Overview 737
31.2 Features 737
31.3 Block Diagram 738
31.4 Functional Description 738
31.5 Pins Description 738
31.6 Data Format Description 739
31.7 Register Description 739
31.7.1 Register Memory Map 740
31.7.2 Register and Fields Description 741
31.8 Operation Flow 783

32 Controller Area Network (CAN) 784

32.1 Overview 784
32.2 Features 784
32.3 Brief Introduction 784
32.4 Block Diagram 788
32.5 Pin Description 788
32.6 Register Description 788
32.6.1 Registers Mapping 789
32.6.2 Register and Fields Description 790
32.7 Basic Operations 810
32.7.1 System Configuration 810
32.7.2 Transmitting a Frame 813
32.7.3 Receive a Frame 814
32.8 Test Modes 814
32.8.1 Self Test Mode 814
32.8.2 Self Receive Request 814

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

32.8.3 Self-loop Test Mode 814
32.8.4 Self Test Example 815
32.8.5 Bit Time Configuration Suggestion 815

33 CDBUS 817

33.1 OVERVIEW 817
33.2 Features 817
33.3 Block Diagram 817
33.4 Arbitration Mode(CDBUS-A) 818
33.5 Break Sync Mode(CDBUS-BS) 818
33.6 Pin Description 819
33.7 Registers Description 819
33.7.1 Instructions 819
33.7.2 Map 820
33.7.3 Register and Fields Description 820
33.8 Operation guide 828
33.8.1 Set sys_seq 828
33.8.2 Init cdbus 828
33.8.3 Send data 829
33.8.4 Receive data 829
33.9 Software Notes 829

BOOT 830

34 Boot Read Only Memory(BOOTROM) 831

34.1 Overview 831
34.2 Boot Select 831
34.3 Boot Procedure 831
34.4 Block Diagram 832
34.5 SPL Structure 832
34.6 SPL Paramaters 833
34.7 MSC Boot Specification 836
34.8 SFC boot Specification 837
34.9 USB Boot Specification 840

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

TABLES

Table 3-1 DDRC Register 14
Table 3-2 PHY Registers Address Mapping 46
Table 3-3 LPDDR2 CMD driver strength table 51
Table 3-4 The rx calibreation delay grade 57
Table 3-5 LPDDR2 DQ/DQS ODT Rsistance 64
Table 3-6 LPDDR2 DQ/DQS driving strength 65
Table 3-7 Low Power DLL Setting 68
Table 3-8 per-bit de-skew tuning resolution 69
Table 4-1 EMC Pin Description 98
Table 4-2 Physical Address Space Map 99
Table 4-3 Default Configuration of EMC Chip Select Signals 100
Table 4-4 Registers Memory Map Base Address 108
Table 4-5 Static Memory Interface Registers Map 108
Table 5-1 I/O Pin Description 118
Table 5-2 SFC Registers Map 121
Table 5-3 Terms and Abbreviations 144
Table 6-1 MIPI_CSI Registers Description 148
Table 7-1 MIPI D-PHY RX Registers Map 160
Table 8-1 Input/Output format corresponding relationship 174
Table 8-2 CIM Registers Map 181
Table 9-1 AIC Pins Description 197
Table 9-2 Sample data bit relate to DAC_SDATA/ADC_SDATA bit 202
Table 9-3 Registers Memory Map Base Address 203
Table 9-4 AIC Registers Map 203
Table 9-5 Audio Sampling rate, BIT_CLK and SYS_CLK frequencies 223
Table 9-6 BIT_CLK divider setting 224
Table 9-7 Approximate common multiple of SYS_CLK for all sample rates 225
Table 9-8 CPM/AIC clock divider setting for various sampling rate if PLL = 270.64MHz 225
Table 9-9 PLL parameters and audio sample errors for EXCLK=12MHz 226
Table 10-1DC Registers Map 232
Table 11-1 Registers Memory Map-Address Base 255
Table 11-2 CGU Registers Configuration 255
Table 11-3 Power/Reset Management Controller Registers Configuration 288
Table 12-1 PWM Pins Description 302
Table 12-2 Registers Memory Map Base Address 303
Table 12-3 TCU Registers Map (n = 0~7) 303
Table 13-1 Registers Memory Map-Address Base 332
Table 13-2 PWM Registers Configuration(n=0,1,2,3) 332
Table 14-1 Registers Memory Map Base Address 346

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Table 14-2 SYS_OST Registers Map 346
Table 15-1 Registers Memory Map Base Address..... 353
Table 15-2 WDT Registers Map..... 354
Table 16-1 Registers Memory Map-Address Base 359
Table 16-2 Registers for real time clock..... 359
Table 16-3 Registers for hibernating mode..... 359
Table 16-4 Clock select registers..... 371
Table 17-1 Registers Memory Map-Address Base 372
Table 17-2 INTC Register 373
Table 18-1 Registers Memory Map-Address Base 382
Table 18-2 DMA Channel Registers (n=0~31) 382
Table 18-3 Registers Memory Map-Address Base 383
Table 18-4 Global Control Registers..... 383
Table 18-5 Transfer Request Types..... 385
Table 18-6 Available RDIL..... 388
Table 18-7 TCSM space..... 401
Table 18-8 Descriptor Structure 404
Table 19-1 SADC Analog Pin..... 409
Table 19-2 Registers Memory Map Base Address..... 410
Table 19-3 SADC Registers Map..... 410
Table 20-2 EFUSE Register Description..... 418
Table 21-1 GPIO port summary table illustration 425
Table 21-2 GPIO Port A summary..... 426
Table 21-3 GPIO Port B summary 428
Table 21-4 GPIO Port C summary 429
Table 21-5 GPIO Port D summary 430
Table 21-6 Registers Memory Map Base Address..... 432
Table 21-7 GPIO Registers Group Map..... 432
Table 22-1 I2C Pin Description 450
Table 22-2 Registers Memory Map-Address Base 451
Table 22-3 Registers Memory Map-Address Offset..... 451
Table 23-1 SSI Controller Pins Description..... 494
Table 23-2 Registers Memory Map Base Address..... 502
Table 23-3 SSI Serial Port Registers Map 502
Table 23-4 SSI Interrupts 512
Table 24-1 SSI_SLV Pins Description..... 515
Table 24-2 SSI Serial Port Registers 520
Table 25-1 UART Pins Description 539
Table 25-2 Registers Memory Map Base Address..... 540
Table 25-3 UART Registers Map 540
Table 25-4 UART Interrupt Identification Register Description 545
Table 26-1 Command Data Block Structure 566
Table 26-2 Card Status Description 569

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Table 26-3 SD Status Structure 572
Table 26-4 Registers Memory Map Base Address..... 577
Table 26-5 MSC Registers Map 577
Table 26-6 How to stop multiple block write..... 606
Table 26-7 How to stop multiple block read 606
Table 26-8 Description of Proprietary Vocabulary..... 610
Table 26-9 The mapping between Commands and Steps..... 610
Table 27-1 Registers Memory Map Base Address..... 613
Table 27-2 On-The-Go（OTG） Registers Map..... 613
Table 27-3 Minimum Duration for Soft Disconnect 673
Table 27-4 Registers Memory Map Base Address..... 699
Table 27-5 OTGPHY Registers Map..... 699
Table 27-6 PHY VBUS compare mode 709
Table 28-1 Registers Memory Map-Address Base 711
Table 28-2 HASH registers description.....711
Table 29-1 Registers Memory Map-Address Base 724
Table 29-2 AES registers description..... 724
Table 30-1 Registers Memory Map Base Address..... 733
Table 30-2 DTRNG Registers Map 733
Table 31-1 GMAC pin description 738
Table 31-2 Registers Memory Map Base Address..... 740
Table 31-3 GMAC Registers Map 740
Table 32-1 CAN 2.0B PinsDescription 788
Table 32-2 Registers Memory Map Base Address..... 789
Table 32-3 CAN Memory Map-Address Offset 789
Table 32-4 Bit Locations of a Lost Arbitration when Transmission 799
Table 32-5 Error Locations..... 802
Table 32-6 Coding of the numbers of data bytes by the DLC..... 804
Table 32-7 CANCLK = 24MHz 816
Table 32-8 CANCLK=80MHz 816
Table 32-9 CANCLK=16MHz 816
Table 33-1 CDBUS Pins Description..... 819
Table 33-2 CDBUS Registers Map 820
Table 34-1 Boot Configuration of X1600..... 831
Table 34-2 SPL parameters structure 833
Table 34-3 SPI NOR flash boot flag informations(in spl signature) 839
Table 34-5 Transfer Types Used by the Boot Program..... 840
Table 34-6 Vendor Request 0 Setup Command Data Structure..... 843
Table 34-7 Vendor Request 1 Setup Command Data Structure..... 843
Table 34-8 Vendor Request 2 Setup Command Data Structure..... 843
Table 34-9 Vendor Request 3 Setup Command Data Structure..... 844
Table 34-10 Vendor Request 4 Setup Command Data Structure..... 844
Table 34-11 Vendor Request 5 Setup Command Data Structure 845

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

FIGURES

Figure 1-1 X1600 Diagram 2
Figure 3-1 DDR system block diagram 13
Figure 4-1 Physical Address Space Map 99
Figure 4-2 Example of 16-Bit Data Width SRAM Connection 101
Figure 4-3 Example of 8-Bit Data Width SRAM Connection 101
Figure 4-4 Example of address and data multiplexed memory Connection 101
Figure 4-5 Normal Memory Read Timing 102
Figure 4-6 Normal Memory Write Timing 103
Figure 4-7 Normal Memory Read/Write Timing 103
Figure 4-8 Normal Memory Read Timing With Wait_Pin-1 104
Figure 4-9 Normal Memory Read Timing With Wait_Pin-2 104
Figure 4-10 Normal Memory Write Timing With Wait_Pin 105
Figure 4-11 Burst ROM Read Timing With Wait 106
Figure 4-12 Burst ROM Write Timing With Wait 106
Figure 4-13 Address/Data Multiplexed Memory Read Timing 107
Figure 4-14 Address/Data Multiplexed Memory Write Timing 107
Figure 5-1 SFC Block Diagram 117
Figure 5-2 Sample point(no delay) 118
Figure 5-3 Sample point(delay) 118
Figure 5-4 AC timing 118
Figure 5-5 Data Format(Standard SPI) 119
Figure 5-6 Data Format(Dual SPI) 119
Figure 5-7 Data Format(Quad SPI) 120
Figure 5-8 Multi phases flow 139
Figure 5-9 One phase flow 140
Figure 7-1Functional Block Diagram 159
Figure 9-2 Master Mode Interface to an External I2S/MSB-Justified CODEC Diagram 198
Figure 9-3 Slave Mode Interface to an External I2S/MSB-Justified CODEC Diagram.. 198
Figure 9-4 Master Mode Interface to an External I2S/MSB-Justified CODEC Diagram (Independent Clock Mode) 199
Figure 9-5 Slave Mode Interface to an External I2S/MSB-Justified CODEC Diagram.. 199
Figure 9-6 I2S data format (A: LR mode) 200
Figure 9-7 I2S data format (B: RL mode) 200
Figure 9-8 MSB-justified data format (C: LR mode) 201
Figure 9-9 MSB-justified data format (D: RL mode) 201
Figure 9-10 Transmitting/Receiving FIFO access via APB Bus 219
Figure 9-11 One channel (Left) and Two channels (right) mode (16 bits packed mode)221
Figure 9-12 Four channels (Left) and Six channels (right) mode (16 bits packed mode) 221

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Figure 9-13 Eight channels mode (16 bits packed mode) 221
Figure 9-14 One channel (Left) and Two channels (right) mode 222
Figure 9-15 Four channels (Left) and Six channels (right) mode 222
Figure 9-16 Eight channels mode 222
Figure 9-17 SYS_CLK, BIT_CLK generation scheme 224
Figure 10-1 Top architecture 228
Figure 11-1 Block Diagram of PLL 286
Figure 12-1 Timming of general mode 324
Figure 12-2 Timming of gate mode 325
Figure 12-3 Timming of direction mode 326
Figure 12-4 Timming of quadrature mode 327
Figure 12-5 Timming of pos mode 328
Figure 12-6 Timming of capture mode 329
Figure 12-7 Timming of filter function 330
Figure 12-8 Timing of store function 330
Figure 13-1 PWM Block Diagram 331
Figure 13-2 Register update mode 342
Figure 16-1 Core Power On 369
Figure 18-1 Block Diagram of PDMA 381
Figure 18-2 Descriptor Transfer Flow 405
Figure 18-3 Example for Stride Transfer Mode 406
Figure 19-1 Block Diagram of SADC 409
Figure 22-1 Master Transmitter — Tx FIFO Empties/STOP Generation 489
Figure 22-2 Master Receiver — Tx FIFO Empties/STOP Generation 489
Figure 22-3 Master Transmitter — Restart bit of I2C_DC is set 489
Figure 22-4 Master Receiver — Restart bit of I2C_DC is set 490
Figure 22-5 Master Transmitter — Stop Bit of I2C_DC Set/Tx FIFO Not Empty 490
Figure 22-6 Master Transmitter — First Byte Loaded Into Tx FIFO Allowed to Empty, Restart Bit Set 490
Figure 22-7 Master Receiver — Stop Bit of IC_DATA_CMD Set/Tx FIFO Not Empty .. 491
Figure 22-8 Master Receiver — First Command Loaded After Tx FIFO Allowed to Empty/Restart Bit Set 491
Figure 23-1 SSI Block Diagram 493
Figure 23-2 Standard SPI Single Character Transfer Format (PHA = 0) 495
Figure 23-3 Standard SPI Single Character Transfer Format (PHA = 1) 496
Figure 23-4 Standard SPI Back-to-Back Transfer Format 497
Figure 23-5 Standard SPI Frame Interval Mode Transfer Format (ITFRM = 0, ITFRM= 0) 498
Figure 23-6 Standard SPI Frame Interval Mode Transfer Format (ITFRM = 1, ITFRM = 1) 498
Figure 23-7 TI's SSP Single Transfer Format 499
Figure 23-8 TI's SSP Back-to-back Transfer Format 499
Figure 23-9 National Microwire Format 1 Single Transfer 500

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Figure 23-10 National Microwire Format 1 Back-to-back Transfer 500
Figure 23-11 National Microwire Format 2 Read Timing 501
Figure 23-12 National Microwire Format 2 Write Timing 501
Figure 24-1 SSI_SLV Block Diagram 514
Figure 24-2 Standard Motorola SPI Single Transfer Format (SCPH= 0) 516
Figure 24-3 Standard Motorola SPI Single Transfer Format (SCPH= 1) 517
Figure 24-4Standard Motorola SPI Continus Transfer Format (SCPH=0) 517
Figure 24-5 Standard Motorola SPI Continus Transfer Format (SCPH=1) 518
Figure 24-6TI's SSP Single Transfer Format 518
Figure 24-7 TI's SSP Contious Transfer Format 519
Figure 24-8 Single Slave Microwire Serial Transfer (MDD=0) 519
Figure 24-9 Single Slave Microwire Serial Transfer (MDD=1) 520
Figure 24-10 Slave Microwire Serial Contious Transfer (MDD=1) 520
Figure 25-1 UART DATA Controller Block Diagram 537
Figure 25-2 UART Frame Structure Diagram 539
Figure 26-1 MMC/SD Controller Block Diagram 561
Figure 26-2 msc data format 576
Figure 29-1 ECB mode encoding 722
Figure 29-2 ECB mode decoding 723
Figure 29-3 CBC mode encoding 723
Figure 29-4 CBC mode decoding 723
Figure 30-1 DTRNG Block Diagram 732
Figure 31-2 GMAC configure flow 783
Figure 32-1 CAN Bus 785
Figure 32-2 SFF and EFF 785
Figure 32-3 Error State 787
Figure 32-4 CAN 2.0B Block Diagram 788
Figure 32-5 Timing Diagram 798
Figure 32-6 Transmit Buffer 803
Figure 32-7 Receive Buffer 807
Figure 32-8 CAN basic communication 810
Figure 32-9 Setting Acceptance Filter 812
Figure 32-10 Extended Frame 812
Figure 32-11 Standard Frame 813
Figure 32-12 CAN Self-Loop 815
Figure 33-1 CDBUS Block Diagram 817
Figure 34-1 Boot sequence diagram of X1600 832
Figure 34-2 The basic SPL structure diagram 833
Figure 34-3 SPL configuration change Procedure 835
Figure 34-4 Typical Procedure of MSC0 boot 836
Figure 34-5 SFC Boot Procedure 838
Figure 34-6 USB Communication Flow 841
Figure 34-7 Typical Procedure of USB Boot 842

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Section 1

OVERVIEW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

1 Overview

X1600 is a low power consumption, high performance and high integrated application processor, the application is focus on IoT devices. And it can match the requirements of many other embedded products.

1.1 Block Diagram

Figure 1-1 X1600 Diagram

1.2 Featrue

1.2.1 CPU Core

- XBurst® core
  - XBurst® FPU instruction set supporting both single and double floating point format which are IEEE754 compatible
  - XBurst® 9-stage pipeline micro-architecture, the operating frequency is 1.0GHz
- MMU
  - 32-entry joint-TLB
  - 8 entry instruction TLB
  - 8 entry data TLB
- L1 Cache

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

- 16KB instruction cache
- 16KB data cache

- Hardware debug support
- 16KB tight coupled memory
- L2 Cache
  - 128KB unify cache

1.2.2 Memory Interface

- Integrated DDR on chip
  - Support LPDDR2, DDR2, 16Bit bus width
- SFC Controller
  - 1 group clock and CE pad
  - Support Standard, Dual and Quad SPI DDR protocol
  - Two slave select signal (SFC0_CE0_/ SFC0_CE1_) supporting up to 2 slave devices
  - Clock frequency up to 80MHz in SDR mode
  - Support multiple transfer modes, standard SPI, dual-output/dual-Input SPI, Quad-Output/Quad-Input SPI, Dual-I/O SPI, Quad-I/O SPI, Full Dual-I/O SPI, Full Quad-I/O SPI.

1.2.3 Media Interface

- MIPI-CSI2(v1.0) interface, resolution up to 1280x1080@60fps
  - Support 1-lane, 2-lane mode
- Camera interface module(CIM)
  - Support DVP 8bit / MIPI input, resolution up to 640x480@60fps
  - Support snapshot control
  - Supported data format: RGB888, RGB565, YCbCr 4:2:2, Raw RGB
  - Support convert to luma(Y)
  - Support area luminance
- AIC controller
  - I2S features
    - 8, 16, 18, 20 and 24 bit audio sample data sizes supported, 16 bits packed sample data is supported
    - Up to 8 channels sample data supported
    - DMA transfer mode supported
    - Stop serial clock supported
    - Programmable Interrupt function supported
    - Support share clock mode and split clock mode.
    - Support mono PCM data to stereo PCM data expansion on audio play back
    - Support endian switch on 16-bits normal audio samples play back
    - Internal programmable or external serial clock and optional system clock supported for I2S or MSB-Justified format
    - Two FIFOs for transmit and receive respectively
- Display controller

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

- Input format: RGB888, RGB565, RGB555
- Output interface:
  - MIPI-DBI(SLCD)
    - Support Type A(6800)、Type B(8080), 8-/9-/16-/18-/24-bit bus
    - Support Type C(Serial data transfer interface, 3/4line-spi), 8-/12-/16-/24-bit bus
    - Display size up to 640x480@60Hz, 24BPP
  - MIPI-DPI(TFT)
    - Support 24bit/pixel(R:8bit, G:8bit, B:8bit)
    - Support 18bit/pixel(R:6bit, G:6bit, B:6bit)
    - Support 16bit/pixel(R:5bit, G:6bit, B:5bit)
    - Display size up to 1280x720@60Hz, 24BPP

1.2.4 System Functions

- Clock generation and power management
  - On-chip 12/24/48MHZ oscillator circuit
  - External 32.768KHZ input
  - Three phase-locked loops (PLL) with programmable multiplier
  - CCLK, HHCLK, H2CLK, PCLK, H0CLK, DDR_CLK frequency can be changed separately for software by setting registers
  - Functional-unit clock gating
  - Supply block power shut down
- TCU
  - 8 channels each channel has two pins
  - Support posedge / negedge / dualedge clock counting
  - Support gate counting(only count for gating signal)
  - Support quadrature counting
  - Support direction counting(add / sub because of input signal)
  - Support counting after posedge / negedge signal
  - Support capture counting, output signal high-level time and total cycle time
  - Support exclk / pclk two clock source
- PWM
  - 8 channels, output signal ~50MHz, signal precision ~500MHz
  - Cpu / dma mode to update config
- OS timer
  - 64-bit counter and 32-bit compare register
  - Support interrupt generation when the counter matches the compare register
  - Two clock sources: RTCLK (real time clock), HCLK (system bus clock) selected with 1, 4, 16, 64, 256 and 1024 clock dividing selected
- Watchdog timer
  - Generates WDT reset
  - A 16-bit Data register and a 16-bit counter
- Counter clock uses the input clock selected by software RTC (Real Time Clock)

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

- Need external 32768Hz oscillator for 32k clock generation
- 32-bits second counter
- Programmable and adjustable counter to generate accurate 1 Hz clock
- Alarm interrupt, 1Hz interrupt
- Stand alone power supply, work in hibernating mode
- Power down controller
- Alarm wakeup
- External pin wakeup with up to 2s glitch filter

- Interrupt controller
  - Total 64 interrupt sources
  - Each interrupt source can be independently enabled
  - Priority mechanism to indicate highest priority interrupt
  - All the registers are accessed by CPU
  - Unmasked interrupts can wake up the chip in sleep mode
  - Another set of source, mask and pending registers to serve for PDMA
- PDMA controller
  - Support up to 32 independent DMA channels
  - Descriptor or No-Descriptor Transfer mode
  - A simple Xburst® CPU supports smart transfer mode controlled by programmable firmware
  - Transfer data units: 1-byte, 2-byte, 4-byte, 16-byte, 32-byte, 64-byte, 128-byte
  - Transfer number of data unit: 1 ~ 2^{24} - 1
  - Independent source and destination port width: 8-bit, 16-bit, 32-bit
  - Fixed three priorities of channel groups: 0~3, highest; 4~11: mid; 12~31: lowest
  - An extra INTC IRQ can be bound to one programmable DMA channel
- SAR A/D Controller
  - 4 Channels
  - Resolution: 12-bit
  - Resolution/speed: up to 1.6Msps

1.2.5 Peripherals

- General-Purpose I/O ports
  - Input / output / function port configurable
  - Low/high, rising/falling edge triggering. Every interrupt source can be masked independent
- Two I2C Controller
  - Three speeds
    - Standard mode (100 Kb/s)
    - Fast mode (400 Kb/s)
    - High mode (3.4Mb/s)
  - Device clock is identical with pclk
  - Programmable SCL generator
  - Master or slave I2C operation

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

- 7-bit addressing/10-bit addressing
- 16-level transmit and receive FIFOs
- Interrupt operation
- The number of devices that you can connect to the same I2C-bus is limited only by the maximum bus capacitance of 400pF
- APB interface
- 2 independent I2C channels (I2C0, I2C1)

- One Normal Speed Synchronous serial interfaces (SPI)
  - 3 protocols support: National's Microwire, TI's SSP, and Motorola's SPI
  - Full-duplex or transmit-only or receive-only operation
  - Programmable transfer order: MSB first or LSB first
  - 128 entries deep x 32 bits wide transmit and receive data FIFOs
  - Configurable normal transfer mode or Interval transfer mode
  - Programmable clock phase and polarity for Motorola's SSI format
  - Two slave select signal (SSI0_CE0_ / SSI0_CE1_) supporting up to 2 slave devices
  - Back-to-back character transmission/reception mode
  - Loop back mode for testing
- One Synchronous serial Slave interfaces(SPI Slave)
  - 3 protocols support: National's Microwire, TI's SSP, and Motorola's SPI
  - Full-duplex, transmit-only or receive-only operation for Motorola's SPI and TI's SSP
  - Half-duplex, transmit-only or receive-only operation for National's Microwire
- Four UARTs (UART0, UART1, UART2,UART3)
  - Full-duplex operation
  - 5-, 6-, 7- or 8-bit characters with optional no parity or even or odd parity and with 1, 1½, or 2 stop bits
  - 64x8 bit transmit FIFO and 64x11bit receive FIFO
  - Independently controlled transmit, receive (data ready or timeout), line status interrupts
  - Internal diagnostic capability Loopback control and break, parity, overrun and framing-error is provided
  - Separate DMA requests for transmit and receive data services in FIFO mode
  - Supports modem flow control by software or hardware
  - Slow infrared asynchronous interface that conforms to IrDA specification
  - Support wakeup
- Two MMC/SD/SDIO controllers
  - Fully compatible with the MMC System Specification version 4.2
  - Support SD Specification 2.0
  - Support SD I/O Specification 2.0 with 1 command channel and 4 data channels
  - Consumer Electronics Advanced Transport Architecture (CE-ATA – version 1.1)
  - Maximum data rate is 50MBps
  - Support MMC data width 1bit ,4bit and 8bit
  - Built-in programmable frequency divider for MMC/SD bus
  - Built-in Special Descriptor DMA

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

- Maskable hardware interrupt for SDIO interrupt, internal status and FIFO status
- 128 x 32 built-in data FIFO
- Multi-SD function support including multiple I/O and combined I/O and memory
- IRQ supported enable card to interrupt MMC/SD controller
- Single or multi block access to the card including erase operation
- Stream access to the MMC card
- Supports SDIO read wait, interrupt detection during 1-bit or 4-bit access
- Supports CE-ATA digital protocol commands
- Support Command Completion Signal and interrupt to CPU
- Command Completion Signal disable feature
- The maximum block length is 4096bytes

- USB 2.0 OTG interface
  - Complies with the USB 2.0 standard for high-speed (480 Mbps) functions and with the On-The-Go supplement to the USB 2.0 specification
  - Operates either as the function controller of a high- /full-speed USB peripheral or as the host/peripheral in point-to-point or multi-point communications with other USB functions
  - Supports Session Request Protocol (SRP) and Host Negotiation Protocol (HNP)
  - UTMI+ Level 3 Transceiver Interface
  - Soft connect/disconnect
  - 16 Endpoints
  - Dedicate FIFO
  - Supports control, interrupt, ISO and bulk transfer
  - Support wakeup
  - Support remote-wakeup
- One MAC controller
  - 10/100 Mbps operation
  - Supports RMII PHY interfaces
- CAN2.0B Controller
  - Support CAN 2.0B protocol in ISO-11898-1:2003
  - Arbitration Bit Rate up to 1Mbps
  - Support DMA mode
- CDBUS
  - Support multiple modes: arbitration mode(CDBUS-A), break sync mode(CDBUS-BS), full-duplex and half-duplex
- Security System
  - Xburst®0 MIPS-Based
  - Secret ROM and RAM
  - 16KB Secret ROM
  - 4KB Secret RAM
  - True Random Number Generator
  - Encryption Engine
    - MD5, SHA, SHA2

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

- AES, support 256-bit, 192-bit, 128-bit key size Algorithm
- Support secure boot

- OTP(EFUSE) Slave interface
  - Total 1Kb.

1.2.6 Bootrom

20KB Boot ROM memory.

1.3 IO Devices Physical Memory Map

Module	Start Address	End Address	Size (KB)	Description
DDRC	0x134F0000 0x13012000	0x134F0FFF 0x13012FFF	128	External DDR Controller
DDRPHY	0x13011000	0x13011FFF	64	External DDR PHY
LCD	0x13050000	0x1305FFFF	64	LCD Controller
CIM	0x13060000	0x1306FFFF	64	Camera interface module
INTC	0x10001000	0x10001FFF	4	Interrupt Controller
EMC	0x13410000	0x1341FFFF	64	External Normal Memory/ Boot ROM/ OTP Controller
PDMA	0x13420000	0x1342FFFF	64	DMA Controller
SC_AES	0x13430000	0x1343FFFF	64	AES
SFC	0x13440000	0x1344FFFF	64	High SPI controller
MSC0	0x13450000	0x1345FFFF	64	MSC0 Controller
MSC1	0x13460000	0x1346FFFF	64	MSC1 Controller
SC_HASH	0x13470000	0x1347FFFF	64	SC_HASH
MAC	0x134B0000	0x134BFFFF	64	Fast Ethernet Media Access Controller
PWM	0x134C0000	0x134CFFFF	64	Pulse Modulator Module
OTG	0x13500000	0x1353FFFF	256	OTG 2.0 Controller
EFUSE	0x13540000	0x1354FFFF	64	EFUSE Controller
CDBUS	0x13550000	0x1355FFFF	64	CDBUS Controller
CAN0	0x13560000	0x1356FFFF	64	CAN0 Controller
CAN1	0x13570000	0x1357FFFF	64	CAN1 Controller
CPM	0x10000000	0x10000FFF	4	Clocks and Power Manager
TCU WDT	0x10002000	0x10002FFF	4	Timer/Counter Unit Watchdog Timer
RTC	0x10003000	0x10003FFF	4	Real-Time Clock
GPIO	0x10010000	0x10017FFF	4	General-Purpose I/O
UART0	0x10030000	0x10030FFF	4	UART 0
UART1	0x10031000	0x10031FFF	4	UART 1
UART2	0x10032000	0x10032FFF	4	UART 2
UART3	0x10033000	0x10033FFF	4	UART 3

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

AIC	0x10079000	0x10079FFF	4	AIC controller
SSI0	0x10043000	0x10043FFF	4	Synchronous Serial Interface 0
SSI_SLV0	0x10045000	0x10045FFF	4	Synchronous Serial Slave Interface 0
I2C0	0x10050000	0x10050FFF	4	I2C 0 Bus Interface
I2C1	0x10051000	0x10051FFF	4	I2C 1 Bus Interface
SADC	0x10070000	0x10070FFF	4	SAR A/D Controller
DTRNG	0x10072000	0x10072FFF	4	Digital True Random Number Generator
MIPI_CSI	0x10073000	0x10073FFF	4	MIPI CSI Controller
MIPI-PHY	0x10076000	0x10076FFF	4	MIPI-CSI PHY
USB-PHY	0x10078000	0x10078FFF	4	USB PHY configure interface
SYS_OST	0x12000000	0x12000FFF	4	System OST Controller

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Section 2

CORE FUNCTION

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

2 CPU

2.1 Overview

The CPU of this X1600-SOC is a uni-core implementation has following features.

- Enhanced FPU compliance with MIPS32-ISA
- 16KB L1-Icache, 16KB L1-Dcache for each core
- 128 KB unified L2 cache supporting WB and WT attribute with hardware prefetch

2.2 PRID of X1600-CPU

Processor ID register (CP0 Register 15, select 0) in XBurst CPUs is a read-only register being used to identify implementation detail of each SOC's CPU. Please refer to the programming manual of XBurst CPU for detail of the register. For X1600, its value is 0x00D0000

2.3 Interrupt Mapping

The IP7 ~ IP2 of Cause Register(CP0 Register 13, Seletet0) indicates an interrupt is pending, but only IP2 and IP4 are used in X1600-CPU.

- IP4: OST Interrupt request.
- IP2: INTC Interrupt request.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Section 3

MEMORY INTERFACE

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

3 DDR Controller

3.1 Overview

DDRC (DDR Controller) is a general IP which provides an interface to DDR2 and LPDDR2 memory. The DDRC IP is designed for SOC usage and is configurable, scalable to meet the requirement of various SOC.

3.2 Features

- Multi-port Architecture and asynchronous interface to all port
- Support clock-stop mode
- Support auto-refresh and self-refresh
- Support power-down mode and deep-power-down mode
- Programmable DDR timing parameters
- Programmable DDR row and column address width
- Programmable remapping from Logic address to Physical address

3.3 Supported DDR SDRAM Types

- DDR2
- LPDDR2

Row address width less than 16-bit & Column width less than 12-bit are supported.

3.4 Block Diagram

Following figure shows the functional block diagram of DDR system.

Figure 3-1 DDR system block diagram

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

3.5 DDR Controller Register Description

Following chapter will descript the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. Register read/write attribute
   R - Read only
   W - Write only
   RW - read and write
   RCW - read and write, but clear to 0 by read
   RSW - read and write, but set to 1 by read
   RWC - read and write, clear to 0 by write 1, write 0 has no effect
   RWS - read and write, set to 1 by write 1, write 0 has no effect
   RC - read only, and clear to 0 by read
   RS - read only, and set to 1 by read
   SPEC - special access method, relate to its description
3. Reset Value
   1 - reset to 1
   0 - reset to 0
   ? - value unknown after reset

3.5.1 Register Memory Map

Following table lists the registers of DDR Controller. All of these registers are 32bit. According different configure ports to be access, these registers are divided into 3 groups.

- DDRC_AHB_CFG_GROUP:
  Registers access by AHB2(CH5_AHB)
  Base Address: *0x134F0000 ~ 0x134F0FFF*
- DDRC_APB_CFG_GROUP:
  Registers access by DDRC_APB_Config port
  Base Address: *0xB3012000 ~ 0xB3012FFF*
- DDRP_APB_CFG_GROUP:
  Registers access by DDRP_APB_Config port
  Base Address: *0xB3011000 ~ 0xB3011FFF*

Please Note that: the DDRC_AHB_CFG_GROUP must not be access under retention mode.

Table 3-1 DDRC Register

Name	Group	Address offset	Width	Access	Description

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

DSTATUS	DDRC_AHB	0x00	32	RW	DDR Status Register
DCFG	DDRC_AHB	0x04	32	RW	DDR Configure Register
DCTRL	DDRC_AHB	0x08	32	RW	DDR Control Register
DLMR	DDRC_AHB	0x0C	32	RW	DDR Load-Mode-Register
DTIMING 1	DDRC_AHB	0x60	32	RW	DDR Timing Configure Register 1
DTIMING 2	DDRC_AHB	0x64	32	RW	DDR Timing Configure Register 2
DTIMING 3	DDRC_AHB	0x68	32	RW	DDR Timing Configure Register 3
DTIMING 4	DDRC_AHB	0x6C	32	RW	DDR Timing Configure Register 4
DTIMING 5	DDRC_AHB	0x70	32	RW	DDR Timing Configure Register 5
DTIMING 6	DDRC_AHB	0x74	32	RW	DDR Timing Configure Register 6
DREFCN T	DDRC_AHB	0x18	32	RW	Auto-Refresh Counter
DMMAP0	DDRC_AHB	0x24	32	RW	DDR Memory CS0 Map Configure Register
DMMAP1	DDRC_AHB	0x28	32	RW	DDR Memory CS1 Map Configure Register
DDLP	DDRC_AHB	0xBC	32	RW	DDR DFI low power handshake register
DREMAP 1	DDRC_AHB	0x9C	32	RW	DDR address remapping register1
DREMAP 2	DDRC_AHB	0xA0	32	RW	DDR address remapping register2
DREMAP 3	DDRC_AHB	0xA4	32	RW	DDR address remapping register3
DREMAP 4	DDRC_AHB	0xA8	32	RW	DDR address remapping register4
DREMAP 5	DDRC_AHB	0xAC	32	RW	DDR address remapping register5
DSTRB	DDRC_AHB	0x34	32	RW	Multi-media stride register
WCMDCT RL1	DDRC_AHB	0x100	32	RW	Write command reorder & grouping (Performance control)

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

RCMDCTRL0	DDRC_AHB	0x104	32	RW	Read Channel mode control (Performance control)
RCMDCTRL1	DDRC_AHB	0x108	32	RW	Read Channel mode control (Performance control)
BOUNDAEYSEL	DDRC_AHB	0x10C	32	RW	Channel boundary select
WDATTHD0	DDRC_AHB	0x114	32	RW	Wdata Channel mode control (Performance control)
WDATTHD1	DDRC_AHB	0x118	32	RW	Wdata Channel mode control (Performance control)
IPORTWPRI	DDRC_AHB	0x240	32	RW	Configuration of Internal Priority for write channel (Performance control)
IPORTRPRI	DDRC_AHB	0x244	32	RW	Configuration of Internal Priority for read channel (Performance control)
CHxWDOS	DDRC_AHB	0x200 0x204 0x208 0x20C 0x210 0x214 0x218	32	RW	WQoS configure for each channel (Performance control)
CHxRDOS	DDRC_AHB	0x220 0x224 0x228 0x22C 0x230 0x234 0x238	32	RW	RQoS configure for each channel (Performance control)
AUTOSR_CNT	DDRC_AHB	0x308	32	RW	Auto Self Refresh counter configuration
AUTOSR_EN	DDRC_AHB	0x304	32	RW	Auto Self Refresh enable
EFPRB_CFG	DDRC_AHB	0x30C	32	RW	Bus efficiency probe configuration
EFPRB_VALUE	DDRC_AHB	0x310	32	R	Bus efficiency data
CLKSTP_CFG	DDRC_APB	0x068	32	RW	Auto Clock Gating configuration

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

DDRC_STATUS	DDRC_APB	0x06C	32	R	DDR status
PHYRET_CFG	DDRC_APB	0x034	32	RW	Retention Mode Configuration
EPD_HADDR	DDRC_APB	0x070	32	RW	EPD wake up configure
EPD_LADDR	DDRC_APB	0x074	32	RW	EPD wake up configure
AUTOPRE_CFG	DDRC_APB	0x07C	32	RW	Auto Pre-charge Configuration
PHYRST_CFG	DDRC_APB	0x080	32	RW	DDR Phy reset control
CKC_CFG0	DDRC_APB	0x084	32	RW	Clock change Configuration
PHY_INIT	DDRC_APB	0x08c	32	RW	DFI initial configuration
CKC_CFG1	DDRC_APB	0x088	32	RW	Clock change Configuration
CPM_DRCG		**0xB00000D0**	32	RW	CPM register, DLL & Clock control for DDR

3.5.2 Register and Fields Description

3.5.2.1 DDR Status Register (DSTATUS，0x134F0000)

	DSTATUS																															0x134F0000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DFI_INIT_C	Reserved																							ENDIAN	MISS	DPD	PD	AREF	SREF	CKE1	CKE0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	DFI_INIT_C	0:DFI initialization not completed.(default) 1: DFI initialization completed	R
30:8	Reserved	Writing has no effect, read as zero.	R
7	ENDIAN	0: Little data Endian. 1: Big data Endian.	R
6	MISS	0: No operation miss DDRC memory mapping. (reset value) 1: At least one operation miss DDRC memory mapping.	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		Indicate the accessed address is out of memory mapping range. (This bit is un-writable. Once read this register, this bit will be set to 0)	
5	DPD	0: DDR memory is NOT in deep-power-down state. 1: DDR memory is in deep-power-down state.	R
4	PD	0: DDR memory is NOT in power-down state. 1: DDR memory is in power-down state.	R
3	AREF	0: DDR memory is NOT in auto-refresh state. 1: DDR memory is in auto-refresh state.	R
2	SREF	0: DDR memory is NOT in self-refresh state. 1: DDR memory is in self-refresh state.	R
1	CKE1	0: CKE1 Pin is low 1: CKE1 Pin is high.	R
0	CKE0	0: CKE0 Pin is low. 1: CKE0 Pin is high.	R

3.5.2.2 DDR Configure Register (DCFG，0x134F0004)

Configure the external memory, static configuration only. ie. This register can NOT be changed on-the-fly.

	DCFG																															0x134F0004
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	AN_TE	Reserved	ROW1			COL1			BA1	IMBA	BSL	Reserved	TYPE			ODTEN	MISPE	Reserved	ROW0			COL0			CS1EN	CS0EN	Reserved				BA0	DW
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	AN_TE	Analog test enable.	RW
30	Reserved	Writing has no effect, read as zero.	R
29:27	ROW1	Row Address width. Specify the row address width of external DDR. 000: 12-bit row address(reset value) 001: 13-bit row address 010: 14-bit row address 011: 15-bit row address 100: 16-bit row address 101~111: Reserved	RW
26:24	COL1	Column Address width. Specify the Column address width of external DDR.	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

			Description 000: 8-bit Column address.(reset value) 001: 9-bit Column address 010: 10-bit Column address 011: 11-bit Column address 100: 12-bit Column address 101~111: Reserved	
23	BA1	Bank address width of external memory device. **BA1** / **Description** 0: 4 bank device(reset value) 1: 8 bank device		RW
22	IMBA	0: CS0, CS1 connected 2 memory chips which have same ROW, COL, BA configuration.In this mode, both chips are configured by ROW0,COL0, BA0 . ROW1,COL1,BA1 does not effect the system. 1: CS0, CS1 connected 2 memory chips which have different ROW, COL, BA configuration. Chip0 is configured by ROW0, COL0, BA0;Chip1 is configured by ROW1, COL1, BA1;		RW
21	BSL	Burst length for DDR chips 1: 8 burst 0: 4 burst		RW
20	Reserved	Writing has no effect, read as zero.		R
19:17	TYPE	Select external memory device type. **Bit [19:17]** / **Description** 000: Normal SDR (Single-Data-Rate) SDRAM(Not support).(reset value) 001: Mobile SDR(Not support). 010: Normal DDR1 (Not support) 011: Mobile DDR(Not support). 100: Normal DDR2. 101: LPDDR2. 110: Normal DDR3 (Not support) 111: LPDDR3 (Not support).		RW
16	ODTEN	On-die terminate enable 0: On-die-termination off 1: On-die-termination on		RW
15	MISPE	Missing CS protection Enable. Set 1 to enable. If software access a memory space which is not selected by any CS, controller will return random data to a read operation (or mask write		

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

<table>
<tr><td></td><td></td><td>operation) to avoid system bus being locked. As long as this happens, a flag will set in DSTATUS.miss.</td><td></td></tr>
<tr><td>14</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td>R</td></tr>
<tr><td>13:11</td><td>ROW0</td><td>Row Address width. Specify the row address width of external DDR.
<table>
<tr><th></th><th>Description</th></tr>
<tr><td>000</td><td>12-bit row address(reset value)</td></tr>
<tr><td>001</td><td>13-bit row address</td></tr>
<tr><td>010</td><td>14-bit row address</td></tr>
<tr><td>011</td><td>15-bit row address</td></tr>
<tr><td>100</td><td>16-bit row address</td></tr>
<tr><td>101~111</td><td>Reserved</td></tr>
</table></td><td>RW</td></tr>
<tr><td>10:8</td><td>COL0</td><td>Column Address width. Specify the Column address width of external DDR.
<table>
<tr><th></th><th>Description</th></tr>
<tr><td>000</td><td>8-bit Column address.(reset value)</td></tr>
<tr><td>001</td><td>9-bit Column address</td></tr>
<tr><td>010</td><td>10-bit Column address</td></tr>
<tr><td>011</td><td>11-bit Column address</td></tr>
<tr><td>100</td><td>12-bit Column address</td></tr>
<tr><td>101~111</td><td>Reserved</td></tr>
</table></td><td>RW</td></tr>
<tr><td>7</td><td>CS1EN</td><td>If an DDR memory chip is connected to ddr pin cs1, set CS1EN=1.
<table>
<tr><th>Bit [7]</th><th>Description</th></tr>
<tr><td>0</td><td>DDR Pin CS1 is not in use. (reset value)</td></tr>
<tr><td>1</td><td>DDR Pin CS1 is in use.</td></tr>
</table></td><td>RW</td></tr>
<tr><td>6</td><td>CS0EN</td><td>If an DDR memory chip is connected to ddr pin cs0, set CS1EN=0.
<table>
<tr><th>Bit [6]</th><th>Description</th></tr>
<tr><td>0</td><td>DDR Pin CS0 is not in use. (reset value)</td></tr>
<tr><td>1</td><td>DDR Pin CS0 is in use.</td></tr>
</table></td><td>RW</td></tr>
<tr><td>5:2</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td>R</td></tr>
<tr><td>1</td><td>BA0</td><td>Bank address width of external memory device.
<table>
<tr><th>Bit [1]</th><th>Description</th></tr>
<tr><td>0</td><td>4 bank device(reset value)</td></tr>
<tr><td>1</td><td>8 bank device</td></tr>
</table></td><td>RW</td></tr>
<tr><td>0</td><td>DW</td><td>External DDR Memory Data Width.Specify the external DDR memory data width.
<table>
<tr><th>Bit [0]</th><th>Description</th></tr>
<tr><td>0</td><td>External memory data width is 16-bit.</td></tr>
</table></td><td>RW</td></tr>
</table>

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

				(reset value)		
			1	External memory data width is 32-bit.		

3.5.2.3 DDR Control Register (DCTRL，0x134F0008)

On the positive edge of START, the command selected by CMD field will be performed.

	DCTRL																															0x134F0008
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								DFI_RST	DLL_RST	CTL_RST	CFG_RST	Reserved		KEEPSR	Reserved	ACTPD	PDT			ACTSTP	Reserved				DPD	SR	Reserved		SLOWEXPD	CKE_PULSE	RESET
RST	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:24	Reserved	Writing has no effect, read as zero.	R
23	DFI_RST	DFI interface reset. Set to 0 before initialize DDR PHY.	RW
22	DLL_RST	Reserved, please keep the default value.	R
21	CTL_RST	Reserved, please keep the default value.	R
20	CFG_RST	Reserved, please keep the default value.	R
19:18	Reserved	Writing has no effect, read as zero.	R
17	KEEPSR	inner usage, keep to 0.	
16	Reserved	Writing has no effect, read as zero.	R
15	ACTPD	Active Power-Down. Some SDRAM devices support Active-Power-Down. By default, ACTPD=0, hardware will percharge all active banks before entering Power-Down mode, so called Precharge-Power-Down. By setting ACTPD=1, hardware drives SDRAM into Power-Down mode without precharge all active banks, some banks are still active in Power-Down mode, so called Active-Power-Down. 0: Precharge all banks before entering power-down. 1: Do not precharge all banks before entering power-down.	RW
14:12	PDT	Power-Down Timer. When there's no access to DDR memory for a period of time, hardware drives DDR into power-down mode to save power consumption. Hardware can exit Power-Down mode automatically when new access arrives. If PDT=0, power-down function is disabled. If enable power-down mode, it is recommended to be set after DDR initialization.	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

<table>
<tr><td></td><td></td><td><table><tr><th>Bit [14:13]</th><th>Description</th></tr><tr><td>000</td><td>power-down disabled, hardware never drive SDRAM into power-down mode.</td></tr><tr><td>001</td><td>Enter power-down after 8 tCK idle.</td></tr><tr><td>010</td><td>Enter power-down after 16 tCK idle.</td></tr><tr><td>011</td><td>Enter power-down after 32 tCK idle.</td></tr><tr><td>100</td><td>Enter power-down after 64 tCK idle.</td></tr><tr><td>101</td><td>Enter power-down after 128 tCK idle.</td></tr><tr><td>110 - 111</td><td>Reserved.</td></tr></table></td><td></td></tr>
<tr><td>11</td><td>ACTSTP</td><td>Active Clock-Stop.
0: Clock can be stopped only after all banks be precharged.
1: Clock can be stopped after some bank’s row actived.</td><td>RW</td></tr>
<tr><td>10:7</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td>R</td></tr>
<tr><td>6</td><td>DPD</td><td>Software drives external Mobile DDR device entering Deep-Power-Down mode.
Software set DPD = 1 drives external Mobile DDR device entering Deep-Power-Down mode instead of Power-Down mode, when there’s no access to DDR memory for a period of time. So you must firstly enable Power-Down mode (refer to PDT).
Software needs to reset DDR controller and re-do a complete initial process to exit Deep-Power-Down mode.
When external device goes to Deep-Power-Down mode, it lose all data store in memory and registers.
The memory chip will cut off inner power supply for power saving.</td><td>RW</td></tr>
<tr><td>5</td><td>SR</td><td>Software drive external DDR device entering Self-Refresh mode.
Software set SR=1 drive external DDR device entering self-refresh mode;
Software set SR=0 drive external DDR device exiting self-refresh mode;
In this mode, the CK to external DDR device would be stopped during self-refresh period;
But the clock supplied to ddr_controller logic would not stop.
Software can read & write ddr_controller registers in this mode.
Software can NOT read or write memory data in this mode.
NOTE: Software must guarantee that there’s no memory access during self-refresh mode. Otherwise, software can NOT exit this mode, system would be hang-up!!
<table><tr><th>SR</th><th>Description</th></tr><tr><td>0</td><td>Drive external DDR device exit self-refresh mode.</td></tr><tr><td>1</td><td>Drive external DDR device enter self-refresh mode.</td></tr></table></td><td></td></tr>
</table>

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

4:3	Reserved	Writing has no effect, read as zero.	R
2	SLOWEXPD	Slow exit power-down enable. If set, the controller use DTIMING6.tXSRD value as tXPDLL. **SLOWEXPD** / **Description** 0 / Slow exit power-down disenable. 1 / Slow exit power-down enable.	
1	CKE_PULSE	If set, a CKE pulse will be trigger. This bit is hardware self cleaning. Note:This register is used only for DDR initializing sequence; software should NOT update this register when DDR memory is in normal working mode.	
0	RESET	Module reset for DDR controller. Software is able to reset DDR controller by setting RESET bit high and ends the reset by clear this bit. **RESET** / **Description** 0 / End resetting DDR controller. 1 / Resetting DDR controller.	

3.5.2.4 DDR Load-Mode-Register (DLMR，0x134F000C)

DLMR register is used for initializing the DDR SDRAM memory device.

On the positive edge of START, the command selected by CMD field will be performed.

	DLMR																															0x134F000C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DDR_ADDR																				Reserved	BA			Reserved		CMD			Reserved		START
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:12	DDR_ADDR	When performing a DDR command, DDR_ADDR[13:0]corresponding to external DDR address Pin A[13:0];DDR_ADDR[15:14] are reserved	RW
11	Reserved	Writing has no effect, read as zero.	R
10:8	BA	Bank Address. When performing a DDR command, BA[2:0] corresponding to external DDR address Pin BA[2:0].	
7:6	Reserved	Writing has no effect, read as zero.	R
5:3	CMD	Select command to process when setting START from low to high. On the positive edge of START, one of the following commands will be	

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		performed. <table><tr><th>Bit [5:3]</th><th>Description</th></tr><tr><td>000</td><td>Precharge one bank / All banks. (dependent field : BA, DDR_ADDR)</td></tr><tr><td>001</td><td>Auto-Refresh.</td></tr><tr><td>010</td><td>Load Mode Register. (dependent field : BA, DDR_ADDR)</td></tr><tr><td>011</td><td>ZQCS for DDR3</td></tr><tr><td>100</td><td>ZQCL for DDR3</td></tr><tr><td>101~111</td><td>Reserved.</td></tr></table>	
2:1	Reserved	Writing has no effect, read as zero.	R
0	START	Start to perform a command to external DDR memory. The command is performed on the positive edge of START; Hardware will clear START bit to zero when command issued out to external DDR memory. Write 0 to START will be ignored and take no effect; START=1 means hardware is busy executing current command and can NOT accept new command; Software must check START=0 before writing 1 to START. 0: No command is performed. 1: On the positive edge of START, perform a command defined by CMD field.	

3.5.2.5 DDR Timing Configure Register 1 (DTIMING1，0x134F0060)

The timing parameters are identical to the JEDEC DDR Specification.

If the DDR clock period are tCK.

All these registers's value equal to the number tCK cycle. For example, if tRTP=2, it means 2 tCK between READ and PRECHARGE;

	DTIMMING1																															0x134F0060
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved		tRTP						Reserved		tWTR						Reserved		tWR						Reserved		tWL					
RST	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	1

Bits	Name	Description	RW
31:30	Reserved	Writing has no effect, read as zero.	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

29:24	tRTP	READ to PRECHARGE command period.	RW
23:22	Reserved	Writing has no effect, read as zero.	R
21:16	tWTR	WRITE to READ command delay.	RW
15:14	Reserved	Writing has no effect, read as zero.	R
13:8	tWR	WRITE Recovery Time defined by register MR of DDR2 DDR3 memory.	RW
7:6	Reserved	Writing has no effect, read as zero.	R
5:0	tWL	Write latency, please notice that this version only support AL=0.	RW

3.5.2.6 DDR Timing Configure Register 2 (DTIMING2，0x134F0064)

	DTIMMING2																															0x134F0064
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved		tCCD						Reserved		tRAS						Reserved		tRCD						Reserved		tRL					
RST	0	0	0	0	0	0	2	0	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	1

Bits	Name	Description	RW
31:30	Reserved	Writing has no effect, read as zero.	R
29:24	tCCD	CAS# to CAS# command delay	RW
23:22	Reserved	Writing has no effect, read as zero.	R
21:16	tRAS	ACTIVE to PRECHARGE command period. tRAS defines the ACTIVE to PRECHARGE command period to the same bank.	RW
15:14	Reserved	Writing has no effect, read as zero.	R
13:8	tRCD	ACTIVE to READ or WRITE command period. tRCD defines the ACTIVE to READ/WRITE command period to the same bank.	RW
7:6	Reserved	Writing has no effect, read as zero.	R
5:0	tRL	Read latency, please notice that this version only support AL=0.	RW

3.5.2.7 DDR Timing Configure Register 3 (DTIMING3，0x134F0068)

	DTIMMING3																															0x134F0068
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Reserved	ONUM				tCKSRE			Reserved		tRP						Reserved		tRRD						Reserved		tRC					
RST	0	0	1	0	0	1	0	1	0	0	0	0	0	1	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	1

Bits	Name	Description	RW
31	Reserved	Writing has no effect, read as zero.	R
30:27	ONUM	Keep to 4 in this version.	RW
26:24	tCKSRE	Valid clock after enter self-refresh(tCKSRX = tCKSRE in this version). Delay time is tCKSRE*8 (tCK)	RW
23:22	Reserved	Writing has no effect, read as zero.	R
21:16	tRP	PRECHARGE command period. tRP defines the PRECHARGE to next command period to the same bank.	RW
15:14	Reserved	Writing has no effect, read as zero.	R
13:8	tRRD	ACTIVE bank A to ACTIVE bank B command period. tRRD defines the ACTIVE to ACTIVE command period to different banks.	RW
7:6	Reserved	Writing has no effect, read as zero.	R
5:0	tRC	ACTIVE to ACTIVE command period. tRC defines the ACTIVE to ACTIVE command period to the same bank.	RW

3.5.2.8 DDR Timing Configure Register 4 (DTIMING4，0x134F006C)

	DTIMING4																															0x134F006C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved		tRFC						tEXTRW			tRWCOV			tCKE		Reserved				tMINSR				Reserved	tXP			Reserved		tMRD	
RST	0	0	0	0	1	1	1	1	0	0	1	0	0	0	1	0	0	0	0	0	0	1	0	1	0	1	0	1	0	0	0	1

Bits	Name	Description	RW
31:30	Reserved	Writing has no effect, read as zero.	R
29:24	tRFC	AUTO-REFRESH command period. tRFC defines the minimum delay after an AUTO-REFRESH command. During tRFC period, no command can be issued to DDR memory. Delay Time = (tRFC + 1)*2. **tRFC** | **Description**	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

			000000 — 2 tCK. 000001 — 4 tCK. 000010 — 6 tCK. 000011 — 8 tCK. **… … — … (tRFC + 1)*2 …** 111101 — 126 tCK. 111110 — 128 tCK. 111111 — 130 tCK.	
23:21	tEXTRW	keep the default value.		R
20:19	tRWCOV	keep the default value.		
18:16	tCKE	minimum CKE pulse width. tCKE define the minimum CKE pulse width, include high level and low level. **Bit [18:16] — Description** 000 — 1 tCK. 001 — 2 tCK. 010 — 3 tCK. 011 — 4 tCK. 100 — 5 tCK. 101 — 6 tCK. 110 — 7 tCK. 111 — 8 tCK.		RW
15:12	Reserved	Writing has no effect, read as zero.		R
11:8	tMINSR	Minimum Self-Refresh / Deep-Power-Down time. After DDR memory turns into Self-Refresh or Deep-Power-Down mode, it will NOT exit until tMINSR condition meets. Delay Time = (tMINSR+1) * 8. **Bit [11:8] — Description** 0000 — 8 tCK. 0001 — 16 tCK. 0010 — 24 tCK. 0011 — 32 tCK. **… … — … (tMINSR+1) * 8 …**		RW
7	Reserved	Writing has no effect, read as zero.		R
6:4	tXP	EXIT-POWER-DOWN to next valid command period. tXP defines the EXIT-POWER-DOWN to next valid command period to all banks.		RW
3:2	Reserved	Writing has no effect, read as zero.		R
1:0	tMRD	Load-Mode-Register to next valid command period. tMRD defines the Load-Mode-Register to next valid command period. **tMRD — Description**		

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

			00	1 tCK.		
			01	2 tCK.		
			10	3 tCK.		
			11	4 tCK.		

3.5.2.9 DDR Timing Configure Register 5 (DTIMING5，0x134F0070)

	DTIMMING5																															0x134F0070
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	tCTLUPD								Reserved		tRTW						Reserved		tRDLAT						Reserved		tWDLAT					
RST	1	1	1	1	1	1	1	1	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	1

Bits	Name	Description	RW
31:24	tCTLUPD	Inner usage. Not need to change.	RW
23:22	Reserved	Writing has no effect, read as zero.	R
21:16	tRTW	Read to Write latency.	RW
15:14	Reserved	Writing has no effect, read as zero.	R
13:8	tRDLAT	tRL-2. (when use LPDDR2, set tRDLAT=tRL).	RW
7:6	Reserved	Writing has no effect, read as zero.	R
5:0	tWDLAT	**t**WL-1(when use LPDDR2, set tWDLAT=tWL).	RW

3.5.2.10 DDR Timing Configure Register 6 (DTIMING6，0x134F0074)

	DTIMING6																															0x134F0074
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	tXSRD								Reserved		tFAW						Reserved		tCFGW						Reserved		tCFGR					
RST	1	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	1

Bits	Name	Description	RW
31:24	tXSRD	exit self-refresh to READ delay. Delay time is tXSRD*4 (tCK)	RW
23:22	Reserved	Writing has no effect, read as zero.	R
21:16	tFAW	4-active command window.	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

15:14	Reserved	Writing has no effect, read as zero.	R
13:8	tCFGW	Write PHY configure registers to other commands delay. Not need to change.	RW
7:6	Reserved	Writing has no effect, read as zero.	R
5:0	tCFGR	Ready PHY configure registers to other commands delay. Not need to change.	RW

3.5.2.11 DDR Auto-Refresh Counter (DREFCNT, 0x134f0018)

	DREFCNT																															0x134f0018
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								CON								CNT								Reserved				CLK_DIV			REF_EN
RST	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:24	Reserved	Writing has no effect, read as zero.	R
23:16	CON	A constant value used to compare with the CNT value. After reset, CON=0xFF and CNT=0x00; It is not recommended to set CON=0x00.	
15:8	CNT	8-bit counter; When the value of CNT match the value of CON, flag bit EQU is set high and an auto-refresh command will be issued to DDR memory. READ only.	
7:4	Reserved	Writing has no effect, read as zero.	R
3:1	CLK_DIV	Clock Divider. Divide the dclk to generate a lower frequency of clock to drive the auto-refresh counter. This helps to save power consumption. Set CLK_DIV=0 can disable the clock to auto-refresh counter. When the DDR memory is in self-refresh mode or in deep-power-down mode, disable the clock of auto-refresh counter can save power consumption. Future more, the module clock to DDRC can also be stopped. dclk is CKO clock, When ddr work in 500Mbps, dclk is 250Mhz.	

Bit [3:1]	Description
000	dclk / 16.
001	dclk / 32.
010	dclk / 64.
011	dclk / 128.
100	dclk / 256.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

			101	dclk / 512.		
			110	dclk / 1024.		
			111	--		
0	REF_EN	Enable Refresh Counter. Software set REF_EN=1 right after initialize ddr memory.				

Bit [29]	Description
0	Disenable auto-refresh counter.
1	Enable auto-refresh counter.

3.5.2.12 DDR Memory CS0 Map Configure Register (DMMAP0, 0x134f0024)

The physical base address and size of external DDR Memory can be configured by DMMAP register.

The size of external DDR Memory must be: **2^(24+n), n=0, 1, 2, 3, ….**

When the following equation is met:

(AXI_BUS_Address[31:24] & MASK[7:0]) == BASE

The DDR Memory is selected.

	DMMAP0																															0x134f0024
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																BASE								MASK							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:8	BASE	base address.	RW
7:0	MASK	address mask.	RW

Examples:

1 DDR address space in system memory : 0x2000_0000 ~ 0x2FFF_FFFF (256MB)
   BASE=0x20 MASK=0xF0.

2 DDR address space in system memory : 0x5000_0000 ~ 0x57FF_FFFF (128MB)
   BASE=0x50 MASK=0xF8.

NOTE: If DDRC is disabled, please set DMMAP=0x0000_FF00 (reset value).

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

3.5.2.13 DDR Memory CS1 Map Configure Register (DMMAP1, 0x134f0028)

The physical base address and size of external DDR Memory can be configured by DMMAP register.

The size of external DDR Memory must be: **2^(24+n), n=0, 1, 2, 3, ….**

When the following equation is met:

(AXI_BUS_Address[31:24] & MASK[7:0]) == BASE

The DDR Memory is selected.

	DMMAP1																															0x134f0028
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																BASE								MASK							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:8	BASE	base address.	RW
7:0	MASK	address mask.	RW

Examples:

3 DDR address space in system memory : 0x2000_0000 ~ 0x2FFF_FFFF (256MB)
BASE=0x20 MASK=0xF0.

4 DDR address space in system memory : 0x5000_0000 ~ 0x57FF_FFFF (128MB)
BASE=0x50 MASK=0xF8.

NOTE: If DDRC is disabled, please set DMMAP=0x0000_FF00 (reset value).

3.5.2.14 DDR DFI low power handshake control register (DDLP, 0x134f00BC)

	DDLP																															0x134f00BC
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved													Only	UAR	UZQ	SLP				FLP				Reserved					FSR	FPD	LPEN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:19	Reserved	Writing has no effect. Read as zero.	R
18	Only	Inner usage, keep to 0	RW
17	UAR	Inner usage, keep to 0	RW
16	UZQ	Inner usage, keep to 0	RW
15:12	SLP	slow LP handshake timing register. Just keep it as reset value.	RW
11:8	FLP	fast LP handshake timing register. Just keep it as reset value.	RW
7:3	Reserved	Writing has no effect. Read as zero.	R
2	FSR	1: Use fast lp handshake process during self-refresh. 0: Use slow lp handshake process during self-refresh.	RW
1	FPD	1: Use fast lp handshake process during power down. 0: Use slow lp handshake process during power down.	RW
0	LPEN	DFI low power(lp) interface enable.	RW

3.5.2.15 DDR Address Remapping Register 1 (DREMAP1, 0x134f009C)

	DREMAP1																															0x134f009C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			BIT3MP					Reserved			BIT2MP					Reserved			BIT1MP					Reserved			BIT0MP				
RST	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

3.5.2.16 DDR Address Remapping Register 2 (DREMAP2, 0x134f00A0)

	DREMAP2																															0x134f00A0
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			BIT7MP					Reserved			BIT6MP					Reserved			BIT5MP					Reserved			BIT4MP				
RST	0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	0	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

3.5.2.17 DDR Address Remapping Register 3 (DREMAP3, 0x134f00A4)

	DREMAP3																															0x134f00A4
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			BIT11MP					Reserved			BIT10MP					Reserved			BIT9MP					Reserved			BIT8MP				
RST	0	0	0	0	1	0	1	1	0	0	0	0	1	0	1	0	0	0	0	0	1	0	0	1	0	0	0	0	1	0	0	0

3.5.2.18 DDR Address Remapping Register 4 (DREMAP4, 0x134f00A8)

	DREMAP4																															0x134f00A8
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			BIT15MP					Reserved			BIT14MP					Reserved			BIT13MP					Reserved			BIT12MP				
RST	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	0	0	0	0	0	1	1	0	1	0	0	0	0	1	1	0	0

3.5.2.19 DDR Address Remapping Register 5 (DREMAP5, 0x134f00AC)

	DREMAP5																															0x134f00AC
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			BIT19MP					Reserved			BIT18MP					Reserved			BIT17MP					Reserved			BIT16MP				
RST	0	0	0	1	0	0	1	1	0	0	0	1	0	0	1	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0

DREMAP1~5 are used to define address mapping in DDRC. The “BITnMP” represents address[31:20]. The low 4KB(bit [11:0]) address are reserved without any change. The high 20 bits are configurable. For example, If you want to remap address between address[27:25] and address[14:12], you can set BIT12MP as 0, BIT13MP as 1, BIT14MP as 2, BIT0MP as 12, BIT1MP as 13 and BIT2MP as 14.

Original address:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11~0
1	1	1	1	1	1	1	1	1	1	9	8	7	6	5	4	3	2	1	0	Reserved

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

9	8	7	6	5	4	3	2	1	0											

Remapped address

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11~0
19	18	17	16	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	Reserved

3.5.2.20 Performance wcmd reorder & grouping (WCMDCTRL1, 0x134f0100)

Terminology:

- Priority: priority of command, the command with higher priority will be processed prior to that with lower priority. The priority is generated from:
  1. on-port control signals (hpri, ARPRI, AWPRI)
  2. iport_pri (register configurable for each port)
  3. QoS counter
- Page-hit-conflit:

  Page-hit: wpage-hit

  Page-conflict: the page of write command is conflict with the page of read command. In this case, to guarantee the read-write coherency, the write command must be process prior to read command.

	WCMDCTRL1																															0x134f0100
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserve					wpage_hit_max								pend_qos_cnt												wram_in_use					disable_reorder	msk_empty_wfifo
RST	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bits	Name	Description	RW
31:27	Reserved	Writing has no effect, read as zero.	R
26:19	wpage_hit_max	Wpage-hit affects the reorder of wcmd, the wcmd with same page should be bonded for higher performance. This register indicates the maximum number of wcmd to be bonded. Higher value improves total bandwidth of ddr, but leads to longer read maximum latency.	RW
18:7	pend_qos_cnt	Once the wcmd is accepted, a counter indicates how long the command is pending, when the pending time is exceed	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		Pend_QoS once, the priority of this command will increase 1, up to 3, which increases the priority to be processed. This mechanism avoids the wcmd with lower priority pending too long. Range: 0x001 ~0xFFF **NOTE**: configure step: 1. set d*isable_reorder* to 0. 2. execute *step1* for 14 times 3. set wcmd_pend_qos to expect value 4. set disable_reorder to 1, (Optional) Higher value improves total bandwidth of ddr, but leads to longer maximum latency for write command with lower priority. **Dynamic configuration is not supported.**	
6:2	wram_in_use	0~12. Ram to be used in write command reorder. Reduction of this number leads to poor performance. **Configuration is not recommended**	RW
1	disable_reorder	0: wcmd will be reordered based on priority and page-hit-conflict 1: wcmd will not be reordered, the commands will be process with the order of being received. **Dynamic configuration is not recommended.**	RW
0	msk_empty_wfifo	0: wcmd is involved in arbitration immediately. 1: wcmd is not involved in arbitration until receives enough wdata.	RW

3.5.2.21 Performance rcmd request control (RCMDCTRL0, 0x134f0104)

Terminology:

rfifo_thd: read fifo threshold. Read command is not involved in arbitration until the vacancy in rfifo is higher than rfifo threshold. This should improves the ddr performance when processing accessing discrete pages. However, for page-access (commands access the same page continuously) the performance will be lagged as the threshold affects the command grouping.

rcmd_igr_cflit: guarantee coherency between wcmd and rcmd. If the coherency if not required in some application (such as LCD), ignoring of confliction would improve ddr read performance.

	RCMDCTRL0																															0x134f0104
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	ch3_rcmd_igr_cflit	ch3_rfifo_thd_en	ch3_rfifo_thd						Reserved								ch1_rcmd_igr_cflit	ch1_rfifo_thd_en	ch1_rfifo_thd						Reserved							
RST	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0	0	0

Bits	Name	Description	RW
31	ch3_rcmd_igr_cflit	1: enable. Consistence between wcmd and rcmd will not be guaranteed. 0: disable.	RW
30	ch3_fifo_thd_en	0: disable rfifo_thd (recommanded) 1: enable rfifo_thd	RW
29:24	ch3_rfifo_thd	If Ch3 rfifo level threshold higher than this value, rcmd request is masked	RW
23:16	Reserved	Writing has no effect, read as zero.	R
15	ch1_rcmd_igr_cflit	1: enable. Consistence between wcmd and rcmd will not be guaranteed. 0: disable.	RW
14	ch1_fifo_thd_en	0: disable rfifo_thd (recommanded) 1: enable rfifo_thd	RW
13:8	ch1_rfifo_thd	If Ch3 rfifo level threshold higher than this value, rcmd request is masked	RW
7:0	Reserved	Writing has no effect, read as zero.	R

3.5.2.22 Performance rcmd request control (RCMDCTRL1, 0x134f0108)

	RCMDCTRL1																															0x134f0108
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																Ch5_rcmd_igr_cflit	Ch5_rfifo_thd_en	Ch5_rfifo_thd						Ch4_rcmd_igr_cflit	Ch4_rfifo_thd_en	Ch4_rfifo_thd					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	1	0	0	0

Bits	Name	Description	Reset
31:16	Reserved	Writing has no effect, read as zero.	R
15	ch5_rcmd_igr_cflit	0: disable rfifo_thd (recommended) 1: enable rfifo_thd	RW
14	ch5_fifo_thd_en	1: enable. consistence between wcmd and rcmd will not be	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		guaranteed. 0: disable.	
13:8	ch5_rfifo_thd	If Ch1 rfifo level threshold higher than this value, rcmd request is masked	RW
7	ch4_rcmd_igr_cflit	0: disable rfifo_thd (recommended) 1: enable rfifo_thd	RW
6	ch4_fifo_thd_en	1: enable. consistence between wcmd and rcmd will not be guaranteed. 0: disable.	RW
5:0	ch4_rfifo_thd	If Ch1 rfifo level threshold higher than this value, rcmd request is masked	RW

3.5.2.23 Channel boundary select (BOUNDARYSEL, 0x134f010C)

	BOUNDARYSEL																															0x134f010C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	CH6_block_wready	CH5_block_wready	CH4_block_wready	CH3_block_wready	CH2_block_wready	CH1_block_wready	CH0_block_wready	Reserved								CH7_boundary		CH6_boundary		CH5_boundary		CH4_boundary		CH3_boundary		CH2_boundary		CH1_boundary		CH0_boundary	
RST	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	Reset
31	Reserved	Writing has no effect, read as zero.	R
30	CH6_block_wready	0: No wready block (default) 1: Wready bolck Debug usage, don't change this bit	RW
29	CH5_block_wready	0: No wready block (default) 1: Wready bolck Debug usage, don't change this bit	RW
28	CH4_block_wready	0: No wready block (default) 1: Wready bolck Debug usage, don't change this bit	RW
27	CH3_block_wready	0: No wready block (default) 1: Wready bolck Debug usage, don't change this bit	RW
26	CH2_block_wready	0: No wready block (default) 1: Wready bolck Debug usage, don't change this bit	RW
25	CH1_block_wready	0: No wready block (default)	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		1: Wready bolck Debug usage, don't change this bit	
24	CH0_block_wready	0: No wready block (default) 1: Wready bolck Debug usage, don't change this bit	RW
23:16	Reserved	Writing has no effect, read as zero.	R
15:14	CH7_boundary	0: 512byte boundary (default) 1: 1024byte boundary 2: 2048byte boundary 3: 4096byte boundary	RW
13:12	CH6_boundary	0: 512byte boundary (default) 1: 1024byte boundary 2: 2048byte boundary 3: 4096byte boundary	RW
11:10	CH5_boundary	0: 512byte boundary (default) 1: 1024byte boundary 2: 2048byte boundary 3: 4096byte boundary	RW
9:8	CH4_boundary	0: 512byte boundary (default) 1: 1024byte boundary 2: 2048byte boundary 3: 4096byte boundary	RW
7:6	CH3_boundary	0: 512byte boundary (default) 1: 1024byte boundary 2: 2048byte boundary 3: 4096byte boundary	RW
5:4	CH2_boundary	0: 512byte boundary (default) 1: 1024byte boundary 2: 2048byte boundary 3: 4096byte boundary	RW
3:2	CH1_boundary	0: 512byte boundary (default) 1: 1024byte boundary 2: 2048byte boundary 3: 4096byte boundary	RW
1:0	CH0_boundary	0: 512byte boundary (default) 1: 1024byte boundary 2: 2048byte boundary 3: 4096byte boundary	RW

3.5.2.24 performance wcmd request control (WDATTHD0, 0x134f0114)

Terminology:

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Wfifo_thd: wdata fifo threshold. In axi port, as the wdata might be far behind of wcmd. The threshold guarantees the wcmd will not be involved in arbitration until receive enough wdata.

11

	WDATTHD0																															0x134f0114
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	Ch3_wfifo_thd_en	Ch3_wfifo_thd						Reserved									Ch1_wfifo_thd_en	Ch1_wfifo_thd						Reserved							
RST	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	1	0	0	0

Bits	Name	Description	RW
31	Reserved	Writing has no effect, read as zero.	R
30	Ch3_wfifo_thd_en	1: Enable 1: Disable (recommended)	RW
29:24	Ch3_wfifo_thd	Wcmd is involved in arbitration before receiving all wdata.	RW
23:15	Reserved	Writing has no effect, read as zero.	R
14	Ch1_wfifo_thd_en	1: Enable 1: Disable (recommended)	RW
13:8	Ch1_wfifo_thd	Wcmd is involved in arbitration before receiving all wdata.	RW
7:0	Reserved	Writing has no effect, read as zero.	R

3.5.2.25 performance wcmd request control (WDATTHD1, 0x134f0118)

	WDATTHD1																															0x134f0118
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																	Ch5_wfifo_thd_en	Ch5_wfifo_thd						Reserved	Ch4_wfifo_thd_en	Ch4_wfifo_thd					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	1	0	0	0

Bits	Name	Description	RW
31:15	Reserved	Writing has no effect, read as zero.	R
14	Ch5_wfifo_thd_en	1: Enable 1: Disable (recommended)	RW
13:8	Ch5_wfifo_thd	Wcmd is involved in arbitration before receiving all wdata.	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

7	Reserved	Writing has no effect, read as zero.	R
6	Ch4_wfifo_thd_en	1: Enable 1: Disable (recommended)	RW
5:0	Ch4_wfifo_thd	Wcmd is involved in arbitration before receiving all wdata.	RW

3.5.2.26 performance priority control (IPORTPRI, 0x134f0240)

Terminology:

Priority affects on arbitration between ports. Transfers with higher priority will be grant first

Port_pri: priority provided by masters.

Iport_pri: register configurable which applies to each ports. The finial priority is the larger value of port_pri and iport_pri.

	IPORTWPRI																															0x134f0240
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								Ch7_iport_wpri_en	Ch6_iport_wpri_en	Ch5_iport_wpri_en	Ch4_iport_wpri_en	Ch3_iport_wpri_en	Ch2_iport_wpri_en	Ch1_iport_wpri_en	Ch0_iport_wpri_en	Ch7_iport_wpri		Ch6_iport_wpri		Ch5_iport_wpri		Ch4_iport_wpri		Ch3_iport_wpri		Ch2_iport_wpri		Ch1_iport_wpri		Ch0_iport_wpri	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	IPORTRPRI																															0x134f0244
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								Ch7_iport_rpri_en	Ch6_iport_rptr_en	Ch5_iport_rptr_en	Ch4_iport_rptr_en	Ch3_iport_rptr_en	Ch2_iport_rptr_en	Ch1_iport_rptr_en	Ch0_iport_rptr_en	Ch7_iport_rptr		Ch6_iport_rptr		Ch5_iport_rptr		Ch4_iport_rptr		Ch3_iport_rptr		Ch2_iport_rptr		Ch1_iport_rptr		Ch0_iport_rptr	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:24	Reserved	Writing has no effect, read as zero.	R
23:16	Chn_iport_wpri_en Chn_iport_rpri_en	Enable iport_pri (iport_wpri is write channel priority, Iport rpri is read channel priority) 0: disable, use external priority 1: enable, use the max priority of external and internal priority	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

15:0	Chn_iport_wpri Chn_iport_rpri	Priority of channel 0x3: the highest priority ... 0x0: the lowest priority	RW

3.5.2.27 performance QoS control (CHxQOS0,1,2,3,4,5)

Terminology:

Qos: Generally speaking, the Qos controller is a timer, it indicates the how long the command is pending. Once the timer exceed predefined threshold (con), the priority increases by 1, up to top-limit (max). The higher priority is, the sooner it will be processed. This register affects the latency.

	CHxWQOS0,1,2,3,4,5,6																0x134f0200,204,208,20C,210,214,218															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Qos_en	Outstanding_en	Reserved												max		con															
RST	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

	CHxRQOS0,1,2,3,4,5,6																0x134f0300,304,308,30C,310,314,318															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Qos_en	Outstanding_en	Reserved												max		con															
RST	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	Qos_en	enable	RW
30	Outstand_en	Outstand enable	RW
29:18	Reserved	Writing has no effect, read as zero.	R
17:16	Max	Up-limit of priority	RW
15:0	Con	Threshold of timer	RW

3.5.2.28 Auto Self Refresh counter configuration (AUTOSR_CNT, 0xB3010308)

Terminology:

AUTOSR: auto self-refresh. When the DDRC bus interface is idle for some time, the DDRC

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

can issue a command to put the DRAM into self-refresh mode. This will same much power in off-chip DRAM.

	AUTOSR_CNT																															0xB3010308
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved												BUS_IDLE_CNT																			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:20	Reserved	Writing has no effect, read as zero.	R
19:0	BUS_IDLE_CNT	Timer Cnt: when the bus interface is idle(all transfer are finished), the internal timer is going to run, after the Timer Cnt is meet, DDR issues Self-Refresh command.	RW

3.5.2.29 Auto Self Refresh enable (AUTOSR_EN, 0xb3010304)

	AUTOSR_EN																															0xb3010304
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															AUTOSR_EN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect, read as zero.	R
0	BUS_IDLE_EN	0: disable auto self-refresh 1: enable auto self-refresh	RW

3.5.2.30 Auto Clock Gating configuration (CLKSTP_CFG, 0xB3012068)

Description:

Under certain condition, the DDRC input clock can be stopped for power saving. For example, when the SDRAM is in self-refresh mode, the clock can be stop.

	CLKSTP_CFG																															0xB3012068
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	clkstp_en	idle_cond_en	lp_cond_en	sr_cond_en	Reserved																dly_timer											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Name	Description	RW
31	clkstp_en	Function enable	RW
30	idle_cond_en	Enable judge condition: ddrc idle	RW
29	lp_cond_en	Enable judge condition: low-power mode (DCTRL.PDT)	RW
28	sr_cond_en	Enable judge condition: self-refresh	RW
27:12	Reserved	Writing has no effect, read as zero.	R
11:0	dly_timer	Specify the time before shutting down the clock after all condition met.	RW

Please Note that:

The CLKSTP will affect the function of lp(low power mode), auto-sr(auto self-refresh)mode. If the Clock is gating, the timer used for lp/auto-sr will stop running. As a result, if the Auto-self-refresh enabled, the bit [28] should be set.

3.5.2.31 DDR status (DDRC_STATUS, 0xB301206C)

Description:

Read-Only register indicates the ddrc status. This register can be accessed even in DDR retention mode.

	DDRC_STATUS																															0xB301206C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved													ckc_reject	ckc_ack	ckc_req	Reserved		ddr_sr_mode	ddr_lp_mode	ddrc_idle	ch6_bus_idle	ch5_bus_idle	ch4_bus_idle	ch3_bus_idle	ch2_bus_idle	ch1_bus_idle	ch0_bus_idle	Reserved			clkstp_req
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:19	Reserved	Writing has no effect, read as zero.	R
18	ckc_reject		R
17	ckc_ack		R
16	ckc_req		R
15:14	Reserved	Writing has no effect, read as zero.	R
13	ddr_sr_mode	0: DRAM is not in self-refresh mode 1: DRAM is in self-refresh mode	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

12	ddr_lp_mode	0: ddr PHY is not in low-power mode 1: ddr PHY is in low-power mode	R
11	ddrc_idle	Indicates the ddrc control logic is idle	R
10:4	ch*x*_bus_idle	Indicates the bus interface for each channel is idle	R
3:1	Reserved	Writing has no effect, read as zero.	R
0	clkstp_req	Indicates the ddrc is requiring CPM gating ddrc clock	R

3.5.2.32 Retention Mode Configuration (PHYRET_CFG, 0xB3012034)

Description:

DDR PHY can be set into retention mode, which allow power cutting-down. This can save the leakage power in highest level.

However, when use this function, please flow the retention flow.

	PHYRET_CFG																															0xB3012034
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																			cfg_iso_en	Reserved			phy_iso_en	Reserved			clk_iso_en	Reserved	bufferen_core	ret_en_n	ret_en
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	1	0

Bits	Name	Description	RW
31:13	Reserved	Writing has no effect, read as zero.	R
12	cfg_iso_en	PHY output prdata isolation enable	RW
11:9	Reserved	Writing has no effect, read as zero.	R
8	phy_iso_en	PHY output dfi signal isolation enable (high-active)	RW
7:5	Reserved	Writing has no effect, read as zero.	R
4	clk_iso_en	PHY output clock isolation enable	RW
3	Reserved	Writing has no effect, read as zero.	R
2	bufferen_core	Bufferen_core enable: low-active.	RW
1	ret_en_n	Retention enable: low-active	RW
0	ret_en	Retention enable: High-active (make sure: ret_en = ~ret_en_n)	RW

3.5.2.33 DDR Phy reset control (PHYRST_CFG, 0xB3012080)

Soft Reset of DDRC

	REG_NAME																															0xB3012080
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Reserved							dfi_reset	dll_reset	ctl_reset	cfg_reset	Reserved																				phy_reset
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:25	Reserved	Writing has no effect, read as zero.	R
24	dfi_reset	Soft reset of dfi	RW
23	dll_reset	Soft reset of dll	RW
22	ctl_reset	Soft reset of ctl	RW
21	cfg_reset	Soft reset of cfg	RW
20:1	Reserved	Writing has no effect, read as zero.	R
0	phy_reset	Soft reset of PHY	RW

3.5.2.34 DFI initial configuration (PHY_INIT, 0xB301208c)

	PHY_INIT																															0xB301208c
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																													ddr_plllock	init_complete	Init_start
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:3	Reserved	Writing has no effect, read as zero.	R
2	ddr_plllock	0: PLL UNLOCKED 1: PLL LOCKED PHY output	R
1	init_complete	PHY output dfi_init_complete signal	R
0	init_start	0: configure signal dfi_init_start low 1: configure signal dfi_init_start high	RW

3.5.2.35 CPM register, DLL & Clock control for DDR (CPM_DRCG, 0xB00000D0)

	CPM_DRCG																															0xB00000D0
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Reserved																									GATEN	Reserved			CFGRST	DLLRESET	Reserved
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Name	Description	RW
31:7	Reserved	Inner usage, keep in default value	R
6	GATEN	Inner usage, keep to 1	RW
5:3	Reserved	Writing has no effect, read as zero.	R
2	CFGRST	1: reset the DDR PHY Configure Port 0: disable the reset.	RW
1	DLLRESET	1: reset the DLL in DDR PHY 0: disable the reset.	RW
0	Reserved	Inner usage, keep in default value	RW

3.6 DDR PHY Register Description

Note： PHY registers aligned in byte

Following table lists the registers of DDR PHY..

PHY_APB:

Registers access by APB

Base Address: *0x13011000 ~ 0x13011FFF*

3.6.1 Register Memory Map

Table 3-2 PHY Registers Address Mapping

Name	Group	Address offset	Width	Access	Description
PHY_RST	DDRP_APB	0x000	8	RW	RHY reset register
MEM_CFG	DDRP_APB	0x004	8	RW	Memory configure register
TRAIN_CTRL	DDRP_APB	0x008	8	RW	Training control register
WL_MODE1	DDRP_APB	0x00c	8	RW	Write leveling load mode1 register
WL_MODE2	DDRP_APB	0x010	8	RW	Write leveling load mode2 register
CL	DDRP_APB	0x014	8	RW	CL register

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

AL	DDRP_APB	0x018	8	RW	AL register
CWL	DDRP_APB	0x01c	8	RW	CWL register
CMD_NRCOMP	DDRP_APB	0x040	8	RW	CMD NRCOMP register
CMD_PRCOMP	DDRP_APB	0x044	8	RW	CMD PRCOMP register
CK/CKB_NRCOMP	DDRP_APB	0x048	8	RW	CK/CKB NRCOMP register
CK/CKB_NRCOMP	DDRP_APB	0x04c	8	RW	CK/CKB PRCOMP register
PU/PD	DDRP_APB	0x050	8	RW	CMD weak pull up/down register
CMD_DLL	DDRP_APB	0x054	8	RW	CMD DLL register
CK_DLL	DDRP_APB	0x058	8	RW	CMD CK DLL register
DFILP_RESP	DDRP_APB	0x060	8	RW	Response timing register
DQ_WIDTH	DDRP_APB	0x07c	8	RW	DQ Width register
PLL_FBDIV	DDRP_APB	0x080	8	RW	PLL feed back divider register
PLL_CTRL	DDRP_APB	0x04	8	RW	PLL control register
PLL_PDIV	DDRP_APB	0x088	8	RW	PLL divider register
WL_DONE	DDRP_APB	0x0c0	8	R	PHY write-leveling done register
PLL_LOCK	DDRP_APB	0x0c8	8	R	PLL lock register
CALIB_DONE	DDRP_APB	0x0cc	8	R	Calibration done register
INIT_COMP	DDRP_APB	0x0d0	8	R	PHY initialize complete
PHY_BIST	DDRP_APB	0x0d8	8	R	The bist complete flag and the bist result
TXDLL_DQML	DDRP_APB	0x110	8	RW	TX DLL delay of DQ[7:0] and DM[0]
TXDLL_DQSB0	DDRP_APB	0x114	8	RW	TX DLL delay of DQS[0] and DQSB[0]
TXDLL_DQMH	DDRP_APB	0x150	8	RW	TX DLL delay of DQ[15:8] and DM[1]

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

TXDLL_DQSB1	DDRP_APB	0x154	8	RW	TX DLL delay of DQS[1] and DQSB[1]
RXDLL_DQSB0	DDRP_APB	0x120	8	RW	RX DLL delay of DQS[0] and DQSB[0]
RXDLL_DQSB1	DDRP_APB	0x160	8	RW	RX DLL delay of DQS[1] and DQSB[1]
PDODT_DQL	DDRP_APB	0x100	8	RW	Pull-down ODT resistance for DQ[7:0]
PUODT_DQL	DDRP_APB	0x104	8	RW	Pull-up ODT resistance for DQ[7:0]
PDDRI_DQL	DDRP_APB	0x108	8	RW	Pull-down driving resistance for DQ[7:0]
PUDRI_DQL	DDRP_APB	0x10c	8	RW	Pull-up driving resistance for DQ[7:0]
PDODT_DQH	DDRP_APB	0x140	8	RW	Pull-down ODT resistance for DQ[15:8]
PUODT_DQH	DDRP_APB	0x144	8	RW	Pull-up ODT resistance for DQ[15:8]
PDDRI_DQH	DDRP_APB	0x148	8	RW	Pull-down driving resistance for DQ[15:8]
PUDRI_DQH	DDRP_APB	0x14c	8	RW	Pull-up driving resistance for DQ[15:8]

3.6.2 Register and Fields Description

3.6.2.1 DDR PHY RST

																									PHY_APB_BASE+0x000							
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												SRST1	SRST0	Reserved	SRST
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1

Bits	Name	Description	RW
[3]	SRST1	soft reset digital core, active low	RW
[2]	SRST0	soft reset analog core, active low	RW
[0]	SRST	Reset initial status, active low	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

3.6.2.2 DDR PHY MEM_CFG

	MEM_CFG																											PHY_APB_BASE+0x004			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											BSTSEL	Reserved		MEMSEL	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Name	Description	RW
[4]	BSTSEL	Burst select calibration 0: Reserved 1: burst8	RW
[1:0]	MEMSEL	memory select 3: LPDDR2 2: LPDDR3	RW

3.6.2.3 DDR PHY TRAINING_CTRL

	TRAINING_CTRL																											PHY_APB_BASE+0x008			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										DGCCS		WLBYPASS	WLCTRL	DSCSE	DSACE
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
[5:4]	DGCCS	DQS gating calibration CS select signal. 10: select CS0 Others:reserved	RW
[1]	DSCSE	DQS gating calibration bypass mode, active high 1:register bypass mode 0:no bypass mode	RW
[0]	DSACE	DQS gating calibration control, active high 1: Enable. 0: Disable.	RW

3.6.2.4 DDR PHY CL

	CL																											PHY_APB_BASE+0x014			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Reserved																												CL			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

Bits	Name	Description	RW
[3:0]	CL	LPDDR3/2 CAS Read Latency Note: When the phy choose the LPDDR3/2 mode, this value should keep the same value to the value of the SDRAM RL.	RW

3.6.2.5 DDR PHY AL

	AL																PHY_APB_BASE+0x018															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												AL			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
[3:0]	AL	LPDDR3/2 Additional Latency Note: Please keep zero when the phy choose the LPDDR3/2.	RW

3.6.2.6 DDR PHY CWL

	CWL																PHY_APB_BASE+0x01c															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												CWL			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
[3:0]	CWL	LPDDR3/2 CAS Write Latency Note: When the phy choose the LPDDR3/2 mode, this value should keep the same with WL.	RW

3.6.2.7 DDR CMD NRCOMP

																	PHY_APB_BASE+0x2c0															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Reserved																															CMD_NRCOMP				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0

Bits	Name	Description	CMD RW
[4:0]	CMD_NRCOMP	CMD NRCOMP, except for CK/CKB. The larger the value, the stronger the drive strength. The resistance relation with the configuration show in Table 3-3.	RW

Table 3-3 LPDDR2 CMD driver strength table

Control bit	5'b11111	5'b11110	5'b11101	5'b11100	units
pull-up	20.91	21.86	22.9	24.05	ohm
pull-down	20.91	21.86	22.9	24.05	ohm
Control bit	5'b11011	5'b11010	5'b11001	5'b11000	units
pull-up	25.31	26.72	28.29	30.06	ohm
pull-down	25.31	26.72	28.29	30.06	ohm
Control bit	5'b10111	5'b10110	5'b10101	5'b10100	units
pull-up	32.06	34.35	37	40.08	ohm
pull-down	32.06	34.35	37	40.08	ohm
Control bit	5'b10011	5'b10010	5'b10001	5'b10000	units
pull-up	43.72	48.1	53.44	60.12	ohm
pull-down	43.72	48.1	53.44	60.12	ohm
Control bit	5'b01111	5'b01110	5'b01101	5'b01100	units
pull-up	32.06	34.35	37	40.08	ohm
pull-down	32.06	34.35	37	40.08	ohm
Control bit	5'b01011	5'b01010	5'b01001	5'b01000	units
pull-up	43.72	48.1	53.44	60.12	ohm
pull-down	43.72	48.1	53.44	60.12	ohm
Control bit	5'b00111	5'b00110	5'b00101	5'b00100	units
pull-up	68.71	80.16	96.19	120.2	ohm
pull-down	68.71	80.16	96.19	120.2	ohm
Control bit	5'b00011	5'b00010	5'b00001	5'b00000	units
pull-up	160.3	240.5	481	+∞	ohm
pull-down	160.3	240.5	481	+∞	ohm

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

3.6.2.8 DDR CMD PRCOMP

																																PHY_APB_BASE+0x2c4
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											CMD_PRCOMP				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0

Bits	Name	Description	RW
[4:0]	CMD_PRCOMP	CMD PRCOMP, except for CK/CKB. The larger the value, the stronger the drive strength. The resistance relation with the configuration show in Table 3-3.	RW

3.6.2.9 DDR CK/CKB NRCOMP

																																PHY_APB_BASE+0x2c8
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											CK_NRCOMP				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0

Bits	Name	Description	RW
[4:0]	CK_NRCOMP	CK/CKB NRCOMP. The larger the value, the stronger the drive strength. The resistance relation with the configuration show in Table 3-3.	RW

3.6.2.10 DDR CK/CKB PRCOMP

																																PHY_APB_BASE+0x2cc
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											CK_PRCOMP				

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0

Bits	Name	Description	RW
[4:0]	CK_PRCOMP	CK/CKB PRCOMP. The larger the value, the stronger the drive strength. The resistance relation with the configuration show in Table 3-3.	RW

3.6.2.11 DDR Weak Pull Up/Down

																															PHY_APB_BASE+0x2d0	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														CMDWPU	CMDWPD
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Name	Description	RW
[1]	CMDWPU	CMD weak pull up enable, active high	RW
[0]	CMDWPD	CMD weak pull down enable, active high	RW

3.6.2.12 DDR CMD DLL

																															PHY_APB_BASE+0x054	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												CMDDLL_en	CMDDLL_delay		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0

Bits	Name	Description	RW
[3]	CMDDLL_en	CMD DLL Enable	RW
[2:0]	CMDDLL_delay	CMD DLL delay 0: no delay 1: 22.5° delay 2: 45° delay 3: 67.5° delay 4: 90° delay 5: 112.5° delay 6: 135° delay 7: 157.5° delay	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

3.6.2.13 DDR CK DLL

																	PHY_APB_BASE+0x058															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												CKDLL_Phase	CKDLL_Delay		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
[3]	CKDLL_Phase	CK DLL clock phase select in bypass mode 0: no delay 1: 90 degree	RW
[2:0]	CKDLL_Delay	CK DLL delay 0: no delay 1: 22.5° delay 2: 45° delay 3: 67.5° delay 4: 90° delay 5: 112.5° delay 6: 135° delay 7: 157.5° delay	RW

3.6.2.14 DDR DFI LP Response Timing

																	PHY_APB_BASE+0x060															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								Resptm_ack				Resptm_req			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

Bits	Name	Description	RW
[7:4]	Resptm_ack	The response timing when high the dfi_lp_ack. Unit: dfi_clk1x.	RW
[3:0]	Resptm_req	The response timing when detect the dfi_lp_req is high. Unit: dfi_clk1x.	RW

3.6.2.15 DDR DQ Width

																	PHY_APB_BASE+0x07c															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Reserved																														DQWidth	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Name	Description	RW
[1:0]	DQWidth	The DQ width select signal. 2'h3: 16bit 2'h1: 8bit	RW

3.6.2.16 DDR PLL Feedbackdiv

																	PHY_APB_BASE+0x080															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								PLL_FbdivL							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0

Bits	Name	Description	RW
[7:0]	PLL_Fbdiv L	PLL Feedbackdivide [7:0] (fbdiv[7:0]). It combines with register 0x024[1] to generate the fbdiv[8:0]. Note: fbdiv >=8.	RW

3.6.2.17 DDR PLL PowerDown Enable

																	PHY_APB_BASE+0x084															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														PLL_PowDown	PLL_FbdivH
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0

Bits	Name	Description	RW
[31:2]	Reserved		
[1]	PLL_PowDown	PLL power down enable 1: power down 0: power up.	RW
[0]	PLL_FbdivH	PLL Feedbackdivide [8].	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

3.6.2.18 DDR PLL Post Divide

																																PHY_APB_BASE+0x088
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								PLL_postdiv			PLL_prediv				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bits	Name	Description	RW
[31:8]	Reserved		
[7:5]	Pll_postdiv	PLL Post-divide(postdiv[2:0])	RW
[4:0]	Pll_prediv	PLL Pre-divide(prediv[4:0])	RW

3.6.2.19 DDR PHY PLL_LOCK

	PLL_LOCK																															PHY_APB_BASE+0x108
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												PLL_LOCK	Reserved		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
[3]	PLL_LOCK	PLL lock signal. High is valid.	R

3.6.2.20 DDR PHY RX CALIBRATION

When the DDR PHY sends the read command to the SDRAM, the SDRAM will return the read data, so we can use the return DQS to latch the read data. We design the RX calibration function to generate the DQS gating signal, the gating signal like a window to let the clean RX DQS pass. Then this signal can be used to latch the read data correctly.

We do the RX calibration after the SDRAM complete the initial and before we send the valid write/read command.

After we complete the initial of the SDRAM, the RX calibration will send the read command to the SDRAM, and then the SDRAM will return read data and read DQS. Because we never write data to the SDRAM, so the current read data is X state. At the time that the DQS is back, the DQS gating signal generate at the same time, then the DDR PHY will adjust the phase

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

between the gating signal and read DQS until the gating signal can cover all the DQS signal.

We have three accuracy grades to adjust the gating signal. The grades show in the Table 3-4 .

Table 3-4 The rx calibreation delay grade

Grades	Type	Description	Unit
1	dll_dly	This grade has 8 steps. It is the minimum of the three grades. 8*DLL step = 2x clock cycle.	per DLL step
2	oph_dly	Thes grade has 4 steps. 2*2x clock = 1x clock cycle.	2x clock cycle
3	cyc_dly	This grade has 8 steps. It is the maximum of the three grades.	1x clock cycle

The phase = dll_dly + oph_dly + cyc_dly.
We have two modes to complete the RX calibration. The first mode is auto-mode, the other mode is
bypass-mode.

When we choose the auto-mode, we only need to enable the calibration function and wait it complete; when we choose the bypass-mode, we need to use the register to adjust the phase between the DQS and gating.

3.6.2.21 DDR PHY DQS_GATING_CALIBRATION

	DQS_GATING_CALIBRATION																PHY_APB_BASE+0x008															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														DSCSE	DSACE
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
[1]	DSCSE	DQS gating calibration bypass mode, active high 1:register bypass mode 0:no bypass mode	RW
[0]	DSACE	DQS gating calibration control, active high 1: Enable. 0: Disable.	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

3.6.2.22 DDR PHY CALIB_DONE

	CALIB_DONE																															PHY_APB_BASE+0x10c
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														HDQCFA	LDQCFA
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
[1]	HDQCFA	The complete flag of the calibration of the channel A high 8bits DQ. High is valid.	R
[0]	LDQCFA	The complete flag of the calibration of the channel A low 8bits DQ. High is valid.	R

Note :

1.Channel A low 8bit signals: A_DQS0, A_DQSB0, A_DQ7~A_DQ0, A_DM0
Channel A high 8bit signals: A_DQS1, A_DQSB1, A_DQ15~A_DQ8, A_DM1

2.Dllsel: one step is 1/8 dfi_clk2x time
Ophsel: one step is 1 dfi_clk2x time
Cyclese: one step is 1 dfi_clk1x time

After we complete the auto-mode RX calibration, we also can read the register to get the result of the dll_dly, oph_dly and cyc_dly corresponding to each channel.

3.6.2.23 DDR PHY Calibration Result of Left Channel A

																																PHY_APB_BASE+0x1d0
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																									Dll_dly_LA			Oph_dly_LA	Cyc_dly_LA		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
[6:4]	Dll_dly_LA	The dll_dly result of left channel A.	R
[3]	Oph_dly_LA	The oph_dly result of left channel A.	R
[2:0]	Cyc_dly_LA	The cyc_dly result of left channel A.	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

3.6.2.24 DDR PHY Calibration Result of Right Channel A

																																PHY_APB_BASE+0x1d4
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																									Dll_dly_RA			Oph_dly_RA	Cyc_cly_RA		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
[6:4]	Dll_dly_RA	The dll_dly result of right channel A.	R
[3]	Oph_dly_RA	The oph_dly result of right channel A.	R
[2:0]	Cyc_dly_RA	The cyc_dly result of right channel A.	R

3.6.2.25 DDR PHY BYPASS-MODE RX CALIBRATION of Left Channel A

When we choose the bypass-mode RX calibration, we can use the register to control the delay of the dll_dly, cyc_dly and oph_dly.

																																PHY_APB_BASE+0x158
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																									Ctl_Dll_dly_LA			Ctl_Oph_dly_LA	Ctl_Cyc_cly_LA		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Name	Description	RW
[6:4]	Ctl_Dll_dly_LA	Use to control the cyc_dly of the left channels A. cyc_dly = CFG * 1x clock cycle.	R
[3]	Ctl_Oph_dly_LA	Use to control the oph_dly of the left channels A. oph_dly = CFG * 2x clock cycle	R
[2:0]	Ctl_Cyc_dly_LA	Use to control the dll_dly of the left channels A. dll_dly = CFG * DLL step	R

3.6.2.26 DDR PHY BYPASS-MODE RX Calibration of Right Channel A

																																PHY_APB_BASE+0x198
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Reserved	Ctl_Dll_dly_RA	Ctl_Oph_dly_RA	Ctl_Cyc_dly_RA
RST	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 1 1	1	0 0 0

Bits	Name	Description	RW
[6:4]	Ctl_Dll_dly_RA	Use to control the cyc_dly of the right channels A. cyc_dly = CFG * 1x clock cycle.	R
[3]	Ctl_Oph_dly_RA	Use to control the oph_dly of the right channels A. oph_dly = CFG * 2x clock cycle	R
[2:0]	Ctl_Cyc_dly_RA	Use to control the dll_dly of the right channels A. dll_dly = CFG * DLL step	R

3.6.2.27 DDR PHY INIT_COMP

	INIT_COMP	PHY_APB_BASE+0x110
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	Reserved	INIT_COMP
RST	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Name	Description	RW
[0]	INIT_COMP	PHY initialize complete flag: 0: Not complete 1: Complete	R

3.6.2.28 DDR PHY Bist

		PHY_APB_BASE+0x118
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	Reserved	Bist_Reg Bist_CMD Bist_DM Bist_DQ Bist_Comp
RST	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Name	Description	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

[4]	Bist_Reg	The bist result of the bist_reg mode. High means error	R
[3]	Bist_CMD	The bist result of the command. High means error.	R
[2]	Bist_DM	The bist result of the dm. High means error.	R
[1]	Bist_DQ	The bist result of the dq channel. High means error	R
[0]	Bist_Comp	The bist complete flag. High valid	R

3.6.2.29 DDR TX DLL control signal of DQ[7:0] and DM[0]

																																	PHY_APB_BASE+0x150
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	Reserved																													TXDLL_Delay0			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	

Bits	Name	Description	RW
[2:0]	TXDLL_Delay0	TX DLL delay of DQ[7:0] and DM[0] 0: no delay 1: 22.5° delay 2: 45° delay 3: 67.5° delay 4: 90° delay 5: 112.5° delay 6: 135° delay 7: 157.5° delay	RW

3.6.2.30 DDR TX DLL control signal of DQS[0] and DQSB[0]

																																	PHY_APB_BASE+0x154
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	Reserved																													TXDLL_Delay1			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bits	Name	Description	RW
[2:0]	TXDLL_Delay1	TX DLL delay of DQS[0] and DQSB[0] 0: no delay 1: 22.5° delay 2: 45° delay 3: 67.5° delay 4: 90° delay 5: 112.5° delay 6: 135° delay 7: 157.5° delay	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

3.6.2.31 DDR TX DLL control signal of DQ[15:8] and DM[1]

																																PHY_APB_BASE+0x190
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																													TXDLL_Delay2		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Name	Description	RW
[2:0]	TXDLL_Delay2	TX DLL delay of DQ[15:8] and DM[1] 0: no delay 1: 22.5° delay 2: 45° delay 3: 67.5° delay 4: 90° delay 5: 112.5° delay 6: 135° delay 7: 157.5° delay	RW

3.6.2.32 DDR TX DLL control signal of DQS[1] and DQSB[1]

																																PHY_APB_BASE+0x194
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																													TXDLL_Delay3		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
[2:0]	TXDLL_Delay3	TX DLL delay of DQS[1] and DQSB[1] 0: no delay 1: 22.5° delay 2: 45° delay 3: 67.5° delay 4: 90° delay 5: 112.5° delay 6: 135° delay 7: 157.5° delay	RW

3.6.2.33 DDR RX DLL control signal of DQS[0] and DQSB[0]

																																PHY_APB_BASE+0x160
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Reserved																														RXDLL_Delay0	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Name	Description	RW
[1:0]	RXDLL_Delay 0	The control signal for RX DLL DQS [0] and DQSB [0]. It is corresponding totheDQ[7:0]. 0: no delay 1: 22.5° delay 2: 45° delay 3: 67.5° delay	RW

Note: Please keep the register 0x08[5:4] has the same value with 0x08[1:0].

3.6.2.34 DDR RX DLL control signal of DQS[1] and DQSB[1]

																		PHY_APB_BASE+0x1a0														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														RXDLL_Delay1	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Name	Description	RW
[1:0]	RXDLL_Delay 1	The control signal for RX DLL DQS [1] and DQSB [1]. It is corresponding totheDQ[15:8]. 0: no delay 1: 22.5° delay 2: 45° delay 3: 67.5° delay	RW

Note: Please keep the register 0x18[5:4] has the same value with 0x18[1:0].

3.6.2.35 DDR PD ODT resistance for DQ[7:0]

																		PHY_APB_BASE+0x0300														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											PDODT_RES0				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bits	Name	Description	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

[4:0]	PDODT_RES0	pull-down ODT resistance for DQ[7:0]. The resistance relation with the configuration show in Table 3-5.	RW

Table 3-5 LPDDR2 DQ/DQS ODT Rsistance

Control bit	5'b11111	5'b11110	5'b11101	5'b11100	units
pull-up	35.68	37.66	39.05	41.43	ohm
pull-down	35.68	37.66	39.05	41.43	ohm
Control bit	5'b11011	5'b11010	5'b11001	5'b11000	units
pull-up	43.11	46.03	48.12	51.79	ohm
pull-down	43.11	46.03	48.12	51.79	ohm
Control bit	5'b10111	5'b10110	5'b10101	5'b10100	units
pull-up	54.44	59.19	62.68	69.05	ohm
pull-down	54.44	59.19	62.68	69.05	ohm
Control bit	5'b10011	5'b10010	5'b10001	5'b10000	units
pull-up	73.85	82.86	89.87	103.6	ohm
pull-down	73.85	82.86	89.87	103.6	ohm
Control bit	5'b01111	5'b01110	5'b01101	5'b01100	units
pull-up	54.44	59.19	62.68	69.05	ohm
pull-down	54.44	59.19	62.68	69.05	ohm
Control bit	5'b01011	5'b01010	5'b01001	5'b01000	units
pull-up	73.85	82.86	89.87	103.6	ohm
pull-down	73.85	82.86	89.87	103.6	ohm
Control bit	5'b00111	5'b00110	5'b00101	5'b00100	units
pull-up	114.8	138.1	158.7	207.2	ohm
pull-down	114.8	138.1	158.7	207.2	ohm
Control bit	5'b00011	5'b00010	5'b00001	5'b00000	units
pull-up	257.5	414.3	679	+∞	ohm
pull-down	257.5	414.3	679	+∞	ohm

3.6.2.36 DDR PU ODT resistance for DQ[7:0]

																																PHY_APB_BASE+0x0304
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											PUODT_RES0				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bits	Name	Description	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

[4:0]	PUODT_RES0	pull-down ODT resistance for DQ[7:0]. The resistance relation with the configuration show in Table 3-5.	RW

3.6.2.37 DDR PD Driving resistance for DQ[7:0]

																		PHY_APB_BASE+0x0308														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											PDDRI_RES0				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0

Bits	Name	Description	RW
[4:0]	PDDRI_RES0	pull-down driving resistance for DQ[7:0]. The resistance relation with the configuration show in Table 3-6.	RW

Table 3-6 LPDDR2 DQ/DQS driving strength

Control bit	5'b11111	5'b11110	5'b11101	5'b11100	units
pull-up	20.91	21.86	22.9	24.05	ohm
pull-down	20.91	21.86	22.9	24.05	ohm
Control bit	5'b11011	5'b11010	5'b11001	5'b11000	units
pull-up	25.31	26.72	28.29	30.06	ohm
pull-down	25.31	26.72	28.29	30.06	ohm
Control bit	5'b10111	5'b10110	5'b10101	5'b10100	units
pull-up	32.06	34.35	37	40.08	ohm
pull-down	32.06	34.35	37	40.08	ohm
Control bit	5'b10011	5'b10010	5'b10001	5'b10000	units
pull-up	43.72	48.1	53.44	60.12	ohm
pull-down	43.72	48.1	53.44	60.12	ohm
Control bit	5'b01111	5'b01110	5'b01101	5'b01100	units
pull-up	32.06	34.35	37	40.08	ohm
pull-down	32.06	34.35	37	40.08	ohm
Control bit	5'b01011	5'b01010	5'b01001	5'b01000	units
pull-up	43.72	48.1	53.44	60.12	ohm
pull-down	43.72	48.1	53.44	60.12	ohm
Control bit	5'b00111	5'b00110	5'b00101	5'b00100	units
pull-up	68.71	80.16	96.19	120.2	ohm
pull-down	68.71	80.16	96.19	120.2	ohm
Control bit	5'b00011	5'b00010	5'b00001	5'b00000	units

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

pull-up	160.3	240.5	481	+∞	ohm
pull-down	160.3	240.5	481	+∞	ohm

3.6.2.38 DDR PU Driving resistance for DQ[7:0]

																																PHY_APB_BASE+0x030c
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											PUDRI_RES0				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0

Bits	Name	Description	RW
[4:0]	PUDRI_RES0	pull-up driving resistance for DQ[7:0]. The resistance relation with the configuration show in Table 3-6.	RW

3.6.2.39 DDR PD ODT resistance for DQ[15:8]

																																PHY_APB_BASE+0x0340
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											PDODT_RES1				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bits	Name	Description	RW
[4:0]	PDODT_RES1	pull-down ODT resistance for DQ[15:8]. The resistance relation with the configuration show in Table 3-3.	RW

3.6.2.40 DDR PU ODT resistance for DQ[15:8]

																																PHY_APB_BASE+0x0344
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											PUODT_RES1				

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bits	Name	Description	RW
[4:0]	PUODT_RES1	pull-down ODT resistance for DQ[15:8]. The resistance relation with the configuration show in Table 3-5.	RW

3.6.2.41 DDR PD Driving resisteance for DQ[15:8]

																													PHY_APB_BASE+0x0348			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											PDDRI_RES1				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0

Bits	Name	Description	RW
[4:0]	PDDRI_RES1	pull-down driving resistance for DQ[15:8]. The resistance relation with the configuration show in Table 3-6.	RW

3.6.2.42 DDR PU Driving resistance for DQ[15:8]

																													PHY_APB_BASE+0x034c			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											PUDRI_RES1				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0

Bits	Name	Description	RW
[4:0]	PUDRI_RES1	pull-up driving resistance for DQ[15:8]. The resistance relation with the configuration show in Table 3-6.	RW

3.6.2.43 DDR PHY LOW SPEED MODE

As a unique powerful compatibility feature, Innosilicon DDR PHY supports low speed DDR SDRAM to high speed DDR3-800 by using two operating mode: normal delay line mode up to 800Mbps or more, low power mode where we support any speed up to533Mbps. If all TX DLLs are bypassed, the PHY will enter low power state.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

The DDR PHY entries low power mode when setting DLLs into Bypass mode. Table 3-7 illustrates related register settings.

Table 3-7 Low Power DLL Setting

ADDR	BIT	DEFAULT	LOW POWER SETTING	DESCRIPTION
0x16c	[3]	0x0	0x1	left channel A TX DQ DLL in bypass mode
0x1ac	[3]	0x0	0x1	right channel A TX DQ DLL in bypass mode
0x050	[4]	0x0	0x1	CMD/CK DLL in bypass mode
0x054	[4]	0x1	0x0	CK DLL phase select
0x150	[4]	0x0	0x1	A_DQ0~A_DQ7 TX DLL phase select
0x154	[3]	0x0	0x0	A_DQS0/A_DQSB0 TX DLL phase select
0x190	[4]	0x0	0x1	A_DQ8~A_DQ15 TX DLL phase select
0x194	[3]	0x0	0x0	A_DQS1/A_DQSB1 TX DLL phase select

Note:

(1) Those bits lead to command DLL in bypass mode.

(2)(3) Both DQS0 DLL and DQ7~DQ0 DLLs are bypassed, but only DQS0 DLL should be in inversion mode because DQS0 step delay is 0x00 and DQ7~DQ0 DLL's step delay is 0x4.

																																	PHY_APB_BASE+0x016c
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												LCA_TX_BP	Reserved		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
[3]	LCA_TX_BP	left channel A TX DQ DLL in bypass mode, active high	RW

																																	PHY_APB_BASE+0x01ac
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Reserved	RCA_TX_BP	Reserved
RST	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0 0 0

Bits	Name	Description	RW
[3]	RCA_TX_BP	right channel A TX DQ DLL in bypass mode, active high	RW

3.6.2.44 DDR PHY PER BIT DE-SKEW TURING

Per-bit de-skew is designed for compensating PCB trace mismatch. DDR PHY support skew individually adjustable for all PHY signals. There are 16 steps for each bit de-skew adjusting, and the adjust resolution under different corners is shown in Table 3-8.

Table 3-8 per-bit de-skew tuning resolution

	ff	tt	ss
de-skew resolution	18ps	28ps	38ps

Pre-bit de-skew is realized with inverter chain delay, per-bit de-skew control signals select how much inverters are connected to data path, the minimum resolution is determined by the 4 inverters minimum delay.

DELAY = REG_CFG * DE-SKEW

TX path de-skew and RX path de-skew employ same delay line, and they have same de-skew tuning resolution. Minimum RX de-skew tuning resolution can be about 30ps in tt corner process, and we can re-design tuning resolution according to system and customer requirement.

The following sections will introduce the registers which used to control per-bit de-skew of the PHY interface. We divided the signal into two parts: CMD and DATA.

3.6.2.44.1 CMD SIGNAL

The related register which used to control per-bit de-skew of command signal shows in following sections.

DDR PHY A0 DE-SKEW

		PHY_APB_BASE+0x0400
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Reserved																														A0_Deskew		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	A0_Deskew	A0 de-skew	RW

DDR PHY A1 DE-SKEW

																																	PHY_APB_BASE+0x0404
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														A1_Deskew		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	A1_Deskew	A1 de-skew	RW

DDR PHY A2 DE-SKEW

																																	PHY_APB_BASE+0x0408
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														A2_Deskew		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	A2_Deskew	A2 de-skew	RW

DDR PHY A3 DE-SKEW

																																	PHY_APB_BASE+0x040c
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Reserved																														A3_Deskew		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	A3_Deskew	A3 de-skew	RW

DDR PHY A4 DE-SKEW

																	PHY_APB_BASE+0x0410																
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														A4_Deskew		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	A4_Deskew	A4 de-skew	RW

DDR PHY A5 DE-SKEW

																	PHY_APB_BASE+0x0414																
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														A5_Deskew		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	A5_Deskew	A5 de-skew	RW

DDR PHY A6 DE-SKEW

																	PHY_APB_BASE+0x0418																
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Reserved																														A6_Deskew		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	A6_Deskew	A6 de-skew	RW

DDR PHY A7 DE-SKEW

																	PHY_APB_BASE+0x041c																
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														A7_Deskew		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	A7_Deskew	A7 de-skew	RW

DDR PHY A8 DE-SKEW

																	PHY_APB_BASE+0x0420																
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														A8_Deskew		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	A8_Deskew	A8 de-skew	RW

DDR PHY A9 DE-SKEW

																	PHY_APB_BASE+0x0424																
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Reserved																														A9_Deskew		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	A9_Deskew	A9 de-skew	RW

DDR PHY CK0 DE-SKEW

																	PHY_APB_BASE+0x0428																
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														CK0_Deskew		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	CK0_Deskew	CK0 de-skew	RW

DDR PHY CKB0 DE-SKEW

																	PHY_APB_BASE+0x042c																
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														CKB0_Deskew		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	CKB0_Deskew	CKB0 de-skew	RW

DDR PHY ODT0 DE-SKEW

																	PHY_APB_BASE+0x0430																
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Reserved																													ODT0_Deskew			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	ODT0_Deskew	ODT0 de-skew	RW

DDR PHY CKE DE-SKEW

																														PHY_APB_BASE+0x0434			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																													CKE_Deskew			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	CKE_Deskew	CKE de-skew	RW

DDR PHY CSB0 DE-SKEW

																														PHY_APB_BASE+0x043c			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																													CSB0_Deskew			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	CSB0_Deskew	CSB0 de-skew	RW

3.6.2.44.2 DATA SIGNAL

The registers of per-bit de-skew for data show in following sections.

DDR PHY DM0 DE-SKEW for RX path

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

																	PHY_APB_BASE+0x0480															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											DM0_Deskew_RX				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	DM0_Deskew_RX	DM0 de-skew for RX path	RW

DDR PHY DM0 DE-SKEW for TX path

																	PHY_APB_BASE+0x0484															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											DM0_Deskew_TX				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	DM0_Deskew_TX	DM0 de-skew for TX path	RW

DDR PHY DQ0 DE-SKEW for RX path

																	PHY_APB_BASE+0x0488															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											DQ0_Deskew_RX				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	DQ0_Deskew_RX	DQ0 de-skew for RX path	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

DDR PHY DQ0 DE-SKEW for TX path

																		PHY_APB_BASE+0x048c															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											DQ0_Deskew_TX				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	DQ0_Deskew_TX	DQ0 de-skew for TX path	RW

DDR PHY DQ1 DE-SKEW for RX path

																		PHY_APB_BASE+0x0490															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											DQ1_Deskew_RX				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	DQ1_Deskew_RX	DQ1 de-skew for RX path	RW

DDR PHY DQ1 DE-SKEW for TX path

																		PHY_APB_BASE+0x0494															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											DQ1_Deskew_TX				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	DQ1_Deskew_TX	DQ1 de-skew for TX path	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

DDR PHY DQ2 DE-SKEW for RX path

																	PHY_APB_BASE+0x0498															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											DQ2_Deskew_RX				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	DQ2_Deskew_RX	DQ2 de-skew for RX path	RW

DDR PHY DQ2 DE-SKEW for TX path

																	PHY_APB_BASE+0x049c															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											DQ2_Deskew_TX				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	DQ2_Deskew_TX	DQ2 de-skew for TX path	RW

DDR PHY DQ3 DE-SKEW for RX path

																	PHY_APB_BASE+0x04a0															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											DQ3_Deskew_RX				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	DQ3_Deskew_RX	DQ3 de-skew for RX path	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

DDR PHY DQ3 DE-SKEW for TX path

																		PHY_APB_BASE+0x04a4															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											DQ3_Deskew_TX				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	DQ3_Deskew_TX	DQ3 de-skew for TX path	RW

DDR PHY DQ4 DE-SKEW for RX path

																		PHY_APB_BASE+0x04a8															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											DQ4_Deskew_RX				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	DQ4_Deskew_RX	DQ4 de-skew for RX path	RW

DDR PHY DQ4 DE-SKEW for TX path

																		PHY_APB_BASE+0x04ac															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											DQ4_Deskew_TX				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	DQ4_Deskew_TX	DQ4 de-skew for TX path	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

DDR PHY DQ5 DE-SKEW for RX path

																	PHY_APB_BASE+0x04b0															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											DQ5_Deskew_RX				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	DQ5_Deskew_RX	DQ5 de-skew for RX path	RW

DDR PHY DQ5 DE-SKEW for TX path

																	PHY_APB_BASE+0x04b4															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											DQ5_Deskew_TX				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	DQ5_Deskew_TX	DQ5 de-skew for TX path	RW

DDR PHY DQ6 DE-SKEW for RX path

																	PHY_APB_BASE+0x04b8															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											DQ0_Deskew_RX				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	DQ6_Deskew_RX	DQ6 de-skew for RX path	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

DDR PHY DQ6 DE-SKEW for TX path

																		PHY_APB_BASE+0x04bc															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											DQ6_Deskew_TX				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	DQ6_Deskew_TX	DQ6 de-skew for TX path	RW

DDR PHY DQ7 DE-SKEW for RX path

																		PHY_APB_BASE+0x04c0															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											DQ7_Deskew_RX				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	DQ7_Deskew_RX	DQ7 de-skew for RX path	RW

DDR PHY DQ7 DE-SKEW for TX path

																		PHY_APB_BASE+0x04c4															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											DQ7_Deskew_TX				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	DQ7_Deskew_TX	DQ7 de-skew for TX path	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

DDR PHY DQS0 DE-SKEW for RX path

																																	PHY_APB_BASE+0x04c8
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												DQS0_Deskew_RX			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	DQS0_Deskew_RX	DQS0 de-skew for RX path	RW

DDR PHY DQS0 DE-SKEW for TX path

																																	PHY_APB_BASE+0x04cc
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												DQS0_Deskew_TX			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	DQS0_Deskew_TX	DQS0 de-skew for TX path	RW

DDR PHY DQSB0 DE-SKEW for TX path

																																	PHY_APB_BASE+0x04d0
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												DQSB0_Deskew_TX			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	DQSB0_Deskew_TX	DQSB0 de-skew for TX path	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

DDR PHY DM1 DE-SKEW for RX path

																		PHY_APB_BASE+0x04d4														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											DM1_Deskew_RX				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	DM1_Deskew_RX	DM1 de-skew for RX path	RW

DDR PHY DM1 DE-SKEW for TX path

																		PHY_APB_BASE+0x04d8														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											DM1_Deskew_TX				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	DM1_Deskew_TX	DM1 de-skew for TX path	RW

DDR PHY DQ8 DE-SKEW for RX path

																		PHY_APB_BASE+0x04dc														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											DQ8_Deskew_RX				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	DQ8_Deskew_RX	DQ8 de-skew for RX path	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

DDR PHY DQ8 DE-SKEW for TX path

																																PHY_APB_BASE+0x04e0
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											DQ8_Deskew_TX				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	DQ8_Deskew_TX	DQ8 de-skew for TX path	RW

DDR PHY DQ9 DE-SKEW for RX path

																																PHY_APB_BASE+0x04e4
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											DQ9_Deskew_RX				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	DQ9_Deskew_RX	DQ9 de-skew for RX path	RW

DDR PHY DQ9 DE-SKEW for TX path

																																PHY_APB_BASE+0x04e8
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											DQ9_Deskew_TX				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	DQ9_Deskew_TX	DQ9 de-skew for TX path	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

DDR PHY DQ10 DE-SKEW for RX path

																		PHY_APB_BASE+0x04ec														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											DQ10_Deskew_RX				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	DQ10_Deskew_RX	DQ10 de-skew for RX path	RW

DDR PHY DQ10 DE-SKEW for TX path

																		PHY_APB_BASE+0x04f0														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											DQ10_Deskew_TX				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	DQ10_Deskew_TX	DQ10 de-skew for TX path	RW

DDR PHY DQ11 DE-SKEW for RX path

																		PHY_APB_BASE+0x04f4														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											DQ11_Deskew_RX				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	DQ11_Deskew_RX	DQ11 de-skew for RX path	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

DDR PHY DQ11 DE-SKEW for TX path

																	PHY_APB_BASE+0x04f8															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											DQ11_Deskew_TX				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	DQ11_Deskew_TX	DQ11 de-skew for TX path	RW

DDR PHY DQ12 DE-SKEW for RX path

																	PHY_APB_BASE+0x04fc															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											DQ12_Deskew_RX				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	DQ12_Deskew_RX	DQ12 de-skew for RX path	RW

DDR PHY DQ12 DE-SKEW for TX path

																	PHY_APB_BASE+0x0500															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											DQ12_Deskew_TX				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	DQ12_Deskew_TX	DQ12 de-skew for TX path	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

DDR PHY DQ13 DE-SKEW for RX path

																		PHY_APB_BASE+0x0504														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											DQ13_Deskew_RX				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	DQ13_Deskew_RX	DQ13 de-skew for RX path	RW

DDR PHY DQ13 DE-SKEW for TX path

																		PHY_APB_BASE+0x0508														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											DQ13_Deskew_TX				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	DQ13_Deskew_TX	DQ13 de-skew for TX path	RW

DDR PHY DQ14 DE-SKEW for RX path

																		PHY_APB_BASE+0x050c														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											DQ14_Deskew_RX				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	DQ14_Deskew_RX	DQ14 de-skew for RX path	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

DDR PHY DQ14 DE-SKEW for TX path

																		PHY_APB_BASE+0x0510														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											DQ14_Deskew_TX				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	DQ14_Deskew_TX	DQ14 de-skew for TX path	RW

DDR PHY DQ15 DE-SKEW for RX path

																		PHY_APB_BASE+0x0514														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											DQ15_Deskew_RX				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	DQ15_Deskew_RX	DQ15 de-skew for RX path	RW

DDR PHY DQ15 DE-SKEW for TX path

																		PHY_APB_BASE+0x0518														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											DQ15_Deskew_TX				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	DQ15_Deskew_TX	DQ15 de-skew for TX path	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

DDR PHY DQS1 DE-SKEW for RX path

																		PHY_APB_BASE+0x051c														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											DQS1_Deskew_RX				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	DQS1_Deskew_RX	DQS1 de-skew for RX path	RW

DDR PHY DQS1 DE-SKEW for TX path

																		PHY_APB_BASE+0x0520														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											DQS1_Deskew_TX				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	DQS1_Deskew_TX	DQS1 de-skew for TX path	RW

DDR PHY DQSB1 DE-SKEW for TX path

																		PHY_APB_BASE+0x0524														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											DQSB1_Deskew_TX				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	RW
[4:0]	DQSB1_Deskew_TX	DQSB1 de-skew for TX path	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

DDR PHY DQSB0 DE-SKEW for RX path

																																	PHY_APB_BASE+0x0528
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	Reserved																												DQSB0_Deskew_RX				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	

Bits	Name	Description	RW
[4:0]	DQSB0_Deskew_RX	DQSB0 de-skew for RX path	RW

DDR PHY DQSB1 DE-SKEW for RX path

																																	PHY_APB_BASE+0x052c
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	Reserved																												DQSB1_Deskew_RX				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	

Bits	Name	Description	RW
[4:0]	DQSB1_Deskew_RX	DQSB1 de-skew for RX path	RW

3.7 Functional Description

3.7.1 DDRC and DDR2 Memory Initialization Sequence

The following content is just an example for initialization, the sequence is already implementation in our BSP。

Example

One 512Mb x16 DDR2 device connected on CS0;

No memory device connected on CS1;

DCK = 133 MHz, CL = 3.

1. After system reset, wait system clock stable before initialize DDRC.
2. Configure the Clock-Control module for DDRC clocks.
3. DDR Memory device need at least 200us initialization time after power-on before it can accept any command.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

//----------
// INIT DDRC
//----------
4 Configure DCFG = 0x.
5 Configure DTIMING1~6 = 0x.
6 Configure DMMAP0 = 0x.
7 Configure DMMAP1 = 0x0000FF00.
//----------
// INIT DDR PHY
//----------
8 Configure DDR PHY and finish PHY training process.(relate to DDRPHY spec)
//----------
// DDRC performance control configure (optional)
//----------
9 Configure RCMDCTRL0 = 0x08080808 (optional)
10 Configure RCMDCTRL1 = 0x00000808 (optional)
11 Configure WDATTHD0 = 0x08080808 (optional)
12 Configure WDATTHD1 = 0x00000808 (optional)
//----------
// INIT DDR memory device
//----------
13 Set CKE Pin HIGH : Configure DCTRL = 0x00000002.
//----------
// Enable Refresh Counter
//----------
14 Enable Refresh Counter : Configure DREFCNT = 0x.
15 AUTO-REFRESH : Configure DCTRL = 0x.
//----------
// END INITIALIZING SEQUENCE
//----------

//----------
// INIT DDR PHY
//----------
1 Provide stable pclk and ddr_clk1x to the DDR PHY.
2 Low the preset_n and system_rstn to reset the register module and digital core.
3 High the preset_n signal to release the register module.
4 Configure the related register. Such as choose the memory type, CL, AL, PLL and DQ width.
5 High the system_rstn to release the digital core.
6 Enabel the pll and wait for the PLL lock.
Note：When we enable the PLL, the reference clock dfi_clk1x need to keep stable.
7 Low dfi_init_start to begin the initialization of the DDR PHY and wait dfi_init_complete

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

change from low to high.

8 Begin the initialization of the SDRAM and wait for the complete.

9 Begin the RX Calibration.

10 Read the RX Calibration result from the register 0x74/0x75/0xa4/0xa5.

If the 0x74[6:4]<=0x1 | 0x75[6:4]<=0x1 | 0xa4[6:4]<=0x1 | 0xa5[6:4]<=0x1, Set reg 0x01[6] to 0x1 and reg 0xa[3:1] to 0x2.

11 Begin to do the normal write or read operation.

3.8 Change Clock Frequency

To reduce power consumption, the system clock frequency may be changed frequently according to the application. There are 3 ways to change the clock frequency.

3.8.1 Manually SELF-REFRESH Mode

DDR can stay in SELF-REFRESH & DEEP-POWER-DOWN mode for a long period of time. System clock frequency can be changed during this time. Even more, the clocks to DDRC module can also be stopped to save power-consumption.

Reference Sequence:

1. Manually issue SELF-REFRESH command to DDR.
2. Change relative register in CPM.
3. Change system clock frequency.
4. Drive DDR exit SELF-REFRESH mode.

3.8.2 CPM driven SELF-REFRESH Mode

CPM will auto drive DDRC to self-refresh mode, when use ddr2, ddr3.

To change clock frequency, please refer CPM spec.

3.8.3 DLL bypass mode

The clock frequency on which DLL in ddr phy works much faster than 200MHz, As the result, when ddr clock is failed to meet this condition (for example, work in 12MHz) , the DLL must be bypassed in order to supply clock to ddr controller.

Step1, Configure DLL into reset mode to guarantee a driving clock.

(0xB00000D0) CPM_DRCG[1] <= 1;

Step2, Configure DLL into bypass mode.

(0xB3011014) DDR_ACDLLCR[0] <= 1;

Then, (0xB00000D0) CPM_DRCG[1] <= 0;

3.9 Data Endian

Fix to little Endian.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

3.10 Retention Flow

3.10.1 Enter Retention mode

Description:

S0: Prepare Retention Program

Before perform retention enter flow, the program for this flow should be mapped to on chip RAM (such as TCSM in PDMA), during retention mode, any content in DRAM is not accessible. The PC of CPU should jump out of DDR range to on chip RAM

S1: Disable All Bus

Disable all device which addressing DDR, only DDRC APB/ DDRP APB port can be active.

S2: Put DRAM in self-refresh mode

there are two ways to drive DRAM into self-refresh

1. manually configuration (please refer DCTRL.SR)
2. Auto-self-refresh (AUTOSR_EN) (*recommended*)

polling the DDRC_STATUS.ddr_sr_mode to make sure the DRAM is in self-refresh mode

S3: Read ZQ value and reserve it future use.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

(refer: X1000_ddrphy_spec: ZQnSR0.ZCTRL)

S4: Enable signal isolation

PHYRET_CFG.cfg_iso_en <= 1
PHYRET_CFG.clk_iso_en <= 1

S5: Assert DDR PHY Retention

PHYRET_CFG.ret_en <= 1
PHYRET_CFG.ret_en_n <= 0

S6: Remove Power

please refer Power off sequence

S7: Further Operation for power saving

- Configure CPM, gating DDR clock
- Others

Now, the DDR is safely in retention mode, any transfer to DDR from CH0~CH6 is forbidden. Please refer 'Exit Retention mode' for wake DDR

Please note that, the retention mode is only used in system sleep mode, which still powering on GPIO. Because GPIO is must for exiting retention operation.

3.10.2 Exit Retention mode

Soft ware control flow

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Description:

S1: Ready for Power-On

S2: Restore DDR Power

Please refer Sequence of DDR Power up.

S3: Guarantee clock

- Turn off CPM: ddr gating if it is gated in '*Enter Retention Mode: S7*'.
- Disable PHY clock isolation

  PHYRET_CFG.clk_iso_en <= 0
- Disable Auto-clk-stp mode

  CLKSTP.clkstp_en <= 0

S4: Soft reset DDR PHY

1) PHYRST_CFT.*_reset <= 1
2) Delay for some cycles
3) PHYRST_CFT.*_reset <= 0

S5: Reconfigure PUBL registers

Please refer '*X1000_ddrphy_spec*'

S6: Set ZQ bypass enable

DDR_PHY_PIR.ZCLBYP <= 1

S7: Polling register

DDR_PHY_PGSR.IDONE = 1

S8: Override ZQ

DDR_PHY_ZQnCR0.ZDEN <= 1 + DDR_PHY_ZQnCR0.ZDATA <= previous value (in '*Enter Retention Mode: S3*').

S9: De-assert ret_en

PHYRET_CFG.ret_en <= 0 + PHYRET_CFG.ret_en_n <= 1

S10: Override ZQ disable

DDR_PHY_ZQnCR0.ZDEN <= 0

S11: Trigger ZQ Calibration

DDR_PHY_PIR.ZQCAL <= 1 + DDR_PHY_PIR.INIT <= 1

S12: Polling register

DDR_PHY_PGSR.IDONE = 1

S13: Grant DFI bus to DDRC

DDR_PHY_PIR.CTLDINIT <= 1 + DDR_PHY_PIR.INIT <= 1

S14: Polling register

DDR_PHY_PGSR.IDONE = 1

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

S15: Disable signal isolation

PHYRET_CFG.cfg_iso_en <= 0

S16: Exit self-refresh

- If system works in Auto-self-refresh mode, disable this function
  AUTOSR_EN <= 0
- if works in manually self-refresh mode. Configure register to exit
  DCTL.SR <= 0

S17: Polling register to ensure ddrc exit self-refresh mode

DDRC_STATUS.ddr_sr_mode = 0

S18: Perform Data training

Please note that it will override some data in DDR, so make sure the training address is not in use.

DDR_PHY_PIR.DQTRN <= 1 + DDR_PHY_PIR.DRAMINIT <= 1

S19: Polling register

DDR_PHY_PGSR.DTDONE = 1 + DDR_PHY_PGSR.DTERR = 0

S20: Reconfigure DDRC feature:

eg:

- AUTODR_EN <= 1
- CLKSTP_CFG.clkstp_en <= 1
- ..... others .....

S21: Finish

DDR is thoroughly get out of Retention mode. Change PC to DDR for normal operation.

3.11 DDR Connection Diagrams

The following diagrams give examples on the connection to external DDR2 devices.
Note not all the possible connections are listed.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

3.11.1 Connection to one 512Mb x16 DDR2 devic

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

3.11.2 Connection to two 512Mb x16 DDR2 devices

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

4 External Memory Controller

4.1 Overview

The External Memory Controller (EMC) divides the off-chip memory space and outputs control signals complying with specifications of various types of static memory and bus interfaces. It enables the connection of static memory such as NOR flash memory, etc. to this processor.

4.2 Features

- Direct interface to 8-bit or 16-bit (no byte control) bus width external memory interface devices or external static memory to each bank.
- Support 2 external chip selection CS2~1#. Each bank can be configured separately
- Support address and data multiplexed NOR flash device
- Offers flexibility to support define assertion and deassertion times of control signals
- Wait insertion by WAIT pin
- Automatic wait cycle insertion to prevent data bus collisions in case of consecutive memory accesses to different banks, or a read access followed by a write access to the same bank
- Support for the following memory types:
  - External asynchoronous memory (non burst device)
  - External asynchoronous burst ROM
  - External asynchoronous address data multiplexed memory

4.3 Pin Description

Following table list the EMC pins.

Table 4-1 EMC Pin Description

Symbo	I/O	Description
AD15-AD0	I/O	Data[15:0] in no-muxed mode. Address[15:0], Data[15:0] in muxed mode.
A15-A0	O	Address output.
CS2-1#	O	Chip select signal that indicates the static bank being accessed.
RE#(OE#)	O	For Static memory read enable signal.
WE#	O	Static memory write enable signal.
AVD#	O	Address Valid input. Indicates to device that the valid address is present on the address.
Wait#	I	External wait state request signal for memory-like devices.

4.4 Physical Address Space Map

Both virtual spaces and physical spaces are 32-bit wide in this architecture. Virtual addresses are translated by MMU into physical address which is further divided into several partitions for static memory, SDRAM, and internal I/O.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Figure 4-1 Physical Address Space Map

Table 4-2 Physical Address Space Map

Start Address	End Address	Connectable Memory	Capacity

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

0x00000000	0x0FFFFFFF	SDRAM Memory	256MB
0x10000000	0x13FFFFFF	Internal I/O Devices	64MB
0x14000000	0x14FFFFFF	Reserved	16MB
0x15000000	0x15FFFFFF	Reserved	16MB
0x16000000	0x1600003F	Reserved	64B
0x16000040	0x16FFFFFF	Reserved	
0x17000000	0x1700003F	Reserved	64B
0x17000040	0x17FFFFFF	Reserved	
0x18000000	0x1800003F	Reserved	64B
0x18000040	0x18FFFFFF	Reserved	
0x19000000	0x1900003F	Reserved	64B
0x19000040	0x19FFFFFF	Reserved	
0x1A000000	0x1A00FFFF	Static Memory, CS2#	64KB
0x1A000040	0x1AFFFFFF	Reserved	
0x1B000000	0x1B00FFFF	Static Memory, CS1#	64KB
0x1B000040	0x1BFFFFFF	Reserved	
0x1C000000	0x1FBFFFFF	Reserved	
0x1FC00000	0x1FC02FFF	On-chip Boot ROM (16kB)	16KB
0x1FC04000	0x1FFFFFFF	Reserved	
0x20000000	0xDFFFFFFF	SDRAM Memory	3072MB
0xE0000000	0xFFFFFFFF	Reserved	512MB

The base address and size of each memory banks are configurable. Software can re-configure these memory banks according to the actual connected memories. Following table lists the default configuration after reset.

Table 4-3 Default Configuration of EMC Chip Select Signals

Chip-Select Signal	Connected Memory	Capacity	Memory Width *1	Start Address	End Address
CS1#	Static memory bank 1	64 KB	8, 16	0x1B000000	0x1B00FFFF
CS2#	Static memory bank 2	64 KB	8, 16	0x1A000000	0x1A00FFFF

NOTES:

1 Data width of static memory banks can be configured to 8, 16 bits by software.

2 The 16KB address space from H'1FC00000 to H'1FC03FFF in bank 0 is mapped to on-chip boot ROM. The other memory spaces in bank 0 are not used.

4.5 Example of Connection

Following figures shows examples of connection to 16- and 8-bit data width normal memory.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Figure 4-2 Example of 16-Bit Data Width SRAM Connection

Figure 4-3 Example of 8-Bit Data Width SRAM Connection

Following figures shows examples of connection to address and data multiplexed memory interface device.

Figure 4-4 Example of address and data multiplexed memory Connection

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

4.6 Timing Setting

4.6.1 Normal Memory

When SMT field in SMCRn (n = 1 to 2) is 0, normal memory (non-burst ROM, Flash, normal SRAM or memory-like device) is connected to bank n. When bank n (n = 1 to 2) is accessed, CSn# is asserted as soon as address is output. In addition, the RD# signal, which can be used as OE#, and write control signals WE# is asserted.

Figure 4-5 Normal Memory Read Timing

The Tras field in SMC0R_i[15:12] defines the address setup time.It is the minimum amount of time the address signal should be held steady before the RD# assert.

The T1 is one access inherent cycle.

The Toe fileld in SMC0R_i[23:20] defines the data capture time relative to RD# assertion time.

The Tch field in SMC0R_i[27:24] defines the CS# signal deassertion time relative to data capture time.

The Trdrv field in SMC1R_i[23:20] defines the number of idle cycles (0~63 cycles) inserted between bus cycles when switching from one bank to another bank or between a read access to a write access in the same bank.

In this example, Tras = 3, Toe = 2, Tch = 2, Trdrv=1, ignore wait_pin.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Figure 4-6 Normal Memory Write Timing

The Twas field in SMC0R_i[11:8] defines the address setup time.It is the minimum amount of time the address signal should be held steady before the WE# assert.

The Tds fileld in SMC0R_i[19:16] defines the data setup time.

The T2 is one write inherent cycle.

The Tch is the minimum amount of the data single hold time from the earliest rising edge of WE#.

In this example, Twas = 3, Tds = 2, Tch = 1, Twrrv = 1, ignore wait_pin

.

Figure 4-7 Normal Memory Read/Write Timing

In this example, Tras = 0, Twas = 0, Toe = , Tds = 0, Tch = 0, Trdrv = 0, Twrrv = 0, ignore wait_pin.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Figure 4-8 Normal Memory Read Timing With Wait_Pin-1

Figure 4-9 Normal Memory Read Timing With Wait_Pin-2

During accesses with wait_pin monitoring enable (the WAIT_ENABLE in SMC0R_i[xxx]), the wait pin must be deasserted before data capture.

The Taw field in SMC0R_i[23:20] defines the WAIT# capture time relative to RD# assertion time.

In this example, Tras = 3, Taw = 2, Tch = 2.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Figure 4-10 Normal Memory Write Timing With Wait_Pin

The Tbp field in SMC1R_i[19:16] defines the WAIT# capture time relative to WE# assertion time.

In this example, Twas = 3, Tbp = 2, Tch = 1.

4.6.2 Burst ROM

Setting SMT to 1 in SMCRn allows burst ROM to be connected to bank n (n = 1 to 2). The burst ROM interface provides high-speed access to ROM that has a nibble access function. Basically, access is performed in the same way as for normal memory, but when the first cycle ends, only the address is changed before the next access is executed. When 8-bit burst ROM is connected, the number of consecutive accesses can be set as 4, 8, 16, or 32 with bits BL1~0. When 16-bit ROM is connected, 4, 8, or 16 can be set in the same way.

Following figures show the timing of burst ROM.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Figure 4-11 Burst ROM Read Timing With Wait

The Taw sets the delay time from read strobe to the first data..
The Tbp sets the delay time from consecutive address to data.
In this example, Taw = 2, Tbp = 2

Figure 4-12 Burst ROM Write Timing With Wait

Burst ROM writes have the same timing as normal memory except Trw instead of Tbp is used to set the delay time of WE#.
In this example, Taw = 2

4.6.3 Address/Data Multiplexed Memory

When SMT field in SMCRn (n = 1 to 2) is 2, address and data multiplexed memory is connected to bank n. The address and the data bus can be multiplexed on the same external bus.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Figure 4-13 Address/Data Multiplexed Memory Read Timing

In this example, Tavds = 1, Tavdp = 2, Tavdh = 1, Tras = 6, Toe = 2, Tch = 2, Trdrv = 1.

Figure 4-14 Address/Data Multiplexed Memory Write Timing

In this example, Tavds = 1, Tavdp = 2, Tavdh = 1, Twas = 6, Tds = 2, Tch = 1, Twrrv = 1.

4.7 Register Description

Following chapter will descript the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. Register read/write attribute

   R - Read only

   W - Write only

   RW - read and write

   RCW - read and write, but clear to 0 by read

   RSW - read and write, but set to 1 by read

   RWC - read and write, clear to 0 by soft write 1, set to 1 by hardware write 1, write 0 has no effect

   RWS - read and write, set to 1 by soft write 1, hardware clear to 0, soft write 0 has no effect

   RC - read only, and clear to 0 by read

   RS - read only, and set to 1 by read

   SPEC - special access method, relate to its description
3. Reset Value

   1 - Reset to 1

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

0 - reset to 0

? - Value unknown after reset

4.7.1 Register Memory Map

Table 4-4 Registers Memory Map Base Address

Name	Base	Description
EMC	0x13410000	EMC base address.

The External Memory Controller is controlled by a set of registers that the application configures before every operation. The following table lists all the registers.

Table 4-5 Static Memory Interface Registers Map

Name	RW	Reset Value	Address Offset	Access Size
SMC0R1	RW	0x0FFF_7700	0x014	32
SMC0R2	RW	0x0FFF_7700	0x018	32
SACR1	RW	0x0000_1BFE	0x034	32
SACR2	RW	0x0000_1AFE	0x038	32
SMC1R1	RW	0x8F00_0121	0x054	32
SMC1R2	RW	0x8F00_0121	0x058	32

4.7.2 Register and Fields Description

4.7.2.1 Static Memory Control0 Register (SMC0R_i)

SMC0R_i are 32-bit read/write registers that contain control bits for static memory. On reset, SMCR_i is initialized to 0x0FFF7700.

	SMC0R1 SMC0R2																															Base+0x14 Base+0x18
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				TCH				TAW_OE				TBP_DS				TRAS				TWAS				BW		BL		Reserved		SMT	
RST	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	0	1	1	1	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
30:28	Reserved	Writing has no effect, read as zero.	
27:24	TCH	**Chip Enable Hold Time.** These bits specify the number of wait cycles to be inserted from from deassertion of RD#/WE# to deassertion of CS#. **TCH2~0 Wait cycle**	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		0000 0 cycle 0001 1 cycle 0010 2 cycles 0011 3 cycles 0100 4 cycles 0101 5 cycles 0110 6 cycles 0111 7 cycles (Initial Value) 1000 8 cycles 1001 9 cycles 1010 10 cycles 1011 11 cycles 1100 12 cycles 1101 13 cycles 1110 14 cycles 1111 15 cycles	
23:20	TAW_OE	**Access Wait Time / Valid Data output after CS# low.** For normal memory, these bits specify the number of wait cycles to be inserted in read strobe time. For burst ROM, these bits specify the number of wait cycles to be inserted in first data read strobe time. **TAW3~0 Wait cycle** 0000 0 cycle 0001 1 cycle 0010 2 cycles 0011 3 cycles 0100 4 cycles 0101 5 cycles 0110 6 cycles 0111 7 cycles 1000 8 cycles 1001 9 cycles 1010 10 cycles 1011 12 cycles 1100 15 cycles 1101 20 cycles 1110 25 cycles 1111 31 cycles (Initial Value)	RW
19:16	TBP_DS	**Write Wait Time / Burst Pitch Time / Data Setup.** For normal memory, these bits specify the number of wait cycles to be inserted in write strobe time. For burst ROM, these bits specify the number of wait cycles to be inserted in subsequent access.	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		TBP3~0 **Wait cycle** 0000 0 cycle 0001 1 cycle 0010 2 cycles 0011 3 cycles 0100 4 cycles 0101 5 cycles 0110 6 cycles 0111 7 cycles 1000 8 cycles 1001 9 cycles 1010 10 cycles 1011 12 cycles 1100 15 cycles 1101 20 cycles 1110 25 cycles 1111 31 cycles (Initial Value)	
15:12	TRAS	**Read Address Setup Time.** These bits specify the number of wait cycles (0~15 cycles) to be inserted from address to assertion of RD#. **TRAS2~0** **Wait cycle** 0000 0 cycle 0001 1 cycle 0010 2 cycles 0011 3 cycles 0100 4 cycles 0101 5 cycles 0110 6 cycles 0111 7 cycles (Initial Value) 1000 8 cycles 1001 9 cycles 1010 10 cycles 1011 12 cycles 1100 15 cycles 1101 20 cycles 1110 25 cycles 1111 31 cycles	RW
11:8	TWAS	**Write Address Setup Time.** These bits specify the number of wait cycles (0~15 cycles) to be inserted from address to assertion of WE#. **TWAS2~0** **Wait cycle** 0000 0 cycle 0001 1 cycle	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		0010 2 cycles 0011 3 cycles 0100 4 cycles 0101 5 cycles 0110 6 cycles 0111 7 cycles (Initial Value) 1000 8 cycles 1001 9 cycles 1010 10 cycles 1011 12 cycles 1100 15 cycles 1101 20 cycles 1110 25 cycles 1111 31 cycles	
7:6	BW	**Bus Width.** These bits specify the bus width. this filed is writeable and are initialized to 0 by a reset. **BW1~0 Bus Width** 00 8 bits (Initial Value) 01 16 bits 10 Reserved 11 Reserved	RW
5:4	BL	**Burst Length (BL1, BL0).** When Burst ROM is connected; these bits specify the number of burst in an access. These bits are only valid when SMT is set to 1. **BL1~0 Burst Length** 00 4 consecutive accesses. Can be used with 8- or 16-bit bus width (Initial Value) 01 8 consecutive accesses. Can be used with 8- or 16-bit bus width 10 16 consecutive accesses. Can only be used with 8- or 16-bit bus width 11 32 consecutive accesses. Can only be used with 8-bit bus width	RW
3:2	Reserved	Writing has no effect, read as zero. **NOTES:** Don't write Bit3 to 1.	R
1:0	SMT	**Static Memory Type (SMT).** This bit specifies the type of static memory. **SMT Description** 0 Normal Memory (Initial Value) 1 Burst ROM 2 Address Data Multiplexed Memory(ADM)	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

4.7.2.2 Static Memory Control1 Register (SMC1R_i)

	SMC1R1 SMC1R2																															Base+0x54 Base+0x58
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WP_EN	DOUBLE	STRV						TRDRV				TWRRV				Reserved				TAVDH				TAVDP				TAVDS			
RST	1	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	1

Bits	Name	Description	RW
31	WP_ EN	**Wait Pin Enable** 1: Access time can be dynamically controlled using WAIT#.(Initial Value) 0: Ingore WAIT#.	RW
30	DOUBLE	All waiting times are doubled.	RW
29:24	STRV	**Static Memory Recovery Time.** Its value is the number of idle cycles (0~63 cycles) inserted between bus cycles when switching from one bank to another bank or between a read access to a write access in the same bank. Its initial value is 0xF (15 cycles).	RW
23:20	TRDRV	**Read Recovery Time from CS# rising edge** **TRDRV3~0 Wait cycle** 0000 0 cycle(Initial Value) 0001 1 cycle 0010 2 cycles 0011 3 cycles 0100 4 cycles 0101 5 cycles 0110 6 cycles 0111 7 cycles 1000 8 cycles 1001 9 cycles 1010 10 cycles 1011 11 cycles 1100 12 cycles 1101 13 cycles 1110 14 cycles 1111 15 cycles	RW
19:16	TWRRV	**Write Recovery from CS# rising edge** **TWRRV3~0 Wait cycle**	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		0000 0 cycle (Initial Value) 0001 1 cycle 0010 2 cycles 0011 3 cycles 0100 4 cycles 0101 5 cycles 0110 6 cycles 0111 7 cycles 1000 8 cycles 1001 9 cycles 1010 10 cycles 1011 11 cycles 1100 12 cycles 1101 13 cycles 1110 14 cycles 1111 15 cycles	
15:12	Reserved	Writing has no effect, read as zero.	R
11:8	TAVDH	**Address Hold from AVD# rising edge** **TAVDH3~0 Wait cycle** 0000 0 cycle 0001 1 cycle (Initial Value) 0010 2 cycles 0011 3 cycles 0100 4 cycles 0101 5 cycles 0110 6 cycles 0111 7 cycles 1000 8 cycles 1001 9 cycles 1010 10 cycles 1011 11 cycles 1100 12 cycles 1101 13 cycles 1110 14 cycles 1111 15 cycles	RW
7:4	TAVDP	**ADV# Low pulse** **TAVDP3~0 Wait cycle** 0000 0 cycle 0001 1 cycle 0010 2 cycles (Initial Value) 0011 3 cycles 0100 4 cycles 0101 5 cycles	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		0110 6 cycles 0111 7 cycles 1000 8 cycles 1001 9 cycles 1010 10 cycles 1011 11 cycles 1100 12 cycles 1101 13 cycles 1110 14 cycles 1111 15 cycles	
3:0	TAVDS	**Address setup to ADV# rising edge** **TAVDH3~0 Wait cycle** 0000 0 cycle 0001 1 cycle (Initial Value) 0010 2 cycles 0011 3 cycles 0100 4 cycles 0101 5 cycles 0110 6 cycles 0111 7 cycles 1000 8 cycles 1001 9 cycles 1010 10 cycles 1011 11 cycles 1100 12 cycles 1101 13 cycles 1110 14 cycles 1111 15 cycles	RW

4.7.2.3 Static Bank Address Configuration Register (SACR_i)

SACR_i defines the physical address for static memory bank i, respectively. Each register contains a base address and a mask. When the following equation is met:

(*physical_address* [31:24] & **MASK**$_i$) == **BASE**$_i$

The bank i is active. The *physical_address* is address output on internal system bus. Static bank regions must be programmed so that each bank occupies a unique area of the physical address space. Programming overlapping bank regions will result in unpredictable error. These registers are initialized by a reset.

	SACR1																														**Base+0x034**
	SACR2																														**Base+0x038**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Reserved																BASE								MASK							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	1	1	1	1	1	1	1	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:8	BASE	**Address Base:** Defines the base address of Static Bank 1. SACR1: The initial value is 0x1B. SACR2: The initial value is 0x1A.	RW
7:0	MASK	**Address Mask:** Defines the mask of Static Bank 1. SACR1: The initial value is 0xFE. SACR2: The initial value is 0xFE.	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

5 SPI Flash Controller(SFC)

5.1 Overview

This module is an SPI master to control the SPI flash device. Data can be transferred in CPU controlling mode or DMA mode.

5.2 Features

- SPI protocol support: Standard, Dual, Quad SPI
- transmit-only or receive-only operation
- MSB always be first in intra transfer of one byte. Least Significant Byte first for inter transfer of data bytes, and Most Significant Byte first for inter transfer of command or address bytes.
- 64 entries x 32 bits wide data FIFO
- two device select
- Configurable sampling point for reception
- Configurable timing parameters: tSLCH, tCHSH and tSHSL
- Configurable flash address wide are supported
- 7 transfer formats: Standard SPI, Dual-Output/Dual-Input SPI, Quad-Output/Quad-Input SPI, Dual-I/O SPI, Quad-I/O SPI, Full Dual-I/O SPI, Full Quad-I/O SPI.
- two data transfer mode: slave mode and DMA mode
- Configurable 6 phases for software flow
- CDT(command descriptor table)
- DMA descriptor chain for data transfer
- SDR trans mode.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

5.3 Block Diagram

Figure 5-1 SFC Block Diagram

The AHB Interface include one slave interface and one master interface. The slave interface is used for register configuration and slave transfer mode, and the master interface is designed for DMA operation.
The FIFO block is bidirectional, used as data buffer for transmission(from AHB to device) and reception(from device to AHB).
The Flow Control module controls the operation of the 6 phases
The Transfer mode Control act as the handler of slave mode and DMA mode.

5.4 Functional Description

5.4.1 Bus function

5.4.2 AHB Slave Interface

- parameter configuration
- transfer data in slave mode.
- data and address must align with 4 bytes.
- only SINGLE transfer is supported.

5.4.3 AHB Master Interface

- transfer data in DMA mode
- SINGLE, INCR, INCR4, INCR8, INCR16, INCR32 are supported.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

5.4.4 Configurable Timing parameter

5.4.4.1 Propagation delay

The propagation delay do not effect the data transmission, and it would not effect the data reception when the serial clock has a low frequency, as shown in the Figure 5-2.

But when the serial clock run at a fast frequency, the propagation delay will cause the incoming data could not arrival at the right clock edge, then the sampling point should be adjustable as shown in the Figure 5-3.

Figure 5-2 Sample point(no delay)

Figure 5-3 Sample point(delay)

5.4.4.2 AC timing

tSETUP(tSLCH), tHOLD(tCHSH), tSH(tSHSL) are configurable.

Figure 5-4 AC timing

5.5 Pin Description

Table 5-1 I/O Pin Description

Name	I/O	Description
clk	Output	Serial clock

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

ce0	Output	Device0 select
ce1	Output	Device1 select
dt	Inout	Serial data IO0
dr	Inout	Serial data IO1
wp	Inout	Serial data IO2(WP#)
hd	Inout	Serial data IO3(HOLD#)

5.6 Date Format Description

5.6.1 Transfer format

Figure 5-5 Data Format(Standard SPI)

Figure 5-6 Data Format(Dual SPI)

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Figure 5-7 Data Format(Quad SPI)

5.6.2 Endian Description

Address is MSB first, as shown in the Figure 5-5;

Flash's status can be configured as LSB or MSB by using SFC_DEV_CFG.STA_ENDIAN

Data's endian and unit can be configured by TRAN_CFG1.DATA_ENDIAN and TRAN_CFG1.WORD_UNIT

5.7 Registers Description

5.7.1 Instructions

Following chapter will descript the functions of all software accessible registers.

Conventions:

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

1. Register Address = Base + Address offset
2. The registers can be read and written by AHB2 bus
3. Register read/write attribute
   - ✧ R - Read only
   - ✧ W - Write only
   - ✧ RW - read and write
   - ✧ RCW - read and write, but clear to 0 by read
   - ✧ RSW - read and write, but set to 1 by read
   - ✧ RWC - read and write, clear to 0 by write 1, write 0 has no effect
   - ✧ RWS - read and write, set to 1 by write 1, write 0 has no effect
   - ✧ RC - read only, and clear to 0 by read
   - ✧ RS - read only, and set to 1 by read
   - ✧ SPEC - special access method, relate to its description
4. Reset Value
   - – 1 - reset to 1
   - – 0 - reset to 0
   - – ? - value unknown after reset

5.7.2 Map

The SFC's registers map base address is 0x13440000

The SFC is controlled by a set of registers that the application configures before every operation. The following table lists all the registers.

Table 5-2 SFC Registers Map

Name	Reset Value	Address Offset	Description	RW	Mask
GLB0	0x0000_008F	Base+0x0000	Global configure register0	RW	0xFFFF_FFFF
DEV_CONF	0x0000_0027	Base+0x0004	Device parameter	RW	0x0007_FFFF
DEV_STA_EXP	0x0000_0000	Base+0x0008	Expected status of device	RW	0xFFFF_FFFF
DEV0_STA_RT	0x0000_0000	Base+0x000c	Real-time status of device	R	0xFFFF_FFFF
DEV_STA_MSK	0x0000_0000	Base+0x0010	Mask flag of device's status	RW	0xFFFF_FFFF
TRAN_CFG0_0	0x0000_0000	Base+0x0014	Transfer parameter0 of phase0	RW	0xFFFF_FFFF
TRAN_CFG0_1	0x0000_0000	Base+0x0018	Transfer parameter0 of phase1	RW	0xFFFF_FFFF
TRAN_CFG0_2	0x0000_0000	Base+0x001c	Transfer parameter0 of phase2	RW	0xFFFF_FFFF
TRAN_CFG0_3	0x0000_0000	Base+0x0020	Transfer parameter0 of phase3	RW	0xFFFF_FFFF
TRAN_CFG0_4	0x0000_0000	Base+0x0024	Transfer parameter0 of phase4	RW	0xFFFF_FFFF
TRAN_CFG0_5	0x0000_0000	Base+0x0028	Transfer parameter0 of phase5	RW	0xFFFF_FFFF
TRAN_LEN	0x0000_0000	Base+0x002c	Transfer length	RW	0xFFFF_FFFF
DEV_ADR0	0x0000_0000	Base+0x0030	Device address of phase0	RW	0xFFFF_FFFF
DEV_ADR1	0x0000_0000	Base+0x0034	Device address of phase1	RW	0xFFFF_FFFF
DEV_ADR2	0x0000_0000	Base+0x0038	Device address of phase2	RW	0xFFFF_FFFF

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

DEV_ADR3	0x0000_0000	Base+0x003c	Device address of phase3	RW	0xFFFF_FFFF
DEV_ADR4	0x0000_0000	Base+0x0040	Device address of phase4	RW	0xFFFF_FFFF
DEV_ADR5	0x0000_0000	Base+0x0044	Device address of phase5	RW	0xFFFF_FFFF
DEV_PLUS0	0x0000_0000	Base+0x0048	Plus address of phase0	RW	0xFFFF_FFFF
DEV_PLUS1	0x0000_0000	Base+0x004c	Plus address of phase1	RW	0xFFFF_FFFF
DEV_PLUS2	0x0000_0000	Base+0x0050	Plus address of phase2	RW	0xFFFF_FFFF
DEV_PLUS3	0x0000_0000	Base+0x0054	Plus address of phase3	RW	0xFFFF_FFFF
DEV_PLUS4	0x0000_0000	Base+0x0058	Plus address of phase4	RW	0xFFFF_FFFF
DEV_PLUS5	0x0000_0000	Base+0x005c	Plus address of phase5	RW	0xFFFF_FFFF
MEM_ADDR	0x0000_0000	Base+0x0060	DDR address	RW	0xFFFF_FFFF
TRIG	0x0000_0000	Base+0x0064	SFC trigger	RW	0x0000_0007
SR	0x0000_0000	Base+0x0068	Status register	R	0x007F_007F
SCR	0x0000_0000	Base+0x006c	Status clear register	RW	0x0000_003F
INTC	0x0000_001F	Base+0x0070	Interrupt control	RW	0x0000_001F
FSM	0x0001_0111	Base+0x0074	Sub-modules' FSM state	R	0x000F_FF77
CGE	0x0000_003F	Base+0x0078	CLK gate function	RW	0x0000_003F
CMD_IDX	0x0000_0000	Base+0x007c	Cmd index in CDT	RW	0xC000_003F
COL_ADDR	0x0000_0000	Base+0x0080	Column addr	RW	0xFFFF_FFFF
ROW_ADDR	0x0000_0000	Base+0x0084	Row addr	RW	0xFFFF_FFFF
STA_ADDR0	0x0000_0000	Base+0x0088	Status addr0	RW	0xFFFF_FFFF
STA_ADDR1	0x0000_0000	Base+0x008c	Status addr1	RW	0xFFFF_FFFF
DES_ADDR	0x0000_0000	Base+0x0090	DMA descriptor address	RW	0xFFFF_FFFF
GLB1	0x0000_008F	Base+0x0094	Global configure register1	RW	0x0000_0003
DEV1_STA_RT	0x0000_0000	Base+0x0098	Real-time status of device	R	0xFFFF_FFFF
TRAN_CFG1_0	0x0000_0000	Base+0x009c	Transfer parameter1 of phase0	RW	0xFFFF_FFFF
TRAN_CFG1_1	0x0000_0000	Base+0x00a0	Transfer parameter1 of phase1	RW	0xFFFF_FFFF
TRAN_CFG1_2	0x0000_0000	Base+0x00a4	Transfer parameter1 of phase2	RW	0xFFFF_FFFF
TRAN_CFG1_3	0x0000_0000	Base+0x00a8	Transfer parameter1 of phase3	RW	0xFFFF_FFFF
TRAN_CFG1_4	0x0000_0000	Base+0x00ac	Transfer parameter1 of phase4	RW	0xFFFF_FFFF
TRAN_CFG1_5	0x0000_0000	Base+0x00b0	Transfer parameter1 of phase5	RW	0xFFFF_FFFF
CDT	0x0000_0000	Base+0x0800 ~ Base+0x0c00	CDT's register interface	RW	0xFFFF_FFFF
DR	0x0000_0000	Base+0x1000	Data register (slave mode)	RW	0xFFFF_FFFF

5.7.3 Registers

5.7.3.1 SFC Global Configure Register0

	SFC_GLB0																															Base + 0x0000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	POLL_TIME																DES_EN	CDT_EN	TRAN_DIR	THRESHOLD						OP_MODE	PHASE_NUM			WP_EN	BURST_LEN	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	1	1

Bits	Name	Description	RW
31:16	POLL_TIME	Interval time counter between twice polling op..	RW
15	DES_EN	Descriptor of DMA enable. 1: DMA will use the memory in descriptor, no longer use the SFC_MEM_ADDR 0: disable.	RW
14	CDT_EN	Use CDT. 0: disable(default) 1: enable	RW
13	TRAN_DIR	The direction of transfer. 0: read data from SPI flash (default) 1: write data to SPI flash	RW
12:7	THRESHOLD	FIFO threshold. (unit: word) Natural number, 1-63(default is 1). Note: cannot be 0	RW
6	OP_MODE	0: slave mode (default) 1: DMA mode	RW
5:3	PHASE_NUM	The number of phase in one flow. 001: 1 phase (default) 010: 2 phases 011: 3 phases 100: 4 phases 101: 5 phases 110: 6 phases Note: cannot be 0	RW
2	WP_EN	Enable the hardware write protection 0: disable WP 1: Enable WP (default)	RW
1:0	BURST_MD	The max beats of burst. 00: reserved 01: INCR8 10: INCR16 11: INCR32 (default)	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

5.7.3.2 SFC Global Configure Register1

	SFC_GLB1																															Base + 0x0094
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CHIP1_SEL	Reserved																													CHIP_SEL	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	CHIP1_SEL	1: Force select chip1	RW
30:3	Reserved	Write has no effect. Read as indeterminate value.	R
2	Reserved	Keep default	RW
1:0	CHIP_SEL	Chip select 00: chip 0(default) 01: keep default 10: keep default 11: reserved	RW

5.7.3.3 SFC Device Configure Register

	SFC_DEV_CONF																															Base + 0x0004
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	STA_ENDIAN	Reserved										SMP_DELAY					CMD_TYPE	STA_TYPE		THOLD		TSETUP		TSH				CPHA	CPOL	CE_DL	HOLD_DL	WP_DL
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1

Bits	Name	Description	RW
31	STA_ENDIAN	0: LSB (default) 1: MSB	RW
30:21	Reserved	Write has no effect. Read as zero.	R
20:16	SMP_DELAY	Sample delay, it's depends on the device output delay, PCB delay and the IO ports delay, etc. 00000: no delay (default) 00001: 45 00010: 90 00011: 135 00100: 180 00101: 225	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		00110: 270 00111: 315 01000: one SFC_CLK cycle 01001: one SFC_CLK cycle + 45 01010: one SFC_CLK cycle + 90 ..... 01111: one SFC_CLK cycle + 315 10000: two SFC_CLK cycle ..... 11111: three SFC_CLK cycle + 315	
15	CMD_TYPE	0: 1 byte (default) 1: 2 bytes	RW
14:13	STA_TYPE	used for polling 00: 1 byte status (default) 01: 2 bytes status 10: 3 bytes status 11: 4 bytes status	RW
12:11	THOLD	Hold time of SFC_CE, the time between the last edge of SFC_CLK and SFC_CE de-assertion. 00: half SFC_CLK cycle (default) 01: one SFC_CLK cycle 10: one and a half SFC_CLK cycle 11: two SFC_CLK cycle	RW
10:9	TSETUP	Setup time of SFC_CE, the time between SFC_CE assertion and the first edge of SFC_CLK. 00: half SFC_CLK cycle (default) 01: one SFC_CLK cycle 10: one and a half SFC_CLK cycle 11: two SFC_CLK cycle	RW
8:5	TSH	The min interval time between twice assertion of SFC_CE. 0000: one SFC_CLK cycle 0001: one SFC_CLK cycle(default) 0010: one and a half SFC_CLK cycle 0011: two SFC_CLK cycle 0100: two and a half SFC_CLK cycle 0101: three SFC_CLK cycle 0110: three and a half SFC_CLK cycle 0111: four SFC_CLK cycle 1000: four and a half SFC_CLK cycle 1001: five SFC_CLK cycle 1010: five and a half SFC_CLK cycle 1011: six SFC_CLK cycle	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		1100: six and a half SFC_CLK cycle 1101: seven SFC_CLK cycle 1110: seven and a half SFC_CLK cycle 1111: eight SFC_CLK cycle	
4	CPHA	This bit is used to select the SPI clock format. 0 = Sampling of data occurs at odd edges (1,3,5,...) of the SFC_CLK clock (default) 1 = Sampling of data occurs at even edges (2,4,6,...) of the SFC_CLK clock	RW
3	CPOL	This bit selects the active level of SFC_CLK. 0 = Active-high clocks selected. In idle state SFC_CLK is low. (default) 1 = Active-low clocks selected. In idle state SFC_CLK is high.	RW
2	CE_DL	The default invalid level of SFC_CE pin 0: low 1: high (default)	RW
1	HOLD_DL	The default invalid level of SFC_HOLD pin 0: low 1: high (default)	RW
0	WP_DL	The default invalid level of SFC_WP pin 0: low 1: high (default)	RW

5.7.3.4 SFC Device Status Expected Register

	SFC_DEV_STA_EXP																															Base + 0x0008
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DEV_STA_EXP																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DEV_STA_EXP	The expected value of flash status for comparing.	RW

5.7.3.5 SFC Device0 Status Real-time Register

	SFC_DEV0_STA_RT																															Base + 0x000c
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DEV0_STA_RT																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:0	DEV0_STA_RT	The real-time status of SPI Flash0	R

5.7.3.6 SFC Device1 Status Real-time Register

	SFC_DEV1_STA_RT																															Base + 0x0098
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DEV1_STA_RT																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DEV1_STA_RT	The real-time status of SPI Flash1	R

5.7.3.7 SFC Device Status Mask Register

	SFC_DEV_STA_MSK																															Base + 0x0010
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DEV_STA_MSK																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DEV_STA_MSK	Flash status mask for comparing. 1: this bit will be checked. 0: this bit will not be checked.	RW

5.7.3.8 SFC Transfer Configure Register0 (phase0-phase5)

	SFC_TRAN_CCFG0(0-5)																															Base + 0x0014 - Base + 0x0028
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CLK_MODE			ADDR_WIDTH			POLL_EN	CMD_EN	PHASE_FORMAT	DMY_BITS						DATA_EN	TRAN_CMD															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:29	CLK_MODE	SDR.	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		000: SDR (default) Note: Keep default	
28:26	ADDR_WIDTH	The width of address used in the phase. 000: no address transfer (default) 001: 1 bytes 010: 2 bytes 011: 3 bytes 100: 4 bytes 101: 5 bytes >=110: 6 bytes	RW
25	POLL_EN	The polling function means that SFC checking the flash device's status. 0: no polling transfer (default) 1: has polling transfer. Note: it's priority is higher than tran_dir and data_en	RW
24	CMD_EN	0: no command transfer(default) 1: has command transfer	RW
23	PHASE_FORMAT	Phase format, see chapter 5.8.1 0: format0(default) 1: format1	RW
22:17	DMY_BITS	The needed dummy cycle num (unit: SFC_CLK cycle) 000000: no dummy transfer (default) 000001: 1 dummy cycles 000010: 2 dummy cycles 000011: 3 dummy cycles ..... 100000: 32 dummy cycles	RW
16	DATE_EN	0: no data transfer(default) 1: has data transfer	RW
15:0	CMD	The transfer command	RW

5.7.3.9 SFC Transfer Configure Register1 (phase0-phase5)

	SFC_TRAN_CFG1																																Base + 0x009c - Base + 0x00b0
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved													DATA_ENDIAN	WORD_UNIT		Reserved								TRAN_MD				Reserved			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

31:19	Reserved	Write has no effect. Read as zero.	RW
18	DATA_ ENDIAN	0: LSB first 1: MSB first	RW
17:16	WORD_UNIT	00: 1 Byte 01: 2 Bytes 10: 4 Bytes	RW
15:8	Reserved	Write has no effect. Read as zero.	RW
7:4	TRAN_MD	Transfer mode: 0000：Standard SPI（default） 0001：Dual Input/Dual Output SPI 0010：Dual I/O SPI 0011：Full Dual I/O SPI 0100：reserved 0101：Quad Input/Quad Output SPI 0110：Quad I/O SPI 0111：Full Quad I/O SPI Others: reserved	RW
3:0	Reserved	Write has no effect. Read as zero.	RW

5.7.3.10 SFC Transfer Length Register

	SFC_TRAN_LEN																															Base + 0x002c
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TRAN_LEN																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	TRAN_LEN	Number of bytes to be transferred. 32'h0: no data transfer Note: 1. This register should be 0 when there isn't data phase in the flow, else the DMA or RMC will start when not use DMA descriptor.	RW

5.7.3.11 SFC Device Address Register (phase0 - phase5)

	SFC_DEV_ADDR0-5																															Base + 0x0030 - Base + 0x0044
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DEV_ADDR																															

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DEV_ADDR	The low bytes of flash address for transfer when do not use CDT.	RW

5.7.3.12 SFC Device Address Plus Register (phase0 - phase5)

	SFC_DEV_ADDR_PLUS0-5																															**Base + 0x0048 - Base + 0x005c**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DEV_ADDR_PLUS																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DEV_ADDR_PLUS	The high bytes of flash address for transfer when do not use CDT.	RW

5.7.3.13 SFC Memory Address Register

	SFC_MEM_ADDR																															**Base + 0x0060**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MEM_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	MEM_ADDR	Memory address for DMA when do not use DMA descriptor.	RW

5.7.3.14 SFC Trigger Register

	SFC_TRIG																															**Base + 0x0064**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																													FLUSH	STOP	START
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:3	Reserved	Write has no effect. Read as zero.	R
2	FLUSH	Write 1 to reset the FIFO. Write 0 has no effect.	W

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

1	STOP	Write 1 to stop all transmission. Write 0 has no effect.	W
0	START	Write 1 to start the transmission Write 0 has no effect.	W

5.7.3.15 SFC Status Register

	SFC_SR																															Base + 0x0068
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved									FIFO_NUM							Reserved								WORKING	BUSY		END	TRAN_REQ	RECE_REQ	OVER	UNDER
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:17	Reserved	Write has no effect. Read as zero.	R
22:16	FIFO_NUM	The quantity of data in FIFO (unit: word)	R
15:8	Reserved	Write has no effect. Read as zero.	R
7	WORKING	0: the SFC is IDLE 1: the SFC is working	R
6:5	BUSY	00: the SPI is IDLE 01: the SPI is in transaction 10: the SPI is in reception 11: the SPI is waiting for transfer	R
4	END	Indicate whether the transfer is end 0: the transfer isn't end or SFC is IDLE 1: the transfer is end This bit will generate INT_END signal.	R
3	TRAN_REQ	0: no request 1: vacancy num in FIFO is more than or equal to the threshold. This bit will generate the INT_TREQ interrupt.	R
2	RECE_REQ	0: no request 1: data num in FIFO is more than or equal to the threshold. This bit will generate the INT_RREQ interrupt.	R
1	OVER	0: no over-run 1: FIFO is over-run. This bit will generate the INT_OVER interrupt.	R
0	UNDER	0: no error. 1: FIFO is under-run This bit will generate INT_UNDR signal.	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

5.7.3.16 SFC Status Clear Register

	SFC_SCR																															Base + 0x006c
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											CLR_END	CLR_TREQ	CLR_RREQ	CLR_OVER	CLR_RUNDR
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:5	Reserved	Write has no effect. Read as zero.	R
4	CLR_END	0: has no effect. 1: clear the SFC_SR.END flag and the INT_END.	W
3	CLR_TREQ	0: has no effect. 1: clear the SFC_SR.TREQ flag and the INT_TREQ	W
2	CLR_RREQ	0: has no effect. 1: clear the SFC_SR.RREQ flag and the INT_RREQ	W
1	CLR_OVER	0: has no effect. 1: clear the SFC_SR.OVER flag and the INT_OVER	W
0	CLR_UNDR	0: has no effect. 1: clear the SFC_SR.UNDER flag and the INT_UNDR	W

5.7.3.17 SFC Interrupt Controller Register

	SFC_INTC																															Base + 0x0070
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											MASK_END	MASK_TREQ	MASK_RREQ	MASK_OVER	MASK_UNDR
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1

Bits	Name	Description	RW
31:5	Reserved	Write has no effect. Read as zero.	R
4	MASK_END	0: the INT_END is not masked, will trigger interrupt signal. 1: the INT_END will be masked (default)	RW
3	MASK_TREQ	0: the INT_TREQ is not masked, will trigger interrupt signal. 1: the INT_TREQ will be masked (default)	RW
2	MASK_RREQ	0: the INT_RREQ is not masked, will trigger interrupt signal. 1: the INT_RREQ will be masked (default)	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

1	MASK_OVER	0: the INT_OVER is not masked, will trigger interrupt signal. 1: the INT_OVER will be masked (default)	RW
0	MASK_UNDR	0: the INT_UNDR is not masked, will trigger interrupt signal. 1: the INT_UNDR will be masked (default)	RW

NOTE: When the interrupt flag is cleared, the next interrupt will be generated immediately, so long as the requirement is contented.

5.7.3.18 SFC FSM Register

	SFC_FSM																															Base + 0x0074
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved												FSM_AHB				FSM_SPI								Reserved	FSM_DMAC			Reserved	FSM_RMC		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	1

Bits	Name	Description	RW
31:20	Reserved	Write has no effect. Read as indeterminate value.	R
19:16	FSM_AHB	The AHB_master module's FSM state	R
15:8	FSM_SPI	The SPI_ctrl module's FSM state	R
7	Reserved	Write has no effect. Read as indeterminate value.	R
6:4	FSM_DMAC	The DMAC module's FSM state	R
3	Reserved	Write has no effect. Read as indeterminate value.	R
2:0	FSM_RMC	The RCM module's FSM state	R

5.7.3.19 SFC Clk_gate Enable register

	SFC_CGE																															Base + 0x0078
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										CGE_FLOW_EN	Reserved	CGE_DMA_EN	CGE_RMC_EN	CGE_SPI_EN	CGE_REG_EN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1

Bits	Name	Description	RW
31:6	Reserved	Write has no effect. Read as indeterminate value.	R
5	CGE_FLOW_EN	0: disable the flow_ctrl modle's clk_gate function 1: enable the flow_ctrl module's clk_gate function (default)	RW
4	Reserved	Write has no effect. Read as indeterminate value.	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

3	CGE_DMA_EN	0: disable the dmac and ahb_mst module's clk_gate function 1: enable the dmac and ahb_mst module's clk_gate function (default)	RW
2	CGE_RMC_EN	0: disable the rmc module's clk_gate function 1: enable the rmc module's clk_gate function (default)	RW
1	CGE_SPI_EN	0: disable the spi and clk_gen module's clk_gate function 1: enable the spi and clk_gen module's clk_gate function (default)	RW
0	CGE_REG_EN	0: disable the reg module's clk_gate function 1: enable the reg module's clk_gate function (default)	RW

Note：please disable all the clock gate function（clear all bits of SFC_CGE）

5.7.3.20 SFC CMD Index register

	SFC_CMD_IDX																															Base + 0x007c
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CDT_DATA_EN	CDT_DIR	Reserved																								CMD_IDX					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	CDT_DATA_EN	This command chain need data transmission.	RW
30	CDT_DIR	Direction of the data transmission. 0: read data from SPI flash 1: write data to SPI flash	RW
29:6	Reserved	Write has no effect. Read as indeterminate value.	R
5:0	CMD_IDX	The cmd index of CDT	RW

5.7.3.21 SFC Column Address Register

	SFC_COL_ADDR																															Base + 0x0080
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	COL_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	COL_ADDR	Column address, cache address. just for CDT mode.	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

5.7.3.22 SFC Row Address Register

	SFC_ROW_ADDR																															Base + 0x0084
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ROW_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	ROW_ADDR	Row address, page address. just for CDT mode.	RW

5.7.3.23 SFC Status Address0 Register

	SFC_STA_ADDR0																															Base + 0x0088
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	STA_ADDR0																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	STA_ADDR0	Status address0. just for CDT mode.	RW

5.7.3.24 SFC Status Address1 Register

	SFC_STA_ADDR1																															Base + 0x008c
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	STA_ADDR1																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	STA_ADDR1	Status address1. just for CDT mode.	RW

5.7.3.25 SFC DMA Descriptor Address Register

	SFC_DES_ADDR	Base + 0x0090

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DES_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DES_ADDR	Descriptor address for DMA.	RW

5.7.3.26 SFC CDT register

	SFC_CDT																															Base + 0x0800 ~ Base + 0x0c00
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CDT																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	CDT	CDT's register interface	RW

5.7.3.27 SFC Date Register

	SFC_DR																															Base + 0x1000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DR	Data register interface for data buffer.	RW

5.8 Software Guideline

5.8.1 CDT Description

Each command consists of 4 words, and each one can link the next one or not.

Hardware execute one command chain each time. At most only once data transmission in one command chain.

The structure of each command as follows:

Num	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

0	LINK													ENDIAN	WORD_UNIT										TRAN_MODE			ADDR_KIND
1	CLK_MODE			ADDR_WIDTH			POLL_EN	CMD_EN	PHASE_FORMAT	DMY_BITS						DATA_EN	TRAN_CMD											
2	DEV_STA_EXP																											
3	DEV_STA_MSK																											

Name	Description
LINK	1: it is not the last command of the chain. 0: it is the last command of the chain.
ADDR_KIND	0: Column address(SFC_COL_ADDR) 1: Row address(SFC_ROW_ADDR) 2: Status address0(SFC_STA_ADDR0) 3: Status address1(SFC_STA_ADDR1)
others	the definition of the rest signals are consistent with the above register definition.

5.8.2 DMA Descriptor

Each descriptor consists of 4 words. Hardware execute one descriptor chain each time.

The structure of each descriptor as follows:

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1st	NEXT_DES_ADDR																															
2nd	MEM_ADDR																															
3rd	TRAN_LEN																															

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

4th		LINK

Name	Description
NEXT_DES_ADDR	The next descriptor's phy address.
MEM_ADDR	Current transfer data phy address
TRAN_LEN	Current transfer data length
LINK	1: this is not the last descriptor. 0: this is the last descriptor.
others	the definition of the rest signals are consistent with the above register definition.

5.8.3 Phase Description

- ✧ The phase is consisted of four sections: CMD, ADDR, DUMMY, DATA.
- ✧ Each phase could have one or more sections, four at the most.
- ✧ For one section, one phase could have one at the most.
- ✧ In all phases, only one phase can have DATA section.(we call this phase as data phase, other are command phase)
- ✧ Sections in a phase will be operated by two sequence format:

CMD	ADDR	DUMMY	DATA

Format0

CMD	DUMMY	ADDR	DATA

Format1

- ✧ For one flow, only one kind of the direction of transmission is supported.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

5.8.4 Multi phases flow

Figure 5-8 Multi phases flow

1 Configure the parameter related to the device hardware.
Such as the default level of IO port, timing parameter, etc.
related reg：SFC_DEV_CONF

2 Configure the parameter related to this transmission flow.
Such as num of phase, command format, operation mode, source address and target address, transfer direction and length, etc.
related reg：SFC_GLB、SFC_DEV_STA_EXP、SFC_DEV_STA_MSK、SFC_TRAN_CONF0-6、SFC_TRAN_LEN、SFC_DEV_ADDR0-6、SFC_MEM_ADDR

3 Open the trigger
related reg：SFC_TRIG

4 Waiting for end_end

5 Repeat step 2 for other flow

5.8.5 One phase flow

The flow can also be executed by only one phase. The NAND write perspective flow shown in the Figure 5-9 as follow:

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Figure 5-9 One phase flow

5.8.6 Meters of DMA operation need attention

DMA need some other parameter on the basic configuration.

- configure SFC_GLB (BURST_LEN、OP_MODE、BURST_LEN)
- configure SFC_MEM_ADDR (the memory address)

5.8.7 Meters of slave mode operation need attention

- For each data transfer phase, there must a flush operation before phase starting.
- The SFC will generate request according to the THRESHOLD. When CPU polling the SFC_SR register or waiting an interrupt, the number of data, that transferred by AHB bus each time must match the THRESHOLD.

5.8.8 Example (NAND flash write with multi phases in DMA mode)

a) configure SFC_DEV_CONF and SFC_GLB register

b) program load (PL)

Configure the parameter of PL into phase0 registers:

– configure the SFC_TRAN_CONF0(TRAN_MODE, CMD_EN, ADDR_WIDTH, DMY_NUM, etc)

– configure SFC_DEV_ADDR0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

– configure SFC_TRAN_LEN

c) write enable (WE)

Configure the parameter of WE into phase1 registers:

– configure SFC_TRAN_CONF1(TRAN_MODE, CMD_EN, CMD, etc)

d) program execute

Configure the parameter of PE into phase2 registers:

– configure SFC_TRAN_CONF2(TRAN_MODE, CMD_EN, ADDR_WIDTH, CMD, etc)

– configure SFC_DEV_ADDR2

e) get features command to read the status

Configure the parameter of PE into phase3 registers:

– configure SFC_TRAN_CONF3(TRAN_MODE, CMD_EN, ADDR_WIDTH, CMD, POLL_EN, etc)

– configure SFC_DEV_ADDR3

– configure SFC_DEV_STA_EXP

– configure SFC_DEV_STA_MSK

f) Start

g) waiting the END interrupt

h) clear the END bit zone

5.8.9 Example (NAND flash write with multi phases in DMA descriptor mode)

a) configure SFC_DEV_CONF and SFC_GLB register

b) configure DMA descriptor

– create dma descriptor in system mem

– configure SFC_DES_ADDR(the first descriptor phy address of the descriptor link)

c) program load (PL)

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Configure the parameter of PL into phase0 registers:

– configure the SFC_TRAN_CONF0(TRAN_MODE, CMD_EN, ADDR_WIDTH, DMY_NUM, etc)
– configure SFC_DEV_ADDR0

d) write enable (WE)

Configure the parameter of WE into phase1 registers:

– configure SFC_TRAN_CONF1(TRAN_MODE, CMD_EN, CMD, etc)

e) program execute

Configure the parameter of PE into phase2 registers:

– configure SFC_TRAN_CONF2(TRAN_MODE, CMD_EN, ADDR_WIDTH, CMD, etc)
– configure SFC_DEV_ADDR2

f) get features command to read the status

Configure the parameter of PE into phase3 registers:

– configure SFC_TRAN_CONF3(TRAN_MODE, CMD_EN, ADDR_WIDTH, CMD, POLL_EN, etc)
– configure SFC_DEV_ADDR3
– configure SFC_DEV_STA_EXP
– configure SFC_DEV_STA_MSK

g) Start

h) waiting the END interrupt

i) clear the END bit zone

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

5.8.10 Example (NAND flash write with multi phases in CDT mode)

a) configure SFC_DEV_CONF and SFC_GLB register
b) configure CDT registers
c) According CDT ADDR_KIND to config Address regiters(SFC_COL_ADDR, SFC_ROW_ADDR, SFC_STA_ADDR0, SFC_STA_ADDR1)
d) configure CDT index register SFC_CMD_IDX
e) Start
f) Waiting END and clear.

5.8.11 Example (NAND flash write with single phase in REG mode)

a) configure SFC_DEV_CONF and SFC_GLB register
b) program load (PL)

i. Set SFC_CTRL.FLUSH
ii. Configure the parameter of PL into phase0 registers:
– configure the SFC_TRAN_CONF0(TRAN_MODE, CMD_EN, ADDR_WIDTH, DMY_NUM, etc)
– configure SFC_DEV_ADDR0
– configure SFC_TRAN_LEN
– configure SFC_GLB.TRANS_DIR
iii. Start
iv. waiting SFC_SR.TREQ and clear, then set data to FIFO according to the THRESHOLD. Looping until all data trans end.
v. Waiting END and clear.

c) write enable (WE)

i. Configure the parameter of WE into phase0 registers:
– configure SFC_TRAN_CONF0(TRAN_MODE, CMD_EN, CMD, etc)
ii. Start
iii. Waiting END and clear.

d) program execute

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

i. Configure the parameter of PE into phase0 registers:
   – configure SFC_TRAN_CONF0(TRAN_MODE, CMD_EN, ADDR_WIDTH, CMD, etc)
   – configure SFC_DEV_ADDR0
ii. Start
iii. Waiting END and clear.

e) get features command to read the status

i. Configure the parameter of PE into phase0 registers:
   – configure SFC_TRAN_CONF0(TRAN_MODE, CMD_EN, ADDR_WIDTH, CMD, etc)
   – configure SFC_DEV_ADDR0
   – configure SFC_TRANS_LEN
   – configure SFC_GLB.TRANS_DIR
ii. Start
iii. waiting SFC_SR.RREQ and clear, then get data from FIFO according to the THRESHOLD. Looping until all data trans end.
iv. Waiting END and clear.

5.9 Index

Table 5-3 Terms and Abbreviations

Name	Description
AHB	Advanced Microcontroller Bus Architecture
Dual SPI	See SPI
CPU	Central Processing Unit
DMA	Direct Memory Access
LUT	Look up table.
Endian	The convention used to interpret the bytes making up a data word when those bytes are stored in computer memory. See Endianness at Wikipedia
FIFO	First In, First Out, a method for organizing and manipulating a data buffer
LSB	See Endian
MSB	See Endian
Quad SPI	See SPI
SPI	Serial Peripheral Interface

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Standard SPI	See SPI
tCHSH	Time from clock pull high to select pull low. See a NOR Flash device spec
tSHSL	Time from select pull high to select pull low. See a NOR Flash device spec
tSLCH	Time from select pull low to clock pull high. See a NOR Flash device spec

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Section 4

CAMERA/AUDIO/DISPLAY

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

6 MIPI_CSI Interface

6.1 Overview

The CSI-2 Host Controller is a digital core that implements all protocol functions defined in the MIPI CSI-2 Specification, providing an interface between the System and the MIPI D-PHY, allowing the communication with a MIPI CSI-2 compliant Camera Sensor.

6.1.1 Features

- Support i2c interface to configure.
- Support up to 2 D-PHY Rx Data Lanes.
- Compliant with MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2).
- Dynamically configurable multi-lane merging.
- Long and Short packet decoding.
- Timing accurate signaling of Frame and Line synchronization packets.
- 32-bit Image Data.
- Support all primary and secondary data formats:
  - RGB, YUV and RAW color space definitions
  - From 24-bit down to 6-bit per pixel
  - Generic or user-defined byte-based data types.
- Error detection and correction.

6.2 Register Descriptions

6.2.1 Register Mapping

Following chapter will descript the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. Register read/write attribute
   R - Read only
   W - Write only
   RW - read and write
   RCW - read and write, but clear to 0 by read
   RSW - read and write, but set to 1 by read
   RWC - read and write, clear to 0 by write 1, write 0 has no effect
   RWS - read and write, set to 1 by write 1, write 0 has no effect
   RC - read only, and clear to 0 by read
   RW - read only, and set to 1 by read
   SPEC - special access method, relate to its description
3. Reset Value
   1 - reset to 1
   0 - reset to 0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

? - value unknown after reset

The base address of MIPI_CSI is 0x10073000.

Table 6-1 MIPI_CSI Registers Description

Name	Description	RW	Reset Value	Offset Address	Width
VERSION	Version of the CSI-2 host controller	R	CSI_VERSION_ID	0x000	32
N_LANES	Number of active data lanes	R/W	CSI_N_LANES	0x004	1
PHY_SHUTDOWNZ	PHY shutdown control	R/W	0	0x008	1
DPHY_RSTZ	DPHY reset control	R/W	0	0x00c	1
CSI2_RESETN	CSI-2 controller reset	R/W	0	0x010	1
PHY_STATE	General settings for all blocks	R	0	0x014	12
DATA_IDS	List of Data Ids for which IDI reports line boundary matching errors (CSI2_HOST_N_DATA_IDS > 0)	R/W	0	0x018	32
ERR1	Error state register 1	R	0	0x020	29
ERR2	Error state register 2	R	0	0x024	16
MASK1	Masks for errors 1	R/W	0	0x028	29
MASK2	Masks for errors 2	R/W	0	0x02c	16
PHY_TST_CRTL0	D-PHY Test interface control 0	R/W	0	0x030	2
PHY_TST_CRTL1	D-PHY Test interface control 1	R/W	0	0x034	17

6.2.2 VERSION

	VERSION																															BASE+0x000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VERSION																															
RST																																

Bits	Name	Description	R/W
31:0	VERSION	Version of the CSI-2 Host Controller	R

6.2.3 N_LANES

	N_LANES																															BASE+0x004
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Reserved																																N_LANES
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:1	Reserved	Writing has no effect, read as zero.	R
0	N_LANES	Number of Active Data Lanes. • 0: 1 Data Lane (Lane 0) • 1: 2 Data Lanes (Lane 0, and 1) Can only be updated when the PHY lane is in stopstate	R/W

6.2.4 PHY_SHUTDOWNZ

	PHY_SHUTDOWNZ																																**BASE+0x008**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	Reserved																																PHY_SHUTDOWNZ
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:1	Reserved	Writing has no effect, read as zero.	R
0	PHY_SHUTDOWNZ	Shutdown input. This line is used to place the complete macro in power down. All analog blocks are in power down mode and digital logic is cleared. Active Low.	R/W

6.2.5 DPHY_RSTZ

	DPHY_RSTZ																																**BASE+0x00C**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	Reserved																																DPHY_RSTZ
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	R/W
31:1	Reserved	Writing has no effect, read as zero.	R
0	DPHY_RSTZ	DPHY reset output. Active Low.	R/W

6.2.6 CSI2_RESETN

	CSI2_RESETN																															BASE+0x010
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Rserved																															CSI_RESETN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:1	Reserved	Writing has no effect, read as zero.	R
0	CSI_RESETN	CSI-2 controller reset output. Active Low.	R/W

6.2.7 PHY_STATE

	PHY_STATE																															BASE+0x014
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				bypass_2ecc_tst	phy_stopstateclk	phy_rxclkactivehs	phy_rxclkactivehs	Reserved		phy_stopstatedata_1	phy_stopstatedata_0	Reserved		phy_rxulpsesc_1	phy_rxulpsesc_0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:12	Reserved	Writing has no effect, read as zero.	R
11	bypass_2ecc_tst	Payload Bypass test mode for double ECC errors	R/W
10	phy_stopstateclk	Clock Lane in Stop state	R
9	phy_rxulpsclknot	Active Low. This signal indicates that the Clock Lane module has entered the Ultra Low Power state	R
8	phy_rxclkactivehs	Indicates that the clock lane is actively receiving a DDR clock	R
7:6	Reserved	Writing has no effect, read as zero.	R
5	phy_stopstatedata_1	Data Lane 1 in Stop state	R
4	phy_stopstatedata_0	Data Lane 0 in Stop state	R
3:2	Reserved	Writing has no effect, read as zero.	R
1	phy_rxulpsesc_1	Lane module 1 has entered the Ultra Low Power mode	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

0	phy_rxulpsesc_0	Lane module 0 has entered the Ultra Low Power mode	R

6.2.8 DATA_IDS

	DATA_IDS																															BASE+0x018
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	di3_vc		di3_dt						di2_vc		di2_dt						di1_vc		di1_dt						di0_vc		di0_dt					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:30	di3_vc	Data ID 3 Virtual channel	R/W
29:24	di3_dt	Data ID 3 Data Type	R/W
23:22	di2_vc	Data ID 2 Virtual channel	R/W
21:16	di2_dt	Data ID 2 Data Type	R/W
15:14	di1_vc	Data ID 1 Virtual channel	R/W
13:8	di1_dt	Data ID 1 Data Type	R/W
7:6	di0_vc	Data ID 0 Virtual channel	R/W
5:0	di0_dt	Data ID 0 Data Type	R/W

6.2.9 ERR1

	ERR1																															BASE+0x020
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			err_ecc_double	vc3_err_crc	vc2_err_crc	vc1_err_crc	vc0_err_crc	err_l_seq_di3	err_l_seq_di2	err_l_seq_di1	err_l_seq_di0	err_l_bndry_match_di3	err_l_bndry_match_di2	err_l_bndry_match_di1	err_l_bndry_match_di0	err_frame_data_vc3	err_frame_data_vc2	err_frame_data_vc1	err_frame_data_vc0	err_f_seq_vc3	err_f_seq_vc2	err_f_seq_vc1	err_f_seq_vc0	err_f_bndry_match_vc3	err_f_bndry_match_vc2	err_f_bndry_match_vc1	err_f_bndry_match_vc0	Reserved		phy_errsotsynchs_1	phy_errsotsynchs_0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:29	Reserved	Writing has no effect, read as zero.	R
28	err_ecc_double	Header ECC contains 2 errors. Unrecoverable	R
27	vc3_err_crc	Checksum Error detected on Virtual Channel 3	R
26	vc2_err_crc	Checksum Error detected on Virtual Channel 2	R
25	vc1_err_crc	Checksum Error detected on Virtual Channel 1	R
24	vc0_err_crc	Checksum Error detected on Virtual Channel 0	R
23	err_l_seq_di3	Error in the sequence of lines for vc0 and dt3	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

22	err_l_seq_di2	Error in the sequence of lines for vc0 and dt2	R
21	err_l_seq_di1	Error in the sequence of lines for vc0 and dt1	R
20	err_l_seq_di0	Error in the sequence of lines for vc0 and dt0	R
19	err_l_bndry_match_di3	Error matching Line Start with Line End for vc3 and dt	R
18	err_l_bndry_match_di2	Error matching Line Start with Line End for vc2 and dt	R
17	err_l_bndry_match_di1	Error matching Line Start with Line End for vc1 and dt	R
16	err_l_bndry_match_di0	Error matching Line Start with Line End for vc0 and dt	R
15	err_frame_data_vc3	Last received frame, in Virtual Channel 3, had at least one CRC error	R
14	err_frame_data_vc2	Last received frame, in Virtual Channel 2, had at least one CRC error	R
13	err_frame_data_vc1	Last received frame, in Virtual Channel 1, had at least one CRC error	R
12	err_frame_data_vc0	Last received frame, in Virtual Channel 0, had at least one CRC error	R
11	err_f_seq_vc3	Incorrect Frame Sequence detected in Virtual Channel 3	R
10	err_f_seq_vc2	Incorrect Frame Sequence detected in Virtual Channel 2	R
9	err_f_seq_vc1	Incorrect Frame Sequence detected in Virtual Channel 1	R
8	err_f_seq_vc0	Incorrect Frame Sequence detected in Virtual Channel 0	R
7	err_f_bndry_match_vc3	Error matching Frame Start with Frame End for Virtual Channel 3	R
6	err_f_bndry_match_vc2	Error matching Frame Start with Frame End for Virtual Channel 2	R
5	err_f_bndry_match_vc1	Error matching Frame Start with Frame End for Virtual Channel 1	R
4	err_f_bndry_match_vc0	Error matching Frame Start with Frame End for Virtual Channel 0	R
3:2	Reserved	Writing has no effect, read as zero.	R
1	phy_errsotsynchs_1	Start of Transmission Error on data lane 1 (no synchronization achieved)	R
0	phy_errsotsynchs_0	Start of Transmission Error on data lane 0 (no synchronization achieved)	R

6.2.10 ERR2

	ERR2																															BASE+0x024
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Reserved																err_id_vc3	err_id_vc2	err_id_vc1	err_id_vc0	vc3_err_ecc_corrected	vc2_err_ecc_corrected	vc1_err_ecc_corrected	vc0_err_ecc_corrected	Reserved		phy_errsoths_1	phy_errsoths_0	Reserved		phy_ erresc _1	phy_erresc_0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15	err_id_vc3	Unrecognized or unimplemented data type detected in Virtual Channel 3	R
14	err_id_vc2	Unrecognized or unimplemented data type detected in Virtual Channel 2	R
13	err_id_vc1	Unrecognized or unimplemented data type detected in Virtual Channel 1	R
12	err_id_vc0	Unrecognized or unimplemented data type detected in Virtual Channel 0	R
11	vc3_err_ecc_corrected	Header error detected and corrected on Virtual Channel 3	R
10	vc2_err_ecc_corrected	Header error detected and corrected on Virtual Channel 2	R
9	vc1_err_ecc_corrected	Header error detected and corrected on Virtual Channel 1	R
8	vc0_err_ecc_corrected	Header error detected and corrected on Virtual Channel 0	R
7:6	Reserved	Writing has no effect, read as zero.	R
5	phy_errsoths_1	Start of Transmission Error on data lane 1(synchronization can still be achieved)	R
4	phy_errsoths_0	Start of Transmission Error on data lane 0(synchronization can still be achieved)	R
3:2	Reserved	Writing has no effect, read as zero.	R
1	phy_ erresc _1	Escape Entry Error (ULPM) on data lane 1	R
0	phy_erresc_0	Escape Entry Error (ULPM) on data lane 0	R

6.2.11 MASK1

	MASK1																BASE+0x028															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Reserved			mask_err_ecc_double	mask_vc3_err_crc	mask_vc2_err_crc	mask_vc1_err_crc	mask_vc0_err_crc	mask_err_l_seq_di3	mask_err_l_seq_di2	mask_err_l_seq_di1	mask_err_l_seq_di0	mask_err_l_bndry_match_di3	mask_err_l_bndry_match_di2	mask_err_l_bndry_match_di1	mask_err_l_bndry_match_di0	mask_err_frame_data_vc3	mask_err_frame_data_vc2	mask_err_frame_data_vc1	mask_err_frame_data_vc0	mask_err_f_seq_vc3	mask_err_f_seq_vc2	mask_err_f_seq_vc1	mask_err_f_seq_vc0	mask_err_f_bndry_match_vc3	mask_err_f_bndry_match_vc2	mask_err_f_bndry_match_vc1	mask_err_f_bndry_match_vc0	Reserved		mask_phy_errsotsynchs_1	mask_phy_errsotsynchs_0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:29	Reserved	Writing has no effect, read as zero.	R
28	mask_err_ecc_double	Mask for err_ecc_double	R/W
27	mask_vc3_err_crc	Mask for vc3_err_crc	R/W
26	mask_vc2_err_crc	Mask for vc2_err_crc	R/W
25	mask_vc1_err_crc	Mask for vc1_err_crc	R/W
24	mask_vc0_err_crc	Mask for vc0_err_crc	R/W
23	mask_err_l_seq_di3	Mask for err_l_seq_di3	R/W
22	mask_err_l_seq_di2	Mask for err_l_seq_di2	R/W
21	mask_err_l_seq_di1	Mask for err_l_seq_di1	R/W
20	mask_err_l_seq_di0	Mask for err_l_seq_di0	R/W
19	mask_err_l_bndry_match_di3	Mask for err_l_bndry_match_di3	R/W
18	mask_err_l_bndry_match_di2	Mask for err_l_bndry_match_di2	R/W
17	mask_err_l_bndry_match_di1	Mask for err_l_bndry_match_di1	R/W
16	mask_err_l_bndry_match_di0	Mask for err_l_bndry_match_di0	R/W
15	mask_err_frame_data_vc3	Mask for err_frame_data_vc3	R/W
14	mask_err_frame_data_vc2	Mask for err_frame_data_vc2	R/W
13	mask_err_frame_data_vc1	Mask for err_frame_data_vc1	R/W
12	mask_err_frame_data_vc0	Mask for err_frame_data_vc0	R/W
11	mask_err_f_seq_vc3	Mask for err_f_seq_vc3	R/W
10	mask_err_f_seq_vc2	Mask for err_f_seq_vc2	R/W
9	mask_err_f_seq_vc1	Mask for err_f_seq_vc1	R/W
8	mask_err_f_seq_vc0	Mask for err_f_seq_vc0	R/W
7	mask_err_f_bndry_match_vc3	Mask for err_f_bndry_match_vc3	R/W
6	mask_err_f_bndry_match_vc2	Mask for err_f_bndry_match_vc2	R/W
5	mask_err_f_bndry_match_v	Mask for err_f_bndry_match_vc1	R/W

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	c1		
4	mask_err_f_bndry_match_vc0	Mask for err_f_bndry_match_vc0	R/W
3:2	Reserved	Writing has no effect, read as zero.	R
1	mask_phy_errsotsynchs_1	Mask for phy_errsotsynchs_1	R/W
0	mask_phy_errsotsynchs_0	Mask for phy_errsotsynchs_0	R/W

6.2.12 MASK2

	MASK2																															BASE+0x02C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																mask_err_id_vc3	mask_err_id_vc2	mask_err_id_vc1	mask_err_id_vc0	mask_vc3_err_ecc_corrected	mask_vc2_err_ecc_corrected	mask_vc1_err_ecc_corrected	mask_vc0_err_ecc_corrected	Reserved		mask_phy_errsoths_1	mask_phy_errsoths_0	Reserved		mask_phy_ erresc _1	mask_phy_erresc_0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15	mask_err_id_vc3	Mask for err_id_vc3	R/W
14	mask_err_id_vc2	Mask for err_id_vc2	R/W
13	mask_err_id_vc1	Mask for err_id_vc1	R/W
12	mask_err_id_vc0	Mask for err_id_vc0	R/W
11	mask_vc3_err_ecc_corrected	Mask for vc3_err_ecc_corrected	R/W
10	mask_vc2_err_ecc_corrected	Mask for vc2_err_ecc_corrected	R/W
9	mask_vc1_err_ecc_corrected	Mask for vc1_err_ecc_corrected	R/W
8	mask_vc0_err_ecc_corrected	Mask for vc0_err_ecc_corrected	R/W
7:6	Reserved	Writing has no effect, read as zero.	R
5	mask_phy_errsoths_1	Mask for phy_errsoths_1	R/W
4	mask_phy_errsoths_0	Mask for phy_errsoths_0	R/W
3:2	Reserved	Writing has no effect, read as zero.	R
1	mask_phy_ erresc _1	Mask for phy_erresc_1	R/W
0	mask_phy_erresc_0	Mask for phy_erresc_0	R/W

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

6.2.13 PHY_TST_CRTL0

	PHY_TST_CRTL0																															BASE+0x030
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														phy_testclk	phy_testclr
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:2	Reserved	Writing has no effect, read as zero.	R
1	phy_testclk	PHY test interface strobe signal. Used to clock TESTDIN bus into the DPHY. In conjunction with TESTEN signal controls the operation selection.	R/W
0	phy_testclr	PHY test interface clear. Used when active performs vendor specific interface initialization (Active High).	R/W

6.2.14 PHY_TST_CRTL1

	PHY_TST_CRTL1																															BASE+0x034
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved															phy_testen	phy_testdout								phy_testdin							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:17	Reserved	Writing has no effect, read as zero.	R
16	phy_testen	PHY test interface operation selector: • 1: Configures address write operation on the falling edge of TESTCLK • 0: Configures a data write operation on the rising edge of TESTCLK	R/W
15:8	phy_testdout	PHY output 8-bit data bus for read-back and internal probing functionalities.	R
7:0	phy_testdin	PHY test interface input 8-bit data bus for internal register programming and test functionalities access	R/W

6.3 Operation

The following sections describe the MIPI_CSI operations of configuration.

The Initialization steps are as follows:

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

1. De-assert CSI-2 presetn signal (global reset).
2. Set number of Lanes(register N_LANES).
3. De-assert PHY shutdown (register PHY_SHUTDOWNZ)
4. De-assert PHY reset (register PHY_RSTZ)
5. De-assert CSI reset (register CSI2-RESETN)
6. Wait for 200us, read the PHY status register (PHY_STATE) to confirm that all data and clock lanes of the D-PHY are in Stop State.
7. Configure the camera sensor to start transmitting a clock on the D-PHY clock lane.
8. Read the PHY status register(PHY_STATE) to confirm that the D-PHY is receiving a clock on the D-PHY clock lane.
9. Meting the steps above, configure the camera sensor to start transmitting packages.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

7 MIPI D-PHY Receiver

MIPI D-PHY RX integrates 1 Clock Lane and up to 2 Data Lanes MIPI D-PHY compatible High-speed receiver that supports 80Mbps up to 1.5GHz data transfer rate, and Low-power receiver that supports data transfer in 10Mbps. It is optimized with low power design for mobile CSI-2 slave application. The interface of D-PHY is designed for standard MIPI D-PHY PPI interface. It can be easily integrated into the lane management of each customer's CSI-2 controller

7.1 Overview

Features:

- Supports standard 8b PPI interface compliant of MIPI D-PHY Spec.
- Supports 1 Clock Lane & up to 2 Data Lanes in DPHY mode.
- Supports HS-Rx Data rate from 80Mbps up to 1.5Gbps. (DPHY)
- Supports LS-Rx Data rate of 10Mbps & Ultra-low power mode.
- Supports Triggers, ULPS and LPDT.
- Supports on-die terminated and non-terminated operation, integrates switchable termination.
- Supports Fault Detection of Sequence Error. (Error Report)
- Build-in BISTTX for at-speed testing.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

7.2 Functional Blocks

Figure 7-1Functional Block Diagram

The MIPI D-PHY IP has the following main blocks:

Item	Description
HS Receiver	Implements high speed RX functionalities. Replicated for each lanes.
LP Receiver	Implements the low power RX functionality. Replicated for each lanes.
Digital Blocks	Includes all control logic as well as PPI interface.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

7.3 Registers Description

7.3.1 Instructions

Following chapter will descript the functions of all software accessible registers.

Conventions:

5. Register Address = Base + Address offset
6. The registers can be read and written by AHB2 bus
7. Register read/write attribute
    - ✧ R - Read only
    - ✧ W - Write only
    - ✧ RW - read and write
    - ✧ RCW - read and write, but clear to 0 by read
    - ✧ RSW - read and write, but set to 1 by read
    - ✧ RWC - read and write, clear to 0 by write 1, write 0 has no effect
    - ✧ RWS - read and write, set to 1 by write 1, write 0 has no effect
    - ✧ RC - read only, and clear to 0 by read
    - ✧ RS - read only, and set to 1 by read
    - ✧ SPEC - special access method, relate to its description
8. Reset Value
    - 1 - reset to 1
    - 0 - reset to 0
    - ? - value unknown after reset

7.3.2 Map

The MIPI-RX-PHY's registers map base address is 0x10076000

Table 7-1 MIPI D-PHY RX Registers Map

Name	Reset Value	Address Offset	Description	RW	Mask
RXPHY_REG_0_00	0x0000_0001	0x0000	RX Configure Input	RW	0x0000_00FF
RXPHY_REG_0_0d	0x0000_00C0	0x0034	RX Configure Input	RW	0x0000_00FF
RXPHY_REG_0_0e	0x0000_0036	0x0038	RX Configure Input	RW	0x0000_00FF
RXPHY_REG_0_0f	0x0000_00DB	0x003C	RX Configure Input	RW	0x0000_00FF
RXPHY_REG_0_12	0x0000_0010	0x0048	RX Configure Input	RW	0x0000_00FF

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

RXPHY_REG_1_00	0x0000_001F	0x0080	RX Configure Input	RW	0x0000_00FF
RXPHY_REG_2_0a	0x0000_000F	0x0128	RX Configure Input	RW	0x0000_00FF
RXPHY_REG_2_10	0x0000_0004	0x0140	RX Configure Input	RW	0x0000_00FF
RXPHY_REG_2_11	0x0000_0001	0x0144	RX Configure Input	RW	0x0000_00FF
RXPHY_REG_2_12	0x0000_0032	0x0148	RX Configure Input	RW	0x0000_00FF
RXPHY_REG_2_18	0x0000_001B	0x0160	RX Configure Input	RW	0x0000_00FF
RXPHY_REG_2_1a	0x0000_007F	0x0168	RX Configure Input	RW	0x0000_00FF
RXPHY_REG_3_0e	0x0000_0086	0x01B8	RX Configure Input	RW	0x0000_00FF
RXPHY_REG_3_10	0x0000_0004	0x01C0	RX Configure Input	RW	0x0000_00FF
RXPHY_REG_3_11	0x0000_0001	0x01C4	RX Configure Input	RW	0x0000_00FF
RXPHY_REG_3_12	0x0000_0032	0x01C8	RX Configure Input	RW	0x0000_00FF
RXPHY_REG_3_18	0x0000_001B	0x01E0	RX Configure Input	RW	0x0000_00FF
RXPHY_REG_3_1a	0x0000_007F	0x01E8	RX Configure Input	RW	0x0000_00FF
RXPHY_REG_4_0e	0x0000_0086	0x0238	RX Configure Input	RW	0x0000_00FF

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

RXPHY_REG_4_10	0x0000_0004	0x0240	RX Configure Input	RW	0x0000_00FF
RXPHY_REG_4_11	0x0000_0001	0x0244	RX Configure Input	RW	0x0000_00FF
RXPHY_REG_4_12	0x0000_0032	0x0248	RX Configure Input	RW	0x0000_00FF
RXPHY_REG_4_18	0x0000_001B	0x0260	RX Configure Input	RW	0x0000_00FF
RXPHY_REG_4_1a	0x0000_007F	0x0268	RX Configure Input	RW	0x0000_00FF

7.3.3 Configure

7.3.3.1 RXPHY_REG_0_00

	RXPHY_REG_0_00																															BASE + 0x0000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																									lane_en_ck	Reserved		lane_en_1	lane_en_0	power_work	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Name	Description	RW
31:7	Reserved	Writing has no effect, read as zero.	R
6	lane_en_ck	Enable D-PHY clock lane: active high	RW
5:4	Reserved	Writing has no effect, read as zero.	R
3	lane_en_1	Enable D-PHY lane1: active high	RW
2	lane_en_0	Enable D-PHY lane0: active high	RW
1:0	power_work	00/01: power work enable 10: power work disable 11:reserved	RW

7.3.3.2 RXPHY_REG_0_0d

	RXPHY_REG_0_0d																															BASE + 0x0034
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Reserved																																phase	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0

Bits	Name	Description	RW
31:3	Reserved	Writing has no effect, read as zero.	R
2:1	phase	Digital clock sample manual set 8 phases: 000: phase 0 (default value) 001: phase 1 010: phase 2 011: phase 3 … 111: phase 7 Phase 0 is earliest and phase 7 is latest. Each step between the adjacent phase is about 40ps.	RW

7.3.3.3 RXPHY_REG_0_0e

	XCFGI_BLOCK_R_11_08																BASE + 0x0038															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																									phase			Reserved			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	0

Bits	Name	Description	RW
31:7	Reserved		R
6:4	phase	Clock lane manual set 8 phases: 000: phase 0 001: phase 1 010: phase 2 011: phase 3 (default value) …. 111: phase 7 Phase 0 is earliest and phase 7 is latest. Each step between the adjacent phase is about 40 ps.	RW
3:0	Reserved		R

7.3.3.4 RXPHY_REG_0_0f

	RXPHY_REG_0_0f	BASE + 0x003C

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										phase1			phase0		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	0	1	1

Bits	Name	Description	RW
31:6	Reserved		RW
5:3	phase1	Data lane 1 manual set 8 phases: 000: phase 0 001: phase 1 010: phase 2 011: phase 3 (default value) …. 111: phase 7 Phase 0 is earliest and phase 7 is latest. Each step between the adjacent phase is about 40 ps	RW
2:0	phase0	Data lane 0 manual set 8 phases: 000: phase 0 001: phase 1 010: phase 2 011: phase 3 (default value) …. 111: phase 7 Phase 0 is earliest and phase 7 is latest. Each step between the adjacent phase is about 40 ps	RW

7.3.3.5 RXPHY_REG_0_12

	RXPHY_REG_0_12																															BASE + 0x0048
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								reverse_clk	Reserved						
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Name	Description	RW
31:8	Reserved		RW
7	reverse_clk	Reverse the digital sample clock 0: make the digital sample clock positive (default value) 1: reverse the digital sample clock	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

6:0	Reserved		RW

7.3.3.6 RXPHY_REG_1_00

	RXPHY_REG_1_00																															BASE + 0x0080
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															reg_dig_rstn
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1

Bits	Name	Description	RW
31:1	Reserved		R
0	reg_dig_rstn	1: normal 0: reset	RW

7.3.3.7 RXPHY_REG_2_0a

	RXPHY_REG_2_0a																															BASE + 0x0128
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										clk_mode		Reserved			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Bits	Name	Description	RW
31:6	Reserved		R
5:4	clk_mode	Only for clock lane 11: enable continuous clock mode 00: disable continuous clock mode	RW
3:0	Reserved		R

7.3.3.8 RXPHY_REG_2_10

	RXPHY_REG_2_10																															BASE + 0x0140
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										Tta-go-counter					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:6	Reserved		RW
5:0	Tta-go-counter	The value of counter for clock lane Tta-go of turnaround Tta-go = Ttxclkesc * value	RW

7.3.3.9 RXPHY_REG_2_11

	RXPHY_REG_2_11																															BASE + 0x0144
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										Tta-sure-counter					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Name	Description	RW
31:6	Reserved		RW
5:0	Tta-wait-counter	The value of counter for clock lane HS Tta-sure of turnaround. Tta-sure = Ttxclkesc * value	RW

7.3.3.10 RXPHY_REG_2_12

	RXPHY_REG_2_12																															BASE + 0x0148
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										Tta-wait-counter					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0

Bits	Name	Description	RW
31:6	Reserved		RW
5:0	Tta-wait-counter	The value of counter for clock lane.Tta-wait of turnaround. Intereval from receiving ppi turnaround request to sending esc request. Tta-wait = Ttxclkesc * value	RW

7.3.3.11 RXPHY_REG_2_18

	RXPHY_REG_2_18																															BASE + 0x0160
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								count_time							

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1

Bits	Name	Description		RW
31:8	Reserved			RW
7:0	count_time	Clock lane configure the count time of the THS-SETTLE by protocol. After the count done, D-PHY will begin to receive the high speed data.		RW
		Frequency(1/UI)	Value	
		80 -- 110 MHz	0x02	
		110 – 150 MHz	0x03	
		150 – 300 MHz	0x06	
		300 – 400 MHz	0x08	
		400 – 500 MHz	0x0b	
		500 – 600 MHz	0x0e	
		600 – 700 MHz	0x10	
		700 – 800 MHz	0x12	
		800 – 1000 MHz	0x16	
		1000 – 1200 MHz	0x1e	
		1200 – 1400 MHz	0x23	
		1400 – 1600 MHz	0x2d	
		1600 – 1800 MHz	0x32	
		1800 – 2000 MHz	0x37	
		2000 – 2200 MHz	0x3c	
		2200 – 2400 MHz	0x41	
		2400 – 2500 MHz	0x46	

7.3.3.12 RXPHY_REG_2_1a

	RXPHY_REG_2_1a																															BASE + 0x0168
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								cal_re_en	Reserved						
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1

Bits	Name	Description	RW
31:8	Reserved		
7	cal_re_en	Clock lane calibration reception enable 1: enable calibration reception 0: disable calibration reception	
6:0	Reserved		

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

7.3.3.13 RXPHY_REG_3_0e

	RXPHY_REG_3_0e																															BASE + 0x01B8
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																									MSB_EN	Reserved					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0

Bits	Name	Description	RW
31:7	Reserved		RW
6	MSB_EN	MSB enable for pin_rxdatahs_0 1: enable 0: enable	RW
5:0	Reserved		RW

7.3.3.14 RXPHY_REG_3_10

	RXPHY_REG_3_10																															BASE + 0x01C0
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										Tta-go-counter					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Name	Description	RW
31:6	Reserved		RW
5:0	Tta-go-counter	The value of counter for data lane 0 Tta-go of turnaround Tta-go = Ttxclkesc * value	RW

7.3.3.15 RXPHY_REG_3_11

	RXPHY_REG_3_11																															BASE + 0x01C4
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										Tta-sure-counter					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Name	Description	RW
31:6	Reserved		RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

5:0	Tta-wait-counter	The value of counter for data lane 0 HS Tta-sure of turnaround. Tta-sure = Ttxclkesc * value	RW

7.3.3.16 RXPHY_REG_3_12

	RXPHY_REG_3_12																															BASE + 0x01C8
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										Tta-wait-counter					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0

Bits	Name	Description	RW
31:6	Reserved		RW
5:0	Tta-wait-counter	The value of counter for data lane 0 Tta-wait of turnaround. Intereval from receiving ppi turnaround request to sending esc request. Tta-wait = Ttxclkesc * value	RW

7.3.3.17 RXPHY_REG_3_18

	RXPHY_REG_3_18																															BASE + 0x01E0
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								count_time							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1

Bits	Name	Description		RW
31:8	Reserved			RW
7:0	count_time	Data lane 0 configure the count time of the THS-SETTLE by protocol. After the count done, D-PHY will begin to receive the high speed data.		RW
		Frequency(1/UI)	Value	
		80 -- 110 MHz	0x02	
		110 – 150 MHz	0x03	
		150 – 300 MHz	0x06	
		300 – 400 MHz	0x08	
		400 – 500 MHz	0x0b	
		500 – 600 MHz	0x0e	
		600 – 700 MHz	0x10	
		700 – 800 MHz	0x12	
		800 – 1000 MHz	0x16	

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		1000 – 1200 MHz	0x1e	
		1200 – 1400 MHz	0x23	
		1400 – 1600 MHz	0x2d	
		1600 – 1800 MHz	0x32	
		1800 – 2000 MHz	0x37	
		2000 – 2200 MHz	0x3c	
		2200 – 2400 MHz	0x41	
		2400 – 2500 MHz	0x46	

7.3.3.18 RXPHY_REG_3_1a

	RXPHY_REG_3_1a																															BASE + 0x01E8
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								cal_re_en	Reserved						
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1

Bits	Name	Description	RW
31:8	Reserved		
7	cal_re_en	Data lane 0 calibration reception enable 1: enable calibration reception 0: disable calibration reception	
6:0	Reserved		

7.3.3.19 RXPHY_REG_4_0e

	RXPHY_REG_4_0e																															BASE + 0x0238
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																									MSB_EN	Reserved					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0

Bits	Name	Description	RW
31:7	Reserved		RW
6	MSB_EN	MSB enable for pin_rxdatahs_1 1: enable 0: enable	RW
5:0	Reserved		RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

7.3.3.20 RXPHY_REG_4_10

	RXPHY_REG_4_10																															BASE + 0x0240
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										Tta-go-counter					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Name	Description	RW
31:6	Reserved		RW
5:0	Tta-go-counter	The value of counter for data lane 1 Tta-go of turnaround Tta-go = Ttxclkesc * value	RW

7.3.3.21 RXPHY_REG_4_11

	RXPHY_REG_4_11																															BASE + 0x0244
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										Tta-sure-counter					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Name	Description	RW
31:6	Reserved		RW
5:0	Tta-wait-counter	The value of counter for data lane 1 HS Tta-sure of turnaround. Tta-sure = Ttxclkesc * value	RW

7.3.3.22 RXPHY_REG_4_12

	RXPHY_REG_4_12																															BASE + 0x0248
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										Tta-wait-counter					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0

Bits	Name	Description	RW
31:6	Reserved		RW
5:0	Tta-wait-counter	The value of counter for data lane 1 Tta-wait of turnaround. Intereval from receiving ppi turnaround request to sending esc request. Tta-wait = Ttxclkesc * value	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

7.3.3.23 RXPHY_REG_4_18

	RXPHY_REG_4_18																															BASE + 0x0260
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								count_time							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1

Bits	Name	Description		RW
31:8	Reserved			RW
7:0	count_time	Data lane 1 configure the count time of the THS-SETTLE by protocol. After the count done, D-PHY will begin to receive the high speed data.		RW
		Frequency(1/UI)	Value	
		80 -- 110 MHz	0x02	
		110 – 150 MHz	0x03	
		150 – 300 MHz	0x06	
		300 – 400 MHz	0x08	
		400 – 500 MHz	0x0b	
		500 – 600 MHz	0x0e	
		600 – 700 MHz	0x10	
		700 – 800 MHz	0x12	
		800 – 1000 MHz	0x16	
		1000 – 1200 MHz	0x1e	
		1200 – 1400 MHz	0x23	
		1400 – 1600 MHz	0x2d	
		1600 – 1800 MHz	0x32	
		1800 – 2000 MHz	0x37	
		2000 – 2200 MHz	0x3c	
		2200 – 2400 MHz	0x41	
		2400 – 2500 MHz	0x46	

7.3.3.24 RXPHY_REG_4_1a

	RXPHY_REG_4_1a																															BASE + 0x0268
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								cal_re_en	Reserved						

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1

Bits	Name	Description	RW
31:8	Reserved		
7	cal_re_en	Data lane 1 calibration reception enable 1: enable calibration reception 0: disable calibration reception	
6:0	Reserved		

7.4 Operation Guide

7.4.1 Logic PHY-Protocol Interface

The PHY Protocol Interface (PPI) is used for making the connection between PHY Lane Modules and the higher protocol layers of a communication stack. The interface described here is intended to be generic and application independent.

This PPI is optimized for controlling a D-PHY and transmitting the parallel data. The interface described here is defined as an on-chip connection, and it does not attempt to minimize signal count or define timing parameters or voltage levels for the PPI signals.

The PPI defines the signals used in the PPI. For a PHY with multiple Data Lanes, a set of PPI signals is used for each Lane

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

8 Camera Interface Module (CIM)

8.1 Overview

The camera interface module (CIM) supports commonly available CMOS/CCD type image sensors. The CIM sources the digital image stream through 8bit DVP or MIPI interface. The CIM can directly connect to external CMOS/CCD image sensors and ITU656 standard video decoders. It is a member of Display System.

8.2 Feature

- ✓ Support ITU656, YCbCr 4:2:2, RGB888, RGB565, 8/10/12-bits MONO, 8/10/12-bits Raw RGB input
- ✓ Support YUV422, RGB888, RGB565, 8-bits MONO, 8-bits RawRGB, 8-bits Y output
- ✓ Support DVP interface and CSI(max 2 lane)
- ✓ Support max to 2047x2047 input and output
- ✓ Crop
- ✓ Support exposure control
- ✓ Auto recovery
- ✓ Support area luminance

Table 8-1 Input/Output format corresponding relationship

Input format	Input order	Output format	Output order
YCbCr4:2:2	Y_0UY_1V, Y_0VY_1U UY_0VY_1, VY_0UY_1	YUV422 8-bits Y	VY_1UY_0
8/10/12-bits Raw RGB	RGGB, BGGR, GRBG, GBRG	8-bits RawRGB 8-bits Y	as same as input order
8/10/12-bits MONO		8-bits MONO 8-bits Y	
RGB565	RGB, RBG GRB, GBR, BRG, BGR	RGB565 8-bits Y	RGB
RGB888	RGB, RBG GRB, GBR, BRG, BGR	RGB888 8-bits Y	RGB
ITU656		YUV422	VY1UY0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

8.3 Function Description

8.3.1 Mode

8.3.1.1 Normal

Camera continuous send frames, the CIM receive selective.

8.3.1.2 Sanpshot

The CIM send an exposure pulse to camera, then receive one frame from camera.

8.4 Data Format Description

8.4.1 Input Data(DVP Interface)

RGB888

RGB565

UYVY

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

8.4.2 Output Data(memory)

RGB888

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

RGB565

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

YUV422package

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
V								Y_1								U								Y_0							

8.4.3 Timing

8.4.4 Others

Start-stop code of ITU656 is composed of FF+00+00+XY. Constitute of XY is as below:

[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	F	V	H	Reserved	Reserved	Reserved	Reserved

F field flag(0:top field,1:bottom field)

V vertical sync(0:active,1:invalid)

H horizontal sync(0:SAV-start of active video,1:EAV-end of active video)

P3-P0 check flag, algorithm is as below:

F	V	H	P3	P2	P1	P0
0	0	0	0	0	0	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

0	1	1	0	1	1	0
1	0	0	0	1	1	1
1	0	1	1	0	1	0
1	1	0	1	1	0	0
1	1	1	0	0	0	1

8.5 Pins Description

Name	Width	I/O	Description
Data	[7:0]	I	DVP interface
hsync	[0:0]	I	
vsync	[0:0]	I	
pixclk	[0:0]	I	pixel clock
exposure	[0:0]	O	Control when to expose

8.6 Architecture map

8.7 Descriptor define

DES_NEXT_ADDR 1st

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	NEXT_ DES_ADDR																															

Bits	Name	Description	RW
31:0	NEXT_ DES_ADDR	The next descriptor's address. **NOTE:** Write **DS_CIM_DES_ADDR** will cover the value.	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

FRM_WRBK_ADDR 2nd

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FRM_WRBK_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	FRM_WRBK_ADDR	Frame WriteBack Buffer head address(aligned to pixel size) When scan mode is 'interlace', these bits are first field buffer's address.	RW

WRBK_STRD 3rd

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																					FRM_WRBK_STRD										
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:11	Reserved	Writing has no effect, read as zero.	R
10:0	FRM_WRBK_STRD	Frame WriteBack stride.(max 2047)(Unit: pixel) Note: For YUV422 format, please set an even.	RW

DES_INTC 4th

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																													SOF_MSK	EOF_MSK	Reserved
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:3	Reserved	Writing has no effect, read as zero.	R
2	SOF_MSK	Mask of SOF. 0: interrupt is masked 1: generate interrupt Work together with DS_CIM_INTC, only when both are 1 will generate interrupt.	RW
1	EOF_MSK	Mask of EOF	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		0: interrupt is masked 1: generate interrupt Work together with DS_CIM_INTC, only when both are 1 will generate interrupt.	
0	Reserved	Writing has no effect, read as zero.	R

DES_CFG 5th

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FRM_ID						Reserved							FRM_WRBK_FMT			Reserved															DES_END
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:26	FRM_ID	Frame ID	RW
18:16	FRM_WRBK_FMT	Frame WriteBack format. 000：reserved(default) 001：RGB565 010：Reserved 011：YUV422(vy_1uy_0 occupy 32bits, v is at [31:24],y_0 is at [7:0]) 100：8-bits MONO/8-bits Raw RGB 101：8-bits Y 110：RGB888	RW
0	DES_END	1: this descriptor is the last one of the chain; 0: not the last one	RW

LUMI_CFG 6th

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	LUMI_EN	Reserved																													
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	Reserved	Writing has no effect, read as zero.	R
30	LUMI_EN	1: enable 0: disable Note: Luminance size is fixed 9 words.	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

29:0	Reserved	Writing has no effect, read as zero.	R

LUMI_WRBK_ADDR 7th

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LUMI_WRBK_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	LUMI_WRBK_ADDR	Luminance Write Back Buffer address(aligned to word)	RW

SF_WRBK_ADDR 8th

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SF_WRBK_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	SF_WRBK_ADDR	Second field Write Back Buffer head address. When scan mode is 'progressive', these bits can be any value.	RW

8.8 Registers Description

8.8.1 Instructions

Following chapter will descript the functions of all software accessible registers.

Conventions:

9. Register Address = Base + Address offset
10. The registers can be read and written by AHB bus
11. Register read/write attribute
    - ✧ R - Read only
    - ✧ W - Write only
    - ✧ RW - read and write
    - ✧ RCW - read and write, but clear to 0 by read
    - ✧ RSW - read and write, but set to 1 by read
    - ✧ RWC - read and write, clear to 0 by write 1, write 0 has no effect
    - ✧ RWS - read and write, set to 1 by write 1, write 0 has no effect
    - ✧ RC - read only, and clear to 0 by read

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

- ✧ RS - read only, and set to 1 by read
- ✧ SPEC - special access method, relate to its description

12. Reset Value
    - 1 - reset to 1
    - 0 - reset to 0
    - ? - value unknown after reset

8.8.2 Map

The CIM's registers map base address is 0x13060000

The CIM is controlled by a set of registers that the application configures before every operation. The following table lists all the registers.

Table 8-2 CIM Registers Map

Name	Reset Value	Address Offset	Description	RW	Mask
GLB_CFG	0x0000_0001	0x0000	Global configure	RW	0x01FF_FF3F
CROP_SIZE	0x0000_0000	0x0004	Org frame size	RW	0x07FF_07FF
CROP_SITE	0x0000_0000	0x0008	Crop start site	RW	0x07FF_07FF
SCAN_CFG	0x0000_0000	0x0018	Second field configure	RW	0xC000_07FF
DLY_CFG	0x0000_0000	0x001C	Delay configure	RW	0xC3FF_FFFD
QOS_CTRL	0x0000_0000	0x0020	QoS control	RW	0x0000_0007
QOS_CFG	0x0319_0842	0x0024	Priority level configure	RW	0x07FF_FFFF
LUMI_POINT_1	0x0000_0000	0x0028	Divide luminance area point 1	RW	0x07FF_07FF
LUMI_POINT_2	0x0000_0000	0x002C	Divide luminance area point 2	RW	0x07FF_07FF
RGB_COEF	0x0042_8119	0x0030	RGB to y coefficient	RW	0x00FF_FFFF
RGB_BIAS	0x0000_1080	0x0034	RGB to y bias	RW	0x0000_FFFF
DES_ADDR	0x0000_0000	0x1000	Descriptor's head address	RW	0xFFFF_FFFF
CTRL	0x0000_0000	0x2000	control	W	0x0000_001F
ST	0x0000_0000	0x2004	status	R	0x0000_0FFF
CLR_ST	0x0000_0000	0x2008	clear status and interrupt flag	W	0x0000_0FFE
CIM_INTC	0x0000_0000	0x200C	interrupt mask	RW	0x0000_07FE
INT_FLAG	0x0000_0000	0x2010	interrupt flag	R	0x0000_07FE
FRM_ID	0x0000_0000	0x2014	Frame ID	R	0x0000_003F
ACT_SIZE	0x0000_0000	0x2018	Actual size of image	R	0x07FF_07FF
DBG_DES	0x0000_0000	0x3000	descriptor's debug reading	R	0xFFFF_FFFF
DBG_DMA	0x0000_0000	0x3004	WDMA's debug reading	R	0xFFFF_FFFF
DBG_CGC	0x0000_003F	0x3008	Clock gating control	RW	0x0000_003F

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

8.8.3 Registers

8.8.3.1 GLOBAL register

	GLB_CFG																															BASE+0x0000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved							C_ORDER					ORG_FMT				DE_PCLK	DL_VSYNC	DL_HSYNC	EXPO_WIDTH					Reserved		SIZE_CHK	IF_SEL	MODE	BURST_LEN		AUTO_RECOVERY
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Name	Description	RW
31:25	Reserved	Writing has no effect, read as zero.	R
24:20	C_ORDER	Source data's color order 00000：RGB(default) 00001：RBG 00010：GRB 00011：GBR 00100：BRG 00101：BGR 01000：Y_0UY_1V 01001：Y_0VY_1U 01010：UY_0VY_1 01011：VY_0UY_1 10000：RGGB 10001：BGGR 10010：GRBG 10011：GBRG **Note:** when DVP interface, indicate the send order; when IDI interface, indicate the position in the 32bits width bus. For example, when DVP, Y_0UY_1V means the Y_0 send first; when IDI, Y_0UY_1V means the Y_0 at high bits.	RW
19:16	ORG_FMT	The source frame's format. 0000：RGB565(default) 0001：RGB888 0010：YUV422 0011：ITU656 0100：8-bits MONO 0101：10-bits MONO 0110：12-bits MONO 0111：8-bits Raw RGB 1000：10-bits Raw RGB	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		1001：12-bits Raw RGB **Note:** 10/12-bits MONO and 10/12-bits Raw RGB only apply to mipi csi interface	
15	DE_PCLK	default edge of PCLK 0: sample at neg-edge(default) 1: sample at pos-edge	RW
14	DL_VSYNC	default level of VSYNC 0: default level is low, active level is high(default) 1: default level is high, active level is low	RW
13	DL_HSYNC	default level of HSYNC 0: default level is low, active level is high(default) 1: default level is high, active level is low	RW
12:8	EXPO_WIDTH	Pulse width. 00000: 1 hclk Others: Num x 16 hclk	RW
7: 6	Reserved	Writing has no effect, read as zero.	R
5	SIZE_CHK	Whether the actual size of image is less than the expect size. 0: disable(default) 1: enable	RW
4	DAT_IF_SEL	Data Interface select. 0: DVP(default) 1: IDI for CSI	RW
3	MODE	Camera operation mode. 0: normal(default) 1: snapshot	RW
2:1	BURST_LEN	The max length of the write back DMA's burst. 00: 4(default) 01: 8 10: 16 11: 32	RW
0	AUTO_RECOVERY	0: stop immediately; 1: If over-run, or size check error when function enabled, the CIM will drop the current image, then receive the next image to fill the current buffer.(default)	RW

8.8.3.2 Crop size register

	DS_CIM_CROP_SIZE																															BASE+0x0004
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Reserved	crop_Height	Reserved	crop_Width
RST	0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0

Bits	Name	Description	RW
31:27	Reserved	Writing has no effect, read as zero.	R
26:16	crop_Height	frame height after cropping **NOTE:** 1.Configured as the full image's height when no need crop; When interlace mode, it is the first field's height. 2. For 8/10/12-bits Raw RGB format, please set an even.	RW
15:11	Reserved	Writing has no effect, read as zero.	R
10:0	crop_Width	frame width after cropping **NOTE:** 1.Configured as the full image's width when no need crop; 2. For 8/10/12-bits Raw RGB format, please set an even.	RW

8.8.3.3 Crop site register

	DS_CIM_CROP_SITE																															BASE+0x0008
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved					crop_y											Reserved					crop_x										
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:27	Reserved	Writing has no effect, read as zero.	R
26:16	crop_y	The start site of the cropped image(start from 0) **NOTE:** For 8/10/12-bits Raw RGB format, please set an even.	RW
15:11	Reserved	Writing has no effect, read as zero.	R
10:0	crop_x	The start site of the cropped image(start from 0) **NOTE:** For 8/10/12-bits Raw RGB format, please set an even.	RW

8.8.3.4 Scan configure register

	DS_CIM_SCAN_CFG																															BASE+0x0018
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	SCAN_MD	F_ORDER	Reserved																			SF_Height										
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	SCAN_MD	0：progressive(default) 1：interlace **NOTE:** It is used only when ITU656, in other mode, this bit is use-less; when interlace mode, resize and crop function are not supported.	R
30	F_ORDER	Field order. 0: top field first, then bottom field(default) 1: bottom field first, then top field	RW
29:11	Reserved	Writing has no effect, read as zero.	R
10:0	SF_Height	Second field height, used when interlace scan mode.	RW

8.8.3.5 Delay counter register

	DS_CIM_DLY_CFG																														BASE+0x001C	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DLY_EN	DLY_MD	Reserved				DLY_NUM																								Reserved	EXPO_CTRL
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	DLY_EN	0: When continuous descriptor chain, start the next frame operation immediately after the current frame operation done; 1: When continuous descriptor chain, delay DLY_NUM after the current frame operation done, then start the next frame operation.	RW
30	DLY_MD	0: only ensure that delay conditions are met within one consecutive frame burst; 1: not only guarantee the delay condition in the frame burst, but also ensure the delay condition between two burst.	RW
29:26	Reserved	Writing has no effect, read as zero.	R
25:2	DLY_NUM	Interval between two frame operating. When normal mode, unit is one frame time; When snapshot mode, unit is 256 HCLK cycles.	RW
1	Reserved	Writing has no effect, read as zero.	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

0	EXPO_CTRL	Exposure pulse width config. 0:interval between two frame 1:EXPO_WIDTH in GLB_CFG register	RW

8.8.3.6 QOS CTRL register

	DS_CIM_QOS_CTRL																															BASE+0x0020
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																													QOS_VAL		QOS_CTRL
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:3	Reserved	Writing has no effect, read as zero.	R
2:1	QOS_VAL	QoS value set by software.	RW
0	QOS_CTRL	0: The QoS value is controlled by PCFG register; 1: The QoS value is set by QOS_VAL bits	RW

8.8.3.7 QOS configure register

	DS_CIM_QOS_CFG																															BASE+0x0024
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved					TH2									TH1									TH0								
RST	0	0	0	0	0	0	1	1	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0	0	0	1	0

Bits	Name	Description	RW
31:27	Reserved	Writing has no effect, read as zero.	R
26:18	TH2	Threshold2: (TH1+1)~263	RW
17:9	TH1	Threshold1: (TH0+1)~262	RW
8:0	TH0	Threshold0: 0~261	RW

PCFG is used to control the write back rate.

The 3 thresholds cut the output FIFO into 4 spaces. When the entries remained triggering one of them, the priority level will be altered by hardware:

QoS	Space
00	Empty ~ TH0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

01	TH0 ~ TH1
10	TH1 ~ TH2
11	TH2 ~ Full

8.8.3.8 Divude kynubabce area point 1 register

	DS_CIM_LUMI_POINT_1																															BASE+0x00028
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved					Y_OFFSET_1											Reserved					X_OFFSET_1										
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:27	Reserved	Writing has no effect, read as zero.	R
26:16	Y_OFFSET_1	The Y-coordinate of first point that divided the image(start from 0)	RW
15:11	Reserved	Writing has no effect, read as zero.	R
10:0	X_OFFSET_1	The X-coordinate of first point that divided the image(start from 0)	RW

8.8.3.9 Divude kynubabce area point 2 register

	DS_CIM_LUMI_POINT_2																															BASE+0x0002C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved					Y_OFFSET_2											Reserved					X_OFFSET_2										
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:27	Reserved	Writing has no effect, read as zero.	R
26:16	Y_OFFSET_2	The Y-coordinate of second point that divided the image(start from 0)	RW
15:11	Reserved	Writing has no effect, read as zero.	R
10:0	X_OFFSET_2	The X-coordinate of second point that divided the image(start from 0)	RW

8.8.3.10 RGB to y coefficient

	DS_CIM_RGB_TO_Y_COEF																															BASE+0x00030
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Reserved								R_COEF								G_COEF								B_COEF							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:24	Reserved	Writing has no effect, read as zero.	R
23:16	R_COEF	Red coefficient, default value is 66.	RW
15:8	G_COEF	Green coefficient, default value is 129.	RW
7:0	B_COEF	Blue coefficient, default value is 25.	RW

8.8.3.11 RGB to y bias

	DS_CIM_RGB_TO_Y_BIAS																BASE+0x00034															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																BIAS															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	BIAS	RGB convert to y bias, default value is 4224.	RW

RGB565/888 to Y:

(R_COEF * R + G_COEF * G + B_COEF * B + BIAS) >> 8

8.8.3.12 Descriptor address register

	DS_CIM_DES_ADDR																BASE+0x1000															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DES_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DES_ADDR	This is the address of the 1st descriptor before working; After start working, it is the address of the next descriptor. It can be changed by software for descriptor inserting	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		operation. **Note:** the address must aligned to 64bits	

8.8.3.13 Control regsister

	DS_CIM_CTRL																															BASE+0x2000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											DBG_DES_RST	SOFT_RST	GEN_STOP	QCK_STOP	START
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:5	Reserved	Writing has no effect, read as zero.	R
4	DBG_DES_RST	reset the reading point of DEBUG_DES register.	W
3	SOFT_RST	Soft reset	W
2	GEN_STOP	General stop. Assure integrity of the current frame	W
1	QCK_STOP	Quick stop. Stop as quickly as possible, the integrity of the current frame not be guaranteed.	W
0	START	module start	W

8.8.3.14 Status register

	DS_CIM_ST																															BASE+0x2004
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				R_SZ_ERR	R_LAST_ERR	R_LINE_OVER	R_PIX_OVER	SRA	SZ_ERR	EOW	OVER	GSA	SOF	EOF	WORKING
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:12	Reserved	Writing has no effect, read as zero.	R
11	R_SZ_ERR	Raw RGB size error	R
10	R_LAST_ERR	Raw RGB buffer last pixel err	R
9	R_LINE_OVER	Raw RGB line buf overrun	R
8	R_PIX_OVER	Raw RGB buf pixel overrun	R
7	SRA	Soft reset acknowledge	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

6	SZ_ERR	Size check error	R
5	EOW	End of normal work	R
4	OVER	over-run	R
3	GSA	General stop acknowledge	R
2	SOF	Start of frame	R
1	EOF	End of frame	R
0	WORKING	Module is working	R

8.8.3.15 Clear status register

	DC_CLR_ST																															BASE+0x2008
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				CLR_RSZ_ERR	CLR_RLAST_ERR	CLR_RLINE_OVER	CLR_RPIX_OVER	CLR_SRA	CLR_SZ_ERR	CLR_EOW	CLR_OVER	CLR_GSA	CLR_SOF	CLR_EOF	Reserved
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:12	Reserved	Writing has no effect, read as zero.	R
11	CLR_RSZ_ERR	clear R_SZ_ERR	W
10	CLR_RLAST_ERR	clear R_LAST_ERR	W
9	CLR_RLINE_OVER	clear R_LINE_OVER	W
8	CLR_RPIX_OVER	clear R_PIX_OVER	W
7	CLR_SRA	clear SRA	W
6	CLR_SZ_ERR	clear SZ_ERR	W
5	CLR_EOW	clear EOW	W
4	CLR_OVER	clear OVER	W
3	CLR_GSA	clear GSA	W
2	CLR_FRM_START	clear SOF	W
1	CLR_FRM_END	clear EOF	W
0	Reserved	Writing has no effect, read as zero.	R

8.8.3.16 CIM INTC regsiter

	DS_CIM_INTC																															BASE+0x200c
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Reserved																					MSK_RSZ_ERR	MSK_RLAST_ERR	MSK_RLINE_OVER	MSK_RPIX_OVER	MSK_SZ_ERR	MSK_EOW	MSK_OVER	MSK_GSA	MSK_SOF	MSK_EOF	Reserved
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:11	Reserved	Writing has no effect, read as zero.	R
10	MSK_RSZ_ERR	Mask of R_SZ_ERR 0: interrupt is masked 1: generate interrupt	RW
9	MSK_RLAST_ERR	Mask of R_LAST_ERR 0: interrupt is masked 1: generate interrupt	RW
8	MSK_RLINE_OVER	Mask of R_LINE_OVER 0: interrupt is masked 1: generate interrupt	RW
7	MSK_RPIX_OVER	Mask of R_PIX_OVER 0: interrupt is masked 1: generate interrupt	RW
6	MSK _SZ_ERR	Mask of SZ_ERR 0: interrupt is masked 1: generate interrupt	RW
5	MSK _EOW	Mask of EOW 0: interrupt is masked 1: generate interrupt	RW
4	MSK _OVER	Mask of OVER 0: interrupt is masked 1: generate interrupt	RW
3	MSK _GSA	Mask of GSA 0: interrupt is masked 1: generate interrupt	RW
2	MSK _SOF	Mask of SOF 0: interrupt is masked 1: generate interrupt Work together with DES_INTC, only when both are 1 will generate interrupt.	RW
1	MSK _EOF	Mask of EOF 0: interrupt is masked 1: generate interrupt Work together with DES_INTC, only when both are 1 will generate interrupt.	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

0	Reserved	Writing has no effect, read as zero.	R

8.8.3.17 INT flag register

	DS_CIM_INT_FLAG																															BASE+0x2010
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																					INT_RSZ_ERR	INT_RLAST_ERR	INT_RLINE_OVER	INT_RPIX_OVER	INT_SZ_ERR	INT_EOW	INT_OVER	INT_GSA	INT_SOF	INT_EOF	Reserved
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:11	Reserved	Writing has no effect, read as zero.	R
10	INT_RSZ_ERR	interrupt of R_SZ_ERR	R
9	INT_RLAST_ERR	interrupt of R_LAST_ERR	R
8	INT_RLINE_OVER	interrupt of R_LINE_OVER	R
7	INT_RPIX_OVER	interrupt of R_PIX_OVER	R
6	INT_SZ_ERR	interrupt of SZ_ERR	R
5	INT_EOW	interrupt of EOW	R
4	INT_OVER	interrupt of OVER	R
3	INT_GSA	interrupt of GSA	R
2	INT_SOF	interrupt of SOF	R
1	INT_EOF	interrupt of EOF	R
0	Reserved	Writing has no effect, read as zero.	R

8.8.3.18 Frame ID register

	DS_CIM_FRM_ID																															BASE+0x2014
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										FRM_ID					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:6	Reserved	Writing has no effect, read as zero.	R
5:0	FRM_ID	Indicate which frame the EOF belongs to.	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

8.8.3.19 Actual image size register

	DS_CIM_ACT_SIZE																															BASE+0x2018
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved					Act_height											Reserved					Act_width										
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:27	Reserved	Writing has no effect, read as zero.	R
26:16	Act_height	The actual height of the image	R
15:11	Reserved	Writing has no effect, read as zero.	R
10:0	Act_width	The actual width of the image	R

8.8.3.20 Descriptor content register(for debug)

	DS_CIM_DBG_DES																															BASE+0x3000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DBG_DES																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DBG_DES	the content of descriptors	R

8.8.3.21 DMA current address register(for debug)

	DS_CIM_DBG_DMA																															BASE+0x3004
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DBG_DMA_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DBG_DMA_ADDR	WDMA's current operating address	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

8.8.3.22 Clock gating control register(for debug)

	DS_CIM_DBG_CGC																													BASE+0x3008					
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										CGC_REG	CGC_WRBK	CGC_DES	CGC_SCALE	CGC_DVP	CGC_FLOW
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Bits	Name	Description	RW
31:6	Reserved	Writing has no effect, read as zero.	R
5	CGC_REG	0: disable clock gating for com_reg module; 1: enable clock gating for com_reg module.	RW
4	CGC_WRBK	0: disable clock gating for wrbk module; 1: enable clock gating for wrbk module.	RW
3	CGC_DES	0: disable clock gating for des module; 1: enable clock gating for des module.	RW
2	CGC_SCALE	0: disable clock gating for scale module; 1: enable clock gating for scale module.	RW
1	CGC_DVP	0: disable clock gating for dvp module; 1: enable clock gating for dvp module.	RW
0	CGC_FLOW	0: disable clock gating for flow_ctrl module; 1: enable clock gating for flow_ctrl module.	RW

8.9 Operation guide

8.9.1 Configure flow

8.9.1.1 Common flow

- configure **DS_CIM_GLB_CFG, DS_CIM_FRM_SIZE, DS_CIM_CROP_SITE**.
- configure **DS_CIM_SF_CFG** when ITU656 mode(this register could not be configured at other mode)
- configure **DS_CIM_DLY_CFG**(when DLY_EN is 0, DLY_NUM could not be configured)
- configure **DS_CIM_INTC**
- configure **DS_CIM_DES_ADDR**
- write START at **DS_CIM_CTRL**
- wait **EOF**

8.9.1.2 Single frame flow

If the DES_END is 1, the hardware will stop working after 错误!未找到引用源。, and then if write START directly, the hardware will use the NEXT_DES_ADDR, read by last descriptor, as

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

the **DS_CIM_DES_ADDR** to execute the next frame flow(read the descriptor and receive one frame, similarly hereinafter); or can the software configure a new **DS_CIM_DES_ADDR**.

8.9.1.3 Continuous frame flow

If the DES_END is 0, the hardware will start counting the DLY_NUM(if DLY_EN is 1) after **错误!未找到引用源。**, and then execute the next frame flow.

8.9.2 Interlace scan mode

Only used when ITU656 protocol.

Two descriptor are needed, corresponding top and bottom field respectively. They have different WRBK_ADDR and appropriate WRBK_STRD, but the DES_INTC and WRBK_FMT must be the same.

DES_END at the first descriptor must be 0.

8.9.3 Area Luminance

8.9.3.1 Compute Area Luminance

- configure **DS_CIM_GLB_CFG**, **DS_CIM_FRM_SIZE**, **DS_CIM_CROP_SITE**.
- configure **DS_CIM_LUMI_POINT_1, DS_CIM_LUMI_POINT_2**, divide image to 9 areas
- configure **LUMI_WRBK_ADDR** descriptor and **LUMI_EN** bit of **LUMI_CFG** descriptor
- configure **DS_CIM_DLY_CFG**(when DLY_EN is 0, DLY_NUM could not be configured)
- configure **DS_CIM_INTC**
- configure **DS_CIM_DES_ADDR**
- write START at **DS_CIM_CTRL**
- wait **EOF**

8.9.3.2 Luminance output format (Memory)

- Every area luminance occupy 1 word, there have 9 luminance totally.
- Luminance output format (Memory)

Luminance0	Luminance1	Luminance2	Luminance3	Luminance4	Luminance5	Luminance6	Luminance7	Luminance8

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

9 Audio Interface Controller (AIC)

9.1 Overview

This chapter describes the AIC (I2S Controller) included in this processor.

The AIC supports the I2S or IIS (for inter-IC sound), a protocol defined by Philips Semiconductor. Both normal I2S and the MSB-justified I2S formats are supported by AIC.

AIC consists of buffers, status registers, control registers, serializers, and counters for transferring digitized audio between the processor's system memory, an external I2S CODEC. AIC can record digitized audio by storing the samples in system memory. For playback of digitized audio or production of synthesized audio, the AIC retrieves digitized audio samples from system memory and sends them to a CODEC through the serial connection with I2S formats. The internal digital-to-analog converter in the CODEC then converts the audio samples into an analog audio waveform. The audio sample data can be stored to and retrieved from system memory either by the DMA controller or by programmed I/O.

Where both normal I2S and MSB-justified-I2S work with a variety of clock rates, which can be obtained either by dividing the PLL clock by two programmable dividers or from an internal clock source.

9.2 Features

- 16, 20 and 24 bit audio sample data sizes supported, 16 bits packed sample data is supported
- DMA transfer mode supported
- Stop serial clock supported
- Programmable Interrupt function supported
- Support PCM data mono to stereo expansion on audio play back
- Support endian switch on 16-bits normal audio samples play back
- Internal programmable or internal serial clock and optional system clock supported for I2S or MSB-Justified format
- Two FIFOs for transmit and receive respectively.
- One FIFO for transmit loop back.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

9.3 Block Diagram

Figure 9-1 AIC Block Diagram

9.4 Signal Descriptions

There are all 8 pins used to connect between AIC and an external audio CODEC device.

Table 9-1 AIC Pins Description

PIN Name	Function Name	I/O	Description
TX_MCLK	SYS_CLK	O	I2S/MSB-Justified formats, supply system clock to CODEC.
TX_DATA	SDATA_OUT	O	Serial audio output data to CODEC / I2S output.
TX_BCLK	BIT_CLK	I/O	Sample rate dependent bit-rate clock input/output for I2S/MSB-Jistified.
TX_LRCLK	LRSYNC	I/O	Indicates the left- or right-channel for I2S/MSB-Justified format.
RX_MCLK	SYS_CLK	O	I2S/MSB-Justified formats, supply system clock to CODEC.
RX_DATA	SDATA_IN	I	Serial audio input data from CODEC.
RX_BCLK	BIT_CLK_ADC	I/O	Similarly as BIT_CLK, can only be use for ADC channel.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

RX_LRCLK	LRSYNC_ADC	I/O	Similarly as SYNC, can only be use for ADC channel.

9.5 Interface Diagram

Figure 9-2 Master Mode Interface to an External I2S/MSB-Justified CODEC Diagram (Share Clock Mode)

Figure 9-3 Slave Mode Interface to an External I2S/MSB-Justified CODEC Diagram (Share Clock Mode)

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Figure 9-4 Master Mode Interface to an External I2S/MSB-Justified CODEC Diagram (Independent Clock Mode)

Figure 9-5 Slave Mode Interface to an External I2S/MSB-Justified CODEC Diagram (Independent Clock Mode)

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

9.6 Data Format Description

9.6.1 I2S and MSB-justified serial audio format

Normal I2S and MSB-justified are similar protocols for digitized stereo audio transmitted over a serial path.

The BIT_CLK supplies the serial audio bit rate, the basis for the external CODEC bit-sampling logic. Its frequency is 64 times the audio sampling frequency. Divided by 64, the resulting 8 kHz to 48 kHz or even higher signal signifies timing for left and right serial data samples passing on the serial data paths. This left/right signal is sent to the CODEC on the SYNC pin. Each phase of the left/right signal is accompanied by one serial audio data sample on the data pins DAC_SDATA and ADC_SDATA.

Figure 9-6 I2S data format (A: LR mode)

In the A: LR mode, first send the left channel in a stereo frame. One Left slot and one Right slot make a sample frame. It is the normal mode of I2S.

Figure 9-7 I2S data format (B: RL mode)

In the B: RL mode, first send the right channel in a stereo frame. One Right slot and one Left slot make a sample frame. It is used in same CODEC.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Figure 9-8 MSB-justified data format (C: LR mode)

In the C: LR mode, first send the left channel in a stereo frame. One Left slot and one Right slot make a sample frame. It is the normal mode in MSB-justified.

Figure 9-9 MSB-justified data format (D: RL mode)

In the D: RL mode, first send the right channel in a stereo frame. One Right slot and one Left slot make a sample frame.

Data is transmitted and received in frames of 64 BIT_CLK cycles(If BIT_CLK is generated internally). Each frame consists of a left sample and a right sample. Each sample holds 8, 16, 18, 20 or 24 bits of valid data. The LSB other bits of each sample is padded with zeroes.

In the normal I2S mode, the SYNC is low for the left sample and high for the right sample. Also, the MSB of each data sample lags behind the SYNC edges by one BIT_CLK cycle.
In the MSB-justified mode, the SYNC is high for the left sample and low for the right sample. Also, the MSB of each data sample is aligned with the SYNC edges.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

9.6.2 Audio sample data placement in DAC_SDATA/ADC_SDATA

The placement of audio sample in incoming/outgoing serial data stream for all formats support in AIC is MSB (Most Significant Bit) justified. Suppose n bit sample composed by

S_{n-1}	S_{n-2}	…	S_2	S_1	S_0

Following table described the how sample data bits are transferred.

Table 9-2 Sample data bit relate to DAC_SDATA/ADC_SDATA bit

I2S/MSB-Justified Format					
SDATA IN/OUT	**8**	**16**	**18**	**20**	**24**
B31	S7	S15	S17	S19	S23
B30	S6	S14	S16	S18	S22
B29	S5	S13	S15	S17	S21
B28	S4	S12	S14	S16	S20
B27	S3	S11	S13	S15	S19
B26	S2	S10	S12	S14	S18
B25	S1	S9	S11	S13	S17
B24	S0	S8	S10	S12	S16
B23	0	S7	S9	S11	S15
B22	0	S6	S8	S10	S14
B21	0	S5	S7	S9	S13
B20	0	S4	S6	S8	S12
B19	0	S3	S5	S7	S11
B18	0	S2	S4	S6	S10
B17	0	S1	S3	S5	S9
B16	0	S0	S2	S4	S8
B15	0	0	S1	S3	S7
B14	0	0	S0	S2	S6
B13	0	0	0	S1	S5
B12	0	0	0	S0	S4
B11	0	0	0	0	S3
B10	0	0	0	0	S2
B9	0	0	0	0	S1
B8	0	0	0	0	S0
B7~ B0	0	0	0	0	0

If in 16 bits packed mode, the data transferred is the same as the 16 bits normal mode as shown above. But there are two samples in one word.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

9.7 Register Description

Following chapter will describe the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. Register read/write attribute
   R- Read only
   W- Write only
   RW- Read and Write
   RCW- Read and Write, but Clear to 0 by Read
   RSW- Read and Write, but Set to 1 by Read
   RWC- Read and Write, Clear to 0 by Write 1, Write 0 has no effect
   RWS- Read and Write, Set to 1 by Write 1, Write 0 has no effect
   RC- Read only, and Clear to 0 by read
   RS- Read only, and Set to 1 by read
3. Reset Value
   1 - reset to 1
   0 - reset to 0
   ? - value unknown after reset

9.7.1 Register Memory Map

Table 9-3 Registers Memory Map Base Address

Name	Base	Description
AIC	0x10079000	Address base of AIC

The AIC is controlled by a set of registers that the application configures before every operation. The following table lists all the registers.

Table 9-4 AIC Registers Map

Name	RW	Reset Value	Address Offset	Access Size
AICFR	RW	0x0780_0000	0x0000	32
AICCR	RW	0x0124_0000	0x0004	32
I2SCR	RW	0x0000_0000	0x0010	32
AICSR	RW	0x0000_0008	0x0014	32
I2SSR	R	0x0000_0000	0x001C	32
I2SDIV	RW	0x0004_0004	0x0030	32
AICDR	RW	0x0000_0000	0x0034	32
AICLR	R	0x0000_0000	0x0038	32
AICTFLR	RW	0x0000_0008	0x003C	32

– AICFR is used to control FIFO threshold, I2S/MSB-justified selection, AIC reset, master/slave selection

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

- AICCR is used to control DMA mode, FIFO flush, interrupt enable, internal loop-back, play back and recording enable. It also controls sample size and signed/unsigned data transfer.
- I2SCR is used to control BIT_CLK stop, audio sample size, I2S or MSB-justified selection in I2S/MSB-justified.
- AICSR is used to reflect FIFOs status.
- I2SDIV is used to set clock divider for BIT_CLK generating in I2S/MSB-justified format.
- AICDR is act as data input/output port to/from transmit/receive FIFO when write/read..
- AICLR is act as data output port from transmit loop FIFO when read.
- AICTFLR is used to set loop FIFO deepth.

9.7.2 Register and Fields Description

9.7.2.1 AIC Configuration Register (AICFR,0x0000)

AICFR contains bits to control FIFO threshold, I2S/MSB-justified selection, AIC reset, master/slave selection, and AIC enable.

	AICFR																															Base + 0x0000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				RFTH				Reserved			TFTH					Reserved			MSB	Reserved			DMODE	Reserved	LSMP	Reserved	AUSEL	RST	TMASTER	RMASTER	ENB
RST	0	0	0	0	0	1	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:28	Reserved	Writing has no effect, Read as zero.	R
27:24	RFTH	Receive FIFO threshold for interrupt or DMA request. The RFTH valid value is 0 ~ 15. This value represents a threshold value of (RFTH * 2 + 1). When the sample number in receive FIFO, indicated by AICSR.RFL, is great than or equal to the threshold value, AICSR.RFS is set. Larger RFTH value provides lower DMA/interrupt request frequency but have more risk to involve receive FIFO overflow. The optimum value is system dependent.	RW
23:21	Reserved	Writing has no effect, Read as zero.	R
20:16	TFTH	Transmit FIFO threshold for interrupt or DMA request. The TFTH valid value 0 ~ 31. This value represents a threshold value of (TFTH * 2 + 1). When the sample number in transmit FIFO, indicated by AICSR.TFL, is less than or equal to the threshold value, AICSR.TFS is set. Smaller TFTH value provides lower DMA/interrupt request frequency but have more risk to involve transmit FIFO underflow. The optimum value is system	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

<table>
<tr><td></td><td></td><td>dependent.</td><td></td></tr>
<tr><td>15:13</td><td>Reserved</td><td>Writing has no effect, Read as zero.</td><td>R</td></tr>
<tr><td>12</td><td>MSB</td><td>The big-endian format enable. When this bit is '1', the replay data will use the big-endian format. The sign bit at the bit 31. Else the replay data is little-endian format.</td><td>RW</td></tr>
<tr><td>11:9</td><td>Reserved</td><td>Writing has no effect, Read as zero.</td><td>R</td></tr>
<tr><td>8</td><td>DMODE</td><td>Share clock mode(a.k.a 4line-mode)/Independent clock mode(a.k.a 6line-mode).
<table>
<tr><th>DMODE</th><th>master/slave mode</th></tr>
<tr><td>0</td><td>Share clock mode(a.k.a 4line-mode).</td></tr>
<tr><td>1</td><td>Independent clock mode(a.k.a 6line-mode).</td></tr>
</table></td><td>RW</td></tr>
<tr><td>7</td><td>Reserved</td><td>Writing has no effect, Read as zero.</td><td>RW</td></tr>
<tr><td>6</td><td>LSMP</td><td>Select between play last sample or play ZERO sample in TX FIFO underflow. ZERO sample means sample value is zero. This bit is better be changed while audio replay is stopped.
<table>
<tr><th>LSMP</th><th>CODEC used</th></tr>
<tr><td>0</td><td>Play ZERO sample when TX FIFO underflow.</td></tr>
<tr><td>1</td><td>Play last sample when TX FIFO underflow.</td></tr>
</table></td><td>RW</td></tr>
<tr><td>5</td><td>Reserved</td><td>Writing has no effect, Read as zero</td><td>RW</td></tr>
<tr><td>4</td><td>AUSEL</td><td>Audio Unit Select. Change this bit in case of BIT_CLK is stopped (I2SCR.STPBK = 1).
<table>
<tr><th>AUSEL</th><th>Selected</th></tr>
<tr><td>0</td><td>Reserved</td></tr>
<tr><td>1</td><td>Select I2S/MSB-justified format.</td></tr>
</table></td><td>RW</td></tr>
<tr><td>3</td><td>RST</td><td>Reset AIC. Write 1 to this bit reset AIC registers and FIFO except AICFR and I2SDIV register. Writing 0 to this bit has no effect and this bit is always reading 0.</td><td>W</td></tr>
<tr><td>2</td><td>TMASTER</td><td>Playback/Record(used in share clock mode) Master-mode, It is only valid in I2S/MSB-justified format.
<table>
<tr><th>TMASTER</th><th>master/slave mode</th></tr>
<tr><td>0</td><td>AIC as a SLAVE.</td></tr>
<tr><td>1</td><td>AIC as a MASTER.</td></tr>
</table></td><td>RW</td></tr>
<tr><td>1</td><td>RMASTER</td><td>Record(used in independent clock mode) Master-mode, only used at independent clock mode. It is only valid in I2S/MSB-justified format.
<table>
<tr><th>RMATER</th><th>master/slave mode</th></tr>
<tr><td>0</td><td>AIC as a SLAVE.</td></tr>
<tr><td>1</td><td>AIC as a MASTER.</td></tr>
</table></td><td>RW</td></tr>
<tr><td>0</td><td>ENB</td><td>Enable AIC function. This bit is used to enable or disable the AIC function.
<table>
<tr><th>ENB</th><th>Description</th></tr>
<tr><td>0</td><td>Disable AIC Controller.</td></tr>
<tr><td>1</td><td>Enable AIC Controller.</td></tr>
</table></td><td>RW</td></tr>
</table>

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

9.7.2.2 AIC Common Control Register (AICCR,0x0004)

AICCR contains bits to control DMA mode, FIFO flush, interrupt enable, internal loop-back, play back and recording enable. It also controls sample size and signed/unsigned data transfer.

	AICCR																															Base + 0x0004
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ETFLOR	ETFLS	Reserved_0	PACK16	Reserved	CHANNEL			ETFL	TLDMS	OSS			ISS			RDMS	TDMS	MONO_CTR		Reserved	ENDSW	Reserved	TFLUSH	RFLUSH	EROR	ETUR	ERFS	ETFS	ENLBF	ERPL	EREC
RST	0	0	0	0	0	0	0	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	ETFLOR	Enable TFLOR Interrupt. This bit is used to control the TFLOR interrupt enable or disable. **ETFLOR** / **TFLOR Interrupt** 0 / **Disabled.** 1 / **Enabled.**	RW
30	ETFLS	Enable TFLS Interrupt. This bit is used to control the TFLS interrupt enable or disable. **ETFLS** / **TFLS Interrupt** 0 / **Disabled.** 1 / **Enabled.**	RW
29	Reserved	Keep this value to 0 in normal use.	R
28	PACK16	Output Sample data 16bit packed mode select. This bit reflects that one word contains two sample data or only one sample data with LSB align. The packed mode is only support 16bit sample size. **PACK16** / **Sample Size** 0 / Unpacked data mode. One word only contains one 16bit sample data aligned LSB. 1 / Packed data mode. One word contains two 16 bit sample data.	RW
27	Reserved	Writing has no effect., read as zero.	R
26:24	CHANNEL	Output Channel Number Select. These bits reflect output data channels from AIC to device. The data supported are: 1(mono), 2(stereo), 4, 6 and 8 channels. The sample data is LSB-justified in memory/register. **CHANNEL** / **Sample Size** 0x0 / 1 channel, mono mode. 0x1 / 2 channels, stereo mode.	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

<table>
<tr><td></td><td></td><td>0x2 ~ 0x7 | Reserved.</td><td></td></tr>
<tr><td>23</td><td>ETFL</td><td>Enable TFIFO LOOP Function. This bit is used to disable or enable the audio sample data receiving.
<table>
<tr><th>ETFL</th><th>Description</th></tr>
<tr><td>0</td><td>AIC tfifo loop Function is Disabled.</td></tr>
<tr><td>1</td><td>AIC tfifo loop Function is Enabled.</td></tr>
</table></td><td>RW</td></tr>
<tr><td>22</td><td>TLDMS</td><td>Transmit FIFO LOOP DMA enable. This bit is used to enable or disable the DMA during transmit audio data.
<table>
<tr><th>TLDMS</th><th>Transmit fifo loop DMA</th></tr>
<tr><td>0</td><td>Disabled.</td></tr>
<tr><td>1</td><td>Enabled.</td></tr>
</table></td><td>RW</td></tr>
<tr><td>21:19</td><td>OSS</td><td>Output Sample Size. These bits reflect output sample data size from memory or register. The data sizes supported are: 8, 16, 18, 20 and 24 bits. The sample data is LSB-justified in memory/register.
<table>
<tr><th>OSS</th><th>Sample Size</th></tr>
<tr><td>0x0</td><td>8 bit.</td></tr>
<tr><td>0x1</td><td>16 bit.</td></tr>
<tr><td>0x2</td><td>18 bit.</td></tr>
<tr><td>0x3</td><td>20 bit.</td></tr>
<tr><td>0x4</td><td>24 bit.</td></tr>
<tr><td>0x5~0x7</td><td>Reserved.</td></tr>
</table></td><td>RW</td></tr>
<tr><td>18:16</td><td>ISS</td><td>Input Sample Size. These bits reflect input sample data size to memory or register. The data sizes supported are: 8, 16, 18, 20 and 24 bits. The sample data is LSB-justified in memory/register.
<table>
<tr><th>ISS</th><th>Sample Size</th></tr>
<tr><td>0x0</td><td>8 bit.</td></tr>
<tr><td>0x1</td><td>16 bit.</td></tr>
<tr><td>0x2</td><td>18 bit.</td></tr>
<tr><td>0x3</td><td>20 bit.</td></tr>
<tr><td>0x4</td><td>24 bit.</td></tr>
<tr><td>0x5~0x7</td><td>Reserved.</td></tr>
</table></td><td>RW</td></tr>
<tr><td>15</td><td>RDMS</td><td>Receive DMA enable. This bit is used to enable or disable the DMA during receiving audio data.
<table>
<tr><th>RDMS</th><th>Receive DMA</th></tr>
<tr><td>0</td><td>Disabled.</td></tr>
<tr><td>1</td><td>Enabled.</td></tr>
</table></td><td>RW</td></tr>
<tr><td>14</td><td>TDMS</td><td>Transmit DMA enable. This bit is used to enable or disable the DMA during transmit audio data.
<table>
<tr><th>TDMS</th><th>Transmit DMA</th></tr>
<tr><td>0</td><td>Disabled.</td></tr>
<tr><td>1</td><td>Enabled.</td></tr>
</table></td><td>RW</td></tr>
</table>

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

<table>
<tr><td>13:12</td><td>MONOCTR</td><td>MONO CONTROL.
00：Both left and right channel will work in recording；
01：Only right channel will work in recording；
10：Only left channel will work in recording；
11：reserved；</td><td>RW</td></tr>
<tr><td>11</td><td>Reserved</td><td>Writing has no effect., read as zero.</td><td>RW</td></tr>
<tr><td>10</td><td>ENDSW</td><td>Endian Switch. This bit control endian change on outgoing 16-bits size audio sample by swapping high and low bytes in the sample data.
<table>
<tr><th>ENDSW</th><th>Description</th></tr>
<tr><td>0</td><td>No change on outgoing sample data.</td></tr>
<tr><td>1</td><td>Swap high and low byte for outgoing 16-bits size sample data.</td></tr>
</table></td><td>RW</td></tr>
<tr><td>9</td><td>Reserved</td><td>Writing has no effect., read as zero.</td><td>RW</td></tr>
<tr><td>8</td><td>TFLUSH</td><td>Transmit FIFO Flush. Write 1 to this bit flush transmit FIFOs to empty. Writing 0 to this bit has no effect and this bit is always reading 0.</td><td>W</td></tr>
<tr><td>7</td><td>RFLUSH</td><td>Receive FIFO Flush. Write 1 to this bit flush receive FIFOs to empty. Writing 0 to this bit has no effect and this bit is always reading 0.</td><td>W</td></tr>
<tr><td>6</td><td>EROR</td><td>Enable ROR Interrupt. This bit is used to control the ROR interrupt enable or disable.
<table>
<tr><th>EROR</th><th>ROR Interrupt</th></tr>
<tr><td>0</td><td>Disabled.</td></tr>
<tr><td>1</td><td>Enabled.</td></tr>
</table></td><td>RW</td></tr>
<tr><td>5</td><td>ETUR</td><td>Enable TUR Interrupt. This bit is used to control the TUR interrupt enable or disable.
<table>
<tr><th>ETUR</th><th>TUR Interrupt</th></tr>
<tr><td>0</td><td>Disabled.</td></tr>
<tr><td>1</td><td>Enabled.</td></tr>
</table></td><td>RW</td></tr>
<tr><td>4</td><td>ERFS</td><td>Enable RFS Interrupt. This bit is used to control the RFS interrupt enable or disable.
<table>
<tr><th>ERFS</th><th>RFS Interrupt</th></tr>
<tr><td>0</td><td>Disabled.</td></tr>
<tr><td>1</td><td>Enabled.</td></tr>
</table></td><td>RW</td></tr>
<tr><td>3</td><td>ETFS</td><td>Enable TFS Interrupt. This bit is used to control the TFS interrupt enable or disable.
<table>
<tr><th>ETFS</th><th>TFS Interrupt</th></tr>
<tr><td>0</td><td>Disabled.</td></tr>
<tr><td>1</td><td>Enabled.</td></tr>
</table></td><td>RW</td></tr>
<tr><td>2</td><td>ENLBF</td><td>Enable AIC Loop Back Function. This bit is used to enable or disable the internal loop back function of AIC, which is used for test only. When the AIC loop back function is enabled, normal audio replay/record functions are disabled.
<table>
<tr><th>ENLBF</th><th>Description</th></tr>
</table></td><td>RW</td></tr>
</table>

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

			0	AIC Loop Back Function is Disabled.	
			1	AIC Loop Back Function is Enabled.	
1	ERPL	Enable Playing Back function. This bit is used to disable or enable the audio sample data transmitting. **ERPL** / **Description** 0 / **AIC Playing Back Function is Disabled.** 1 / **AIC Playing Back Function is Enabled.**			RW
0	EREC	Enable Recording Function. This bit is used to disable or enable the audio sample data receiving. **EREC** / **Description** 0 / **AIC Recording Function is Disabled.** 1 / **AIC Recording Function is Enabled.**			RW

9.7.2.3 AIC I2S/MSB-justified Control Register (I2SCR,0x0010)

I2SCR contains bits to control BIT_CLK stop, audio sample size, I2S or MSB-justified selection in I2S/MSB-justified. It is valid only in I2S/MSB-justified format.

	I2SCR																															Base + 0x0010
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved														RFIRST	SWLH	Reserved															AMSL
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:18	Reserved	Writing has no effect Read as zero.	R
17	RFIRST	Send R channel first in stereo mode. This bit should only be set in 2 channels configuration. The frame is LR like or RL like. It takes effective immediately when the bit is changed. Change this before replay started. **RFIRST** / **Description** 0 / **Send L channel first. (LR)** 1 / **Send R channel first. (RL)**	RW
16	SWLH	Switch LR channel in 16bit-packed stereo mode. This bit control whether the low address data is L or R. This bit should only be set in 2 channels configuration and 16bit-packed mode. That means it can only valid with packed mode (PACK16 =1) and 2 channels (CHANNEL=0x1). It takes effective immediately when the bit is changed. Change this	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		before replay started. SWLH: 0 — **16 bit LSB and 16bit MSB is not switched.** SWLH: 1 — **16 bit LSB and 16bit MSB is switched.**	
15:1	Reserved	Writing has no effect, Read as zero.	R
0	AMSL	Specify Alternate Mode (I2S or MSB-Justified) Operation. AMSL: 0 — Select I2S Operation Mode. AMSL: 1 — Select MSB-Justified Operation Mode.	RW

9.7.2.4 AIC Controller FIFO Status Register (AICSR,0x0014)

AICSR contains bits to reflect FIFOs status. Most of the bits are read-only except two, which can be written a 0.

	AICSR																															Base + 0x0014
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved		RFL						Reserved			TFLL					Reserved	TFL							Reserved	ROR	TUR	RFS	TFS	TFLOR	TFLS	Reserved
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bits	Name	Description	RW
31:30	Reserved	Writing has no effect, Read as zero.	R
29:24	RFL	Receive FIFO Level. The bits indicate the amount of valid PCM data in Receive FIFO. RFL Value: 0x00 ~ 0x20 — RFL valid PCM data in receive FIFO. RFL Value: 0x21 ~ 0x3F — Reserved.	R
23:21	Reserved	Writing has no effect, read as zero.	R
20:15	TFLL	Transmit FIFO LOOP Level. The bits indicate the amount of valid PCM data in Transmit FIFO LOOP. TFL Value: 0x00 ~ 0x20 — TFL valid PCM data in transmit FIFO LOOP TFL Value: 0x21 ~ 0x3F — Reserved	R
14	Reserved	Writing has no effect, read as zero.	

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

<table>
<tr><td>13:8</td><td>TFL</td><td>Transmit FIFO Level. The bits indicate the amount of valid PCM data in Transmit FIFO.
<table><tr><th>TFL Value</th><th>Description</th></tr><tr><td>0x00 ~ 0x3F</td><td>TFL valid PCM data in transmit FIFO.</td></tr></table></td><td>R</td></tr>
<tr><td>7</td><td>Reserved</td><td>Writing has no effect, Read as zero.</td><td>R</td></tr>
<tr><td>6</td><td>ROR</td><td>Receive FIFO Over Run. This bit indicates that receive FIFO has or has not experienced an overrun.
<table><tr><th>ROR</th><th>Description</th></tr><tr><td rowspan="2">0</td><td>When read, indicates over-run has not been found.</td></tr><tr><td>When write, clear itself.</td></tr><tr><td rowspan="2">1</td><td>When read, indicates data has even been written to full receive FIFO.</td></tr><tr><td>When write, not effects.</td></tr></table></td><td>RW</td></tr>
<tr><td>5</td><td>TUR</td><td>Transmit FIFO Under Run. This bit indicates that transmit FIFO has or has not experienced an under-run.
<table><tr><th>TUR</th><th>Description</th></tr><tr><td rowspan="2">0</td><td>When read, indicates under-run has not been found.</td></tr><tr><td>When write, clear itself.</td></tr><tr><td rowspan="2">1</td><td>When read, indicates data has even been read from empty transmit FIFO.</td></tr><tr><td>When write, not effects.</td></tr></table></td><td>RW</td></tr>
<tr><td>4</td><td>RFS</td><td>Receive FIFO Service Request. This bit indicates that receive FIFO level is or not below receive FIFO threshold, which is controlled by AICFR.RFTH. When RFS is 1, it may trigger interrupt or DMA request depends on the interrupt enable and DMA setting.
<table><tr><th>RFS</th><th>Description</th></tr><tr><td>0</td><td>Receive FIFO level below RFL threshold.</td></tr><tr><td>1</td><td>Receive FIFO level at or above RFL threshold.</td></tr></table></td><td>R</td></tr>
<tr><td>3</td><td>TFS</td><td>Transmit FIFO Service Request. This bit indicates that transmit FIFO level is below Transmit FIFO threshold, which is controlled by AICFR.TFTH. When TFS is 1, it may trigger interrupt or DMA request depends on the interrupt enable and DMA setting.
<table><tr><th>TFS</th><th>Description</th></tr><tr><td>0</td><td>Transmit FIFO level exceeds TFL threshold.</td></tr><tr><td>1</td><td>Transmit FIFO level at or below TFL threshold.</td></tr></table></td><td>R</td></tr>
<tr><td>2</td><td>TFLOR</td><td>Transmit FIFO LOOP over Run. This bit indicates that transmit FIFO LOOP has or has not experienced an over-run.
<table><tr><th>TFLOR</th><th>Description</th></tr><tr><td rowspan="2">0</td><td>When read, indicates over-run has not been found.</td></tr><tr><td>When write, clear itself.</td></tr><tr><td>1</td><td>When read, indicates data has even been read from empty transmit FIFO LOOP.</td></tr></table></td><td>RW</td></tr>
</table>

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		When write, not effects.	
1	TFLS	Transmit FIFO LOOP Service Request. This bit indicates that receive FIFO level is or not below receive FIFO threshold, which is controlled by AICFR.TFFL. When TFLS is 1, it may trigger interrupt or DMA request depends on the interrupt enable and DMA setting. **RFS** / **Description** 0: Transmit FIFO level below RFL threshold. 1: Transmit FIFO LOOP level at or above TFLS threshold.	R
0	Reserved	Writing has no effect, Read as zero.	R

9.7.2.5 AIC I2S/MSB-justified Status Register (I2SSR,0x001C)

I2SSR is used to reflect AIC status in I2S/MSB-justified. It is a read-only register.

	I2SSR																																Base+0x001C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										CHBSY	TBSY	RBSY	BSY	Reserved	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:6	Reserved	Writing has no effect, Read as zero.	R
5	CHBSY	AIC Transmitter busy in I2S/MSB-justified format.(Multi-channel status) **CHBSY** / **Description** 0: AIC Transmitter part is idle or disabled. 1: AIC Transmitter part currently is transmitting or receiving a frame.	R
4	TBSY	AIC Transmitter busy in I2S/MSB-justified format. **TBSY** / **Description** 0: AIC Transmitter part is idle or disabled. 1: AIC Transmitter part currently is transmitting or receiving a frame.	R
3	RBSY	AIC Receiver busy in I2S/MSB-justified format. **RBSY** / **Description** 0: AIC Receiver part is idle or disabled. 1: AIC Receiver part currently is transmitting or receiving a frame.	R
2	BSY	AIC busy in I2S/MSB-justified format.	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		BSY	**Description**	
		0	AIC controller is idle or disabled.	
		1	AIC controller currently is transmitting or receiving a frame.	
1:0	Reserved	Writing has no effect, Read as zero.		R

9.7.2.6 AIC I2S/MSB-justified Clock Divider Register (I2SDIV,0x0030)

I2SDIV is used to set a EVEN-NUMBER clock divider to generated BIT_CLK from SYS_CLK in I2S/MSB-justified format.

	I2SDIV																															**Base + 0x0030**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved							RDIV																TDIV								
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	**Name**	**Description**	**RW**
31:25	Reserved	Writing has no effect, Read as zero.	R
24:16	RDIV	Audio Receiver BIT_CLK clock divider value which is a EVEN-number. The ODD-number value will be floor to EVEN-number value. The frequency relationship of SYS_CLK, BIT_CLK, and LRSYNC(the frequency equal audio sample frequency) are: $f_{LRSYNC} = f_{sample}$ $f_{BIT_CLK} = 64 \times f_{LRSYNC}$ f_{SYS_CLK} = (I2SDIV.RDIV – mod(I2SDIV.RDIV, 2)) × f_{BIT_CLK} Please reference to 9.8.8.	RW
15:9	Reserved	Writing has no effect, Read as zero.	R
8:0	TDIV	Audio Transmitter BIT_CLK clock divider value which is a EVEN-number. The ODD-number value will be floor to EVEN-number value. The frequency relationship of SYS_CLK, BIT_CLK, and LRSYNC(the frequency equal audio sample frequency) are: $f_{LRSYNC} = f_{sample}$ $f_{BIT_CLK} = 64 \times f_{LRSYNC}$ f_{SYS_CLK} = (I2SDIV.TDIV – mod(I2SDIV.TDIV, 2)) × f_{BIT_CLK} Please reference to 9.8.8.	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

9.7.2.7 AIC FIFO Data Port Register (AICDR,0x0034)

AICDR is act as data input port to transmit FIFO when write and data output port from receive FIFO when read, one audio sample every time. The FIFO width is 24 bits. Audio sample with size N that is less than 24 is located in LSB N-bits. The sample size is specified by I2SCR.WL in I2S/MSB-justified. In I2S/MSB-justified, the left channel sample is prior to the right channel sample.

Care should be taken to monitor the status register to insure that there is room for data in the FIFO when executing a program read or write transaction. This is taken care automatically in DMA.

	AICDR																															Base + 0x0034
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								DATA																							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:24	Reserved	Writing has no effect, Read as zero.	R
23:0	DATA	FIFO port. When write to it, data is push to the transmit FIFO. When read from it, data is pop from the receiving FIFO.	RW

9.7.2.8 AIC Loop Data Register (AICLR,0x0038)

	AICLR																															Base + 0x0038
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								DATALP																							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:24	Reserved	Writing has no effect, Read as zero.	R
23:0	DATALP	FIFO port.When read from it, data is pop from the TFIFO_LOOP.	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

9.7.2.9 AIC TFIFO LOOP Register (AICTFLR,0x003C)

	AICTFLR																															Base + 0x003C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												TFLTH			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bits	Name	Description	RW
31:4	Reserved	Writing has no effect, read as zero.	R
3:0	TFLTH	TFIFO LOOP threshold for interrupt or DMA request. The TFLTH valid value is 0 ~ 15. This value represents a threshold value of (TFLTH * 2 + 1). When the sample number in receive FIFO, indicated by AICSR.RFL, is great than or equal to the threshold value, AICSR.TFLS is set. Larger TFLTH value provides lower DMA/interrupt request frequency but have more risk to involve TFIFO LOOP overflow. The optimum value is system dependent.	RW

9.8 Operation Flow

The AIC can be accessed either by the processor using programmed I/O instructions or by the DMA controller. The processor uses programmed I/O instructions to access the AIC and can access the following types of data.

- **The AIC memory mapped registers data**—All registers are 32 bits wide and are aligned to word boundaries.
- **AIC controller FIFO data—**An entry is placed into the transmit FIFO by writing to the I2S controller's Serial Audio Data register (AICDR). Writing to AICDR updates a transmit FIFO entry. Reading AICDR flushes out a receive FIFO entry.
- **The external CODEC registers for I2S CODEC—**CODEC registers can be accessed through the L3 bus. The L3 bus operation is emulated by software controlling three GPIO pins.

The DMA controller can only access the FIFOs. Accesses are made through the data registers, as explained in the previous paragraph. The DMA controller responds to the following DMA requests made by the I2S controller:

- The transmit FIFO request is based on the transmit trigger-threshold (AICFR.TFTH) setting. See 9.7.2.1 for further details regarding AICFR.TFTH.
- The receive FIFO request is based on the receive trigger-threshold (AICFR.RFTH) setting. See 9.7.2.1 for further details regarding AICFR.RFTH.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

9.8.1 Initialization

At power-on or other hardware reset (WDT and etc), AIC is disabled. Software must initiate AIC and the external CODEC after power-on or reset. If errors found in data transferring, or in other places, software must initial AIC and optional, the external CODEC. Here is the initial flow.

1. If I2S/MSB-Justified is selected, select between I2S and MSB-Justified (I2SCR.AMSL).
2. Decide master mode / slave mode direction (AICFR.TMASTER/AICFR.RMASTER).
3. If BIT_CLK is configured as output, BIT_CLK divider I2SDIV.DV must be set to what correspond with the values as shown in 9.7.2.6. And the clock selection and the divider between PLL clock out and AIC also must be set (CFCR.I2S and I2SCDR in CPM). Enable AIC by write 1 to AICFR.ENB.
4. If it needs to reset AIC registers and flush FIFOs, write 1 to AICFR.RST. If it need only flush FIFOs, write 1 to AICCR.FLUSH. BIT_CLK must exist here and after.
5. In case of internal CODEC with I2S/MSB-Justified format, configure I2S/MSB-justified CODEC via the control bus connected to the CODEC, for instance I2C or L3, depends on CODEC. If the resettlement without involving I2S/MSB-justified CODEC or ADC/DAC function changing, this step can be skip.

9.8.2 External CODEC Registers Access Operation

The external audio CODEC can be configured/controlled by its internal registers. To access these registers, an I2S/MSB-justified CODEC usually employs L3 bus, SPI bus, I2C bus or other control bus. The L3 bus operation can be emulated by software by using 3 GPIO pins of the chip.

9.8.3 Audio Replay

Outgoing audio sample data (from AIC to CODEC) is written to AIC transmit FIFO from processor via store instruction or from memory via DMA. AIC then takes the data from the FIFO, serializes it, and sends it over the serial wire DAC_SDATA to an external CODEC.

The audio transmission is enabled automatically when the AIC is enabled by set AICFR.ENB. But all replay data is zero at this time except both of the following conditions are true:

1. AICCR.ERPL must be 1. If AICCR.ERPL is 0, value of zero is send to CODEC even if there are samples in transmit FIFO.
2. At least one audio sample data in the transmit FIFO. If the transmit FIFO is empty, value of zero or last sample depends on AICFR.LSMP, is send to CODEC even if AICCR.ERPL is 1.

Here is the audio replay flow:

1. Configure the CODEC as needed.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

2 Configure sample size by AICCR.OSS.
3 Configure sample channels (AICCR.CHANNEL).
4 If sample size is configured 16 bit, select packed or unpacked mode (AICCR.PACK16).
5 If two channels is configured, select the right-channel-first sample data or not (I2SCR.RFIRST).
6 If two channels is configured, select the sample data switched or not (I2SCR.SWLH).
7 Configure sample rate by clock dividers (for I2S/MSB-Justified format with BIT_CLK is provided internally) or by CODEC registers (for BIT_CLK provided by internal CODEC).
8 Some other configurations: mono to stereo, endian switch, signed/unsigned data transfer, transmit FIFO configuration, play ZERO or last sample when TX FIFO under-run, and etc.
9 Write 1 to AICCR.ERPL.
It is suggested that at least a frame of PCM data is pre-filled in the transmit FIFO to prevent FIFO under-run flag (AICSR.TUR).
Fill sample data to the transmit FIFO. Repeat this till finish all sample data. In this procedure, please control the FIFO to make sure no FIFO under-run and other errors happen. When the transmit FIFO under-run, noise or pause may be heard in the audio replay, AICSR.TUR is 1, and if AICCR.ETUR is 1, AIC issues an interrupt. Please reference to 9.8.5 for detail description on FIFO.
10 Waiting for AICSR.TFL change to 0. So that all samples in the transmit FIFO has been replayed, then we can have a clean start up next time.
11 Write 0 to AICCR.ERPL.

9.8.4 Audio Record

Incoming audio sample data (from CODEC to AIC) is received from ADC_SDATA (for an external CODEC) serially and converted to parallel word and stored in AIC receive FIFO. Then the data can be taken from the FIFO to processor via load instruction or to memory via DMA.

The audio recording is enabled automatically when the AIC is enabled by set AICFR.ENB. But all received data is discarded at this time except both of the following conditions are true:

1 AICCR.EREC must be 1. If AICCR.EREC is 0, the received data is discarded even if there are rooms in the receive FIFO.
2 At least one room left in the receive FIFO. If the receive FIFO is full, the received data is discarded even if AICCR.EREC is 1.

Here is the audio record flow:

1 Configure the CODEC as needed.
2 Configure sample size by AICCR.ISS.
3 Configure sample rate by clock dividers (for I2S/MSB-Justified format with BIT_CLK is provided internally) or by CODEC registers (for BIT_CLK provided by internal

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

CODEC).

4 Some other configurations: signed/unsigned data transfer, receive FIFO configuration, and etc.

5 Write 1 to AICCR.EREC. Make sure there are rooms available in the receive FIFO before set AICCR.EREC. Usually, it should empty the receive FIFO by fetch data from it before set AICCR.EREC.

6 Take sample data form the receive FIFO. Repeat this till the audio finished. In this procedure, please control the FIFO to make sure no FIFO over-run and other errors happen. When the receive FIFO over-run, same recorded audio samples will be lost, AICSR.ROR is 1, and if AICCR.EROR is 1, AIC issues an interrupt. Please reference to 9.8.5 for detail description on FIFO. Write 0 to AICCR.EREC.

7 Take sample data from the receive FIFO until AICSR.RFL change to 0. So that all samples in the receive FIFO has been taken away, then we can have a clean start up next time. When the receive FIFO is empty, read from it returns zero.

9.8.5 FIFOs operation

AIC has two FIFOs, one for transmit audio sample and one for receive. All AIC played/recorded audio sample data is taken from/send to transmit/receive FIFOs. The RX FIFO is in 24 bits width and 32 entries depth, one entry for keeping one audio sample regardless of the sample size. The RX FIFO is in 32 bits width and 64 entries depth, one entry for keeping one audio sample regardless of the sample size, but in 16 bits packed mode, one entry for keeping two audio samples. AICDR.DATA provides the access point for processor/DMA to write to transmit FIFO and read from receive FIFO. One time access to AICDR.DATA process one sample. The sample data should be put in LSB (Least Significant Bit) in memory or processor registers. For transmitting, bits exceed sample are discarded. For receiving, these bits are set to 0. Figure 9-10 illustrates the FIFOs access.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Figure 9-10 Transmitting/Receiving FIFO access via APB Bus

The software and bus initiator must guarantee the right sample placement at the bus.

In case of DMA bus initiator, one 24, 20, 18 bits audio sample must occupies one 32-bits word in memory, so 32-bits width DMA must be used. One 16 bits sample occupies one 16-bits half word in memory, so 16-bits width DMA must be used. One 8-bits sample occupies one byte in memory, and use 8-bits width DMA except 16bits packed mode. If in 16 bits packed mode, Two 16 bits sample occupies one 32-bits word in memory, so 32-bits width DMA must be used.

In case of processor bus initiator, any type of the audio sample must occupy one CPU general-purpose register at LSB, and read/write from/to AICDR.DATA with 32-bits load/store instruction. When process small sample size, 16-bits or 8-bits, software may need to do the data pack/unpack except 16 bits packed mode. In the 16bits packed mode, the sample data is packed, and two 16 bits audio samples occupy one CPU general-purpose register.

The AICFR.TFTH and AICFR.RFTH are used to set the FIFO level thresholds, which are the trig levels of DMA request and/or FIFO service interrupt. The AICFR.TFTH and AICFR.RFTH should be set to proper value; too small or too big are not good. When AICFR.RFTH is too small, or AICFR.TFTH is too big, the DMA burst length or the number of sample can be processed by processor is too small, which harms the bus or processor efficiency. When AICFR.RFTH is too big or AICFR.TFTH is too small, the bus or the interrupt latency left for

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

under-run/over-run is too small, which may causes replay/record errors.

AICSR.TUR is set to 1 during transmit under-run conditions. If AICCR.ETUR is 1, this can trigger an interrupt. During transmit under-run conditions, zero or last sample is continuously sent out across the serial link. Transmit under-run can occur under the following conditions:

1. Valid transmit data is still available in memory, but the DMA controller/processor starves the transmit FIFO, as it is busy servicing other higher-priority tasks.
2. The DMA controller/processor has transferred all valid data from memory to the transmit FIFO.

AICSR.ROR is set to 1 during receive over-run conditions. If AICCR.EROR is 1, this can trigger an interrupt. During receive over-run conditions, data sent by the CODEC is lost and is not recorded.

When replay/record two channels data, the left channel is default the first data in FIFOs and in the serial link. In 16bits packed mode, could configure that the left channel is the first data or the right channel. By default, the 16 bits LSB is left channel, 16 bits MSB is the right channel. But it also could be switched the Left or the Right channel (I2SCR.SWLH).

9.8.6 Data Flow Control

There are three approaches provided to control/synchronize the audio incoming/outgoing data flow.

9.8.6.1 Polling and Processor Access

AICSR.RFL and AICSR.TFL reflect how many samples exist in receiving and transmitting FIFOs. Through read these register fields, processor can detect when there are samples in receiving FIFO in audio record and then load them from the RX-FIFO, and when there are rooms in transmitting FIFO in audio replay and then store samples to the TX-FIFO.

Polling approach is in very low efficiency and is not recommended.

9.8.6.2 Interrupt and Processor Access

Set proper values to AICFR.TFTH and AICFR.RFTH, the FIFO interrupts trig thresholds. Set AICCR.ETFS and/or AICCR.ERFS to 1 to enable transmitting and/or receiving FIFO level trigger interrupts. When the interrupt found, it means there are rooms or samples in the TX or RX FIFO, and processor can store or load samples to or from the FIFO.
Interrupt approach is more efficient than polling approach.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

9.8.6.3 DMA Access

Audio data is real time stream, though it is in low data bandwidth, usually less than 1.2Mbps. DMA approach is the most efficient and is the recommended approach.

To enable DMA operation, set AICCR.TDMS and AICCR.RDMS to 1 for transmit and receive respectively. It also needs to allocate two channels in DMA controller for data transmitting and receiving respectively. Please reference to the processor's DMA controller spec for the details. The AICFR.TFTH and AICFR.RFTH are used to set the transmitting and receiving FIFO level thresholds, which determine the issuing of DMA request to DMA controller. To respond the request, DMAC initiator and controls the data movement between memory and TX/RX FIFO.

9.8.7 Audio Samples format

9.8.7.1 16 bits packed mode

One channel (mono) mode and two channels (stereo) mode:

Figure 9-11 One channel (Left) and Two channels (right) mode (16 bits packed mode)

Four channels mode and six channels mode:

Figure 9-12 Four channels (Left) and Six channels (right) mode (16 bits packed mode)

Eight channels mode:

Figure 9-13 Eight channels mode (16 bits packed mode)

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

9.8.7.2 Normal mode.

One channel (Mono) and two channels (stereo) mode:

Figure 9-14 One channel (Left) and Two channels (right) mode

Four channels mode and six channels mode:

Figure 9-15 Four channels (Left) and Six channels (right) mode

Eight channel mode:

Figure 9-16 Eight channels mode

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

9.8.8 Serial Audio Clocks and Sampling Frequencies

Following are for BIT_CLK/SYS_CLK configuration in I2S/MSB-Justified format with external CODEC.

The BIT_CLK is the rate at which audio data bits enter or leave the AIC. BIT_CLK can be supplied either by the CODEC or an internally PLL. If it is supplied internally, BIT_CLK is configured as output pins, and is supplied out to the CODEC. If BIT_CLK is supplied by the CODEC, then it is configured as an input pin. Register bit AICFR.BCKD is used to select BIT_CLK direction.

The audio sampling frequency is the frequency of the SYNC signal, which must be 1/64 of BIT_CLK, $f_{BIT_CLK} = 64\ f_S$.
SYS_CLK is only for CODEC. It usually takes one of the two roles, as CODEC master clock input or as CODEC over-sampling clock input. If SYS_CLK roles as CODEC master clock input, it usually should be set to a fixed frequency according to CODEC requirement but independent to audio sample rate. In this case, usually there is a PLL in the CODEC and CODEC roles master mode. See Figure 9-2 for the interface diagram. This is the recommended AIC CODEC system configuration.

If SYS_CLK roles as CODEC over-sampling clock, its frequency is usually 4, 6, 8 or 12 times of BIT_CLK frequency, which are 256, 384, 512 and 768 times of audio sample rates. Following table lists the relation between sample rate, BIT_CLK and SYS_CLK frequencies.

Table 9-5 Audio Sampling rate, BIT_CLK and SYS_CLK frequencies

Sample Rate f_S (kHz)	BIT_CLK (MHz) $f_{BIT_CLK} = 64\ f_S$	SYS_CLK (MHz)			
		256 f_S	**384 f_S**	**512 f_S**	**768 f_S**
48	3.072	12.288	18.432	24.576	36.864
44.1	2.8224	11.2896	16.9344	22.5792	33.8688
32	2.048	8.192	12.288	16.384	24.576
24	1.536	6.144	9.216	12.288	18.432
22.05	1.4112	5.6448	8.4672	11.2896	16.9344
16	1.024	4.096	6.144	8.192	12.288
11.025	0.7056	2.8224	4.2336	5.6448	8.4672
8	0.512	2.048	3.072	4.096	6.144

In this processor, SYS_CLK can be selected from EXCLK or generated by dividing the PLL output clock in a CPM divider controlled by I2SCDR. If BIT_CLK is chosen as an output, another divider in AIC is used to divide SYS_CLK for it.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Figure 9-17 SYS_CLK, BIT_CLK generation scheme

Note: SCLK_A and SCLK_M please refer to CPM.

The setting of I2SDIV.DV is shown in Table 9-6

Table 9-6 BIT_CLK divider setting

I2SDIV.DV	f_{SYS_CLK}	f_{BIT_CLK}	f_{SYS_CLK} / f_{BIT_CLK}
0x0	64fs	64fs	1
0x1	128 f_S	64 f_S	2
0x2	196 f_S	64 f_S	3
0x3	256 f_S	64 f_S	4
0x5	384 f_S	64 f_S	6
0x7	512 f_S	64 f_S	8
0xB	768 f_S	64 f_S	12

As we observe in Table 9-5, if SYS_CLK is taken as over-sampling clock by CODEC, the common multiple of all SYS_CLK frequencies is much bigger than the PLL output clock frequency. To generate all different SYS_CLK frequencies, one approach is change PLL frequency according to sample rate. This is not realistic, since frequently change PLL frequency during normal operation is not recommended.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Another approach is to found some approximate common multiples of all SYS_CLK frequencies according to the fact that there tolerance in audio sample rate. Take f_{SYS_CLK} = 256 f_S, Table 9-7 list most frequencies, which are less than 400MHz, with relatively small sample rate errors. It is suggested to set PLL frequency as close to the frequencies listed as possible, then use clock dividers to generate different SYS_CLK/BIT_CLK for different sample rate.

Table 9-7 Approximate common multiple of SYS_CLK for all sample rates

Approximate Common Frequency (MHz)	Max Error Caused in Audio Sample Rate (%)
123.53	0.53
147.11	0.24
170.68	0.79
235.5	0.87
247.06	0.53
270.64	0.11
280.56	0.73
294.22	0.24
305.14	0.67
317.79	0.53
329.57	0.66
341.35	0.79
347	0.85
353.13	0.90
358.79	0.69
370.59	0.53
382.96	0.54
394.17	0.24

Take PLL = 270.64 MHz as an example, Table 9-8 lists the divider settings for various sample rates.

Table 9-8 CPM/AIC clock divider setting for various sampling rate if PLL = 270.64MHz

Sample Rate (kHz)	I2SCDR	I2SDIV.DV	Sample Rate Error (%)
48	1	11	0.11
44.1	1	12	-0.11
32	0	33	0.11
24	1	22	0.11
22.05	1	24	-0.11
16	1	33	0.11
12	1	44	0.11
11.025	1	48	-0.11
8	1	66	0.11

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

For an EXCLK clock frequency, try to generate PLL frequencies as close to the frequencies listed in Table 9-9 as possible. Table 9-9 lists the PLL parameters and audio sample errors at different PLL frequencies for EXCLK at 12MHz.

Table 9-9 PLL parameters and audio sample errors for EXCLK=12MHz

PLL			Max Sample Rate Error
M	N	Freq (MHz)	
103	10	123.6	0.59%
49	4	147	0.31%
128	9	170.67	0.79%
157	8	235.5	0.87%
103	5	247.2	0.59%
65	3	260	0.82%
45	2	270	0.35%
203	9	270.67	0.12%
113	5	271.2	0.32%
187	8	280.5	0.75%
237	10	284.4	0.81%
49	2	294	0.31%
178	7	305.14	0.67%
53	2	318	0.60%
302	11	329.45	0.70%
256	9	341.33	0.79%
318	11	346.91	0.88%
206	7	353.14	0.90%
299	10	358.8	0.69%
247	8	370.5	0.55%
351	11	382.91	0.55%
230	7	394.29	0.27%

The BIT_CLK should be stopped temporary when change the divider settings, or when change BIT_CLK source (from external), to prevent clock glitch. Register I2SCR.STPBK is provided to assist the task. When I2SCR.STPBK = 1, BIT_CLK is disabled no matter whether it is generated internally or inputted from the external source. The operation flow is described in following.

1. Stop all replay/record by clear AICCR.ERPL and AICCR.EREC.
2. Polling I2SSR.BSY till it is 0.
3. Stop the BIT_CLK by write 1 to I2SCR.STPBK.
4. Operations concerning BIT_CLK.
5. Resume the BIT_CLK by write 0 to I2SCR.STPBK.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

9.8.9 Interrupts

The following status bits, if enabled, interrupt the processor:

- Transmit FIFO Service (AICSR.TFS). It's also DMA Request.
- Receive FIFO Service (AICSR.RFS). It's also DMA Request.
- Transmit loop FIFO Service(AICSR.TFLS). It's also DMA Request.
- Transmit Under-Run (AICSR.TUR).
- Receive Over-Run (AICSR.ROR).
- Transmi Loop Over-Run(AICSR.TFLOR)

For further details, see the corresponding register description sections.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

10 Display Controller

10.1 Features

- Support input format: RGB888, RGB565, RGB555.
- Support frame size up to 720p
- Support Display interface types:
  - MIPI-DBI(SLCD)
    - Support Type A(6800)、Type B(8080), 8-/9-/16-/18-/24-bit bus
    - Support Type C(Serial data transfer interface, 3/4line-spi, 8-/12-/16-/24-bit bus)
  - MIPI-DPI(TFT)
    - Support 24bit/pixel(R:8bit, G:8bit, B:8bit)
    - Support 18bit/pixel(R:6bit, G:6bit, B:6bit)
    - Support 16bit/pixel(R:5bit, G:6bit, B:5bit)
- Support 720P@60hz

10.2 Architecture map

Figure 10-1 Top architecture

10.3 Data Format Description

10.3.1 Source data define (the format of source data in DDR memory)

RGB888

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

RGB565

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

RGB555

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Note: These are examples, the color orders can be changed.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

10.3.2 SLCD output pin define

8bpp (565)：

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																R7	R6	R5	R4	R3	G7	G6	G5
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																G4	G3	G2	B7	B6	B5	B4	B3

8bpp (888):

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																R7	R6	R5	R4	R3	R2	R1	R0
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																G7	G6	G5	G4	G3	G2	G1	G0
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																B7	B6	B5	B4	B3	B2	B1	B0

9bpp(666):

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
															R7	R6	R5	R4	R3	R2	G7	G6	G5
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
															G4	G3	G2	B7	B6	B5	B4	B3	B2

16bpp(565):

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								R7	R6	R5	R4	R3	G7	G6	G5	G4	G3	G2	B7	B6	B5	B4	B3

1bpp(SPI mode)

The data will be transferred by D0 pin.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

10.3.3 GPIO Pads relation

For LCD:

- RGB888: R,G,B align from high to low in lower 24 GPIO Pads
- RGB666: R,G,B align from high to low in lower 18 GPIO Pads
- RGB565: R,G,B align from high to low in lower 16 GPIO Pads

For SLCD:

- RGB565: R,G,B align from high to low in lower 16 GPIO Pads
- RGB565 but with 8bits data width: B,G,R in orders go through 8 GPIO Pads

10.4 Descriptor definition

10.4.1 Simple read DMA(SRD) Configure descriptor definition

Num	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	RdmaNextCfgAddr																															
1	FrameBufferAddr																															
2																				Stride												
3										Format				Color																		CHAIN_END
4															EOD_MSK															SOS_MSK	EOS_MSK	

Num	Bits	Name	Description
0	31:0	RdmaNextCfg Addr	Simple read DMA 's next descriptor address
1	31:0	FrameBuffer Addr	The head address of the frame buffer in DDR memory.
2	12:0	Stride	Support 4k(4096)(Unit: pixel). The value must not be less than the width of the frame.
3	22:19	Format	Format of **source** data 0000:RGB555 0010:RGB565 0100:RGB888 others:reserved
	18:16	Color	Color of source data in memory 000:RGB→RGB 001:RBG→RGB 010:GRB→RGB 011:GBR→RGB

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

			100:BRG→RGB 101:BGR→RGB The module will transform these colors to RGB, which will be used for output to display module directly.
	0	CHAIN_END	1: this descriptor is the last one of the chain; 0: not the last one
4	17	EOD_MSK	mask of DISP_END 1: generate interrupt 0: interrupt is masked
	2	SOS_MSK	mask of SRD_START 1: generate interrupt 0: interrupt is masked
	1	EOS_MSK	mask of SRD_END 1: generate interrupt 0: interrupt is masked

10.5 Registers Description

10.5.1 Instructions

Following chapter will descript the functions of all software accessible registers.

Conventions:

13. Register Address = Base + Address offset
14. The registers can be read and written by AHB0 bus.
15. Register read/write attribute
    - ✧ R - Read only
    - ✧ W - Write only
    - ✧ RW - read and write
    - ✧ RCW - read and write, but clear to 0 by read
    - ✧ RSW - read and write, but set to 1 by read
    - ✧ RWC - read and write, clear to 0 by write 1, write 0 has no effect
    - ✧ RWS - read and write, set to 1 by write 1, write 0 has no effect
    - ✧ RC - read only, and clear to 0 by read
    - ✧ RS - read only, and set to 1 by read
    - ✧ SPEC - special access method, relate to its description
16. Reset Value
    - – 1 - reset to 1
    - – 0 - reset to 0
    - – ? - value unknown after reset

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

10.5.2 Map

The DC's registers map base address is 0x13050000.

The DC is controlled by a set of registers that the application configures before every operation. The following table lists all the registers.

Table 10-1DC Registers Map

Name	Reset Value	Address Offset	Description	RW
DC_SRD_CHAIN_ADDR	0x0000_0000	0x1000	RDMA descriptor's address	RW
DC_SRD_CHAIN_CTRL	0x0000_0000	0x1004	RDMA descriptor's control	W
DC_CTRL	0x0000_0000	0x2000	DC control	W
DC_ST	0x0000_0000	0x2004	DC status	R
DC_CLR_ST	0x0000_0000	0x2008	DC clear status	W
DC_INTC	0x0000_0000	0x200C	DC interrupt mask	RW
DC_INT_FLAG	0x0000_0000	0x2010	DC interrupt flag	R
DC_COM_CONFIG	0x0000_0000	0x2014	DC common config	RW
DC_PCFG_RD_CTRL	0x0000_0006	0x2018	Back door for read channel's QoS	RW
DC_PCFG_OFIFO	0x0319_0842	0x2020	Priority level threshold config when rdma	RW
DC_RDMA_DES	0x0000_0000	0x2114	for debug	R
DC_RDMA_CHAIN_SITE	0x0000_0000	0x2204	rdma descriptor's current site	R
DC_RDMA_SITE	0x0000_0000	0x3110	rdma's current site	R
DISP_COM	0x0000_0000	0x8000	display common configure	RW
TFT_TIMING_HSYNC	0x0000_0000	0x9000	TFT HSYNC	RW
TFT_TIMIING_VSYNC	0x0000_0000	0x9004	TFT VSYNC	RW
TFT_ TIMIING_HDE	0x0000_0000	0x9008	TFT HDE	RW
TFT_ TIMIING_VDE	0x0000_0000	0x900C	TFT VDE	RW
TFT_TRAN_CFG	0x0000_0000	0x9010	TFT configure	RW
TFT_ST	0x0000_0000	0x9014	TFT status	R
SLCD_PANEL_CFG	0x0154_0D20	0xA000	SLCD configure	RW
SLCD_WR_DUTY	0x0000_0000	0xA004	SLCD WR's duty	RW
SLCD_TIMING	0x0000_0000	0xA008	SLCD timing	RW
SLCD_FRM_SIZE	0x0000_0000	0xA00C	frame size	RW
SLCD_SLOW_TIME	0x0000_0000	0xA010	slow time	RW
SLCD_REG_IF	0x8000_0000	0xA014	SLCD reg-op interface	RW
SLCD_ST	0x0000_0000	0xA018	SLCD status	R
SLCD_REG_CTRL	0x0000_0000	0xA01C	SLCD reg-op interface control	W

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

10.5.3 Basic configure

10.5.3.1 Simple read DMA descriptor configure

10.5.3.1.1 RDMA descriptor address

	DC_SRD_CHAIN_ADDR																															BASE+0x1000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SRD_CHAIN_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	SRD_CHAIN_ADDR	This is the address of the 1st descriptor before working; After start working, it is the address of the next descriptor. It can be changed by software for descriptor inserting operation. Note: the address must aligned to 64bits	RW

10.5.3.1.2 RDMA descriptor control

	DC_SRD_CHAIN_CTRL																															BASE+0x1004
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															SRD_CHAIN_START
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
0	SRD_CHAIN_START	RDMA descriptor DMA start	W

10.5.3.2 Control configure

	DC_CTRL																															BASE+0x2000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Reserved	GEN_STP_SRD	Reserved	DES_CNT_RST	QCK_STP_SRD	Reserved
RST	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0	0	0	0

Bits	Name	Description	RW
31:5	Reserved	Writing has no effect, read as zero.	R
4	GEN_STP_SRD	Generic stop the simple read channel. Assure integrity of the current frame	W
3	Reserved	Writing has no effect, read as zero.	R
2	DES_CNT_RST	Reset the counter of RDMA_DES	W
1	QCK_STP_SRD	Quick stop the simple read channel. Stop as quickly as possible, the integrity of the current frame not be guaranteed.	W
0	Reserved	Writing has no effect, read as zero.	R

10.5.3.3 Status Register

	DC_ST																															BASE+0x2004
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved														DISP_END	Reserved								TFT_UNDR	STOP_SRD_ACK	Reserved			SRD_WORKING	SRD_START	SRD_END	WORKING
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:18	Reserved	Writing has no effect, read as zero.	R
17	DISP_END	One frame display end	R
16:9	Reserved	Writing has no effect, read as zero.	R
8	TFT_UNDR	TFT jump into under-run mode	R
7	STOP_SRD_ACK	Simple read channel is generic stopped	R
6:4	Reserved	Writing has no effect, read as zero.	R
3	SRD_WORKING	Simple read channel is working	R
2	SRD_START	Start reading one frame by SRD channel	R
1	SRD_END	One frame read end by SRD channel	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

0	WORKING	display controller is working	R

10.5.3.4 Clear status Register

	DC_CLR_ST																															BASE+0x2008
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved														CLR_DISP_END		Reserved							CLR_TFT_UNDR	CLR_STP_SRD_ACK	Reserved				CLR_SRD_START	CLR_SRD_END	Reserved
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:18	Reserved	Writing has no effect, read as zero.	R
17	CLR_DISP_END	clear DISP_END	W
16:9	Reserved	Writing has no effect, read as zero.	R
8	CLR_TFT_UNDR	clear TFT_UNDR	W
7	CLR_STP_SRD_ACK	clear STOP_SRD_ACK	W
6:3	Reserved	Writing has no effect, read as zero.	R
2	CLR_SRD_START	clear SRD_RD_START	W
1	CLR_SRD_END	clear SRD_RD_END	W
0	Reserved	Writing has no effect, read as zero.	R

10.5.3.5 DPU INTC register

	DC_INTC																															BASE+0x200c
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved														EOD_MSK		Reserved							UOT_MSK	SSA_MSK	Reserved				SOS_MSK	EOS_MSK	Reserved
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:18	Reserved	Writing has no effect, read as zero.	R
17	EOD_MSK	mask of DISP_END 1: generate interrupt	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		0: interrupt is masked	
16:9	Reserved	Writing has no effect, read as zero.	R
8	UOT_MSK	mask of TFT_UNDR 1: generate interrupt 0: interrupt is masked	RW
7	SSA_MSK	mask of STOP_SRD_ACK 1: generate interrupt 0: interrupt is masked	RW
6:3	Reserved	Writing has no effect, read as zero.	R
2	SOS_MSK	mask of SRD_START 1: generate interrupt 0: interrupt is masked	RW
1	EOS_MSK	mask of SRD_END 1: generate interrupt 0: interrupt is masked	RW
0	Reserved	Writing has no effect, read as zero.	R

10.5.3.6 INT flag register

	DC_INT_FLAG																																BASE+0x2010
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved														INT_EOD	Reserved								INT_UOT	INT_SSA	Reserved				INT_SOS	INT_EOS	Reserved
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:18	Reserved	Writing has no effect, read as zero.	R
17	INT_EOD	interrupt of DISP_END	R
16:9	Reserved	Writing has no effect, read as zero.	R
8	INT_UOT	interrupt of TFT_UNDR	R
7	INT_SSA	interrupt of STOP_SRD_ACK	R
6:3	Reserved	Writing has no effect, read as zero.	R
2	INT_SOS	interrupt of SRD_START	R
1	INT_EOS	interrupt of SRD_END	R
0	Reserved	Writing has no effect, read as zero.	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

10.5.3.7 Common configure register

	DC_COM_CONFIG																															BASE+0x2014
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										BURST_LEN_RDMA		Reserved			
RST	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:18	Reserved	Writing has no effect, read as zero.	R
5:4	BURST_LEN_RDMA	The max length of the simple read DMA's burst. 00: 4(default) 01: 8 10: 16 11: 32	RW
3:0	Reserved	Writing has no effect, read as zero.	R

10.5.3.8 Priority configure register

10.5.3.8.1 PCFG_RD_CTRL register

	DC_PCFG_RD_CTRL																															BASE+0x2018
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																													arqos_val		arqos_ctrl
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

Bits	Name	Description	RW
31:3	Reserved	Writing has no effect, read as zero.	R
2:1	Arqos_val	QoS value. 00~11, and reset value is 11.	RW
0	Arqos_ctrl	Whether use the value set by software. 0: the value is generated by the hardware; 1: the value is specified by software.	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

10.5.3.8.2 OFIFO's PCFG register

	DC_OFIFO_PCFG																															BASE+0x2020
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved					Pcfg2									Pcfg1									Pcfg0								
RST	0	0	0	0	0	0	1	1	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0	0	0	1	0

OFIFO_PCFG is used when simple read dma..

The 3 thresholds cut the output FIFO into 4 space. When the entries remained triggers one of them, the priority level will be altered by hardware. And the 3 thresholds must follow the order: pcfg2 ≥ pcfg1 ≥ pcfg0.

Priority level（arqos）:

Priority_lv	Space
11	Empty ~ threshold0
10	Threshold0 ~ threshold1
01	Threshold1 ~ threshold2
00	Threshold2 ~ full

Bits	Name	Description	RW
31:27	Reserved	Writing has no effect, read as zero.	R
26:18	Pcfg2	Threshold2:0~263	RW
17:9	Pcfg1	Threshold1:0~263	RW
8:0	Pcfg0	Threshold0:0~263	RW

10.5.3.9 Descriptor read registers

10.5.3.9.1 Simple read configure descriptor register

	DC_RDMA_DES																															BASE+0x2114
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RDMA_DES																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	RDMA_DES	Read the simple read DMA configure descriptor in order, one at a time.	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		The counter will reset when writing DES_CNT_RST	

10.5.3.10 Software locate register

10.5.3.10.1 RDMA descriptor's current site register

	DC_RDMA_CHAIN_SITE																															BASE+0x2204
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RDMA_CHAIN_SITE																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	RDMA_CHAIN_SITE	Read the current descriptor site in DDR memory of simple reading.	R

10.5.3.10.2 Simple read DMA's current pixel site register

	DC_RDMA_SITE																															BASE+0x3110
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RDMA_SITE																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	RDMA_SITE	Read the current pixel site in DDR memory of simple reading.	R

10.5.4 Display interfaces configure

10.5.4.1 Common

	DISP_COM																															BASE+0x8000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved										DP_DITHER_DW						Reserved								DITHER_CLKGATE_EN	LCD_CLKGATE_EN	TFT_CLKGATE_EN	DP_DITHER_EN	Reserved		DP_IF_SEL	

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0

Bits	Name	Description	RW
31:22	Reserved	Writing has no effect, read as zero.	R
21:16	DP_DITHER_DW	Dither drop bit. 0: drop low 0 bit(default) 1: drop low 2 bit 2: drop low 3 bit 3: drop low 4 bit [17:16]: configure blue color [19:18]: configure green color [21:20]: configure red color When source pixel is RGB888, and output at RGB666/565, the value should be 010101/100110.	RW
15:8	Reserved	Writing has no effect, read as zero.	R
7	DITHER_CLKGATE_EN	Clk gate enable, 1:indicate open clk gate. 0:indicate disable clk gate, Dither always has clock.	RW
6	SLCD_CLKGATE_EN	Clk gate enable, 1:indicate open clk gate. 0:indicate disable clk gate, SLCD always has clock.	RW
5	TFT_CLKGATE_EN	Clk gate enable, 1:indicate open clk gate. 0:indicate disable clk gate, TFT always has clock.	RW
4	DP_DITHER_EN	Dither enable. 0: dither disable(default) 1: dither enable **NOTE**: If source data is not 888 format, dither need be disabled.	RW
3:2	Reserved	Writing has no effect, read as zero.	R
1:0	DP_IF_SEL	Display interfaces select. 0: no display(default) 1: TFT 2: SLCD	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

10.5.4.2 TFT

10.5.4.2.1 TIMING_HSYNC

	TFT_TIMING_HSYNC																															BASE+0x9000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				HPS												Reserved				HPE											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:28	Reserved	Writing has no effect, read as zero.	R
27:16	HPS	HSYNC pulse start point(base on dot clock cycle) This bit must not be 0.	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

15:12	Reserved	Writing has no effect, read as zero.	R
11:0	HPE	HSYNC pulse end point(base on dot clock cycle) This bit must not be 0.	RW

10.5.4.2.2 TIMING_VSYNC

	TFT_TIMING_VSYNC																															BASE+0x9004
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			VPS													Reserved			VPE												
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:28	Reserved	Writing has no effect, read as zero.	R
27:16	VPS	VSYNC pulse start point(base on dot clock cycle) This bit must not be 0.	RW
15:12	Reserved	Writing has no effect, read as zero.	R
11:0	VPE	VSYNC pulse end point(base on dot clock cycle) This bit must not be 0.	RW

10.5.4.2.3 TIMING_HDE

	TFT_TIMING_HDE																															BASE+0x9008
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			HDS													Reserved			HDE												
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:28	Reserved	Writing has no effect, read as zero.	R
27:16	HDS	Horizontal display area start point (base on dot clock cycle). And it is also the DE pulse start point in horizontal. It indicate the end point of horizontal back porch.	RW
15:12	Reserved	Writing has no effect, read as zero.	R
11:0	HDE	Horizontal display area end point (base on dot clock cycle). And it is also the DE pulse end point in horizontal. It indicate the start point of horizontal front porch.	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

10.5.4.2.4 TIMING_VDE

	TFT_TIMING_VDE																															BASE+0x900C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			VDS													Reserved			VDE												
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:28	Reserved	Writing has no effect, read as zero.	R
27:16	VDS	Vertical display area start point(base on dot clock cycle). And it is also the DE pulse start point in vertical. It indicate the end point of vertical back porch.	RW
15:12	Reserved	Writing has no effect, read as zero.	R
11:0	VDE	Vertical display area end point(base on dot clock cycle). And it is also the DE pulse end point in vertical. It indicate the start point of vertical front porch.	RW

10.5.4.2.5 TRANS_CONFIG

	TFT_TRAN_CFG																															BASE+0x9010
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved										COLOR_EVEN			COLOR_ODD			Reserved					PIXCLK_INV	DE_DL	SYNC_DL	Reserved					MODE		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:18	Reserved	Writing has no effect, read as zero.	R
21:19	COLOR_EVEN	Output color mode of even lines(2, 4, 6...) 000: RGB→RGB 001: RGB→RBG 010: RGB→BGR 011: RGB→BRG 100: RGB→GBR 101: RGB→GRB	RW
18:16	COLOR_ODD	Output color mode of odd lines(1, 3, 5...) 000: RGB→RGB 001: RGB→RBG	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		010: RGB→BGR 011: RGB→BRG 100: RGB→GBR 101: RGB→GRB	
15:11	Reserved	Writing has no effect, read as zero.	R
10	PIX_CLK_INV	Inverse the polarity of the DOT_CLK	RW
9	DE_DL	Default level of DE(Data Enable)(invalid level)	RW
8	HSYNC_DL	Default level of HSYNC (invalid level)	RW
7	VSYNC_DL	Default level of VSYNC (invalid level)	RW
6:3	Reserved	Writing has no effect, read as zero.	R
2:0	MODE	000: 888 parallel mode 001: 666 parallel mode 010: 565 parallel mode 100: 8bits serial mode without dummy(RGB) 101: 8bits serial mode with dummy(RGBD)	RW

10.5.4.2.6 STATUS

	TFT_ST																															BASE+0x9014
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														WORKING	UNDER
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:2	Reserved	Writing has no effect, read as zero.	R
1	WORKING	0: TFT is not working 1: TFT is working	R
0	UNDER	Indicate the controller jump into recovery state, and starting trans one frame 0 to panel. 0: TFT is working order 1: TFT is in UNDER mode.	R

10.5.4.3 SLCD (Smart LCD)

10.5.4.3.1 SLCD_CONFIG

	SLCD_PANEL_CFG																															BASE+0xA000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Reserved				RDY_JIT	FMT_EN	DBI_TYPE			PIX_FMT		TE_JIT	TE_MD	TE_SWITCH	RDY_SWITCH	CS_EN	Reserved				CS_DP	RDY_DP	DC_MD	WR_MD	Reserved	TE_DP	DWIDTH			CWIDTH		
RST	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	0	0	0	0	0	1	1	0	1	0	0	1	0	0	0	0	0

Bits	Name	Description	RW
31:28	Reserved	Writing has no effect, read as zero.	R
27	RDY_ANTI_JIT	Anti-jitter for RDY. 0: sample RDY with 1 pixclk cycle(default) 1: sample RDY with 3 pixclk cycles for anti-jitter.	RW
26	FMT_EN	Whether the pixels by REG_IF need conversion 0: no use conversion;(default) 1: need conversion.	RW
25:23	DBI_TYPE	001: typeA(6800) 010: typeB(8080)(default) 100: typeC(SPI-3line) 101: typeC(SPI-4line) other: reserved	RW
22:21	PIX_FMT	Color format. 00: 565 (typeA/B、typeC) 01: 666 (typeA/B) 01: 444 (typeC) 10: 888 (typeA/B、typeC)(default) NOTE: typeA/B For 565, the DWIDTH can be 8bits and 16bits; For DWIDTH = 9bits, there is only 666 format; For DWIDTH = 16bits, there is only 565 format; For DWIDTH = 18bits, there is only 666 format; For 888, the DWIDTH can be 8bits and 24bits; Note: The pairing of DWIDTH and DATA_FMT is only these 5 modes, other configure is error. typeC: There are 444、565、888（for 888,high six bits are valid each byte for lcd screen, so format is 666 for lcd screen）	
20	TE_ANTI_JIT	Anti-jitter for TE. 0: sample TE with 1 pixclk cycle; 1: sample TE with 3 pixclk cycles for anti-jitter(default).	RW
19	TE_MD	The active edge of TE. 0: the front edge(default)	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		1: the back edge	
18	TE_SWITCH	0: do not wait TE, send pix_data after SLCD_START; 1: wait TE, and then send pix_data.(default)	RW
17	RDY_SWITCH	0: do not wait RDY, send command or data immediately;(default) 1: wait RDY, and then send command or data.	RW
16	CS_EN	CS control enable. 0: The CS pin is controlled by GPIO.(default) 1: The CS pin is controlled by SLCD.	RW
15:12	Reserved	Writing has no effect, read as zero.	R
11	CS_DP	The CS's default polarity 0: the default(invalid) level is low; 1: the default(invalid) level is high;(default)	RW
10	RDY_DP	The RDY's default polarity 0: the default(invalid) level is low; 1: the default(invalid) level is high;(default)	RW
9	DC_MD	DC's definition. 0: Command DC = low, Data DC = high(default) 1: Command DC = high, Data DC = low	RW
8	WR_MD	WR's definition. 0: drive at posedge(drive level is high) sample at negedge(sample level is low); 1: drive at negedge(drive level is low) sample at posedge(sample level is high).(default) Note: When typeC, the WR pin is SPI_CLK.	RW
7	Reserved	Writing has no effect, read as zero.	R
6	TE_DP	The TE' default polarity 0: the default(invalid) level is low;(default) 1: the default(invalid) level is high;	RW
5:3	DWIDTH	Panel's data bus width at typeA/B. 000: 8bits(typeA/B) 001: 9bits(typeA/B) 010: 16bits(typeA/B) 011: 18bits(typeA/B) 100: 24bits(typeA/B) (default) Note: When typeC, DWIDTH is no use.	RW
2:0	CWIDTH	The width of panel's command and it's parameters. 000: 8bits(typeA/B) (default) 001: 9bits(typeA/B) 010: 16bits(typeA/B) 011: 18bits(typeA/B) 100: 24bits(typeA/B) Note: When typeC, CWIDTH is no use. But only 8bits command	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		can be supported.	

NOTE1: When configure stage, keep CS inactive.

NOTE2:

When DMA mode, pixels will be formatted, not controlled by FMT_EN;

When register mode, command and parameters will not be formatted, not controlled by FMT_EN;

When register mode, pixels will be controlled by FMT_EN (0: SLCD will directly output the low 8/16/18 bits of content of REG_IF directly; 1: SLCD will convert the content of REG_IF.

Note:

When send command by REG_IF, the output command is only decided by CWIDTH. If CWIDTH is 8bits, only the low 8 bits of content of REG_IF are useful, other bits will be lost; if CWIDTH is 9bits, only the low 9bit of content of REG_IF are useful, other bits will be lost; and so on.

10.5.4.3.2 SLCD_WR_DUTY

	SLCD_WR_DUTY																															BASE+0xA004
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DSTIME								DDTIME								CSTIME								CDTIME							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:24	DSTIME	WR's sample level period when transmitting pixels or parameters.	RW
23:16	DDTIME	WR's drive level period when transmitting pixels or parameters.	RW
15:8	CSTIME	WR's sample level period when transmitting command	RW
7:0	CDTIME	WR's drive level period when transmitting command	RW

NOTE: The description is based on 8080(MIPI DBI TypeB) and SPI(MIPI DBI TypeC)mode, it's opposite when 6800(MIPI DBI TypeA) mode. The actual cycle is n+1.

10.5.4.3.3 SLCD_TIMING

	SLCD_TIMING																															BASE+0xA008
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TCH								TCS								TAH								TAS							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:24	TCH	Chip select hold time.	RW
23:16	TCS	Chip select setup time.	RW
15:8	TAH	Address hold time.	RW
7:0	TAS	Address setup time.	RW

Note：TAS, TCS, TCH are used in both parallel and serial mode, while TAH is only used in serial mode. The actual cycle is n+1.

10.5.4.3.4 SLCD_FRM_SIZE

	SLCD_FRM_SIZE																															BASE+0xA00C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	V_SIZE																H_SIZE															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	V_SIZE	Line number of each frame.	RW
15:0	H_SIZE	Pixel number of each line.	RW

10.5.4.3.5 SLCD_SLOW_TIME

	SLCD_SLOW_TIME																															BASE+0xA010
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																SLOW_TIME															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

31:16	Reserved	Writing has no effect, read as zero.	R
15:0	SLOW_TIME	SLCD will delay some period of pixclk before transmitting data, after TE's relative edge. NOTE: If want to use this function, must set SLCD_PANEL_CFG.bit18=1.	WR

10.5.4.3.6 SLCD_REG_IF

	SLCD_REG_IF																															BASE+0xA014
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FLAG		CMD_END	Reserved					content																							
RST	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:30	FLAG	It is used to decide the meanings of the DATA/CMD/PARAMETER. 00: pix_data; 01: parameter; 1x: command(default).	RW
29	CMD_END	Indicate this is the last content, the hardware will disable the CS	RW
28:24	Reserved	Writing has no effect, read as zero.	R
23:0	content	content	RW

NOTE: The next command(include its parameters) or pix_data must wait BUSY is 0 when using the reg_if for transmission.

There would no frm_end when sending pixels by SLCD_REG_IF.

10.5.4.3.7 SLCD_STATUS

	SLCD_ST																															BASE+0xA018
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															BUSY
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect, read as zero.	R
0	BUSY	Indicate whether the SLCD DBI interface controller is working or not.	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		0: idle 1: busy	

10.5.4.3.8 SLCD_REG_CTRL

	SLCD_REG_CTRL																															BASE+0xA01C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															RESET_3LINE
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect, read as zero.	R
0	RESET_3LINE	Write 1 to reset an inner counter when sending frame by SLCD_REG_IF, write one before each frame(only used at typeC 3line 444 mode	W

10.6 Operation guide

10.6.1 Simple read dma(SRD) operation

(1) Set DC_INTC for DISP_END(EOD_MASK).

(2) Prepare SRD descriptor chain.

(3) Set CHAIN_END of the SRD descriptor if this is the last frame for display.

(4) Set SRD descriptor's address by DC_SRD_CHAIN_ADDR register.

(5) Set DIS_IF_SEL of DISP_COM register for TFT or SLCD.

(6) Set DC_SRD_CHAIN_CTRL register to start SRD.

10.6.2 TFT operation

(1) Set TFT_TIMING_HSYNC, TFT_TIMING_VSYNC, TFT_TIMING_HDE, TFT_TIMING_VDE;

for example, see picture of 10.5.4.2: HS, invalid time of HSYNC, need 5 cycles at least, HBP need 10 cycles, HFP need 10 cycles, and there are 800 pixels per line. So HPS need set 5, HPE need set 825; HDS need set 15, HDE need set 815; configure VSYNC and VDE use same method.

(2) Set TFT_TRAN_CFG

PIX_CLK_INV, DE_DL and SYNC_DL respectively used to adjust the phase of DOT_CLK, DE, HSYNC and VSYNC; COLOR_EVEN and COLOR_ODD used to change the output mode of pixel color mode; MODE used to configure the transfer mode.

(3) Start to configure SRD as steps 10.6.1

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

10.6.3 SLCD operation

(7) Configure each bit of SLCD_PANEL_CFG according to the relevant instructions;
(8) Set SLCD_WR_DUTY, SLCD_TIMING and SLCD_SLOW_TIME to meet panel requirements;
(9) Set SLCD_FRM_SIZE to the actual size;
(10) Start to configure SRD as steps 10.6.1
(11) Set FMT_EN of SLCD_PANEL_CFG to 0(if no command, skip this step);
(12) Write a command and its flag to SLCD_CMD(if no command, skip this step);
(13) Wait BUSY of SLCD_ST is 0(if no command, skip this step);
(14) Repeat step(5) and (6) until all command send out(if no command, skip this step);
(15) Set FMT_EN to 1;
(16) Write SLCD_START;
(17) Wait FRM_END of DC_ST, and clear it;
(18) Repeat step(5) to (11) for next frame transfer.

10.6.4 Insert new descriptor into current chain

Write the new descriptor's address in FRM_CHAIN_ADDR/SRD_CHAIN_ADDR, hardware will change to the new chain at appropriate time.

10.6.5 Interrupt control

The mask of interrupt in descriptor must cooperate with the same mask in INTC reg, interrupt can be generate only if both mask is 1; other interrupt are controlled only by INTC reg.

10.7 Software Notes

When frame is less than 500 pixels, descriptor chain cannot be continuous, only one descriptor can be executed.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Section 5

SYSTEM FUNCTIONS

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

11 Clock Reset and Power Controller

11.1 Overview

The Clock & Power management block consists of: Clock control, PLL control, and Power control, Reset control.

The Clock control logic can generate the required clock signals including CCLK for CPU/L2CACHE, HHCLK for BIU, H0CLK for the AHB0, H2CLK for the AHB2, PCLK for the APB bus peripherals , DDR_CLK for DDR.

The Chip has three Phase Locked Loops (PLL):

1. APLL mainly is used to CPU and L2CACHE, also may use the AHB0 and AHB2, or other peripherals
2. MPLL mainly is used to DDR, also uses AHB0 and AHB2 APB, or other peripherals
3. EPLL mainly is used to AUDIO and other peripherals.

For the power control logic, there are various power management schemes to keep optimal power consumption for a given task. The power management block can activate four modes: NORMAL mode, IDLE mode, PD_IDLE mode, SLEEP mode.

For reset control logic, the hardware reset and hibernate reset is extended to more 10ms. It controls or distributes all of the system reset signals.

Feature:

- On-chip 2MHz~27MHZ oscillator circuit
- On-chip 32.768KHZ oscillator circuit
- One three-chip phase-locked loops (PLL) with programmable multiplier
- CCLK, HHCLK, H2CLK, PCLK, H0CLK, DDR_CLK frequency can be changed separately for software by setting registers
- Functional-unit clock gating

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

11.1.1 CGU Block Diagram

Following figure illustrates a block diagram of CGU.

Note:

Clock mux **in grey color** represents **glitch-free** clock mux, which is free of glitches if clock selection is changed. Clock mux in white color represents non-glitch-free clock mux, which can suffer from glitches when changing clock sources. **Care must be taken in using each of clock muxes**.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

11.1.2 CGU Registers

Following chapter will descript the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. Register read/write attribute
   R - Read only
   W - Write only
   RW - read and write
   RCW - read and write, but clear to 0 by read
   RSW - read and write, but set to 1 by read
   RWC - read and write, clear to 0 by write 1, write 0 has no effect
   RWS - read and write, set to 1 by write 1, write 0 has no effect
   RC - read only, and clear to 0 by read
   RS - read only, and set to 1 by read
   SPEC - special access method, relate to its description
3. Reset Value
   1 - reset to 1
   0 - reset to 0
   ? - value unknown after reset

Table 11-1 Registers Memory Map-Address Base

Name	Base	Description
CPM	0x10000000	Address base of CPM

Table 11-2 CGU Registers Configuration

Name	description	RW	Reset Value	Address offset	Access Size
CPCCR	Clock Control Register	RW	0x95000000	0x0000	32
CPCSR	Clock status register	RW	0x00000000	0x00D4	32
DDCDR	DDR clock divider Register	RW	0x40000000	0x002C	32
MACPHYCDR	MACPHY divider Register	RW	0x00000000	0x0054	32
I2S0CDR	I2S device clock divider Register	RW	0x00000000	0x0060	32
I2S0CDR1	I2S device clock divider Register	RW	0x00000000	0x0070	32
LPCDR	LCD pix clock divider Register	RW	0x00000000	0x0064	32
MSC0CDR	MSC0 clock divider Register	RW	0x40000000	0x0068	32
MSC1CDR	MSC1 clock divider Register	RW	0x00000000	0x00A4	32
SFCCDR	SFC clock divider Register	RW	0x00000000	0x0074	32
SSICDR	SSI clock divider Register	RW	0x00000000	0x005C	32
CIMCDR	CIM MCLK clock divider	RW	0x00000000	0x0078	32

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Register				
PWMCDR	PWM clock divider Register	RW	0x00000000	0x006C	32
CAN0CDR	CAN0 clock divider Register	RW	0x00000000	0x00A0	32
CAN1CDR	CAN1 clock divider Register	RW	0x00000000	0x00A8	32
CDBUSCDR	CDBUS clokc divider Register	RW	0x00000000	0x00AC	32
MACPHYC0	GMAC0 PHY Control Register	RW	0x00000000	0x00E4	32
CPM_INTR	CPM interrupt Register	RW	0x00000000	0x00B0	32
CPM_INTRE	CPM interrupt Enable Register	RW	0x00000000	0x00B4	32
CPM_SFTINT	CPM software interrupt	RW	0x00000000	0x00BC	32
DRCG	DDR clk gate register	RW	0x00000001	0x00D0	32
CPSPR	CPM Scratch Pad Register	RW	0x????????	0x0034	32
CPSPPR	CPM Scratch Protected Register	RW	0x0000a5a5	0x0038	32
USBPCR	USB Parameter control register	RW	0x409919b8	0x003C	32
USBRDT	USB Reset Detect Timer Register	RW	0x02000096	0x0040	32
USBVBFIL	USB jitter filter Register	RW	0x00ff0080	0x0044	32
USBPCR1	USB Parameter control register 1	RW	0x00000004	0x0048	32
CPPCR	PLL Control Register	RW	0x00000020	0x000C	32
CPAPCR	APLL Control Register	RW	0x06305060	0x0010	32
CPAPACR	APLL FRAC Register	RW	0x00000000	0x0084	32
CPMPCR	MPLL Control Register	RW	0x06305060	0x0014	32
CPMPACR	MPLL FRAC Register	RW	0x00000000	0x0088	32
CPEPCR	EPLL Control Register	RW	0x06305060	0x0018	32
CPEPACR	EPLL FRAC Register	RW	0x00000000	0x008c	32

11.1.2.1 Clock Control Register(CPCCR,0x00)

The Clock Control Register (CPCCR) is a 32-bit read/write register, which controls CCLK, H0CLK, H2CLK and PCLK division ratios. It is initialized to 0x95000000 by any reset. Only word access can be used on CPCCR.

	CPCCR																															BASE+0x00
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SEL_SRC		SEL_CPLL		SEL_H0PLL		SEL_H2PLL		GATE_SCLKA	CE_CPU	CE_AHB0	CE_AHB2	PDIV				H2DIV				H0DIV				L2CDIV				CDIV			
RST	0	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:30	SEL_SRC	00: stop MUX clock output 01: EXCLK 10: APLL The mux clock output is SCLK_A The clock mux is free of glitches if clock selection is changed When switching clock source, it should be ensured that the clock switched from and the clock switched to both are running.	RW
29:28	SEL_CPLL	00: stop MUX clock output 01: SCLK_A 10: MPLL The mux clock output is to CPU and L2CAHE The clock mux is free of glitches if clock selection is changed When switching clock source, it should be ensured that the clock switched from and the clock switched to both are running.	RW
27:26	SEL_H0PLL	00: stop MUX clock output 01: SCLK_A 10: MPLL The mux clock output is to AHB0 The clock mux is free of glitches if clock selection is changed When switching clock source, it should be ensured that the clock switched from and the clock switched to both are running.	RW
25:24	SEL_H2PLL	00 : stop MUX clock output 01: SCLK_A 10: MPLL The mux clock output is to AHB2 The clock mux is free of glitches if clock selection is changed When switching clock source, it should be ensured that the clock switched from and the clock switched to both are running.	RW
23	GATE_SCLKA	0: SCLK_A not gating 1: SCLK_A is gating. Gating modules: LCD MSC MAC AIC USB SSI PCM CIM etc	RW
22	CE_CPU	Change enable for CPU and L2CAHE. If CE_CPU is 1 , write on CDIV, L2CDIV will start a frequency changing sequence immediately. If CE_CPU is 0, writes on CDIV and L2CDIV have no affect.	RW
21	CE_AHB0	Change enable for AHB0. If CE_AHB0 is 1 , write on H0DIV will start a frequency changing sequence immediately. If CE_AHB0 is 0, writes on H0DIV have no affect.	RW
20	CE_AHB2	Change enable for AHB2. If CE_AHB2 is 1 , write on H2DIV, PDIV will start a frequency changing sequence immediately. If CE_AHB2 is 0, writes on H2DIV, PDIV have no affect.	RW
19:16	PDIV	Divider for Peripheral Frequency. Specified the PCLK division ratio.	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

			Bit 19~16: PDIV				Description
			0	0	0	0	X1
			0	0	0	1	X1/2
			0	0	1	0	X1/3
			0	0	1	1	X1/4
			0	1	0	0	X1/5
			0	1	0	1	X1/6
			0	1	1	0	X1/7
			0	1	1	1	X1/8
			1	0	0	0	X1/9
			1	0	0	1	X1/10
			1	0	1	0	X1/11
			1	0	1	1	X1/12
			1	1	0	0	X1/13
			1	1	0	1	X1/14
			1	1	1	0	X1/15
			1	1	1	1	X1/16
15:12	H2DIV	Divider for AHB2 Frequency. Specified the AHB2 CLK division ratio.					RW
			Bit 15~12: H2DIV				Description
			0	0	0	0	X1
			0	0	0	1	X1/2
			0	0	1	0	X1/3
			0	0	1	1	X1/4
			0	1	0	0	X1/5
			0	1	0	1	X1/6
			0	1	1	0	X1/7
			0	1	1	1	X1/8
			1	0	0	0	X1/9
			1	0	0	1	X1/10
			1	0	1	0	X1/11
			1	0	1	1	X1/12
			1	1	0	0	X1/13
			1	1	0	1	X1/14
			1	1	1	0	X1/15
			1	1	1	1	X1/16
11:8	H0DIV	Divider for AHB0 Frequency. Specified the AHB0 CLK division ratio.					RW
			Bit 11~8: H0DIV				Description
			0	0	0	0	X1
			0	0	0	1	X1/2
			0	0	1	0	X1/3
			0	0	1	1	X1/4

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

			0	1	0	0	X1/5	
			0	1	0	1	X1/6	
			0	1	1	0	X1/7	
			0	1	1	1	X1/8	
			1	0	0	0	X1/9	
			1	0	0	1	X1/10	
			1	0	1	0	X1/11	
			1	0	1	1	X1/12	
			1	1	0	0	X1/13	
			1	1	0	1	X1/14	
			1	1	1	0	X1/15	
			1	1	1	1	X1/16	
7:4	L2CDIV	Divider for L2CACHE output bus（BIU）Frequency. Specified the L2C CLK division ratio.						RW
			Bit 7~4: L2CDI				Description	
			0	0	0	0	X1	
			0	0	0	1	X1/2	
			0	0	1	0	X1/3	
			0	0	1	1	X1/4	
			0	1	0	0	X1/5	
			0	1	0	1	X1/6	
			0	1	1	0	X1/7	
			0	1	1	1	X1/8	
			1	0	0	0	X1/9	
			1	0	0	1	X1/10	
			1	0	1	0	X1/11	
			1	0	1	1	1/12	
			1	1	0	0	X1/13	
			1	1	0	1	X1/14	
			1	1	1	0	X1/15	
			1	1	1	1	X1/16	
3:0	CDIV	Divider for CPU Frequency. Specified the CPU CLK division ratio.						
			Bit 3~0: CDIV				Description	
			0	0	0	0	X1	
			0	0	0	1	X1/2	
			0	0	1	0	X1/3	
			0	0	1	1	X1/4	
			0	1	0	0	X1/5	
			0	1	0	1	X1/6	
			0	1	1	0	X1/7	
			0	1	1	1	X1/8	

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

			1	0	0	0	X1/9	
			1	0	0	1	X1/10	
			1	0	1	0	X1/11	
			1	0	1	1	X1/12	
			1	1	0	0	X1/13	
			1	1	0	1	X1/14	
			1	1	1	0	X1/15	
			1	1	1	1	X1/16	

Import Note1 : for PDIV and AHB2DIV, AHB2's clock frequency must be 1 or 2 times of PDIV's clock frequency. For L2CDIV and CDIV, CPU's clock frequency must be 1,2,3, or 4 times of L2CACHE's clock frequency.

Import Note2 : After reset, H0DIV and CE_AHB0 will be zero, and ahb0's clock freq and apb0's clock freq will be 1:1, but if you have ever set CE_AHB0 and change the value of H0DIV, ahb0's clock freq and apb0's clock freq will be 2:1 from then on.

11.1.2.2 Clock Status Register(CPCSR,0xD4)

Clock status register (CPCSR) is a 32-bit read/write register that specifies the status of CPCCR .This register is initialized to 0x00000000 only by any reset. Only word access can be used on CPCSR.

	CPCSR																															BASE+0xD4
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SRC_MUX	CPU_MUX	AHB0_MUX	AHB2_MUX	DDR_MUX	Reserved																								H2DIV_BUSY	H0DIV_BUSY	CDIV_BUSY
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	SRC_MUX	0: it indicates that mux switch has not stable 1: it indicates that mux switch has stable Software must check the value, then go next	R
30	CPU_MUX	0: it indicates that mux switch has not stable 1: it indicates that mux switch has stable Software must check the value, then go next	R
29	AHB0_MUX	0: it indicates that mux switch has not stable 1: it indicates that mux switch has stable Software must check the value, then go next	R
28	AHB2_M	0: it indicates that mux switch has not stable	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	UX	1: it indicates that mux switch has stable Software must check the value, then go next	
27	DDR_MUX	0: it indicates that mux switch has not stable 1: it indicates that mux switch has stable Software must check the value, then go next	R
26:3	Reserved	Writing has no effect, read as zero.	R
2	H2DIV_BUSY	The bit is a read-only bit. It indicates whether the frequency change has finished. When the bit is 0, it indicates frequency change has finished., otherwise it indicates the frequency change is on going Software should be wait until H2DIV_BUSY == 0, then may begin another frequency change.	R
1	H0DIV_BUSY	The bit is a read-only bit. It indicates whether the frequency change has finished. When the bit is 0, it indicates frequency change has finished., otherwise it indicates the frequency change is on going Software should be wait until H0DIV_BUSY == 0, then may begin another frequency change.	R
0	CDIV_BBBUSY	The bit is a read-only bit. It indicates whether the frequency change has finished. When the bit is 0, it indicates frequency change has finished., otherwise it indicates the frequency change is on going Software should be wait until CDIV_BUSY == 0, then may begin another frequency change.	R

11.1.2.3 DDR Memory clock divider Register(DDRCDR,0x2C)

DDR memory clock divider Register (DDRCDR) is a 32-bit read/write register that specifies the divider of DDR memory clock . This register is initialized to 0x40000000 only by any reset.
Only word access can be used on DDRCDR.

	DDRCDR																															BASE+0x002C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DCS		CE_DDR	DDR_BUSY	DDR_STOP	GATE_EN	CHANGE_EN	FLAG	Reserved																				DDRCDR			
RST	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:30	DCS	DDR Clock Source Selection. Selects the DDR clock source between APLL output and MPLL output. 00: stop MUX clock output 01: DDR clock source is SCLK_A 10: DDR clock source is MPLL	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		The clock mux is free of glitches if clock selection is changed When switching clock source, it should be ensured that the clock switched from and the clock switched to both are running.	
29	CE_DDR	Change enable for DDR. If CE_DDR is 1 , write on DDRCDR will start a frequency changing sequence immediately. If CE_DDR is 0, writes on DDRCDR have no affect	RW
28	DDR_BUSY	The bit is ready only bit. It indicates whether the frequency change has finished. When the bit is 0, it indicates frequency change has finished., otherwise it indicates the frequency change is on going Software should be wait until DDR_BUSY == 0, then may begin another frequency change.	R
27	DDR_STOP	When DDR_STOP is 1 and CE_DDR is 1, the DDR clock will stop. When DDR_STOP is 0 and CE_DDR is 1, the DDR clock will continue. Software should wait until DDR_BUSY == 0, then may begin another frequency change. DDR_STOP is prior to DDRCDR.	RW
26	GATE_EN	1'b1: if DDR gives a clock stop request to CPM, and CPM will gate DDR's clock.	
25	CHANGE_EN	When this bit set high, CPM will change DDR's clock when CE_DDR is high and FLAG is low	RW
24	FLAG	1：DDR reject frequency change 0: DDR not reject frequency change	R
23:4	Reserved	Writing has no effect, read as zero.	R
3:0	DDRCDR	Divider for DDR Frequency. Specified the DDR memory clock division ratio, which varies from 1 to 16 (division ratio = DDRCDR + 1).	RW

11.1.2.4 MACPHY clock divider Register(MACCDR,0x54)

MAC clock divider Register (MACCDR) is a 32-bit read/write register that specifies the divider of MAC PHY clock . This register is initialized to 0x00000000 only by any reset. Only word access can be used on MACCDR.

	MACCDR																															BASE+0x54
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MACPCS		CE_MAC	MAC_BUSY	MAC_STOP	Reserved																			MACCDR							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:30	MACPCS	MAC PHY Clock Source Selection. Selects the MAC PHY clock source 00: MAC PHY clock source is SCLK_A	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		01: MAC PHY clock source is MPLL 10: MAC PHY clock source is EPLL It is no glitch free mux.	
29	CE_MAC	Change enable for MAC. If CE_MAC is 1 , write on MACCDR ill start a frequency changing sequence immediately. If CE_MAC is 0, writes on MACCDR have no affect	RW
28	MAC_BUSY	The bit is read only bit. It indicates whether the frequency change has finished. When the bit is 0, it indicates frequency change has finished., otherwise it indicates the frequency change is on going Software should wait until MAC_BUSY == 0, may begin another frequency change.	R
27	MAC_STOP	When MAC_STOP is 1 and CE_MAC is 1, the MAC clock will stop. When MAC_STOP is 0 and CE_MAC is 1, the MAC clock will continue. Software should wait until MAC_BUSY == 0, may begin another frequency change.	RW
26:8	Reserved	Writing has no effect, read as zero.	R
7:0	MACCDR	Divider for MAC PHY Frequency. Specified the MAC device clock division ratio division ratio = MACCDR + 1	RW

11.1.2.5 I2S device clock divider Register(I2SxCDR,0x60)

I2S device clock divider Register (I2SxCDR) is a 32-bit read/write register that specifies the divider of I2S device clock . This register is initialized to 0x00000000 only by any reset. Only word access can be used on I2SxCDR.

Note: I2S0 for i2s0_dev_rclk; I2S1 for i2s0_dev_tclk;

	I2SxCDR																															BASE+0x60
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	I2PCS	CE_I2S	I2SDIV_M									I2SDIV_N																			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	Reserved	Writing has no effect, read as zero.	R
30	I2PCS	0: SCLK_A output 1: EPLL output	RW
29	CE_I2S	AIC M/N divider(1) enable.	RW
28:20	I2SDIV_M	Number M of AIC M/N divider(1).	RW
19:0	I2SDIV_	Number N of AIC M/N divider(1).	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	N		

Note [1]: AIC M/N divider is a decimal divider. The output clock frequency of AIC M/N divider is:

Fout = Fin * M / N.

N should not be less than M*2.

AIC M/N divider output clock duty cycle is possible not 50%. But adjusting the M and N value, which makes the duty cycle is close to 50%. Error of duty cycle is:

De_p = (ceill(N / M) - (N / M)) / (N / M). ceil: Round toward positive infinity.

and:

De_n = (floor(N / M) - (N / M)) / (N / M). floor: Round toward negative infinity.

Recommend the De_p is less than 5% and De_n is great than -5%.

11.1.2.6 I2S device clock divider Register1(I2SxCDR1,0x70)

I2S device clock divider Register 1(I2SxCDR1) is a 32-bit read/write register that specifies the divider of I2S device clock . This register is initialized to 0x00000000 only by any reset. Only word access can be used on I2SxCDR1.

	I2SxCDR1																															BASE+0x70
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	I2S_NEN	I2S_DEN	Reserved										I2SDIV_D																			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	I2S_NEN	0: The number N of AIC M/N divider is automatic calculate. 1: The number N of AIC M/N divider is set by I2SDIV_N. The automatic calculation is: $f_{out} = f_{in} * M/(N-0x1fff+M)$	RW
30	I2S_DEN	0: The number D of AIC M/N divider is automatic calculate. 1: The number D of AIC M/N divider is set by I2SDIV_D.	RW
29:20	Reserved	Writing has no effect, read as zero.	R
19:0	I2SDIV_D	The number D of AIC M/N divider[2].	RW

Note [2]: General D = N/2. Normal we can keep I2S_DEN \ I2S_NEN to '0' and don't care 'I2SDIV_D'.

There is a little mistake in this register: the 30 and 31 bit is miss-connected. For example, write 30 bit to "1", but it will be reflected in 31 bit; write 31 bit to "1", but it will be reflected in 30 bit.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

11.1.2.7 LCD pix clock divider Register(LPCDR,0x64)

LCD pix clock divider Register (LPCDR) is a 32-bit read/write register that specifies the divider of LCD pixel clock (LPCLK). This register is initialized to 0x00000000 by any reset. Only word access can be used on LPCDR.

	LPCDR																															BASE+0x64
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LPCS		CE_LCD	LCD_BUSY	LCD_STOP	LCD_IO_INV	Reserved																		LPCDR							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:30	LPCS	00: SCLK_A output 01: MPLL output 10: EPLL It is no glitch free mux. Software should be stop PIX clock, when change this bit.	RW
29	CE_LCD	Change enable for LCD. If CE_LCD is 1 , write on LPCDR will start a frequency changing sequence immediately. If CE_LCD is 0, writes on LPCDR have no affect	RW
28	LCD_BUSY	The bit is read only bit. It indicates whether the frequency change has finished. When the bit is 0, it indicates frequency change has finished., otherwise it indicates the frequency change is on going Software should be wait until LCD_BUSY == 0, may begin another frequency change.	R
27	LCD_STOP	When LCD_STOP is 1 and CE_LCD is 1, the LCD clock will stop. When LCD_STOP is 0 and CE_LCD is 1, the LCD clock will continue. Software should wait until LCD_BUSY == 0, may begin another frequency change. LCD_STOP is prior to LPCDR. If system don't use this module, may set this bit to reduce power .	RW
26	LCD_IO_INV	LCD IO clock invert enable.	RW
25:8	Reserved	Writing has no effect, read as zero.	RW
7:0	LPCDR	Divider for Pixel Frequency. Specified the LCD pixel clock (LPCLK) division ratio, which varies from 1 to 256 (division ratio = LPCDR + 1).	RW

11.1.2.8 MSC0 device clock divider Register(MSC0CDR,0x68)

MSC0 device clock divider Register (MSC0CDR) is a 32-bit read/write register that specifies the divider of MSC0 device clock . This register is initialized to 0x40000000 only by any reset.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Only word access can be used on MSC0CDR.

	MSC0CDR																															BASE+0x68
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MPCS		CE_MSC0	MSC0_BUSY	MSC0_STOP	Reserved											S_CLK0_SEL	Reserved							MSC0CDR							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:30	MPCS	00: select SCLK_A clock output 01: select MPLL clock output 10: select EPLL clock output The clock mux is not free of glitches if clock selection is changed The clock mux output is to MSC0. It is source clock of MSC0.	RW
29	CE_MSC0	Change enable for MSC0. If CE_MSC0 is 1 , write on MSC0CDR ill start a frequency changing sequence immediately. If CE_MSC0 is 0, writes on MSC0CDR have no affect	RW
28	MSC0_BUSY	The bit is read only bit. It indicates whether the frequency change has finished. When the bit is 0, it indicates frequency change has finished., otherwise it indicates the frequency change is on going Software should be wait until MSC0_BUSY == 0, may begin another frequency change.	R
27	MSC0_STOP	When MSC0_STOP is 1 and CE_MSC0 is 1, the MSC0 clock will stop. When MSC0_STOP is 0 and CE_MSC0 is 1, the MSC0 clock will continue. Software should wait until MSC0_BUSY == 0, may begin another frequency change.MSC0_STOP is prior to MSC0CDR. If system don't use this module, may set this bit to reduce power .	RW
26:16	Reserved	Writing has no effect, read as zero.	R
15	S_CLK0_SEL	MSC sample clock selection: 0: Sample clock is 90-degree phase shifted by device clock. 1: Sample clock is 180-degree phase shifted by device clock	RW
14:8	Reserved	Writing has no effect, read as zero.	R
7:0	MSC0CDR	Divider for MSC0 Frequency. Specified the MSC0 device clock division ratio division ratio = (MSC0CDR + 1)*2.	RW

11.1.2.9 MSC1 device clock divider Register(MSC1CDR,0xA4)

MSC1 device clock divider Register (MSC1CDR) is a 32-bit read/write register that specifies the divider of MSC1 device clock . This register is initialized to 0x40000000 only by any reset. Only word access can be used on MSC1CDR.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	MSC1CDR																															BASE+0xA4
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MPCS		CE_MSC1	MSC1_BUSY	MSC1_STOP	Reserved											S_CLK1_SEL	Reserved							MSC1CDR							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:30	MPCS	00: select SCLK_A clock output 01: select MPLL clock output 10: select EPLL clock output The clock mux is not free of glitches if clock selection is changed The clock mux output is to MSC0. It is source clock of MSC0.	RW
29	CE_MSC1	Change enable for MSC1. If CE_MSC1 is 1 , write on MSC1CDR ill start a frequency changing sequence immediately. If CE_MSC1 is 0, writes on MSC1CDR have no affect	RW
28	MSC1_BUSY	The bit is read only bit. It indicates whether the frequency change has finished. When the bit is 0, it indicates frequency change has finished., otherwise it indicates the frequency change is on going Software should be wait until MSC1_BUSY == 0, may begin another frequency change.	R
27	MSC1_STOP	When MSC1_STOP is 1 and CE_MSC1 is 1, the MSC1 clock will stop. When MSC1_STOP is 0 and CE_MSC1 is 1, the MSC1 clock will continue. Software should wait until MSC1_BUSY == 0, may begin another frequency change.MSC1_STOP is prior to MSC1CDR. If system don't use this module, may set this bit to reduce power .	RW
26:16	Reserved	Writing has no effect, read as zero.	R
15	S_CLK1_SEL	MSC sample clock selection: 0: Sample clock is 90-degree phase shifted by device clock. 1: Sample clock is 180-degree phase shifted by device clock	RW
14:8	Reserved	Writing has no effect, read as zero.	R
7:0	MSC1CDR	Divider for MSC1 Frequency. Specified the MSC1 device clock division ratio division ratio = (MSC1CDR + 1)*2.	RW

11.1.2.10 SFC device clock divider Register(SFCCDR,0x74)

SFC device clock divider Register (SFCCDR) is a 32-bit read/write register that specifies the divider of SFC device clock . This register is initialized to 0x00000000 only by any reset. Only word access can be used on SFCCDR.the clk relation ship of SFC as follows:

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	SFCCDR																															BASE+0x74
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SFCS		CE_SFC	SFC_BUSY	SFC_STOP	Reserved																			SFCCDR							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:30	SFCS	00: select SCLK_A output 01: select MPLL output 10: EPLL It is direct to SFC module It is no glitch free mux. Software should be stop the module clock, when change this bit	RW
29	CE_SFC	Change enable for SFC. If CE_SFC is 1 , write on SFCCDR will start a frequency changing sequence immediately. If CE_SFC is 0, writes on SFCCDR have no affect	RW
28	SFC_BUSY	this bit is ready only bit. It indicates whether the frequency change has finished. When the bit is 0, it indicates frequency change has finished., otherwise it indicates the frequency change is on going Software should be wait until SFC_BUSY == 0, may begin another frequency change.	R
27	SFC_STOP	When SFC_STOP is 1 and CE_SFC is 1, the SFC clock will stop. When SFC_STOP is 0 and CE_SFC is 1, the SFC clock will continue. Software should wait until SFC_BUSY == 0, may begin another frequency change. SFC_STOP is prior to SFCCDR. If system don't use this module, may set this bit to reduce power .	RW
26:8	Reserved	Writing has no effect, read as zero.	R
7:0	SFCCDR	Divider for SFC Frequency. Specified the SFC device clock division ratio, which varies from 1 to 256 (division ratio = SFCCDR + 1).	RW

11.1.2.11 SSI device clock divider Register(SSICDR,0x5C)

SSI device clock divider Register (SSICDR) is a 32-bit read/write register that specifies the divider of SSI device clock . This register is initialized to 0x00000000 only by any reset. Only word access can be used on SSICDR.the clk relation ship of SSI is as follows:

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	SSICDR																															BASE+0x5C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SPCS		CE_SSI	SSI_BUSY	SSI_STOP	Reserved																			SSICDR							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:30	SPCS	00: select SCLK_A output 01: select MPLL output 10: EPLL It is direct to SSI module It is no glitch free mux. Software should be stop the module clock, when change this bit	RW
29	CE_SSI	Change enable for SSI. If CE_SSI is 1 , write on SSICDR will start a frequency changing sequence immediately. If CE_SSI is 0, writes on SSICDR have no affect	RW
28	SSI_BUSY	this bit is ready only bit. It indicates whether the frequency change has finished. When the bit is 0, it indicates frequency change has finished., otherwise it indicates the frequency change is on going Software should be wait until SSI_BUSY == 0, may begin another frequency change.	R
27	SSI_STOP	When SSI_STOP is 1 and CE_SSI is 1, the SSI clock will stop. When SSI_STOP is 0 and CE_SSI is 1, the SSI clock will continue. Software should wait until SSI_BUSY == 0, may begin another frequency change. SSI_STOP is prior to SSICDR. If system don't use this module, may set this bit to reduce power .	RW
26:8	Reserved	Writing has no effect, read as zero.	R
7:0	SSICDR	Divider for SSI Frequency. Specified the SSI device clock division ratio, which varies from 1 to 256 (division ratio = SSICDR + 1).	RW

11.1.2.12 CIM MCLK clock divider Register(CIMCDR,0x78)

CIM mclk clock divider Register (CIMCDR) is a 32-bit read/write register that specifies the divider of CIM mclk clock (CIM_MCLK). This register is initialized to 0x00000000 only by any reset. Only word access can be used on CIMCDR.

	CIMCDR	BASE+0x78

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CIMPCS		CE_CIM	CIM_BUSY	CIM_STOP	Reserved																			CIMCDR							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Name	Description	RW
31:30	CIMPCS	00: select SCLK_A clock output 01: select MPLL clock output 10: EPLL It is no glitch free mux. Software should be stop the module clock, when change this bit	RW
29	CE_CIM	Change enable for CIM. If CE_CIM is 1 , write on CIMCDR ill start a frequency changing sequence immediately. If CE_CIM is 0, writes on CIMCDR have no affect	RW
28	CIM_BUSY	The bit is ready only bit. It indicates whether the frequency change has finished. When the bit is 0, it indicates frequency change has finished., otherwise it indicates the frequency change is on going Software should be wait until CIM_BUSY == 0, may begin another frequency change.	R
27	CIM_STOP	When CIM_STOP is 1 and CE_CIM is 1, the CIM clock will stop. When CIM_STOP is 0 and CE_CIM is 1, the CIM clock will continue. Software should wait until CIM_BUSY == 0, may begin another frequency change. CIM_STOP is prior to CIMCDR. If system don't use this module, may set this bit to reduce power.	RW
26:8	Reserved	Writing has no effect, read as zero.	R
7:0	CIMCDR	Divider for CIM MCLK Frequency. Specified the CIM MCLK clock (CIM_MCLK) division ratio, which varies from 1 to 256 (division ratio = CIMCDR + 1). the output clock is "io_setup.cim_mclk_o".	RW

11.1.2.13 PWM clock divider Register(PWMCDR,0x6C)

PWM clock divider Register (PWMCDR) is a 32-bit read/write register that specifies the divider of PWM clock. This register is initialized to 0x00000000 only by any reset. Only word access can be used on PWMCDR.

	PWMCDR																															BASE+0x6C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	PWMPCS		CE_PWM	PWM_BUSY	PWM_STOP	Reserved																									CIMCDR			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Name	Description	RW
31:30	PWMPCS	00: select SCLK_A clock output 01: select MPLL clock output 10: EPLL It is no glitch free mux. Software should be stop the module clock, when change this bit	RW
29	CE_PWM	Change enable for PWM. If CE_PWM is 1 , write on PWMCDR will start a frequency changing sequence immediately. If CE_PWM is 0, writes on PWMCDR have no affect	RW
28	PWM_BUSY	The bit is ready only bit. It indicates whether the frequency change has finished. When the bit is 0, it indicates frequency change has finished., otherwise it indicates the frequency change is on going Software should be wait until PWM_BUSY == 0, may begin another frequency change.	R
27	PWM_STOP	When PWM_STOP is 1 and CE_PWM is 1, the PWM clock will stop. When PWM_STOP is 0 and CE_PWM is 1, the PWM clock will continue. Software should wait until PWM_BUSY == 0, may begin another frequency change. PWM_STOP is prior to PWMCDR. If system don't use this module, may set this bit to reduce power.	RW
26:4	Reserved	Writing has no effect, read as zero.	R
3:0	PWMCDR	Divider for PWM clock Frequency. Specified the clock division ratio, which varies from 1 to 256 (division ratio = PWMCDR + 1).	RW

11.1.2.14 CAN0 device clock divider Register(CAN0CDR,0xA0)

CAN0 device clock divider Register (CAN0CDR) is a 32-bit read/write register that specifies the divider of CAN0 device clock . This register is initialized to 0x00000000 only by any reset. Only word access can be used on CAN0CDR.the clk relation ship of CAN0 is as follows:

	CAN0CDR																															BASE+0xA0
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	CA0CS		CE_CAN0	CAN0_BUSY	CAN0_STOP	Reserved																			CAN0CDR							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:30	CA0CS	00: select SCLK_A output 01: select MPLL output 10: EPLL 11: EXCLK It is direct to CAN0 module It is no glitch free mux. Software should be stop the module clock, when change this bit	RW
29	CE_CAN0	Change enable for CAN0. If CE_CAN0 is 1 , write on CAN0CDR will start a frequency changing sequence immediately. If CE_CAN0 is 0, writes on CAN0CDR have no affect	RW
28	CAN0_BUSY	this bit is ready only bit. It indicates whether the frequency change has finished. When the bit is 0, it indicates frequency change has finished., otherwise it indicates the frequency change is on going Software should be wait until CAN0_BUSY == 0, may begin another frequency change.	R
27	CAN0_STOP	When CAN0_STOP is 1 and CE_CAN0 is 1, the CAN0 clock will stop. When CAN0_STOP is 0 and CE_CAN0 is 1, the CAN0 clock will continue. Software should wait until CAN0_BUSY == 0, may begin another frequency change. CAN0_STOP is prior to CAN0CDR. If system don't use this module, may set this bit to reduce power .	RW
26:21	Reserved	Writing has no effect, read as zero.	R
20	CAN0_EXCLK_EN	Exclk enable	RW
19:8	Reserved	Writing has no effect, read as zero.	R
7:0	CAN0CDR	Divider for CAN0 Frequency. Specified the CAN0 device clock division ratio, which varies from 1 to 256 (division ratio = CAN0CDR + 1).	RW

11.1.2.15 CAN1 device clock divider Register(CAN1CDR,0xA8)

CAN1 device clock divider Register (CAN1CDR) is a 32-bit read/write register that specifies the divider of CAN1 device clock . This register is initialized to 0x00000000 only by any reset.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Only word access can be used on CAN1CDR.the clk relation ship of CAN is as follows:

	CAN1CDR																															BASE+0xA8
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CA1CS		CE_CAN1	CAN1_BUSY	CAN1_STOP	Reserved																			CAN1CDR							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:30	CA1CS	00: select SCLK_A output 01: select MPLL output 10: EPLL 11: EXCLK It is direct to CAN1 module It is no glitch free mux. Software should be stop the module clock, when change this bit	RW
29	CE_CAN1	Change enable for CAN1. If CE_CAN1 is 1 , write on CAN1CDR will start a frequency changing sequence immediately. If CE_CAN1 is 0, writes on CAN1CDR have no affect	RW
28	CAN1_BUSY	this bit is ready only bit. It indicates whether the frequency change has finished. When the bit is 0, it indicates frequency change has finished., otherwise it indicates the frequency change is on going Software should be wait until CAN1_BUSY == 0, may begin another frequency change.	R
27	CAN1_STOP	When CAN1_STOP is 1 and CE_CAN1 is 1, the CAN1 clock will stop. When CAN1_STOP is 0 and CE_CAN1 is 1, the CAN1 clock will continue. Software should wait until CAN1_BUSY == 0, may begin another frequency change. CAN1_STOP is prior to CAN0CDR. If system don't use this module, may set this bit to reduce power .	RW
26:21	Reserved	Writing has no effect, read as zero.	R
20	CAN1_EXCLK_EN	Exclk enable	RW
19:8	Reserved	Writing has no effect, read as zero.	R
7:0	CAN1CDR	Divider for CAN1 Frequency. Specified the CAN1 device clock division ratio, which varies from 1 to 256 (division ratio = CAN1CDR + 1).	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

11.1.2.16 CDBUS device clock divider Register(CDBUSCDR,0xAC)

CDBUS device clock divider Register (CDBUSCDR) is a 32-bit read/write register that specifies the divider of CDBUS device clock . This register is initialized to 0x00000000 only by any reset. Only word access can be used on CDBUSCDR the clk relation ship of CDBUS is as follows:

	CDBUSCDR																															BASE+0xAC
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CDCS		CE_CDBUS	CDBUS_BUSY	CDBUS_STOP	Reserved																			CDBUSCDR							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:30	CDCS	00: select SCLK_A output 01: select MPLL output 10: EPLL It is direct to CDBUS module It is no glitch free mux. Software should be stop the module clock, when change this bit	RW
29	CE_CDBUS	Change enable for CDBUS. If CE_CDBUS is 1 , write on CDBUSCDR will start a frequency changing sequence immediately. If CE_CDBUS is 0, writes on CDBUSCDR have no affect	RW
28	CDBUS_BUSY	this bit is ready only bit. It indicates whether the frequency change has finished. When the bit is 0, it indicates frequency change has finished., otherwise it indicates the frequency change is on going Software should be wait until CDBUS_BUSY == 0, may begin another frequency change.	R
27	CDBUS_STOP	When CDBUS_STOP is 1 and CE_CDBUS is 1, the CDBUS clock will stop. When CDBUS_STOP is 0 and CE_CDBUS is 1, the cdbus clock will continue. Software should wait until CDBUS_BUSY == 0, may begin another frequency change. CDBUS_STOP is prior to CDBUSCDR. If system don't use this module, may set this bit to reduce power .	RW
26:8	Reserved	Writing has no effect, read as zero.	R
7:0	CDBUSCDR	Divider for CDBUS Frequency. Specified the CDBUS device clock division ratio, which varies from 1 to 256 (division ratio = CDBUSCDR + 1).	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

11.1.2.17 MAC PHY0 Control Register(MPHY0C,0xE4)

The MAC PHY0 Control Register is a 32-bit read/write register that control GMAC interface.It is initialized to 0x0000000 0by reset.

	MPHY0C																															BASE+0xE4
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Mode_sel	MAC_SPEED		Reserved																									SOFT_RST	PHY_INTF		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	Mode_sel	useless now	RW
30:29	MAC_SPEED	It is only read. 10: 10M 11: 100M	R
28:4	Reserved		R
3	SOFT_RST	1:reset GMAC0 0:don't reset GMAC0	RW
2:0	PHY_INTF	100: RMII other reserved	RW

11.1.2.18 CPM interrupt Register(CPM_INTR,0xB0)

	CPM_INTR																															BASE+0xB0
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														VBUS_INTR	ADEV_INTR
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:2	Reserved	Writing has no effect, read as zero.	R
1	VBUS_INTR	B device insert interrupt.	R
0	ADEV_INTR	A device insert interrupt.	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

11.1.2.19 CPM interrupt enable Register(CPM_INTRE,0xB4)

	CPM_INTRE																															BASE+0xB4
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														VBUS_INTRE	ADEV_INTRE
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:2	Reserved	Writing has no effect, read as zero.	R
1	VBUS_INTRE	B device insert interrupt enable.	RW
0	ADEV_INTRE	A device insert interrupt enable.	RW

11.1.2.20 CPM software interrupt Register(CPM_SFTINT,0xBC)

	CPM_SFTINT																															BASE+0xBC
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															SOFT
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect, read as zero.	R
0	SOFT	set 1 will send interrupt to each interrupt controller. relate to intc spec.	RW

11.1.2.21 DDR Clk Gate Register(DRCG,0xD0)

	DRCG																															BASE+0xD0
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																							DRCG								

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note: obsolete，keep it just for obsolete code

11.1.2.22 CPM Scratch Pad Protected Register(CPSPPR,0x38)

The Scratch Pad Protected Register is reset to 0x0000a5a5. When CPSPPR value equals to 0x00005a5a, software can write the CPSPR. or else can't.

	CPSPPR																															**BASE+0x38**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																CPSPPR															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1	0	1	1	0	1	0	0	1	0	1

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	CPSPPR	When the value is only = 0x00005a5a, software can write CPSPR.	RW

11.1.2.23 CPM Scratch Pad Register(CPSPR,0x34)

The Scratch Pad Register is a 32-bit read/write register that allows software to preserve some critical data. It is not initialized by power on and WDT reset.

	CPSPR																															**BASE+0x34**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CPSPR																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

11.1.2.24 USB Parameter Control Register(USBPCR,0x3C)

The USBPCR is a 32-bit read/write register that allows software to control OTG PHY some functions. It is initialized to 0x00000000.

	USBPCR																															**BASE+0x3C**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	USB_MODE	AVLD_REG	IDPULLUP_MASK		Reserved					POR	Reserved																					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	USB_MODE	0: work as USB device 1: work as OTG	RW
30	AVLD_REG	This bit is used to set “avalid”(VBUS above A-device session threshold) signal.	RW
29:28	IDPULLUP_MASK	These 2 bits control “idpullup” signal in otg mode. 2’b1x: “idpullup” always active 2’b01: “idpullup” always active when usb suspend 2’b00: use “idpullup” from otg controller	RW
27:23	Reserved	Writing has no effect, read as zero.	RW
22	POR	This bit controls OTG PHY power on reset. The POR signal must be asserted for a minimum of 10 µs. 1: reset 0: not reset	RW
21:0	Reserved	Writing has no effect, read as zero.	RW

11.1.2.25 USB Reset Detect Timer Register(USBRDT,0x40)

It is initialized to 0x2000096

	USBRDT																															**BASE+0x40**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Resu_inten	Resu_intclr	Resu_speed		Resume_stat	Reserved	VBFIL_LD_EN	IDDIG_EN	IDDIG_REG	Reserved																						
RST	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	1	0

Bits	Name	Description	RW
31	Resume_inten	Resume interrupt enable from sleep mode 1: enable 0:disable	RW
30	Resume_intclr	Resume interrupt flag clear 1: clear to 0 0: no effect	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

29:28	Resume_speed	usb speed before resume 00: high speed 01: full speed 10: low speed	RW
27	Resume_status	Resume status. 1: be Resumed 0: not Resumed	R
26	Reserved	Writing has no effect, read as zero.	RW
25	VBFIL_LD_EN	VBUS filter data load enable.	RW
24	IDDIG_EN	This bit indicates using IDDIG_REG to control “iddig” signal.	RW
23	IDDIG_REG	This bit controls “iddig” when IDDIG_REG_EN = 1’b1.	RW
22:0	Reserved	Writing has no effect, read as zero.	RW

11.1.2.26 USB VBUS Jitter Filter Register(USBVBFIL,0x44)

	USBVBFIL																															BASE+0x44
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IDDIGFIL																USBVBFIL															
RST	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	IDDIGFIL	These bits controls iddig jitter filter time.	RW
15:0	USBVBFIL	These bits controls VBUS jitter filter time.	RW

11.1.2.27 USB Parameter Control Register1(USBPCR1,0x48)

The USBPCR1 is a 32-bit read/write register that allows software to control OTG and OHCI PHY some functions. It is initialized to 0x80000000.

	USBPCR1																															BASE+0x48
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BVLD_REG	Reserved	dppulldown	dmpulldown	Reserved						PORT0_RST	Reserved																				
RST	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	BVLD_REG	This bit is used to set "bvalid"(VBUS above B-device session	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		threshold) signal.	
30	Reserved	Writing has no effect, read as zero.	R
29	Dppulldown	OTG PHY DP pull down 0: OTG PHY DP didn't pull down 1: OTG PHY DP pull down controlled by otg controller	RW
28	Dmpulldown	OTG PHY DM pull down 0: OTG PHY DM didn't pull down 1: OTG PHY DM pull down controlled by otg controller	RW
27:22	Reserved	Writing has no effect, read as zero.	R
21	PORT_RST	OTG PHY Port reset: 1: The transmit and receive finite state machines are reset, and the linestate logic combinatorially reflects the state of the single-ended receivers 0: The transmit and receive finite machines are operational, and the linestate inputs becomes sequential after 11 PHYCLOCK cycles.	RW
20:0	Reserved	Writing has no effect, read as zero.	R

11.1.2.1 PLL Control Register(CPPCR,0x0C)

The PLL Control Register (CPPCR) is a 32-bit read/write register, which controls PLL some controls bits and stabilize time. It is initialized to 0x00000020 only by any reset. Only word access can be used on CPPCR. It is used to control all PLL.

	CPPCR																															BASE+0x0C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	A_DACPD	APLL_BP	M_DACPD	MPLL_BP	E_DACPD	EPLL_BP	Reserved																		PLLST							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Name	Description	RW
31	A_DACPD	APLL DAC Power Down 0 - active mode 1 - test mode Don't change the value	RW
30	APLL_BP	APLL ByPass Mode: 0 - not bypass 1- bypass mode	RW
29	M_DACPD	MPLL DAC Power Down 0 - active mode 1 - test mode Don't change the value	RW
28	MPLL_B	MPLL ByPass Mode:	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	P	0 - not bypass 1 - bypass mode	
27	E_DACPD	EPLL DAC Power Down 0 - active mode 1 - test mode Don't change the value	RW
26	EPLL_BP	EPLL ByPass Mode: 0 - not bypass 1- bypass mode	RW
25:8	Reserved		R
7:0	PLLST	PLL Stabilize Time. Specifies the PLL stabilize time by unit of RTCCLK (approximate 32kHz) cycles. It is used when change PLL multiplier or change PLL from off to on. It is initialized to H'20. It is used to control all PLL.	RW

11.1.2.2 APLL Control Register(CPAPCR,0x10)

The APLL Control Register (CPAPCR) is a 32-bit read/write register, which controls PLL multiplier, on/off state and stabilize time. It is initialized to 0x99009020 only by any reset. Only word access can be used on CPAPCR

	CPAPCR																															BASE+0x10
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	APLLM												APLLN						APLLOD1			APLLOD0			A_DSMPD	A_PHASEPD	A_POSTDIVPD	A_VCOPD	APLL_ON	ALOCK	Reserved	APLLEN
RST	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	1	1	1	0	0	0	0	0	0

Bits	Name	Description	RW
31:20	APLLM	APLL feedback 12-bit multiplication factor NF = APLLM[11:0]	RW
19:14	APLLN	APLL input reference 6-bit divider. NR = APLLN[5:0]	RW
13:11	APLLOD1	APLL post VCO divider1 OD1 = APLLOD1[2:0]	RW
10:8	APLLOD0	APLL post VCO divider0 OD0 = APLLOD0[2:0]	RW
7	A_DSMPD	Power Down Delta-Sigma Modulator 0 - DSM is active 1 - DSM is power down	RW
6	A_PHASEPD	Power down 4 phase clock generator	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		0 - active 1 - power down	
5	A_POSTDIVPD	PLL post divide power down 0 - active 1 - power down	R
4	A_VCOPD	VCO output Power Down 0 - active 1 - power down	RW
3	APLL_ON	PLL ON Flag. 0: PLL is off or not stable 1: PLL is on and stable	R
2	ALOCK	When change stable , alock bit is set to 1 . Stable Flag bit .	R
1	Reserved	Writing has no effect, read as zero.	R
0	APLLEN	APLL Enable. When APLLEN is set to 1, APLL starts to lock phase. After APLL stabilizes, APLL_ON bit is set.	RW

11.1.2.3 MPLL Control Register(CPMPCR,0x14)

The MPLL Control Register (CPMPCR) is a 32-bit read/write register, which controls PLL multiplier, on/off state and stabilize time. It is initialized to 0x99009020 only by any reset. Only word access can be used on CPMPCR.

	CPMPCR																															BASE+0x14
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MPLLM												MPLLN						MPLLOD1			MPLLOD0			M_DSMPD	M_PHASEPD	M_POSTDIVPD	M_VCOPD	MPLL_ON	MLOCK	Reserved	MPLLEN
RST	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	1	1	1	0	0	0	0	0	0

Bits	Name	Description	RW
31:20	MPLLM	MPLL feedback 12-bit multiplication factor NF = MPLLM[11:0]	RW
19:14	MPLLN	MPLL input reference 6-bit divider. NR = MPLLN[5:0]	RW
13:11	MPLLOD1	MPLL post VCO divider1 OD1 = MPLLOD1[2:0]	RW
10:8	MPLLOD0	MPLL post VCO divider0 OD0 = MPLLOD0[2:0]	RW
7	M_DSMPD	Power Down Delta-Sigma Modulator	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		0 - DSM is active 1- DSM is power down	
6	M_PHASE PD	Power down 4 phase clock generator 0 - active 1- power down	RW
5	M_POSTDI VPD	PLL post divide power down 0 - active 1 - power down Note :The bit be connected to 1'b0 in clkgen's RTL, so there isn't power down function.	R
4	M_VCOPD	VCO output Power Down 0 - active 1- power down	RW
3	MPLL_ON	PLL ON Flag. 0: PLL is off or not stable 1: PLL is on and stable	R
2	ALOCK	When change stable , alock bit is set to 1 . Stable Flag bit .	R
1	Reserved	Writing has no effect, read as zero.	R
0	MPLLEN	MPLL Enable. When MPLLEN is set to 1, MPLL starts to lock phase. After MPLL stabilizes, MPLL_ON bit is set.	RW

11.1.2.4 EPLL Control Register(CPEPCR,0x18)

The EPLL Control Register (CPEPCR) is a 32-bit read/write register, which controls PLL multiplier, on/off state and stabilize time. It is initialized to 0x99009020 only by any reset. Only word access can be used on CPEPCR.

	CPVPCR																															BASE+0x0018
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EPLLM												EPLLN						EPLLOD1			EPLLOD0			E_DSMPD	E_PHASEPD	E_POSTDIVPD	E_VCOPD	EPLL_ON	ELOCK	Reserved	EPLLEN
RST	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	1	1	1	0	0	0	0	0	0

Bits	Name	Description	RW
31:20	EPLLM	VPLL feedback 12-bit multiplication factor NF = EPLLM[11:0]	RW
19:14	EPLLN	VPLL input reference 6-bit divider. NR = VPLLN[5:0]	RW
13:11	EPLLOD1	VPLL post VCO divider1	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		OD1 = VPLLOD1[2:0]	
10:8	EPLLOD0	VPLL post VCO divider0 OD0 = VPLLOD0[2:0]	RW
7	E_DSMPD	Power Down Delta-Sigma Modulator 0 - DSM is active 1- DSM is power down	RW
6	E_PHASEPD	Power down 4 phase clock generator 0 - active 1- power down	RW
5	E_POSTDIVPD	PLL post divide power down 0 - active 1 - power down	R
4	E_VCOPD	VCO output Power Down 0 - active 1- power down	RW
3	EPLL_ON	PLL ON Flag. 0: PLL is off or not stable 1: PLL is on and stable	R
2	ELOCK	When change stable , alock bit is set to 1 . Stable Flag bit .	R
1	Reserved	Writing has no effect, read as zero.	R
0	EPLLEN	EPLL Enable. When EPLLEN is set to 1, EPLL starts to lock phase. After VPLL stabilizes, EPLL_ON bit is set.	RW

11.1.2.5 APLL FRAC Register(CPAPACR,0x84)

The APLL FRAC Register (CPAPACR) is a 32-bit read/write register, which controls PLL Fractional value. It is initialized to 0x00000000 only by any reset. Only word access can be used on CPAPACR.

	CPAPACR																															BASE+0x0084
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								FRAC																							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:24	Reserved	Writing has no effect, read as zero.	R
23:0	FRAC	Fractional part of the APLL feedback divide value controlled by the Delta-Sigma modulator. Total feedback divide value is (FBDIV +	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		FRAC/2^{24}).	

11.1.2.6 MPLL FRAC Register(CPMPACR,0x88)

The MPLL FRAC Register (CPMPACR) is a 32-bit read/write register, which controls PLL Fractional value. It is initialized to 0x00000000 only by any reset. Only word access can be used on CPMPACR.

	CPMPACR																															BASE+0x0088
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								FRAC																							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:24	Reserved	Writing has no effect, read as zero.	R
23:0	FRAC	Fractional part of the MPLL feedback divide value controlled by the Delta-Sigma modulator. Total feedback divide value is (FBDIV + FRAC/2^{24}).	RW

11.1.2.7 EPLL FRAC Register(CPEPACR,0x8c)

The EPLL FRAC Register (CPEPACR) is a 32-bit read/write register, which controls PLL Fractional value. It is initialized to 0x00000000 only by any reset. Only word access can be used on CPEPACR.

	CPEPACR																															BASE+0x008c
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								FRAC																							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:24	Reserved	Writing has no effect, read as zero.	R
23:0	FRAC	Fractional part of the EPLL feedback divide value controlled by the Delta-Sigma modulator. Total feedback divide value is (FBDIV +	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		FRAC/2^{24}).	

11.1.3 PLL Operation

The PLL developed as a macro cell for clock generator. It can generate a stable high-speed clock from a slower clock signal. The output frequency is adjustable from 40Mhz to 2400MHz. The PLL integrates a phase frequency detector (PFD), a low pass filter (LPF), a voltage controlled oscillator (VCO) and other associated support circuitry. All fundamental building blocks as well as fully programmable dividers are integrated on the core. It is useful for clock multiplication of stable crystal oscillator sources and for de-skew clock signals.

The PLL block diagram is shown in following figure:

Figure 11-1 Block Diagram of PLL

11.1.3.1 PLL Configuration

PLL Divider Value Setting

There are 3 divider values (N, M and NO) to set the PLL output clock frequency CLKOUT: The PLL output frequency, FOUT, is determined by the ratio set between the value set in the input divider and the feedback divider. PLL output frequency FOUT is calculated from the following equations:

FBDIV = PLLM ;

REFDIV = PLLN ;

POSTDIV2= PLLOD0;

POSTDIV1 = PLLOD1;

FVCO = FREF * FBDIV / REFDIV

FOUTPOSTDIV = FVCO / POSTDIV2/ POSTDIV1

FREF range between 1M -800M

FVCO should between600M – 2400M; 600M is the lowest power mode, while 2400M is the lowest gitter mode

FOUTPOSTDIV between 12M - 2400M

Note0：POSTDIV1 should always be programmed to be greater than or equal to

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

POSTDIV2

Not:1: PLLM, PLLN, PLLOD0 and PLLOD1 should not be set 0.

Note2：when you want to change the frequency of any PLL, you should disable the PLL first and after rewrite the FBDIV, **REFDIV, POSTDIV2 and POSTDIV1, then you can enable the PLL again.**

11.1.4 Main Clock Division Change Sequence

Main clock (CCLK, L2CLK, H2CLK, PCLK) frequencies can be changed separately or simultaneously by changing division ratio. Following conditions must be obeyed:

1 the frequency of CCLK must be 1,2,3 or 4 times of the frequency of L2CLK
2 the frequency of H2CLK must be 1 or 2 times of the frequency of PCLK

Don't violate this limitation, otherwise unpredictable error may occur.

Important Note: When CPU enters sleep mode, the APLLEN must be set to 1.

11.2 Power Manager

In the Low-Power mode, part or whole processor is halted. This will reduce power consumption. The Power Management Controller contains low-power mode control and reset sequence control.

11.2.1 Low-Power Modes and Function

The processor supports six low-power modes and function:

- NORMAL mode
  In Normal mode, all peripherals and the basic blocks including power management block, the CPU core, the bus controller, the memory controller, the interrupt controller, DMA, and the external master may operate completely. But, the clock to each peripheral, except the basic blocks, can be stopped selectively by software to reduce the power consumption.

- IDLE mode
  In IDLE mode, the clock to the CPU core is stopped except the bus controller, the memory controller, the interrupt controller, and the power management block. To exit the IDLE mode, the any interrupts should be activated.

- IDLE power down mode
  In IDLE power down mode, on the basic of idle mode, the CPU core will also power down.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

- SLEEP mode

  In SLEEP mode, all clocks except RTC clock are disabled. PLL is disabled also. SLEEP mode is canceled by reset or interrupt. When SLEEP mode is canceled, PLL is restarted , the PLL needs clock stabilization time (PLL lock time). This PLL stabilization time is automatically inserted by the internal logic with lock time count register. and all clocks start operating after PLL stability time.

- CLOCK GATE function

  CLOCK GATE function is used to gate specified on-chip module when it is not used. Set specified CLKG0~31 bits in CLKGR will enter specified CLK gate function. CLOCK gate function is canceled by reset or clearing specified bits in CLKGR0/1 to 0.

- Power down Mode

  In order to reduce power leakage, software may shut down power supply for no used device. When system enters into SLEEP mode, the software may shut down power for core according to OPCR.PD bit.

11.2.2 Register Description

All PMC register 32bit access address is physical address.

Table 11-3 Power/Reset Management Controller Registers Configuration

Name	description	RW	Initial Value	Offset Address	Access Size
LCR	Low Power Control Register	RW	0x00000000	0x0004	32
PSWC0ST	Power Switch Chain0 Start Time	RW	0x00000000	0x0090	32
PSWC1ST	Power Switch Chain1 Start Time	RW	0x00000000	0x0094	32
PSWC2ST	Power Switch Chain2 Start Time	RW	0x00000000	0x0098	32
PSWC3ST	Power Switch Chain3 Start Time	RW	0x00000000	0x009c	32
SRBC	Soft Reset and Bus Control Register	RW	0x00000000	0x00C4	32
SLBC	Sleep Boot Control Register	RW	0x00000000	0x00C8	32
SLPC	Sleep PC Register	RW	0x????????	0x00CC	32
CLKGR0	Clock Gate Register0	RW	0x47FFFFE0	0x 0020	32
CLKGR1	Clock Gate Register1	RW	0x37FFFFFF	0x 0028	32
MEMPD0	Sram power down Register0	RW	0x00000000	0x00F8	32
MEMPD1	Sram power down Register1	RW	0x00000000	0x00FC	32
OPCR	Oscillator and Power Control Register	RW	0x10801500	0x 0024	32
MESTSEL	asnyc handshake control register	RW	0x00000000	0x00EC	32

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

11.2.2.1 Low Power Control Register(LCR,0x04)

The Low Power Control Register (LCR) is a 32-bit read/write register that controls low-power mode status. It is initialized to 0x00000000 by any reset.

	LCR																															BASE+0x04
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved												PST												Reserved			PD_IDLES	Reserved		LPM	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:20	Reserved	Write has no effect, read as 0.	R
19:8	PST	Power stability Time. Specifies the Power stabilize time by unit of RTCCLK (approximate 32kHz) cycles.	RW
7:5	Reserved	Write has no effect, read as 0.	R
4	PD_IDLES	0: CPU core not enter power down state 1: CPU core enter power down state	R
3:2	Reserved	Write has no effect, read as 0.	R
1:0	LPM	Low Power Mode. Specifies which low-power mode will be entered when SLEEP instruction is executed. Bit 1~0: **00**: IDLE mode will be entered when SLEEP instruction is executed **01**: SLEEP mode will be entered when SLEEP instruction is executed **10**: IDEL mode , CPU core will be power gated when SLEEP instruction is executed	RW

11.2.2.2 Power Switch Chain0 Start Time Register(PSWC0ST,0x90)

	PSWC0ST																															0x90
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				PSWC0ST											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

11.2.2.3 Power Switch Chain1 Start Time Register(PSWC1ST,0x94)

	PSWC1ST																															0x94
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				PSWC1ST											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

11.2.2.4 Power Switch Chain2 Start Time Register(PSWC2ST,0x98)

	PSWC2ST																															0x98
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				PSWC2ST											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

11.2.2.5 Power Switch Chain3 Start Time Register(PSWC3ST,0x9C)

	PSWC3ST																															0x1000009C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				PSWC3ST											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

NOTE: The Start Time by the unit of PCLK cycles.

11.2.2.6 Clock Gate Register(CLKGR,0x20)

The Clock Gate Register (CLKGR) is a 32-bit read/write register that controls the CLOCK GATE function of peripherals. It is reset to 0x07FFFF10.

	CLKGR																															BASE+0x20
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CLKGR																															
RST	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:0	CLKGR	Clock gate Bits. Controls the clock supplies to some peripherals. If set, clock supplies to associated devices are stopped, and registers of the device cannot be accessed also. The reset value of this register reflects the clock gate information of the relative modules. RST 0: After reset period, the clock is not stopped. RST 1: After reset period, the clock is stopped.	RW

Bit	Module	Description
31	DDR	If set, gate the clock.
30	Reseved	
29	AHB0	If set, gate the clock.
28	APB0	If set, gate the clock.
27	RTC	If set, gate the clock.
26	Reseved	
25	Reseved	
24	AES	If set, gate the clock.
23	LCD	If set, gate the clock.
22	CIM	If set, gate the clock.
21	PDMA	If set, gate the clock.
20	OST	If set, gate the clock.
19	SSI0	If set, gate the clock.
18	TCU	If set, gate the clock.
17	DTRNG	If set, gate the clock.
16	UART2	If set, gate the clock.
15	UART1	If set, gate the clock.
14	UART0	If set, gate the clock.
13	SADC	If set, gate the clock.
12	Reseved	
11	AUDIO	If set, gate the clock.
10	SSI_SLV	If set, gate the clock.
9	reserved	
8	I2C1	If set, gate the clock.
7	I2C0	If set, gate the clock.
6	Reseved	
5	MSC1	If set, gate the clock.
4	MSC0	If set, gate the clock.
3	OTG	If set, gate the clock.
2	SFC	If set, gate the clock.
1	EFUSE	If set, gate the clock.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		0	NEMC	If set, gate the clock.		

Note`: you can use XXCDR.XX_STOP, CLKGR.XX or SRBC.XX_STP to stop XX module's clk, and when CLKGR.XX or SRBC.XX_STP is set high , CPU can turn into sleep mode successfully, but if only set XXCDR.XX_STOP high, CPU may not turn into sleep mode, because XX module can not give out stop_ack when clk is stopped; CPM will not wait for XX module's stop_ack if you stop it's clk by set CLKGR.XX.

Note2: Scc's clk is 1/8 of exclk.

11.2.2.7 Clock Gate Register1(CLKGR1,0x28)

	CLKGR1																															BASE+0x28
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CLKGR1																															
RST	0	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Name	Description	RW
31	Reserved		RW
30	ARB		RW
29	Reserved		RW
28	MIPI_CSI	If set, gate the clock.	RW
27	Reserved		RW
26	INTC	If set, gate the clock.	RW
25	Reserved		RW
24	Reserved		RW
23	GMAC0	If set, gate the clock.	RW
22	Reseved		RW
21	Reseved		RW
20	Reseved		RW
19	Reseved		RW
18	Reseved		RW
17	Reseved		RW
16	UART3	If set, gate the clock.	RW
15	Reseved		RW
14	Reseved		RW
13	Reseved		RW
12	Reseved		RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

11	Reseved		RW
10	Reseved		RW
9	I2S0_dev_tclk	If set, gate the clock.	RW
8	I2S0_dev_rclk	If set, gate the clock.	RW
7	Reseved		RW
6	HASH	If set, gate the clock.	RW
5	PWM	If set, gate the clock.	RW
4	Reseved		RW
3	Reseved		RW
2	CDBUS	If set, gate the clock.	RW
1	CAN1	If set, gate the clock.	RW
0	CAN0	If set, gate the clock.	RW

11.2.2.8 Mest Sel Register(MESTSEL,0xEC)

	MESTSEL																															BASE+0xEC
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Mux-priority																				Reserved						TST5	TST4	TST3	TST2	TST1	TST0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:12	Mux-priority	Dpu-mux-priority 31:24 null 23:22 lcd 21:20 cim 19:15 null 14 slave 13:12 null	RW
11:7	Reserved	Write has no effect, read as 0.	R
5	TST5	AHB2 and DDR	RW
4	TST4	LCD and DDR	RW
3	TST3	CPU and DDR	RW
2	TST2	AHB0 and APB0	RW
1	TST1	CPU and AHB0	RW
0	TST0	CPU and AHB2	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

11.2.2.9 Soft Reset and Bus Control Register (SRBC,0xC4)

The Soft Reset and Bus Control Register is a 32-bit read/write register that control some module reset and bus transmission. It is initialized to 0x0000000 0by reset.Remember GMAC's soft reset is in MPHYC.SOFT_RST.

	SRBC																															BASE+0xC4
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved												LCD_SR	CIM_SR	Reserved		CAN0_SR	CAN1_SR	CDBUS_SR	OTG_SR	HASH_SR	AES_SR	Reserved	AUDIO_SR	DDR_STOP	Reserved					CPU_ACK	DDR_ACK
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:20	Reserved	Write has no effect, Read as 0.	R
19	LCD_SR	LCD soft reset.	RW
18	CIM_SR	CIM soft reset.	RW
17:16	Reserved	Write has no effect, Read as 0.	R
15	CAN0_SR	CAN0 soft reset.	RW
14	CAN1_SR	CAN1 soft reset.	RW
13	CDBUS_SR	CDBUS soft reset.	RW
12	OTG_SR	OTG soft reset.	RW
11	HASH_SR	HASH soft reset.	RW
10	AES_SR	AES soft reset.	RW
9	Reserved	Write has no effect, Read as 0.	R
8	AUDIO_SR	AUDIO soft reset.	RW
7	DDR_STOP	DDR CLK Stop Req.	RW
6:2	Reserved	Write has no effect, Read as 0.	R
1	CPU_ACK	CPU CLK Stop Ack.	R
0	DDR_ACK	DDR CLK Stop Ack.	R

11.2.2.10 Memory Power Down Control Register0(MEMORY_PD0,0xF8)

The Memory Power Down Control Register 0 is a 32-bit read/write register

	MEMORY_PD0																															BASE + 0xF8
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MPDCR																															

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:30	Reserved		RW
29	CDBUS		RW
28:27	Reserved		RW
26	PWM		RW
25	GMAC		RW
24	USB		RW
23	SFC		RW
22	MSC1		RW
21	MSC0		RW
20	AES		RW
19	PDMA_SLP		RW
18	PDMA_SEC		RW
17	PDMA		RW
16	NEMC		RW
15:7	Reserved		RW
6	AIC		RW
5	SSI_SLV		RW
4	SSI0		RW
3	UART3		RW
2	UART2		RW
1	UART1		RW
0	UART0		RW

Noter: whe shut down these module SRAM, the module clock mustn't be gated.

11.2.2.11 Memory Power Down Control Register1 (MEMORY_PD1,0xFC)

The Memory Power Down Control Register 1 is a 32-bit read/write register

	MEMORY_PD1																															BASE + 0xFC
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MPDCR1																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:6	Reserved		RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

5	CIM		RW
4	DPU		RW
3	DDR_CH6		RW
2	DDR_CH5		RW
1	DDR_CH3		RW
0	DDR_TOP		RW

11.2.2.12 Sleep Boot Control Register (SLBC,0xC8)

The Sleep Boot Control Register is a 32-bit read/write register that control sleep boot mode.It is initialized to 0x0000000 0by reset.

	SLBC																															0xC8
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															SLBC
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved		R
0	SLBC	0: Sleep Mode Wake up Boot Process is same with any reset. 1: Sleep Mode Wake up Boot Process is jumped to SLPC, don't care Boot_Sel. The bit is only valid When shut down P0 in Sleep Mode	RW

11.2.2.13 Sleep PC Register (SLPC,0xCC)

The Sleep PC Register is a 32-bit read/write register that control sleep mode jump address.

	SLPC																															0xCC
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SLPC																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:0	SLPC	When SLBC is 1, sleep boot is jumped to SLPC, not true boot as any reset. The register is only valid When shut down P0 in Sleep Mode and SLBC is set high.	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

11.2.2.14 Oscillator and Power Control Register (OPCR,0x24)

The Oscillator and Power Control Register is a 32-bit read/write register that specifies some special controls to oscillator and analog block. It is initialized to 0x00801500 by reset.

	OPCR																															BASE+0x24
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IDLE_DIS	MASK_INT	Reserved	Gate_sclka_bus	Reserved	L2C_PD	Reserved	REQ_MODE	Gate_usbphyclk				O1ST												SPENDN0	Reserved		O1SE	PD	ERCS	BUS_MODE	Reserved
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	IDLE_DIS	0: when CPU enters idle mode, CPU clock is stopped 1: When CPU enters idle mode, CPU clock is not stopped	RW
30	MASK_INT	0: interrupt not mask 1: interrupt masked When enters sleep/idle mode, cpu should set MASK_INT 1, hardware will clear.	RW
29	Reserved		R
28	GATE_SCLKA_BUS	Gate SCLK_A for AHB0 AHB2 DDR	RW
27	Reserved	Write has no effect, read as 0	RW
26	L2C_PD	L2C power down select 0: no power down l2c in sleep mode 1: power down l2c in sleep mode	RW
25	Reserved		
24	REQ_MODE	0: Before go into sleep mode, CPM send stop req signal to relatvie modules in SRBC 1: Before go into sleep mode, CPM doesn't send stop req signal to those modules When DDR enters retention mode, software should be set the bit to 1	RW
23	gate_usbphy_clk	1:gate usb phy clk12m 0:not gate usb phy clk12m	RW
22	Nemc_rom_clr_ds_en	0: after sleep mode return, hardware don't clear rom DS bit 1: after sleep mode return, hardware clear rom DS bit	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

21	Pdma_ram_clr_en	0: after sleep mode return, hardware don't clrear PDMA TCSM bank0~3 SD bit 1: after sleep mode return, hardware clrear PDMA TCSM bank0~3 SD bit	RW
20	Ddr_clr_sd_en	0: after sleep mode return, hardware don't clear ddr ram SD bit 1: after sleep mode return, hardware clear DDR ram SD bit	RW
19:8	O1ST	EXCLK Oscillator Stabilize Time. This filed specifies the EXCLK oscillator stabilize time by unit of 16 RTCCLK periods (oscillator stable time O1ST × 16 / 32768) cycles. It is initialized to H'15.	RW
7	SPENDN0	force USB PHY to enter suspend mode when OTG is enable. 0: USB PHY has forced to entered SUSPEND mode 1: USB PHY hasn't forced to entered SUSPEND mode	RW
6	Reserved	Write has no effect, Read as 0	R
5	CIM_MCLK_gate	0: don't gate CIM_MCLK_o 1: gate CIM_MCLK_o	RW
4	O1SE	EXCLK Oscillator Sleep Mode Enable. This filed controls the state of the EXCLK oscillator in Sleep mode. 0: EXCLK oscillator is disabled in Sleep mode 1: EXCLK oscillator is enabled in Sleep mode	RW
3	PD	0: no power down cpu_core in sleep mode 1: power down cpu_core in sleep mode	RW
2	ERCS	EXCLK/512 clock and RTCLK clock selection. 0: select EXCLK/512 division ration clock 1: select RTCLK clock the clock only output to CPM INTC SSI TCU etc.	RW
1	BUS_MODE	The default value is 0 When the value is 1, the BUS access is accelerated.	RW
0	reserved	Write has no effect, Read as 0	R

Note: Before you want to power down cpu buy set PD in OPCR, you need to reduce cpu's frequency as the same as L2C's freq; or else unpredictable error will accurs when CPU is waken up again.

11.2.3 IDLE Mode

In normal mode, when LPM bits in LCR are 0 and SLEEP instruction is executed, the processor enters idle mode. CPU is halted but its register contents are retained All critical application must be finished and peripherals must be configured to generate interrupts when they need CPU attention.

The procedure of entering sleep mode is shown blow:

1 Set LPM bits in LCR to 0.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

2 Executes SLEEP instruction.
3 When current operation of CPU core has finished and CPU core is idle, CCLK supply to CPU core is stopped.

IDLE mode is exited by an interrupt (IRQ or on-chip devices) or a reset.

11.2.4 SLEEP Mode

In normal mode, when LPM bits in LCR is 1 and SLEEP instruction is executed, the processor enter SLEEP mode. CPU and on-chip devices are halted, except some wakeup-logic. PLL is shut off. Clock output from CKO pin is also stopped. SDRAM content is preserved by driving into self-refresh state. CPU registers and on-chip devices registers contents are retained.

Before enter SLEEP mode, software should ensure that all peripherals are not running. The procedure of entering SLEEP mode is shown blow:

1 Set LPM bit in LCR to 1.
2 Execute a SLEEP instruction.
3 When current access on system bus complete, the arbiter will not grant any following request. EMC will drive SDRAM from auto-refresh mode to self-refresh mode.
4 When system bus is idle state and SDRAM is self-refresh mode, internal clock supplies are stopped.
5 SLEEP mode can be exited by an interrupt (IRQ or on-chip devices), WDT reset or a poweron reset via the RESETP pin.
6 If SLEEP mode can be waked up by OTG interrupt, before entry SLEEP mode, select USBRDT.Resume_speed; set OPCR.SPENDN0=0; set OPCR.gate_usbphy_clk=1; set OPCR.ERCS=1, use rtc clock; set USBRDT.Resume_inten=1, enable USB resume interrupt; unmask OTG interrupt by INTC.

11.3 Reset Control Module

11.3.1 Register Description

All RCM register 32bit access address is physical address.

Name	description	RW	Initial Value	Address	Access Size
RSR	Reset Status Register	RW	0x????????	0x0008	32

11.3.1.1 Reset Status Register (RSR)

The Reset Status Register (RSR) is a 32-bit read/write register which records last cause of reset. Each RSR bit is set by a different source of reset. Please refer to Reset Sequence Control for reset sources description.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	RSR																															BASE+0x0008
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												HR	P0R	WR	PR
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?

Bits	Name	Description	RW
31:4	Reserved	Writing has no effect, read as zero.	R
3	HR	Hibernate Reset. Software can only write 0,Write 1 will be ignored	RW
2	P0R	P0 power up Reset. It indicates that P0 has been shut down, now it has been power up. When P0 reset is detected, P0R is set and remains set until software clears it or another reset occurs. This bit can only be written with 0. Write with 1 will be ignored. 0: P0 reset has not occurred since the last time the software clears this bit 1: P0 reset has occurred since the last time the software clears this bit	
1	WR	WDT Reset. When a WDT reset is detected, WR is set and remains set until software clears it or another reset occurs. This bit can only be written with 0. Write with 1 will be ignored. 0: WDT reset has not occurred since the last time the software clears this bit 1: WDT reset has occurred since the last time the software clears this bit	RW
0	PR	Power On Reset. When a power-on reset via PRESET pin is detected, PR is set and remains set until software clears it or another reset occurs. This bit can only be written with 0. Write with 1 is ignored. 0: Power on reset has not occurred since the last time the software clears this bit 1: Power on reset has occurred since the last time the software clears this bit	RW

11.3.2 Power On Reset

Power on reset is generated when PRESET pin is driven to low. Internal reset is asserted immediately. All pins return to their reset states. The Power on reset is extended to 40MS.

PRESET pin must be held low until power stabilizes and the EXCLK oscillator stabilize. CPU and peripherals are clocked by EXCLK oscillator output directly. PLL is reset to off state. All

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

internal modules are initialized to their predefined reset states.

11.3.3 WDT Reset

WDT reset is generated when WDT overflow. Internal reset is asserted within two RTCCLK cycles. All pins return to their reset states.

Then WDT reset source is cleared because of internal reset. The internal reset is asserted for about 10 milliseconds. CPU and peripherals are clocked by EXCLK oscillator output directly. PLL is reset to off state.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

12 Timer/Counter Unit

12.1 Overview

The TCU include two Genera Purpose Timer, four Periodical Interrupt Timer and four Quad Timer.

12.2 Features

- Include 0,1,2,3,4,5,6 and 7 channel;
- Support the below modes:
  - General Mode: counter counts when clock posedge or negedge or double.
  - Gate Mode: counter counts when gate is 0.
  - Direction Mode: counter add or sub because of control signal.
  - Quadrature Mode: counter counts because of the quadrature input.
    - When the input control signal1 and signal2 are orthogonal, the counter will add 1 for each time. Otherwise, the value of counter will be unchanged.
  - Pos Mode: counter starts count from 0 when capture a posedge or a negedge of the control signal.
  - Capture Mode: counter counts a period and output high level time and the whole period time.
    - Similar to the Pos Mode, the counter starts count from 0 when capture a posedge or a negedge of the control signal, and the capture time depends on the value of CAPTURE_NUM of CAPCR register.
    - The CAPVR register will record the whole time and high level time of the capture period.
- Support filter and gpio store function.
- Support 1/4/16/64/256/1024 prescale for EXTAL(inner clock).
- Support EXTAL(inner clock) and input clock
- Can't work on sleep mode.

12.3 Pin Description

Table 12-1 PWM Pins Description

Name	I/O	Description
Gpio_input[15:0]	Input	Use to control counter.
Gpio_store_input	Input	Use to save tcu counter

12.4 Register Description

Following chapter will descript the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

2. Register read/write attribute
   R - Read only
   W - Write only
   RW - read and write
   RCW - read and write, but clear to 0 by read
   RSW - read and write, but set to 1 by read
   RWC - read and write, clear to 0 by write 1, write 0 has no effect
   RWS - read and write, set to 1 by write 1, write 0 has no effect
   RC - read only, and clear to 0 by read
   RS - read only, and set to 1 by read
   SPEC - special access method, relate to its description
3. Reset Value
   1 - reset to 1
   0 - reset to 0
   ? - value unknown after reset

12.4.1 Register Memory Map

Table 12-2 Registers Memory Map Base Address

Name	Base	Description
TCU	0x10002000	Address Base of TCU

The Timer/Counter Unit is controlled by a set of registers that the application configures before every operation. The following table lists all the registers.

Table 12-3 TCU Registers Map (n = 0~7)

Name	Description	RW	Reset Value	Address offset
TER	Enable timer counter	R	0x0000_0000	0x010
TESR	Set enable	W	0x0000_?00?	0x014
TECR	Clear enable	W	0x0000_?00?	0x018
TSR	Stop timer counter	R	0x0000_0000	0x01C
TSSR	Set stop	W	0x000?_?00?	0x02C
TSCR	Clear stop	W	0x000?_?00?	0x03C
TFR	Comparison flag	R	0x0000_0000	0x020
TFSR	Set comparison flag	W	0x000?_?00?	0x024
TFCR	Clear comparison flag	W	0x000?_?00?	0x028
TMR	Interrupt mask	R	0x010F_800F	0x030
TMSR	Set interrupt mask	W	0x000?_?00?	0x034
TMCR	Clear interrupt mask	W	0x000?_?00?	0x038
TDFRn	Channel n full data value	RW	0x0000_????	0x040 + n * 0x10
TDHRn	Channel n half data value	RW	0x0000_????	0x044 + n * 0x10
TCNTn	Channel n timer counter	RW	0x0000_????	0x048 + n * 0x10
TCRn	Channel n timer control	RW	0x0000_0000	0x04C + n * 0x10

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

CAPCRn	Channel n capture control	RW	0x0000_0000	0x0C0 + n * 0x04
CAPVR0	Channel 0 capture value	RW	0x????_????	0x0E0
CAPVR1	Channel 1 capture value	RW	0x????_????	0x0E4
CAPVR2	Channel 2 capture value	RW	0x????_????	0x0E8
CAPVR3	Channel 3 capture value	RW	0x????_????	0x0EC
FIRVRn	Channel n filter counter value	RW	0x0000_0000	0x1A0 + n * 0x04
TSFR	Store flag	R	0x0000_0000	0x200
TSFSR	Set store falg	W	0x0000_0000	0x204
TSFCR	Clear store flag	W	0x0000_0000	0x208
TSMR	Store interrupt mask	R	0x0000_00FF	0x210
TSMSR	Set store interrupt mask	W	0x0000_0000	0x214
TSMCR	Clear store interrupt mask	W	0x0000_0000	0x218
TSVRn	Channel n value of stored conter	RW	0x0000_0000	0x220 + n * 0x04
TSFVRn	Channel n value of stored filter conter	RW	0x0000_0000	0x240 + n * 0x04

12.4.2 Register and Fields Description

12.4.2.1 Timer Counter Enable Register (TER, 0x010)

The TER is a 16-bit read-only register. It contains the counter enable control bits for each channel. It is initialized to 0x0000 by any reset. It can only be set by register TESR and TECR. Since the timer enable control bits are located in the same addresses, two or more timers can be set at the same time.

THIS ENABLE IS ONLY USE IN COUNTER_MODE

	TER																															Base + 0x010
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																OSTEN	Reserved							TCEN7	TCEN6	TCEN5	TCEN4	TCEN 3	TCEN 2	TCEN 1	TCEN 0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
15	OSTEN	Enable the counter in OST. 0: Stop counting up 1: Begin counting up	R
14:9	Reserved	Writing has no effect, read as zero.	R
7	TCEN 7	Enable the counter in timer 7. 0: Stop counting up 1: Begin counting up	R
6	TCEN 6	Enable the counter in timer 6.	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		0: Stop counting up 1: Begin counting up	
5	TCEN 5	Enable the counter in timer 5. 0: Stop counting up 1: Begin counting up	R
4	TCEN 4	Enable the counter in timer 4. 0: Stop counting up 1: Begin counting up	R
3	TCEN 3	Enable the counter in timer 3. 0: Stop counting up 1: Begin counting up	R
2	TCEN 2	Enable the counter in timer 2. 0: Stop counting up 1: Begin counting up	R
1	TCEN 1	Enable the counter in timer 1. 1: Begin counting up 0: Stop counting up	R
0	TCEN 0	Enable the counter in timer 0. 0: Stop counting up 1: Begin counting up	R

12.4.2.2 Timer Counter Enable Set Register (TESR, 0x014)

The TESR is a 16-bit write-only register. It contains the counter enable set bits for each channel. Since the timer enable control set bits are located in the same addresses, two or more timers can be started at the same time.

	TESR																															Base + 0x014
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																OSTST	Reserved							TCST 7	TCST 6	TCST 5	TCST 4	TCST 3	TCST 2	TCST 1	TCST 0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
15	OSTST	Set OSTEN bit of TER. 0: Ignore 1: Set OSTEN bit to 1	W
14:8	Reserved	Writing has no effect, read as zero.	RW
7	TCST 7	Set TCEN 7 bit of TER. 0: Ignore 1: Set TCEN 7 bit to 1	W

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

6	TCST 6	Set TCEN 6 bit of TER 0: Ignore. 1: Set TCEN 6 bit to 1	W
5	TCST 5	Set TCEN 5 bit of TER. 0: Ignore 1: Set TCEN 5 bit to 1	W
4	TCST 4	Set TCEN 4 bit of TER. 0: Ignore 1: Set TCEN 4 bit to 1	W
3	TCST 3	Set TCEN 3 bit of TER. 0: Ignore 1: Set TCEN 3 bit to 1	W
2	TCST 2	Set TCEN 2 bit of TER. 0: Ignore 1: Set TCEN 2 bit to 1	W
1	TCST 1	Set TCEN 1 bit of TER. 0: Ignore 1: Set TCEN 1 bit to 1	W
0	TCST 0	Set TCEN 0 bit of TER. 0: Ignore 1: Set TCEN 0 bit to 1	W

12.4.2.3 Timer Counter Enable Clear Register (TECR, 0x018)

The TECR is a 16-bit write-only register. It contains the counter enable clear bits for each channel. Since the timer enable clear bits are located in the same addresses, two or more timers can be stoped at the same time.

	TECR																															Base + 0x018
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																OSTCL	Reserved							TCCL 7	TCCL 6	TCCL 5	TCCL 4	TCCL 3	TCCL 2	TCCL 1	TCCL 0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
15	OSTCL	Set OSTEN bit of TER. 0: Ignore 1: Set OSTEN 5 bit to 0	W
14:8	Reserved	Writing has no effect. Read as zero.	RW
7	TCCL 7	Set TCEN 7 bit of TER.	W

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		0: Ignore 1: Set TCEN 7 bit to 0	
6	TCCL 6	Set TCEN 6 bit of TER. 0: Ignore 1: Set TCEN 6 bit to 0	W
5	TCCL 5	Set TCEN 5 bit of TER. 0: Ignore 1: Set TCEN 5 bit to 0	W
4	TCCL 4	Set TCEN 4 bit of TER. 0: Ignore 1: Set TCEN 4 bit to 0	W
3	TCCL 3	Set TCEN 3 bit of TER. 0: Ignore 1: Set TCEN 3 bit to 0	W
2	TCCL 2	Set TCEN 2 bit of TER. 0: Ignore 1: Set TCEN 2 bit to 0	W
1	TCCL 1	Set TCEN 1 bit of TER. 0: Ignore 1: Set TCEN 1 bit to 0	W
0	TCCL 0	Set TCEN 0 bit of TER. 0: Ignore 1: Set TCEN 0 bit to 0	W

12.4.2.4 Timer Stop Register (TSR, 0x01C)

The TSR is a 32-bit read-only register. It contains the timer stop control bits for each channel, WDT and OST. It is initialized to 0x00000000 by any reset. It can only be set by register TSSR and TSCR. If set, clock supplies to timer n / WDT / OST is stopped, and registers of the timer / WDT / OST can not be accessed also.

	TSR																															Base + 0x01C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved															WDTS	OSTS	Reserved							STOP7	STOP6	STOP5	STOP4	STOP 3	STOP 2	STOP 1	STOP 0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:17	Reserved	Writing has no effect, read as zero.	R
16	WDTS	0: The clock supplies to WDT is supplied 1: The clock supplies to WDT is stopped	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

15	OSTS	0: The clock supplies to OST is supplied 1: The clock supplies to OST is stopped	R
14:8	Reserved	Writing has no effect, read as zero.	R
7	STOP 7	0: The clock supplies to timer 7 is supplied 1: The clock supplies to timer 7 is stopped	R
6	STOP 6	0: The clock supplies to timer 6 is supplied 1: The clock supplies to timer 6 is stopped	R
5	STOP 5	0: The clock supplies to timer 5 is supplied 1: The clock supplies to timer 5 is stopped	R
4	STOP 4	0: The clock supplies to timer 4 is supplied 1: The clock supplies to timer 4 is stopped	R
3	STOP 3	0: The clock supplies to timer 3 is supplied 1: The clock supplies to timer 3 is stopped	R
2	STOP 2	0: The clock supplies to timer 2 is supplied 1: The clock supplies to timer 2 is stopped	R
1	STOP 1	0: The clock supplies to timer 1 is supplied 1: The clock supplies to timer 1 is stopped	R
0	STOP 0	0: The clock supplies to timer 0 is supplied 1: The clock supplies to timer 0 is stopped	R

12.4.2.5 Timer Stop Set Register (TSSR, 0x02C)

The TSSR is a 32-bit write-only register. It contains the timer stop set bits for each channel, WDT and OST. Since the timer stop control set bits are located in the same addresses, two or more timers can be started at the same time.

	TSSR																															Base + 0x02C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved															WDTSS	OSTSS	Reserved							STPS7	STPS6	STPS5	STPS4	STPS 3	STPS 2	STPS 1	STPS 0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:17	Reserved	Writing has no effect, read as zero.	R
16	WDTSS	Set WDTS bit of TSR. 0: Ignore 1: Set WDTS bit to 1	W
15	OSTSS	Set OSTS bit of TSR. 0: Ignore 1: Set OSTS bit to 1	W

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

14:8	Reserved	Writing has no effect, read as zero.	R
7	STPS 7	Set STOP 7 bit of TSR. 0: Ignore 1: Set STOP 7 bit to 1	W
6	STPS 6	Set STOP 6 bit of TSR. 0: Ignore 1: Set STOP 6 bit to 1	W
5	STPS 5	Set STOP 5 bit of SR. 0: Ignore 1: Set STOP 5 bit to 1	W
4	STPS 4	Set STOP 4 bit of TSR. 0: Ignore 1: Set STOP 4 bit to 1	W
3	STPS 3	Set STOP 3 bit of TSR. 0: Ignore 1: Set STOP 3 bit to 1	W
2	STPS 2	Set STOP 2 bit of TSR. 0: Ignore 1: Set STOP 2 bit to 1	W
1	STPS 1	Set STOP 1 bit of TSR. 0: Ignore 1: Set STOP 1 bit to 1	W
0	STPS 0	Set STOP 0 bit of TSR. 0: Ignore 1: Set STOP 0 bit to 1	W

12.4.2.6 Timer Stop Clear Register (TSCR, 0x03C)

The TSCR is a 32-bit write-only register. It contains the timer stop clear bits for each channel, WDT and OST. Since the timer stop clear bits are located in the same addresses, two or more timers can be stop at the same time.

	TSCR																															Base + 0x03C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved															WDTSC	OSTSC	Reserved							STPC7	STPC6	STPC5	STPC4	STPC 3	STPC 2	STPC 1	STPC 0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:17	Reserved	Writing has no effect. Read as zero.	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

16	WDTSC	Clear WDTS bit of TSR. 0: Ignore 1: Clear WDTS bit to 0	W
15	OSTSC	Clear OSTS bit of TSR. 0: Ignore 1: Clear OSTS bit to 0	W
14:8	Reserved	Writing has no effect. Read as zero.	R
7	STPC 7	Clear STOP 7 bit of TSR. 0: Ignore 1: Clear STOP 7 bit to 0	W
6	STPC 6	Clear STOP 6 bit of TSR. 0: Ignore 1: Clear STOP 6 bit to 0	W
5	STPC 5	Clear STOP 5 bit of TSR. 0: Ignore 1: Clear STOP 5 bit to 0	W
4	STPC 4	Clear STOP 4 bit of TSR. 0: Ignore 1: Clear STOP 4 bit to 0	W
3	STPC 3	Clear STOP 3 bit of TSR. 0: Ignore 1: Clear STOP 3 bit to 0	W
2	STPC 2	Clear STOP 2 bit of TSR. 0: Ignore 1: Clear STOP 2 bit to 0	W
1	STPC 1	Clear STOP 1 bit of TSR. 0: Ignore 1: Clear STOP 1 bit to 0	W
0	STPC 0	Clear STOP 0 bit of TSR. 0: Ignore 1: Clear STOP 0 bit to 0	W

12.4.2.7 Timer Flag Register (TFR, 0x020)

The TFR is a 32-bit read-only register. It contains the comparison match flag bits for all the channels. It can also be set and cleared by register TFSR and TFCR. It is initialized to 0x0000_0000 by any reset.

	TFR																															Base + 0x020
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Reserved							HFLAGW	HFLAG 7	HFLAG 6	HFLAG 5	HFLAG 4	HFLAG 3	HFLAG 2	HFLAG 1	HFLAG 0	OSTFLAG	Reserved							FFLAG 7	FFLAG 6	FFLAG 5	FFLAG 4	FFLAG 3	FFLAG 2	FFLAG 1	FFLAG 0
RST	0	0	0	0	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:25	Reserved	Writing has no effect, read as zero.	R
24	HFALGW	HALF comparison match flag of WDT.(TCNT == THR) 0: Comparison not match 1: Comparison match pending of tcu_int[0] **Note:** THR: the half value of timer want to counter, refer to reg WDT_FULL (0x0) of Watchdog Timer. TCNT: the value of Timer Counter.	R
23:16	HFLAG 7~0	HALF comparison match flag. (TCNTn = =TDHRn) 0: Comparison not match 1: Comparison match pending of tcu_int[0] **Note:** TDHRn: the value of reg Timer Data HALF Register(n= 0~7).	R
15	OSTFLAG	OST comparison match flag. (OST1CNT= = OST1DFR) 0: Comparison not match 1: Comparison match pending of tcu_int[2] **Note:** OST1CNT: the value of OST Timer Counter register in Operating System Timer. OST1DFR:the value of OST Data FULL register in Operating Systerm Timer.	R
14:8	Reserved	Writing has no effect, read as zero.	R
7:0	FFLAG 7~0	FULL comparison match flag. (TCNTn == TDFRn) 0: Comparison not match 1: Comparison match pending of tcu_int[0] **Note:** TDFRn: the value of reg Timer Data FULL Register(n=0~7)	R

12.4.2.8 Timer Flag Set Register (TFSR, 0x024)

The TFSR is a 32-bit write-only register. It contains the comparison match flag set bits for all

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

the channels.

	TFSR																															Base + 0x024
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								HFST7	HFST6	HFST5	HFST4	HFST 3	HFST 2	HFST 1	HFST 0	OSTFST	Reserved							FFST7	FFST6	FFST5	FFST4	FFST 3	FFST 2	FFST 1	FFST 0
RST	0	0	0	0	0	0	0	0	?	?	?	?	?	0	0	?	?	0	0	0	0	0	0	0	?	?	?	?	?	0	0	?

Bits	Name	Description	RW
31:24	Reserved	Writing has no effect, read as zero.	R
23:16	HFST 7~0	Set HFLAG n bit of TFR. 0: Ignore 1: Set HFLAG n bit to 1	W
15	OSTFST	Set OSTFLAG n bit of TFR. 0: Ignore 1: Set OSTFLAG n bit to 1	W
14:8	Reserved	Writing has no effect, read as zero.	R
7:0	FFST 7~0	Set FFLAG n bit of TFR. 0: Ignore 1: Set FFLAG n bit to 1	W

12.4.2.9 Timer Flag Clear Register (TFCR, 0x028)

The TFCR is a 32-bit write-only register. It contains the comparison match flag clear bits for all the channels.

	TFCR																															Base + 0x028
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved							HFCLW	HFCL7	HFCL6	HFCL5	HFCL4	HFCL 3	HFCL 2	HFCL 1	HFCL 0	OSTFCL	Reserved							FFCL7	FFCL6	FFCL5	FFCL4	FFCL 3	FFCL 2	FFCL 1	FFCL 0
RST	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:25	Reserved	Writing has no effect, read as zero.	R
24	HFCLW	Clear HFLAG of WDT_THR. 0: Ignore 1: Clear FFLAG n bit to 0	W
23:16	HFCL 7~0	Clear HFLAG n bit of TFR. 0: Ignore 1: Clear FFLAG n bit to 0	W
15	OSTFCL	Clear OSTFLAG n bit of TFR.	W

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		0: Ignore 1: Clear OSTFLAG n bit to 0	
14:8	Reserved	Writing has no effect, read as zero.	R
7:0	FFCL 7~0	Clear FFLAG n bit of TFR. 0: Ignore 1: Clear FFLAG n bit to 0	W

12.4.2.10 Timer Mask Register (TMR, 0x30)

The TMR is a 32-bit read-only register. It contains the comparison match flag bits for all the channels. It is initialized to 0x003F003F by any reset. It can only be set by register TMSR and TMCR.

	TMR																															Base + 0x30
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved							HMASKW	HMASK7	HMASK6	HMASK5	HMASK4	HMASK 3	HMASK 2	HMASK 1	HMASK 0	OSTMASK	Reserved							FMASK7	FMASK6	FMASK5	FMASK4	FMASK 3	FMASK 2	FMASK 1	FMASK 0
RST	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bits	Name	Description	RW
31:25	Reserved	Writing has no effect, read as zero.	R
24	HMASKW	HALF mask for WDT. 0: Comparison match interrupt not mask 1: Comparison match interrupt mask Mask pending of tcu_int[0]	R
23:16	HMASK 7~0	HALF comparison match interrupt mask. 0: Comparison match interrupt not mask 1: Comparison match interrupt mask Mask pending of tcu_int[0]	R
15	OSTMASK	OST comparison match interrupt mask. 0: Comparison match interrupt not mask 1: Comparison match interrupt mask Mask pending of tcu_int[2]	R
14:8	Reserved	Writing has no effect, read as zero.	R
7:0	FMASK 7~0	FULL comparison match interrupt mask. 0: Comparison match interrupt not mask 1: Comparison match interrupt mask Mask pending of tcu_int[0]	R

12.4.2.11 Timer Mask Set Register (TMSR, 0x034)

The TMSR is a 32-bit write-only register. It contains the comparison match flag set bits for all

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

the channels.

	TMSR																															Base + 0x034
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved							HMSTW	HMST7	HMST6	HMST5	HMST4	HMST 3	HMST 2	HMST 1	HMST 0	OSTMST	Reserved							FMST7	FMST6	FMST5	FMST4	FMST 3	FMST 2	FMST 1	FMST 0
RST	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:25	Reserved	Writing has no effect, read as zero.	R
24	HMSKW	Set HMASK of WDT. 0: Ignore 1: Set HMASKW to 1	W
23:16	HMSK 7~0	Set HMASK n bit of TMR. 0: Ignore 1: Set HMASK n bit to 1	W
15	OSTMSK	Set OSTMASK n bit of TMR. 0: Ignore 1: Set OSTMASK n bit to 1	W
14:8	Reserved	Writing has no effect, read as zero.	R
7:0	FMSK 7~0	Set FMASK n bit of TMR. 0: Ignore 1: Set FMASK n bit to 1	W

12.4.2.12 Timer Mask Clear Register (TMCR, 0x38)

The TMCR is a 32-bit write-only register. It contains the comparison match flag clear bits for all the channels.

	TMCR																															Base + 0x38
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved							HMCLW	HMCL7	HMCL6	HMCL5	HMCL4	HMCL 3	HMCL 2	HMCL 1	HMCL 0	OSTMCL	Reserved							FMCL7	FMCL6	FMCL5	FMCL4	FMCL 3	FMCL 2	FMCL 1	FMCL 0
RST	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:25	Reserved	Writing has no effect. Read as zero.	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

24	HMCLW	Set HMASK of WDT. 0: Ignore 1: Set HMASKW to 0	W
23:16	HMCL 7~0	Set HMASK n bit of TMR. 0: Ignore 1: Set HMASK n bit to 0	W
15	OSTMCL	Set OSTMASK n bit of TMR. 0: Ignore 1: Set OSTMASK n bit to 0	W
14:8	Reserved	Writing has no effect. Read as zero.	R
7:0	FMCL 7~0	Set FMASK n bit of TMR. 0: Ignore 1: Set FMASK n bit to 0	W

12.4.2.13 Timer Data FULL Register (TDFRn, 0x040 + n * 0x10, n= 0~7)

This is a 16-bit read/write register. The comparison data FULL registers TDFRn is used to store the data to be compared with the content of the up-counter TCNTn. This register can be directly read and written. (Default: indeterminate)

	TDFRn																															Base + 0x040 + (n*0x10)
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																TDFR															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	TDFR	The full data to be compared with the TCNT reg.	RW

12.4.2.14 Timer Data HALF Register (TDHRn, 0x044 + n * 0x10, n=0~7)

This is a 16-bit read/write register. The comparison data HALF registers TDHRn is used to store the data to be compared with the content of the up-counter TCNTn. This register can be directly read and written. (Default: indeterminate)

	TDHRn																															Base + 0x044 + (n * 0x10)
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Reserved																TDHR															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	TDHR	The half data to be compared with the TCNT reg.	RW

12.4.2.15 Timer Counter (TCNTn, 0x048 + n * 0x10, n = 0~7)

TCNTn is a 16-bit read/write register. The up-counter TCNTn can be reset to 0 by software and counts up using the prescaler output clock. The counter data can be read out at any time. The data can be written at any time. This makes it possible to change the interrupt and/or clock output cycles temporarily. (Default: indeterminate)

	TCNTn																Base + 0x048 + (n * 0x10)															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																TCNT															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	TCNT	The counter value.	RW

12.4.2.16 Timer Control Register (TCRn, 0x04C + n * 0x10, n = 0~7)

The TCRn is a 32-bit read/write register. It contains the control bits for each channel. It is initialized to 0x0 by any reset.

	TCRn																Base + 0x04C + (n * 0x10)															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved					STORE_NEG_EN	STORE_POS_EN	STORE_EN	COUNT_MODE		GPIO1_NEG_EN	GPIO1_POS_EN	GPIO0_NEG_EN	GPIO0_POS_EN	CLK_NEG_EN	CLK_POS_EN	SHUTDOWN	GATE_POLA	DIRECTION_POLA	GATE_SEL		DIRECTION_SEL			GPIO1_EN	GPIO0_EN	PRESCALE			EXT_EN	Reserved	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

31:27	Reserved	Writing has no effect, read as zero.	R
26	STORE_NEG_EN	Indicate TCU will store count when store gpio input a negedge.	RW
25	STORE_POS_EN	Indicate TCU will store count when store gpio input a negedge.	RW
24	STORE_EN	Store TCU count enable	RW
23:22	COUNT_MODE	0：count range[0, TDFR] with clear to 0 when count up to TDFR. 1：count range [0, 0xFFFF] with clear to 0 when count up to 0xFFFF. 2：count range [0, 0xFFFF] with hold on 0xFFFF when count up to 0xFFFF..	RW
21	GPIO1_NEG_EN	Indicate TCU will count when gpio1 input a negedge.	RW
20	GPIO1_POS_EN	Indicate TCU will count when gpio1 input a posedge.	RW
19	GPIO0_NEG_EN	Indicate TCU will count when gpio0 input a negedge.	RW
18	GPIO0_POS_EN	Indicate TCU will count when gpio0 input a posedge.	RW
17	CLK_NEG_EN	Indicate TCU will count when select clock input a negedge.	RW
16	CLK_POS_EN	Indicate TCU will count when select clock input a posedge.	RW
15	SHUTDOWN	When this bit is 1, counter will stop counting after full, the count value is full value.	RW
14	GATE_POLA	0：counter starts when control signal is 0. 1：counter starts when control signal is 1. Note: If GATE_PLOA is 0: when input control signal is 0, the counter will add 1 for each time. when input control signal is 1, the counter will not count until input signal is 0. And, if GATE_POLA is 1, it is opposite.	RW
13	DIRECTION_POLA	0：counter subs when control signal is 0. 1：counter subs when control signal is 1. Note: If DIRECTION_POLA is 1: when input control signal is 1, the counter will add 1 for each time. but when input control signal is 0, the counter will sub 1 for each time.	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

12:11	GATE_SEl	0：gate signal hold on 0. 1：use clock with gate signal. 2：use gpio0 with gate signal. 3：use gpio1 with gate signal.	RW
10:8	DIRECTION_SEL	0: direction signal hold on 1. 1: use clock with direction signal. 2: use gpio0 with direction signal. 3: use gpio1 with direction signal. 4: use gpio0 and gpio1 quadrature result with direction signal.	RW
7	GPIO1_EN	Enable gpio1 function.	RW
6	GPIO0_EN	Enable gpio0 function.	RW
5:3	PRESCALE	These bits select the TCNT count clock frequency. Don't change this field when the channel is running. Only for EXTAL(inner clock).	RW

Bit 2	Bit1	Bit 0	Description
0	0	0	Internal clock: CLK/1
0	0	1	Internal clock: CLK/4
0	1	0	Internal clock: CLK/16
0	1	1	Internal clock: CLK/64
1	0	0	Internal clock: CLK/256
1	0	1	Internal clock: CLK/1024
110~111			Reserved

2	EXT_EN	Select EXTAL(inner clock) as the timer clock input. 0: Disable 1: Enable	RW
1:0	Reserved	Writing has no effect, read as zero.	R

12.4.2.17 Capture Control Register (CAPCRn, 0x0C0 + n*0x4, n= 0~7)

This register can set capture control signal and capture num of capture mode (i.e enable capture mode).

	CAPCRn																															Base + 0x0C0 + (n * 0x4)
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved													CAPTURE_SEL			Reserved								CAPTURE_NUM							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:19	Reserved	Writing has no effect, read as zero.	R
18:16	CAPTURE_SEL	0：TCU will capture clock. 1：TCU will capture gpio0. 2：TCU will capture gpio1. * if capture mode is disable(CAPTURE_NUM is 0) then these bits will: 1：counter will clear when gpio0 posedge. 2：counter will clear when gpio1 posedge. 3：counter will clear when gpio0 negedge.	RW
15:8	Reserved	Writing has no effect, read as zero.	R
7:0	CAPTURE_NUM	Capture times, when the value of CATURE_NUM is bigger than 0x80, than TCU will always in capture mode. Note: Only when CAPTURE_NUM is not equal to zero, the capture mode is enabled.	RW

12.4.2.18 Capture Value Register (CAPVRn, 0x0E0 +n *0x4n n = 0~3)

This register records the whole time and high level time of the capture period.

	CAPVRn																																Base + 0x0E0 + (n * 0x4)
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CAPTURE_ALL																CAPTURE_HEIGHT																
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	CAPTURE_ALL	Indicate the whole time of the capture period.	R
15:0	CAPTURE_HEIGHT	Indicate the time of high level. of the capture period	R

12.4.2.19 Filter Value Register (FIRVRn, 0x1A0 + n *0x4, n = 0~7)

	FIRVRn																																Base + 0x1A0 + (n * 0x4)
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Reserved						FIL_B										Reserved						FIL_A									
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:26	Reserved	Writing has no effect, read as zero.	R
25:16	FIL_B	Gpio1 filter counter value. When detect a posdage or negedge of gpio1, the counter value will add from 0. Only when counter num is larger than FIL_B, gpio1 will be get.	RW
15:10	Reserved	Writing has no effect, read as zero.	R
9:0	FIL_A	Gpio0 filter counter value. When detect a posdage or negedge of gpio0, the counter value will add from 0. Only when counter num is larger than FIL_A, gpio0 will be get.	RW

12.4.2.20 Store Flag Register (TSFR, 0x200)

It contains flag bits for all the channels. It can also be set by register TSFSR and TSFCR.

	TSFR																															Base + 0x200
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								SFLAG 7	SFLAG 6	SFLAG 5	SFLAG 4	SFLAG 3	SFLAG 2	SFLAG 1	SFLAG 0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect, read as zero.	R
7:0	SFLAG 7:0	store flag. 0: has't be stored 1: has be stored pending of tcu_int[1]	R

12.4.2.21 Store Flag Set Register (TSFSR, 0x204)

	TSFSR																															Base + 0x204
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Reserved																								SFS 7	SFS 6	SFS 5	SFS 4	SFS 3	SFS 2	SFS 1	SFS 0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect, read as zero.	R
7:0	SFS 7:0	Set SFLAGn bit of TSFR. 0: Ignore 1: Set SFLAGn bit to 1	W

12.4.2.22 Store Flag Clear Register (TSFCR, 0x208)

	TSFCR																															Base + 0x0208
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								SFC 7	SFC 6	SFC 5	SFC 4	SFC 3	SFC 2	SFC 1	SFC 0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect, read as zero.	R
7:0	SFC 7:0	Clear SFLAGn bit of TSFR. 0: Ignore 1: Clear SFLAGn bit to 0	W

12.4.2.23 Store Mask Register (TSMR, 0x210)

It contains flag bits for all the channels. It is initialized to 0x0000_00FF by any reset. It can only be set by register TSMSR and TSMCR.

	TSMR																															Base + 0x210
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								SMSK 7	SMSK 6	SMSK 5	SMSK 4	SMSK 3	SMSK 2	SMSK 1	SMSK 0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect, read as zero.	R
7:0	SMSK 7:0	store interrupt mask. 0: interrupt not mask 1: interrupt mask Mask pending of tcu_int[1]	R

12.4.2.24 Store Mask Set Register (TSMSR, 0x0214)

	TSMSR																															Base + 0x0214
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								SMSKS 7	SMSKS 6	SMSKS 5	SMSKS 4	SMSKS 3	SMSKS 2	SMSKS 1	SMSKS 0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect, read as zero.	R
7:0	SMSKS 7:0	Set SMSK n bit of TSMR. 0: Ignore 1: Set SMSK n bit to 1	W

12.4.2.25 Store Mask Clear Register (TSMCR, 0x218)

	TSMCR																															Base + 0x218
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								SMSKC 7	SMSKC 6	SMSKC 5	SMSKC 4	SMSKC 3	SMSKC 2	SMSKC 1	SMSKC 0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect, read as zero.	R
7:0	SMSKC 7:0	Set SMSK n bit of TSMR. 0: Ignore 1: Set SMSK n bit to 0	W

12.4.2.26 Store Value Register (TSVRn, 0x220 + n * 0x4, n = 0~7)

	TSVRn	Base + 0x220 + (n * 0x4)

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																STR_VALUE															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	STR_VALUE	The value of the stored tcu count.	RW

12.4.2.27 Store Filter Value Register (TSFVRn, 0x240 + n * 0x4, n = 0~7)

	TSFVRn																															Base + 0x240 + (n * 0x4)
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																						STR_FIL									
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
9:0	STR_FIL	Store gpio filter counter value. Only when the duration of gpio high/low level time is bigger than STR_FIL*Tpclk, the gpio will be get and the value of TCNT can be stored to TSVR.	RW

12.5 Operation Guide

12.5.1 Operation in TCU Mode

12.5.1.1 General Mode (example for ch0)

In general mode, the count will add 1 when get a posedge or a negedge or double of the clock or the control signal.

The follow steps are the example of channel 0 to use general mode.

- Step1: Set the value of TDFR0(0x40) and TDHR0(0x44) , and TDFR0 should be larger than TDHR0.
- Step2: make sure the interrupt is open.(use register 0x38)
- Step3: send a initial value for counter.(use register 0x48).
- Step4
  - if use inner clock, choose the clock choose the prescale, choose

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

CLK_POS/NEG_EN, choose count mode is 0~full.(use register 0x4c)

- if use input clock, and if this clock is input by gpio0, choose GPIO0_EN, GPIO0_POS/NEG_EN, choose count mode is 0~full.(use register 0x4c)

- Step5: enable TCU counter.(use register 0x14)

Ex(Use inner clock):

Step1:0x40 is 4 and 0x44 is 2.

Step2:0x38 bit0 and bit16(mask_clr) is 1

Step3:0x48(cnt_value) write 0

Step4:0x4c bit2 is 1, bit[5:3] is 0, bit16,17 is 1(use double edge).

Step5:0x14 bit0 is 1(cnt_en).

Figure 12-1 Timming of general mode

12.5.1.2 Gate Mode (example for ch0)

In gate mode, if gate_pola is 0, counter counts:

- when input gate control signal is 0, the value of counter will add 1 for each time.
- when input gate control signal is 1, the value of counter will remain unchanged.

To use gate mode, can follow the below steps:

- Step1: set value of TDFR0(0x40) and TDHR0(0x44).
- Step2: make sure the interrupt is open.(use register 0x38)
- Step3: send a initial value for counter.(use register 0x48).
- Step4:
  - if use inner clock, choose the clock choose the prescale, choose CLK_POS/NEG_EN, choose count mode is 0~full.(use register 0x4c)
  - if use input clock, and if this clock is input by gpio0, choose GPIO0_EN, GPIO0_POS/NEG_EN, choose count mode is 0~full.(use register 0x4c)
- Step5: if use gpio1 to control the gate, choose GPIO1_EN, choose GATE_SEL to 3.(use register 0x4c)
- Step6: enable TCU counter.(use register 0x14)

Ex(use inner clock):

Step1:0x40 is 2 and 0x44 don't mind

Step2:0x38 bit0(mask_clr) is 1

Step3:0x48(cnt_value) write 0

Step4: 0x4c bit[5:3] is 1, and bit2 is 1.(Use inner clock and prescale is 4.)

Step5:0x4c bit[12:11](use gpio0 to be gate signal) is 2, bit6(gpio0) is 1 and

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

bit14(GATE_POLA) is 0.

Step6:0x14 bit0 is 1(cnt_en).

Figure 12-2 Timming of gate mode

Note:

If gate_control is 0, the value of the counter will add 1 for each time.

If gate_control is 1, the value of the counter will remain unchanged until gate_control is 0 at the posedge of EXTAL/4.

12.5.1.3 Direction Mode(example for ch0)

In direction mode, counter will add or sub depend on the direction pola and the direction control signal.

If DIRECTION_PLOA is 1:

- ✧ when direction control signal is 0, the value of counter will add 1 for each time.
- ✧ when direction control signal is 1, the value of counter will sub 1 for each time.

To use direction mode, can follow the below steps:

- Step1: set value of TDFR0(0x40) and TDHR0(0x44).
- Step2: make sure the interrupt is open.(use register 0x38)
- Step3: send a initial value for counter.(use register 0x48).
- Step4:
  - ■ if use inner clock, choose the clock choose the prescale, choose CLK_POS/NEG_EN, choose count mode for you want.(use register 0x4c)
  - ■ if use input clock, and if this clock is input by gpio0, choose GPIO0_EN, GPIO0_POS/NEG_EN, choose count mode for you want.(use register 0x4c)
- Step5: if use gpio1 to control the direction, choose GPIO1_EN, choose DIRECTION_SEL to 3.(use register 0x4c)
- Step6: enable TCU counter.(use register 0x14)

Ex:(Use Inner Clock)

Step1:0x40(TDFR0) is 4 and do not care the value to be written to 0x44(TDHR0);

Step2:0x38 bit0(mask_clr) is 1

Step3:0x48(cnt_value) write 0

Step4: 0x4c bit[5:3] is 1, and bit2 is 1.(Use inner clock and prescale is 4.)

Step5:0x4c bit6(gpio0_en) is 1, bit[10:8](use gpio0 to be direction) is 2 and bit13(DIRECTION_POLA) is 0.

Step6:0x14 bit0 is 1(cnt_en).

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Figure 12-3 Timming of direction mode

Note:

- In direction mode, after enable timer0, the initial value of TCNT0 is TDFR0.
- If direction_control signal is 0, the counter will add 1 for each time(at the posedge of EXTAL/4).
- If direction_control signal is 1, the counter will sub 1 for each time(at the posedge of EXTAL/4).

12.5.1.4 Quadrature Mode(example for ch0)

In quadrature mode, counter counts because of the quadrature input.

✧ When the input control signal1 and signal2 are orthogonal (control signal1 and signal2 are different from each other), the counter will add 1 for each time. Otherwise(signal1 and signal2 are the same), the value of counter will be unchanged.

To use quadrature mode, can follow the below steps:

- Step1: set value of TDFR0(0x40) and TDHR0(0x44).
- Step2: make sure the interrupt is open.(use register 0x38)
- Step3: send a initial value for counter.(use register 0x48).
- Step4: it must use inner clock, choose the clock choose the prescale, choose count mode for you want.(use register 0x4c)
- Step5: it must use gpio0 and gpio1 to calculate the quadrature, so choose GPIO0_EN and GPIO1_EN. you can use GPIO_POS/NEG_EN to sample the value of quadrature.(use register 0 x4c)
- Step6: because of use quadrature mode, so if you want to get direction, you should choose DIRECTION_SEL to 4, if not , you will choose 1.(use register 0x4c)
- Step7: enable TCU counter.(use register 0x14)

Ex(Use inner clock):

Step1:Write proper value you want to 0x40 and 0x44

Step2:0x38 bit0 and bit16(mask_clr) is 1

Step3:0x48(cnt_value) write 0

Step4: 0x4c bit[5:3] is 0, and bit2 is 1.(Use inner clock and prescale is 1.)

Step5:0x4c bit6,7(gpio0,1_en) is 1, bit19, 20(gpio0_neg_en and gpio1_pos_en) is 1.

Step6:0x4c bit[10:8] is 4

Step7:0x14 bit0 is 1(cnt_en).

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Figure 12-4 Timming of quadrature mode

Note:

- When direction_control is 1:
  - If gpio0_value and gpio1_value are different form each other, when detecting a negedge of gpio0_value(such as A0) or a posedge of gpio1_value(such as B0 and B1), the TCNT0 will add1 each time.
  - But if gpio0_value and gpio1_value are the same(A1), the TCNT0 will not be changed.
- When direction_control is 0:
  - If gpio0_value and gpio1_value are different form each other, when detecting a negedge of gpio0_value(A4) or a posedge of gpio1_value(B2), the TCNT0 will sub 1 each time.
  - But if gpio0_value and gpio1_value are the same(A2, A3 and B3), the value of TCNT0 will remain unchanged.

12.5.1.5 Pos Mode(example for ch0)

In pos mode, counter start counts from 0 when capture a posedge or a negedge of the control singnal.

To use pos mode, can follow the below steps:

- Step1: set value of TDFR0(0x40) and TDHR0(0x44).
- Step2: make sure the interrupt is open.(use register 0x38)
- Step3: send a initial value for counter.(use register 0x48).
- Step4:
  - if use inner clock, choose the clock prescale, choose CLK_POS/NEG_EN, choose count mode is 0~full.(use register 0x4c)
  - if use input clock, and if this clock is input by gpio0, choose GPIO0_EN, GPIO0_POS/NEG_EN, choose count mode is 0~full.(use register 0x4c)
- Step5: if use gpio1 to control the pos, choose GPIO1_EN.(use register 0x4c)
- Step6: because of use pos mode, so choose CAPTURE_SEL to 2.(use register 0xc0)
- Step7: enable TCU counter.(use register 0x14)

Ex:

Step1:0x40 is 4 and 0x44 don't mind

Step2:0x38 bit0(mask_clr) is 1

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Step3:0x48(cnt_value) write 0

Step4: 0x4c bit[5:3] is 0, and bit2 is 1.(Use inner clock and prescale is 1.)

Step5:0x4c bit6(gpio0_en) is 1 and bit16(clk_pos) is 1.

Step6:0xc0 bit[16:18](gpio0_pos) is 1

Step7:0x14 bit0 is 1(cnt_en).

Figure 12-5 Timming of pos mode

12.5.1.6 Capture Mode(example for ch0)

In capture mode, counter counts a period and output high level time and the whole period time.

- ✧ Similar to the Pos Mode, the counter starts count from 0 when capture a posedge or a negedge of the control signal, and the capture time depends on the value of CAPTURE_NUM of CAPCR register.
- ✧ The TCU_CAP_VALUE register will record the whole time and high level time of the capture period.

To use capture mode, can follow the below steps:

- Step1: make sure the interrupt is open.(use register 0x38)
- Step2: send a initial value for counter.(use register 0x48).
- Step3: if wants to capture gpio1, choose GPIO1_EN.(use register 0x4c)
- Step4: if wants to use exclk posedge, choose CLK_POSE_EN.(use register 0x4c)
- Step5: because of use capture mode, so choose CAPTURE_SEL to 3. set the CAPTURE_NUM(must not be 0) you want to capture(if number bigger then 0x80 then the capture will not stop)(use register 0xc0). And if you want to close the capture mode,set CAPTURE_NUM to be 0.
- Step6: enable TCU counter.

Ex:

Step1:0x38 bit0 and bit16 (mask_clr) is 1;

Step2: 0x40 is 100, and 0x48(cnt_value) write 0

Step3:0x4c bit16(clk_pos) is 1 and bit6(gpio0_en) is 1

Step4:0x4c bit[5:3] is 0, and bit2 is 1.(Use inner clock and prescale is 1.)

Step5:0xc0 bit[16:18](gpio0_pos) is 1 and bit[7:0] is 3.

Step6:0x14 bit0 is 1(cnt_en).

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Figure 12-6 Timming of capture mode

Note:

- When capture_enable is 1(capture mode is eanbled), TCNT0 will start from 0 when get a posedeg of gpio0_value (such as A0, A2 and A4). But if capture_enable is 0, the posedge of gpio0_value will not affect the value of TCNT0 (A5).
- After capture_enable is 1, the first posedge of gpio0_value (A0) will clear TCNT0 to 0 but not stroe it to CAPVR0.
- The second and the third posedge of gpio0_value (A2 and A4) store TCNT0 to CAPVR0 and then clear TCNT0 to 0 during capture moude enabled.
- The high 16bits of CAPVR0 is the whole time between previous and current posedge of gpio0_value;
- And the low 16bits is the high level time between previous and current posedge of gpio0_value.That means, when getting a negedge of gpio0_value (A1 and A3), the TCNT0 will be strored to low 16bits of CAPVR0.

12.5.2 Operation in TCU Function

12.5.2.1 Filter function (example for ch0)

For filter function, it will cut the input signal that we do not want. It also filters the posedge/ negedge that holding for very short time. If you want to enable filter function, can follow the below stepsto set registers. This function can open wheneven you want and whatever operation mode.

- Step1: Write 0x6 to FIRVR0.FIL_A(0x1a0)；
- Step2: Set bit6 of TCR0(0x4C) to 1 to enable gpio0 as the input signal;
- Step3: Set bi18 of TCR0(0x4C) to 1 to use the posedge of gpio0 to count.
- Setp4: Set bit0 of TESR(0x14) to 1 to enable channel0 counter.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Figure 12-7 Timming of filter function

Note:

- filter_sig is the filtered signal of gpio0_value and the unit of filter_cnt is pclk.
- If gpio0_value and filter_sig are different(such as A0, A2 and A4), the filter_cnt will add 1 for each pclk until filter_cnt is equal to FIL_A, then filter_cnt will not change. But if gpio0_value and filter_sig are same(A1, A3 and A5), the filter_cnt will change to be 0.
- The filter_sig will change to be same as input when filter_cnt is equal to FIL_A(C0 and C1). Then the filter_cnt will change to 0(B0 and B1) until gpio0_value change to be different from the fiter_sig(A2 and A4).
- The value of TCNT0 will add 1 when detect a posedge of filter_sig(C0).
- If the high level of input is too smaller, such as A4~A5, filter_sig will not change, and the TCNT0 remains unchanged. That menas the input value is invalid during this period(A4~A5) and that is what filter means.

12.5.2.2 Gpio store function (example for ch0)

In this function, the value fo TCNTn will be stroed to TSVRn when get a posedge/negedge of gpio(PB03).

- Step1: Set store_en and select which edge(posedge/negedge) (0x4c)
- Step2: Set store_mask_clr you can unmask store interrupt (0x218)
- Step3: Set clock, cont control signal(0x4c);
- Step4: enable TCU conter of channel.

Ex(ch0)

Step1: 0x4c bit24 is1 to enable store funcitn, and bit25 is 1 to store when get a posedeg of the gpio(PB03).

Step2: 0x218 bit0 is 0.

Step3: 0x4c bit2(use inner clock) is 1, bit16(count when clock posedge) is 1.

Stepp4: 0x14 bit0 is 1(cnt_en).

Figure 12-8 Timing of store function

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

13 Pulse Modulator Module

13.1 Overview

This chapter describes the pluse modulator module, explains its modes of operation, and defines its registers.This module can produce PWM according to the configuration.

13.2 Features

- 8 separate channels
- Count clock is up to 500MHz
- 2 modes : CPU, DMA
- 64 entries x 32 bits wide data FIFO for each DMA Channel
- GPIO save output waveforms number

13.3 Block Diagram

Figure 13-1 PWM Block Diagram

13.4 Register description

Following chapter will descript the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. Register read/write attribute

   R - Read only

   W - Write only

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

RW - read and write
RCW - read and write, but clear to 0 by read
RSW - read and write, but set to 1 by read
RWC - read and write, clear to 0 by write 0, write 1 has no effect
RWS - read and write, set to 1 by write 1, write 0 has no effect
RC - read only, and clear to 0 by read
RS - read only, and set to 1 by read
SPEC - special access method, relate to its description

3. Reset Value
   1 - reset to 1
   0 - reset to 0
   ? - value unknown after reset

Table 13-1 Registers Memory Map-Address Base

Name	Base	Description
PWM	0x134C0000	Address base of PWM

Table 13-2 PWM Registers Configuration(n=0,1,2,3)

Name	Description	RW	Reset Value	Address offset	Width
PWMENS	Channel enable set	W	-	0x0000	32
PWMENC	Channel enable clear	W	-	0x0004	32
PWMEN	Channel enable status	R	0x00000000	0x0008	32
PWMUPT	Update waveform	W	-	0x0010	32
PWMBSY	Update process busy	R	0x00000000	0x0014	32
PWMMS	Channel mode select	RW	0x00000000	0x0020	32
PWMINL	Channel init level	RW	0x00000000	0x0024	32
PWMIDL	Channel idle level	RW	0x00000000	0x0028	32
PWMCCn	Channel n Counter configure	RW	0x00000000	0x0040+n*4	32
PWMWCn	Channel n waveform configure	RW	0x00000000	0x0080+n*4	32
PWMDRn	DMA Channel data register	W	-	0x00C0+n*4	32
PWMDFNn	DMA Channel FiFo data number	R	0x00000000	0x0100+n*4	32
PWMDRTNn	Channel n DMA req trigger number	RW	0x00000000	0x0140+n*4	32
PWMDRE	DMA Channel n DMA req enable	RW	0x00000000	0x0180	32
PWMDRS	DMA Channel n DMA req status	R	0x00000000	0x0184	32

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

PWMDFIE	DMA channel FiFO Interrupt Enable	RW	0x00000000	0x0188	32
PWMDFS	DMA channel FIFO status	R	0x00000000	0x018C	32
PWMDAFF	Inner DMA async fifo flush	W	0x00000000	0x0190	32
PWMDCFF	Inner DMA channel fifo flush	W	0x00000000	0x0194	32
PWMSS	Pwm store status	RW	0x00000000	0x0200	
PWMSIE	Pwm store int enable	RW	0x00000000	0x0204	
PWMSC	Pwm store control	RW	0x00000000	0x0210+n*4	
PWMSN	Pwm store number	RW	0x00000000	0x0250+n*4	
PWMON	Pwm output number	R	0x00000000	0x0290+n*4	

13.4.1 PWM Counter Enable Register (PWMEN, PWMENS, PWMENC)

The PWMEN is a 32-bit read-only register. It contains the counter enable control bits for each channels. It is initialized to 0x00000000 by any reset. It can only be set/clear by the register PWMENS and PWMENC. Since the enable control bits are located in the same addresses, different channel can be started at the same time. (Default: disable)

	PWMENS																															BASE+0x0000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								PWM7ENS	PWM6ENS	PWM5ENS	PWM4ENS	PWM3ENS	PWM2ENS	PWM1ENS	PWM0ENS
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect, read as zero.	R
7:0	PWMnENS	Enable the counter in PWM channeln's timer. 0: no effect 1: set PWNEN.PWMnEN to 1	W

	PWMENC																															BASE+0x0004
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								PWM7ENC	PWM6ENC	PWM5ENC	PWM4ENC	PWM3ENC	PWM2ENC	PWM1ENC	PWM0ENC
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect, read as zero.	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

7:0	PWMnENC	Disable the counter in channel2's timer. 0: no effect 1: clear PWNEN.PWMnEN to 0	W

	PWMEN																															BASE+0x0008
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								PWM7EN	PWM6EN	PWM5EN	PWM4EN	PWM3EN	PWM2EN	PWM1EN	PWM0EN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect, read as zero.	R
7:0	PWMnEN	Enable the counter in channeln's timer. 0: The PWM is disable 1: The PWM is enable	R

13.4.2 PWM Update Register (PWMUPT)

Write 1 to each bit to update related PWM channel's counter period and pulse start/end position. Only set in common mode.

	PWMUPT																															BASE+0x0010
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								PWM7UP	PWM6UP	PWM5UP	PWM4UP	PWM3UP	PWM2UP	PWM1UP	PWM0UP
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect, read as zero.	R
7:0	PWMnUP	Update the PWM's waveform configuration. Write 0 has no effect. Write 1 to update.	W

13.4.3 PWM Update Process Busy Status Register (PWMBSY)

After setting update bit for one channel, the related PWMnBUSY bit will keep 1 until the update takes effection. Only used in common mode.

	PWMBSY	BASE+0x0014

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								PWM7BSY	PWM6BSY	PWM5BSY	PWM4BSY	PWM3BSY	PWM2BSY	PWM1BSY	PWM0BSY
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect, read as zero.	R
7:0	PWMnBUSY	Busy in updating the PWM's waveform configuration. 0, idle in updating. 1, busy in updating.	R

13.4.4 PWM Channel Mode Select Register (PWMMS)

Channel n mode select configuration(n represents the PWM channel n).

	PWMMS																															BASE+0x0020
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																Reserved								PWM7MS	PWM6MS	PWM5MS	PWM4MS	PWM3MS	PWM2MS	PWM1MS	PWM0MS
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect, read as zero.	R
7:0	PWMnMS	0: Channel n select reg mode 1: Channel n select dma mode	RW

13.4.5 PWM INIT LEVEL Register (PWMINL)

Channel n wave Init level configuration(n represents the PWM channel n).

	PWMINL																															BASE+0x0024
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																Reserved								PWM7INL	PWM6INL	PWM5INL	PWM4INL	PWM3INL	PWM2INL	PWM1INL	PWM0INL
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

31:8	Reserved	Writing has no effect, read as zero.	R
7:0	PWMnINL	Channel n wave init level configuration	RW

13.4.6 PWM IDLE LEVEL Register (PWMIDL)

Channel n wave Idle level configuration(n represents the PWM channel n).

	PWMIDL																															BASE+0x0028
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																Reserved								PWM7IDL	PWM6IDL	PWM5IDL	PWM4IDL	PWM3IDL	PWM2IDL	PWM1IDL	PWM0IDL
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect, read as zero.	R
7:0	PWMnIDL	Channel n wave idle level configuration	RW

13.4.7 PWM Counter Configure Register (PWMCCn)

	PWMCCn																															BASE+0x0040+n*4 n=0~7
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																Reseved												PRESCALE			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:4	Reserved	Writing has no effect, read as zero.	
3:0	PRESCALE	These bits select the PWM count clock frequency for each channel. Don't change this field when the channel is running. For PRESCALE <8:Freq= input counter clock/(2^PRESCALE) For PRESCALE >=8:Reserved	RW

13.4.8 PWM Waveform Configuration(PWMWCn)

Only set in common mode.

	PWMWCn																															BASE+0x0080+n*4 n=0~7
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	HIGH																LOW															

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	HIGH	Waveform high level cycle number. Can't be zero.	RW
15:0	LOW	Waveform low level cycle number. Can't be zero.	RW

The PWM's waveform show in figure below:

13.4.9 PWM DMA Channel Data Register (PWMDRn)

Only set in dma mode.

	PWMDRn																															BASE+0x00C0+n*4 n=0~7
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DATA	Data register	W

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

13.4.10 PWM DMA Channel FiFo Number Register (PWMDFNn)

	PWMDFNn																															BASE+0x0100+n*4 n=0~7
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																									FNUM						
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
6:0	FNUM	Data Number	R

13.4.11 PWM DMA Request Trigger Number Register (PWMDRTNn)

	PWMDRTNn																															BASE+0x0140+n*4 n=0~7
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																									TNUM						
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
6:0	TNUM	DMA Requset Tigger Number (64-FNUM) >= TNUM，DMA request will active	W

13.4.12 PWM DMA Request enable Register(PWMDRE)

	PWMDRE																															BASE+0x0180
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								PWM7DRE	PWM6DRE	PWM5DRE	PWM4DRE	PWM3DRE	PWM2DRE	PWM1DRE	PWM0DRE
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect, read as zero.	R
7:0	PWMnDRE	1: enable	WR

13.4.13 PWM DMA Request Status Register(PWMDRS)

	PWMDRS																															BASE+0x0184
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Reserved																								PWM7DRS	PWM6DRS	PWM5DRS	PWM4DRS	PWM3DRS	PWM2DRS	PWM1DRS	PWM0DRS
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect, read as zero.	R
7:0	PWMnDRS	If DMA req, this bit set 1	R

13.4.14 PWM DMA FiFo Under Run Interrupt enable Register(PWMDFIE)

	PWMDFIE																															BASE+0x0188
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								PWM7DFIE	PWM6DFIE	PWM5DFIE	PWM4DFIE	PWM3DFIE	PWM2DFIE	PWM1DFIE	PWM0DFIE
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect, read as zero.	R
7:0	PWMnDFIE	1: enable	WR

13.4.15 PWM DMA Channel FiFo Status Register(PWMDFS)

	PWMDFS																															BASE+0x018C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								PWM7DFS	PWM6DFS	PWM5DFS	PWM4DFS	PWM3DFS	PWM2DFS	PWM1DFS	PWM0DFS
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect, read as zero.	R
7:0	PWMnDFS	1: FIFO empty 0: FIFO not empty	R

13.4.16 PWM DMA Async FiFo Flush(PWMDAFF)

	PWMDAFF																															BASE+0x0190
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Reserved																															FLUSH
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect, read as zero.	R
0	FAF	Write 1 to Flush Async FiFo, hardware auto clear	W

13.4.17 PWM DMA Channel FiFo Flush(PWMDCFF)

	PWMDCFF																															BASE+0x0194
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								FLUSH7	FLUSH6	FLUSH5	FLUSH4	FLUSH3	FLUSH2	FLUSH1	FLUSH0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:4	Reserved	Writing has no effect, read as zero.	R
3:0	PWMnFCF	Write 1 to Flush channel FiFo, hardware auto clear	W

13.4.18 PWM Store Status Register(PWMSS)

	PWMSS																															BASE+0x0200
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								PWM7SS	PWM6SS	PWM5SS	PWM4SS	PWM3SS	PWM2SS	PWM1SS	PWM0SS
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:4	Reserved	Writing has no effect, read as zero.	R
3:0	PWMnSS	1: the pwm output count has be stored 0: the pwm output count has't be stored	RW1C

13.4.19 PWM Store Interrupt Enable Register(PWMSIE)

	PWMSIE																															BASE+0x0204
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Reserved																								PWM7SIE	PWM6SIE	PWM5SIE	PWM4SIE	PWM3SIE	PWM2SIE	PWM1SIE	PWM0SIE
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:4	Reserved	Writing has no effect, read as zero.	R
3:0	PWMnSIE	1: store interrupt enable 0: store interrupt disable	RW

13.4.20 PWM Store Control Register(PWMSCn)

	PWMSCn																															BASE+0x0210+n*4 n=0~7
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved													store_en	pos_edge_en	neg_edge_en	Reserved						FILTER_NUM									
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:19	Reserved	Writing has no effect, read as zero.	R
18	SE	Store enable	RW
17	SPE	Store IO posedge enable 1: At IO posedge to store the pwm ouput count	RW
16	SNE	Store IO negedge enable 1: At IO negedge to store the pwm ouput count	RW
15:10	Reserved	Writing has no effect, read as zero.	R
9:0	SFNUM	store filter number Filter count clk was h2clk	RW

13.4.21 PWM Store Number(PWMSNn)

	PWMSNn																															BASE+0x0250+n*4 n=0~7
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SNUM																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:0	SNUM	The Stored number.	R

13.4.22 PWM Output Number(PWMONn)

	PWMONn																															
																	BASE+0x0290+n*4 n=0~7															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ONUM																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	ONUM	The Output waveform number.	R

13.5 Basic Operation

13.5.1 Register update mode

Figure 13-2 Register update mode

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

1. Configuration.
   a) Write **PWMCCn** to set related channel count clock frequency.
   b) Write **PWMINL, PWMIDL, PWMWC** to set the related PWM channel's waveform.
   c) Write 0 to **PWMMS** to select the register mode.
2. Enable
   Set the **PWMENS** bit to 1 to enable the related PWM channels. You can enable different channels at same time, and the related PWM channels will keep synchronized.
3. Update
   During PWM is working, if you want to change the waveform, you can set related registers as follows:
   Set **PWMINL**，**PWMIDL, PWMWC** and set **PWMUPT** for related channel. Then polling related **PWMBSY** bit, after it is cleared to 0, the update information will take effection.
4. Disable
   Set **PWMENC** to clear related channel's enable. The waveform will keep the last wave configuration.

13.5.2 DMA mode

1. Configuration.
   a) Write **PWMCCn** to set related channel count clock frequency.
   b) Write **PWMINL, PWMIDL** to set the related PWM channel's waveform.
   c) Write 1 to **PWMMS** to select the dma mode.
   d) Write **PWMDRTNn** to config the DMA fifo request trigger num.
   e) Config PDMA, the Destination address is **PWMDRn.**

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

2. Enable
   a) Set the **PWMDRE** bit to 1, enable dma fifo request.
   b) Set the **PWMENS** bit to 1 to enable the related PWM channels. You can enable different channels at same time, and the related PWM channels will keep synchronized.
3. Disable
   Set **PWMENC** to clear related channel's enable. The waveform will keep the last wave configuration.
4. Status
   FiFO empty status : **PWMDFS**
   DMA FIFO Data Request Status : **PWMDRS**
   PWM Ouput Number Stored Status : **PWMSS**
5. Interrupt
   Write 1 to **PWMSIE** bit n to enable channel n GPIO Store interrupt..
   Write 1 to **PWMDFIE** bit n to enable channel n fifo under run Interrupt. Just For Debug.
6. Flush FiFo
   a) Write 1 to **PWMDAFF** to flush internal async fifo.
   b) Write 1 to **PWMDCFF** bit n to flush channel n fifo.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

14 Operating System Timer

14.1 overview

This module include 2 channels, sys_ost32(ost1) and sys_ost64(ost2)

- sys_ost32: 32-bit timer, use to generate operating system's time slice.
  - Has counter Full-match interrupt.
  - Counter by an chip external clock(EXCLK), which can be divide by 1,4,16
  - Read by an asynchronous system clock.

- sys_ost64: 64-bit timer.
  - Counter by an chip external clock(EXCLK), which can be divide by 1,4,16
  - Read by an asynchronous system clock

14.2 feature

- There are three speed mode of the counter, it can be 1,4,16 exclk that the counter add 1.
- The time of interrupt signal enable can be control by user, and is also can be mask by user.
- The counter will set to 0 by user or when it is full.
- This module will disable the hready signal indicate it is operating a read.

14.3 register description

Following chapter will descript the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. Register read/write attribute
   R - Read only
   W - Write only
   RW - read and write
   RCW - read and write, but clear to 0 by read
   RSW - read and write, but set to 1 by read
   RWC - read and write, clear to 0 by write 0, write 1 has no effect
   RWS - read and write, set to 1 by write 1, write 0 has no effect
   RC - read only, and clear to 0 by read
   RS - read only, and set to 1 by read
   SPEC - special access method, relate to its description
3. Reset Value
   1 - reset to 1
   0 - reset to 0
   ? - value unknown after reset

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

14.3.1 Registers Memory Map

Table 14-1 Registers Memory Map Base Address

Name	Base	Description
SYS_OST	0x12000000	Address base of SYS_OST

The SYS_OST is controlled by a set of registers that the application configures before every operation. The following table lists all the registers.

Table 14-2 SYS_OST Registers Map

Name	RW	Reset Value	Address offset	Access Size
OSTCCR	RW	0x0000_0000	0x00	32
OSTER	R	0x0000_0000	0x04	32
OSTCR	RW	0x0000_0000	0x08	32
OSTFR	RWC	0x0000_0000	0x0C	32
OSTMR	RW	0x0000_0001	0x10	32
OST1DFR	RW	0xFFFF_FFFF	0x14	32
OST1CNT	R	0x0000_0000	0x18	32
OST2CNTH	R	0x0000_0000	0x1C	32
OST2CNTL	R	0x0000_0000	0x20	32
OST2CNTHBUF	R	0x0000_0000	0x24	32
OSTESR	W	0x0000_0000	0x34	32
OSTECR	W	0x0000_0000	0x38	32

14.3.2 Register and Fields Description

14.3.2.1 Timer Clock Control Register (OSTCCR,0x00)

	OSTCCR																															Base + 0x00
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												PRESCALE2		PRESCALE1	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:4	Reserved	Writing has no effect. Read as zero.	R
3:2	PRESCALE2	These bits select the TCNT count clock frequency for ost2. Don't	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

<table>
<tr><td></td><td></td><td>change this field when the channel is running.
<table>
<tr><th>Bit1</th><th>Bit 0</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>Internal clock: CLK/1</td></tr>
<tr><td>0</td><td>1</td><td>Internal clock: CLK/4</td></tr>
<tr><td>1</td><td>0</td><td>Internal clock: CLK/16</td></tr>
<tr><td>1</td><td>1</td><td>Reserved</td></tr>
</table></td><td></td></tr>
<tr><td>1:0</td><td>PRESCALE1</td><td>These bits select the TCNT count clock frequency for ost1. Don’t change this field when the channel is running.
<table>
<tr><th>Bit1</th><th>Bit 0</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>Internal clock: CLK/1</td></tr>
<tr><td>0</td><td>1</td><td>Internal clock: CLK/4</td></tr>
<tr><td>1</td><td>0</td><td>Internal clock: CLK/16</td></tr>
<tr><td>1</td><td>1</td><td>Reserved</td></tr>
</table></td><td>RW</td></tr>
</table>

14.3.2.2 Timer Counter Enable Register (OSTER,0x04)

The OSTER is a 32-bit read-only register. It contains the counter enable control bits for both channels. It is initialized to 0x00000000 by any reset. It can only be set by register OSTESR and OSTECR. Since the timer enable control bits are located in the same addresses, two timers can be started at the same time. (Default: disable)

	OSTER																															**Base + 0x04**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														OST2EN	OST1EN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:2	Reserved	Writing has no effect. Read as zero.	R
1	OST2EN	Enable the counter in channel2’s timer. 0: Stop counting up 1: Begin counting up	R
0	OST1EN	Enable the counter in channel1’s timer 0: Stop counting up 1: Begin counting up	R

14.3.2.3 Timer Counter Clear Register (OSTCR,0x08)

The OSTCR is a 32-bit write-only register. It used to clear the two channel .

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	OSTCR																															Base + 0x08
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														OST2CLR	OST1CLR
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:2	Reserved	Writing has no effect, read as zero.	R
1	OST2CLR	Clear the counter in channel2's timer. 0: Invalid 1: Set the counter to 0	W
0	OST1CLR	Clear the counter in channel1's timer. 0: Invalid 1: Set the counter to 0	W

14.3.2.4 Timer Flag Register (OSTFR,0x0C)

The OSTFR is a 32-bit read-only register. It contains the comparison match flag bits for both channels. It is initialized to 0x00000000 by any reset.

	TFR																															Base + 0x0C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															FFLAG
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect, read as zero.	R
0	FFLAG	channel1's FULL comparison match flag. (OST1CNT = OST1DFR) 0: Comparison not match 1: Comparison match	RWC

14.3.2.5 Timer Mask Register (OSTMR,0x10)

The OSTMR is a 32-bit read-only register. It contains the comparison match flag bits for both channels. It is initialized to 0x00000001 by any reset.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	OST1MR																															Base + 0x10
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															FMASK
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect, read as zero.	R
0	FMASK	Channel1's FULL comparison match interrupt mask. 0: Comparison match interrupt be not masked 1: Comparison match interrupt be masked	RW

14.3.2.6 Timer Data FULL Register (OST1DFR,0x14)

The comparison data FULL registers OST1DFR is used to store the data to be compared with the content of the counter OST1CNT.

	OST1DFR																															Base + 0x14
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OST1DFR																															
RST	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

14.3.2.7 Timer Counter (OST1CNT,0x18)

OST1CNT is a 32-bit read/write register. The up-counter OST1CNT can be reset to 0 by software and counts up using the pre-scale output clock. When OST1CNT count up to equal to OST1DFR, it will reset to 0 and continue to count up.

The counter data can be read out at any time. The data can be clear by OSTCR. (Default: indeterminate)

	OST1CNT																															Base + 0x18
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OST1CNT																															

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

14.3.2.8 Operating System Timer Counter (OST2CNTH, OST2CNTL)

The operating system timer counter (OST2CNT) is a 64-bit read/write counter. OST2CNTH is the high 32 bits and OST2CNTL is the low 32 bits. The up-counter OST2CNT can be enable by software and counts up using the pre-scale output clock. When read OST2CNTL, the OST2CNTH is store at OST2CNTBUF, the software can read OST2CNTBUF to get the total 64-bit number.

	OST2CNTH																															**Base + 0x1C**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OST2CNTH																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	OST2CNTL																															**Base + 0x20**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OST2CNTL																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

14.3.2.9 Operating System Timer Counter high 32 bits buffer (OST2CNTHBUF,0x24)

The operating system timer counter high 32 bits buffer OST2CNTHBUF is used to store the high 32 bits of OSTCNT2 when its lower 32 bits are read by software. This register can be directly read. (Default: indeterminate)

	OST2CNTHBUF																															**Base + 0x24**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OST2CNTHBUF																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

14.3.2.10 Timer Counter Enable Set Register (OSTESR,0x34)

The OSTESR is a 32-bit write-only register, It used to set register OSTER.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	OSTESR																															Base + 0x34	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														OST2ENS	OST1ENS
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:2	Reserved	Writing has no effect, read as zero.	R
1	OST2ENS	Enable the counter in channel2's timer. 0: no effect 1: set OSTER.OST2EN to 1	W
0	OST1ENS	Enable the counter in channel1's timer 0: no effect 1: set OSTER.OST1EN to 1	W

14.3.2.11 Timer Counter Enable Clear Register (OSTECR,0x38)

The OSTECR is a 32-bit write-only register, It used to clear register OSTER.

	OSTECR																															Base + 0x38	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														OST2ENC	OST1ENC
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:2	Reserved	Writing has no effect, read as zero.	R
1	OST2ENC	Disable the counter in channel2's timer. 0: no effect 1: clear OSTER.OST2EN to 0	W
0	OST1ENC	Disable the counter in channel1's timer 0: no effect 1: clear OSTER.OST1EN to 0	W

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

14.4 Operation

14.4.1 Basic Operation in channel1

1.Initial the configuration.
Writing OSTCCR.PRESCALE to set OST1CNT OST2CNT count clock frequency.
Writing OSTCR.OST1CLR and OST2CLR to set the begin number to 0.
2.If the test need to mask the interrupt then you will setting the suit bit of OST1MR
If the test need to enable the ost1's interrupt, then you will setting a acceptable value of OST1DFR, then the counter will enable a interrupt when it's count value is equal to the value you set.

3.After initialize the register of timer, we should start the counter as follows:
Setting the OSTESR.OST1EN(and/or OST2EN) bit to 1 to enable the OST1CNT(and/or OST2CNT). Then it will begin to count up.

14.4.2 Stop Operation in channel1

Set the OSTER.OST1EN 0 to disable the OST1CNT.
Set the OSTER.OST2EN 0 to disable the OST2CNT.

14.4.3 modify the pre-scale in channel1

1.It’s not permitted to modify the pre-scale when the counter is running.
2.if you want to modify the pre-scale, you should
first: Setting the OSTER.OST1EN bit to 0 to disable the OST1CNT. Set the OSTER.OST2EN bit to 0 to disable the OSTCNT
second: modify the pre-scale in OSTCCR
third: Setting the OSTESR.TCST bit to 1 to enable the TCNT again. Setting the TESR.OSTST bit to 1 to enable the OSTCNT again.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

15 Watchdog Timer

15.1 Overview

The watchdog timer is used to resume the processor whenever it is disturbed by malfunctions such as noise and system errors. The watchdog timer can generate the reset signal.

15.2 Features

- Generates WDT reset
- A 16-bit Data register and a 16-bit counter
- WDT has a half interrupt.(use flag 24bit, more information please refer to tcu_spec)
- Counter clock uses the input clock selected by software
  - only RTCCLK can be used as the clock for counter
  - The division ratio of the clock can be set to 1, 4, 16, 64, 256 and 1024 by software

15.3 Register Description

Following chapter will descript the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. Register read/write attribute
   R - Read only
   W - Write only
   RW - read and write
   RCW - read and write, but clear to 0 by read
   RSW - read and write, but set to 1 by read
   RWC - read and write, clear to 0 by write 1, write 0 has no effect
   RWS - read and write, set to 1 by write 1, write 0 has no effect
   RC - read only, and clear to 0 by read
   RS - read only, and set to 1 by read
   SPEC - special access method, relate to its description
3. Reset Value
   1 - reset to 1
   0 - reset to 0
   ? - value unknown after reset

15.3.1 Register Memory Map

Table 15-1 Registers Memory Map Base Address

Name	Base	Description

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

WDT	0x10002000	Address base of WDT

The WDT is controlled by a set of registers that the application configures before every operation. The following table lists all the registers.

Table 15-2 WDT Registers Map

Name	RW	Reset Value	Address offset	Access Size
WDT_FULL	RW	0x0000_0000	0x00	16
WDT_ENABLE	RW	0x0000_0000	0x04	8
WDT_COUNT	R	0x0000_????	0x08	16
WDT_CONTROL	RW	0x0000_0000	0x0C	16

15.3.2 Register and Fields Description

15.3.2.1 Watchdog Timer Data Register (WDT_FULL,0x00)

The watchdog timer data register TDR is used to store the data to be compared with the content of the watchdog timer up-counter TCNT. This register can be directly read and written. (Default: indeterminate)

	WDT_FULL																															Base + 0x00
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	THR																TDR															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:16	THR	The half value of timer counter want to count. When TCNT count up to THR, the comparison match signal will be generated and a WDT flag(refer to bit24 of 错误!未找到引用源。) is generated.	RW
15:0	TDR	The value of timer counter want to count. When TCNT count up to TDR, the comparison match signal will be generated and a WDT reset is generated.	RW

15.3.2.2 Watchdog Enable Register (WDT_ENABLE,0x04)

The TCER is an 8-bit read/write register. It contains the counter enable control bits for watchdog. It is initialized to 0x00 by any reset.

	WDT_ENABLE	Base + 0x04

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															TCEN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect, read as zero.	R
0	TCEN	Counter enable control. 0: Timer stop 1: Timer running	RW

15.3.2.3 Watchdog Timer Counter (WDT_COUNT,0x08)

The watchdog timer counter (TCNT) is a 16-bit read/write counter. The up-counter TCNT can be reset to 0 by software and counts up using the prescaler output clock. When TCNT count up to equal to TDR, the comparison match signal will be generated and a WDT reset is generated. The data can be read out at any time. The counter data can be written at any time. (Default: indeterminate)

	WDT_COUNT																															Base + 0x08
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																TCNT															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

15.3.2.4 Watchdog Control Register(WDT_CONTROL,0x0C)

The TCSR1 is a 16-bit read/write register. It contains the control bits for each channel. It is initialized to 0x00 by any reset.

	WDT_CONTROL																															Base + 0x0C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																					CLRZ	Reserved				PRESCALE			Reserved	RTC_EN	Reserved
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

<table>
<tr><th>Bits</th><th>Name</th><th>Description</th><th>RW</th></tr>
<tr><td>31:11</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td>R</td></tr>
<tr><td>10</td><td>CLRZ</td><td>Clear counter to 0. It is only used in TCU2 mode.
Writing 1 to this bit will clear the counter to 0. When the counter is finished setting to 0, it will be cleared by hardware.
Writing 0 to this bit will be ignored.</td><td>RW</td></tr>
<tr><td>9:6</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td>R</td></tr>
<tr><td>5:3</td><td>PRESCALE</td><td>These bits select the TCNT count clock frequency. Don’t change this field when the channel is running.
<table>
<tr><th>Bit 2</th><th>Bit1</th><th>Bit 0</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Internal clock: CLK/1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Internal clock: CLK/4</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Internal clock: CLK/16</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Internal clock: CLK/64</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Internal clock: CLK/256</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Internal clock: CLK/1024</td></tr>
<tr><td colspan="3">110~111</td><td>Reserved</td></tr>
</table></td><td>RW</td></tr>
<tr><td>2</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td>R</td></tr>
<tr><td>1</td><td>RTC_EN</td><td>Select RTCCLK as the timer clock input.
0: Disable 1: Enable</td><td>RW</td></tr>
<tr><td>0</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td>R</td></tr>
</table>

NOTE: The input clock of timer and the PCLK should keep to the rules as follows:

Input clock of timer: IN_CLK	**Clock generated from the frequency divider (PRESCALE): DIV_CLK**
PCK_EN == 0, RTC_EN == 1 and EXT_EN == 0 (IN_CLK = RTCCLK)	$f_{DIV_CLK} < ½ f_{PCLK}$
PCK_EN == 0, RTC_EN == 0 and EXT_EN == 1 (IN_CLK = EXTAL)	$f_{DIV_CLK} < ½ f_{PCLK}$
PCK_EN == 1, RTC_EN == 0 and EXT_EN == 0 (IN_CLK = PCLK)	ANY

15.4 Watchdog Timer Function

Step1:use CLEARZ to clear the counter.(use register 0x0c)

Step2: send a initial value for counter.(use register 0x08)

Step3: it must use inner clock, choose the clock, and choose the prescale.(use register 0x0c)

Step6: enable WDT counter.(use register 0x04)

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

16 Real Time Clock

16.1 Overview

The Real-Time Clock (RTC) unit can be operated in either chip main power is on or the main power is down but the RTC power is still on. In this case, the RTC power domain consumes only a few micro watts power.

The RTC contains a real time, alarm logic and the power down and wakeup control logic.

16.2 Features

- Embedded 32768Hz oscillator for 32k clock generation with an external 32k crystal
- 32-bits second counter
- Programmable and adjustable counter to generate accurate 1 Hz clock
- Alarm interrupt, 1Hz interrupt
- Stand alone power supply, work in hibernating mode
- Power down controller
- Alarm wakeup
- External pin wakeup with up to 2s glitch filter

16.3 Block Diagram

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

16.4 Pins Description

RTC has 6 signal IO pins and 1 power pin. They are listed and described in.

Pin Names	Pin Loc	IO	IO Cell Char.	Pin Description	Power
RTCLK		AI	32768Hz	RTCLK: 32768 clock input or OSC input	VDDRTC33
XRTCLK		AO		XRTCLK: OSC output	VDDRTC33
PWRON		O		PWRON: Power on/off control of main power	VDDRTC33
WKUP_		I	Schmitt	WKUP_: Wake signal after main power down	VDDRTC33
PPRST_		I	Schmitt	PPRST_: RTC power on reset and RESET-KEY reset input	VDDRTC33
VDDRTC33		P		VDDRTC33: 3.3V power for RTC and hibernating mode controlling that never power down (normally you can use 1.8V instead to reduce power consumption)	-
VDDRTC11		P		VDDRTC11: 1.1V power for RTC logic power	

RTCLK pin. need input 32.768KHz rtc clock. If do not use any clock, hibernate mode will be NOT available any more, and the time will lose if power down.

PWRON pin: this pin is used to control the main power on/off. Output high voltage means on and low voltage means off.

WKUP_ pin: hibernating mode wakeup input. (low active)

PPRST_ pin: This pin should be set to low voltage only in two cases.

- When RTC power is turned on. (so that whole chip is power on)
- A RESET-KEY is pressed.

16.5 Registers Description

Following chapter will descript the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. The registers can be read and written by APB bus
3. Register read/write attribute

   R - Read only

   W - Write only

   RW - read and write

   RCW - read and write, but clear to 0 by read

   RSW - read and write, but set to 1 by read

   RWC - read and write, clear to 0 by write 1, write 0 has no effect

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

RWS - read and write, set to 1 by write 1, write 0 has no effect
RC - read only, and clear to 0 by read
RS - read only, and set to 1 by read
SPEC - special access method, relate to its description

4. Reset Value

1 - reset to 1
0 - reset to 0
? - value unknown after reset

Table 16-1 Registers Memory Map-Address Base

Name	Base	Description
RTC	0x10003000	Address base of RTC

Table 16-2 Registers for real time clock

Name	Description	Reset Value	Address offset	Access Size
RTCCR	RTC Control Register	0x000000??*[1]*[2]	0x000	32
RTCSR	RTC Second Register	0x????????	0x004	32
RTCSAR	RTC Second Alarm Register	0x????????	0x008	32
RTCGR	RTC Regulator Register	0x0???????	0x00C	32

NOTES:

1 *[1]: Unless otherwise stated, the reset value is for PPRST_ and Hibernating wakeup reset.
WDT reset doesn't change the value.

2 *[2]: The reset value can be either of 0x00000081, 0x00000091, 0x00000089, 0x00000099.

Table 16-3 Registers for hibernating mode

Name	Description	Reset Value	Address offset	Access Size
HCR	Hibernate Control Register	0x00000000*[1]	0x020	32
HWFCR	Wakeup filter counter Register in Hibernate mode	0x0000???0	0x024	32
HRCR	Hibernate reset counter Register in Hibernate mode	0x00000??0	0x028	32
HWCR	Wakeup control Register in Hibernate mode	0x2d52d2d0*[1]	0x02C	32
HWRSR	Wakeup Status Register in	0x00000???*[1]	0x030	32

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Hibernate mode			
HSPR	Scratch pattern register	0x????????	0x034	32
WENR	Write enable pattern register	0x00000000	0x03C	32
WKUPPINCR	Configure the extend press WKUP pin to reset chip	0x00050064	0x048	32

NOTE:

*[1]: Unless otherwise stated, the reset value is for PPRST_ and Hibernating wakeup reset. WDT reset doesn't change the value.

All these registers, include those for real time clock and for hibernating mode control, except otherwise stated, are implemented in RTCLK clock domain. When write to these registers, it needs about 1 ~ 2 RTCLK cycles to actually change the register's value and needs another RTCLK cycle to allow the next write access. A bit RTCCR.WRDY is used to indicate it. When RCR.WRDY is 1, it means the previous write is finished, a right value can be read from the target register, and a new write access can be issued. So before any write access, please make sure RCR.WRDY = 1.

16.5.1 RTC Control Register (RTCCR)

RTCCR contains bits to configure the real time clock features. Unless otherwise stated, the reset value is for PPRST_ and Hibernating wakeup reset. WDT reset doesn't change the value.

	RTCCR																															BASE + 0x000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								WRDY	1HZ	1HZIE	AF	AIE	AE	SELEXC	RTCE
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1*[1]	0	0*[1]	?	0	?	0*[1]	1

NOTE:

*[1]: These bits are reset in all resets: PPRST_ input pin reset, hibernating reset and WDT reset.

Bits	Name	Description	RW
31:7	Reserved	Writing has no effect, read as zero.	R
7	WRDY	Write ready flag. It is 0 when a write is currently processing and the value has not been written to the writing target register. No write to any RTC registers can be issued in this case, or the result is undefined. The read value from the target register is also undefined. The reading is meaningful and another write can be issued when it is 1. This bit is read	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		only and write to it is ignored.	
6	1HZ	1Hz flag. This bit is set by hardware once every 1 second through the 1Hz pulse if the real time clock is enabled (RTCCR.RTCE = 1). This bit can be cleared by software. Write 1 to this bit is ignored.	RW
5	1HZIE	1Hz interrupt enable. Writing to this bit takes effect immediately without delay. **1HZIE** / **Description** 0: 1Hz interrupt is disabled. 1: 1Hz interrupt is enabled. RTC issues interrupt when 1HZ bit is set.	RW
4	AF	Alarm flag. This bit is set by hardware when alarm match (RTCSR = RTCSAR) is found and alarm is enabled (RTCCR.AE = 1) and the real time clock is enabled (RTCCR.RTCE = 1). This bit can be cleared by software. Write 1 to this bit is ignored. Writing to this bit takes effect immediately.	RW
3	AIE	Alarm interrupt enable. **AIE** / **Description** 0: Alarm interrupt is disabled. 1: Alarm interrupt is enabled. RTC issues interrupt when AF is set.	RW
2	AE	Alarm enable. **AE** / **Description** 0: Alarm function is disabled. 1: Alarm function is enabled.	RW
1	Reserved	Writing has no effect, read as zero.	R
0	RTCE	Real time clock enable. **RTCE** / **Description** 0: Real time clock function is disabled. 1: Real time clock function is enabled.	RW

16.5.2 RTC Second Register (RTCSR)

RTCSR is a 32-bit width second counter. It can be read and write by software. It is increased by 1 at every 1Hz pulse if the real time clock is enabled (RTCCR.RTCE = 1). When read, it should be read continued more than once and take the value if the adjacent results are the same. RTCSR is not initialized by any reset.

	RTCSR																															BASE + 0x004
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RTCSR																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

16.5.3 RTC Second Alarm Register (RTCSAR)

RTCSAR serves as a second alarm register. Alarm flag (RTCCR.AF) is set to 1 when the RTCSR equals the RTCSAR in the condition of alarm is enabled (RTCCR.AE = 1) and the real time clock is enabled (RTCCR.RTCE = 1). RTCSAR can be read and write by software and is not initialized by any reset.

	RTCSAR																															BASE + 0x008
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RTCSAR																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

16.5.4 RTC Regulator Register (RTCGR)

RTCGR is serves as the real time clock regulator, which is used to adjust the interval of the 1Hz pulse.

	RTCGR																															BASE + 0x00C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LOCK	Reserved					ADJC										NC1HZ															
RST	0*[1]	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

NOTE:

*[1]: This bit is reset in all resets: PPRST_ input pin reset, hibernating reset and WDT reset.

Bits	Name	Description	RW
31	LOCK	Lock bit. This bit is used to safeguard the validity of the data written into the RTCGR register. Once it is set, write to RTCGR is ignored. This bit can only be set by software and cleared by (any type of) resets. **LOCK** / **Description** 0 / Write to RTCGR is allowed. 1 / Write to RTCGR is forbidden.	RW
30:26	Reserved	Writing has no effect, read as zero.	R
25:16	ADJC	This field specifies how many times it needs to add one 32kHz cycle for the 1Hz pulse interval in every 1024 1Hz pulses. In other words, among every 1024 1Hz pulses, ADJC number of them are trigged in every (NC1HZ + 2) 32kHz clock cycles, (1024 – ADJC) number of them are	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		trigged in every (NC1HZ + 1) 32kHz clock cycles.	
15:0	NC1HZ	This field specifies the number plus 1 of the working 32kHz clock cycles are contained in the 1Hz pulse interval. In other words, 1Hz pulse is trigged every (NC1HZ + 1) 32kHz clock cycles, if RTCGR.ADJC = 0.	RW

16.5.5 Hibernate Control Register (HCR)

HCR contains the bit to control the main chip power on/off. Unless otherwise stated, the reset value is for PPRST_ and Hibernating wakeup reset.

	HCR																															BASE + 0x020
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															PD
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect, read as zero.	R
0	PD	Power down or power on bit. Besides writing by CPU, this bit will be set to 1 if an unknown reason main power supply off is detected. This bit controls the PWRON pin level. When co-working with some external components, this bit is used for power management of this chip. It is supposed when 1 is written to this bit, the main power supply of the chip, except RTC power, will be shut down immediately. After this bit is set to 1, all registers in RTC module, except RTCCR.1HZ and RTCCR.1HZIE, cannot be changed by write access. This bit is cleared by reset pin reset and hibernating reset. The later one is asserted by wakeup procedure. **PD** / **PWRON** / **Description** 0 / VDDRTC33 / No power down, keep power on. 1 / 0 V / Power down enable, turn power off.	RW

16.5.6 HIBERNATE mode Wakeup Filter Counter Register (HWFCR)

The HIBERNATE mode Wakeup Filter Counter Register (HWFCR) is a 32-bit read/write register .It filter the glitch generated by a dedicated wakeup pin. The HWFCR is not initialized by any reset.

	HWFCR																															BASE + 0x024
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Reserved																HWFCR											Reserved				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:5	HWFCR	Wakeup pin effective minimum time in number of 32 RTCLK cycles, used as glitch filter logic. Maximum of 2 seconds if the RTCLK is 32768Hz If this value is configured to 0, and the WKUP pin keeps low longer than 15 RTCLK periods, it will wakes up RTC from Hibernate. The glitch filter time equals to HWFCR*32 RTCLK period.	RW
4:0	Reserved	Writing has no effect, read as zero.	R

16.5.7 Hibernate Reset Counter Register (HRCR)

The Hibernate Reset Counter Register is a 32-bit read/write register that specifies hibernate reset assertion time. The HRCR is initialized by PPRST_ .

	HRCR																															**BASE + 0x028**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																	HRCR				Reserved										
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:15	Reserved	Writing has no effect, read as zero.	R
14:11	HRCR	HIBERNATE Reset asserting time. Number of 2048 RTCLK cycles. Default value 0x1, assert 125 ms. Maximum 1 second if the RTCLK is 32768Hz. If this value is configured to 0, it will generate 2048 RTCLK HIBERNATE Reset, about 62.5 milliseconds.	RW
10:0	Reserved	Writing has no effect, read as zero.	R

16.5.8 HIBERNATE Wakeup Control Register (HWCR)

The HIBERNATE Wakeup Control Register is a 32-bit read/write register that controls real time clock alarm wake up enable. The reset value only for PPRST_ .

	HWCR	**BASE + 0x02C**

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EPDET																													Reserved		EALM
RST	0	0	1	0	1	1	0	1	0	1	0	1	0	0	1	0	1	1	0	1	0	0	1	0	1	1	0	1	0	0	0	0*[1]

NOTE:

*[1]: This bit is reset in PPRST_ input pin reset and hibernating reset .

Bits	Name	Description	RW
31:3	EPDET	Power detect enable. 0x5aa5a5a: enable(default) 0x1a55a5a5: disable Only 0x1a55a5a5 can disable power detect, other values will enable the power detect.	RW
2:1	Reserved	Writing has no effect, read as zero.	R
0	EALM	RTC Alarm wakeup enable. 0: disable 1: enable	RW

16.5.9 HIBERNATE Wakeup Status Register (HWRSR)

The HIBERNATE Wakeup Status Register is a 32-bit read/write register that reflects wakeup status bits.

	HWRSR																															BASE + 0x030
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																							APD	Reserved		HR	PPR	Reserved		PIN	ALM
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	0	0	1*[2]	1*[1]	0	0	?	?

NOTES:

*[1]: This reset value only for PPRST_. It is undefined in case of other resets.

*[2]: This reset value only for HRST_. It is undefined in case of other resets.

Bits	Name	Description	RW
31:9	Reserved	Writing has no effect, read as zero.	R
8	APD	Accident power down. When the software has not set to HIBERNATE state, the core power is down, then an accident power down is detected. APD is set and remains set until software clears it. This bit can only be written with 0. Write with 1 is ignored.	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		HR / **Description** 0 / Accident power down has not occurred since the last time the software clears this bit. 1 / Accident power down has occurred since the last time the software clears this bit.	
7:6	Reserved	Writing has no effect, read as zero.	R
5	HR	Hibernate Reset. When a Hibernate reset detected, HR is set and remains set until software clears it. This bit can only be written with 0. Write with 1 is ignored. **HR** / **Description** 0 / Hibernate reset has not occurred since the last time the software clears this bit. 1 / Hibernate reset has occurred since the last time the software clears this bit.	RW
4	PPR	PAD PIN Reset. When a PPRST_ is detected, PPR is set and remains set until software clears it. This bit can only be written with 0. Write with 1 is ignored. **PPR** / **Description** 0 / PPRST_ reset has not occurred since last time the software clears this bit. 1 / PPRST_ reset has occurred since last time the software clears this bit.	RW
3:2	Reserved	Writing has no effect, read as zero.	R
1	PIN	Wakeup Pin Status bit. The bit is cleared when chip enters hibernating mode. It is set when exit the hibernating mode by wakeup pin. This bit can only be written with 0. Write with 1 is ignored.	RW
0	ALM	RTC Alarm Status bit. The bit is cleared when chip enters hibernating mode. It is set when exit the hibernating mode by alarm. This bit can only be written with 0. Write with 1 is ignored.	RW

16.5.10 Hibernate Scratch Pattern Register (HSPR)

This is a scratch register used to hold a pattern. The software can check the pattern is kept to know whether RTC power has ever been down and whether it is needed to setup the real time clock.

	HSPR																															**BASE + 0x034**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PAT																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:0	PAT	The pattern.	RW

16.5.11 Write Enable Pattern Register (WENR)

This is a write protect register to may the rtc registers can write only in certain condition.

	WENR																															BASE + 0x03C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WEN	Reserved															WENPAT															
RST	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31	WEN	The write enable flag. If the WENPAT is 0xA55A then this bit will be 1. When the WEN changes to 1, the RTCCR, RTCSR, RTCSAR, RTCGR, HCR, HWFCR, HRCR, HWCR, HWRSR, HSPR registers could be changed. But RTCCR.SELEXC, RTCCR.HZIE, RTCCR.WRDY may change in any time. This bit is read only and write to it is ignored. This bit only reset by PPRST_ and HRST_. <table><tr><th>WEN</th><th>Description</th></tr><tr><td>0</td><td>Other RTC registers is locked, write these registers will be ignored.</td></tr><tr><td>1</td><td>Other RTC registers can be changed.</td></tr></table>	R
30:16	Reserved	Writing has no effect, read as zero.	R
15:0	WENPAT	The write enable pattern. Before writing any value to RTCCR, RTCSR, RTCSAR, RTCGR, HCR, HWFCR, HRCR, HWCR, HWRSR, HSPR registers, write 0xA55A to WENPAT to set these register writable. If this value is ok, WEN will change to 1. But RTCCR.HZIE are writable in any time. These bits are write-only, always read as 0.	W

16.5.12 WKUP_PIN_RST control register (WKUPPINCR)

This is a register used to control the enable and set the judge time to reset the chip when extend press the WKUP pin. The are only initialized by PPRST_ and HRST_.

	WKUPPINCR																															BASE + 0x048
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Reserved												OSC_TE	OSC_RETON	Reserved	OSC_EN	Reserved								P_JUD_LEN				P_RST_EN			
RST	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0

Bits	Name	Description	RW
31:20	Reserved	Writing has no effect, read as zero.	R
19	OSC_TE	RTC oscillator PAD Test enable (Keep default).	RW
18	OSC_RETON	0: RTC oscillator XRTCLK keep low. 1: RTC oscillator XRTCLK follow RTCLK.	RW
17	Reserved	Writing has no effect.	RW
16	OSC_EN	RTC internal oscillator enable 1: enable 0: disable	RW
15:5	Reserved	Writing has no effect, read as zero.	R
7:4	P_JUD_LEN	WKUP up pin extend press length judge value The judge time equals to FLT_LEN multiply RTC 1HZ period, and only the active press length equal or greater than judge time, the chip reset can assert.	RW
3: 0	P_RST_EN	Enable reset chip by extend press WKUP pin Others value: disable 4'hB: enable	RW

16.6 Operation Flow

16.6.1 Registers Access

16.6.1.1 Registers Read

All registers can read directly, but the RTCSR and RTCSAR should be read continued more than once and take the value if the adjacent results are the same. Please check and make sure RTCCR.WRDY equals to 1 before execute a register read.

16.6.1.2 Registers Write

Only the RTCCR.SELEXC, RTCCR.HZIE, RTCGR.LOCK, WENR.WENPAT bits can write directly.

Others bits need following the below procedure

1) Check RTCCR.WRDY, make sure it equals to 1
2) Write 0xa55a to WENR register to enable other registers write.
3) Waiting WENR.WEN change to 1
4) Check RTCCR.WRDY, make sure it equals to 1
5) Write the target register

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

6) Waiting RTCCR.WRDY equals to 1 to make sure the current write processing was finished.

16.6.2 Normal Mode

16.6.2.1 Power Detect

When PPRST_ reset, the HWCR.EPDET set to 0x5aa5a5a, and the power detect is enable. If you want To disable the power detect, you should set HWCR.EPDET to 0x1a55a5a5. If power detect is enable, when CORE power supply was lose, the RTC will into hibernate mode. And if power detect is not enable, the RTC can't enter hibernate mode even CORE power supply was lose.

16.6.2.2 Power On Timing Diagram

The RTC power on procedure likes the following figure.

Figure 16-1 Core Power On

16.6.3 HIBERNATE Mode

The purpose of hibernate mode is to save the power. When in hibernate mode, CORE will no power consumption.

If you want to use hibernate mode, please first make sure RTCCR.SELEXC is 0.
When Software writes 1 to PD bit of HCR, the system at once enters HIBERNATE mode. The powers of CORE and IO are disconnected by PWRON pin, no power consumption in core and IO. When a wakeup event occurs, the core enters normal mode through a hibernate reset.

16.6.3.1 Procedure to Enter HIBERNATE mode

Before enter HIBERNATE mode, software must complete following steps:

1 Finish the current operation and preserve all data to flash.
2 Configure the wake-up sources properly by configure HWCR.
3 Set HIBERNATE MODE. (Set PD bit in HCR to 1)

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

16.6.3.2 Procedure to Wake-up from HIBERNATE mode

1. The internal hibernate reset signal will be asserted if one of the wake-up sources is issued.
2. Check RSR to determine what caused the reset.
3. Check PIN/ALM bits of HWRSR in order to know whether or not the power-up is caused by which wake-up from HIBERNATE mode.
4. Configure the SDRAM memory controller.
5. Recover the data from flash.

16.6.4 Time Regulation

Because of the inherent inaccuracy of crystal and other variables, the time counter may be inaccurate. This requires a slight adjustment. The application processor, through the RTCGR, lets you adjust the 1Hz time base to an error of less than 1ppm. Such that if the Hz clock were set to be 1Hz, there would be an error of less than 5 seconds per month.

To determine the value programmed into the RTCGR, you must first measure the output frequency at the oscillator multiplex (approximately 32 kHz) using an accurate time base, such as a frequency counter. This clock is externally visible by selecting the alternate function of GPIO.
To gain access to the clock, program this pin as an output and then switch to the alternate function. To trim the clock, divide the output of the oscillator by an integer value and fractional adjust it by periodically deleting clocks from the stream driving this integer divider.

After the true frequency of the oscillator is known, it must be split into integer and fractional portions. The integer portion of the value (minus one) is loaded into the NC1HZ field of the RTCGR.

The fractional part of the adjustment is done by periodically deleting clocks from the clock stream driving the Hz divider. The trim interval period is hardwired to be 1024 1Hz clock cycles (approximately 17 minutes). The number of clocks (represented by ADJC field of RTCGR) are deleted from the input clock stream per trim interval. If ADJC is programmed to be zero, then no trim operations occur and the RTC is clocked with the raw 32 kHz clock. The relationship between the Hz clock frequency and the nominal 32 kHz clock (f1 and f32K, respectively) is shown in the following equation.

$$f1 = \frac{2^{10} \times (NC1HZ + 1)}{2^{10} \times (NC1HZ + 1) + ADJC} \times \frac{f32k}{NC1HZ + 1}$$

f1 = actual frequency of 1Hz clock
f32k = frequency of either 32.768KHz crystal output or 3.6864MHz crystal output further divided down to 32.914KHz

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

16.6.5 Clock select

There could be two clock input to TCU/USB/CPM called rtclk. One is OSC32k clock; the other is EXCLK/512.

The software MUST make sure the RTC run in valid clock configuration.

Table 16-4 Clock select registers

CPM.ERCS	Description	Valid
0	RTC use EXCLK/512 clock.	OK
1	RTC use OSC32K clock.	OK

Changing RTCLK sequence:

1. There are both 32KHz crystal and 24Mhz EXCLK crystal connected, so RTCLK input path has 32Khz clock.
   In this case, you can set OPCR.ERCS of CPM to 1, the rtclk of TCU/USB/CPM becomes OSC32K

2. There is no 32KHz crystal connected but only 24Mhz EXCLK crystal connected, so RTCLK input path has no clock, the RTC function is not available.
   In this case, OPCR.ERCS Keep default.

NOTE: If using HIBERNATE mode, MUST have both 32KHz crystal (or input 32Khz clock) and 24Mhz EXCLK crystal connected, or RTC time will be insignificant.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

17 Interrupt Controller

17.1 Overview

This chapter describes the interrupt controller included in the XBurst Processor, explains its modes of operation, and defines its registers. The interrupt controller controls the interrupt sources available to the processor and contains the location of the interrupt source to allow software to determine source of all interrupts. It also determines whether an IRQ occurs or not and masks the interrupts.

Features:

- Total 64 interrupt sources
- INTC0, INTC1 for CPU core
- INTC4 for PDMA
- Each interrupt source can be independently enabled
- Priority mechanism to indicate highest priority interrupt
- INTC 4's Unmasked interrupts can wake up the chip in sleep mode

17.2 Register Description

Following chapter will descript the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. Register read/write attribute
   R - Read only
   W - Write only
   RW - read and write
   RCW - read and write, but clear to 0 by read
   RSW - read and write, but set to 1 by read
   RWC - read and write, clear to 0 by write 1, write 0 has no effect
   RWS - read and write, set to 1 by write 1, write 0 has no effect
   RC - read only, and clear to 0 by read
   RS - read only, and set to 1 by read
   SPEC - special access method, relate to its description
3. Reset Value
   1 - reset to 1
   0 - reset to 0
   ? - value unknown after reset

Table 17-1 Registers Memory Map-Address Base

Name	Base	Description
INTC	0x10001000	Address base of INTC

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Table 17-2 lists the registers of Interrupt Controller. All of these registers are 32bit, and each bit of the register represents or controls one interrupt source that list in Table 17-2.

Table 17-2 INTC Register

Name	Description	RW	Reset Value	Address offset	Access Size
ICSR0	IRQ Source Register	R	0x00000000	0x00	32
ICMR0	IRQ Mask Register	RW	0xFFFFFFFF	0x04	32
ICMSR0	IRQ Mask Set Register	W	0x????????	0x08	32
ICMCR0	IRQ Mask Clear Register	W	0x????????	0x0C	32
ICPR0	IRQ Pending Register	R	0x00000000	0x10	32
ICSR1	IRQ Source Register	R	0x00000000	0x20	32
ICMR1	IRQ Mask Register	RW	0xFFFFFFFF	0x24	32
ICMSR1	IRQ Mask Set Register	W	0x????????	0x28	32
ICMCR1	IRQ Mask Clear Register	W	0x????????	0x2C	32
ICPR1	IRQ Pending Register	R	0x00000000	0x30	32
DSR0	IRQ Source Register0 for PDMA	R	0x00000000	0x34	32
DMR0	IRQ Mask Register0 for PDMA	RW	0xFFFFFFFF	0x38	32
DPR0	IRQ Pending Register0 for PDMA	R	0x00000000	0x3C	32
DSR1	IRQ Source Register1 for PDMA	R	0x00000000	0x40	32
DMR1	IRQ Mask Register1 for PDMA	RW	0xFFFFFFFF	0x44	32
DPR1	IRQ Pending Register1 for PDMA	R	0x00000000	0x48	32

17.2.1 Interrupt Controller Source Register (ICSR0)

This register contains all the interrupts' status. A "1" indicates that the corresponding interrupt is pending . A "0" indicates that the interrupt is not pending now. The register is read only.

	ICSR0																															0x10001000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LCD	CIM	Reserved	MIPI_CSI	TCU0	TCU1	TCU2	Reserved	AES	HASH	Reserved	Reserved	Reserved	Reserved	GPIO0	GPIO1	GPIO2	GPIO3	Reserved	Reserved	SADC	Reserved	SSI0	Reserved	SFC	PWM	PDMAM	PDMAD	PDMA	Reserved	USB_OTG	AUDIO
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits Of ICSR0	Description
0	The corresponding interrupt source is not pending.
1	The corresponding interrupt source is pending.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

17.2.2 Interrupt Controller Source Register (ICSR1)

This register contains all the interrupts' status. A "1" indicates that the corresponding interrupt is pending . A "0" indicates that the interrupt is not pending now. The register is read only.

	ICSR1																															0x10001020
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	SSI_SLV	I2C0	I2C1	Reserved	Reserved	Reserved	Reserved	GMAC	EFUSE	Reserved	DDR	CPM	HARB0	HARB2	Reserved	UART0	UART1	UART2	UART3	Reserved	CDBUS	CAN1	CAN0	Reserved	Reserved	MSC0	MSC1	Reserved	DTRNG	SOFT	RTC
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits Of ICSR1	Description
0	The corresponding interrupt source is not pending.
1	The corresponding interrupt source is pending.

17.2.3 Interrupt Controller Mask Register (ICMR0)

This register is used to mask the interrupt input sources and defines which active sources are allowed to generate interrupt requests to the processor. Its value can be changed either by writing ICMSR and ICMCR or by writing itself. The masked interrupts are invisible to the processor.

	ICMR0																															0x10001004
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LCD	CIM	Reserved	MIPI_CSI	TCU0	TCU1	TCU2	Reserved	AES	HASH	Reserved	Reserved	Reserved	Reserved	GPIO0	GPIO1	GPIO2	GPIO3	Reserved	Reserved	SADC	Reserved	SSI0	Reserved	SFC	PWM	PDMAM	PDMAD	PDMA	Reserved	USB_OTG	AUDIO
RST	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits Of ICMR0	Description
0	The corresponding interrupt is not masked.
1	The corresponding interrupt is masked.

17.2.4 Interrupt Controller Mask Register (ICMR1)

This register is used to mask the interrupt input sources and defines which active sources are allowed to generate interrupt requests to the processor. Its value can be changed either by writing ICMSR and ICMCR or by writing itself. The masked interrupts are invisible to the processor.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	ICMR1																															0x10001024
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	SSI_SLV	I2C0	I2C1	Reserved	Reserved	Reserved	Reserved	GMAC	EFUSE	Reserved	DDR	CPM	HARB0	HARB2	Reserved	UART0	UART1	UART2	UART3	Reserved	CDBUS	CAN1	CAN0	Reserved	Reserved	MSC0	MSC1	Reserved	DTRNG	SOFT	RTC
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits Of ICMR1	Description
0	The corresponding interrupt is not masked.
1	The corresponding interrupt is masked.

17.2.5 Interrupt Controller Mask Set Register (ICMSR0)

This register is used to set bits in the interrupt mask register. This register is write only.

	ICMSR0																															0x10001008
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LCD	CIM	Reserved	MIPI_CSI	TCU0	TCU1	TCU2	Reserved	AES	HASH	Reserved	Reserved	Reserved	Reserved	GPIO0	GPIO1	GPIO2	GPIO3	Reserved	Reserved	SADC	Reserved	SSI0	Reserved	SFC	PWM	PDMAM	PDMAD	PDMA	Reserved	USB_OTG	AUDIO
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits Of ICMSR0	Description
0	Ignore.
1	Will set the corresponding interrupt mask bit.

17.2.6 Interrupt Controller Mask Set Register (ICMSR1)

This register is used to set bits in the interrupt mask register. This register is write only.

	ICMSR1																															0x10001028
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	SSI_SLV	I2C0	I2C1	Reserved	Reserved	Reserved	Reserved	GMAC	EFUSE	Reserved	DDR	CPM	HARB0	HARB2	Reserved	UART0	UART1	UART2	UART3	Reserved	CDBUS	CAN1	CAN0	Reserved	Reserved	MSC0	MSC1	Reserved	DTRNG	SOFT	RTC
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits Of ICMSR1	Description
0	Ignore.
1	Will set the corresponding interrupt mask bit.

17.2.7 Interrupt Controller Mask Clear Register (ICMCR0)

This register is used to clear bits in the interrupt mask register. This register is write only.

	ICMCR0																															0x1000100C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LCD	CIM	Reserved	MIPI_CSI	TCU0	TCU1	TCU2	Reserved	AES	HASH	Reserved	Reserved	Reserved	Reserved	GPIO0	GPIO1	GPIO2	GPIO3	Reserved	Reserved	SADC	Reserved	SSI0	Reserved	SFC	PWM	PDMAM	PDMAD	PDMA	Reserved	USB_OTG	AUDIO
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits Of ICMCR0	Description
0	Ignore.
1	Will clear the corresponding interrupt mask bit.

17.2.8 Interrupt Controller Mask Clear Register (ICMCR1)

This register is used to clear bits in the interrupt mask register. This register is write only.

	ICMCR1																															0x1000102C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	SSI_SLV	I2C0	I2C1	Reserved	Reserved	Reserved	Reserved	GMAC	EFUSE	Reserved	DDR	CPM	HARB0	HARB2	Reserved	UART0	UART1	UART2	UART3	Reserved	CDBUS	CAN1	CAN0	Reserved	Reserved	MSC0	MSC1	Reserved	DTRING	SOFT	RTC
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits Of ICMCR1	Description
0	Ignore.
1	Will clear the corresponding interrupt mask bit.

17.2.9 Interrupt Controller Pending Register (ICPR0)

This register contains the status of the interrupt sources after masking. This register is read only.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

ICPR0																																0x10001010
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LCD	CIM	Reserved	MIPI_CSI	TCU0	TCU1	TCU2	Reserved	AES	HASH	Reserved	Reserved	Reserved	Reserved	GPIO0	GPIO1	GPIO2	GPIO3	Reserved	Reserved	SADC	Reserved	SSI0	Reserved	SFC	PWM	PDMAM	PDMAD	PDMA	Reserved	USB_OTG	AUDIO
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits Of ICPR0	Description
0	The corresponding interrupt is not active or is masked.
1	The corresponding interrupt is active and is not masked to the processor.

17.2.10 Interrupt Controller Pending Register (ICPR1)

This register contains the status of the interrupt sources after masking. This register is read only.

ICPR1																																0x10001030
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	SSI_SLV	I2C0	I2C1	Reserved	Reserved	Reserved	Reserved	GMAC	EFUSE	Reserved	DDR	CPM	HARB0	HARB2	Reserved	UART0	UART1	UART2	UART3	Reserved	CDBUS	CAN1	CAN0	Reserved	Reserved	MSC0	MSC1	Reserved	DTRNG	SOFT	RTC
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits Of ICPR1	Description
0	The corresponding interrupt is not active or is masked.
1	The corresponding interrupt is active and is not masked to the processor.

17.2.11 Interrupt Source Register0 for PDMA (DSR0)

This register contains status of all interrupts. A “1” indicates the corresponding interrupt is pending. The register is read only.

DSR0																																0x10001034
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	LCD	CIM	Reserved	MIPI_CSI	TCU0	TCU1	TCU2	Reserved	AES	HASH	Reserved	Reserved	Reserved	Reserved	GPIO0	GPIO1	GPIO2	GPIO3	Reserved	Reserved	SADC	Reserved	SSI0	Reserved	SFC	PWM	PDMAM	PDMAD	PDMA	Reserved	USB_OTG	AUDIO
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits Of DSR0	Description
0	The corresponding interrupt source is not pending.
1	The corresponding interrupt source is pending.

17.2.12 Interrupt Mask Register0 for PDMA (DMR0)

This register is used to mask the interrupt input sources and defines which active sources are allowed to generate interrupt requests to the processor. The masked interrupts are invisible to the processor.

	DMR0																															**0x10001038**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LCD	CIM	Reserved	MIPI_CSI	TCU0	TCU1	TCU2	Reserved	AES	HASH	Reserved	Reserved	Reserved	Reserved	GPIO0	GPIO1	GPIO2	GPIO3	Reserved	Reserved	SADC	Reserved	SSI0	Reserved	SFC	PWM	PDMAM	PDMAD	PDMA	Reserved	USB_OTG	AUDIO
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits Of DMR0	Description
0	The corresponding interrupt source is not pending.
1	The corresponding interrupt source is pending.

17.2.13 Interrupt Pending Register0 for PDMA (DPR0)

This register contains the status of the interrupt sources after masking. This register is read only.

	DPR0																															**0x1000103C**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LCD	CIM	Reserved	MIPI_CSI	TCU0	TCU1	TCU2	Reserved	AES	HASH	Reserved	Reserved	Reserved	Reserved	GPIO0	GPIO1	GPIO2	GPIO3	Reserved	Reserved	SADC	Reserved	SSI0	Reserved	SFC	PWM	PDMAM	PDMAD	PDMA	Reserved	USB_OTG	AUDIO

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits Of ICPR0	Description
0	The corresponding interrupt is not active or is masked.
1	The corresponding interrupt is active and is not masked to the processor.

17.2.14 Interrupt Source Register1 to PDMA (DSR1)

This register contains status of all interrupts. A “1” indicates the corresponding interrupt is pending. The register is read only.

	DSR1																															**0x10001040**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	SSI_SLV	I2C0	I2C1	Reserved	Reserved	Reserved	Reserved	GMAC	EFUSE	Reserved	DDR	CPM	HARB0	HARB2	Reserved	UART0	UART1	UART2	UART3	Reserved	CDBUS	CAN1	CAN0	Reserved	Reserved	MSC0	MSC1	Reserved	DTRNG	SOFT	RTC
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits Of DSR1	Description
0	The corresponding interrupt source is not pending.
1	The corresponding interrupt source is pending.

17.2.15 Interrupt Mask Register1 for PDMA (DMR1)

This register is used to mask the interrupt input sources and defines which active sources are allowed to generate interrupt requests to the processor. The masked interrupts are invisible to the processor.

	DMR1																															**0x10001044**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	SSI_SLV	I2C0	I2C1	Reserved	Reserved	Reserved	Reserved	GMAC	EFUSE	Reserved	DDR	CPM	HARB0	HARB2	Reserved	UART0	UART1	UART2	UART3	Reserved	CDBUS	CAN1	CAN0	Reserved	Reserved	MSC0	MSC1	Reserved	DTRNG	SOFT	RTC
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits Of DMR1	Description
0	The corresponding interrupt is not masked.
1	The corresponding interrupt is masked.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

17.2.16 Interrupt Pending Register1 for PDMA (DPR1)

This register contains the status of the interrupt sources after masking. This register is read only.

	DPR1																															0x10001048
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	SSI_SLV	I2C0	I2C1	Reserved	Reserved	Reserved	Reserved	GMAC	EFUSE	Reserved	DDR	CPM	HARB0	HARB2	Reserved	UART0	UART1	UART2	UART3	Reserved	CDBUS	CAN1	CAN0	Reserved	Reserved	MSC0	MSC1	Reserved	DTRNG	SOFT	RTC
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits Of ICPR0	Description
0	The corresponding interrupt is not active or is masked.
1	The corresponding interrupt is active and is not masked to the processor.

17.3 Software Considerations

The interrupt controller is reflecting the status of interrupts sources in the peripheral.

Software should perform the task - determine the interrupt source from in ICPRx. In this chip, pending interrupts have two levels in structure. Interrupting module in the system that contains more than one interrupt sources need software to determine how to service it by reading interrupt status registers within it.

In the interrupt handler, the serviced interrupt source needs to be cleared in the interrupting device. In order to make certain the cleared source request status has been reflected at the corresponding ICPRx bit, software should wait enough time before exiting interrupt state.

The procedure is described following:

1. Interrupt generated.
2. CPU query interrupt sources, saves the current environment and then goes to interrupt common service routine.
3. Get ICPRx.
4. Find the highest priority interrupt and vector it. (The software decides which one has the highest priority)
5. Mask the chosen interrupt by writing the register ICMSRx.
6. Enable the system interrupt to allow the interrupt nesting. (software decided)
7. Execute the interrupt handler and unmask it by writing the register ICMCRx when exit the handler.
8. CPU restores the saved environment and exits the interrupt state.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

18 PDMA Controller

18.1 Overview

Programmable DMA controller (PDMAC) is dedicated to smartly transfer data between on-chip peripherals (MSC, AIC, UART, etc.), external memories, and memory-mapped external devices.

18.2 Features

- Support up to 32 independent DMA channels
- Descriptor or No-Descriptor Transfer mode compatible with previous JZ SOC
- A simple Xburst-1 CPU supports smart transfer mode controlled by programmable firmware
- Transfer data units: 1-byte, 2-byte, 4-byte, 16-byte, 32-byte, 64-byte, 128-byte
- Transfer number of data unit: 1 ~ 224 - 1
- Independent source and destination port width: 8-bit, 16-bit, 32-bit
- Fixed three priorities of channel groups: 0~3, highest; 4~11: mid; 12~31: lowest
- An extra INTC IRQ can be bound to one programmable DMA channel

18.3 Block Diagram

Figure 18-1 Block Diagram of PDMA

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

18.4 Memory Mapped Register Descriptions

18.4.1 DMA Channel Registers

Following chapter will descript the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. Register read/write attribute
   R - Read only
   W - Write only
   RW - read and write
   RCW - read and write, but clear to 0 by read
   RSW - read and write, but set to 1 by read
   RWC - read and write, clear to 0 by write 1, write 0 has no effect
   RWS - read and write, set to 1 by write 1, write 0 has no effect
   RC - read only, and clears to 0 by read
   RS - read only, and set to 1 by read
   SPEC - special access method, relate to its description
3. Reset Value
   1 - Reset to 1
   0 - reset to 0
   ? - Value unknown after reset

Table 18-1 Registers Memory Map-Address Base

Name	Base	Description
Channel n	0x13420000 + n*0x20	PDMA channel n.

Table 18-2 DMA Channel Registers (n=0~31)

Name	Description	Reset Value	Address offset	Access Size (bit)
DSAn	Channel n Source Address	0x?	0x00 + n*0x20	32
DTAn	Channel n Target Address	0x?	0x04 + n*0x20	32
DTCn	Channel n Transfer Count	0x?	0x08 + n*0x20	32
DRTn	Channel n Request Source	0x?	0x0C + n*0x20	32
DCSn	Channel n Control/Status	0x?	0x10 + n*0x20	32
DCMn	Channel n Command	0x?	0x14 + n*0x20	32
DDAn	Channel n Descriptor Address	0x?	0x18 + n*0x20	32
DSDn	Channel n Stride Difference	0x?	0x1C + n*0x20	32

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

18.4.2 Global Control Registers

Table 18-3 Registers Memory Map-Address Base

Name	Base	Description
GCR	0x13420000	PDMA global control registers.

Table 18-4 Global Control Registers

Name	Description	Reset Value	Address offset	Access Size (bit)
DMAC	DMA Control	0x0	0x1000	32
DIRQP	DMA Interrupt Pending	0x0	0x1004	32
DDB	DMA Doorbell	0x0	0x1008	32
DDS	DMA Doorbell Set	0x0	0x100C	32
DIP	Descriptor Interrupt Pending	0x0	0x1010	32
DIC	Descriptor Interrupt Clear	0x0	0x1014	32
DMACP	DMA Channel Programmable	0x0	0x101C	32
DSIRQP	Channel soft IRQ to MCU	0x0	0x1020	32
DSIRQM	Channel soft IRQ mask	0xffffffff	0x1024	32
DCIRQP	Channel IRQ to MCU	0x0	0x1028	32
DCIRQM	Channel IRQ to MCU mask	0xffffffff	0x102C	32
DMCS	MCU Control and Status	0xe1	0x1030	32
DMNMB	MCU Normal Mailbox	0x0	0x1034	32
DMSMB	MCU Security Mailbox	0x0	0x1038	32
DMINT	MCU Interrupt	0x3	0x103C	32

NOTES:

Grey ones are obsolete registers defined in previous JZ SOC. They are relative to clock gating and have no real function, and they are not supported any longer.

18.5 DMA Channel Register Definition

18.5.1 DMA Source Address (DSAn, n = 0 ~ 31)

	DSAn																BASE + 0x0 + (n*0x20)															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SA																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

31:0	SA	Source physical address.	RW

18.5.2 DMA Target Address (DTAn, n = 0 ~ 31)

	DTAn																															BASE + 0x4 + (n*0x20)
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TA																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:0	TA	Target physical address.	RW

18.5.3 DMA Transfer Count (DTCn, n = 0 ~ 31)

	DTCn																															BASE + 0x8 + (n*0x20)
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								TC																							
RST	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:24	Reserved	Write has no effect, read as zero.	R
23:0	TC	TC records the number of data unit to be transferred. Moreover, when Stride transfer mode is enabled, TC composes of two parts: the lower 16 bits is the number of data unit for sub-block transfer, the higher 8 bits is the number of sub-block. TC automatically counts down to 0 at the end. For tsz-ex-4w such external decide trans data unit type, TC minus 1 only if last signal assert which means TC indicate frameNum	RW

18.5.4 DMA Request Types (DRTn, n = 0 ~ 31)

	DRTn																															BASE + 0xC + (n*0x20)
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										RT					

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?

Bits	Name	Description	RW
31:6	Reserved	Write has no effect, read as zero.	R
5:0	RT	Transfer request type.	RW

Table 18-5 Transfer Request Types

RT5-0	Description
000000 ~ 000111	Reserved.
001000	Auto-request. (external address → external address)
001010	Can0 tx.
001011	Can0 rx fifo request. 4 or 1 word according to rx_single input port
001100	Can1 tx.
001101	Can1 rx.
001110	UART3 transmit-fifo-empty transfer request. (external address → UTHR)
001111	UART3 receive-fifo-full transfer request. (URBR → external address)
010000	UART2 transmit-fifo-empty transfer request. (external address → UTHR)
010001	UART2 receive-fifo-full transfer request. (URBR → external address)
010010	UART1 transmit-fifo-empty transfer request. (external address → UTHR)
010011	UART1 receive-fifo-full transfer request. (URBR → external address)
010100	UART0 transmit-fifo-empty transfer request. (external address → UTHR)
010101	UART0 receive-fifo-full transfer request. (URBR → external address)
010110	SSI0 transmit-fifo-empty transfer request.
010111	SSI0 receive-fifo-full transfer request.
011000	Reserved.
011001	Reserved.
100100	I2C0 transmit-fifo-empty transfer request.
100101	I2C0 receive-fifo-full transfer request.
100110	I2C1 transmit-fifo-empty transfer request.
100111	I2C 1 receive-fifo-full transfer request.
101000	Reserved.
101001	Reserved.
101010	SSI SLV transmit transfer request.
101011	SSI SLV receive transfer request.
101100 ~ 110011	PWM0~7 transfer request.
110100	MSC0 transmit-fifo-empty transfer request.
110101	MSC0 receive-fifo-full transfer request.
110110	MSC1 transmit-fifo-empty transfer request.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

110111	MSC1 receive-fifo-full transfer request.
111000	SADC receive request
111001~111100	reserved
111101 ~ 111111	AIC TL/T/R request

NOTES:

1 Only auto request can be concurrently set in all channels with different source and target add1ress.

2 For on-chip device DMA request, the corresponding source or target address that map to on-chip device must be set as fixed.

18.5.5 DMA Channel Control/Status (DCSn, n = 0 ~ 31)

	DCSn																BASE + 0x10 + (n*0x20)															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	NDES	DES8															CDOA										STOP	AR	TT	HLT		CTE
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	NDES	Descriptor or No-Descriptor Transfer Select. 0: Descriptor Transfer; 1: No-descriptor Transfer.	RW
30	DES8	Descriptor 8 Word. 0: 4-word descriptor; 1: 8-word descriptor.	RW
29:16	Reserved	Write has no effect, read as zero.	R
15:8	CDOA	Copy of offset address of last completed descriptor from that in DMA command register. (The field is Ignored in No-Descriptor Transfer)	RW
7:6	Reserved	Write has no effect, read as zero.	R
5	Stop	Software set 1 to require ch-dma stop current transfer, right after sw set1, ch-desc/dma request and peripheral request would be block(ch-dma signal for ahb/apb request), then software polling if this bit is set, if set, it means hardware find curr-channel descriptor or normal dma mission have reach to stable state which is not using bus; Software can clear other register to cancel not finished ch-desc/dma command(eg. STOP, TT, CTE) Note: one time only one channel can co-operate with software to do stop action, software should ensure current stop action finished then start new one, otherwise the result is unpredictable.	RW
4	AR	Address Error. Hardware set it to 1 and software clear it to 0.	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		0: no address error; 1: address error occurred.	
3	TT	Transfer Terminate. 0: Descriptor or No-Descriptor DMA transfer does not end 1: No-Link Descriptor or No-Descriptor DMA transfer end	RW
2	HLT	DMA halt. Hardware sets it to 1 when an abnormal case occurs during transfer, then software has to clear it to 0 for re-using the channel later.	RW
1	Reserved	Write has no effect, read as zero.	R
0	CTE	Channel transfer enable: 0: disable; 1: enable. In normal situation, software desert TT set CTE hardware set TT desert CTE; For cancel working pdma, software desert CTE clear TT	RW

NOTES:

1. For a working channel, when an address error occurs or an on-going transfer is stopped by software writing 0 to CTE, HLT becomes 1 but TT keeps 0 that denotes an abnormal situation occurs.
2. Software can stop any working channel at any time. However, after setting 0 to CTE, software must read TT, HLT and CTE to ensure the stop behavior has been done for the channel, that is,
   a) TT=0, HALT=0, CTE =1, not halt yet, need polling again
   b) TT=1, HALT=0, CTE=0, the channel just ends its work when software wants to stop it.
   c) TT=0, HALT=1, CTE=0, the channel has been stopped but its transfer not complete yet.

18.5.6 DMA Channel Command (DCMn, n = 0 ~ 31)

	DCMn																															BASE + 0x14 + (n*0x20)
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				SID		DID		SAI	DAI	SAIW	DAIW	RDIL				SP		DP		Reserved	TSZ			SACIDX	DACIDX	Reserved			STDE	TIE	LINK
RST	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	0	?	?	?	?	?	0	0	0	0	0	0

Bits	Name	Description	RW
31:28	Reserved	Write has no effect, read as zero	R
27:26	SID	Don't set this bit, keep as 0.	RW
25:24	DID	Don't set this bit, keep as 0.	RW
23	SAI	Source Address Increment. 0: no increment; 1: increment.	RW
22	DAI	Destination Address Increment. 0: no increment; 1: increment.	RW
21	SAIW	Source Address Incr then Wrap: 0: no incr_then_wrap; 1: incr_then_wrap. Note:[SAI:SAIW] comprise of source address pattern,	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		00: no change 10: increment; 01: increment then wrap when external device assert last single to dmac, address return to SAIDX refer to global register	
20	DAIW	Destination Address Incr then Wrap: 0: no incr_then_wrap; 1: incr_then_wrap. It works only for TX, and return to start address after each bus transfer done. Eg. 4word start from 0x40,44,48,4C then return to 0x40	RW
19:16	RDIL	Recommended data unit size (unit: byte) for triggering device's DMA request when TSZ is autonomy.	RW
15:14	SP	Source port width. 00: 32-bit; 01: 8-bit; 10: 16-bit; 11: reserved.	RW
13:12	DP	Destination port width. 00: 32-bit; 01: 8-bit; 10: 16-bit; 11: reserved.	RW
11:8	TSZ	Transfer Data Size of a data unit. 000: 32-bit; 001: 8-bit; 010: 16-bit; 011: 16-byte; 100: 32-byte; 101: 64-byte; 110: 128-byte; 111: autonomy; 1000:extr-decide Note: canbus use 1000 type, actual trans size is 4/1 word according to rx-single is 0/1	RW
7	SACIDX	Source address compare index, refer to global SACIDX0/1 for detail	RW
6	DACIDX	Destination address compare index	RW
5:3	Reserved	Write has no effect, read as zero	R
2	STDE	Stride Disable/Enable. 0: address stride disable; 1: address stride enable.	RW
1	TIE	Transfer Interrupt Enable (TIE). 0: disable interrupt; 1: enable interrupt when TT is set to 1.	RW
0	LINK	Descriptor Link Enable. 0: disable; 1: enable. (the field is ignored in No-Descriptor Transfer mode)	RW

NOTES:

SP and DP are only available for device FIFO or NEMC. But when transfer data between device and DDR memory, must set the port width of DDR side as the same as the device side; however, when both source and destination are in DDR memory, both SP and DP must be 32-bit by setting 0.

Table 18-6 Available RDIL

RDIL	Description
0	Reserved
1	Recommended data unit is 1 bytes
2	Recommended data unit is 2 bytes
3	Recommended data unit is 3 bytes
4	Recommended data unit is 4 bytes
5	Recommended data unit is 8 bytes
6	Recommended data unit is 16 bytes

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

7	Recommended data unit is 32 bytes
8	Recommended data unit is 64 bytes
9	Recommended data unit is 128 bytes
10~15	Reserved

NOTES:

1. if TSZ is autonomy, total bytes to be transferred equal the value of DCTn.TC (so maximum transfer bytes for autonomy are 16MB -1).
2. Programmer must care the detail of the FIFO of the device binding with relative DMA channel to set the correct and best recommended data unit value according to FIFO's data width and depth, refer to following table.

FIFO form	Best recommended RDIL
8x8bits	4 (half of total entries just accommodate 4 bytes)
8x16bits	5 (half of total entries just accommodate 8 bytes)
32x8bits	6 (half of total entries just accommodate 16 bytes)
16x16bits	6 (half of total entries just accommodate 16 bytes)
64x8bits	7 (half of total entries just accommodate 32 bytes)
64x32bits	9 (half of total entries just accommodate 128 bytes)
128x16bits	9 (half of total entries just accommodate 128 bytes)
128x32bits	9 (because maximum data unit is 128 bytes)

Moreover, programmer must be carefully obey following rules for correctness and best performance concern of DMA transfer:

1. ***auto-request, both source and destination device are DDR memory***. No alignment constraint for address, however, both source port width and destination port width must be set 32bit, and transferred bytes in a bus transaction denoted by TSZ (when TSZ !=7) must not be less than 4. Setting autonomy (TSZ=7) is the best choice for transfer efficiency[*0]
2. ***auto-request, both source and destination device are NEMC*****,** then
   a) if both source and destination port width are 8bit, no alignment constraint for address, setting autonomy (TSZ=7) is the best choice for transfer efficiency.
   b) If either source port or destination port width is not 8bit, must not set autonomy to TSZ. The relative source or destination address must be 2-byte (port width is 16bit) or 4-byte (port width is 32bit) aligned. Moreover, the byte number denoted by TSZ must not be less than the least common multiple of the byte number denoted by source port width and destination port width. Larger TSZ means better transfer efficiency.
3. ***auto-request, source device is NEMC while destination device is DDR memory*****,** then
   a) if source port width is 8bit. no alignment constraint for address, setting autonomy (TSZ=7) is the best choice for transfer efficiency.
   b) if source port width is 16bit, source address must be 2-byte aligned and TSZ must be

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

the times of 2-byte (so must not set autonomy to TSZ); no alignment constraint for destination address, larger TSZ means better transfer efficiency.

c) If source port width is 32bit, source address must be 4-byte aligned and TSZ must be the times of 4-byte (so must not set autonomy to TSZ); no alignment constraint for destination address, larger TSZ means better transfer efficiency.

4. ***auto-request, source device is DDR memory while destination device is NEMC***, then
   a) if destination port width is 8bit, no alignment constraint for address, setting autonomy (TSZ=7) is the best choice for transfer efficiency
   b) if destination port width is 16bit, destination address must be 2-byte aligned and TSZ must be the times of 2-byte (so must not set autonomy to TSZ); no alignment constraint for source address, larger TSZ means better transfer efficiency.
   c) If destination port width is 32bit, destination address must be 4-byte aligned and TSZ must be the times of 4-byte (so must not set autonomy to TSZ); no alignment constraint for source address, larger TSZ means better transfer efficiency.
5. ***external device fifo receive request, destination device is DDR memory***, then no alignment constraint for destination address, and
   a) if non-autonomy (TSZ !=7), for transferred bytes in a bus transaction denoted by TSZ, it must not exceed the critical value of triggering DMA request[*1] meanwhile must be times of 2-byte when source port width is 16bit or times of 4-byte when source port width is 32bit.
   b) If autonomy (TSZ=7), for transferred bytes in a bus transaction denoted by RDIL, it must not exceed the critical value of triggering DMA request[*1] meanwhile must be times of 2-byte when source port width is 16bit or times of 4-byte when source port width is 32bit.

6. ***external device fifo receive request, destination device is NEMC***, then
   a) if destination port width is 8bit, no alignment constraint for destination address, and if non-autonomy (TSZ !=7), for transferred bytes in a bus transaction denoted by TSZ, it must not exceed the critical value of triggering DMA request[*1] meanwhile must be times of 2-byte when source port width is 16bit or times of 4-byte when source port width is 32bit.
      If autonomy (TSZ=7), for transferred bytes in a bus transaction denoted by RDIL, it must not exceed the critical value of triggering DMA request[*1] meanwhile must be times of 2-byte when source port width is 16bit or times of 4-byte when source port width is 32bit.
   b) If destination port width is 16bit, must not set autonomy to TSZ and destination address must be 2-byte aligned. For transferred bytes in a bus transaction denoted by TSZ, it must not exceed the critical value of triggering DMA request[*1] meanwhile must not be less than the least common multiple of the byte number denoted by source port width and destination port width.
   c) If destination port width is 32bit, must not set autonomy to TSZ and destination address must be 4-byte aligned. For transferred bytes in a bus transaction denoted by TSZ, it must not exceed the critical value of triggering DMA request[*1] meanwhile

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

must not be less than the least common multiple of the byte number denoted by source port width and destination port width.

7. ***external device fifo transmit request, source device is DDR memory***, then no alignment constraint for source address, and
   a) if destination port width is 8bit, setting autonomy (TSZ=7) is the best choice for transfer efficiency
   b) if destination port width is 16bit, when setting autonomy (TSZ=7), total transferred bytes must be the times of 2-byte, and for transferred bytes in a bus transaction denoted by RDIL, it must not exceed the critical value of triggering DMA request[*1] meanwhile must be the times of 2-byte; when setting non-autonomy (TSZ!=7), for transferred bytes in a bus transaction denoted by TSZ, it must not exceed the critical value of triggering DMA request[*1] meanwhile must be the times of 2-byte.
   c) if destination port width is 32bit, when setting autonomy (TSZ=7), total transferred bytes must be the times of 4-byte, and for transferred bytes in a bus transaction denoted by RDIL, it must not exceed the critical value of triggering DMA request[*1] meanwhile must be the times of 4-byte; when setting non-autonomy (TSZ!=7), for transferred bytes in a bus transaction denoted by TSZ, it must not exceed the critical value of triggering DMA request[*1] meanwhile must be the times of 4-byte.

8. ***external device fifo transmit request, source device is NEMC***, then
   a) if source port width is 8bit, no alignment constraint for source address, and if non-autonomy (TSZ !=7), for transferred bytes in a bus transaction denoted by TSZ, it must not exceed the critical value of triggering DMA request[*1] meanwhile must be times of 2-byte when destination port width is 16bit or times of 4-byte when destination port width is 32bit.
      If autonomy (TSZ=7), for transferred bytes in a bus transaction denoted by RDIL, it must not exceed the critical value of triggering DMA request[*1] meanwhile must be times of 2-byte when destination port width is 16bit or times of 4-byte when destination port width is 32bit.
   b) If source port width is 16bit, must not set autonomy to TSZ and source address must be 2-byte aligned. For transferred bytes in a bus transaction denoted by TSZ, it must not exceed the critical value of triggering DMA request[*1] meanwhile must not be less than the least common multiple of the byte number denoted by source port width and destination port width.
   c) If source port width is 32bit, must not set autonomy to TSZ and source address must be 4-byte aligned. For transferred bytes in a bus transaction denoted by TSZ, it must not exceed the critical value of triggering DMA request[*1] meanwhile must not be less than the least common multiple of the byte number denoted by source port width and destination port width.

NOTES:

*0 - when TSZ is not autonomy, total bytes to be transferred are bytes represented by TSZ * TC, and each bus transaction can only transfer bytes represented by TSZ, so larger

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

data unit is better for transfer efficiency. But since in practical, in most cases, total bytes to be transferred are not the times of the best data unit, or source and/or destination address violates alignment, thus **setting autonomy for TSZ is recommended** when condition is ok.

*1 - Please refer to relative device's spec for detail information of how to set critical trigger value.

18.5.7 DMA Descriptor Address (DDAn, n = 0 ~ 31)

This register is ignored in No-Descriptor Transfer mode.

	DDAn																															
																	BASE + 0x18 + (n*0x20)															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DBA																				DOA								Reserved			
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0

Bits	Name	Description	RW
31:12	DBA	Descriptor Base Address.	RW
11:4	DOA	Descriptor Offset Address.	RW
3:0	Reserved	Write has no effect, read as zero.	R

18.5.8 DMA Stride Difference (DSDn, n = 0 ~ 31)

This register is ignored in No-Descriptor Transfer mode.

When address stride transfer mode is enabled in Descriptor mode, after a sub-block's transfer defined in DTCn completes, the source or target stride difference will be added to perform the new sub-block's start address, and the transfer will keep going until the transfer ends which means TC in DTCn reaches 0.

	DSDn																															
																	BASE + 0x1C + (n*0x20)															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TSD																SSD															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:16	TSD	Target Stride Difference (next sub-block's start address – current sub-block's end address - 1), value range is -32768 ~ 32767	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

15:0	SSD	Source Stride Difference (next sub-block's start address – current sub-block's end address - 1), value range is -32768 ~ 32767	RW

18.6 DMA Global Register Definition

18.6.1 DMA Control

	DMAC																															BASE+0x1000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FMSC	FSSI	FTSSI	FUART	FAIC	Reserved											Reserved												HLT	AR	CH01	DMAE
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	FMSC	0: 0.5-data/clk for MSC on APB;1: 1-data/clk for MSC on APB.	RW
30	FSSI	0: 0.5-data/clk for SSI on APB;1: 1-data/clk for SSI on APB.	RW
29	FTSSI	0: 0.5-data/clk for TSSI on APB;1: 1-data/clk for TSSI on APB.	RW
28	FUART	0: 0.5-data/clk for UART on APB;1: 1-data/clk for UART on APB.	RW
27	FAIC	0: 0.5-data/clk for AIC on APB;1: 1-data/clk for AIC on APB.	RW
21:17	Reserve	Write has no effect, read as zero.	R
16	Reserve	Write has no effect, read as zero.	R
15:4	Reserve	Write has no effect, read as zero.	R
3	HLT	Global halt status, halt occurs in any channel, the bit should be set to 1 by hardware and cleared to 0 by software. 0: no halt occurred 1: halt occurred in one or more channels	RW
2	AR	Global address error status, address error occurs in any channel, the bit should be set to 1 by hardware and cleared to 0 by software. 0: no address error occurred 1: address error occurred	RW
1	CH01	Don't set this bit, keep as 0.	RW
0	DMAE	Global DMA enable. 0: disable DMA 1: enable DMA	RW

NOTES:

1. any of FMSC/FSSI/FTSSI/FUART/FAIC has been set, the corresponding DMA transfer on APB for MSC(MSC1, MSC2), SSI(SSI1), UART0~4, AIC will be in fast mode.
2. DMAE is a global switch, so software must be careful to toggle it from 0 to 1 or 1 to 0. It is

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

UNPREDICTABLE to set 0 to DMAE abruptly when some channels are still working.

3. For more detail of CH01, refer to later chapter of special channel 0 and channel 1

18.6.2 DMA Interrupt Pending (DIRQP)

	DIRQP																															BASE+0x1004
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IRQ31	IRQ30	IRQ29	IRQ28	IRQ27	IRQ26	IRQ25	IRQ24	IRQ23	IRQ22	IRQ21	IRQ20	IRQ19	IRQ18	IRQ17	IRQ16	IRQ15	IRQ14	IRQ13	IRQ12	IRQ11	IRQ10	IRQ9	IRQ8	IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	IRQ0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	IRQn	IRQn denotes pending IRQ to main CPU for corresponding channel. 0: normal DMA transfer is in-progress or the channel is idle 1: an address error occurs (only available for UARTn) or normal DMA transfer done; moreover, if the relative channel is programmable, MCU can only set 1 to it. Hardware can only set 1 to it and main CPU can only set 0 to it.	RW

18.6.3 DMA Doorbell (DDB)

	DDB																															BASE+0x 1008
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DDB31	DDB30	DDB29	DDB28	DDB27	DDB26	DDB25	DDB24	DDB23	DDB22	DDB21	DDB20	DDB19	DDB18	DDB17	DDB16	DDB15	DDB14	DDB13	DDB12	DDB11	DDB10	DDB9	DDB8	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DDBn	DMA Doorbell. Software sets it to 1 and hardware clears it to 0. 0: disable DMA controller to fetch the first descriptor or DMA controller clears it to 0 as soon as it starts to fetch the descriptor 1: Writing 1 to DDS will set the corresponding DDBn bit to 1 and enable DMA controller to fetch the first descriptor For example, write 0x00000001 to DDS, DDB0 bit is set to 1 and enable DMA channel 0 to fetch its first descriptor. Write 0 to DDS, no meaning.	RWS

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

18.6.4 DMA Doorbell Set (DDS)

	DDS																															BASE+0x 100C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DDS31	DDS30	DDS29	DDS28	DDS27	DDS26	DDS25	DDS24	DDS23	DDS22	DDS21	DDS20	DDS19	DDS18	DDS17	DDS16	DDS15	DDS14	DDS13	DDS12	DDS11	DDS10	DDS9	DDS8	DDS7	DDS6	DDS5	DDS4	DDS3	DDS2	DDS1	DDS0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DDSn	DMA Doorbell Set for each channel. Read as zero, and when write: 0: ignore 1: Set the corresponding DDBn bit to 1	W

18.6.5 Descriptor Interrupt Pending (DIP)

	DIP																															BASE+0x 1010
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DIP31	DIP30	DIP29	DIP28	DIP27	DIP26	DIP25	DIP24	DIP23	DIP22	DIP21	DIP20	DIP19	DIP18	DIP17	DIP16	DIP15	DIP14	DIP13	DIP12	DIP11	DIP10	DIP9	DIP8	DIP7	DIP6	DIP5	DIP4	DIP3	DIP2	DIP1	DIP0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DIPn	Descriptor interrupt pending. If any of the descriptor, except the last one, set TIE, the corresponding bit of this register shall set after the very descriptor finished. This function provide more flexible method to be aware of the process of the long descriptor links. 0: No descriptor interrupt pending 1: The corresponding bit channel has completed a descriptor with TIE Read only for software..	R

18.6.6 Descriptor Interrupt Clear (DIC)

	DIC																															BASE+0x 1014
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DIC31	DIC30	DIC29	DIC28	DIC27	DIC26	DIC25	DIC24	DIC23	DIC22	DIC21	DIC20	DIC19	DIC18	DIC17	DIC16	DIC15	DIC14	DIC13	DIC12	DIC11	DIC10	DIC9	DIC8	DIC7	DIC6	DIC5	DIC4	DIC3	DIC2	DIC1	DIC0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:0	DICn	Descriptor interrupt pending clear. 1: ignore 0: Clear the corresponding DIPn bit Only write 1 for software, read has no effect.	W1

18.6.7 DMA Channel Programmable (DMACP)

	DMACP																															BASE+0x 101C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DCP31	DCP30	DCP29	DCP28	DCP27	DCP26	DCP25	DCP24	DCP23	DCP22	DCP21	DCP20	DCP19	DCP18	DCP17	DCP16	DCP15	DCP14	DCP13	DCP12	DCP11	DCP10	DCP9	DCP8	DCP7	DCP6	DCP5	DCP4	DCP3	DCP2	DCP1	DCP0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DCPn	Channel programmable enable. 0, compatible with previous JZ SOC; 1, firmware controlled channel	RW

18.6.8 DMA Soft IRQ Pending (DSIRQP)

	DSIRQP																															BASE+0x 1020
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SIRQ31	SIRQ30	SIRQ29	SIRQ28	SIRQ27	SIRQ26	SIRQ25	SIRQ24	SIRQ23	SIRQ22	SIRQ21	SIRQ20	SIRQ19	SIRQ18	SIRQ17	SIRQ16	SIRQ15	SIRQ14	SIRQ13	SIRQ12	SIRQ11	SIRQ10	SIRQ9	SIRQ8	SIRQ7	SIRQ6	SIRQ5	SIRQ4	SIRQ3	SIRQ2	SIRQ1	SIRQ0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	SIRQn	Soft IRQ to MCU. Set any bit of this register to 1, if not masked correspond with that in DSIRQM, will issue a software interrupt to MCU. Note that the register is read-only for other masters but is entirely controlled (R/W) by the MCU of PDMA	R

18.6.9 DMA Soft IRQ Mask (DSIRQM)

	DSIRQM																															BASE+0x 1024
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	SIRQM31	SIRQM30	SIRQM29	SIRQM28	SIRQM27	SIRQM26	SIRQM25	SIRQM24	SIRQM23	SIRQM22	SIRQM21	SIRQM20	SIRQM19	SIRQM18	SIRQM17	SIRQM16	SIRQM15	SIRQM14	SIRQM13	SIRQM12	SIRQM11	SIRQM10	SIRQM9	SIRQM8	SIRQM7	SIRQM6	SIRQM5	SIRQM4	SIRQM3	SIRQM2	SIRQM1	SIRQM0
RST	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Name	Description	RW
31:0	SIRQMn	Soft IRQ mask. 0, not mask corresponding DSIRQP soft IRQ; 1, mask corresponding DSIRQP soft IRQ Note that the register is read-only for other masters but is entirely controlled (R/W) by the MCU of PDMA	R

18.6.10 DMA Channel IRQ Pending to MCU (DCIRQP)

	DCIRQP																															**BASE+0x 1028**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CIRQ31	CIRQ30	CIRQ29	CIRQ28	CIRQ27	CIRQ26	CIRQ25	CIRQ24	CIRQ23	CIRQ22	CIRQ21	CIRQ20	CIRQ19	CIRQ18	CIRQ17	CIRQ16	CIRQ15	CIRQ14	CIRQ13	CIRQ12	CIRQ11	CIRQ10	CIRQ9	CIRQ8	CIRQ7	CIRQ6	CIRQ5	CIRQ4	CIRQ3	CIRQ2	CIRQ1	CIRQ0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	CIRQn	Channel IRQ Pending to MCU. The register is read-only 0, no channel IRQ to MCU; 1, pending channel IRQ to MCU When channel n is not programmable, the CIRQn is ignored by hardware. When channel n is programmable and DCMn.TIE is active 1, DIRQP.IRQn can not be set automatically any more after address error occurs or TT becomes active 1, instead, if DCIRQMn==0, CIRQn may be set 1 immediately to raise an IRQ to MCU. Moreover, when an channel m with above attribute is bound with the INTC_IRQ, if DCIRQMm==0, an active INTC_IRQ request will trigger an active CIRQn immediately	R

18.6.11 DMA Channel IRQ to MCU Mask (DCIRQM)

	DCIRQM																															**BASE+0x 102C**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CIRQM31	CIRQM30	CIRQM29	CIRQM28	CIRQM27	CIRQM26	CIRQM25	CIRQM24	CIRQM23	CIRQM22	CIRQM21	CIRQM20	CIRQM19	CIRQM18	CIRQM17	CIRQM16	CIRQM15	CIRQM14	CIRQM13	CIRQM12	CIRQM11	CIRQM10	CIRQM9	CIRQM8	CIRQM7	CIRQM6	CIRQM5	CIRQM4	CIRQM3	CIRQM2	CIRQM1	CIRQM0
RST	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:0	CIRQMn	Mask of Channel IRQ to MCU. The register is read-only for other master but is entirely controlled (R/W) by the MCU of PDMA 0, not mask corresponding channel's IRQ to MCU; 1, mask corresponding channel's IRQ to MCU When channel n is not programmable, the CIRQMn is ignored by hardware. When channel n is programmable and DCMn.TIE is active 1, CIRQMn can mask corresponding channel's IRQ to MCU.	R

18.6.12 DMA Channel Source Address Compare INDEX 0 (SACIDX0)

	DSDn																															BASE + 0x1060
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																START															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

31:16	Reserved	Write has no effect.	RW
15:0	START	wrap start address	RW

18.6.13 DMA Channel Source Address Compare INDEX 1 (SACIDX1)

	DSDn																															BASE + 0x1064
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																START															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

31:16	Reserved	Write has no effect.	RW
15:0	START	wrap start address	RW

18.6.14 DMA Channel Destination Address Compare INDEX 0(DACIDX0)

	DSCIDX0																															BASE + 0x1068
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																START															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

31:16	Reserved	Write has no effect.	RW
15:0	start	wrap start address	RW

18.6.15 DMA Channel Destination Address Compare INDEX 1(DACIDX1)

	DSCIDX0																BASE + 0x106c															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																START															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

31:16	Reserved	Write has no effect.	RW
15:0	start	wrap start address	RW

18.7 MCU

MCU in PDMA is a mini CPU compatible with XBurst-1 ISA without implementing CACHE, MMU, DEBUG, FPU and MXU. It is very similar as the AUX in VPU but has different memory mapped control and status register.

18.7.1 MCU Control & Status

	DMCS																BASE+0x 1030															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SLEEP	SCMD	Reserved						SC _OFF																				SC_CALL			SW_RST
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	1

Bits	Name	Description	RW
31	SLEEP	Sleep status of MCU. Read only by main CPU.	R
30	SCMD	Security Mode. Read only by main CPU.	R
29:24	reserved	Write has no effect, read as zero.	R
23:8	SC_OFF	Set the offset of the caller's data structure for SC_CALL	RW
7	reserved	Write has no effect, read as zero.	R
6	reserved	Write has no effect, read as zero.	R
5	reserved	Write has no effect, read as zero.	R
4	BTB_INV	Writing 1 invalidates BTB in MCU. Writing 0 has no effect, read as zero.	W
3	SC_CALL	Security Call. Writing 1 triggers a security exception which directs MCU to run security code located in the on-chip security ROM., read as zero.	W
2:1	reserved	Write has no effect, read as zero.	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

0	SW_RST	Software reset. 1, MCU keeps at reset state; 0, do not soft-reset MCU any more	RW

NOTES:

BCH_DB, BCH_DF and BCH_EF are only available when special channel 0 and channel 1 is used for implementing storage of raw NAND chipsets. Please refer to BCH spec for detail.

18.7.2 MCU Normal MailBox

	DMNMB																															BASE+0x 1034
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MB																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	MB	Contents of Normal Mailbox. Writing any value to the register will trigger a normal mailbox IRQ to main CPU when relative MASK field in DMINT is not set	RW

18.7.3 MCU Security MailBox

	DMSMB																															BASE+0x 1038
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MB																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	MB	Contents of Security Mailbox. Writing any value to the register will trigger a security mailbox IRQ to main CPU when relative MASK field in DMINT is not set. Note that writing the register is inhibited by HW when DMCS.SCMD == 0	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

18.7.4 MCU Interrupt

	DMINT																															BASE+0x 103C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved														S_IP	N_IP	Reserved														S_IMSK	N_IMSK
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Name	Description	RW
31:18	Reserved	Write has no effect, read as zero.	R
17	S_IP	Security Mailbox IRQ pending. 1-pending IRQ. Hardware only set 1 by writing DMSMB when DMCS.SCMD == 1. Can be clear to 0 in any mode.	RW
16	N_IP	Normal Mailbox IRQ pending. 1-pending IRQ. Hardware only set 1 by writing DMNMB. Can be clear to 0 in any mode.	RW
15:2	Reserved	Write has no effect, read as zero.	R
1	S_IMSK	Security Mailbox IRQ mask. 1-mask; 0-not mask Can only be modified in security mode.	RW
0	N_IMSK	Normal Mailbox IRQ mask. 1-mask; 0-not mask	RW

18.7.5 Multiple Bank Tightly Coupled Sharing Memory

In MCU, there is a Tightly Coupled Sharing Memory (TCSM) with 32KB size and total 8 banks. Multiple- bank TCSM permits several masters accessing different banks in parallel. TCSM works at the same speed as MCU and both instruction fetch and data read/write to TCSM by MCU can be performed in one cycle.

Table 18-7 TCSM space

	VA (only available for MCU)	PA (not remapped)	PA (remapped)
BANK0	F4000000h ~ F4000FFFh	13422000h ~ 13422FFFh	F3422000h ~ F3422FFFh
BANK1	F4001000h ~ F4001FFFh	13423000h ~ 13423FFFh	F3423000h ~ F3423FFFh
BANK2	F4002000h ~ F4002FFFh	13424000h ~ 13424FFFh	F3424000h ~ F3424FFFh
BANK3	F4003000h ~ F4003FFFh	13425000h ~ 13425FFFh	F3425000h ~ F3425FFFh
BANK4	F4004000h ~ F4004FFFh	13426000h ~ 13426FFFh	F3426000h ~ F3426FFFh
BANK5	F4005000h ~ F4005FFFh	13427000h ~ 13427FFFh	F3427000h ~ F3427FFFh
BANK6	F4006000h ~ F4006FFFh	13428000h ~ 13428FFFh	F3428000h ~ F3428FFFh
BANK7	F4007000h ~ F4007FFFh	13429000h ~ 13429FFFh	F3429000h ~ F3429FFFh

18.7.6 CP0 Registers of MCU

Available CP0 registers of MCU are not entirely compatible with MIPS PRA spec, they are

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

listed below.

CP0 Name (number)	Description	*slt*
STATUS (12)	Bit 31~27:: reserved, read as zero Bit26: readable; only 1 can bet written into*1 Bit25: readable; only 1 can bet written into*1 Bit24: only being active during running Security Call routine *2 Bit2: ERL, Bit1: EXL, Bit0: IE	*0*
INTCTL (12)	Bit31~3: reserved, read as zero; Bit2: IRQ pending of soft IRQ to MCU; Bit1: IRQ pending of channel IRQ to MCU; Bit0: IRQ pending of INTC_IRQ Note that the register is read-only by MCU	*1*
CAUSE (13)	Bit31:BD， whether the interrupted PC is located in branch delay slot Bit30 ~ 0: reserved, read as zero	*0*
SeCAUSE (13)	Bit31:BD, similar as CAUSE, but being active when an IRQ interrupted a running Security Call routine. Bit30 ~ 0: reserved, read as zero	*1*
EPC (14)	IRQ Exception program counter	*0*
SePC (24)	Security Exception program counter	*0*
ErrorPC (30)	*Reset exception program counter*	*0*

NOTE:

*1 : once value 1 is set, only chip reset signal can clear it to 0.

*2 : STATUS.Bit24 is hard wired outside of PDMA.

18.7.7 Normal Exceptions Accepted by MCU

There are two kinds of normal exceptions that can be accepted by MCU: RESET and IRQ. Note that RESET exception has the handler entry: 0xF4000000, while IRQ has another one: 0xF4000100.

Once the MCU accepts a normal exception, according to the definition of XBurst-1 Programming Manual, current interrupted PC will be pushed into CP0.EPC or CP0.ErrPC, and further CP0.STATUS.ERL or CP0.SATUS.EXL will be automatically set 1. Firmware can take use of MTC0/MFC0 to access these three CP0 registers: EPC, ErrPC and STATUS. Firmware must use ERET instruction to return to the interrupted locale to resume executing.

18.7.8 How to Boot MCU Up

After power-on reset, MCU keeps at reset state due to DMCS.SW_RST==1. To boot MCU up, first of all, RESET exception handler must be loaded into TCSM at the physical address range beginning from 0x13422000 or 0xF3422000 for remapped case. Programmer can use main

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

CPU or some Non-programmable DMA channel to finish this loading work. Then clear DMCS.SW_RST to 0 by main CPU so that MCU can acknowledge a RESET exception, now MCU begins to run from the PC 0xF4000000. Following is a simple example.

1. Prepare a simple RESET exception handler, total 3 instructions:

```
1:  WAIT   //sleep
B   1b     //endless loop
NOP        //delay slot
```

2. Load the handler into TCSM at the physical address range beginning from 0x13422000 or 0xF3422000 for remapped case.
3. Clear DMCS.SW_RST to 0 by main CPU

Now MCU will execute WAIT instruction and then enter sleep state

18.8 DMA manipulation

18.8.1 Descriptor Transfer Mode

18.8.1.1 Non-Stride (1-Dimensional) Transfer Mode

To do proper Descriptor DMA transfer in a channel, do following steps:

1 Check whether the status of DMA controller is available, that is, for global control (DMAC), ensure that DMAC.AR=0 and DMAC.HLT=0; and then for expected channel n, ensure that DCSn.AR=0, DCSn.HLT=0, DCSn.TT=0, DTCn=0.

2 guarantee DCSn.NDES=0, and select 4 word or 8 word descriptor by DCSn.DES8.

3 Build descriptor in memory. Write the first descriptor's address in DDAn and the address must be 16Bytes aligned for 4word descriptor and 32Bytes aligned for 8word descriptor, otherwise, the hardware behavior later is **UNPREDICTABLE**. The address includes two parts: Base and Offset address. If the descriptor is linked, the 32-bit address of next descriptor is composed of 20-bit Base address in DDAn and 8-bit Offset address in DESn.CDOA. See Table 18-8 Descriptor Structure for the detailed descriptor structure.

4 Don't update DRTn manually by software, instead, hardware will manage the request type of descriptor's transfer automatically.

5 Set 1 to the corresponding bit in DDB to initiate descriptor fetch.

6 Set DMAC.DMAE=1 and expected DCSn.CTE=1 to activate channel n.

7 Hardware will automatically clear the corresponding bit in DDB as soon as it starts to fetch the descriptor.

8 Wait for DMA request from peripherals to start channel n's DMA transfer.

9 After DMA transfers described by the current descriptor complete, if current DCMn.LINK =0, then DCSn.TT will be set to 1 immediately. Further, if DCMn.TIE=1, it will issue an interrupt request. However, if DCMn.LINK=1, next descriptor will be automatically fetched to repeat step 8 and 9 but ignore setting DCSn.TT until a final descriptor with settting of DCMn.LINK=0 has been done.

10 When channel n's transfer ends normally (DCSn.TT=1) or abnormally (DCSn.HLT=1),

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

to correctly reuse the channel later, software must close the channel first by setting 0 to DCSn.CTE, and then safely clear DCSn.TT or DCSn.HLT to 0.

Table 18-8 Descriptor Structure

Word	Bit	Name	Function
1st (DES0)	31	EACKS	External DMA DACKn output polarity select
	30	EACKM	External DMA DACKn output Mode select
	29-28	ERDM	External DMA request detection Mode
	27-24	Reserved	--
	23	SAI	Source Address Increment
	22	DAI	Target Address Increment
	21-20	Reserved	--
	19-16	RDIL	Request Detection Interval Length
	15-14	SP	Source port width
	13-12	DP	Target port width
	11	Reserved	--
	10-8	TSZ	Transfer Data Size
	7-3	Reserved	--
	2	STDE	Stride transfer enable
	1	TIE	Transfer Interrupt Enable
	0	LINK	Descriptor Link Enable
2nd (DES1)	31-0	DSA	Source Address
3rd (DES2)	31-0	DTA	Target Address
4th (DES3)	31-24	DOA	Descriptor Offset address
	23-0	DTC	Transfer Counter
5th (DES4)	31-16	TSD	Target Stride Address
	15-0	SSD	Source Stride Address
6th(DES5)	31-6	Reserved	--
	5-0	DRT	DMA Request Type
7th(DES6)	31-0	Reserved	--
8th(DES7)	31-0	Reserved	--

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Figure 18-2 Descriptor Transfer Flow

18.8.1.2 Stride (2-dimensional) Transfer Mode

Stride transfer mode means total transfer counts are subdivided into dozens of or even hundreds of sub-blocks with same size, and each adjacent two sub-blocks has fixed nonzero address gap between the tail of preceding one and the head of subsequent one.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Figure 18-3 Example for Stride Transfer Mode

Manipulation steps of Stride Transfer Mode are similar to Non-stride Transfer Mode. However, each new sub-block's start address (source or destination) is performed by adding the next adjacent byte address of very completed sub-block's end address to corresponding stride difference.

18.8.2 No-Descriptor Transfer Mode

To do proper No-Descriptor DMA transfer, do following steps:

1. Check whether the status of DMA controller is available, that is, for global control (DMAC), ensure that DMAC.AR=0 and DMAC.HLT=0; and then for expected channel n, ensure that DCSn.AR=0, DCSn.HLT=0, DCSn.TT=0, DTCn=0.
2. Forx channel n, initialize DSAn, DTAn, DTCn, DRTn, DCSn, DCMn properly.
3. Set DMAC.DMAE=1 and DCSn.CTE=1 to launch DMA transfer.

For a channel with auto-request (DRTn.RT=0x8), the transfer begins automatically when the DCSn.CTE bit and DMAC.DMAE bit are set to 1. While for a channel with other request types, the transfer does not start until a transfer request is issued and detected.

For any channel n, The DTCn value is decremented by 1 for each successful transaction of a data unit. When the specified number of transfer data unit has been completed (DTCn = 0), the transfer ends normally. Meanwhile if DCMn.TIE=1, corresponding bit of DIRQP will be set to 1 to raise an interrupt request. However, during the transfer, if a DMA address error occurs, the transfer should be suspended, both DCSn.AR and DMAC.AR are set to 1 as well as corresponding bit of DIRQP to raise an interrupt request despite of DCMn.TIE.

Sometimes, for example, an UART parity error occurs for a channel that is transferring data between such UART and another terminal. In the case, both DCSn.HLT and DMAC.HLT are set to 1 and the transfer is suspended. Software should identify halt status by checking such two bits and re-configure DMA to let DMA rerun properly later.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

18.8.3 Descriptor Transfer Interrupt/Stop control

DMA descriptor provides a more fast and easy way to transfer data. Usually in a long descriptor linked-line, it's hard to specifically know where the current descriptor point is. Here are the recommended ways to help software to control this.

Register	Part	Name	Function
DCSn	15:8	CDOA	Copy of offset address of last completed descriptor from that in DMA command register.
	0:0	CTE	Channel transfer enable: 0: disable; 1: enable. **Note: If set during a long descriptor linked-line, DMA will finish the current data unit transfer and terminate the whole transfer. If it is not necessary, don't use this method to end the transfer.**
DCMn	1:1	TIE	Transfer Interrupt Enable (TIE). 0: disable interrupt; 1: enable interrupt when TT is set to 1. **Note: If set during a long descriptor linked-line, DMA will raise a interrupt to INTC, if not masked, and this can be acknowledged by visit DSP register. Also if TIE has already been set in the descriptor, DMA will also raise interrupt except that is the last descriptor, and if it happens, DIRQP will raise instead of DIP.**
	0:0	LINK	Descriptor Link Enable. 0: disable; 1: enable. **Note: If set during a long descriptor linked-line, DMA will finish the current descriptor, and then regard it as a no-linked descriptor and stop transfer. However, it has a change that write this bit to 0 is ignored by hardware, so a double write or a read-check is recommended.**
DIP	7:0	DIP	Descriptor interrupt pending. If any of the descriptor, except the last one, set TIE, the corresponding bit of this register shall set after the very descriptor finished. This function provide more flexible method to be aware of the process of the long descriptor links. 0: No descriptor interrupt pending 1: The corresponding bit channel has completed a descriptor with TIE Read only for software. **Note: DIP will raise if the two conditions satisfy, one is this is not the last descriptor, the other is the current TIE in DCMn or TIE in current descriptor is set.**

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

18.9 DMA Requests

DMA transfer requests are normally generated from either the data transfer source or target, but also they can be issued by on-chip peripherals that are neither the source nor the target. There are two DMA transfer request types: auto-request, and on-chip peripheral request. For any channel n, its transfer request type is determined through DRTn.

18.9.1 Auto Request

When there is no explicit transfer request signal available, for example, memory-to-memory transfer or memory to some on-chip peripherals like GPIO, the auto-request mode allows the DMA to automatically generate a transfer request signal internally. Therefore, when DMA initialization done, once the DMAC.DMAE and DCSn.CTE are set to 1, the transfer begins immediately in channel n which DRTn=0x8.

18.9.2 On-Chip Peripheral Request

In the mode, transfer request signals come from on-chip peripherals or even off-chip devices. When a device issues a peripheral request to its corresponding channel n, the transferred byte number for the request is equals to:

1. byte number determined by the bytes denoted by DCMn.TSZ when DCMn.TSZ != 7
2. byte number determined by the bytes denoted by RDIL when DCMn.TSZ == 7

Be careful that the above number must not exceed the device's expected one otherwise FIFO under-run or over-run may occur. However, if the number is too small than the expected one, DMA's bus efficiency will become worse.

18.10 How to Use Programmable DMA Channel

When system needs to setup one programmable channel for later use of smart data transfer, do following steps:

1. Load elaborate firmware to TCSM, should use physical address 0x13422xxx. Common code fragment of IRQ exception handler must be located at physical address range beginning from 0x13422100.
2. Prepare a DMA channel n using expected transfer mode as description in preceding chapters
3. Must set DCMn.TIE=1 and DMACP.DCPn=1
4. Must ensure DCIRQM.CIRQMn==0
5. Launch the channel n as description in preceding chapters

Now the channel n becomes a working programmable channel. It is the responsibility of local channel IRQ's handler to remove corresponding channel IRQ source by setting 0 to DCSn.TT.

Moreover, if programmer wants to let the channel can be triggered by local soft IRQ, DSIRQM.SIRQMn must be set 0, then at expected moment, the MCU sets 1 to DSIRQP.SIRQn to trigger a soft IRQ. It is the responsibility of this soft IRQ's handler to remove the IRQ by setting 0 to DSIRQP.SIRQn.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

19 SAR A/D Controller

19.1 Overview

The SAR A/D controller is dedicated to control A/D to work at two different modes: normal operation mode and repeat sampling. The sampling data can transfer to memory though CPU.

19.2 Features

- 4 Channels
- Resolution: 12-bit
- Integral nonlinearity: ±2 LSB
- Differential nonlinearity: ±1 LSB
- Resolution/speed: up to 1.6Msps
- Max Clock Frequency: 24MHZ
- Support four auxiliary input (Through pin AUX0 to AUX3)

19.3 Block Diagram

Figure 19-1 Block Diagram of SADC

19.4 Pins Description

SADC has 4 analog input pin. They are listed and described in.

Table 19-1 SADC Analog Pin

Name	I/O	Description
AUX0	AI	Auxiliary Input

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

AUX1	AI	Auxiliary Input
AUX2	AI	Auxiliary Input
AUX3	AI	Auxiliary Input

19.5 Register Description

Following chapter will descript the functions of all software accessible registers.

Conventions:

5. Register Address = Base + Address offset
6. The registers can be read and written by APB bus
7. Register read/write attribute
   R - Read only
   W - Write only
   RW - read and write
   RCW - read and write, but clear to 0 by read
   RSW - read and write, but set to 1 by read
   RWC - read and write, clear to 0 by write 1, write 0 has no effect
   RWS - read and write, set to 1 by write 1, write 0 has no effect
   RC - read only, and clear to 0 by read
   RS - read only, and set to 1 by read
   SPEC - special access method, relate to its description
8. Reset Value
   1 - reset to 1
   0 - reset to 0
   ? - value unknown after reset

19.5.1 Register Memory Map

Table 19-2 Registers Memory Map Base Address

Name	Base	Description
SADC	0x10070000	Address base of SADC

The SAR A/D Controller is controlled by a set of registers that the application configures before every operation. The following table lists all the registers.

Table 19-3 SADC Registers Map

Name	RW	Reset Value	Address Offset	Access Size
ADENA	RW	0x8000	0x0000	16
ADCFG	RW	0x0000_0001	0x0004	32
ADCTRL	RW	0xFF	0x0008	8

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

ADSTATE	RW	0x00	0x000C	8
ADATA0	RW	0x0000_0000	0x0010	32
ADATA1	RW	0x0000_0000	0x0014	32
ADCLK	RW	0x0004_1000	0x0020	32
ADSTB	RW	0x0003_0000	0x0024	32
ADRETM	RW	0x0000_0000	0x0028	32

19.5.2 Register and Fields Description

19.5.2.1 ADC Enable Register (ADENA,0x0000)

The register ADENA is used to trigger A/D to work.

	ADENA																															BASE + 0x0000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																POWRR	Pow_opt_	Reserved				REPTEN	Reserved					AUX3EN	AUX2EN	AUX1EN	AUX0EN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15	POWER	SADC Power control bit. 1: SADC power down 0: SADC power on When POWER is set from 1 to 0, you should wait at least 2ms to enable SADC.	RW
14	POW_OPT	Power optimize enable 1: enable 0: disable	RW
13:10	Reserved	Writing has no effect, read as zero.	RW
9	REPTEN	Repeat sampling enable	RW
8:4	Reserved	Writing has no effect, read as zero.	RW
3	AUX3EN	AUX3 Enable Control.	RW
2	AUX2EN	AUX2 Enable Control.	RW
1	AUX1EN	AUX1 Enable Control.	RW
0	AUX0EN	AUX0 Enable Control.	RW

Note:

When two or more channel enable, the controller will sampling all the enabled channel from low to high.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

19.5.2.2 ADC Configure Register (ADCFG,0x0004)

The register ADCFG is used to Sadc's PHY testmode and rst_n to work.

	ADCFG																															BASE + 0x0004
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ADC_TRIM																Reserved															ADC_RST
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Name	Description	RW
31:16	ADC_TRIM	Connection to SAR_ADC's PHY for control SAR_ADC's PHY saradc_ana_reg, only used in adc testmode. please keep the value to 16'h0.	R
15:1	Reserved	Writing has no effect, read as zero.	RW
0	ADC_RST	Connection to ADC's PHY for control SAR_ADC's PHY saradc_rst_n 0: soft reset valid 1: soft reset unvalid	RW

19.5.2.3 ADC Control Register (ADCTRL,0x0008)

The register ADCTRL is used to control A/D to work.

	ADCTRL																															BASE + 0x0008
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												ARDYM3	ARDYM2	ARDYM1	ARDYM0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1

Bits	Name	Description	RW
31:4	Reserved	Writing has no effect. Read as zero.	RW
3	ARDYM3	AUX3 data ready interrupt mask. 0: enabled 1: masked	RW
2	ARDYM2	AUX2 data ready interrupt mask. 0: enabled	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		1: masked	
1	ARDYM1	AUX1 data ready interrupt mask. 0: enabled 1: masked	RW
0	ARDYM0	AUX0 data ready interrupt mask. 0: enabled 1: masked	RW

19.5.2.4 ADC Status Register (ADSTATE,0x000C)

The register ADSTATE is used to keep the status of A/D.

	ADSTATE																															BASE + 0x000C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												ARDY3	ARDY2	ARDY1	ARDY0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:4	Reserved	Writing has no effect. Read as zero.	R
3	ARDY3	AUX3 data ready interrupt flag. Write 1 to this bit, the bit will clear to 0. 1: active 0: not active	RWC
2	ARDY2	AUX2 data ready interrupt flag. Write 1 to this bit, the bit will clear to 0. 1: active 0: not active	RWC
1	ARDY1	AUX1 data ready interrupt flag. Write 1 to this bit, the bit will clear to 0. 1: active 0: not active	RWC
0	ARDY0	AUX0 data ready interrupt flag. Write 1 to this bit, the bit will clear to 0. 1: active 0: not active	RWC

19.5.2.5 ADC AUX Data Register (ADATA0,0x0010)

The read-only ADATA0 is a 32-bit register, it keep the sample data.

	ADATA0																															BASE + 0x0010
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Reserved				ADATA1												Reserved				ADATA0											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:28	Reserved	Writing has no effect. Read as zero.	R
27:16	ADATAH	Data of AUX1. When write to the register, DATA will be clear to 0.	RW
15:12	Reserved	Writing has no effect. Read as zero.	R
11:0	ADATAL	Data of AUX0. When write to the register, DATA will be clear to 0.	RW

19.5.2.6 ADC AUX Data Register (ADATA1,0x0014)

	ADATA1																															**BASE + 0x0014**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				ADATA3												Reserved				ADATA2											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:28	Reserved	Writing has no effect. Read as zero.	R
27:16	ADATAH	Data of AUX3. When write to the register, DATA will be clear to 0.	RW
15:12	Reserved	Writing has no effect. Read as zero.	R
11:0	ADATAL	Data of AUX2. When write to the register, DATA will be clear to 0.	RW

The measured voltage V_{SAD} (V_{SAD0} ~ V_{SAD3}) is as follows:

$$V_{SAD} = \frac{ADATA}{4096} \bullet VREF_ADC$$

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

19.5.2.7 ADC Clock Divide Register (ADCLK,0x0020)

The register ADCLK is used to set the A/D's clock dividing number.

	ADCLK																															BASE + 0x0020
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CLKDIV_MS																CLKDIV_US								CLKDIV							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	CLKDIV_MS	Dividing number to get ms clock from ADC clock. ms_clk = us_clk / (CLKDIV_MS +1)	RW
15:8	CLKDIV_US	Dividing number to get us clock from ADC clock. 0 : bypss ADC clock 2 -- 127 : CLKDIV_US is odd number : us_clk = adc_clk / (CLKDIV_US - 1) CLKDIV_US is even number : us_clk = adc_clk / CLKDIV_US	RW
7:0	CLKDIV	Dividing number to get ADC clock from device clock. 0 : bypass device clock 2 -- 255 : CLKDIV is odd number : adc_clk = dev_clk / (CLKDIV - 1) CLKDIV is even number : adc_clk = dev_clk / CLKDIV	RW

19.5.2.8 ADC Stable Register (ADSTB,0x0024)

ADC Stable register is used for delay some ADC clock cycle to wait ADC power down or stable when sampling AUX voltage.

	ADSTB																															BASE + 0x0024
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PD_DELAY																STABLE															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

31:16	PD_DELAY	Delay some ADC clock cycle to wait ADC power down	RW
15:0	STABLE	delay some ADC clock cycle to wait ADC stable when sampling AUX voltage.	RW

19.5.2.9 ADC REPEAT TIME Register (ADRETM,0x0028)

ADC REPEAT TIME register is used to set the sampling VBAT delay time when ADENA.REPEN is set to 1, and the repeat sampling wait time is RETTIME multiply clk_ms.

	ADRETM																															
																																BASE + 0x0028
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RETIME																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

19.6 SAR A/D Controller Guide

The following describes steps of using SAR-ADC.

19.6.1 Power Down Mode

1. When initial value of ADENA POWER is 1, the state of SADC is in power down state.
2. When you want to use SADC, you should first set ADENA.POWERON to 0 to power on SADC. And wait for at least 2ms, then you can enable required AUX.
3. When you want to power down SADC to get lower power, you should disable AUX, and then set ADENA.POWER to 1.

19.6.2 AUX Sample Operation

1. Set ADCLK.CLKDIV, ADCLK.CLKDIV_US and ADCLK.CLKDIV_MS to set A/D clock frequency.
2. Set ADENA.AUXn(0-3) to 1 to enable the channel.
3. When ADSTATE.VRDYn(0-3) = 1, you can read the sample data from corresponding ADVDATn(0-3). And the AUXEN will be set to 0 auto.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

20 EFUSE Slave Interface (EFUSE)

20.1 Overview

The EFUSE is provided 1K programmable bit, Total 1K bits are separated into eight segments.

Each segment can be programmed separately.
Each segment has a protect bit, which has higher priority than program segment selection.

Programming frequency is wide, and programming time can adjust use the EFUSE register.

Initial value of EFUSE is 0, when programmed to 1, it doesn't able to program back to 0 anymore.
Do not attempt to program any bit that already programmed to 1, such action will result unpredictable status to whole EFUSE block.

Programming voltage supply pin AVDEFUSE:
In program mode, supply AVDEFUSE with 2.5V.
Maximum accumulative time for AVDEFUSE pin exposed under 2.5V+/-10% should be less than 1 sec.
In read mode, leave AVDEFUSE to 0V or floating

20.2 Registers

Following chapter will descript the functions of all software accessible registers.
Conventions:
1. Register Address = Base + Address offset
2. Register read/write attribute
   R - Read only
   W - Write only
   RW - read and write
   RCW - read and write, but clear to 0 by read
   RSW - read and write, but set to 1 by read
   RWC - read and write, clear to 0 by write 1, write 0 has no effect
   RWS - read and write, set to 1 by write 1, write 0 has no effect
   RC - read only, and clear to 0 by read
   RS - read only, and set to 1 by read
   SPEC - special access method, relate to its description
3. Reset Value
   1 - reset to 1
   0 - reset to 0
   ? - value unknown after reset

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

20.2.1 Registers Memory Map

Table 20-1 Registers Memory Map-Address Base

Name	Base	Description
EFUSE	0x13540000	Address base of EFUSE

Table 20-2 EFUSE Register Description

Name	Description	Reset Value	Address Offset	Access Size
EFUCTRL	EFUSE Control Register	0x001F0000	0x0000	32
EFUCFG	EFUSE Configure Register	0x00000000	0x0004	32
EFUSTATE	EFUSE Status Register	0x00????00	0x0008	32
EFUDATA0	EFUSE Data 0 Register	0x0000????	0x000C	32
EFUDATA1	EFUSE Data 1 Register	0x00000000	0x0010	32
EFUDATA2	EFUSE Data 2 Register	0x00000000	0x0014	32
EFUDATA3	EFUSE Data 3 Register	0x00000000	0x0018	32
EFUDATA4	EFUSE Data 4 Register	0x00000000	0x001C	32
EFUDATA5	EFUSE Data 5 Register	0x00000000	0x0020	32
EFUDATA6	EFUSE Data 6 Register	0x00000000	0x0024	32
EFUDATA7	EFUSE Data 7 Register	0x00000000	0x0028	32

20.2.2 Registers and Fields Description

20.2.2.1 EFUSE Control Registers(EFUCTRL)

	EFUCTRL																															BASE + 0x0000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				address							Length					PG_EN	Reserved													WR_EN	RD_EN
RST	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:30	Reserved	Writing has no effect, read as zero.	R
27:21	Address	Indicate the start address wants to program or read Aligned to Byte	RW
20:16	Length	Indicate the length wants to program or read, efuse operate length equals to this value add 1. Byte number(min: 1byte, max: 32byte, default: 32byte)	RW
15	PG_EN	Programming EFUSE enable	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		1: Enable 0: Disable	
14:2	Reserved	Writing has no effect, read as zero.	RW
1	WR_EN	Write data to EFUSE data buffer enable 1: Enable 0: Disable This bit will change to 0 automatically when write procedure done	RW
0	RD_EN	Read data to EFUSE data buffer enable 1: Enable 0: Disable This bit will change to 0 automatically when read procedure done	RW

20.2.2.2 EFUSE Configure Register(EFUCFG)

	EFUCFG																															BASE + 0x0004
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	INT_EN	Reserved							RD_ADJ				RD_STROBE				WR_ADJ				WR_STROBE											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	INT_EN	Interrupt enable when read/write EFUSE done. 1: Enable 0: Disable	RW
30:24	Reserved	Writing has no effect, read as zero.	R
23:20	RD_ADJ	Adjust number of h2clk cycles when EFUSE reading unsigned value, h2clk period multiply (RD_ADJ + 1) should greater than 6.5 ns.	RW
19:16	RD_STROBE	Adjust number of h2clk cycles when EFUSE reading STROBE Signed value, h2clk period multiply(RD_ADJ + 5 + RD_STROBE) should greater than 35 ns.	RW
15:12	WR_ADJ	Adjust number of h2clk cycles when EFUSE programming unsigned value, h2clk period multiply (WR_ADJ + 1) should greater than 6.5 ns.	RW
11:0	WR_STROBE	Adjust number of h2clk cycles when EFUSE programming STROBE Signed value, h2clk period multiply(WR_ADJ + 1666 + WR_STROBE) should between 9us and 11us, typical 10us	RW

20.2.2.3 EFUSE Status Register (EFUSTATE)

	EFUSTATE	BASE + 0x0008

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved										NKU_PRT	UK_PRT	CHIPKEY	HIDEBLK	SOCINFO	TRIM3	TRIM2	TRIM1	TRIM0	CUT_PRT	CHIP_PRT	SCBT_PRT	DIS_JTAG	SCBT_EN	Reserved						WR_DONE	RD_DONE
RST	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
30:22	Reserved	Writing has no effect, read as zero.	R
21	NKU _PRT	NKU segment write protect 1: protect, this segment can't write 0: no protect, this segment can write	R
20	UK_PRT	User key segment write protect 1: protect, this segment can't write 0: no protect, this segment can write	R
19	CHIPKEY	Chip key segment write protect 1: protect, this segment can't write 0: no protect, this segment can write	R
18	HIDEBLK	hideblk segment write protect bit 1: protect, this segment can't write 0: no protect, this segment can write	R
17	SOCINFO	socinfo segment protect bit 1: protect, this segment can't write 0: no protect, this segment can write	R
16:13	TRIMn	Trim 0/1/2/3 segment protect bit 1: protect, this segment can't write 0: no protect, this segment can write	R
12	CUT_PRT	Custormer ID segment protect bit 1: protect, this segment can't write 0: no protect, this segment can write	R
11	CHIP_PRT	CHIP ID segment protect bit 1: protect, this segment can't write 0: no protect, this segment can write	R
10	SCBT _PRT	Security boot enable protect bit 1: protect, this segment can't write 0: no protect, this segment can write	R
9	DIS_JTAG	Disable JTAG 1: disable JTAG 0: enable JTAG	R
8	SCBT_EN	Security boot enable 1: enable Security boot 0: Normal boot	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

7:2	Reserved	Writing has no effect, read as zero.	RW
1	WR_DONE	Write data to EFUSE operate done flag 1: done 0: not done *This bit only can write to 0, and write to 0 will clear this flag.	RW
0	RD_DONE	Read EFUSE data operate done flag 1: done 0: not done *This bit only can write to 0, and write to 0 will clear this flag	RW

20.2.2.4 EFUSE Data Register(EFUDATAn)

	EFUDATAn (n=0,1,2,3,4,5,6,7)																BASE + 0x000C ~ BASE + 0x0028															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DATA	EFUSE DATA register. *EFUSE DATA0 register mapped low operate address, others mapped increased address.	RW

NOTE:

1. The EFUSE 1K bits are mapped to chip memory address, from 0x13540200 to 0x1354027F.
2. The EFUSE 1K programmable bits are separated into eight segments as below table. The first Segment used to store Ingenic chip id, second segment store customer id, third segment used to store ingenic chip information, forth segment store hide block, fifth segment used to store segment protect bit, sixth segment used to store chip key, seventh used to sore user key, the last segment used to store NKU.

Segment	1	2	3	4	5	6	7	8	9
Function	CHIP ID	CUT ID	TRIM	SOC INFO	HIDE BLK	PRT	CK	UK	NKU
Mapped Address	200 | 20F	210 | 21A	21B | 22A	22B | 22C	22D | 22D	22E | 22F	230 | 24F	250 | 26F	270 | 27F
Bits	128	88	128	16	8	16	256	256	128

3. The protect bit segment store others segment write protect bit, if protect bit programmed to 1, corresponding segment can not be able to program. The protect bit map as below table.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Bit	Mapped To EFUSE Status Register
The Protect bit Segment	15	Reserved
	14	Reserved
	13	NKU _PRT
	12	UK_PRT
	11	CHIPKEY
	10	HIDEBLK
	9	SOCINFO
	5~8	TRIMn
	4	CUT_PRT
	3	CHIP_PRT
	2	SCBT _PRT
	1	DIS_JTAG
	0	SCBT_EN

4. The EFUSE can read or write maximum 256bit in each time, but we strongly recommend operate each segment separately.
5. The segment(Root key/Chip key/User key/NKU) can only read/write by SC-ROM

20.3 Flow

20.3.1 Program EFUSE Flow

1. Set EFUCFG register(reading and programming timing).
2. Write want program data to EFUSE data buffer 0-7 registers
3. Set control register, indicate want to program address, data length.
4. Write control register PG_EN bit to 1
5. Connect AVDEFUSE pin to 2.5V
6. Write control register WR_EN bit to 1
7. Wait status register WR_DONE set to 1.
8. Disconnect AVDEFUSE pin from 2.5V.
9. Write control register PG_EN bit to 0.

20.3.2 Program Security Key Flow

1. Set EFUCFG register(reading and programming timing).
2. Write control register PG_EN bit to 1
3. Connect AVDEFUSE pin to 2.5V
4. Invoke SC-ROM controller to write data to Security key mapped address
5. Wait status register WR_DONE set to 1
6. jump to step 4, program all data like this
7. Disconnect AVDEFUSE pin from 2.5V.
8. Write control register PG_EN bit to 0.

NOTE:

*1: Do NOT pre-charge AVDEFUSE too early before EFUSE program started.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

The maximum 2.5V supply time to AVDEFUSE must be strictly controlled less than 1sec. Use on-chip counter and GPIO to coordinate external supply source.

*2: Only the 1.3.2 flow can be used to program the User Key and NKU Segment, The Root key and Chip key Segment will be programmed at CP by Ingenic, other segments only can program use 1.3.1 flow.

*3: The SC-ROM Controller can write Key segment 32bits once time.

20.3.3 Read EFUSE Flow

1. Set EFUCFG register(reading and programming timing).
2. Set control register to indicate what to read data address, read data length.
3. Set read enable register.
4. Wait status register RD_DONE set to 1 or EFUSE interrupted, software application can read EFUSE data buffer 0 – 7 registers.

20.3.4 Read Security Key/Random Number Flow

1. Invoke SC-ROM controller to read corresponding map address.

NOTE:

*1: EFSUE controller will read EFUSE protect bit segment automatically when chip reset, and update the EFUSE state register.

*2: Only 1.3.4 flow can be used to read all Keys, other segments only can read use 1.3.3 flow.

*3: The SC-ROM Controller can read Keys value 32bits once time.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Section 6

PERIPHERALS

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

21 General-Purpose I/O Ports(GPIO)

21.1 Overview

General Purpose I/O Ports (GPIO) is used in generating and capturing application-specific input and output signals. Each port can be programmed as an output, an input or function port that serves certain peripheral. As input, pull up/down can be enabled/disabled for the port and the port also can be configured as level or edge tripped interrupt source.

21.2 Features

- Each port can be configured as an input, an output or an alternate function port.
- Each port can be configured as an interrupt source of low/high level or rising/falling edge triggering, and every interrupt source can be masked independently.
- Each port has an internal PULL-UP/DOWN or pull-down resistor connected. The PULL-UP/DOWN/down resistor can be disabled.
- GPIO output 4interrupts, each group had an interrupt to INTC(Interrupt Controller).

21.3 About GPIO Port Summary Table

1) In the GPIO port summary, different pad type will determine different pad characteristics. it may just have pull up/down/hi-Z enable , power-on-start and receiver enable control port.
2) Each Pad can configured as four module function.
3) PC31 it's not GPIO port, but it will used with RTC to realize wakeup operate.

Table 21-1 GPIO port summary table illustration

PAD_ID	PAD_TYPE	PULL_RST	FUNC0	FUNC1	FUNC2	FUNC3
PA00	TYPEA	HIZ	sd0(io-0)	msc0_d0(io-0)	(i-0)	(i-0)
PA01	TYPEB	PU	sd2(io-0)	msc0_d1(io-0)	ssi0_dt(io-0)	sfc_dt(io-0)
PA02	TYPEA	PD	sd2(io-0)	msc0_d2(io-0)	ssi0_dr(io-0)	sfc_dr(io-0)
Group number	Instance pad type name (different type will decide GPIO function)	Pad pull enable active value. 00: HIZ 01: pull up(PU) 10: pull down(PD) 11: repeater	In table, each function column will expression one module port using relationship. such as the pad PA00, the FUNC0 "sd0_(io-0)", "sd0" means the NEMC module data port 0, "io" means function as I/O, "0" means when configure as other functions, GPIO supply value 0 to this function port.			

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

21.3.1 GPIO Port A Summary

Table 21-2 GPIO Port A summary

PAD_ID	PAD_NAME	Fun_0	Fun_1	Fun_2	Fun_3
PA00	PRUW08DGZ_G	lcd_d0_o(o)	slcd_d0_o(o)	tcu0_in0_i(i-0)	sa0_o(o)
PA01	PRUW08DGZ_G	lcd_d1_o(o)	slcd_d1_o(o)	tcu0_in1_i(i-0)	sa1_o(o)
PA02	PRUW08DGZ_G	lcd_d2_o(o)	slcd_d2_o(o)	tcu1_in0_i(i-0)	sa2_o(o)
PA03	PRUW08DGZ_G	lcd_d3_o(o)	slcd_d3_o(o)	tcu1_in1_i(i-0)	sa3_o(o)
PA04	PRUW08DGZ_G	lcd_d4_o(o)	slcd_d4_o(o)	tcu2_in0_i(i-0)	sa4_o(o)
PA05	PRUW08DGZ_G	lcd_d5_o(o)	slcd_d5_o(o)	tcu2_in1_i(i-0)	sa5_o(o)
PA06	PRUW08DGZ_G	lcd_d6_o(o)	slcd_d6_o(o)	tcu3_in0_i(i-0)	sa6_o(o)
PA07	PRUW08DGZ_G	lcd_d7_o(o)	slcd_d7_o(o)	tcu3_in1_i(i-0)	sa7_o(o)
PA08	PRUW08DGZ_G	lcd_d8_o(o)	slcd_d8_o(o)	cim_d0_i(i-0)	ad0(io-0)
PA09	PRUW08DGZ_G	lcd_d9_o(o)	slcd_d9_o(o)	cim_d1_i(i-0)	ad1(io-0)
PA10	PRUW08DGZ_G	lcd_d10_o(o)	slcd_d10_o(o)	cim_d2_i(i-0)	ad2(io-0)
PA11	PRUW08DGZ_G	lcd_d11_o(o)	slcd_d11_o(o)	cim_d3_i(i-0)	ad3(io-0)
PA12	PRUW08DGZ_G	lcd_d12_o(o)	slcd_d12_o(o)	cim_d4_i(i-0)	ad4(io-0)
PA13	PRUW08DGZ_G	lcd_d13_o(o)	slcd_d13_o(o)	cim_d5_i(i-0)	ad5(io-0)
PA14	PRUW08DGZ_G	lcd_d14_o(o)	slcd_d14_o(o)	cim_d6_i(i-0)	ad6(io-0)
PA15	PRUW08DGZ_G	lcd_d15_o(o)	slcd_d15_o(o)	cim_d7_i(i-0)	ad7(io-0)
PA16	PRUW08DGZ_G	lcd_d16_o(o)	(i-0)	(i-0)	ad8(io-0)
PA17	PRUW08DGZ_G	lcd_d17_o(o)	(i-0)	(i-0)	ad9(io-0)

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

PA18	PRUW08DGZ_G	lcd_d18_o(o)	(i-0)	(i-0)	ad10(io-0)
PA19	PRUW08DGZ_G	lcd_d19_o(o)	(i-0)	cim_exposure_o(o)	ad11(io-0)
PA20	PRUW08DGZ_G	lcd_d20_o(o)	(i-0)	cim_pclk_i(i-0)	ad12(io-0)
PA21	PRUW08DGZ_G	lcd_d21_o(o)	(i-0)	cim_vsync_i(i-0)	ad13(io-0)
PA22	PRUW08DGZ_G	lcd_d22_o(o)	(i-0)	cim_hsync_i(i-0)	ad14(io-0)
PA23	PRUW08DGZ_G	lcd_d23_o(o)	slcd_ce__o(o)	(i-0)	ad15(io-0)
PA24	PDUW08DGZ_G	lcd_pclk_o(o)	(i-0)	cim_mclk_o(o)	rd__o(o)
PA25	PRUW08DGZ_G	lcd_vsync_o(o)	slcd_dc_o(o)	(i-0)	we__o(o)
PA26	PRUW08DGZ_G	lcd_hsync_o(o)	slcd_wr_o(o)	(i-0)	AVD__o(o)
PA27	PRUW08DGZ_G	lcd_de_o(o)	slcd_te_i(i-1)	(i-0)	nemc_cs1__o(o)
PA28	PRUW08DGZ_G	ssi0_ce0__o(o)	ssi_slv_ce0__i(i-1)	i2c0_sck(io-1)	nemc_cs2__o(o)
PA29	PRUW08DGZ_G	ssi0_dr_i(i-0)	ssi_slv_dr_i(i-0)	i2c0_sda(io-1)	wait__i(i-1)
PA30	PRUW08DGZ_G	ssi0_dt_o(o)	ssi_slv_dt_o(o)	uart2_txd_o(o)	(i-0)
PA31	PRUW08DGZ_G	ssi0_clk_o(o)	ssi_slv_clk_i(i-0)	uart2_rxd_i(i-1)	pwm_tcu_trig_i(i-0)

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

21.3.2 GPIO Port B Summary

Table 21-3 GPIO Port B summary

PAD_ID	PAD_NAME	Fun_0	Fun_1	Fun_2	Fun_3
PB00	PRUW08DGZ_G	tdo_o(o)	uart2_txd_o(o)	(i-0)	(i-0)
PB01	PRUW08DGZ_G	tdi_i(i-0)	uart2_rxd_i(i-	(i-0)	(i-0)
PB02	PRUW08DGZ_G	tck_i(i-0)	uart1_txd_o(o)	ssi0_ce1__o(o)	(i-0)
PB03	PRUW08DGZ_G	tms_i(i-1)	uart1_rxd_i(i-	pwm_tcu_trig_i(i	(i-0)
PB04	PRUW08DGZ_G	uart3_txd_o(o)	uart1_rts__o(o	sfc0_ce1__o(o)	(i-0)
PB05	PRUW08DGZ_G	uart3_rxd_i(i-1)	uart1_cts__i(i	cdbus_tx_en_o(o)	(i-0)
PB06	PRUW08DGZ_G	(i-0)	(i-0)	(i-0)	(i-0)
PB07	PRUW08DGZ_G	uart0_rxd_i(i-1)	(i-0)	(i-0)	(i-0)
PB08	PRUW08DGZ_G	uart0_txd_o(o)	(i-0)	(i-0)	sa15_o(o)
PB09	PRUW08DGZ_G	uart0_cts__i(i-1)	pwm6_o(o)	tcu7_in0_i(i-0)	sa14_o(o)
PB10	PRUW08DGZ_G	uart0_rts__o(o)	pwm7_o(o)	tcu7_in1_i(i-0)	sa13_o(o)
PB11	PRUW08DGZ_G	(i-0)	(i-0)	(i-0)	(i-0)
PB12	PDUW08DGZ_G	msc0_clk_o(o)	ssi0_clk_o(o)	ssi_slv_clk_i(i-	(i-0)
PB13	PRUW08DGZ_G	msc0_cmd(io-0)	ssi0_dt_o(o)	ssi_slv_dt_o(o)	sa12_o(o)
PB14	PRUW08DGZ_G	msc0_d0(io-1)	ssi0_dr_i(i-0)	ssi_slv_dr_i(i-0	sa11_o(o)
PB15	PRUW08DGZ_G	msc0_d1(io-1)	ssi0_gpc_o(o)	i2c1_sck(io-1)	sa10_o(o)
PB16	PRUW08DGZ_G	msc0_d2(io-1)	ssi0_ce1__o(o)	i2c1_sda(io-1)	sa9_o(o)
PB17	PRUW08DGZ_G	msc0_d3(io-1)	ssi0_ce0__o(o)	ssi_slv_ce0__i(i	sa8_o(o)
PB18	PRUW08DGZ_G	(i-0)	(i-0)	(i-0)	(i-0)
PB19	PRUW08DGZ_G	i2c1_sck(io-1)	gmac_rxd0_i(i-	pwm5_o(o)	tcu6_in1_
PB20	PRUW08DGZ_G	i2c1_sda(io-1)	gmac_rxd1_i(i-	pwm6_o(o)	tcu7_in0_
PB21	PRUW08DGZ_G	i2s0_rx_data_i(i-1)	gmac_txd0_o(o)	pwm7_o(o)	tcu7_in1_
PB22	PDUW08DGZ_G	i2s0_rx_mclk_o(o)	gmac_phy_clk_o	(i-0)	(i-0)
PB23	PRUW08DGZ_G	i2s0_rx_bclk(io-0)	gmac_ref_clk_i	(i-0)	(i-0)

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

PB24	PRUW08DGZ_G	i2s0_rx_lrck(io-0)	gmac_rxdv_i(i-	(i-0)	(i-0)
PB25	PRUW08DGZ_G	i2s0_tx_data_o(o)	gmac_txd1_o(o)	(i-0)	(i-0)
PB26	PRUW08DGZ_G	i2s0_tx_mclk_o(o)	gmac_txen_o(o)	(i-0)	(i-0)
PB27	PRUW08DGZ_G	i2s0_tx_bclk(io-0)	gmac_mdc_o(o)	(i-0)	(i-0)
PB28	PRUW08DGZ_G	i2s0_tx_lrck(io-0)	gmac_mdio(io-0	(i-0)	(i-0)
PB29	PDUW08DGZ_G	(i-0)	(i-0)	(i-0)	(i-0)
PB30	PDUW08SDGZ_G	i2c0_sck(io-1)	cdbus_tx_en_o(	(i-0)	(i-0)
PB31	PDUW04SDGZ_G	i2c0_sda(io-1)	sfc0_ce1__o(o)	(i-0)	(i-0)

21.3.3 GPIO Port C Summary

Table 21-4 GPIO Port C summary

PAD_ID	PAD_NAME	Fun_0	Fun_1	Fun_2	Fun_3
PC00	PRDW08DGZ_G	pwm0_o(o)	tcu4_in0_i(i-0)	(i-0)	(i-0)
PC01	PRDW08DGZ_G	pwm1_o(o)	tcu4_in1_i(i-0)	(i-0)	(i-0)
PC02	PRDW08DGZ_G	pwm2_o(o)	tcu5_in0_i(i-0)	(i-0)	(i-0)
PC03	PRUW08DGZ_G	(i-0)	(i-0)	(i-0)	(i-0)
PC04	PRUW08DGZ_G	(i-0)	(i-0)	(i-0)	(i-0)
PC05	PRUW08DGZ_G	(i-0)	(i-0)	(i-0)	(i-0)
PC06	PRUW08DGZ_G	(i-0)	(i-0)	(i-0)	(i-0)
PC07	PRUW08DGZ_G	(i-0)	(i-0)	(i-0)	(i-0)
PC08	PRUW08DGZ_G	(i-0)	(i-0)	(i-0)	(i-0)
PC09	PRUW08DGZ_G	(i-0)	(i-0)	(i-0)	(i-0)
PC10	PRUW08DGZ_G	(i-0)	(i-0)	(i-0)	(i-0)
PC11	PRUW08DGZ_G	(i-0)	(i-0)	(i-0)	(i-0)
PC12	PRUW08DGZ_G	(i-0)	(i-0)	(i-0)	(i-0)
PC13	PRUW08DGZ_G	(i-0)	(i-0)	(i-0)	(i-0)
PC14	PRUW08DGZ_G	(i-0)	(i-0)	(i-0)	(i-0)
PC15	PRUW08DGZ_G	(i-0)	(i-0)	(i-0)	(i-0)
PC16	PRUW08DGZ_G	(i-0)	(i-0)	(i-0)	(i-0)
PC17	PDUW08DGZ_G	sfc0_clk_o(o)	msc0_clk_o(o)	(i-0)	(i-0)
PC18	PRUW08DGZ_G	sfc0_ce__o(o)	msc0_d3(io-1)	(i-0)	(i-0)
PC19	PRUW08DGZ_G	sfc0_dq0(io-0)	msc0_cmd(io-0)	(i-0)	(i-0)
PC20	PRUW08DGZ_G	sfc0_dq1(io-0)	msc0_d0(io-1)	(i-0)	(i-0)
PC21	PRUW08DGZ_G	sfc0_dq2_wp_(io-0)	msc0_d2(io-1)	(i-0)	(i-0)

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

PC22	PRUW08DGZ_G	sfc0_dq3_hold_(io-0)	msc0_d1(io-1)	(i-0)	(i-0)
PC23	PRUW08DGZ_G	(i-0)	(i-0)	(i-0)	(i-0)
PC24	PRDW08DGZ_G	drv_vbus_o(o)	pwm3_o(o)	tcu5_in1_i(i-0)	(i-0)
PC25	PRDW08DGZ_G	exclk_o(o)	pwm4_o(o)	tcu6_in0_i(i-0)	(i-0)
PC26	PRDW08DGZ_G	rtc32k_o(o)	pwm5_o(o)	tcu6_in1_i(i-0)	(i-0)
PC27	PDUW04SDGZ_G	BOOT_SEL0	(i-0)	(i-0)	(i-0)
PC28	PDUW04SDGZ_G	BOOT_SEL1	(i-0)	(i-0)	(i-0)
PC29	PRUW08DGZ_G	(i-0)	(i-0)	(i-0)	(i-0)
PC30	PRUW08DGZ_G	(i-0)	(i-0)	(i-0)	(i-0)
PC31	PDUW08SDGZ_G	WKUP_	(i-0)	(i-0)	(i-0)

21.3.4 GPIO Port D Summary

Table 21-5 GPIO Port D summary

PAD_ID	PAD_NAME	Fun_0	Fun_1	Fun_2	Fun_3
PD00	PDUW08DGZ	msc1_clk_o(o)	cdbus_tx_o(o)	(i-0)	(i-0)
PD01	PRUW08DGZ	msc1_cmd(io-0)	cdbus_rx_i(i-1)	(i-0)	(i-0)
PD02	PRUW08DGZ	msc1_d0(io-1)	can0_tx_o(o)	(i-0)	(i-0)
PD03	PRUW08DGZ	msc1_d1(io-1)	can0_rx_i(i-1)	(i-0)	(i-0)
PD04	PRUW08DGZ	msc1_d2(io-1)	can1_tx_o(o)	uart3_txd_o(o)	(i-0)
PD05	PRUW08DGZ	msc1_d3(io-1)	can1_rx_i(i-1)	uart3_rxd_i(i-1)	(i-0)
PD06	PRUW08DGZ_G	(i-0)	(i-0)	(i-0)	(i-0)
PD07	PRUW08DGZ_G	(i-0)	(i-0)	(i-0)	(i-0)
PD08	PRUW08DGZ_G	(i-0)	(i-0)	(i-0)	(i-0)
PD09	PRUW08DGZ_G	(i-0)	(i-0)	(i-0)	(i-0)
PD10	PRUW08DGZ_G	(i-0)	(i-0)	(i-0)	(i-0)
PD11	PRUW08DGZ_G	(i-0)	(i-0)	(i-0)	(i-0)
PD12	PRUW08DGZ_G	(i-0)	(i-0)	(i-0)	(i-0)
PD13	PRUW08DGZ_G	(i-0)	(i-0)	(i-0)	(i-0)
PD14	PRUW08DGZ_G	(i-0)	(i-0)	(i-0)	(i-0)
PD15	PRUW08DGZ_G	(i-0)	(i-0)	(i-0)	(i-0)
PD16	PRUW08DGZ_G	(i-0)	(i-0)	(i-0)	(i-0)
PD17	PRUW08DGZ_G	(i-0)	(i-0)	(i-0)	(i-0)
PD18	PRUW08DGZ_G	(i-0)	(i-0)	(i-0)	(i-0)
PD19	PRUW08DGZ_G	(i-0)	(i-0)	(i-0)	(i-0)
PD20	PRUW08DGZ_G	(i-0)	(i-0)	(i-0)	(i-0)
PD21	PRUW08DGZ_G	(i-0)	(i-0)	(i-0)	(i-0)
PD22	PRUW08DGZ_G	(i-0)	(i-0)	(i-0)	(i-0)
PD23	PRUW08DGZ_G	(i-0)	(i-0)	(i-0)	(i-0)
PD24	PRUW08DGZ_G	(i-0)	(i-0)	(i-0)	(i-0)

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

PD25	PRUW08DGZ_G	(i-0)	(i-0)	(i-0)	(i-0)
PD26	PRUW08DGZ_G	(i-0)	(i-0)	(i-0)	(i-0)
PD27	PRUW08DGZ_G	(i-0)	(i-0)	(i-0)	(i-0)
PD28	PRUW08DGZ_G	(i-0)	(i-0)	(i-0)	(i-0)
PD29	PRUW08DGZ_G	(i-0)	(i-0)	(i-0)	(i-0)
PD30	PRUW08DGZ_G	(i-0)	(i-0)	(i-0)	(i-0)
PD31	PRUW08DGZ_G	(i-0)	(i-0)	(i-0)	(i-0)

21.3.5 GPIO Port Z-Shadow Group

The group is a dummy group which is not mapping to any on-chip ports. It is used to avoid 3rd (intermittent) state error during configuration. Please refer for detailed information.

21.4 Registers Description

Following chapter will descript the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. Register read/write attribute
   - R - Read only
   - W - Write only
   - RW - read and write
   - RCW - read and write, but clear to 0 by read
   - RSW - read and write, but set to 1 by read
   - RWC - read and write, clear to 0 by write 1, write 0 has no effect
   - RWS - read and write, set to 1 by write 1, write 0 has no effect
   - RC - read only, and clear to 0 by read
   - RS - read only, and set to 1 by read
   - SPEC - special access method, relate to its description
3. Reset Value
   - 1 - reset to 1
   - 0 - reset to 0
   - ? - value unknown after reset
4. Not all the register will be use in this chapter, please review the chapter of "Function Overview" for more detail.
5. Table 21-7 summarized all memory-mapped registers, which can be programmed to operate GPIO port and alternate function port sharing configuration.
6. All registers are in 32-bits width. Usually, 1 bit in the register affects a corresponding GPIO port and every GPIO port can be operated independently.
7. Gray bits in the register description indicates that this feature in the GPIO group who did not

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

use, program can be ignored.

21.4.1 Register Memory Map

Table 21-6 Registers Memory Map Base Address

Name	Base	Description
PA	0x10010000	Address base of GPIO Port A
PB	0x10010100	Address base of GPIO Port B
PC	0x10010200	Address base of GPIO Port C
PD	0x10010300	Address base of GPIO Port D
PZ	0x10010700	Address base of GPIO Group Z (Shadow group)

Table 21-7 GPIO Registers Group Map

Name	RW	Description	Reset Value	Address Offset	Access Size
GPIO PORT A					
PAPINL	R	PORTA PIN Level Register	0x????_????	0x00	32
PAINT	RW	PORTA Interrupt Register	0x0000_0000	0x10	32
PAINTS	W	PORTA Interrupt Set Register	0x0000_0000	0x14	32
PAINTC	W	PORTA Interrupt Clear Register	0x0000_0000	0x18	32
PAMSK	RW	PORTA Interrupt Mask Register	0xFFFF_FFFF	0x20	32
PAMSKS	W	PORTA Interrupt Mask Set Register	0x0000_0000	0x24	32
PAMSKC	W	PORTA Interrupt Mask Clear Register	0x0000_0000	0x28	32
PAPAT1	RW	PORTA Pattern 1 Register	0xFFFF_FFFF	0x30	32
PAPAT1S	W	PORTA Pattern 1 Set Register	0x0000_0000	0x34	32
PAPAT1C	W	PORTA Pattern 1 Clear Register	0x0000_0000	0x38	32
PAPAT0	RW	PORTA Pattern 0 Register	0x0000_0000	0x40	32
PAPAT0S	W	PORTA Pattern 0 Set Register	0x0000_0000	0x44	32
PAPAT0C	W	PORTA Pattern 0 Clear Register	0x0000_0000	0x48	32
PAFLG	R	PORTA FLAG Register	0x0000_0000	0x50	32
PAFLGC	RC	PORTA FLAG Clear Register	0x0000_0000	0x58	32
PAEDG	RW	PORTA Dual-Edge Interrupt Register	0x0000_0000	0x70	32
PAEDGS	W	PORTA Dual-Edge Interrupt Set Register	0x0000_0000	0x74	32
PAEDGC	W	PORT A Dual-Edge Interrupt Clear Register	0x0000_0000	0x78	32
PAPU	RW	PORTA PULL-UP/DOWN enabled State Register	0x0000_0000	0x80	32
PAPUS	W	PORTA PULL-UP/DOWN enabled State Set Register	0x0000_0000	0x84	32
PAPUC	W	PORTA PULL-UP/DOWN enabled State	0x0000_0000	0x88	32

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		Clear Register			
GPIO PORT B					
PBPINL	R	PORTB PIN Level Register	0x????_????	0x00	32
PBINT	RW	PORTB Interrupt Register	0x0000_0000	0x10	32
PBINTS	W	PORTB Interrupt Set Register	0x0000_0000	0x14	32
PBINTC	W	PORTB Interrupt Clear Register	0x0000_0000	0x18	32
PBMSK	RW	PORTB Interrupt Mask Register	0xDFFB_F7B0	0x20	32
PBMSKS	W	PORTB Interrupt Mask Set Register	0x0000_0000	0x24	32
PBMSKC	W	PORTB Interrupt Mask Clear Register	0x0000_0000	0x28	32
PBPAT1	RW	PORTB Pattern 1 Register	0xDFFB_F7B0	0x30	32
PBPAT1S	W	PORTB Pattern 1 Set Register	0x0000_0000	0x34	32
PBPAT1C	W	PORTB Pattern 1 Clear Register	0x0000_0000	0x38	32
PBPAT0	RW	PORTB Pattern 0 Register	0x0000_0000	0x40	32
PBPAT0S	W	PORTB Pattern 0 Set Register	0x0000_0000	0x44	32
PBPAT0C	W	PORTB Pattern 0 Clear Register	0x0000_0000	0x48	32
PBFLG	R	PORTB FLAG Register	0x0000_0000	0x50	32
PBFLGC	RC	PORTB FLAG Clear Register	0x0000_0000	0x58	32
PBEDG	RW	PORTB Dual-Edge Interrupt Register	0x0000_0000	0x70	32
PBEDGS	W	PORTB Dual-Edge Interrupt Set Register	0x0000_0000	0x74	32
PBEDGC	W	PORTB Dual-Edge Interrupt Clear Register	0x0000_0000	0x78	32
PBPU	RW	PORTB PULL-UP/DOWN enabled State Register	0x0000_000e	0x80	32
PBPUS	W	PORTB PULL-UP/DOWN enabled State Set Register	0x0000_0000	0x84	32
PBPUC	W	PORTB PULL-UP/DOWN enabled State Clear Register	0x0000_0000	0x88	32
GPIO PORT C					
PCPINL	R	PORTC PIN Level Register	0x????_????	0x00	32
PCINT	RW	PORTC Interrupt Register	0x0000_0000	0x10	32
PCINTS	W	PORTC Interrupt Set Register	0x0000_0000	0x14	32
PCINTC	W	PORTC Interrupt Clear Register	0x0000_0000	0x18	32
PCMSK	RW	PORTC Interrupt Mask Register	0x9F7E_0007	0x20	32
PCMSKS	W	PORTC Interrupt Mask Set Register	0x0000_0000	0x24	32
PCMSKC	W	PORTC Interrupt Mask Clear Register	0x0000_0000	0x28	32
PCPAT1	RW	PORTC Pattern 1 Register	0x9F7E_0007	0x30	32
PCPAT1S	W	PORTC Pattern 1 Set Register	0x0000_0000	0x34	32
PCPAT1C	W	PORTC Pattern 1 Clear Register	0x0000_0000	0x38	32
PCPAT0	RW	PORTC Pattern 0 Register	0x0000_0000	0x40	32
PCPAT0S	W	PORTC Pattern 0 Set Register	0x0000_0000	0x44	32
PCPAT0C	W	PORTC Pattern 0 Clear Register	0x0000_0000	0x48	32

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

PCFLG	R	PORTC FLAG Register	0x0000_0000	0x50	32
PCFLGC	RC	PORTC FLAG Clear Register	0x0000_0000	0x58	32
PCEDG	RW	PORTC Dual-Edge Interrupt Register	0x0000_0000	0x70	32
PCEDGS	W	PORTC Dual-Edge Interrupt Set Register	0x0000_0000	0x74	32
PCEDGC	W	PORTC Dual-Edge Interrupt Clear Register	0x0000_0000	0x78	32
PCPU	RW	PORTC PULL-UP/DOWN enabled State Register	0x0700_0007	0x80	32
PCPUS	W	PORTC PULL-UP/DOWN enabled State Set Register	0x0000_0000	0x84	32
PCPUC	W	PORTC PULL-UP/DOWN enabled State Clear Register	0x0000_0000	0x88	32
GPIO PORT D					
PDPINL	R	PORTD PIN Level Register	0x????_????	0x00	32
PDINT	RW	PORTD Interrupt Register	0x0000_0000	0x10	32
PDINTS	W	PORTD Interrupt Set Register	0x0000_0000	0x14	32
PDINTC	W	PORTD Interrupt Clear Register	0x0000_0000	0x18	32
PDMSK	RW	PORTD Interrupt Mask Register	0x0000_003F	0x20	32
PDMSKS	W	PORTD Interrupt Mask Set Register	0x0000_0000	0x24	32
PDMSKC	W	PORTD Interrupt Mask Clear Register	0x0000_0000	0x28	32
PDPAT1	RW	PORTD Pattern 1 Register	0x0000_003F	0x30	32
PDPAT1S	W	PORTD Pattern 1 Set Register	0x0000_0000	0x34	32
PDPAT1C	W	PORTD Pattern 1 Clear Register	0x0000_0000	0x38	32
PDPAT0	RW	PORTD Pattern 0 Register	0x0000_0000	0x40	32
PDPAT0S	W	PORTD Pattern 0 Set Register	0x0000_0000	0x44	32
PDPAT0C	W	PORTD Pattern 0 Clear Register	0x0000_0000	0x48	32
PDFLG	R	PORTD FLAG Register	0x0000_0000	0x50	32
PDFLGC	RC	PORTD FLAG Clear Register	0x0000_0000	0x58	32
PDEDG	RW	PORTD Dual-Edge Interrupt Register	0x0000_0000	0x70	32
PDEDGS	W	PORTD Dual-Edge Interrupt Set Register	0x0000_0000	0x74	32
PDEDGC	W	PORTD Dual-Edge Interrupt Clear Register	0x0000_0000	0x78	32
PDPU	RW	PORTD PULL-UP/DOWN enabled State Register	0x0000_0000	0x80	32
PDPUS	W	PORTD PULL-UP/DOWN enabled State Set Register	0x0000_0000	0x84	32
PDPUC	W	PORTD PULL-UP/DOWN enabled State Clear Register	0x0000_0000	0x88	32
Shadow Register Group PZ					
PzINTS	W	Shadow Interrupt Set Register	0x0000_0000	0x0014	32
PzINTC	W	Shadow Interrupt Clear Register	0x0000_0000	0x0018	32
PzMSKS	W	Shadow Interrupt Mask Set Register	0x0000_0000	0x0024	32

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

PzMSKC	W	Shadow Interrupt Mask Clear Register	0x0000_0000	0x0028	32
PzPAT1S	W	Shadow Interrupt Pattern 1 Set Register	0x0000_0000	0x0034	32
PzPAT1C	W	Shadow Interrupt Pattern 1 Clear Register	0x0000_0000	0x0038	32
PzPAT0S	W	Shadow Interrupt Pattern 0 Set Register	0x0000_0000	0x0044	32
PzPAT0C	W	Shadow Interrupt Pattern 0 Clear Register	0x0000_0000	0x0048	32
PzGID2LD	W	PORT Group ID to be load from PZ Register	0x0000_0000	0x00F0	32

Note: 1. Pz* in the description of register is use for shadow operation for other groups, more details will description as follow chapters.

21.4.2 Register and Fields Description

21.4.2.1 PORT PIN Level Registers (PxPINL,0x0000)

PAPINL,PBPINL,PCPINL and PDPINL are four 32-bit PORT PIN level registers. They are read-only registers.

	PxPINL																															Base + 0x0000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PINL31	PINL30	PINL29	PINL28	PINL27	PINL26	PINL25	PINL24	PINL23	PINL22	PINL21	PINL20	PINL19	PINL18	PINL17	PINL16	PINL15	PINL14	PINL13	PINL12	PINL11	PINL10	PINL09	PINL08	PINL07	PINL06	PINL05	PINL04	PINL03	PINL02	PINL01	PINL00
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
31:0	PINL n	Where n = 0 ~ 31 and PBPINL n = PBPINL0 ~ PBPINL31. The PORTB PIN level can be read by reading PINL n bit in register PBPINL.	R

Note: 1. In the table, "x" represents the group A,B,C,D and E behind the description of similar.

21.4.2.2 PORT Interrupt Registers (PxINT,0x0010)

PAINT,PBINT,PCINT and PDINT are four 32-bit PORT interrupt registers.

	PxINT																															Base + 0x0010
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	INT31	INT30	INT29	INT28	INT27	INT26	INT25	INT24	INT23	INT22	INT21	INT20	INT19	INT18	INT17	INT16	INT15	INT14	INT13	INT12	INT11	INT10	INT09	INT08	INT07	INT06	INT05	INT04	INT03	INT02	INT01	INT00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	INT n	Where n = 0 ~ 31 and INT n = INT31 ~ INT00. Interrupt enable. 0: Corresponding pin is used as device functions or normal gpio 1: Corresponding pin is used as interrupt	RW

21.4.2.3 PORT Interrupt Set Registers (PxINTS,0x0014)

PAINTS,PBINTS,PCINTS and PDINTS are four 32-bit PORT interrupt set registers.

	PxINTS																															**Base + 0x0014**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	INTS31	INTS30	INTS29	INTS28	INTS27	INTS26	INTS25	INTS24	INTS23	INTS22	INTS21	INTS20	INTS19	INTS18	INTS17	INTS16	INTS15	INTS14	INTS13	INTS12	INTS11	INTS10	INTS09	INTS08	INTS07	INTS06	INTS05	INTS04	INTS03	INTS02	INTS01	INTS00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	INTS n	Writing 1 to INTS n will set INT n to 1 in register PBINT. Writing 0 to INTS n will no use.	W

21.4.2.4 PORT Interrupt Clear Registers (PxINTC,0x0018)

PAINTC,PBINTC,PCINTC and PDINTC are four 32-bit PORT interrupt clear registers.

	PxINTC																															**Base + 0x0018**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	INTC31	INTC30	INTC29	INTC28	INTC27	INTC26	INTC25	INTC24	INTC23	INTC22	INTC21	INTC20	INTC19	INTC18	INTC17	INTC16	INTC15	INTC14	INTC13	INTC12	INTC11	INTC10	INTC09	INTC08	INTC07	INTC06	INTC05	INTC04	INTC03	INTC02	INTC01	INTC00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	R/W
31:0	INTC n	Writing 1 to INTC n will set INT n to 0 in register PxINT. Writing 0 to INTC n will no use.	W

21.4.2.5 PORT Mask Registers (PxMSK,0x0020)

PAMSK,PBMSK,PCMSK and PDMSK are four 32-bit PORT mask registers.

	PxMSK																															Base + 0x0020
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSK31	MSK30	MSK29	MSK28	MSK27	MSK26	MSK25	MSK24	MSK23	MSK22	MSK21	MSK20	MSK19	MSK18	MSK17	MSK16	MSK15	MSK14	MSK13	MSK12	MSK11	MSK10	MSK09	MSK08	MSK07	MSK06	MSK05	MSK04	MSK03	MSK02	MSK01	MSK00
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
31:0	MSK n	Where n = 0 ~ 31 and MSK n = MSK31 ~ MSK0. When INT n = 1: 0: Enable the pin as an interrupt source 1: Disable the pin as an interrupt source When INT n = 0: 0: Corresponding pin will be used as device function 1: Corresponding pin will be used as gpio	RW

Note:

1. Not every PBD support Input Enable Control, please check out Function Overview chapter for details.

21.4.2.6 PORT Mask Set Registers (PxMSKS,0x0024)

PAMSKS,PBMSKS,PCMSKS and PDMSKS are four 32-bit PORT mask set registers.

	PxMSKS																															Base + 0x0024
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSKS31	MSKS30	MSKS29	MSKS28	MSKS27	MSKS26	MSKS25	MSKS24	MSKS23	MSKS22	MSKS21	MSKS20	MSKS19	MSKS18	MSKS17	MSKS16	MSKS15	MSKS14	MSKS13	MSKS12	MSKS11	MSKS10	MSKS09	MSKS08	MSKS07	MSKS06	MSKS05	MSKS04	MSKS03	MSKS02	MSKS01	MSKS00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	MSKS n	Writing 1 to MSKS n will set MSK n to 1 in register PxMSK.	W

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		Writing 0 to MSKS n will no use.	

21.4.2.7 PORT Mask Clear Registers (PxMSKC,0x0028)

PAMSKC,PBMSKC,PCMSKC and PDMSKC are four 32-bit PORT mask clear registers.

	PxMSKC																															Base + 0x0028
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSKC31	MSKC30	MSKC29	MSKC28	MSKC27	MSKC26	MSKC25	MSKC24	MSKC23	MSKC22	MSKC21	MSKC20	MSKC19	MSKC18	MSKC17	MSKC16	MSKC15	MSKC14	MSKC13	MSKC12	MSKC11	MSKC10	MSKC09	MSKC08	MSKC07	MSKC06	MSKC05	MSKC04	MSKC03	MSKC02	MSKC01	MSKC00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	MSKC n	Writing 1 to MSKC n will set MSK n to 0 in register PxMSK. Writing 0 to MSKC n will no use.	W

21.4.2.8 PORT PAT1/Direction Registers (PxPAT1,0x0030)

PAPAT1,PBPAT1,PCPAT1 and PDPAT1 are four 32-bit PORT Pattern1/direction registers.

	PxPAT1																															Base + 0x0030
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PAT131	PAT130	PAT129	PAT128	PAT127	PAT126	PAT125	PAT124	PAT123	PAT122	PAT121	PAT120	PAT119	PAT118	PAT117	PAT116	PAT115	PAT114	PAT113	PAT112	PAT111	PAT110	PAT109	PAT108	PAT107	PAT106	PAT105	PAT104	PAT103	PAT102	PAT101	PAT100
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W

31:0	PAT1 n	Where n = 0 ~ 31 and PAT1 n = PAT131 ~ PAT10.
		● When INT n = 1 (Interrupt function):
		  ● 0: Level trigger interrupt
		  ● 1: Edge trigger interrupt
		● When INT n = 0 and MSK = 0 (Device function):
		  ● 0: Corresponding pin is used as device 0 or device 1 function
		  ● 1: Corresponding pin is used as device 2 or device 3 function
		● When INT n = 0 and MSK = 1 (GPIO function):
		  ● 0: Corresponding pin is used as gpio output
		  ● 1: Corresponding pin is used as gpio input
			RW

Note:

1. Not every PBD support Input Enable Control, please check out Function Overview chapter for details.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

21.4.2.9 PORT PAT1/Direction Set Registers (PxPAT1S,0x0034)

PAPAT1S,PBPAT1S,PCPAT1S and PDPAT1S are four 32-bit PORT Pattern1 or direction set registers.

	PxPAT1S																															Base + 0x0034
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PAT1S31	PAT1S30	PAT1S29	PAT1S28	PAT1S27	PAT1S26	PAT1S25	PAT1S24	PAT1S23	PAT1S22	PAT1S21	PAT1S20	PAT1S19	PAT1S18	PAT1S17	PAT1S16	PAT1S15	PAT1S14	PAT1S13	PAT1S12	PAT1S11	PAT1S10	PAT1S09	PAT1S08	PAT1S07	PAT1S06	PAT1S05	PAT1S04	PAT1S03	PAT1S02	PAT1S01	PAT1S00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	PAT1S n	Writing 1 to PAT1S n will set PAT1 n to 1 in register PxPAT1. Writing 0 to PAT1S n will no use.	W

21.4.2.10 PORT PAT1/Direction Clear Registers (PxPAT1C,0x0038)

PAPAT1C,PBPAT1C,PCPAT1C and PDPAT1C are four 32-bit PORT Pattern1 or direction clear registers.

	PxPAT1S,																															Base + 0x0038
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PAT1C31	PAT1C30	PAT1C29	PAT1C28	PAT1C27	PAT1C26	PAT1C25	PAT1C24	PAT1C23	PAT1C22	PAT1C21	PAT1C20	PAT1C19	PAT1C18	PAT1C17	PAT1C16	PAT1C15	PAT1C14	PAT1C13	PAT1C12	PAT1C11	PAT1C10	PAT1C09	PAT1C08	PAT1C07	PAT1C06	PAT1C05	PAT1C04	PAT1C03	PAT1C02	PAT1C01	PAT1C00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	PAT1C n	Writing 1 to PAT1C n will set PAT1 n to 0 in register PxPAT1. Writing 0 to PAT1C n will no use.	W

21.4.2.11 PORT PAT0/Data Registers (PxPAT0,0x0040)

PAPAT0,PBPAT0,PCPAT0 and PDPAT0 are four 32-bit PORT Pattern0 or data registers.

	PxPAT0,																															Base + 0x0040
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PAT031	PAT030	PAT029	PAT028	PAT027	PAT026	PAT025	PAT024	PAT023	PAT022	PAT021	PAT020	PAT019	PAT018	PAT017	PAT016	PAT015	PAT014	PAT013	PAT012	PAT011	PAT010	PAT009	PAT008	PAT007	PAT006	PAT005	PAT004	PAT003	PAT002	PAT001	PAT000
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

31:0	PAT0 n	Where n = 0 ~ 31 and PAT0 n = PAT00 ~ PAT031. When INTn = 1 and PAT1 = 0: 0: Port is low level triggered interrupt input 1: Port is high level triggered interrupt input When INTn = 1 and PAT1 = 1: 0: Port is falling edge triggered interrupt input 1: Port is rising edge triggered interrupt input When INTn = 0 and MSK = 0 and PAT1 = 0: 0: Port is pin of device 0 1: Port is pin of device 1 When INTn = 0 and MSK = 0 and PAT1 = 1: 0: Port is pin of device 2 1: Port is pin of device 3 When INTn = 0 and MSK = 1 and PAT1 = 0: 0: Port is GPIO output 0 1: Port is GPIO output 1	RW

Note:

1. Not every PBD support Input Enable Control, please check out Function Overview chapter for details.

21.4.2.12 PORT PAT0/Data Set Registers (PxPAT0S,0x0044)

PAPAT0S,PBPAT0S,PCPAT0S and PDPAT0S are four 32-bit PORT Pattern0 or data set registers.

	PxPAT0S																															Base + 0x0044
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PAT0S31	PAT0S30	PAT0S29	PAT0S28	PAT0S27	PAT0S26	PAT0S25	PAT0S24	PAT0S23	PAT0S22	PAT0S21	PAT0S20	PAT0S19	PAT0S18	PAT0S17	PAT0S16	PAT0S15	PAT0S14	PAT0S13	PAT0S12	PAT0S11	PAT0S10	PAT0S09	PAT0S08	PAT0S07	PAT0S06	PAT0S05	PAT0S04	PAT0S03	PAT0S02	PAT0S01	PAT0S00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	PAT0S n	Writing 1 to PAT0S n will set PAT0 n to 1 in register PAT0. Writing 0 to PAT0S n will no use.	W

21.4.2.13 PORT PAT0/Data Clear Registers (PxPAT0C,0x0048)

PAPAT0C,PBPAT0C,PCPAT0C and PDPAT0C are four 32-bit PORT Pattern 0 or data clear registers.

	PxPAT0C																															Base + 0x0048
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	PAT0C31	PAT0C30	PAT0C29	PAT0C28	PAT0C27	PAT0C26	PAT0C25	PAT0C24	PAT0C23	PAT0C22	PAT0C21	PAT0C20	PAT0C19	PAT0C18	PAT0C17	PAT0C16	PAT0C15	PAT0C14	PAT0C13	PAT0C12	PAT0C11	PAT0C10	PAT0C09	PAT0C08	PAT0C07	PAT0C06	PAT0C05	PAT0C04	PAT0C03	PAT0C02	PAT0C01	PAT0C00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	PAT0C n	Writing 1 to PAT0C n will set PAT0 n to 0 in register PAT0. Writing 0 to PAT0C n will no use.	W

21.4.2.14 PORT FLAG Registers (PxFLG,0x0050)

PAFLG,PBFLG,PCFLG and PDFLG are four 32-bit PORT flag registers. They are read-only registers.

	PxFLG																															**Base + 0x0050**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FLAG31	FLAG30	FLAG29	FLAG28	FLAG27	FLAG26	FLAG25	FLAG24	FLAG23	FLAG22	FLAG21	FLAG20	FLAG19	FLAG18	FLAG17	FLAG16	FLAG15	FLAG14	FLAG13	FLAG12	FLAG11	FLAG10	FLAG09	FLAG08	FLAG07	FLAG06	FLAG05	FLAG04	FLAG03	FLAG02	FLAG01	FLAG00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	FLAG n	Where n = 0 ~ 31 and FLAG n = FLAG00 ~ FLAG31. ● FLAG n is interrupt flag bit for checking the interrupt whether to happen. ● When GPIO is used as interrupt function and the interrupt happened, the FLAG n in PBFLG will be set to 1.	R

Note:

1. Not every PBD support Input Enable Control, please check out Function Overview chapter for details.

21.4.2.15 PORT FLAG Clear Registers (PxFLGC,0x0058)

PAFLGC,PBFLGC,PCFLGC and PDFLGC are four 32-bit PORT flag clear registers. They are read-only registers.

	PxFLGC																															**Base + 0x0058**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	FLAGC31	FLAGC30	FLAGC29	FLAGC28	FLAGC27	FLAGC26	FLAGC25	FLAGC24	FLAGC23	FLAGC22	FLAGC21	FLAGC20	FLAGC19	FLAGC18	FLAGC17	FLAGC16	FLAGC15	FLAGC14	FLAGC13	FLAGC12	FLAGC11	FLAGC10	FLAGC09	FLAGC08	FLAGC07	FLAGC06	FLAGC05	FLAGC04	FLAGC03	FLAGC02	FLAGC01	FLAGC00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	FLAGC n	• When GPIO is used as interrupt function and when write 1 to the bit, the bit FLAG n in PxFLG will be cleared.	RC

21.4.2.16 PORT Dual-Edge Interrupt Register (PxEDG,0x70)

PORT x GROUP dual-edge interrupt register.

	PxEDG																															**0x70**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EDG31	EDG30	EDG29	EDG28	EDG27	EDG26	EDG25	EDG24	EDG23	EDG22	EDG21	EDG20	EDG19	EDG18	EDG17	EDG16	EDG15	EDG14	EDG13	EDG12	EDG11	EDG10	EDG09	EDG08	EDG07	EDG06	EDG05	EDG04	EDG03	EDG02	EDG01	EDG00
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
31:0	EDG n	Where n = 0 ~ 31 and EDG n = EDG00 ~ EDG31. EDG n is used to switch active edge of the interrupt from the pad. (please refer to chapter 21.5.1) 0: single-edge interrupt detection (the edge selection bits, PAT0 n enabled) 1: dual-edge interrupt detection (the edge selection bits, PAT0 n ignored)	RW

21.4.2.17 PORT Dual-Edge Interrupt Set Register (PxEDGS,0x74)

PORT x GROUP dual-edge interrupt set register, WRITE-ONLY.

	PxEDGS																															**0x74**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	EDGS31	EDGS30	EDGS29	EDGS28	EDGS27	EDGS26	EDGS25	EDGS24	EDGS23	EDGS22	EDGS21	EDGS20	EDGS19	EDGS18	EDGS17	EDGS16	EDGS15	EDGS14	EDGS13	EDGS12	EDGS11	EDGS10	EDGS09	EDGS08	EDGS07	EDGS06	EDGS05	EDGS04	EDGS03	EDGS02	EDGS01	EDGS00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	EDGS n	Writing 1 to EDGS n will set EDG n to 1 in register PEEDG. Writing 0 to EDGS n will be ignored.	W

21.4.2.18 PORT Dual-Edge Interrupt Clear Register (PxEDGC,0x78)

PORT x GROUP dual-edge interrupt clear register, WRITE-ONLY.

	PxEDGC																															**0x78**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EDGC31	EDGC30	EDGC29	EDGC28	EDGC27	EDGC26	EDGC25	EDGC24	EDGC23	EDGC22	EDGC21	EDGC20	EDGC19	EDGC18	EDGC17	EDGC16	EDGC15	EDGC14	EDGC13	EDGC12	EDGC11	EDGC10	EDGC09	EDGC08	EDGC07	EDGC06	EDGC05	EDGC04	EDGC03	EDGC02	EDGC01	EDGC00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	EDGC n	Writing 1 to EDGC n will clear EDG n to 0 in register PEEDG. Writing 0 to EDGC n will be ignored.	W

21.4.2.19 PORT PULL-UP/DOWN State Register (PxPU,0x80)

PORT A GROUP PULL-UP/DOWN enabled State register.

	PAPU																															**0x80**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PU31	PU30	PU29	PU28	PU27	PU26	PU25	PU24	PU23	PU22	PU21	PU20	PU19	PU18	PU17	PU16	PU15	PU14	PU13	PU12	PU11	PU10	PU09	PU08	PU07	PU06	PU05	PU04	PU03	PU02	PU01	PU00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	PU n	Where n = 0 ~ 31 and PU n = PU0 ~ PU31. PU n is used to switch PULL-UP/DOWN of the corresponding PAPUn. 0: HI-Z	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		1: PULL-UP/DOWN Enable	

PORT B GROUP PULL-UP/DOWN enabled State register.

	PBPU																															0x80
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PU31	PU30	PU29	PU28	PU27	PU26	PU25	PU24	PU23	PU22	PU21	PU20	PU19	PU18	PU17	PU16	PU15	PU14	PU13	PU12	PU11	PU10	PU09	PU08	PU07	PU06	PU05	PU04	PU03	PU02	PU01	PU00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0

Bits	Name	Description	R/W
31:0	PU n	Where n = 0 ~ 31 and PU n = PU0 ~ PU31. PU n is used to switch PULL-UP/DOWN of the corresponding PBPUn. 0: HI-Z 1: PULL-UP/DOWN Enable	RW

PORT C GROUP PULL-UP/DOWN enabled State register.

	PCPU																															0x80
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PU31	PU30	PU29	PU28	PU27	PU26	PU25	PU24	PU23	PU22	PU21	PU20	PU19	PU18	PU17	PU16	PU15	PU14	PU13	PU12	PU11	PU10	PU09	PU08	PU07	PU06	PU05	PU04	PU03	PU02	PU01	PU00
RST	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Name	Description	R/W
31:0	PU n	Where n = 0 ~ 31 and PU n = PU0 ~ PU31. PU n is used to switch PULL-UP/DOWN of the corresponding PCPUn. 0: HI-Z 1: PULL-UP/DOWN Enable **Note:** Where n = 0 ~ 2 and PU n = PU24 ~ PU26. The register will be used to switch pull-down for. 0: HI-Z 1: PULL-DOWN Enable	RW

PORT D GROUP PULL-UP/DOWN enabled State register.

	PDPU																															0x80
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PU31	PU30	PU29	PU28	PU27	PU26	PU25	PU24	PU23	PU22	PU21	PU20	PU19	PU18	PU17	PU16	PU15	PU14	PU13	PU12	PU11	PU10	PU09	PU08	PU07	PU06	PU05	PU04	PU03	PU02	PU01	PU00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	R/W
31:0	PU n	Where n = 0 ~ 31 and PU n = PU0 ~ PU31. PU n is used to switch PULL-UP/DOWN of the corresponding PDPUn. 0: HI-Z 1: PULL-UP/DOWN Enable	RW

21.4.2.20 PORT PULL-UP/DOWN State Set Register (PxPUS,0x84)

PORT x GROUP PULL-UP/DOWN state set register7, WRITE-ONLY.

	PxPUS																															0x84
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PUS31	PUS30	PUS29	PUS28	PUS27	PUS26	PUS25	PUS24	PUS23	PUS22	PUS21	PUS20	PUS19	PUS18	PUS17	PUS16	PUS15	PUS14	PUS13	PUS12	PUS11	PUS10	PUS09	PUS08	PUS07	PUS06	PUS05	PUS04	PUS03	PUS02	PUS01	PUS00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	PUS n	Writing 1 to PUS n will set PU n to 1 in register PxPUS. Writing 0 to PUS n will be ignored.	W

21.4.2.21 PORT PULL-UP/DOWN State Clear Register (PxPUC,0x88)

PORT x GROUP PULL-UP/DOWN state clear register, WRITE-ONLY.

	PxPUC																															0x88
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PUC31	PUC30	PUC29	PUC28	PUC27	PUC26	PUC25	PUC24	PUC23	PUC22	PUC21	PUC20	PUC19	PUC18	PUC17	PUC16	PUC15	PUC14	PUC13	PUC12	PUC11	PUC10	PUC09	PUC08	PUC07	PUC06	PUC05	PUC04	PUC03	PUC02	PUC01	PUC00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	PUC n	Writing 1 to PUC n will clear PU n to 1 in register PxPUC. Writing 0 to PUC n will be ignored.	W

21.4.2.22 PORT Z Shadow Register Group

PORT Z group only have eight registers,
PZINTS,PZINTC,PZMSKS,PZMSKC,PZPAT1S,PZPAT1C, PZPAT0S,PZPAT0C. those registers shadow as same as other group registers function which the offset address equal.

	PZINTS																															Base + 0x0014
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	INTS31	INTS30	INTS29	INTS28	INTS27	INTS26	INTS25	INTS24	INTS23	INTS22	INTS21	INTS20	INTS19	INTS18	INTS17	INTS16	INTS15	INTS14	INTS13	INTS12	INTS11	INTS10	INTS09	INTS08	INTS07	INTS06	INTS05	INTS04	INTS03	INTS02	INTS01	INTS00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	PZINTC																															**Base + 0x0018**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	INTC31	INTC30	INTC29	INTC28	INTC27	INTC26	INTC25	INTC24	INTC23	INTC22	INTC21	INTC20	INTC19	INTC18	INTC17	INTC16	INTC15	INTC14	INTC13	INTC12	INTC11	INTC10	INTC09	INTC08	INTC07	INTC06	INTC05	INTC04	INTC03	INTC02	INTC01	INTC00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	PZMSKS																															**Base + 0x0024**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSKS31	MSKS30	MSKS29	MSKS28	MSKS27	MSKS26	MSKS25	MSKS24	MSKS23	MSKS22	MSKS21	MSKS20	MSKS19	MSKS18	MSKS17	MSKS16	MSKS15	MSKS14	MSKS13	MSKS12	MSKS11	MSKS10	MSKS09	MSKS08	MSKS07	MSKS06	MSKS05	MSKS04	MSKS03	MSKS02	MSKS01	MSKS00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	PZMSKC																															**Base + 0x0028**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSKC31	MSKC30	MSKC29	MSKC28	MSKC27	MSKC26	MSKC25	MSKC24	MSKC23	MSKC22	MSKC21	MSKC20	MSKC19	MSKC18	MSKC17	MSKC16	MSKC15	MSKC14	MSKC13	MSKC12	MSKC11	MSKC10	MSKC09	MSKC08	MSKC07	MSKC06	MSKC05	MSKC04	MSKC03	MSKC02	MSKC01	MSKC00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	PZPAT1S																															**Base + 0x0034**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PAT1S31	PAT1S30	PAT1S29	PAT1S28	PAT1S27	PAT1S26	PAT1S25	PAT1S24	PAT1S23	PAT1S22	PAT1S21	PAT1S20	PAT1S19	PAT1S18	PAT1S17	PAT1S16	PAT1S15	PAT1S14	PAT1S13	PAT1S12	PAT1S11	PAT1S10	PAT1S09	PAT1S08	PAT1S07	PAT1S06	PAT1S05	PAT1S04	PAT1S03	PAT1S02	PAT1S01	PAT1S00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	PZPAT1S																															**Base + 0x0038**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	PAT1C31	PAT1C30	PAT1C29	PAT1C28	PAT1C27	PAT1C26	PAT1C25	PAT1C24	PAT1C23	PAT1C22	PAT1C21	PAT1C20	PAT1C19	PAT1C18	PAT1C17	PAT1C16	PAT1C15	PAT1C14	PAT1C13	PAT1C12	PAT1C11	PAT1C10	PAT1C09	PAT1C08	PAT1C07	PAT1C06	PAT1C05	PAT1C04	PAT1C03	PAT1C02	PAT1C01	PAT1C00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	PZPAT0S																															**Base + 0x0044**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PAT0S31	PAT0S30	PAT0S29	PAT0S28	PAT0S27	PAT0S26	PAT0S25	PAT0S24	PAT0S23	PAT0S22	PAT0S21	PAT0S20	PAT0S19	PAT0S18	PAT0S17	PAT0S16	PAT0S15	PAT0S14	PAT0S13	PAT0S12	PAT0S11	PAT0S10	PAT0S09	PAT0S08	PAT0S07	PAT0S06	PAT0S05	PAT0S04	PAT0S03	PAT0S02	PAT0S01	PAT0S00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	PZPAT0C																															**Base + 0x0048**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PAT0C31	PAT0C30	PAT0C29	PAT0C28	PAT0C27	PAT0C26	PAT0C25	PAT0C24	PAT0C23	PAT0C22	PAT0C21	PAT0C20	PAT0C19	PAT0C18	PAT0C17	PAT0C16	PAT0C15	PAT0C14	PAT0C13	PAT0C12	PAT0C11	PAT0C10	PAT0C09	PAT0C08	PAT0C07	PAT0C06	PAT0C05	PAT0C04	PAT0C03	PAT0C02	PAT0C01	PAT0C00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

21.4.2.23 GPIOZ Group ID to Load Register (PzGID2LD,0x00F0)

This register controls which Port Group to be load from GPIOZ.

	PzGID2LD																															**Base + 0x00F0**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																													GPID		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GPIOZ Group can shadow four register groups for GPIO Group A to C, when set or clear A to C register groups below four types, it will through shadow register to implement. the GPIOZ ID used for controls which Group to be manipulate.

Bits	Name	Description	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

31:3	Reserved	Writing has no effect, Read as zero	R
2:0	GPID	GPIO Port ID load control register, according the values of GPID to load Shadow register group to the same offset address of group ID meet the GPID. GPID: Shadow register load to work groups 0: Load to GPIO Port A 1: Load to GPIO Port B 2: Load to GPIO Port C 3: Load to GPIO Port D 4: Undefine 5: Undefine	W

21.5 Program Guide

21.5.1 Port Function Guide

EDG	INT	MASK	PAT1	PAT0	Port Description
0	1	0	0	0	Port is low level triggered interrupt input.
0	1	0	0	1	Port is high level triggered interrupt input.
0	1	0	1	0	Port is fall edge triggered interrupt input.
0	1	0	1	1	Port is rise edge triggered interrupt input.
1	1	0	1	x	Port is dual-edge(both rise and fall edge) triggered interrupt input.
0	1	1	0	0	Port is low level triggered interrupt input. Interrupt is masked. Flag is recorded.
0	1	1	0	1	Port is high level triggered interrupt input. Interrupt is masked. Flag is recorded.
0	1	1	1	0	Port is fall edge triggered interrupt input. Interrupt is masked. Flag is recorded.
0	1	1	1	1	Port is rise edge triggered interrupt input. Interrupt is masked. Flag is recorded.
1	1	1	1	x	Port is dual-edge(both rise and fall edge) triggered interrupt input. Interrupt is masked. Flag is recorded.
x	0	0	0	0	Port is pin of device 0.
x	0	0	0	1	Port is pin of device 1.
x	0	0	1	0	Port is pin of device 2.
x	0	0	1	1	Port is pin of device 3.
x	0	1	0	0	Port is GPIO output 0.
x	0	1	0	1	Port is GPIO output 1.
x	0	1	1	x	Port is GPIO input.

21.5.2 Configure without 3rd-unexpected state

Function switching between devices and gpio is controlled by combination of 4 registers:

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

INT/MASK/PAT1/PAT0. As the four register is accessed by soft ware in serial sequence, which posing a risk that third states occur during configuration.

For example:

current state is:

INT = 0x0, MASK = 0x0, PAT0 = 0x0, PAT1 = 0x0;

target state is:

INT = 0x1, MASK = 0x1, PAT0 = 0x1, PAT1 = 0x1;

If the first step is to configure INT to 0x1, the 3rd state is:

INT = 0x1, MASK = 0x0, PAT0 = 0x0, PAT1 = 0x0;

This might triggers interrupt if port is low level.

To avoid the unexpected 3-state, the four registers must be updated in the same time.

There is an dummy group GPIOZ, which only used in this purpose. The working mechanism is the information of configure can be temporarily stored in the GPIOZ. When assert GPIOZ.LD, all the four registers will load their content into target group at the same time.

Example:

If the Port B current state is:

INT = 0x0, MASK = 0x0, PAT0 = 0x0, PAT1 = 0x0;

It needs to be configured to state:

INT = 0x1, MASK = 0x1, PAT0 = 0x1, PAT1 = 0x1;

There are two steps to finish:

Step1: put the configuration to temporary buffer: GPIOZ

PzINTS = 0x1;

PzMSKS = 0x1;

PzPAT0S = 0x1;

PzPAT1S = 0x1;

alternatively, PzINT, PzMSK, PzPAT0, PzPAT1 are also can be configured straightly.

Step2: configure PzGID2LD to specify which port group to load

PzGID2LD = 0x1; (0x1 stands for GPIO Port B)

21.5.3 Dual-edge Interrupt Configure Guide

When you want to enable the dual-edge trigger interrupt function, follow the settings below:

1.set the bit of PxEDG(x=A~D) register;

2.set the bit of PxINT and PxPAT1 (x=A~D) register;

3.clear the INT flag bit of PxFLG(x=A~D) register;

4.clear the mask bit of PxMSK(x=A~D) register;

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

22 I2C Controller

22.1 Overview

The I2C bus is a two-wire serial interface, consisting of a serial data line (SDA) and a serial clock
(SCL). These wires carry information between the devices connected to the bus. Each device is recognized by a unique address and can operate as either a “transmitter” or “receiver,” depending on the function of the device. Devices can also be considered as masters or slaves when performing data transfers. A master is the device that initializes/terminates a data transfer on the bus and generates clock signals to permit that transfer. During that time, any addressed device is considered as a slave. The I2C controller is software controlled. It behaves as a master or a slave. However, operating as a master and slave simultaneously is not supported.

22.1.1 Features

- Two-wire I2C serial interface – consists of a serial data line (SDA) and a serial clock (SCL)
- Three speeds
  - Standard mode (100 Kb/s)
  - Fast mode (400 Kb/s)
  - High mode (3.4Mb/s)
- Device clock is identical with pclk(APB clock)
- Programmable SCL generator
- Master or slave I2C operation
- 7-bit addressing/10-bit addressing whether configure as Master or Slave
- Transmit General Call or START byte
- level transmit and receive FIFOs
- Interrupt operation
- The number of devices that you can connect to the same I2C-bus is limited only by the maximum bus capacitance of 400pF
- APB interface
- 2 independent I2C channels (I2C0, I2C1)
-

22.1.2 Pin Description

Table 22-1 I2C Pin Description

Name	Width	IO	Description
SDA	1-bit	IO	I2C serial data
SCL	1-bit	IO	I2C serial clock

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Please note that dedicate pull-up resistors must be introduced on board-level. The low-to-high (rise time) transition is highly dependent on RC time constant of the bus.

Totally speaking, for standard-mode I2C-bus system, the pull up resistor depends on following parameters:

- Supply voltage
- Bus capacitance
- Number of connected devices

For fast-mode I2C-bus system, switched pull-up circuit may be essential for strict speed and load requirement. (Please refer NXP Semiconductors, *UM10204: I2C-Bus specification and user manual (Rev.6--4 April 2014)*')

22.2 Registers

22.2.1 Registers Memory Map

A read operation to an address location that contains unused bits results in a 0 value being returned on each of the unused bits.

Registers in I2C controller can be accessed by indicating 24-bit Address Base combined with 8-bit Address Offset.

Table 22-2 Registers Memory Map-Address Base

Name	Addr Base	Description
I2C0	0x10050000	Address base of I2C0
I2C1	0x10051000	Address base of I2C1

Table 22-3 Registers Memory Map-Address Offset

Name	Addr Offset	Description	RW	Reset
I2C_CON	0x00	I2C control	RW	0x7D
I2C_TAR	0x04	I2C target address	RW	0x1055
I2C_SAR	0x08	I2C slave address	RW	0x055
I2C_HS_MADDR	0x0C	I2C HS Master Mode Code Address	RW	0x1
I2C_DC	0x10	I2C data buffer and command	RW	0x000
I2C_SHCNT	0x14	Standard speed I2C SCL high count	RW	0x0190
I2C_SLCNT	0x18	Standard speed I2C SCL low count	RW	0x01D6
I2C_FHCNT	0x1C	Fast speed I2C SCL high count	RW	0x003C
I2C_FLCNT	0x20	Fast speed I2C SCL low count	RW	0x0082
I2C_HHCNT	0x24	High speed I2C SCL high count	RW	0x006
I2C_HLCNT	0x28	High speed I2C SCL low count	RW	0x0010

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

I2C_INTST	0x2C	I2C Interrupt Status	R	0x000
I2C_INTM	0x30	I2C Interrupt Mask	RW	0x8FF
I2C_RINTST	0x34	I2C Raw Interrupt Status	R	0x0
I2C_RXTL	0x38	I2C RxFIFO Threshold	RW	0x1F
I2C_TXTL	0x3C	I2C TxFIFO Threshold	RW	0x20
I2C_CINT	0x40	Clear Interrupts	R	0x0
I2C_CRXUF	0x44	Clear RXUF Interrupt	R	0x0
I2C_CRXOF	0x48	Clear RX_OVER Interrupt	R	0x0
I2C_CTXOF	0x4C	Clear TX_OVER Interrupt	R	0x0
I2C_CRXREQ	0x50	Clear RDREQ Interrupt	R	0x0
I2C_CTXABT	0x54	Clear TX_ABRT Interrupt	R	0x0
I2C_CRXDN	0x58	Clear RX_DONE Interrupt	R	0x0
I2C_CACT	0x5C	Clear ACTIVITY Interrupt	R	0x0
I2C_CSTP	0x60	Clear STOP Interrupt	R	0x0
I2C_CSTT	0x64	Clear START Interrupt	R	0x0
I2C_CGC	0x68	Clear GEN_CALL Interrupt	R	0x0
I2C_ENABLE	0x6C	I2C Enable	RW	0x0
I2C_ST	0x70	I2C Status register	R	0x06
I2C_TXFLR	0x74	TxFIFO Level Register	R	0x0
I2C_RXFLR	0X78	RxFIFO Level Register	R	0x0
I2C_SDAHD	0x7C	I2C SDA Hold time Register	RW	0x55
I2C_ABTSRC	0x80	I2C Transmit Abort Status Register	R	0x0000
I2CSDNACK	0x84	GenerateSLV_DATA_NACK Register	R/W	0x0
I2C_DMACR	0x88	DMA Control Register	R/W	0x0
I2C_DMATDLR	0x8C	DMA Transmit Data Level	R/W	0x0
I2C_DMARDLR	0x90	DMA Receive Data Level	R/W	0x0
I2C_SDASU	0x94	I2C SDA Setup Register	RW	0x64
I2C_ACKGC	0x98	I2C ACK General Call Register	RW	0x1
I2C_ENBST	0x9C	I2C Enable Status Register	R	0x0
I2C_FSPKLEN	0xA0	SS and FS Spike Suppression Limit	RW	0x1

22.2.2 Registers and Fields Description

22.2.2.1 I2C_CON (I2C Control Register)

This register can be written only when I2C is disabled, which corresponds to I2C_ENABLE[0] being set to 0. Writes at other time have on effect.

	I2C_CON																															BASE + 0x00
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

																	Reserved									SLVDIS	RESTART	MATP	SATP	SPEED		MD
RST																	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1

Bits	Name	Description	RW
15:7	Reserved	Writing has no effect, read as zero.	R
6	SLVDIS	This bit controls whether I2C has its slave disabled. 0: slave is enabled 1: slave is disabled Note: Software should ensure that if this bit is written with'0', then bit 0 should also be written with '0'.	RW
5	RESTART	Determines whether RESTART conditions may be sent when acting as a master. Some older slaves do not support handling RESTART conditions. 0: disable 1: enable	RW
4	MATP	This bit is a read-only copy of I2C_TAR.MATP. 0: 7-bit addressing 1: 10-bit addressing	R
3	SATP	When acting as a slave, this bit controls whether the I2C responds to 7-bit or 10-bit addresses. 0: 7-bit addressing 1: 10-bit addressing	RW
2:1	SPEED	These bits control at which speed the I2C operates. 1: standard mode (100 kb/s) 2: fast mode (400 kb/s)(default) 3: high mode (3.4Mb/s) **NOTE:** when these two bits are set to 2'b00 ,the speed mode will be automatically set to 2'b10 i.e. fast mode.	RW
0	MD	This bit controls whether the I2C master is enabled. 0: master disabled 1: master enabled Note: Software should ensure that if this bit is written with'1', then bit 6 should also be written with '1'.	RW

22.2.2.2 I2C_TAR (I2C Target Address Register)

	I2C_TAR																BASE + 0x04															
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

																	Reserved			MATP	SPECIAL	GC_OR_START	I2CTAR									
RST																	0	0	0	1	0	0	0	0	0	1	0	1	0	1	0	1

Bits	Name	Description	R/W
15:13	Reserved	Writing has no effect, read as zero.	R
12	MATP	This bit controls whether the I2C starts its transfers in 7- or 10-bit addressing mode when acting as a master. 0: 7-bit addressing 1: 10-bit addressing **NOTE:** this bit is initially set to 0.	RW
11	SPECIAL	This bit indicates whether software performs a General Call or START BYTE command. 0: ignore the bit of GC_OR_START and use I2CTAR normally 1: perform special I2C command as specified in GC_OR_START bit **NOTE:** this bit is initially set to 0	RW
10	GC_OR_START	If bit 11 (SPECIAL) is set to 1, then this bit indicates whether a General Call or START byte command is to be performed by the I2C. 0: General Call Address – after issuing a General Call, only writes may be performed. Attempting to issue a read command results in setting bit 6 (TX_ABRT) of the I2C_INTST register. The I2C remains in General Call mode until the SPECIAL bit value (bit 11) is cleared 1: START BYTE	RW
9:0	I2CTAR	This is the target address for any master transaction. When transmitting a General Call, these bits are ignored. To generate a START BYTE, the CPU needs to write only once into these bits. If the I2C_TAR and I2C_SAR are the same, loopback exists but the FIFOs are shared between master and slave, so full loopback is not feasible. Only one direction loopback mode is supported (simplex), not duplex. A master cannot transmit to itself, but only to a slave.	RW

NOTE:

(1).It is not necessary to perform any write to this register if I2C is enabled as an I2C slave only.

(2).The meaning of "START byte" in bit 10 is different with the I2C "start condition". "START byte" can only be applied when a device does not have such an interface, it must constantly monitor the bus via software. For more detail information, please refer *UM10204: I2C-Bus specification and user manual (Rev.6--4 April 2014),* '3.1.15 START byte' section. "start condition" means A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. please refer *UM10204: I2C-Bus specification and user manual (Rev.6--4*

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

April 2014), '3.1.4 START and STOP' section for more information.

22.2.2.3 I2C_SAR (I2C Slave Address Register)

	I2C_SAR																														BASE + 0x08
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																	Reserved						I2CSAR									
RST																	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1

Bits	Name	Description	R/W
15:10	Reserved	Writing has no effect, read as zero.	R
9:0	I2CSAR	The I2CSAR holds the slave address when the I2C is operating as a slave. For 7-bit addressing, only I2CSAR[6:0] is used. This register can be written only when the I2C interface is disabled. Writes at other times have no effect.	RW

NOTE: It is not necessary to perform any write to this register if I2C is enabled as an I2C master only.

22.2.2.4 I2C_HS_MADDR (I2C High Speed Master Mode Code Address Register)

This register can be written only when the I2C interface is disabled, which corresponds to I2C_ENABLE[0] being set to 0. Writes at other times have no effect.

	I2C_HS_MAR																														BASE + 0x0C
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																	Reserved													HSMAR		
RST																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Name	Description	R/W
15:3	Reserved	Writing has no effect, read as zero.	R
2:0	HSMAR	The HSMAR holds the value of the I2C HS mode master code. HS-mode master codes are reserved 8-bit codes (00001xxx) that are not used for slave addressing or other purposes. Each master has its unique master code; up to eight high speed mode masters can be present on the same I2C bus system. Valid values are from 0 to 7. This register goes away and becomes read-only returning 0's if the	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		I2C_MAX_SPEED_MODE configuration parameter is set to either Standard or Fast.	

NOTE:

It is not necessary to perform any write to this register if DW_apb_i2c is enabled as an I2C slave only.

22.2.2.5 I2C_DC (I2C Rx/Tx Data Buffer and Command Register)

This is the register the CPU writes to when filling the TX FIFO and the CPU reads from when retrieving bytes from RX FIFO.

	I2C_DC																															BASE + 0x10
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																	Reserved					RESTART	STOP	CMD	DAT							
RST																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
15:11	Reserved	Writing has no effect, read as zero.	R
10	RESTART	This bit controls whether a RESTART is issued before the byte is sent or received. 1: If I2C_CON.RESTART is 1, a RESTART is issued before the byte is sent or received, regardless of whether or not the transfer direction is changing from the previous command; if I2C_CON.RESTART is 0, a STOP followed by a START is issued instead. 0: If I2C_CON.RESTART is 1, a RESTERT is issued if the transfer direction is changing from the previous command, if I2C_CON.RESTART is 0, a STOP followed by a START is issued instead.	W
9	STOP	This bit controls whether a STOP is issued after the byte is sent or received. 1: STOP is issued after the byte, regardless of whether or not the Tx FIFO is empty. If the Tx FIFO is not empty, the master immediately tries to start a new transfer by issuing a START and arbitrating for the bus. 0: STOP is not issued after the byte, regardless of whether or not the Tx FIFO is empty. If the Tx FIFO is not empty, the master continues the current transfer by sending/receiving data bytes according to the value of the CMD bit. If the Tx FIFO is empty, the master holds the SCL line low and stalls the bus until a new command is available in the Tx FIFO.	W
8	CMD	This bit controls whether a read or a write is performed. This bit does not control the direction when the I2C acts as a slave. It controls only the direction when it acts as a master.	W

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		1: Read 0: Write When programming this bit, you should remember the following: attempting to perform a read operation after a General Call command has been sent results in a *TX_ABRT* interrupt (bit 6 of the *I2C_RAW_INTR_STAT* register), unless bit 11 (*SPECIAL*) in the *I2C_TAR* register has been cleared. If a "1" is written to this bit after receiving a *RD_REQ* interrupt, then a *TX_ABRT* interrupt occurs.	
7:0	DAT	This register contains the data to be transmitted or received on the I2C bus. If you are writing to this register and want to perform a read, bits 7:0 (*DAT*) are ignored by the I2C module. However, when you read this register, these bits return the value of data received on the I2C interface.	RW

NOTE: [1].this command only transfer 8-bit data combined with 1-bit CMD, extra bits on the bus will be eliminated. i.e. only 8-0 bits on the bus are accepted by I2C controller.

[2].For the detail information about what condition could generate START, STOP and RESTART, please refer 22.3.6.

[3].The differences between *I2C_ENABLE[5]*(RESTART) and *I2C_DC[10]*(RESTART) is that I2C_ENABLE[5] determine whether or not I2C the capability of generating repeat start, but not transmit RESTART when this bit be setted. If this bit set "1", I2C_DC[10] controls whether a RESTART is issued, if set "0", I2C_DC[10] have no meaning.

22.2.2.6 I2C_SHCNT (I2C Standard Speed SCL High Count Register)

	I2C_SHCNT																BASE + 0x14															
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																	I2CSHCNT															
RST																	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0

Bits	Name	Description	R/W
15:0	I2CSHCNT	This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. The register sets the SCL clock high-period count for standard speed. This register can be written only when the I2C interface is disabled which corresponds to I2C_ENABLE[0] being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		being written, and if attempted results in 6 being set.	

22.2.2.7 I2C_SLCNT (I2C Standard Speed SCL Low Count Register)

	I2C_SLCNT																															BASE + 0x18
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																	I2CSLCNT															
RST																	0	0	0	0	0	0	0	1	1	1	0	1	0	1	1	0

Bits	Name	Description	R/W
15:0	I2CSLCNT	This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for standard speed. This register can be written only when the I2C interface is disabled which corresponds to I2C_ENABLE[0] being set to 0. Writes at other times have no effect. The minimum valid value is 8; hardware prevents values less than this being written, and if attempted, results in 8 being set.	RW

22.2.2.8 I2C_FHCNT (I2C Fast Speed SCL High Count Register)

	I2C_FHCNT																															BASE + 0x1C
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																	I2CFHCNT															
RST																	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0

Bits	Name	Description	R/W
15:0	I2CFHCNT	This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for fast speed. This register can be written only when the I2C interface is disabled which corresponds to I2C_ENABLE[0] being set to 0. Writes at other times have no effect. Minimum value allowed for the I2CSHCNT registers is 6. If the set value was less than 6, it will be automatically set to 6.	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

22.2.2.9 I2C_FLCNT (I2C Fast Speed SCL Low Count Register)

	I2C_FLCNT																BASE + 0x20															
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																	I2CFLCNT															
RST																	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0

Bits	Name	Description	R/W
15:0	I2CFLCNT	This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for fast speed. This register can be written only when the I2C interface is disabled which corresponds to I2C_ENABLE[0] being set to 0. Writes at other times have no effect. Minimum value that can be programmed in the I2CSLCNT registers is 8. If the set value was less than 8, it will be automatically set to 8	RW

22.2.2.10 I2C_HHCNT (I2C High Speed SCL High Count Register)

	I2C_HHCNT																BASE + 0x24															
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																	I2CHHCNT															
RST																	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

Bits	Name	Description	R/W
15:0	I2CHHCNT	This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for high speed. This register can be written only when the I2C interface is disabled which corresponds to I2C_ENABLE[0] being set to 0. Writes at other times have no effect. Minimum value allowed for the I2CSHCNT registers is 6. If the set value was less than 6, it will be automatically set to 6.	RW

22.2.2.11 I2C_HLCNT (I2C High Speed SCL Low Count Register)

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	I2C_HLCNT																BASE + 0x28															
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																	I2CHLCNT															
RST																	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Name	Description	R/W
15:0	I2CHLCNT	This register must be set before any I2C bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for high speed. This register can be written only when the I2C interface is disabled which corresponds to I2C_ENABLE[0] being set to 0. Writes at other times have no effect. Minimum value that can be programmed in the I2CSLCNT registers is 8. If the set value was less than 8, it will be automatically set to 8	RW

22.2.2.12 I2C_INTST (I2C Interrupt Status Register)

Each bit in this register has a corresponding mask bit in the I2CINTM register. These bits are cleared by reading the matching interrupt clear register. The unmasked raw versions of these bits are available in the *I2C_RAW_INTR_STAT* register

	I2C_INTST																BASE + 0x2C															
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																	Reserved				IGC	ISTT	ISTP	IACT	RXDN	TXABT	RDREQ	TXEMP	TXOF	RXFL	RXOF	RXUF
RST																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
15:12	Reserved	Writing has no effect, read as zero.	R
11	IGC	Set only when a General Call address is received and it is acknowledged. It stays set until it is cleared either by disabling I2C or when the CPU reads bit 0 of the *I2C_CGC* register. I2C stores the received data in the Rx buffer.	R
10	ISTT	Indicates whether a START or RESTART condition has occurred on the I2C interface regardless of whether I2C is operating in slave or master mode.	R
9	ISTP	Indicates whether a STOP condition has occurred on the I2C interface regardless of whether I2C is operating in slave or master mode.	R
8	IACT	This bit captures I2C activity and stays set until it is cleared. There are	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		four ways to clear it: 1 Disabling the I2C 2 Reading the I2C_CACT register 3 Reading the I2C_CINT register 4 System reset Once this bit is set, it stays set unless one of the four methods is used to clear it. Even if the I2C module is idle, this bit remains set until cleared, indicating that there was activity on the bus.	
7	RXDN	When the I2C is acting as a slave-transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte. This occurs on the last byte of the transmission, indicating that the transmission is done.	R
6	TXABT	This bit indicates if I2C, as an I2C transmitter, is unable to complete the intended actions on the contents of the transmit FIFO. This situation can occur both as an I2C master or an I2C slave, and is referred to as a “transmit abort”. When this bit is set to 1, the I2C_ABTSRC register indicates the reason why the transmit abort takes places. **NOTE:** The I2C flushes/resets/empties the TX FIFO whenever this bit is set. The TX FIFO remains in this flushed state until the register I2C_CTXABT is read. Once this read is performed, the TX FIFO is then ready to accept more data bytes from the APB interface.	R
5	RDREQ	This bit is set to 1 when I2C is acting as a slave and another I2C master is attempting to read data from I2C. The I2C holds the I2C bus in a wait state (SCL=0) until this interrupt is serviced, which means that the slave has been addressed by a remote master that is asking for data to be transferred. The processor must respond to this interrupt and then write the requested data to the I2C_DC register. This bit is set to 0 just after the processor reads the I2C_CRREQ register.	R
4	TXEMP	This bit is set to 1 when the transmit buffer is at or below the threshold value set in the I2C_TXTL register. It is automatically cleared by hardware when the buffer level goes above the threshold. When the I2C_ENB bit 0 is 0, the TX FIFO is flushed and held in reset. There the TX FIFO looks like it has no data within it, so this bit is set to 1, provided there is activity in the master or slave state machines. When there is no longer activity, then with I2C_ENB[0]=0.	R
3	TXOF	Set during transmit if the transmit buffer is filled to I2C_TX_BUFFER_DEPTH and the processor attempts to issue another I2C command by writing to the I2C_DC register. When the module is disabled, this bit keeps its level until the master or slave state machines go into idle, and when I2C_ENB[0]=0, this interrupt is cleared.	R
2	RXFL	Set when the receive buffer reaches or goes above the I2C_RXTL threshold in the I2C_RXTL register. It is automatically cleared by hardware when buffer level goes below the threshold.	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		If the module is disabled (I2C_ENB[0]=0), the RX FIFO is flushed and held in reset; therefore the RX FIFO is not full. So this bit is cleared once the I2C_ENB bit 0 is set to 0, regardless of the activity that continues.	
1	RXOF	Set if the receive buffer is completely filled to 64 and an additional byte is received from an external I2C device. The I2C acknowledges this, but any data bytes received after the FIFO is full are lost. If the module is disabled (I2C_ENB[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when I2C_ENB[0]=0, this interrupt is cleared.	R
0	RXUF	Set if the processor attempts to read the receive buffer when it is empty by reading from the I2C_DC register. If the module is disabled (I2C_ENB[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when I2C_ENB[0]=0, this interrupt is cleared.	R

NOTE: 22.3.5 summary all the condition could flush TX FIFO.

22.2.2.13 I2C_INTM (I2C Interrupt Mask Register)

These bits mask their corresponding interrupt status bits. This register is active low; a value of 0 masks the interrupt, whereas a value of 1 unmasks the interrupt.

	I2C_INTM																															BASE + 0x30
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																	Reserved				MIGC	MISTT	MISTP	MIACT	MRXDN	MTXABT	MRDREQ	MTXEMP	MTXOF	MRXFL	MRXOF	MRXUF
RST																	0	0	0	0	1	0	0	0	1	1	1	1	1	1	1	1

Bits	Name	Description	R/W
15:12	Reserved	Writing has no effect, read as zero.	R
11	MIGC	These bits mask their corresponding interrupt status bits in the I2CINTST register.	RW
10	MISTT		RW
9	MISTP		RW
8	MIACT		RW
7	MRXDN		RW
6	MTXABT		RW
5	MRDREQ		RW
4	MTXEMP		RW
3	MTXOF		RW
2	MRXFL		RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

1	MRXOF		RW
0	MRXUF		RW

22.2.2.14 I2C_RAW_INTR_STAT

Unlike the *I2C_INTST* register, these bits are not masked so they always show the true status of the I2C. See *I2C_INTST* for a detailed description of these bits. All bits are only read.

	I2C_RAW_INTM_STAT																BASE + 0x34															
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																	Reserved				IGC	ISTT	ISTP	IACT	RXDN	TXABT	RDREQ	TXEMP	TXOF	RXFL	RXOF	RXUF
RST																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
15:12	Reserved	Writing has no effect, read as zero.	R
11	GEN_CALL	Set only when a General Call address is received and it is acknowledged. It stays set until it is cleared either by disabling I2C or when the CPU reads bit 0 of the I2C_CLR_GEN_CALL register. I2C stores the received data in the Rx buffer.	R
10	START_DET	Indicates whether a START or RESTART condition has occurred on the I2C interface regardless of whether I2C is operating in slave or master mode.	R
9	STOP_DET	Indicates whether a STOP condition has occurred on the I2C interface regardless of whether I2C is operating in slave or master mode.	R
8	ACTIVITY	This bit captures I2C activity and stays set until it is cleared. There are four ways to clear it: ■ Disabling the I2C ■ Reading the I2C_CLR_ACTIVITY register ■ Reading the I2C_CLR_INTR register ■ System reset Once this bit is set, it stays set unless one of the four methods is used to clear it. Even if the I2C module is idle, this bit remains set until cleared, indicating that there was activity on the bus.	R
7	RX_DONE	When the I2C is acting as a slave-transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte. This occurs on the last byte of the transmission, indicating that the transmission is done.	R
6	TX_ABRT	This bit indicates if I2C, as a I2C transmitter, is unable to complete the intended actions on the contents of the transmit FIFO. This situation can occur both as a I2C master or a I2C slave, and is	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		referred to as a “transmit abort”. When this bit is set to 1, the I2C_TX_ABRT_SOURCE register indicates the reason why the transmit abort takes places. **NOTE:** The I2C flushes/resets/empties the TX FIFO whenever this bit is set. The TX FIFO remains in this flushed state until the register I2C_CLR_TX_ABRT is read. Once this read is performed, the TX FIFO is then ready to accept more data bytes from the APB interface.	
5	RD_REQ	This bit is set to 1 when I2C is acting as a slave and another I2C master is attempting to read data from I2C. The I2C holds the I2C bus in a wait state (SCL=0) until this interrupt is serviced, which means that the slave has been addressed by a remote master that is asking for data to be transferred. The processor must respond to this interrupt and then write the requested data to the I2C_DATA_CMD register. This bit is set to 0 just after the processor reads the I2C_CLR_RD_REQ register.	R
4	TX_EMPTY	This bit is set to 1 when the transmit buffer is at or below the threshold value set in the I2C_TX_TL register. It is automatically cleared by hardware when the buffer level goes above the threshold. When I2C_ENABLE[0] is set to 0, the TX FIFO is flushed and held in reset. There the TX FIFO looks like it has no data within it, so this bit is set to 1, provided there is activity in the master or slave state machines. When there is no longer activity, then with I2C_en=0, this bit is set to 0.	R
3	TX_OVER	Set during transmit if the transmit buffer is filled to I2C_TX_BUFFER_DEPTH and the processor attempts to issue another I2C command by writing to the I2C_DATA_CMD register. When the module is disabled, this bit keeps its level until the master or slave state machines go into idle, and when I2C_en goes to 0, this interrupt is cleared.	R
2	RX_FULL	Set when the receive buffer reaches or goes above the RX_TL threshold in the I2C_RX_TL register. It is automatically cleared by hardware when buffer level goes below the threshold. If the module is disabled (I2C_ENABLE[0]=0), the RX FIFO is flushed and held in reset; therefore the RX FIFO is not full. So this bit is cleared once I2C_ENABLE[0] is set to 0, regardless of the activity that continues.	R
1	RX_OVER	Set if the receive buffer is completely filled to I2C_RX_BUFFER_DEPTH and an additional byte is received from an external I2C device. The I2C acknowledges this, but any data bytes received after the FIFO is full are lost. If the module is disabled (I2C_ENABLE[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when I2C`_en goes to 0, this interrupt is cleared.	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

0	RX_UNDER	Set if the processor attempts to read the receive buffer when it is empty by reading from the I2C_DATA_CMD register. If the module is disabled (I2C_ENABLE[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when I2C_en goes to 0, this interrupt is cleared.	R

22.2.2.15 I2C_RXTL (I2C Receive FIFO Threshold Register)

	I2C_RXTL																														BASE + 0x38
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																	Reserved										RXTL					
RST																	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1

Bits	Name	Description	R/W
15:6	Reserved	Writing has no effect, read as zero.	R
5:0	RXTL	Receive FIFO Threshold Level. Controls the level of entries that triggers the RxFIFO full interrupt. A value of n sets the threshold for (n+1) entries. For example, a value of 0 sets the threshold for 1 entry, and a value of 255 sets the threshold for 256 entries.	RW

22.2.2.16 I2C_TXTL (I2C Transmit FIFO Threshold Register)

	I2C_TXTL																														BASE + 0x3C
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																	Reserved										TXTL					
RST																	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Name	Description	R/W
15:6	Reserved	Writing has no effect, read as zero.	R
5:0	TXTL	Transmit FIFO Threshold Level. Controls the level of entries that trigger the TxFIFO empty interrupt. A value of n sets the threshold for n entries. For example, A value of 0 sets the threshold for 0 entries, and a value of 255 sets the threshold for 255 entries.	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

22.2.2.17 I2C_CINT (I2C Clear Combined and Individual Interrupt Register)

	I2C_CINT																															BASE + 0x40
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																	Reserved															CINT
RST																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
15:1	Reserved	Writing has no effect, read as zero.	R
0	CINT	Read this register to clear the combined interrupt, all individual interrupts, and the I2C_ABTSRC register. This bit does not clear hardware clearable interrupts but software clearable interrupts. Refer to Bit 9 of the I2C_ABTSRC register for an exception to clearing I2C_ABTSRC.	R

22.2.2.18 I2C_CRXUF (I2C Clear RXUF Interrupt Register)

	I2C_CRXUF																															BASE + 0x44
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																	Reserved															CRXUF
RST																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
15:1	Reserved	Writing has no effect, read as zero.	R
0	CRXUF	Read this register to clear the RXUF interrupt (bit 0) of the I2C_INTST register.	R

22.2.2.19 I2C_CRXOF (I2C Clear RXOF Interrupt Register)

	I2C_CRXOF																															BASE + 0x48
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

																	Reserved															CRXOF
RST																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
15:1	Reserved	Writing has no effect, read as zero.	R
0	CRXOF	Read this register to clear the RXOF interrupt (bit 1) of the I2CINTST register.	R

22.2.2.20 I2C_CTXOF (I2C Clear TX_OVER Interrupt Register)

	I2C_CTXOF																BASE + 0x4C															
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																	Reserved															CTXOF
RST																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
15:1	Reserved	Writing has no effect, read as zero.	R
0	CTXOF	Read this register to clear the TX_OVER interrupt (bit 3) of the I2CINTST register.	R

22.2.2.21 I2C_CRXREQ (I2C Clear RDREQ Interrupt Register)

	I2C_CRXREQ																BASE + 0x50															
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																	Reserved															CLRDREQ
RST																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
15:1	Reserved	Writing has no effect, read as zero.	R
0	CLRDREQ	Read this register to clear the RDREQ interrupt (bit 5) of the I2CINTST register.	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

22.2.2.22 I2C_CTXABT (I2C Clear TX_ABRT Interrupt Register)

	I2C_CTXABT																BASE + 0x54															
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															CTXABT
RST																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
15:1	Reserved	Writing has no effect, read as zero.	R
0	CTXABT	Read this register to clear the TX_ABRT interrupt (bit 6) of the I2C_INTST register, and the I2C_ABTSRC register. This also releases the TX FIFO from the flushed/reset state, allowing more writes to the TX FIFO. Refer to Bit 9 of the I2C_ABTSRC register for an exception to clearing I2C_ABTSRC.	R

22.2.2.23 I2C_CRXDN (I2C Clear RX_DONE Interrupt Register)

	I2C_CRXDN																BASE + 0x58															
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															CRXDN
RST																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
15:1	Reserved	Writing has no effect, read as zero.	R
0	CRXDN	Read this register to clear the RX_DONE interrupt (bit 7) of the I2C_INTST register.	R

22.2.2.24 I2C_CACT (I2C Clear ACTIVITY Interrupt Register)

	I2C_CACT																BASE + 0x5C															
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															CACT

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

RST																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
15:1	Reserved	Writing has no effect, read as zero.	R
0	CACT	Reading this register clears the ACTIVITY interrupt if the I2C is not active anymore. If the I2C module is still active on the bus, the ACTIVITY interrupt bit continues to be set. It is automatically cleared by hardware if the module is disabled and if there is no further activity on the bus. The value read from this register to get status of the ACTIVITY interrupt (bit 8) of the I2CINTST register.	R

22.2.2.25 I2C_CSTP (I2C Clear STOP Interrupt Register)

	I2C_CSTP																															**BASE + 0x60**
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																	Reserved															CSTP
RST																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
15:1	Reserved	Writing has no effect, read as zero.	R
0	CSTP	Read this register to clear the STOP interrupt (bit 9) of the I2CINTST register.	R

22.2.2.26 I2C_CSTT (I2C Clear START Interrupt Register)

	I2C_CSTT																															**BASE + 0x64**
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																	Reserved															CSTT
RST																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
15:1	Reserved	Writing has no effect, read as zero.	R
0	CSTT	Read this register to clear the START interrupt (bit 10) of the I2CINTST register.	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

22.2.2.27 I2C_CGC (I2C Clear GEN_CALL Interrupt Register)

	I2C_CGC																															BASE + 0x68
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																	Reserved															CGC
RST																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
15:1	Reserved	Writing has no effect, read as zero.	R
0	CGC	Read this register to clear the GEN_CALL interrupt (bit 11) of I2CINTST register.	R

22.2.2.28 I2C_ENABLE (I2C Enable Register)

	I2C_ENABLE																															BASE + 0x6C
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																	Reserved														ABORT	I2CENB
RST																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
15:2	Reserved	Writing has no effect, read as zero.	R
1	ABORT	When set, the controller initiates the transfer abort. 0: ABORT not initiated or ABORT done 1: ABORT operation in progress The software can abort the I2C transfer in master mode by setting this bit. The software can set this bit only when ENABLE is already set; otherwise, the controller ignores any write to ABORT bit. The software cannot clear the ABORT bit once set. In response to an ABORT, the controller issues a STOP and flushes the Tx FIFO after completing the current transfer, then sets the TX_ABORT interrupt after the abort operation. The ABORT bit is cleared automatically after the abort operation.	R/W
0	I2CENB	Controls whether the I2C is enabled. 0: Disables I2C (TX and RX FIFOs are held in an erased state) 1: Enables I2C Software can disable I2C while it is active. However, it is important that	R/W

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		care be taken to ensure that I2C is disabled properly. When I2C is disabled, the following occurs: – The TX FIFO and RX FIFO get flushed. – Status bits in the I2C_INTST register are still active until I2C goes into IDLE state. If the module is transmitting, it stops as well as deletes the contents of the transmit buffer after the current transfer is complete. If the module is receiving, the I2C stops the current transfer at the end of the current byte and does not acknowledge the transfer.	

22.2.2.29 I2C_ST(I2C Status Register)

This is a read-only register used to indicate the current transfer status and FIFO status. The status register may be read at any time. None of the bits in this register request an interrupt.

When the I2C is disabled by writing 0 in bit 0 of the I2C_ENABLE register:

- Bits 1 and 2 are set to 1
- Bits 3 and 4 are set to 0

When the master or slave state machine goes to idle and I2C_ENABLE[0]=0:

- Bits 5 and 6 are set to 0

	I2C_ST																BASE + 0x70															
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																	Reserved									SLVACT	MSTACT	RFF	RFNE	TFE	TFNF	ACT
RST																	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

Bits	Name	Description	R/W
15:7	Reserved	Writing has no effect, read as zero.	R
6	SLVACT	Slave FSM Activity Status. 0: Slave FSM is in IDLE state so the Slave part of I2C is not Active 1: Slave FSM is not in IDLE state so the Slave part of I2C is Active	R
5	MSTACT	Master FSM Activity Status. 0: Master FSM is in IDLE state so the Master part of I2C is not Active 1: Master FSM is not in IDLE state so the Master part of I2C is Active	R
4	RFF	Receive FIFO Completely Full. When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared. 0: Receive FIFO is not full 1: Receive FIFO is full	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

3	RFNE	Receive FIFO Not Empty. This bit is set when the receive FIFO contains one or more entries; it is cleared when the receive FIFO is empty. 0: Receive FIFO is empty 1: Receive FIFO is not empty	R
2	TFE	Transmit FIFO Completely Empty. When the transmit FIFO is completely empty, this bit is set. When it contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt. 0: Transmit FIFO is not empty 1: Transmit FIFO is empty	R
1	TFNF	Transmit FIFO Not Full. Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full. 0: Transmit FIFO is full 1: Transmit FIFO is not full	R
0	ACT	I2C Activity Status. The OR of SLVACT and MSTACT bits.	R

22.2.2.30 I2C_TXFLR(I2C Transmit FIFO Level Register)

This register contains the number of valid data entries in the transmit FIFO buffer. It is cleared whenever:

- The I2C is disabled
- There is a transmit abort—that is, TX_ABRT bit is set in the I2C_RAW_INTR_STAT register
- The slave bulk transmit mode is aborted

The register increments whenever data is placed into the transmit FIFO and decrements when data is taken from the transmit FIFO.

																																BASE+0X74					
Bit																																5	4	3	2	1	0
	Reserved																															TXFLR					
RST																																0	0	0	0	0	0

Bits	Name	Description	R/W
31:6	Reserved	Reserved.	N/A
5:0	TXFLR	Contains the number of valid data entries in the transmit FIFO	R

22.2.2.31 I2C_RXFLR(I2C Receive FIFO Level Register)

This register contains the number of valid data entries in the receive FIFO buffer. It is cleared whenever:

- The I2C is disabled

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

– Whenever there is a transmit abort caused by any of the events tracked in I2C_ABTSRC

The register increments whenever data is placed into the receive FIFO and decrements when data is taken from the receive FIFO.

																														BASE+0X78					
Bit																														5	4	3	2	1	0
	Reserved																													RXFLR					
RST																														0	0	0	0	0	0

Bits	Name	Description	R/W
31:6	Reserved	Reserved.	N/A
5:0	RXFLR	Contains the number of valid data entries in the receive FIFO	R

22.2.2.32 I2C_SDAHD (I2C SDA Hold Time Register)

This register controls the amount of hold time on the SDA signal after a negative edge of SCL in both master and slave mode, in units of APB clock period. The value programmed must be greater than the minimum hold time in each mode for the value to be implemented—one cycle in master mode, seven cycles in slave mode. Writes to this register succeed only when I2C_ENABLE[0]=0.

The programmed SDA hold time cannot exceed at any time the duration of the low part of scl. Therefore the programmed value cannot be larger than N_SCL_LOW-2, where N_SCL_LOW is the duration of the low part of the scl period measured in APB clock cycles.

	I2C_SDAHD																																	BASE + 0x7C	
Bit																		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																	SDAHD																	
RST																		0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1

Bits	Name	Description	R/W
31:16	Reserved	Reserved.	N/A
15:0	SDAHD	I2C Hold Time. Sets the required SDA hold time in units of APB clock period.	RW

22.2.2.33 I2C_ABTSRC (I2C Transmit Abort Source Register)

This register has 32 bits that indicate the source of the TX_ABRT bit. Except for Bit 9, this

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

register is cleared whenever the I2CCTXABT register or the I2CCINT register is read. To clear Bit 9, the source of the SBYTE_NORSTRT must be fixed first; RESTART must be enabled (I2C_CON[5]=1), the SPECIAL bit must be cleared (I2C_TAR[11]), or the GC_OR_START bit must be cleared (I2C_TAR[10]). Once the source of the SBYTE_NORSTRT is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the SBYTE_NORSTRT is not fixed before attempting to clear this bit, Bit 9 clears for one cycle and is then re-asserted.

	I2C_ABTSRC																															**BASE + 0x80**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TX_FLUSH_CNT								Reserved							USER_ABRT	SLVRD_INTX	SLV_ARBLOST	SLVFLUSH_TXFIFO	ARB_LOST	ABRT_MASTER_DIS	ABRT_10B_RD_NORSTRT	SBYTE_NORSTRT	ABRT_HS_NORSTRT	SBYTE_ACKDET	ABRT_HS_ACKDET	ABRT_GCALL_READ	ABRT_GCALL_NOCK	ABRT_TXDATA_NOACK	ABRT_10ADDR2_NOACK	ABRT_10ADDR1_NOACK	ABRT_7B_ADDR_NOACK
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:24	TX_FLUSH_CNT	This field preserves the TXFLR value prior to the last TX_ABRT event. It is cleared whenever I2C is disabled.	R
23:17	Reserved	Read as zero.	
16	USER_ABRT	This is a master-mode-only bit. Master has detected the transfer abort	R
15	SLVRD_INTX	1: When the processor side responds to a slave mode request for data to be transmitted to a remote master and user writes a 1 in CMD (bit 8) of I2C_DC register.	R
14	SLV_ARBLOST	1: Slave lost the bus while transmitting data to a remote master. I2C_ABTSRC[12] is set at the same time. **NOTE:** Even though the slave never “owns” the bus, something could go wrong on the bus. This is a fail safe check. For instance, during a data transmission at the low-to-high transition of SCL, if what is on the data bus is not what is supposed to be transmitted, then I2C no longer own the bus. Reset value: 0x0.	R
13	SLVFLUSH_TXFIFO	1: Slave has received a read command and some data exists in the TX FIFO so the slave issues a TX_ABRT interrupt to flush old data in TX FIFO. Reset value: 0x0.	R
12	ARB_LOST	1: Master has lost arbitration, or if I2C_ABTSRC[14] is also set,	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		then the slave transmitter has lost arbitration. **NOTE:** I2C can be both master and slave at the same time. Reset value: 0x0.	
11	ABRT_MASTER_DIS	1: User tries to initiate a Master operation with the Master mode disabled. Reset value: 0x0.	R
10	ABRT_10B_RD_NORSTRT	1: The restart is disabled (RESTART bit (I2C_CON[5]) = 0) and the master sends a read command in 10-bit addressing mode. Reset value: 0x0.	R
9	SBYTE_NORSTRT	To clear Bit 9, the source of the SBYTE_NORSTRT must be fixed first; restart must be enabled (I2C_CON[5]=1), the SPECIAL bit must be cleared (I2C_TAR[11]), or the GC_OR_START bit must be cleared (I2C_TAR[10]). Once the source of the SBYTE_NORSTRT is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the SBYTE_NORSTRT is not fixed before attempting to clear this bit, bit 9 clears for one cycle and then gets re-asserted. 1: The restart is disabled (RESTART bit (I2C_CON[5]) = 0) and the user is trying to send a START Byte. Reset value: 0x0.	R
8	ABRT_HS_NORSTRT	1: The restart is disabled (RESTART bit (I2C_CON[5]) = 0) and the user is trying to use the master to transfer data in High Speed mode. Reset value: 0x0.	R
7	SBYTE_ACKDET	1: Master has sent a START Byte and the START Byte was acknowledged (wrong behavior). Reset value: 0x0.	R
6	ABRT_HS_ACKDET	1: Master is in High Speed mode and the High Speed Master code was acknowledged (wrong behavior). Reset value: 0x0.	R
5	ABRT_GCALL_READ	1: I2C in master mode sent a General Call but the user programmed the byte following the General Call to be a read from the bus (I2CDC[9] is set to 1). Reset value: 0x0.	R
4	ABRT_GCALL_NOACK	1: I2C in master mode sent a General Call and no slave on the bus acknowledged the General Call. Reset value: 0x0.	R
3	ABRT_TXDATA_NOACK	1: This is a master-mode only bit. Master has received an acknowledgement for the address, but when it sent data byte(s)	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		following the address, it did not receive an acknowledgement from the remote slave(s). Reset value: 0x0.	
2	ABRT_10ADDR2_NOACK	1: Master is in 10-bit address mode and the second address byte of the 10-bit address was not acknowledged by any slave. Reset value: 0x0.	R
1	ABRT_10ADDR1_NOACK	1: Master is in 10-bit address mode and the first 10-bit address byte was not acknowledged by any slave. Reset value: 0x0.	R
0	ABRT_7B_ADDR_NOACK	1: Master is in 7-bit addressing mode and the address sent was not acknowledged by any slave. Reset value: 0x0.	R

22.2.2.34 I2C_SLV_DATA_NACK_ONLY (I2C Generate Slave Data NACK Register)

The register is used to generate a NACK for the data part of a transfer when I2C is acting as a slave-receiver. This register only exists when the I2C_SLV_DATA_NACK_ONLY parameter is set to 1. When this parameter disabled, this register does not exist and writing to the register's address has no effect.

A write can occur on this register if either of the following conditions are met:

- DW_apb_i2c is disabled (I2C_ENABLE[0] = 0)
- Slave part is inactive (I2C_STATUS[6] = 0)

	I2C_SLV_DATA_NACK_ONLY																BASE + 0x84															
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															NACK
RST																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
15:1	Reserved	Writing has no effect, read as zero.	R
0	NACK	Generate NACK. This NACK generation only occurs when I2C is a slave receiver. If this register is set to a value of 1, it can only generate a NACK after a data byte is received; hence, the data transfer is aborted and the data received is not pushed to the receive buffer. When the register is set to a value of 0, it generates NACK/ACK, depending on normal criteria. ■ 1 = generate NACK after data byte received ■ 0 = generate NACK/ACK normally	R/W

Note: The I2C_STATUS[6] is a register read-back location for the internal slv_activity signal; the user

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

should poll this before writing the I2C_slv_data_nack_only bit.

22.2.2.35 I2C_DMACR (I2C DMA Control Register)

The register is used to enable the DMA Controller interface operation. There is a separate bit for transmit and receive. This can be programmed regardless of the state of I2C_ENABLE.

	I2C_DMACR																															BASE + 0x88
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														TDEN	RDEN
RST																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
15:2	Reserved	Writing has no effect, read as zero.	R
1	TDEN	**Transmit DMA Enable**. This bit enables/disables the transmit DMA channel. 0: Transmit DMA disabled 1: Transmit DMA enabled Reset value: 0x0.	R/W
0	RDEN	**Receive DMA Enable**. This bit enables/disables the receive DMA channel. 0: Receive DMA disabled 1: Receive DMA enabled Reset value: 0x0.	R/W

22.2.2.36 I2C_DMATDLR (I2C DMA Transmit Data Level Register)

	I2C_DMACR																															BASE + 0x8c
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										TDLR					
RST																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
15:5	Reserved	Writing has no effect, read as zero.	R
4:0	TDLR	**DMA Transmit Data Level**. This bit field controls the level at which a DMA request is made by the transmit logic. The dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value.	R/W

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

22.2.2.37 I2C_DMARDLR (I2C DMA Transmit Data Level Register)

	I2C_DMACR																															BASE + 0x90
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										RDLR					
RST																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
15:5	Reserved	Writing has no effect, read as zero.	R
4:0	RDLR	**DMA Receive Data Level**. This bit field controls the level at which a DMA request is made by the receive logic. The dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or more than this field value + 1.	R/W

22.2.2.38 I2C_SDASU (I2C SDA Setup Register)

This register controls the amount of time delay (in terms of number of APB clock periods) introduced in the rising edge of SCL, relative to SDA changing, when I2C services a read request in a slave-transmitter operation. The relevant I2C requirement is $t_{SU:DAT}$(*NOTE 5*)as detailed in the I2C Bus Specification(Please Google "*UM10204 pdf*").

NOTE: The length of setup time is calculated using [(I2C_SDASU - 1) * (apb_clk_period)], so if the user requires 10 apb clock periods of setup time, they should program a value of 11. The I2C_SDA_SETUP register is only used by the I2C when operating as a slave transmitter

NOTE 5: A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement $t_{SU;DAT}$ >= 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r\ max}$ + $t_{SU;DAT}$ = 1000 +250 =1250 ns (according to the Standard-mode I2C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time(Please refer NXP Semiconductors, *UM10204: I2C-Bus specification and user manual (Rev.6--4 April 2014), Table 10, Fig 38*)

	I2C_SDASU																															BASE + 0x94
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

																	Reserved								SDASU						
RST																	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0

Bits	Name	Description	R/W
15:8	Reserved	Writing has no effect, read as zero.	R
7:0	SDASU	SDA Setup. It is recommended that if the required delay is 1000ns, then for an APB clock frequency of 10 MHz, I2CSDASU should be programmed to a value of 11.	R/W

22.2.2.39 I2C_ACKGC (I2C ACK General Call Register)

The register controls whether I2C responds with an ACK or NACK when it receives an I2C General Call address.

	I2C_ACKGC																														BASE + 0x98
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																	Reserved															ACKGC
RST																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Name	Description	R/W
15:1	Reserved	Writing has no effect, read as zero.	R
0	ACKGC	ACK General Call. When set to 1, I2C responds with an ACK when it receives a General Call. When set to 0, the I2C does not generate General Call interrupts.	R/W

22.2.2.40 I2C_ENBST (I2C Enable Status)

The register is used to report the I2C hardware status when the I2C_ENABLE[0] is set from 1 to 0; that is, when I2C is disabled.

If I2C_ENABLE[0] has been set to 1, bits 2:1 are forced to 0, and bit 0 is forced to 1.

If I2C_ENABLE[0] has been set to 0, bits 2:1 is only be valid as soon as bit 0 is read as ‘0’.

Note: When I2C_ENABLE[0] has been set to 0, a delay occurs for bit 0 to be read as 0 because

disabling the I2C depends on I2C bus activities.

	I2C_ENBST																														BASE + 0x9C
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

																	Reserved													SLVRDLST	SLVDISB	I2CEN
RST																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
15:3	Reserved	Writing has no effect, read as zero.	R
2	SLVRDLST	Slave Received Data Lost. This bit indicates if a Slave-Receiver operation has been aborted with at least one data byte received from an I2C transfer due to the setting of I2C_ENABLE[0] from 1 to 0. When read as 1, I2C is deemed to have been actively engaged in an aborted I2C transfer (with matching address) and the data phase of the I2C transfer has been entered, even though a data byte has been responded with a NACK. **NOTE:** If the remote I2C master terminates the transfer with a STOP condition before the I2C has a chance to NACK a transfer, and I2C_ENABLE[0] has been set to 0, then this bit is also set to 1. When read as 0, I2C is deemed to have been disabled without being actively involved in the data phase of a Slave-Receiver transfer. **NOTE:** The CPU can safely read this bit when I2C_ENABLE[0] is read as 0. Reset value: 0x0.	R
1	SLVDISB	Slave Disabled While Busy (Transmit, Receive). This bit indicates if a potential or active Slave operation has been aborted due to the setting of the I2C_ENABLE register from 1 to 0. This bit is set when the CPU writes a 0 to the I2C_ENABLE register while: (a) I2C is receiving the address byte of the Slave-Transmitter operation from a remote master; OR, (b) address and data bytes of the Slave-Receiver operation from a remote master. When read as 1, I2C is deemed to have forced a NACK during any part of an I2C transfer, irrespective of whether the I2C address matches the slave address set in I2C (I2CSAR register) OR if the transfer is completed before I2CENB is set to 0 but has not taken effect. **NOTES:** 1 If the remote I2C master terminates the transfer with a STOP condition before the I2C has a chance to NACK a transfer, and I2CENB has been set to 0, then this bit will also be set to 1. When read as 0, I2C is deemed to have been disabled when there is master activity, or when the I2C bus is idle. 2 The CPU can safely read this bit when I2C_ENABLE[0] is read as 0.	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		Reset value: 0x0.	
0	I2CEN	When read as 1, I2C is deemed to be in an enabled state. When read as 0, I2C is deemed completely inactive.	R

22.2.2.41 I2C_FS_SPKLEN (I2C SS and FS Spike Suppression Limit Register)

This register is used to store the duration, measured in APB clock cycles, of the longest spike that is filtered out by the spike suppression logic when the component is operating in SS or FS modes. This register must be programmed with a minimum value of 1.

	I2C_FS_SPKLEN																															BASE + 0xA0
Bit																									7	6	5	4	3	2	1	0
																									FSSPKLEN							
RST																									0	0	0	0	0	0	0	1

Bits	Name	Description	R/W
7:0	FSSPKLEN	This register sets the duration, measured in I2C device clock cycles, of the longest value in the SCL or SDA lines that are filtered out by the spike suppression logic. This register can be written only when the I2C interface is disabled. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted, results in 1 being set.	RW

22.3 Operating Flow

This section provides information on the following topics:

- "Slave Mode Operation"
- "Master Mode Operation"
- "Disabling I2C"

NOTE: It is important to note that the I2C should only be set to operate as an I2C Master, or I2C Slave, but not both simultaneously. This is achieved by ensuring that bit 6 (I2CSLAVE_DISABLE) and 0 (I2CMASTER_MODE) of the I2CCON register are never set to 0 and 1, respectively.

22.3.1 I2C Behavior

The I2C can be controlled via software to be either:

- An I2C master only, communicating with other I2C slaves.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

- OR
  - An I2C slave only, communicating with one more I2C masters.

The master is responsible for generating the clock and controlling the transfer of data. The slave is responsible for either transmitting or receiving data to/from the master. The device that is receiving data, which can be either a master or a slave, sends the acknowledgement of data. As mentioned previously, the I2C protocol also allows multiple masters to reside on the I2C bus and uses an arbitration procedure to determine bus ownership.

Each slave has a unique address that is determined by the system designer. When a master wants to communicate with a slave, the master transmits a START/RESTART condition that is then followed by the slave's address and a control bit (R/W) to determine if the master wants to transmit data or receive data from the slave. The slave then sends an acknowledgement (ACK) pulse after the address.

If the master (master-transmitter) is writing to the slave (slave-receiver), the receiver gets one byte of data. This transaction continues until the master terminates the transmission with a STOP condition. If the master is reading from a slave (master-receiver), the slave transmits (slave-transmitter) a byte of data to the master, and the master then acknowledges the transaction with the ACK pulse. This transaction continues until the master terminates the transmission by not acknowledging (NACK) the transaction after the last byte is received, and then the master issues a STOP condition or addresses another slave after issuing a RESTART condition.

22.3.2 Master Mode Operation

This section includes the following topics:

- "Initial Configuration"
- "Dynamic I2CTAR or I2C10BITADDR_MASTER Update"
- "Master Transmit and Master Receive"
-

22.3.2.1 Configuration

To use the I2C as a master perform the following steps:

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

1 Disable the I2C by writing 0 to the I2CENB register. And wait for the I2CENBST.I2CEN = 0.
2 Write to the I2C_CON register to set the speed mode supported (bits 2:1). Please note that the MATP (bit4) is NOT writable. The addressing mode is controlled by Register I2C_TAR.
3 Set the expected SCL frequency. I2C_CON.SPEED = 2'b01, only I2C_SHCNT and I2CSLCNT are needed to be configured; I2C_CON.SPEED = 2'b10, only I2C_FHCNT and I2C_FLCNT are needed to be configured. I2C_CON.SPEED = 2'b11, only I2C_HHCNT and I2C_HLCNT are needed to be configured.
   Supposed:
   T_{scl} : I2C SCL period
   T_{I2C_clk}: I2C device clock period
   $T_{min_scl_l}$: Protocol minimum SCL low time
   $T_{min_scl_h}$: Protocol minimum SCL high time
   Then can get the equation:
   $T_{scl} = T_{I2C_clk} * ((I2C*HCNT + 8) + (I2C*LCNT + 1))$
   And the following conditions should be met:
   $(I2C*HCNT + 8) * T_{I2C_clk} >= T_{min_scl_h}$
   $(I2C*LCNT + 1) * T_{I2C_clk} >= T_{min_scl_l}$
   I2C*HCNT >= 6
   I2C*LCNT >= 8
4 Write to the I2C_TAR register the address of the I2C device to be addressed. It also indicates whether a General Call or a START BYTE command is going to be performed by I2C. The addressing mode that master starts, either 7-bit or 10-bit addressing, is controlled by the I2C10BITADDR_MASTER bit field (bit 12).
5 Enable the I2C by writing a 1 into I2C_ENABLE register. And wait for the I2C_ENBST.I2CEN = 1.
6 Now write the transfer direction and data to be sent to the I2C_DC register (This can be done by DMA). If the I2C_DC register is written before the I2C is enabled, the data and commands are lost as the buffers are kept cleared when I2C is not enabled.

NOTE: For multiple I2C transfers, perform additional writes to the TX FIFO such that the TX FIFO does not become empty during the I2C transaction. If the TX FIFO is completely emptied at any stage and I2C_CON.STPHLD is 0, then further writes to the TX FIFO results in an independent I2C transaction.

22.3.2.2 Dynamic I2CTAR or I2C10BITADDR_MASTER Update

The I2C supports dynamic updating of the I2CTAR (bits 9:0) and I2C10BITADDR_MASTER (bit 12) bit fields of the I2CTAR register. You can dynamically write to the I2CTAR register provided the following conditions are met:

1 I2C is not enabled (I2CENB=0);

OR

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

2 I2C is enabled (I2CENB=1);
AND
I2C is NOT engaged in any Master (tx, rx) operation (I2CST[5]=0);
AND
I2C is enabled to operate in Master mode (I2CCON[0]=1);
AND
there are NO entries in the TX FIFO (I2CST[2]=0).

22.3.2.3 Master Transmit and Master Receive

The I2C supports switching back and forth between reading and writing dynamically. To transmit data, write the data to be transferred to lower byte of the I2C Rx/Tx Data Buffer and Command Register (I2C_DC). The *CMD* bit (I2C_DC[8]) should be written to 0 for I2C write operations.

Subsequently, a read command may be issued by writing “don’t cares” to the lower byte of the I2CDC register, and a 1 should be written to the *CMD* bit.

22.3.3 Slave Mode Operation

This section includes the following procedures:

- “Initial Configuration”
- “Slave-Transmitter Operation for a Single Byte”
- “Slave-Receiver Operation for a Single Byte”
- “Slave-Transfer Operation For Bulk Transfers”

22.3.3.1 Initial Configuration

To use the I2C as a slave, perform the following steps:

1 Disable the I2C by writing a ‘0’ to bit 0 of the I2CENB register.
2 Write to the I2C_SAR register (bits 9:0) to set the slave address. This is the address to which the I2C responds.
3 Write to the I2C_CON register to specify which type of addressing is supported (7- or 10-bit by setting bit 3). Enable the I2C in slave-only mode by writing a ‘0’ into bit 6 (I2CSLAVE_DISABLE) and a ‘0’ to bit 0 (MASTER_MODE).
NOTE: Slaves and masters do not have to be programmed with the same type of addressing 7- or 10-bit address. For instance, a slave can be programmed with 7-bit addressing and a master with 10-bit addressing, and vice versa.
4 Enable the I2C by writing a ‘1’ in bit 0 of the I2C_ENB register.
NOTE: Depending on the reset values chosen, steps 2 and 3 may not be necessary because the reset values can be configured. For instance, if the device is only going to be a master, there would be no need to set the slave address because you can configure I2C to have the slave disabled after reset and to enable the master after reset. The values stored are static and do not need to be

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

reprogrammed if the I2C is disabled.

22.3.3.2 Slave-Transmitter Operation for a Single Byte

When another I2C master device on the bus addresses the I2C and requests data, the I2C acts as a slave-transmitter and the following steps occur:

1. The other I2C master device initiates an I2C transfer with an address that matches the slave address in the I2C_SAR register of the I2C.
2. The I2C acknowledges the sent address and recognizes the direction of the transfer to indicate that it is acting as a slave-transmitter.
3. The I2C asserts the RDREQ interrupt (bit 5 of the I2CINTST register) and holds the SCL line low. It is in a wait state until software responds.
   If the RDREQ interrupt has been masked, due to I2C_INTM[5] register (MRDREQ bit field) being set to 0, then it is recommended that a hardware and/or software timing routine be used to instruct the CPU to perform periodic reads of the I2C_INTST register.
   a. Reads that indicate I2C_INTST[5] (RDREQ bit field) being set to 1 must be treated as the equivalent of the RDREQ interrupt being asserted.
   b. Software must then act to satisfy the I2C transfer.
   c. The timing interval used should be in the order of 10 times the fastest SCL clock period the I2C can handle. For example, for 400 kb/s, the timing interval is 25us.

   NOTE: The value of 10 is recommended here because this is approximately the amount of time required for a single byte of data transferred on the I2C bus.

4. If there is any data remaining in the TX FIFO before receiving the read request, then the
   I2C asserts a TX_ABRT interrupt (bit 6 of the I2CINTST register) to flush the old data from the TX FIFO.

   NOTE: Because the I2C's TX FIFO is forced into a flushed/reset state whenever a TX_ABRT event occurs, it is necessary for software to release the I2C from this state by reading the I2C_CTXABT register before attempting to write into the TX FIFO. See register I2C_INTST for more details. If the TX_ABRT interrupt has been masked, due to of I2C_INTM[6] register (MTX_ABRT bit field) being set to 0, then it is recommended that re-using the timing routine (described in the previous step), or a similar one, be used to read the I2CINTST register.

   a. Reads that indicate bit 6 (TXABT) being set to 1 must be treated as the equivalent of the TX_ABRT interrupt being asserted.
   b. There is no further action required from software.
   c. The timing interval used should be similar to that described in the previous step

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

for the
I2CINTST[5] register.

5 Software writes to the I2C_DC register with the data to be written (by writing a ‘0’ in bit 8).
6 Software must clear the RDREQ and TX_ABRT interrupts (bits 5 and 6, respectively) of the I2CINTST register before proceeding.
If the RDREQ and/or TX_ABRT interrupts have been masked, then clearing of the I2C_INTST register will have already been performed when either the RDREQ or TXABT bit has been read as 1.
7 The I2C releases the SCL and transmits the byte.
8 The master may hold the I2C bus by issuing a RESTART condition or release the bus by issuing a STOP condition.

22.3.3.3 Slave-Receiver Operation for a Single Byte

When another I2C master device on the bus addresses the I2C and is sending data, the I2C acts as a slave-receiver and the following steps occur:

1 The other I2C master device initiates an I2C transfer with an address that matches the I2C’s slave address in the I2CSAR register.
2 The I2C acknowledges the sent address and recognizes the direction of the transfer to indicate that the I2C is acting as a slave-receiver.
3 I2C receives the transmitted byte and places it in the receive buffer.

NOTE: If the RX FIFO is completely filled with data when a byte is pushed, then an overflow occurs and the I2C continues with subsequent I2C transfers. Because a NACK is not generated, software must recognize the overflow when indicated by the I2C (by the RXOF bit in the I2CINTST register) and take appropriate actions to recover from lost data. Hence, there is a real time constraint on software to service the RX FIFO before the latter overflow as there is no way to re-apply pressure to the remote transmitting master. You must select a deep enough RX FIFO depth to satisfy the interrupt service interval of their system.

4 I2C asserts the RX_FULL interrupt (I2CINTST[2] register).
If the RX_FULL interrupt has been masked, due to setting I2C_INTM[2] register to 0 or setting I2C_TX_TL to a value larger than 0, then it is recommended that a timing routine be implemented for periodic reads of the “I2CST”. Reads of the I2C_ST register, with bit 3 (RFNE) set at 1, must then be treated by software as the equivalent of the RX_FULL interrupt being asserted.
5 Software may read the byte from the I2C_DC register (bits 7:0).
6 The other master device may hold the I2C bus by issuing a RESTART condition or release the bus by issuing a STOP condition.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

22.3.3.4 Slave-Transfer Operation For Bulk Transfers

In the standard I2C protocol, all transactions are single byte transactions and the programmer responds to a remote master read request by writing one byte into the slave's TX FIFO.

When a slave (slave-transmitter) is issued with a read request (RDREQ) from the remote master (master-receiver), at a minimum there should be at least one entry placed into the slave-transmitter's TX FIFO.

I2C is designed to handle more data in the TX FIFO so that subsequent read requests can take that data without raising an interrupt to get more data. Ultimately, this eliminates the possibility of significant latencies being incurred between raising the interrupt for data each time had there been a restriction of having only one entry placed in the TX FIFO.

This mode only occurs when I2C is acting as a slave-transmitter. If the remote master acknowledges the data sent by the slave-transmitter and there is no data in the slave's TX FIFO, the I2C holds the I2C SCL line low while it raises the read request interrupt (RDREQ) and waits for data to be written into the TX FIFO before it can be sent to the remote master.

If the RDREQ interrupt is masked, due to bit 5 (MRDREQ) of the I2C_INTST register being set to 0, then it is recommended that a timing routine be used to activate periodic reads of the I2C_INTST register. Reads of I2C_INTST that return bit 5 (RDREQ) set to 1 must be treated as the equivalent of the RDREQ interrupt referred to in this section.

The RDREQ interrupt is raised upon a read request, and like interrupts, must be cleared when exiting the interrupt service handling routine (ISR). The ISR allows you to either write 1 byte or more than 1 byte into the TX FIFO. During the transmission of these bytes to the master, if the master acknowledges the last byte. Then the slave must raise the RDREQ again because the master is requesting for more data.

22.3.4 Disabling I2C

The register I2C_ENBST is added to allow software to unambiguously determine when the hardware has completely shutdown in response to the I2C_ENABLE register being set from 1 to 0.

22.3.4.1 Procedure

1. Define a timer interval (tI2C_poll) equal to the 10 times the signaling period for the highest I2C transfer speed used in the system and supported by I2C. For example, if the highest I2C transfer mode is 400 kb/s, then this tI2C_poll is 25us.
2. Define a maximum time-out parameter, MAX_T_POLL_COUNT, such that if any repeated polling operation exceeds this maximum value, an error is reported.
3. Execute a blocking thread/process/function that prevents any further I2C master

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

transactions to be started by software, but allows any pending transfers to be completed.

NOTE: This step can be ignored if I2C is programmed to operate as an I2C slave only.

4 The variable POLL_COUNT is initialized to zero.

5 Set I2CENB to 0.

6 Read the I2C_ENBST register and test the I2C_ENABLE[0]. Increment POLL_COUNT by one. If POLL_COUNT >= MAX_T_POLL_COUNT, exit with the relevant error code.

7 If I2C_ENBST[0] is 1, then sleep for tI2C_poll and proceed to the previous step. Otherwise, exit with a relevant success code.

22.3.5 Summary the condition could flush TX FIFO

1. When IC_ENABLE[0] is set to 0, the TX FIFO is flushed and held in reset.
2. TX_ABRT event occurs. The TX FIFO remains in this flushed state until the register I2C_CTXABT is read. Once this read is performed, the TX FIFO is then ready to accept more data bytes from the APB interface.
3. When act as a slave, the slave has received a read command and some data exists in the TX FIFO so the slave issues a TX_ABRT interrupt to flush old data in TX FIFO.

22.3.6 The condition could generate START, STOP and RESTART

A STOP condition is generated only when the user specifically requests it by setting bit 9 (Stop bit) of the command written to I2C_DC register. Naturally, if the last byte send out does not set bit 9 (Stop bit), the component does not generate a STOP if the Tx FIFO becomes empty; in this situation the component holds the SCL line low, stalling the bus until a new entry is available in the Tx FIFO

Figure 22-1 illustrates the behavior of the I2C when the Tx FIFO becomes empty while operating as a master transmitter, as well as showing the generation of a STOP condition.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Figure 22-1 Master Transmitter — Tx FIFO Empties/STOP Generation

Figure 22-2 illustrates the behavior of the I2C when the Tx FIFO becomes empty while operating as a master receiver, as well as showing the generation of a STOP condition.

Figure 22-2 Master Receiver — Tx FIFO Empties/STOP Generation

Figure 22-3 and Figure 22-4 illustrate configurations where the user can control the generation of RESTART conditions on the I2C bus. If bit 10 (Restart) of the I2C_DC register is set and the restart capability is enabled (IC_RESTART_EN=1), a RESTART is generated before the data byte is written to or read from the slave. If the restart capability is not enabled a STOP followed by a START is generated in place of the RESTART. Figure 22-3 illustrates this situation during operation as a master transmitter.

Figure 22-3 Master Transmitter — Restart bit of I2C_DC is set

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Figure 22-4 illustrates the same situation, but during operation as a master receiver.

Figure 22-4 Master Receiver — Restart bit of I2C_DC is set

Figure 22-5 illustrates operation as a master transmitter where the Stop bit of the I2C_DC register is set and the Tx FIFO is not empty

Figure 22-5 Master Transmitter — Stop Bit of I2C_DC Set/Tx FIFO Not Empty

Figure 22-6 illustrates operation as a master transmitter where the first byte loaded into the Tx FIFO is allowed to go empty with the Restart bit set.

Figure 22-6 Master Transmitter — First Byte Loaded Into Tx FIFO Allowed to Empty, Restart Bit Set

Figure 22-7 illustrates operation as a master receiver where the Stop bit of the I2C_DC register is set and the Tx FIFO is not empty.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Figure 22-7 Master Receiver — Stop Bit of IC_DATA_CMD Set/Tx FIFO Not Empty

Figure 22-8 illustrates operation as a master receiver where the first command loaded after the Tx FIFO is allowed to empty and the Restart bit is set

Figure 22-8 Master Receiver — First Command Loaded After Tx FIFO Allowed to Empty/Restart Bit Set

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

23 Synchronous Serial Interface(SSI)

23.1 Overview

The SSI is a full-duplex synchronous serial interface and can connect to a variety of external analog-to-digital (A/D) converters, audio and telecom CODECS, and other devices that use serial protocols for transferring data. The SSI supports National's Microwire, Texas Instruments Synchronous Serial Protocol (SSP), and Motorola's Serial Peripheral Interface (SPI) protocol.

The SSI operates in master mode (the attached peripheral functions as a slave) and supports serial bit rates from 7.2 KHz to 50 MHz. Serial data formats may range from 2 to 32 bits in length. The SSI provides 128 entries deep x 32 bits wide transmit and receive data FIFOs.

The FIFOs may be loaded or emptied by the Central Processor Unit (CPU) using programmed I/O, or DMA transfers while receiving or transmitting.

23.2 Features

- 3 protocols support: National's Microwire, TI's SSP, and Motorola's SPI
- Full-duplex or transmit-only or receive-only operation
- Programmable transfer order: MSB first or LSB first
- 128 entries deep x 32 bits wide transmit and receive data FIFOs
- Configurable normal transfer mode or Interval transfer mode
- Programmable clock phase and polarity for Motorola's SPI format
- Two slave select signal supporting up to 2 slave devices
- Back-to-back character transmission/reception mode
- Loop back mode for testing

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

23.3 Block Diagram

Figure 23-1 SSI Block Diagram

The APB Interface is a slave interface. It is used for register configuration and data transfer.
The FIFO block is bidirectional. There are two 128x32 memory in this block, one used as transmission data buffer, and the other used for data reception.
The Clk_gen module generate the sub-clocks for the Transfer Control module.
The Transfer Control act as the handler of SPI timing generation.

23.4 Functional Description

Serial data is transferred between the processor and external peripheral through FIFO buffers in the SSI. Data transfers to system memory are handled by either the CPU (using programmed I/O) or by DMA. Operation is full duplex-separate buffers and serial data paths permit simultaneous transfers to and from the external peripheral.

Programmed I/O transmits and receives data directly between the CPU and the transmit/receive FIFO's. The DMA controller transfers data during transmit and receive operations between memory and the FIFO's.

Transmit data is written by the CPU or DMA to the SSI's transmit FIFO. The SSI then takes the data from the FIFO, serializes it, and transmits it via the SSI_DO signal to the peripheral. Data from the peripheral is received via the SSI_DIsignal, converted to parallel words and is stored in the Receive FIFO. Read operations automatically target the receive FIFO, while write operations write data to the transmit FIFO. Both the transmit and receive FIFO buffers are 128

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

entries deep by 17 bits wide. As the received data fills the receive FIFO, a programmable threshold triggers an interrupt to the Interrupt Controller. If enabled, an interrupt service routine responds by identifying the source of the interrupt and then performs one or several read operations from the inbound (receive) FIFO buffer.

23.5 Pin Description

Table 23-1 SSI Controller Pins Description

Name	I/O	Description
SSI_CLK	Output	Serial bit-rate clock
SSI_FRM1	Output	First slave select enable
SSI_DO	Output	Transmit data
SSI_DI	Input	Receive data
SSI_CE2	Output	Second slave select enable
SSI_GPC	Output	General purpose control signal to external chip

SSI_CLK is the bit-rate clock driven from the SSI to the peripheral. SSI_CLK is toggled only when data is actively being transmitted and received.
SSI_FRM1 or SSI_CE2 are the frame signal, indicating the begin and the end of a serialized data word.
SSI_DO and SSI_DI are the Transmit and Receive serial data lines in standard SPI, SSP and NM protocol.
SSI_GPC is general-purpose control signal, synchronized with SSI_CLK, can be used for LCD control.

23.6 Data Formats

Four signals are used to transfer data between the processor and external peripheral. The SSI supports three formats: Motorola SPI, Texas Instruments SSP, and National Microwire.
Although they have the same basic structure the three formats have significant differences, as described below:

1 SSI_FRM1/SSI_CE2 varies for each protocol as follows:
   - For SPI and Microwire formats, SSI_FRM1/SSI_CE2 functions as a chip select to enable the external device (target of the transfer), and is held active-low during the data transfer.
   - For SSP format, this signal is pulsed high for one serial bit-clock period at the start of each frame.

2 SSI_CLK varies for each protocol as follows:
   - For Microwire, both transmit and receive data sources switch data on the falling edge of SSI_CLK, and sample incoming data on the rising edge.
   - For SSP, transmit and receive data sources switch data on the rising edge of SSI_CLK, and sample incoming data on the falling edge.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

- For SPI, the user has the choice of which edge of SSI_CLK to use for switching outgoing data, and for sampling incoming data. In addition, the user can move the phase of SSI_CLK, shifting its active state one-half period earlier or later at the start and end of a frame.

While SSP and standard SPI are full-duplex protocols, Microwire use a half-duplex master-slave messaging protocol. At the start of a frame, a 1 or 2-byte control message is transmitted from the controller to the peripheral. The peripheral does not send any data. The peripheral interprets the message and, if it is a READ request, responds with requested data, one clock after the last bit of the requesting message.

The serial clock (SSI_CLK) only toggles during an active frame. At other times it is held in an inactive or idle state, as defined by its specified protocol.

23.6.1 Motorola's SPI Format Details

23.6.1.1 General Single Transfer Formats

The figures below show the timing of general single transfer format.

Figure 23-2 Standard SPI Single Character Transfer Format (PHA = 0)

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Figure 23-3 Standard SPI Single Character Transfer Format (PHA = 1)

For SSICR1.PHA = 0, when SSICR1.TFVCK = B'00, hardware ensures the first clock edge appears one SSI_CLK period after SSI_FRM1/SSI_CE2 goes valid; when SSICR1.TCKFI = B'00, hardware ensures the SSI_FRM1/SSI_CE2negated half SSI_CLK period after last clock change edge; when SSICR1.TFVCK ≠ B'00 or SSICR1.TCKFI ≠ B'00, 1/2/3 more clock cycles are inserted.

For SSICR1.PHA = 1, when SSICR1.TFVCK = B'00, hardware ensures the first clock edge appears half SSI_CLK period after SSI_FRM1/SSI_CE2 goes valid; when SSICR1.TCKFI = B'00, hardware ensures the SSI_FRM1/SSI_CE2 negated one SSI_CLK period after last clock change edge; when SSICR1.TFVCK ≠ B'00 or SSICR1.TCKFI ≠ B'00, 1/2/3 more clock cycles are inserted.
Data is sampled from SSI_DI_IO1 at every rising edge (when PHA = 0, POL = 0 or PHA = 1, POL = 1) or at every falling edge (when PHA = 0, POL = 1 or PHA = 1, POL = 0). According to Standard SPI protocol, input data should be stable at every sample clock edge.

Drive data onto output line at every rising edge (when PHA = 0, POL = 1 or PHA = 1, POL = 0) or at every falling edge (when PHA = 0, POL = 0 or PHA = 1, POL = 1).

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

23.6.1.2 Back-to-Back Transfer Formats

Figure 23-4 Standard SPI Back-to-Back Transfer Format

For Motorola's SPI format transfers those continuous characters are exchanged during SSI_FRM1/SSI_CE2being valid, the timing is illustrated in the figure (SSICR1.ITFRM = 0).

Back-to-back transfer is performed as transmit-only/full-duplex operation when transmit-FIFO is not empty before the completion of the last character's transfer or performed as receive-only operation.

23.6.1.3 Frame Interval Mode Transfer Format

When in interval mode (SSIITR. IVLTM ≠ '0'), SSI always wait for an interval time (SSIITR.IVLTM), transfer fixed number of characters (SSIICR), then repeats the operation.

When SSICR0.RFINE = 1, if transmit-FIFO is still empty after the interval time, receive-only transfer will occur.

During interval-wait time, SSI stops SSI_CLK, and when SSICR1.ITFRM = 0 it negates the SSI_FRM1/SSI_CE2, when SSICR1.ITFRM = 1 it keeps asserting the SSI_FRM1/SSI_CE2.

For transfers finished with transmit-FIFO empty, if the SSI transmit-FIFO is empty before fixed number of characters being loaded to transfer (SSICR1.UNFIN must be 1), then the SSI will set SSISR.UNDR = 1; if enabled, it'll send out a SSI under-run interrupt. At the same time, SSI will hold the SSI_FRM1/SSI_CE2 and SSI_CLK signals at current status and wait for the transmit-FIFO filling. The SSI will continue transfer after transmit-FIFO being filled. The SSI always stops after completion of fixed number of characters' transfer (SSICR1.UNFIN must be

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

0) with transmit-FIFO empty.

For transfers finished by SSICR0.RFINC being valid set, the SSI will stop after finished current character transfer and needn't wait for a whole completion of fixed number of characters' transfer.

Two Interval transfer mode are illustrated in the following figures. In these timing diagram, SSICR1.PHA = 0, SSICR1.POL = 0 and SSIICR = 0.

Figure 23-5 Standard SPI Frame Interval Mode Transfer Format (ITFRM = 0, ITFRM= 0)

Figure 23-6 Standard SPI Frame Interval Mode Transfer Format (ITFRM = 1, ITFRM = 1)

23.6.2 TI's SSP Format Details

In this format, each transfer begins with SSI_FRM1 pulsed high for one SSI_CLK period. Then both master and slave drive data at SSI_CLK's rising edge and sample data at the falling edge. Data are transferred with MSB first or LSB first. At the end of the transfer, SSI_DO retains the

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

value of the last bit sent through the next idle period.

Figure 23-7 TI's SSP Single Transfer Format

Figure 23-8 TI's SSP Back-to-back Transfer Format

23.6.3 National Microwire Format Details

It supports format 1 and format 2.

Format		Drive Edge	Sample Edge
NM1	Master	↓	↑
	Slave	↓	↑
NM2	Master	↓	↓
	Slave	↑	↑

If format 1 is selected, both master and slave drive data at SSI_CLK falling edge and sample data at the rising edge.

If format 2 is selected, master drive and sample data at SSI_CLK falling edge, slave drive and sample data at SSI_CLK rising edge.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

SSI_CLK goes high midway through the command's MSB (or LSB) and continues to toggle at the bit rate. One bit clock (format 1) or half bit clock (format 2) period after the last command bit, the external slave must return the serial data requested, with MSB first (or LSB first) on SSI_DI.

SSI_FRM1/SSI_CE2 de-asserts high half clock (SSI_CLK) period (and 1/2/3 additional clock periods) later.

Format 1 support back-to-back transfer, the start and end of back-to-back transfers are similar to those of a single transfer. However, SSI_FRM1/SSI_CE2 remains asserted throughout the transfer. The end of a character data on SSI_DI is immediately followed by the start of the next command byte on SSI_DO.

Figure 23-9 National Microwire Format 1 Single Transfer

Figure 23-10 National Microwire Format 1 Back-to-back Transfer

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Figure 23-11 National Microwire Format 2 Read Timing

Figure 23-12 National Microwire Format 2 Write Timing

23.7 Register Description

Following chapter will descript the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. The registers can be read and written by APB bus
3. Register read/write attribute

   R - Read only

   W - Write only

   RW - read and write

   RCW - read and write, but clear to 0 by read

   RSW - read and write, but set to 1 by read

   RWC - read and write, clear to 0 by write 1, write 0 has no effect

   RWS - read and write, set to 1 by write 1, write 0 has no effect

   RC - read only, and clear to 0 by read

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

RS - read only, and set to 1 by read

SPEC - special access method, relate to its description

4. Reset Value

1 - reset to 1

0 - reset to 0

? - value unknown after reset

23.7.1 Registers Mapping

Table 23-2 Registers Memory Map Base Address

Name	Base	Description
SSI0	0x10043000	Address base of SSI0

The SSI is controlled by a set of registers that the application configures before every operation. The following table lists all the registers.

Table 23-3 SSI Serial Port Registers Map

Name	RW	Reset Value	Address Offset	Access Size
SSIDR	RW	0x????_????	0x0000	32
SSICR0	RW	0x0000_0000	0x0004	32
SSICR1	RW	0x0008_7830	0x0008	32
SSISR	RW	0x0000_0098	0x000C	32
SSIITR	RW	0x????_0000	0x0010	16
SSIICR	RW	0x????_????	0x0014	8
SSIGR	RW	0x????_??00	0x0018	16
SSIRCNT	RW	0x0000_0000	0x001C	32

23.7.2 Register and Fields Description

23.7.2.1 SSI Data Register(SSIDR,0x0000)

	SSIDR																															Base + 0x0000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	D31-D17															GPC/D16	D15-10															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:17	D31-D17	D31-D17 to be written to/read from Transmit/Receive FIFO.	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

16	GPC/D16	This bit can be used as normal data bus bit 16 or GPC bit alternatively. When it is used as normal data bus bit, it's readable / writable; when SSI_GPC is used, it is GPC bit for SSI_GPC pin output and it's write-only.	RW
15:0	D15-D0	D15-D0 to be written to/read from Transmit/Receive FIFO. When the transfer frame length is less than 17-bit, received data is automatically right justified in the receive-FIFO and the upper unused bits are filled with '0'. For transmission, the upper unused bits of the data written into SSIDR is ignored by the transmit logic. **Note:** "upper unused bits" does not include the SSIDR.GPC bit. National Microwire format includes format 1 and format2, when national Microwire format 2 is selected, Bit 16 of SSIDR is defined as read/write operation judge bit, if it is 0, bit 15~0 represent one read command; if it is 1, bit 15~0 represent one write command and following is the written data. So the maximum length of one command (is defined in MCOM) is 16, the maximum length of one written or read data (is defined in FLEN) can be 17. Transmit-FIFO only contain one read operation command once, or one write operation command and its data once, after transmit-FIFO is empty, next command can be filled in transmit-FIFO.	RW

23.7.2.2 SSI Control Register0(SSICR0,0x0004)

	SSICR0																															Base + 0x0004
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved												TENDIAN		RENDIAN		SSIE	TIE	RIE	TEIE	REIE	LOOP	RFINE	RFINC	EACLRUN	FSEL	Reserved	VRCNT	TFMODE	TFLUSH	RFLUSH	DISREV
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:20	Reserved	Writing has no effect, read as '0'.	R
19:18	TENDIAN	Transfer endian 0: Most significant byte in a word first, most significant bit in a byte first. 1: Most significant byte in a word first, least significant bit in a byte first. 2: Least significant byte in a word first, least significant bit in a byte first. 3: Least significant byte in a word first, most significant bit in a byte first.	RW
17:16	RENDIAN	Receive endian 0: Most significant byte in a word first, most significant bit in a byte first. 1: Most significant byte in a word first, least significant bit in a byte first. 2: Least significant byte in a word first, least significant bit in a byte first. 3: Least significant byte in a word first, most significant bit in a byte first	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

<table>
<tr><td>15</td><td>SSIE</td><td>This bit is used to enable/disable SSI module. 0: disable; 1: enable. Clearing SSIE will not reset SSI FIFO, SSICR0, SSICR1, SSIGR, SSIITR and SSIICR automatically. Software should ensure the FIFOs/registers are properly configured and be flush/reset manually when necessary before enabling SSI.</td><td>RW</td></tr>
<tr><td>14</td><td>TIE</td><td>This bit enables/disables the transmit-FIFO half-empty interrupt TXI and the tdreq signal to PDMA.
0: disable; 1: enable for the TXI interrupt
1: disable; 0: enable for the tdreq signal to PDMA.
Note: the TXI interrupt and tdreq signal to PDMA can't work at the same time.</td><td>RW</td></tr>
<tr><td>13</td><td>RIE</td><td>This bit enables/disables the receive-FIFO half-full interrupt RXI and the rdreq signal to PDMA.
0: disable; 1: enable.for the RXI interrupt
1: disable; 0: enable for the rdreq signal to PDMA.
Note: the RXI interrupt and rdreq signal to PDMA can't work at the same time.</td><td>RW</td></tr>
<tr><td>12</td><td>TEIE</td><td>This bit enables/disables the transmit-error interrupt TEI.
0: disable; 1: enable.</td><td>RW</td></tr>
<tr><td>11</td><td>REIE</td><td>This bit enables/disables the receive-error interrupt REI.
0: disable; 1: enable.</td><td>RW</td></tr>
<tr><td>10</td><td>LOOP</td><td>Used for test purpose. In loop mode, the output of SSI transmit shift register is connected to input of SSI receive shift register internally. The data received should be the same as the data transmitted. And do not output any valid signals on the pins.
0: normal SSI mode; 1: LOOP mode.</td><td>RW</td></tr>
<tr><td>9</td><td>RFINE</td><td>Receive finish control enable.
0: disable; 1: enable.
For SSICR1.FMAT = B’010 (National Microwire format 1 is selected), SSICR0.RFINE must be 0.
The receive finish condition list below:
<table>
<tr><th>RFINE</th><th>RFINC</th><th>Receive Finish Condition</th></tr>
<tr><td>0</td><td>x</td><td>Same as transmit completion condition (transmit-fifo is empty and SSICR1.UNFIN = 0)</td></tr>
<tr><td>1</td><td>0</td><td>Receive continue</td></tr>
<tr><td>1</td><td>1</td><td>Receive finish</td></tr>
</table></td><td>RW</td></tr>
<tr><td>8</td><td>RFINC*</td><td>Receive finish control bit.
0: receive continue
1: receive finished</td><td>RW</td></tr>
<tr><td>7</td><td>EACLRUN</td><td>0: don’t auto clear under flag, software clear under
1: software auto clear under flag when tfifo don’t empty</td><td>RW</td></tr>
<tr><td>6</td><td>FSEL</td><td>This bit sets the frame signal to be used for slave select. The unselected</td><td>RW</td></tr>
</table>

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		frame signal always output invalid level. 0: SSI_FRM1 is selected 1: SSI_CE2_IO2 is selected	
5	Reserved	Writing has no effect, read as zero.	R
4	VRCNT	Receive counter (RCNT) valid flag. 0: SSIRCNT.RCNT will be ignored. 1: SSIRCNT.RCNT will be used.	RW
3	TFMODE	0: new tfifo empty mode(with Grey code convert, recommended) 1: old tfifo empty mode(not recommended)	RW
2	TFLUSH	Flush the transmit FIFO when set to 1. Always return 0 after one cycle of pclk.	RW
1	RFLUSH	Flush the receive FIFO when set to 1. Always return 0 after one cycle of pclk	RW
0	DISREV	Receive function enable. 0: enable. 1: disable.	RW

Note:

*: When transmitting finished or for receive-only operation, transmit function can be disabled and this bit is used to control receiving completion, and the SSI will consume less power.

When the finish condition is set, the receiving will complete after present character is completely shifted in, then the SSI will stop the SSI_CLK and negate the SSI_FRM1 / SSI_CE2_IO2 if necessary. To make sure present transfer is completed, user must read and get SSISR.END = 1 (or SSISR.BUSY = 0).

23.7.2.3 SSI Control Register1(SSICR1,0x0008)

	SSICR1																															Base + 0x0008
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FRMHL		TFVCK		TCKFI		GPCMD	ITFRM	UNFIN	Reserved	FMAT		TTRG				MCOM				RTRG				FLEN					GPCHL	PHA	POL
RST	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	1	0	0	0	0	0	1	1	0	0	0	0

Bits	Name	Description	RW
31:30	FRMHL	Frame valid level select, FRMHL [1: 0] correspond to SSI_CE2_IO2 and SSI_FRM1 respectively. **FRMHL[1:0]** / **Description** / 00 / SSI_FRM1 is low level valid and / Initial value	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

			SSI_CE2_IO2 is low level valid	
		01	SSI_FRM1 is high level valid and SSI_CE2_IO2 is low level valid	
		10	SSI_FRM1 is low level valid and SSI_CE2_IO2 is high level valid	
		11	SSI_FRM1 is high level valid and SSI_CE2_IO2 is high level valid	
29:28	TFVCK	Time from frame valid to clock start. When TFVCK = B'00, the time is fixed half or one SSI_CLK cycle according to SSICR1.POL and SSICR1.PHA configuration. For SSICR1.FMAT = B'001, SSICR1.TFVCK is ignored.		RW
		TFVCK[1:0]	**Description**	
		00	half or one SSI_CLK cycle delay time	Initial value
		01	1 more SSI_CLK cycle delay is added	
		10	2 more SSI_CLK cycle delay is added	
		11	3 more SSI_CLK cycle delay is added	
27:26	TCKFI	Time from clock stop to frame invalid. When TCKFI = B'00, the time is fixed one SSI_CLK or half SSI_CLK cycle according to SSICR1.POL and SSICR1.PHA configuration. For SSICR1.FMAT = B'001, SSICR1.TFVCK is ignored.		RW
		TCKFI[1:0]	**Description**	
		00	half or one SSI_CLK cycle delay	Initial value
		01	1 more SSI_CLK cycle delay is added	
		10	2 more SSI_CLK cycle delay is added	
		11	3 more SSI_CLK cycle delay is added	
25	GPCMD	SSI_GPC in normal mode or special mode, 0:normal; 1:special In normal mode, SSI_GPC level is related to SSIDR; In special mode, SSI_GPC can be configured, and its level is GPCHL.		RW
24	ITFRM	Frame during interval, selects if the Frame (SSI_FRM1 /SSI_CE2_IO2) signal is negated or not during interval time at Interval Mode (SSICR1.FMAT = B'000(quad and dual spi?) and SSIITR.IVLTM ≠ H'0000). It's ignored at Normal Mode. 0: SSI_FRM1 /SSI_CE2_IO2 de-asserts during interval time at Interval Mode 1: SSI_FRM1 /SSI_CE2_IO2 keeps asserted during interval time at Interval Mode		RW
23	UNFIN	This bit controls whether the SSI finishes transmission or wait for data filling (underrun happen) after all data in transmit-FIFO are sent out during transfer. This bit must be cleared to 0 when SSICR1.FMAT = B'001. (TI's SSP format) 0: TxFIFO empty means end of transmission 1: Transmission didn't finish when transmit-FIFO is empty, SSI underrun		RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

<table>
<tr><td></td><td></td><td>error would occur and SSI waits for data filling; SSI_CLK and SSI_FRM1 /SSI_CE2_IO2 keeps asserted, SSI_CLK stop at the current level
Note: For TxFIFO empty before any transfer after SSI enabled, if SSICR1.UNFIN = 1 or SSICR0.RFINE = 0, SSI will wait till TxFIFO isn't empty then start to transfer and no underrun error will occur; if SSICR1.UNFIN = 0 and SSICR0.RFINE = 1, after transmit-FIFO become empty, SSI will start a receive-only transfer.</td><td></td></tr>
<tr><td>22</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td>R</td></tr>
<tr><td>21:20</td><td>FMAT</td><td>These bits set the operating transfer format.
<table>
<tr><th>FMAT</th><th>Description</th><th></th></tr>
<tr><td>00</td><td>Motorola's SPI format(standard)</td><td>Initial value</td></tr>
<tr><td>01</td><td>TI's SSP format</td><td></td></tr>
<tr><td>10</td><td>National Microwire 1 format</td><td></td></tr>
<tr><td>11</td><td>National Microwire 2 format</td><td></td></tr>
</table></td><td>RW</td></tr>
<tr><td>19:16</td><td>TTRG</td><td>These bits define the transmit-FIFO half-empty threshold value, which when equal or less characters left in transmit-FIFO, the SSISR.TFHE will be set to '1'.
0000: less than or equal to 1
n: less than or equal to nx8
Note: 0000 is not recommended</td><td>RW</td></tr>
<tr><td>15:12</td><td>MCOM</td><td>Defines the length of command.
Only used when SSICR1.FMAT = b'010 or b'011 (National Microwire format 1 or 2 is selected).
The command length is (MCOM + 1).
Initial value is b'0111.</td><td>RW</td></tr>
<tr><td>11:8</td><td>RTRG</td><td>These bits define the receive-FIFO half-full threshold value, which when equal or more characters received in receive-FIFO, the SSISR.RFHF will be set to '1'.
0000: more than or equal to 1
n: more than or equal to nx8</td><td>RW</td></tr>
<tr><td>7:3</td><td>FLEN</td><td>These bits set the bit length of every character to be transmitted/received. The maximum data length can be configured is 32 bits. For data length longer than 17 bits (multiples of the SSICR1.FLEN configured length), the software should ensure properly processing.
When SSI_GPC pin is used, the FLEN shouldn't be configured as B'01111 (17-bit data).
When TI SSP mode is selected (FMAT = 2'b001), 2-bit data length (FLEN = 0) isn't supported.
The bit length of one data = FLEN + 2
Note: In Dual SPI/Quad SPI, the bit length should be multiple of 2/4. If it is not proper, the BLI interrupt will be generated.</td><td>RW</td></tr>
</table>

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

2	GPCHL	SSI_GPC level. This bit is valid when GPCMD is high 0:low; 1:high	RW
1	PHA	This bit sets the phase of the SSI_CLK from the beginning of a data frame for SPI format (SSICR1.FMAT = B'000 or B'100 or B'101). 0: The leading edge of SSI_CLK is used to sample data from SSI_DI_IO1 after the SSI_FRM1 /SSI_CE2_IO2 goes valid, it is initial value 1: The leading edge of SSI_CLK is used to drive data onto SSI_DO_IO0 after the SSI_FRM1 /SSI_CE2_IO2 goes valid	RW
0	POL	SSI_CLK polarity for SPI format during idle state. (SSICR1.FMAT = B'000 or B'100 or B'101). 0: SSI_CLK keeps low level when idle 1: SSI_CLK keeps high level when idle	RW

23.7.2.4 SSI Status Register(SSISR,0x000C)

	SSISR																															Base + 0x000C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								TFIFO-NUM								RFIFO-NUM								END	BUSY	TFF	RFE	TFHE	RFHF	TUNDR	ROVER
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	0	0	0

Bits	Name	Description	RW
31:24	Reserved	Writing has no effect, read as zero.	R
23:16	TFIFO-NUM	These bits indicate the Characters Number in Transmit-FIFO.	R
15:8	RFIFO-NUM	These bits indicate the Characters Number in Receive-FIFO.	R
7	END	This bit indicates transfer end status. It is the inverse of SSISR.BUSY when transfer is in process, but it'll keep cleared at interval time before transfer is completed. It'll be set when transfer finished. When SSICR0.FIE is set, It will generate the XFI interrupt. This interrupt will be auto cleared to '0' after reading SSISR.	R
6	BUSY	This bit indicates SSI's working status. 0: SSI is idle or at interval time 1: Transmission and/or reception is in process	R
5	TFF	This bit denotes transmit-FIFO is full or not. 0: Transmit-FIFO is not full 1: Transmit-FIFO is full	R
4	RFE	This bit denotes receive-FIFO is empty or not. 0: Receive-FIFO is not empty 1: Receive-FIFO is empty	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

3	TFHE	This bit denotes whether the characters number in transmit-FIFO being less or equal to SSICR1.TTRG. 0: The data in transmit-FIFO is more than the condition set by SSICR1.TTRG 1: The data in transmit-FIFO meets the condition set by SSICR1.TTRG When SSICR0.TIE is set , it will generate the TXI interrupt	R
2	RFHF	This bit denotes whether the characters number in receive-FIFO being more or equal to the number set by SSICR1.RTRG. 0: The data in receive-FIFO is less than the condition set by SSICR1.RTRG 1: The data in receive-FIFO meets the condition set by SSICR1.RTRG When SSICR0.RIE is set, it will generate the RXI interrupt	R
1	TUNDR	Transmit-FIFO underrun status. When underrun happens, SSI set this bit and keeps the current status of SSI_CLK and SSI_FRM1/SSI_CE2_IO2, waiting for transmit-FIFO filling. 0: Transmit-FIFO underrun has not occurred 1: Transmit-FIFO underrun was occurred When SSICR0.TEIE is set, it will generate the TEI interrupt. Write ‘0’ to clear this bit, writing ‘1’ has no effect	RW
0	ROVER	Receive-FIFO overrun status, new received data will lose. 0: Receive-FIFO overrun has not occurred 1: Receive-FIFO overrun was occurred; When SSICR0.REIE is set, it will generate the REI interrupt. Write ‘0’ to clear this bit, writing ‘1’ has no effect	RW

23.7.2.5 SSI Interval Time Control Register(SSIITR,0x0010)

	SSIITR																															Base + 0x0010
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																CNTCLK	IVLTM														
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as indeterminate figure.	R
15	CNTCLK	Counting clock source select. 0: Use SSI bit clock (SSI_CLK) as the interval counter clock source 1: Use 32K clock as the interval counter clock source	RW
14:0	IVLTM	Interval time set, set the cycle number of counting clock source for	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		desired interval time. When SSIITR.IVLTM = 0x0000, normal mode is selected, and SSIITR.CNTCLK and SSIICR are ignored. When SSIITR.IVLTM ≠ 0x0000, interval mode(not supported by Dual and Quad mode) is selected. The interval time is calculated as follows: *Interval time ≈ [CNTCLK clock period] *[Value of IVLTM]* The actual interval time is as follow: When SSIITR.CNTCLK = 0: *Interval time = [CNTCLK clock period] * [Value of IVLTM] + 3 * dev_clk period* When SSIITR.CNTCLK = 1: *Interval time ≥ [CNTCLK clock period] * [Value of IVLTM + 1] + 1 * dev_clk period;* *Interval time ≤ [CNTCLK clock period] * [Value of IVLTM + 2] + 2 * dev_clk period*	

23.7.2.6 SSI Interval Character-per-frame Control Register(SSIICR,0x0014)

	SSIICR																															Base + 0x0014
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																													ICC		
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0

Bits	Name	Description	RW
31:3	Reserved	Writing has no effect, read as indeterminate figure.	R
2:0	ICC	Sets the fixed number of characters to be transmitted / received each time during SSI_CLK changing (and SSI_FRM1 /SSI_CE2_IO2 asserting) in interval mode for SSICR1.FMAT = B'000 (Motorola's standard SPI format is selected). SSIICR is ignored for SSICR1.FMAT ≠ B'000. The desired transfer number of characters-per-frame is (SSIICR set value + 1).	RW

23.7.2.7 SSI Clock Generator Register(SSIGR,0x0018)

	SSIGR																															Base + 0x0018
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Reserved																								CGV							
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect, read as indeterminate figure.	R
7:0	CGV	Sets the frequency of serial bit clock (SSI_CLK). The serial bit clock (SSI_CLK) is generated by dividing device-clock as follows: F_{SSI_CLK} = [Frequency of device clock] / (2 * (CGV + 1)) Device clock is generated in CPM module. The value in SSIGR can be set from 0 to 255, and initialized to 0x0000 on power-on reset.	RW

23.7.2.8 SSI Receive Counter Register(SSIRCNT,0x001C)

	SSIRCNT																															Base + 0x001C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																RCNT															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	RCNT	Number of data to be received. If SSICR1.UNFIN = 0 and SSICR0.RFINE = 1, after transmit-FIFO become empty, SSI will start a receive-only transfer. If SSICR0.VRCNT = 1, a special internal counter will be increased automatically. When the value of the internal counter equals to the RCNT, the receiving operation will be stopped automatically.	RW

23.8 Software Guideline

23.8.1 Common flow

The initial steps are:

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

1) set GPIO
2) disable interrupt (or not) by setting SSICR0
3) clear SSISR (write 0x0, clear interrupt, FIFO state and working condition)
4) flush FIFO (write SSICR0.xFLUSH once for each FIFO)
5) select the counting clock by configuring SSIITR
6) configure SSIGR (set the frequency of serial bit clock)
7) configure SSICR1 (set valid level of CE signals, set head and end delay of the transfer, set state of CE signals in interval time, select protocols, set threshold of FIFO, set bit length, etc.)
8) configure SSIICR (set the fixed number of characters to be transmit/received each time during SSI_CLK changing in interval mode)
9) configure SSIRCNT (number of data to be received)
10) configure SSICR0 (the start trigger is in this register)

Note: the frequency of dev_clk should not be 4 times or more higher than PCLK

23.8.2 Interrupt Operation

In SSI, there are TXI, TEI, TFI, RXI, REI 4 interrupts, all these interrupts are combined together to make one SSI interrupt, which can be masked by writing '1' into corresponding mask bit in INTC interrupt mask register (IMR). See Table 23-4

Table 23-4 SSI Interrupts

Operation	Condition	Flag Bit	Mask Bit	Interrupt	DMAC Activation
Transmit	T-FIFO is half-empty or less	SSISR.TFHE	SSICR0.TIE	**TXI**	Possible
	Transmit under-run error	SSISR.TUNDR	SSICR0.TEIE	**TEI**	Impossible
Receive	R-FIFO is half-full or more	SSISR.RFHF	SSICR0.RIE	**RXI**	Possible
	Receive overrun error	SSISR.ROVER	SSICR0.REIE	**REI**	Impossible

Either SSISR.TFHE or SSISR.RFHF can activate DMA transferring when corresponding individual interrupt mask bit in SSICR0 is cleared (masked) and DMA is enabled and configured.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

24 Synchronous Serial Slave Interface(SSI_SLV)

24.1 Overview

The SSI_SLV is a configurable, programmable component that is a full-duplex slave-synchronous serial interface. The host processor accesses data, control, and status information on the SSI_SLV through the APB interface. The SSI_SLV also interface with a DMA Controller using a set of DMA signals, which can be selected at configuration time. As described in more detail later, the SSI_SLV can connect to any serial-master peripheral device using one of the following interfaces: Motorola Serial Peripheral Interface (SPI), Texas Instruments Serial Protocol (SSP), and National Semiconductor Microwire.

The SSI_SLV only operates in slave mode (the attached peripheral functions as a master) and supports serial bit rates up to 40MHz. Serial data formats may range from 4 to 32 bits in length. The SSI_SLV provides 64 entries deep x 32 bits wide transmit and receive data FIFOs.

24.2 Features

- Three protocols support: Motorola's SPI, TI's SSP and National's Microwire
- Full-duplex, transmit-only or receive-only operation for Motorola's SPI and TI's SSP
- Half-duplex, transmit-only or receive-only operation for National's Microwire
- 64 entries deep x 32 bits wide transmit and receive data FIFOs
- Serial data formats may range from 4 to 32 bits in length.
- Programmable clock phase and polarity for Motorola's SPI format
- Back-to-back character transmission/reception mode
- Loop back mode for testing
- DMA controller interface, enables the SSI_SLV to interface to a DMA controller over the bus using a handshaking interface for transfer requests

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

24.3 Block Diagram

Figure 24-1 SSI_SLV Block Diagram

The APB Interface is a slave interface. It is used for register configuration and data transfer.

The FIFO block is bidirectional. There are two 64x32 memory in this block, one used as transmission data buffer, and the other used for data reception.

The Flow Control and Shift Control act as the handler of Motorola SPI/SSP/Microwire timing generation.

24.4 Functional Description

SSI_SLV is a slave communicate with SSI Master. Serial data is transferred between the processor and external peripheral through FIFO buffers in the SSI_SLV. Data transfers to system memory are handled by either the CPU (using programmed I/O) or by DMA. Motorola's SPI, TI's SSP is full duplex, National's Microwire is half duplex, the SSI_SLV has separate buffers and serial data paths permit simultaneous transfers to and from the external peripheral. Programmed I/O transmits and receives data directly between the CPU and the transmit/receive FIFO's.

Transmit data is written by the CPU or DMA to the SSI_SLV's transmit FIFO. The SSI_SLV then takes the data from the FIFO, serializes it, and transmits it via the SSI_SLV_DT signal to the peripheral. Data from the peripheral is received via the SSI_SLV_DR signal, converted to parallel words and is stored in the Receive FIFO.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Read operations automatically target the receive FIFO, while write operations write data to the transmit FIFO. Both the transmit and receive FIFO buffers are 64 entries deep by 32 bits wide. As the received data fills the receive FIFO, a programmable threshold triggers an interrupt to the Interrupt Controller. If enabled, an interrupt service routine responds by identifying the source of the interrupt and then performs one or several read operations from the inbound (receive) FIFO buffer.

DMA threshold register control the request to PDMA, then it can transfers data during transmit and receive operations between memory and the FIFO's efficiently.

24.5 Pin Description

Table 24-1 SSI_SLV Pins Description

Name	I/O	Description
SSI_SLV_CLK	Input	Serial bit-rate clock
SSI_SLV_CE0	Input	Ssi slave select enable
SSI_SLV_DT	Output	Transmit data
SSI_SLV_DR	Input	Receive data

24.6 Data Formats

Four signals are used to transfer data between the processor and external peripheral. The SSI_SLV supports three formats: Motorola SPI, Texas Instruments SSP, and National Microwire. Although they have the same basic structure the three formats have significant differences, as described below:

1. Motorola Serial Peripheral Interface (SPI) – A four-wire, full-duplex serial protocol from Motorola. There are four possible combinations for the serial clock phase and polarity. The clock phase (SCPH) determines whether the serial transfer begins with the falling edge of the slave select signal or the first edge of the serial clock. With the Motorola SPI, the clock polarity (SCPOL) configuration parameter determines whether the inactive state of the serial clock is high or low. The slave select line is held high when the SSI_SLV is idle or disabled.

2. Texas Instruments Serial Protocol (SSP) – A four-wire, full-duplex serial protocol. The slave select line used for Motorola SPI and Microwire protocols doubles as the frame indicator for the SSP protocol. Data transfers begin by asserting the frame indicator line (SSI_SLV_CE0) for one serial clock period. Data to be transmitted are driven onto the txd line one serial clock cycle later; similarly data from the slave are driven onto the rxd line. Data are propagated on the rising edge of the serial clock (SSI_SLV_SERICLK) and captured on the falling edge. The length of the data frame ranges from 4 to 32-bits.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

3. National Semiconductor Microwire – A half-duplex serial protocol, which uses a control word transmitted from the serial master to the target serial slave. Data transmission begins with the falling edge of the slave select signal (SSI_SLV_CE0). One-half serial clock (SSI_SLV_SERICLK) period later, the first bit of the control is present on the rxd line. The length of the control word can be in the range of 1 to 16 bits and is set by writing bit field CFS in the CTRLR register. The CFS bit field must be set to the size of the expected control word from the SSI_SLV serial slave. During this reception, no data are driven (high impedance) on the serial slave's txd line. The direction of the data word is controlled by the MDD bit field (bit 1) MWCR register. When MDD=0, this indicates that the SSI_SLV serial slave is to receive data from the external serial master. Immediately after the control word is transmitted, the serial master begins to drives the data frame onto the SSI_SLV slave rxd line. Data are propagated on the falling edge of the serial clock and captured on the rising edge. The slave-select signal is held active-low during the transfer and is de-asserted one-half clock cycle later after the data are transferred. The SSI_SLV slave output enable signal (ssi_oe_n, SLV_OE in the CTRLR register) is held inactive for the duration of the transfer.

24.6.1 Motorola's SPI Format Details

24.6.1.1 General Single Transfer Formats

When the configuration parameter SCPH = 0, data transmission begins on the falling edge of the slave select signal. The first data bit is captured by the master and slave peripherals on the first edge of the serial clock; therefore, valid data must be present on the txd and rxd lines prior to the first serial clock edge.

Figure 24-2 Standard Motorola SPI Single Transfer Format (SCPH= 0)

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Figure 24-3 Standard Motorola SPI Single Transfer Format (SCPH= 1)

When the configuration parameter SCPH = 1, both master and slave peripherals begin transmitting data on the first serial clock edge after the slave select line is activated. The first data bit is captured on the second (trailing) serial clock edge. Data are propagated by the master and slave peripherals on the leading edge of the serial clock. During continuous data frame transfers, the slave select line may be held active-low until the last bit of the last frame has been captured.

24.6.1.2 Back-to-Back Transfer Formats

When the SCPH =0, the SSI_SLV transfer continuous data, it toggles the slave select signal between frames and the serial clock is held to its default value .

Figure 24-4 Standard Motorola SPI Continus Transfer Format (SCPH=0)

When the SCPH =1, the SSI_SLV transfer continuous data, the slave select signal is active until data are all transfered.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Figure 24-5 Standard Motorola SPI Continus Transfer Format (SCPH=1)

24.6.2 TI's SSP Format Details

Data transfers begin by asserting the frame indicator line (ss_0_n/ss_in_n) for one serial clock period. Data to be transmitted are driven onto the txd line one serial clock cycle later; similarly data from the slave are driven onto the rxd line. Data are propagated on the rising edge of the serial clock (sclk_out/sclk_in) and captured on the falling edge. The length of the data frame ranges from 4 to 32-bits.

Figure 24-6TI's SSP Single Transfer Format

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Figure 24-7 TI's SSP Contious Transfer Format

24.6.3 National Microwire Format Details

Figure 24-8 Single Slave Microwire Serial Transfer (MDD=0)

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Figure 24-9 Single Slave Microwire Serial Transfer (MDD=1)

Figure 24-10 Slave Microwire Serial Contious Transfer (MDD=1)

24.7 Register Description

Following chapter will descript the functions of all software accessible registers.

The SSI_SLV's registers map base address is 0x10045000.

The SSI_SLV is controlled by a set of registers that the application configures before every operation. The following table lists all the registers.

Table 24-2 SSI Serial Port Registers

Name	Description	Reset Value	Address Offset	Access Size
CTRLR	Control register	0x0007_0000	0x00	32
SSIENR	Enable register	0x0000_0000	0x08	32
MWCR	Microwire Control register	0x0000_0000	0x0C	32
TXFTLR	Transmit FIFO Threshold Level register	0x0000_0000	0x18	32
RXFTLR	Receive FIFO Threshold Level register	0x0000_0000	0x1C	32
TXFLR	Transmit FIFO Level Register	0x0000_0000	0x20	32
RXFLR	Receive FIFO Level Register	0x0000_0000	0x24	32
SR	Status Register	0x0000_0006	0x28	32
IMR	Interrupt Mask Register	0x0000_001F	0x2C	32
ISR	Interrupt Status Register	0x0000_0000	0x30	32
RISR	Raw Interrupt Status Register	0x0000_0000	0x34	32
TXOICR	Transmit FIFO Overflow Interrupt Clear Register	0x0000_0000	0x38	32

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

RXOICR	Receive FIFO Overflow Interrupt Clear Register	0x0000_0000	0x3c	32
RXUICR	Receive FIFO Underflow Interrupt Clear Register	0x0000_0000	0x40	32
ICR	Interrupt Clear Register	0x0000_0000	0x48	32
DMACR	DMA Control Register	0x0000_0000	0x4c	32
DMATDLR	DMA Transmit Data Level	0x0000_0000	0x50	32
DMARDLR	DMA Receive Data Level	0x0000_0000	0x54	32
IDR	Identification Register	0xFFFF_FFFF	0x58	32
DR	Data Register	0x0000_0000	0x60	32

24.7.1 Register and Field Descriptions

24.7.1.1 SSI_SLV Control Register(CTRLR,0x00)

This register controls the serial data transfer. It is impossible to write to this register when the SSI_SLV is enabled. The SSI_SLV is enabled and disabled by writing to the SSIENR register.

	CTRLR																															Base + 0x00
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved									SPI_FRF		DFS_32					CFS				SRL	SLV_OE	TMOD		SCPOL	SCPH	FRF		Reserved			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:23	Reserved	Reserved for future use	R
22:21	SPI_FRF	Motorola SPI Frame Format: Selects data frame format for transmitting or receiving data. 00 – Standard Motorola SPI Format 01 – Reserved 10 – Reserved 11 – Reserved	RW
20:16	DFS_32	Data Frame Size in 32-bit mode Used to select the data frame size in 32-bit mode. When the data frame size is programmed to be less than 32 bits, the receive data is automatically right-justified by the receive logic, with the upper bits of the receive FIFO zero-padded. You are responsible for making sure the transmit data is right-justified before writing into the transmit FIFO. The transmit logic ignores the upper unused bits when transmitting the data. For the field decode value:	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		00000 Reserved 00001 Reserved 00010 Reserved 00011 4-bit serial data transfer 00100 5-bit serial data transfer 00101 6-bit serial data transfer 00110 7-bit serial data transfer 00111 8-bit serial data transfer ..... 11110 31-bit serial data transfer 11111 32-bit serial data transfer	
15:12	CFS	Control Frame Size. Selects the length of the control word for the Microwire frame format. For the field decode: 0000 1-bit control word 0001 2-bit control word 0010 3-bit control word 0011 4-bit control word ..... 1110 15-bit control word 1111 16-bit control word	RW
11	SRL	Shift Register Loop. Used for testing purposes only. When internally active, connects the transmit shift register output to the receive shift register input. Can be used in both serial-slave and serial-master modes. 0 – Normal Mode Operation 1 – Test Mode Operation When SSI_SLV is in loopback mode, the SSI_SLV_CE0 and SSI_SLV_SERICLK signals must be provided by an external source. In this mode, the SSI_SLV cannot generate these signals because there is nothing to which to loop back.	RW
10	SLV_OE	Slave Output Enable. This bit enables or disables the setting of the ssi_oe_n output from the SSI_SLV serial slave. When SLV_OE = 1, the ssi_oe_n output can never be active. When the ssi_oe_n output controls the tri-state buffer on the txd output from the slave, a high impedance state is always present on the slave txd output when SLV_OE = 1. This is useful when the master transmits in broadcast mode (master transmits data to all slave devices). Only one slave may respond with data on the master rxd line. This bit is enabled after reset and must be disabled by software (when broadcast mode is used), if you do not want this device to respond with data. 0 –- Slave txd is enabled 1 –- Slave txd is disabled	RW
9:8	TMOD	Transfer Mode. Selects the mode of transfer for serial communication. This	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		field does not affect the transfer duplicity. Only indicates whether the receive or transmit data are valid. In transmit-only mode, data received from the external device is not valid and is not stored in the receive FIFO memory; it is overwritten on the next transfer. In receive-only mode, transmitted data are not valid. After the first write to the transmit FIFO, the same word is retransmitted for the duration of the transfer. In transmit-and-receive mode, both transmit and receive data are valid. The transfer continues until the transmit FIFO is empty. Data received from the external device are stored into the receive FIFO memory, where it can be accessed by the host processor. 00 –- Transmit & Receive 01 –- Transmit Only 10 –- Receive Only 11 –- Reserved	
7	SCPOL	Serial Clock Polarity. Valid when the frame format (FRF) is set to Motorola SPI. Used to select the polarity of the inactive serial clock, which is held inactive when the ssi master is not actively transferring data on the serial bus.The SSI_SLV's SCPOL must be consistent with the master. 0 – Inactive state of serial clock is low 1 – Inactive state of serial clock is high	RW
6	SCPH	Serial Clock Phase. Valid when the frame format (FRF) is set to Motorola SPI. The serial clock phase selects the relationship of the serial clock with the slave select signal. When SCPH = 0, data are captured on the first edge of the serial clock. When SCPH = 1, the serial clock starts toggling one cycle after the slave select line is activated, and data are captured on the second edge of the serial clock. The SSI_SLV's SCPH must be consistent with the master. 0: Serial clock toggles in middle of first data bit 1: Serial clock toggles at start of first data bit	RW
5:4	FRF	Frame Format. Selects which serial protocol transfers the data. 00 –- Motorola SPI 01 –- Texas Instruments SSP 10 –- National Semiconductors Microwire 11 –- Reserved	RW
3:0	Reserved	Writing has no effect, read as zero.	R

24.7.1.2 SSI_SLV Enable Register(SSIENR,0x08)

This register enables and disables the SSI_SLV.

	SSIENR																															Base + 0x08
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Reserved																															SSI_SLV_EN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect, read as zero.	R
0	SSI_SLV_EN	SSI_SLV Enable. Enables and disables all SSI_SLV operations. When disabled, all serial transfers are halted immediately. Transmit and receive FIFO buffers are cleared when the device is disabled. It is impossible to program some of the SSI_SLV control registers when enabled.	RW

24.7.1.3 SSI_SLV Microwire Control Register(MWCR,0x0C)

This register controls the direction of the data word for the half-duplex Microwire serial protocol. It is impossible to write to this register when the SSI_SLV is enabled. The SSI_SLV is enabled and disabled by writing to the SSIENR register.

	MWCR																														Base + 0x0C	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														MDD	MWMOD
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:2	Reserved	Writing has no effect, read as zero.	R
1	MDD	Microwire Control. Defines the direction of the data word when the Microwire serial protocol is used. When this bit is set to 0, the data word is received by the SSI_SLV Macro Cell from the external serial device. When this bit is set to 1, the data word is transmitted from the SSI_SLV MacroCell to the external serial device.	RW
0	MWMOD	Microwire Transfer Mode. Defines whether the Microwire transfer is sequential or non-sequential. When sequential mode is used, only one control word is needed to transmit a block of data words. When non-sequential mode is used, there must be a control word for each data word that is transmitted or received. 0 – non-sequential transfer	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		1 – sequential transfer	

24.7.1.4 SSI_SLV Transmit FIFO Threshold Level Register(TXFTLR,0x18)

This register controls the threshold value for the transmit FIFO memory. The SSI_SLV is enabled and disabled by writing to the SSIENR register.

	TXFTLR																															Base + 0x18
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										TFT					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect. Read as zero.	R
5:0	TFT	Transmit FIFO Threshold. Controls the level of entries (or below) at which the transmit FIFO controller triggers an interrupt. The FIFO depth is configurable in the range 2-64; this register is sized to the number of address bits needed to access the FIFO. If you attempt to set bits [7:0] of this register to a value greater than or equal to the depth of the FIFO, this field is not written and retains its current value. When the number of transmit FIFO entries is less than or equal to this value, the transmit FIFO threshold interrupt is triggered. For field decode: 00_0000 ssi_txe_intr is asserted when 0 data entries are present in transmit FIFO 00_0001 ssi_txe_intr is asserted when 1 or less data entry are present in transmit FIFO 00_0010 ssi_txe_intr is asserted when 2 or less data entry are present in transmit FIFO 00_0011 ssi_txe_intr is asserted when 3 or less data entry are present in transmit FIFO ..... 11_1110 ssi_txe_intr is asserted when 62 or less data entry are present in transmit FIFO 11_1111 ssi_txe_intr is asserted when 63 or less data entry are present in transmit FIFO	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

24.7.1.5 SSI_SLV Receive FIFO Threshold Level Register(RXFTLR,0x1C)

This register controls the threshold value for the receive FIFO memory. The SSI_SLV is enabled and disabled by writing to the SSIENR register.

	RXFTLR																															Base + 0x1C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										RFT					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect, read as zero.	R
5:0	RFT	Receive FIFO Threshold. Controls the level of entries (or above) at which the receive FIFO controller triggers an interrupt. The FIFO depth is configurable in the range 2-64. This register is sized to the number of address bits needed to access the FIFO. If you attempt to set this value greater than the depth of the FIFO, this field is not written and retains its current value. When the number of receive FIFO entries is greater than or equal to this value + 1, the receive FIFO threshold interrupt is triggered. For field decode: 00_0000 ssi_rxf_intr is asserted when 1 or more data entry is present in receive FIFO 00_0001 ssi_rxf_intr is asserted when 2 or more data entry is present in receive FIFO 00_0010 ssi_rxf_intr is asserted when 3 or more data entry is present in receive FIFO 00_0011 ssi_rxf_intr is asserted when 4 or more data entry is present in receive FIFO ..... 11_1110 ssi_rxf_intr is asserted when 63 or more data entry is present in receive FIFO 11_1111 ssi_rxf_intr is asserted when 64 or more data entry is present in receive FIFO	RW

24.7.1.6 SSI_SLV Transmit FIFO Level Register(TXFLR,0x20)

This register contains the number of valid data entries in the transmit FIFO memory.

	TXFLR																															Base + 0x20
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Reserved																									TXTFL						
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Reserved	R
6:0	TXTFL	Transmit FIFO Level. Contains the number of valid data entries in the transmit FIFO.	R

24.7.1.7 SSI_SLV Receive FIFO Level Register(RXFLR,0x24)

This register contains the number of valid data entries in the receive FIFO memory. This register can be read at any time.

	RXFLR																															Base + 0x24
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																									RXTFL						
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect, read as zero.	R
6:0	RXTFL	Receive FIFO Level. Contains the number of valid data entries in the receive FIFO.	R

24.7.1.8 SSI_SLV Status Register(SR,0x28)

This is a read-only register used to indicate the current transfer status, FIFO status, and any transmission/reception errors that may have occurred. The status register may be read at any time. None of the bits in this register request an interrupt.

	SR																															Base + 0x28
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										TXE	RFF	RFNE	TFE	TFNF	BUSY
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:6	Reserved	Writing has no effect, read as zero.	RW
5	TXE	Transmission Error. Set if the transmit FIFO is empty when a transfer is started. Data from the previous transmission is resent on the txd line. This bit is cleared when read. 0 – No error 1 – Transmission error	R
4	RFF	Receive FIFO Full. When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared. 0 – Receive FIFO is not full 1 – Receive FIFO is full	R
3	RFNE	Receive FIFO Not Empty. Set when the receive FIFO contains one or more entries and is cleared when the receive FIFO is empty. This bit can be polled by software to completely empty the receive FIFO. 0 – Receive FIFO is empty 1 – Receive FIFO is not empty	R
2	TFE	Transmit FIFO Empty. When the transmit FIFO is completely empty, this bit is set. When the transmit FIFO contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt. 0 – Transmit FIFO is not empty 1 – Transmit FIFO is empty	R
1	TFNF	Transmit FIFO Not Full. Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full. 0 – Transmit FIFO is full 1 – Transmit FIFO is not full	R
0	BUSY	SSI_SLV Busy Flag. When set, indicates that a serial transfer is in progress; when cleared indicates that the SSI_SLV is idle or disabled. 0 – SSI_SLV is idle or disabled 1 – SSI_SLV is actively transferring data	R

24.7.1.9 SSI_SLV Interrupt Mask Register(IMR,0x2C)

This read/write register masks or enables all interrupts generated by the SSI_SLV.

	IMR																															Base + 0x2C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											RXFIM	RXOIM	RXUIM	TXOIM	TXEIM

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1

Bits	Name	Description	RW
31:5	Reserved	Writing has no effect, read as zero.	R
4	RXFIM	Receive FIFO Threshold Interrupt Mask 0 – ssi_rxf_intr interrupt is masked 1 – ssi_rxf_intr interrupt is not masked	RW
3	RXOIM	Receive FIFO Overflow Interrupt Mask 0 – ssi_rxo_intr interrupt is masked 1 – ssi_rxo_intr interrupt is not masked	RW
2	RXUIM	Receive FIFO Underflow Interrupt Mask 0 – ssi_rxu_intr interrupt is masked 1 – ssi_rxu_intr interrupt is not masked	RW
1	TXOIM	Transmit FIFO Overflow Interrupt Mask 0 – ssi_txo_intr interrupt is masked 1 – ssi_txo_intr interrupt is not masked	RW
0	TXEIM	Transmit FIFO Threshold Interrupt Mask 0 – ssi_txe_intr interrupt is masked 1 – ssi_txe_intr interrupt is not masked	RW

24.7.1.10 SSI_SLV Interrupt Status Register(ISR,0x30)

This register reports the status of the SSI_SLV interrupts after they have been masked.

	ISR																															Base + 0x30
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										MSTIS	RXFIS	RXOIS	RXUIS	TXOIS	TXEIS
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:5	Reserved	Writing has no effect, read as zero.	R
4	RXFIS	Receive FIFO Threshold Interrupt Status 0 = ssi_rxf_intr interrupt is not active after masking 1 = ssi_rxf_intr interrupt is full after masking	R
3	RXOIS	Receive FIFO Overflow Interrupt Status 0 = ssi_rxo_intr interrupt is not active after masking 1 = ssi_rxo_intr interrupt is active after masking	R
2	RXUIS	Receive FIFO Underflow Interrupt Status 0 = ssi_rxu_intr interrupt is not active after masking	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		1 = ssi_rxu_intr interrupt is active after masking	
1	TXOIS	Transmit FIFO Overflow Interrupt Status 0 = ssi_txo_intr interrupt is not active after masking 1 = ssi_txo_intr interrupt is active after masking	R
0	TXEIS	Transmit FIFO Threshold Interrupt Status 0 = ssi_txe_intr interrupt is not active after masking 1 = ssi_txe_intr interrupt is active after masking	R

24.7.1.11 SSI_SLV Raw Interrupt Status Register(RISR,0x34)

This read-only register reports the status of the SSI_SLV interrupts prior to masking.

	RISR																															Base + 0x34
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											RXFIR	RXOIR	RXUIR	TXOIR	TXEIR
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:6	Reserved	Writing has no effect, read as zero.	R
4	RXFIR	Receive FIFO Threshold Raw Interrupt Status 0 = ssi_rxf_intr interrupt is not active prior to masking 1 = ssi_rxf_intr interrupt is active prior to masking	R
3	RXOIR	Receive FIFO Overflow Raw Interrupt Status 0 = ssi_rxo_intr interrupt is not active prior to masking 1 = ssi_rxo_intr interrupt is active prior masking	R
2	RXUIR	Receive FIFO Underflow Raw Interrupt Status 0 = ssi_rxu_intr interrupt is not active prior to masking 1 = ssi_rxu_intr interrupt is active prior to masking	R
1	TXOIR	Transmit FIFO Overflow Raw Interrupt Status 0 = ssi_txo_intr interrupt is not active prior to masking 1 = ssi_txo_intr interrupt is active prior masking	R
0	TXEIR	Transmit FIFO Threshold Raw Interrupt Status 0 = ssi_txe_intr interrupt is not active prior to masking 1 = ssi_txe_intr interrupt is active prior masking	R

24.7.1.12 SSI_SLV Transmit FIFO Overflow Interrupt Clear Register(TXOICR,0x38)

Transmit FIFO Overflow Interrupt Clear Register

	TXOICR	Base + 0x38

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															TXOICR
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect, read as zero.	R
0	TXOICR	Clear Transmit FIFO Overflow Interrupt .This register reflects the status of the interrupt. A read from this register clears the ssi_txo_intr interrupt; writing has no effect.	R

24.7.1.13 SSI_SLV Receive FIFO Overflow Interrupt Clear Register(RXOICR,0x3C)

Receive FIFO Overflow Interrupt Clear Register

	RXOICR																															Base + 0x3C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															RXOICR
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect, read as zero.	R
0	RXOICR	Clear Receive FIFO Overflow Interrupt. This register reflects the status of the interrupt. A read from this register clears the ssi_rxo_intr interrupt; writing has no effect.	R

24.7.1.14 SSI_SLV Receive FIFO Underflow Interrupt Clear Register(RXUICR,0x40)

Receive FIFO Underflow Interrupt Clear Register

	RXUICR																															Base + 0x40
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Reserved																															RXOICR
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect, read as zero.	R
0	RXUICR	Clear Receive FIFO Underflow Interrupt. This register reflects the status of the interrupt. A read from this register clears the ssi_rxu_intr interrupt; writing has no effect.	R

24.7.1.15 SSI_SLV Interrupt Clear Register(ICR,0x48)

Interrupt Clear Register

	ICR																															Base + 0x48
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															MSTICR
RST	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect, read as zero.	R
0	ICR	Clear Interrupts. This register is set if any of the interrupts below are active. A read clears the ssi_txo_intr, ssi_rxu_intr and ssi_rxo_intr, interrupts. Writing to this register has no effect.	R

24.7.1.16 SSI_SLV DMA Control Register(DMACR,0x4C)

DMA Control Register

The register is used to enable the DMA Controller interface operation.

	DMACR																															Base + 0x4C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														TDMAE	RDMAE
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:2	Reserved	Writing has no effect, read as zero.	R
1	TDMAE	Transmit DMA Enable. This bit enables/disables the transmit FIFO DMA channel. 0 = Transmit DMA disabled 1 = Transmit DMA enabled	RW
0	RDMAE	Receive DMA Enable. This bit enables/disables the receive FIFO DMA channel 0 = Receive DMA disabled 1 = Receive DMA enabled	RW

24.7.1.17 SSI_SLV DMA Transmit Data Level(DMATDLR,0x50)

DMA Transmit Data Level

	DMATDLR																															Base + 0x50
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										DMATDL					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect, read as zero.	R
5:0	DMATDL	Transmit Data Level. This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and TDMAE = 1. For field decode: 00_0000 dma_tx_req is asserted when 0 data entries are present in the transmit FIFO 00_0001 dma_tx_req is asserted when 1 or less data entry is present in the transmit FIFO 00_0010 dma_tx_req is asserted when 2 or less data entries are present in the transmit FIFO 00_0011 dma_tx_req is asserted when 3 or less data entries are present in the transmit FIFO ..... 11_1110 dma_tx_req is asserted when 62 or less data entries are present in the transmit FIFO 11_1111 dma_tx_req is asserted when 63 or less data entries are present in the transmit FIFO	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

24.7.1.18 SSI_SLV DMA Receive Data Level（DMARDLR,0x54)

DMA Receive Data Level

	DMARDLR																															Base + 0x54
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										DMARDL					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect, read as zero.	R
5:0	DMARDL	Receive Data Level. This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or above this field value + 1, and RDMAE=1. For field decode: 00_0000 dma_rx_req is asserted when 1 or more data entries are present in the receive FIFO 00_0001 dma_rx_req is asserted when 2 or more data entries are present in the receive FIFO 00_0010 dma_rx_req is asserted when 3 or more data entries are present in the receive FIFO 00_0011 dma_rx_req is asserted when 4 or more data entries are present in the receive FIFO ..... 11_1110 dma_rx_req is asserted when 63 or more data entries are present in the receive FIFO 11_1111 dma_rx_req is asserted when 64 or more data entries are present in the receive FIFO	RW

24.7.1.19 SSI_SLV Identification Register(IDR,0x58)

Identification Register. This read-only register is available for use to store a peripheral identification code.

	IDR																															Base + 0x58
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ID																															
RST	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:0	ID	Identification Code. This register contains the SSI_SLV's identification code. When read, the value is 0xffffffff.	R

24.7.1.20 SSI_SLV Data Register(DR,0x60)

Data Register. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.

	DR																															Base + 0x60
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:0	DR	Data Register. When writing to this register, you must right-justify the data. Read data are automatically right-justified. Read = Receive FIFO buffer Write = Transmit FIFO buffer	RW

24.8 Software Guideline

24.8.1 Configure Flow

If the SSI_SLV is receive only (TMOD=10), the transmit FIFO need not contain valid data because the data currently in the transmit shift register is reset each time the slave device is selected. The TXE error flag in the status register (SR) is not set when TMOD=01. You should mask the transmit FIFO empty interrupt when this mode is used.

If the SSI_SLV transmits data to the master, you must ensure that data exists in the transmit FIFO before a transfer is initiated by the serial-master device. If the master initiates a transfer to the SSI_SLV when no data exists in the transmit FIFO, an error flag (TXE) is set in the SSI_SLV status register, and the previously transmitted data frame is resent on txd. For continuous data transfers, you must ensure that the transmit FIFO buffer does not become empty before all the data have been transmitted. The transmit FIFO threshold level register (TXFTLR) can be used to early interrupt (ssi_txe_intr) the processor, indicating that the transmit FIFO buffer is nearly empty. When a DMA Controller is used for APB accesses, the DMA transmit data level register (DMATDLR) can be used to early request (dma_tx_req) the

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

DMA Controller, indicating that the transmit FIFO is nearly empty. The FIFO can then be refilled with data to continue the serial transfer.

The receive FIFO buffer should be read each time the receive FIFO generates a FIFO full interrupt request to prevent an overflow. The receive FIFO threshold level register (RXFTLR) can be used to give early indication that the receive FIFO is nearly full. When a DMA Controller is used for APB accesses, the DMA receive data level register (DMARDLR) can be used to early request (dma_rx_req) the DMA controller, indicating that the receive FIFO is nearly full. A typical software flow for completing a continuous serial transfer from a serial master to the SSI_SLV is described as follows:

1. If the SSI_SLV is enabled, disable it by writing 0 to SSIENR.
2. Set up the SSI_SLV control registers for the transfer. These registers can be set in any order.
   a. Write CTRLR0 (for Motorola SPI transfers SCPH and SCPOL must be set identical to the master device).
   b. Write TXFTLR and RXFTLR to set FIFO threshold levels.
   c. Write the IMR register to set up interrupt masks.
3. Enable the SSI_SLV by writing 1 to the SSIENR register.
4. If the transfer mode is transmit and receive (TMOD=2'b00) or transmit only (TMOD=2'b01), write data for transmission to the master into the transmit FIFO (Write DR). If the transfer mode is receive only (TMOD=2'b10), there is no need to write data into the transmit FIFO; the current value in the transmit shift register is retransmitted.
5. The SSI_SLVi slave is now ready for the serial transfer. The transfer begins when the SSI_SLV is selected by a serial-master device.
6. When the transfer is underway, the BUSY status can be polled to return the transfer status. If a transmit FIFO empty interrupt request is made, write the transmit FIFO (write DR). If a receive FIFO full interrupt request is made, read the receive FIFO (read DR).
7. The transfer ends when the serial master removes the select input to the SSI_SLV. When the transfer is completed, the BUSY status is reset to 0.
8. If the transfer mode is not transmit only (TMOD != 01), read the receive FIFO until empty.
9. Disable the SSI_SLV by writing 0 to SSIENR.

NOTE: ssi_slv_dev_clk must be less than or equal to the frequency of pclk; ssi_slv_dev_clk shold be 4 times or more than the ssi_slv_sericlk

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

25 Universal Asynchronous Receiver/Transmitter (UART)

25.1 Overview

This chapter describes the universal asynchronous receiver/transmitter (UART) serial ports. There are two UARTs: All UARTs use the same programming model. Each of the serial ports can operate in interrupt-based mode or DMA-based mode.

The Universal asynchronous receiver/transmitter (UART) is compatible with the 16550-industry standard and can be used as slow infrared asynchronous interface that conforms to the Infrared Data Association (IrDA) serial infrared specification 1.1.

25.2 Features

- Full-duplex operation
- 5-, 6-, 7- or 8-bit characters with optional no parity or even or odd parity and with 1, 1½, or 2 stop bits
- 64x8 bit transmit FIFO and 64x11bit receive FIFO
- Transmission, reception and line status Independently
- Internal diagnostic capability Loopback control and break, parity, overrun and framing-error is provided
- Separate DMA requests for transmit and receive data services in FIFO mode
- Supports modem flow control by software or hardware
- Slow infrared asynchronous interface that conforms to IrDA specification

25.3 Block Diagram

Figure 25-1 UART DATA Controller Block Diagram

As shown in UART DATA Controller Block Diagram，the two part includes receiving data and sending data in UART; From PIN to receive the data processing and put it on the APB bus. For the transmission direction, UART gets the data from the APB bus and sent to the PIN.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

25.4 Functional Description

25.4.1 Full-duplex operation

UART bidirectional communication，can realize full duplex transmission and reception.

25.4.2 The meaning of all bits

1. **start:** first sends a signal to a logic "0", to indicate the beginning of transmission or reception character.
2. **data bit:** after the start bit. data bits can be 5,6,7,8etc, constitute a character. Began to transfer from the lowest.
3. **parity bit:** it is optional and used to check the accuracy of data transmission and reception.
4. **stop bit:** it marks the end of a character data. can be high level 1,1.5,2. stop bit is not only the end of said transmission, and provides computer correction clock synchronization opportunity.
5. **idle bit:** In a logic "1" state, said the current line without data transfer.

25.4.3 RFIFO and TFIFO

TFIFO is 64*8bit transmission FIFO; RFIFO is 64*11bit receiving FIFO. they used to cache data.

The data in the UART registers(temporary memory block), and then through the FIFO transmitted to the serial device, without the FIFO, the information will become be, may not transfer to Modem.

25.4.4 Transmission, reception and line status Independently

Independently controlled transmit, receive (data ready or timeout), line status interrupts

25.4.5 Slow infrared asynchronous interface

UART also contains a IrDA serial infrared(SIR) encoder/decoder module. IrDA SIR module is used to convert between asynchronous UART data stream and a half duplex serial SIR interface. The SIR module's task is to give the UART to provide a digital output code and a decoding input . UART signal pin and a infrared transceiver connected to implement IrDA SIR physical layer connection.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

25.5 Pins Description

Table 25-1 UART Pins Description

Name	Type	Description
RxD	Input	Receive data input
TxD	Output	Transmit data output
CTS_	Input	Clear to Send --- Modem Transmission enabled
RTS_	Output	Request to Send --- UART Transmission request

NOTE:UART0/UART2 support RxD, TxD, RTS_, CTS_, UART1/UART3 support RxD, TxD.

25.6 Data Format Description

Figure 25-2 UART Frame Structure Diagram

As shown in UART Frame Structure Diagram, the frame data from left to right transmission. The start bit and parity bit are all 1bit; Data bits and stop bits can be changed, so data bits range is 5bit to 8bit; stop bits range is 1bit ,1.5bit and 2bit;

25.7 Register Description

Following chapter will describe the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. Register read/write attribute
   R- Read only
   W- Write only
   RW- Read and Write
   RCW- Read and Write, but Clear to 0 by Read
   RSW- Read and Write, but Set to 1 by Read
   RWC- Read and Write, Clear to 0 by Write 1, Write 0 has no effect
   RWS- Read and Write, Set to 1 by Write 1, Write 0 has no effect
   RC- Read only, and Clear to 0 by read
   RS- Read only, and Set to 1 by read
3. Reset Value
   1 - reset to 1
   0 - reset to 0
   ? - value unknown after reset

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

25.7.1 Register Memory Map

There are 3 UART controllers in chip, name UART0, UART1, UART2 respectively. The base address of UARTS(s) as follows:

Table 25-2 Registers Memory Map Base Address

Name	Base	Description
UART0	0x10030000	Address base of UART 0
UART1	0x10031000	Address base of UART 1
UART2	0x10032000	Address base of UART 2
UART3	0x10033000	Address base of UART 3

The UART is controlled by a set of registers that the application configures before every operation. The following table lists all the registers.

Table 25-3 UART Registers Map

Name	RW	Reset Value	Address Offset	Access Size
URBR	R	0x000000??	0x00	32
UTHR	W	0x000000??	0x00	32
UDLLR	RW	0x00000000	0x00	32
UDLHR	RW	0x00000000	0x04	32
UIER	RW	0x00000000	0x04	32
UIIR	R	0x00000001	0x08	32
UFCR	W	0x00000000	0x08	32
ULCR	RW	0x00000000	0x0C	32
UMCR	RW	0x00000000	0x10	32
ULSR	R	0x00000060	0x14	32
UMSR	R	0x00000000	0x18	32
USPR	RW	0x00000000	0x1C	32
ISR	RW	0x00000000	0x20	32
UMR	RW	0x00000000	0x24	32
UACR	RW	0x00000000	0x28	32
URCR	R	0x000000??	0x40	32
UTCR	R	0x000000??	0x44	32
URFCR	RW	0x0000002C	0x48	32
URTDCR	RW	0x00000000	0x50	32

25.7.2 Register and Fields Description

25.7.2.1 UART Receive Buffer Register(URBR,0x00)

The read-only URBR is corresponded to one level 11bit buffer in non-FIFO mode and a 32x11bit FIFO that holds the character(s) received by the UART. Bits in URBR are right justified when being configured to use fewer than eight bits, and the rest of most significant

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

data bits are zeroed and the most significant three bits of each buffer are the status for the character in the buffer. If ULSR.DRY is 0, don't read URBR, otherwise wrong operation may occur.

	URBR																															Base + 0x00
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								URBR							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect. Read as zero.	R
7:0	URBR	8-bit UART receive read data.	R

NOTE:

The URBR register is valid when *ULCR* register's field DLAB = 0 and CPU to request read operation.

25.7.2.2 UART Transmit Hold Register(UTHR,0x00)

The write-only UTHR is corresponded to one level 8 bit buffer in non-FIFO mode and a 32x8bit FIFO in FIFO mode that holds the data byte(s) to be transmitted next.

	UTHR																															Base + 0x00
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								UTHR							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect. Read as zero.	R
7:0	UTHR	8-bit UART transmit write hold data.	W

NOTE:

The UTHR register is valid when *ULCR* register's field DLAB = 0 and cpu to request writing operation.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

25.7.2.3 UART Divisor Latch Low Register (UDLLR,0x00)

UART Divisor Latch registers, *UDLLR* or *UDLHR* together compose the divisor for the programmable baud rate generator that can take the UART device clock and divide it by 1 to (2^{16} – 1).

The UART device source clock is EXCLK. *UDLHR* or *UDLLR* stores the high/low 8-bit of the divisor respectively. Load these divisor latches during initialization to ensure that the baud rate generator operates properly. If both Divisor Latch registers are 0, the 16X clock stops.

If you don't set *UMR* and *UACR*, UART will work at normal mode with the specified frequency. The relationship between baud rate and the value of Divisor is shown by the formula when *UMR* and *UACR* are not set:

Baud Rate = (UART device clock) / (16 * **Divisor**)

	UDLLR																															**Base + 0x00**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								DLL_8bit							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect. Read as zero.	R
7:0	DLL_8bit	Low 8-bit divisor Latch	RW

NOTE:

1. [1]: clock control module for clock tree generate
2. The *UDLLR* register is valid when *ULCR* register's field DLAB = 1;

25.7.2.4 UART Divisor Latch High Register (UDLHR,0x04)

The interpretation of the same with *UDLLR*.

	UDLHR																															**Base + 0x04**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								DLH_8bit							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect. Read as zero.	R
7:0	DLH_8bit	high 8-bit divisor Latch	RW

NOTE:

The *UDLHR* register is valid when *ULCR* register's field DLAB = 1.

25.7.2.5 UART Interrupt Enable Register (UIER,0x04)

The UART Interrupt Enable Register (UIER) contains the interrupt enable bits for the five types of interrupts (receive data ready, timeout, line status, and transmit data request, and modem status) that set a value in *UIIR*.

	UIER																															Base + 0x04
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										RETOIE	RTOIE	MSIE	RLSIE	TDRIE	RDRIE
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:6	Reserved	Writing has no effect, read as zero.	R
5	RETOIE	**Receive Fifo Empty Timeout Interrupt Enable.** 0: Disable the receive fifo empty timeout interrupt 1: Enable the receive fifo empty timeout interrupt Timeout means the *URCR* (FIFO mode) has been empty but for a period of time URFCR.ETO_CNT.	RW
4	RTOIE	**Receive Timeout Interrupt Enable.** 0: Disable the receive timeout interrupt 1: Enable the receive timeout interrupt Timeout means the *URCR* (FIFO mode) is not empty but no character has received for a period of time T: T (bits) = 4 X Word length + 12.	RW
3	MSIE	**Modem Status Interrupt Enable.** 0: Disable the modem status interrupt 1: Enable the modem status interrupt	RW
2	RLSIE	**Receive Line Status Interrupt Enable.** 0: Disable receive line status interrupt 1: Enable receive line status interrupt	RW
1	TDRIE	**Transmit Data Request Interrupt Enable.**	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		0: Disable the transmit data request interrupt 1: Enable the transmit data request interrupt	
0	RDRIE	**Receive Data Ready Interrupt Enable.** 0: Disable the receive data ready interrupt 1: Enable the receive data ready interrupt	RW

NOTE: The UIER register is valid when *ULCR* register's field DLAB = 0;

25.7.2.6 UART Interrupt Identification Register (UIIR,0x08)

The read-only UART Interrupt Identification Register (UIIR) records the prioritized pending interrupt source information. Its initial value after power-on reset is 0x01.

	UIIR																															**Base + 0x08**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								FFMSEL		Reserved		INID			INPEND
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect. Read as zero.	R
7:6	FFMSEL	**FIFO Mode Select.** 0b00: Non-FIFO mode 0b01: Reserved 0b10: Reserved 0b11: FIFO mode	R
5:4	Reserved	Writing has no effect Read as zero.	R
3:1	INID	**Interrupt Identifier.** These bits identify the current highest priority pending interrupt. *See Table 25-4 for details.*	R

INID	Description
0b000	Modem Status
0b001	Transmit Data Request
0b010	Receive Data Ready
0b011	Receive Line Status
0b100	Reserved
0b101	Receive Empty Time Out
0b110	Receive Time Out
0b111	Reserved

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

0	INPEND	**Interrupt Pending.** 0: interrupt is pending 1: No interrupt pending	R

Table 25-4 UART Interrupt Identification Register Description

UIIR.INID	Interrupt Set/Clear Cause			
	Priority	**Type**	**Source**	**Clear Condition**
0b0001	-	None	No pending interrupt	-
0b0110	1st Highest	Receive Line Status	Overrun, Parity, Frame Error, Break Interrupt, and FIFO Error (DMA mode only)	Reading *ULSR* or empty all the error characters in DMA mode
0b0100	2nd Highest	Receive Data Ready	FIFO mode: Trigger threshold was reached Non-FIFO mode: *URBR* full	FIFO mode: Reading *URBR* till below trigger threshold. Non-FIFO mode: Empty *URBR*
0b1010	2nd Highest	Receive fifo Empty	FIFO mode only	Clear by read.
0b1100	2nd Highest	Receive Timeout	FIFO mode only: *URBR* not empty but no data read in for a period of time	Reset receive buffer by setting *UFCR.RFRT* to 1 or Reading *URBR*
0b0010	3rd Highest	Transmit Data Request	FIFO mode: Empty location in *UTHR* equal to half or more than half Non-FIFO mode: *UTHR* empty	FIFO mode: Data number in *UTHR* more than half Non-FIFO mode: Writing *UTHR*
0b0000	4th Highest	Modem Status	Modem CTS_ pin status change	Reading *UMSR*

25.7.2.7 UART FIFO Control Register (UFCR,0x08)

The write-only register UFCR contains the control bits for receive and transmit FIFO.

	UFCR																															**Base + 0x08**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								RDTR		Reserved	UME	DME	TFRT	RFRT	FME
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect. Read as zero.	R
7:6	RDTR	**Receive Buffer Data Number Trigger.** These bits are used to select the trigger level for the receive data ready interrupt in FIFO mode. 0b00: 1 0b01: 8 0b10: 16 0b11: 32 Note: When enable DMA Mode, RDTR set 0b10 (16).	W
5	Reserved	Writing has no effect, read as zero.	R
4	UME	**UART Module Enable.** 0: Disable UART 1: Enable UART	W
3	DME	**DMA Mode Enable.** 0: Disable DMA mode 1: Enable DMA mode	W
2	TFRT	**Transmit Holding Register Reset.** 0: Not reset 1: Reset transmit FIFO	W
1	RFRT	**Receive Buffer Reset.** 0: Not reset 1: Reset receive FIFO	W
0	FME	**FIFO Mode Enable.** Set this bit before the trigger levels. 0: non-FIFO mode 1: FIFO mode	W

25.7.2.8 UART Line Control Register (ULCR,0x0C)

The ULCR defines the format for UART data transmission.

	ULCR																															Base + 0x0C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								DLAB	SBK	STPAR	PARM	PARE	SBLS	WLS	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

31:8	Reserved	Writing has no effect. Read as zero.	R
7	DLAB	**Divisor Latch Access Bit.** 0: Enable to access *URBR*, *UTHR* or *UIER* 1: Enable to access *UDLLR* or *UDLHR*	RW
6	SBK	**Set Break.** Causes a break condition (at least one 0x00 data) to be transmitted to the receiving UART. Acts only on the TXD pin and has no effect on the transmit logic. 0: No effect on TXD output 1: Forces TXD output to 0	RW
5	STPAR	**Sticky Parity.** Setting this bit forces parity location to be opposite of PARM bit when PARE is 1 (it is ignored when PARE is 0). 0: Disable Sticky parity 1: Enable Sticky parity (opposite o f PARM bit)	RW
4	PARM	**Parity Odd/Even Mode Select.** If PARE = 0, PARM is ignored. 0: Odd parity 1: Even parity	RW
3	PARE	**Parity Enable.** Enables a parity bit to be generated on transmission or checked on reception. 0: No parity 1: Parity	RW
2	SBLS	**Stop Bit Length Select.** Specifies the number of stop bits transmitted and received in each character. When receiving, the receiver checks only the first stop bit. 0: 1 stop bit 1: 2 stop bits, except for 5-bit character then 1-1/2 bits	RW
1:0	WLS	**Word Length Select.** 0b00: 5-bit character 0b01: 6-bit character 0b10: 7-bit character 0b11: 8-bit character	RW

25.7.2.9 UART Modem Control Register (UMCR,0x10)

The UMCR uses the modem control pins RTS_ and CTS_ to control the interface with a modem or data set. UMCR also controls the loopback mode. Loopback mode must be enabled before the UART is enabled.

	UMCR	**Base + 0x10**

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								MDCE	FCM	Reserved	LOOP	Reserved		RTS	Reserved
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect. Read as zero.	R
7	MDCE	**Modem Control Enable.** 0: Modem function is disabled 1: Modem function is enabled	RW
6	FCM	**Flow Control Mode.** 0: Flow control by software 1: Flow control by hardware	RW
5	Reserved	Writing has no effect Read as zero.	R
4	LOOP	**Loop Back.** This bit is used for diagnostic testing of the UART. When LOOP is 1, TXD output pin is set to a logic 1 state, RXD is disconnected from the pin, and the output of the transmitter shifter register is looped back into the receiver shift register input internally, similar to CTS_ and RTS_ pins and the RTS bit of the *UMCR* is connected to CTS bit of *UMSR* respectively. Loopback mode must be selected before the UART is enabled. 0: Normal operation mode 1: Loopback-mode UART operation	RW
3:2	Reserved	Writing has no effect Read as zero.	R
1	RTS	**Request To Send.** This bit can control the RTS_ output state. 0: RTS_ force to high 1: RTS_ force to low	RW
0	Reserved	Writing has no effect. Read as zero.	R

25.7.2.10 UART Line Status Register (ULSR,0x14)

The read-only ULSR indicates status information during the data transfer. Receive error information in ULSR[4:1] remains set until software reads ULSR and it must be read before the error character is read.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	ULSR																															Base + 0x14
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								FIFOE	TEMP	TDRQ	BI	FMER	PARER	OVER	DRY
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect. Read as zero.	R
7	FIFOE	**FIFO Error Status. (FIFO mode only)** FIFOE is set when there is at least one kind of receive error (parity, frame, overrun, break) for any of the characters in receive buffer. FIFOE is reset when all error characters are read out of the buffer. During DMA transfer, the error interrupt generates when FIFOE is 1, and no receive DMA request generates even when data in receive buffer reaches the trigger threshold until all the error characters are read out. In non-DMA mode, FIFOE set does not generate error interrupt. 0: No error data in receive buffer or non-FIFO mode 1: One or more error character in receive buffer	R
6	TEMP	**Transmit Holding Register Empty.** Set when both *UTHR* and shift register are empty. It is cleared when either the *UTHR* or the shift register contains a data character. 0: There is data in the transmit shifter and *UTHR* 1: All the data in the transmit shifter and *UTHR* has been shifted out	R
5	TDRQ	**Transmit Data Request.** Set when *UTHR* has half or more empty location (FIFO mode) or empty (non-FIFO mode). When both *UIER.TDRIE* and TDRQ are 1, transmit data request interrupt generates or during DMA transfer, DMA request to the DMA controller generates when *UIER.TDRIE* is 0 and TDRQ is 1. 0: There is one (non-FIFO mode) or more than half data (FIFO mode) in *UTHR* 1: None data (non-FIFO mode) or half or less than half data (FIFO mode) in *UTHR*	R
4	BI	**Break Interrupt.** BI is set when the received data input is held low for longer than a full-word transmission time (the total time of start bit + data bits + parity bit + stop bits). BI is cleared when the processor reads the ULSR. In FIFO mode, only one character equal to 0x00 is loaded into the FIFO regardless of the	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		length of the break condition. BI shows the break condition for the character at the front of the FIFO, not the most recently received character. 0: No break signal has been received 1: Break signal received	
3	FMER	**Framing Error.** Set when the bit following the last data bit or parity bit is detected to be 0. If the *ULCR* had been set for two or one and half stop bits, the other stop bits are not checked except the first one. In FIFO mode, FMER shows a framing error for the character at the front of the receive buffer, not for the most recently received character. Cleared when the processor reads the ULSR register. 0: No framing error 1: Invalid stop bit has been detected	R
2	PARER	**Parity Error.** Indicates that the received data character does not have the correct even or odd parity, as selected by the even parity select bit. PARER is set upon detection if a parity error and is cleared when the processor reads the ULSR register. In FIFO mode, PARER shows a parity error for the character at the front of the FIFO, not the most recently received character. 0: No parity error 1: Parity error has occurred	R
1	OVER	**Overrun Error.** Set when both receive buffer and shifter are full and new data is received which will be lost. Cleared when the processor reads the ULSR register. 0: No data has been lost 1: Receive data has been lost	R
0	DRY	**Data Ready.** Set when a complete incoming character has been received into the Receive Buffer registers. DRY is cleared when the receive buffer is read (non-FIFO mode) or when the buffer is empty or when the buffer is reset by setting *UFCR.RFRT* to 1. 0: No data has been received 1: Data is available in *URBR*	R

25.7.2.11 UART Modem Status Register (UMSR,0x18)

The read-only UMSR provides the current state of the control lines from the modem to the processor. They are cleared when the processor reads UMSR.

	UMSR																															**Base + 0x18**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Reserved																											CTS	Reserved			CCTS
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:5	Reserved	Writing has no effect. Read as zero.	R
4	CTS	**Status of Clear To Send.** When MDCE bit is 1, this bit is the complement of CTS_ input. If Loop bit of *UMCR* is 1, this bit is equivalent to RTS bit of *UMCR*. 0: CTS_ pin is 1 1: CTS_ pin is 0	R
3:1	Reserved	Writing has no effect, read as zero.	R
0	CCTS	**Change status of CTS_.** When MDCE bit is 1, this bit indicates the state change on CTS_ pin. 0: No state change on CTS_ pin since last read of UMSR 1: A change occurs on the state of CTS_ pin	R

25.7.2.12 UART Scratchpad Register(USPR,0x1C)

This Scratchpad register is used as a scratch register for the programmer and has no effect on the UART.

	USPR																																Base + 0x1C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								STCH_D							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect Read as zero.	R
7:0	STCH_D	Be scratched data	RW

25.7.2.13 Infrared Selection Register (ISR,0x20)

The ISR is used to configure the slow-infrared (SIR) interface that is provided in each UART to

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

support two-way wireless communication using infrared transmission that conforms to the IrDA serial infrared specification 1.1. The maximum frequency is up to 115.2kbps.

	ISR																															Base + 0x20
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											RDPL	TDPL	XMODE	RCVEIR	XMITIR
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:5	Reserved	Writing has no effect. Read as zero.	R
4	RDPL	**Receive Data Polarity.** 0: Slow-infrared (SIR) interface decoder takes positive pulses as zeros 1: SIR decoder takes negative pulses as zeros	RW
3	TDPL	**Transmit Data Polarity.** 0: SIR encoder generates a positive pulse for a data bit of zero 1: SIR encoder generates a negative pulse for a data bit of zero	RW
2	XMODE	**Transmit Pulse Width Mode.** Set when the transmit encoder needs to generate 1.6us pulses (that are 3/16 of a bit-time at 115.2 kbps). Cleared when the transmit encoder needs to generate 3/16 of a bit-time wide according to current baud rate. 0: Transmit pulse width is 3/16 of a bit-time wide 1: Transmit pulse width is 1.6 us	RW
1	RCVEIR	**Receiver SIR Enable.** This bit is used to select the signal from the RXD pin is processed by the IrDA decoder before it is fed to the UART (RCVEIR = 1) or bypass IrDA decoder and is fed directly to the UART (RCVEIR = 0). 0: Receiver is in UART mode 1: Receiver is in SIR mode	RW
0	XMITIR	**Transmitter SIR Enable.** This bit is used to select TXD output pin is processed by the IrDA encoder before it is fed to the device pin (XMITIR = 1) or bypass IrDA encoder and is fed directly to the device pin (XMITIR = 0). **NOTE:** disable infrared LED before XMITIR is set, otherwise a false start bit may occur. 0: Transmitter is in UART mode 1: Transmitter is in SIR mode	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

25.7.2.14 UART M Register (UMR, 0x24)

It will take UART at least M cycles to transmit or receive one bit.

It will take UART at most M+1 cycles to transmit or receive one bit.

	UMR																															Base + 0x24
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											M				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:5	Reserved	Writing has no effect. Read as zero.	R
4:0	M	The value of UMR register.	RW

25.7.2.15 UART Add Cycle Register (UACR,0x28)

It controls time that UART need to transmit or receive the nth bit of the data.

	UACR																															Base + 0x28
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				AC											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:12	Reserved	Writing has no effect, read as zero.	R
11:0	AC	If the nth bit of the register is： 12'h1：it will take UART M+1 cycles to transmit or receive the bit of data; 12'h0：it will take UART M cycles to transmit or receive the bit of data For except; 12'h0: it will take UART M cycles to transmit or receive one bit of data; 12'hFFF: it will take UART M+1 cycles to transmit or receive one bit of data;	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

25.7.2.16 UART RXFIFO Counter Register (URCR,0x40)

Indicates there are n data in RXFIFO.

	URCR																															Base + 0x40
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																									RCNT						
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:7	Reserved	Writing has no effect, read as zero.	R
6:0	RCNT	RXFIFO Counter. Indicates there are n data in RXFIFO when this field is n.	R

25.7.2.17 UART TXFIFO Counter Register (UTCR,0x44)

Indicates there are n data in TXFIFO

	UTCR																															Base + 0x44
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																									TCNT						
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:7	Reserved	Writing has no effect, read as zero.	R
6:0	TCNT	TXFIFO Counter. Indicates there are n data in TXFIFO when this field is n.	R

25.7.2.18 UART RXFIFO Control Register (URFCR,0x48)

	URFCR																															Base + 0x48
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								Reserved	ETO_CNT						
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect, read as zero.	R
7	Reserved	Writing has no effect, read as zero.	R
6:0	ETO_CNT	RXFIFO Empty Timeout Count. At least 1.	RW

25.7.2.19 UART Separate RX/TX DMA Register (URTDCR,0x50)

	URTDCR																															Base + 0x50
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								RTD_EN						RTD_R	RTD_T
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect, read as zero.	R
7	RTD_EN	Sparate receive and transmit dma control enable	RW
6:2	Reserved	Writing has no effect, read as zero.	R
1	RTD_R	Enable receive dma	RW
0	RTD_T	Enable transmit dma.	RW

25.8 Operation Flow

The following sections describe the UART operations that include flow of configuration, data transmission, data reception, and Infrared mode.

25.8.1 UART Configuration

Before UART starts to transfer data or changing transfer format, configuration must be done to define the transfer format. The sample flow is as the following:

In FIFO mode, set *UFCR.FME* to 1, reset receive and transmit FIFO, then initialize the UART as described below:

1. Clear *UFCR.UME* to 0.
2. Set value in *UDLLR* and *UDLHR* to generate the baud rate clock.
3. Set data format in *ULCR*.
4. If it is in FIFO MODE, set FME bit and other FIFO control in *UFCR*, reset receive and transmit FIFO, otherwise skip item 4.
5. Set each interrupt enable bit in *UIER* in interrupt-based transfer or set *UFCR.DME* in

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

DMA-based transfer (DMA transfer is FIFO mode only), then set *UFCR.UME*.

25.8.2 Data Transmission

After configuration, UART is ready for data transfer. For data transmission, refer to the following procedure:

1. Read *ULSR.TDRQ* (interrupt disable) or wait for transmit data request interrupt (interrupt enable), if *ULSR.TDRQ* = 1 or transmit data request interrupt generates, that means there is enough empty location in *UTHR* for new data.
2. If *ULSR.TDRQ* is 1 or get the transmit data request interrupt, write transmit data to *UTHR* to start transmission.
3. Do item 1 and item 2 if there are more data waiting for transmit.
4. After all necessary data are written to *UTHR*, wait *ULSR.TEMP* = 1, that means all data completely transmitted.
5. If it is necessary to send break, set *ULCR.SBK* and at least wait for 1-bit interval time to send a valid break, then clear *ULCR.SBK*.
6. Clear *UFCR.UME* bit to finish UART transmission.

25.8.3 Data Reception

After configuration, UART is ready for data transfer. For data reception, refer to the following sample procedure:

1. Read *ULSR.DRY* (interrupt disable) or wait for receive data request interrupt (interrupt enable), if *ULSR.DRY* =1 or receive data request interrupt generates, that means *URBR* has one data (non-FIFO mode) or data in *URBR* reaches the trigger value. (FIFO mode)
2. If *ULSR.DRY* = 1 or receive data request interrupt generates, then read *ULSR.FIFOE* or see if there is error interrupt, if *ULSR.FIFOE* = 1, it means received data has receive error, then go to error handler, other wise go to item 3.
3. Read one received data in *URBR* (non-FIFO mode) or data equal to trigger value in *URBR*. (FIFO mode)
4. Check whether all data received: check whether *ULSR.DRY* = 0, in FIFO mode and interrupt is enabled, timeout interrupt may generate, when timeout interrupt generates, read *URBR* till *ULSR.DRY* = 0.
5. Clear *UFCR.UME* to end data reception when all data are received and *ULSR.DRY* = 0.

25.8.4 Receive Error Handling

A sample error handling flow is as the following:

1. If *ULSR.FIFOE* = 1, it means there is receive error in received data, then check what error it is.
2. If *ULSR.OVER* = 1, go to OVER error handling.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

3 If *ULSR.BI* = 1, go to Break handling.
4 If *ULSR.FMER* = 1, go to Frame error handling.
5 If *ULSR.PARER* = 1, go to PARER error handling.

25.8.5 Modem Transfer

When *UMCR.MDCE* = 1, modem control is enabled. Transfer flow can be stopped and restarted by software through RTS_ and CTS_ pin. When UART transmitter detects low level on CTS_ pin, it stops transmission and TxD pin goes to mark state after finishing transmitting the current character until it detects CTS_ pin goes back to high level. RTS_ pin is output to receiving UART and its state can be controlled by setting *UMCR.RTS* bit, that is, setting *UMCR.RTS* to 1, RTS_ pin is low level output that means UART is ready to receive data, on the contrary, it means UART currently can't receive more data.

25.8.6 DMA Transfer

UART can operate in DMA-based (*UFCR.DME* = 1, FIFO mode only), that is, DMA request initiated by UART takes the place of interrupt request and transmission/reception is carried out using DMA instead of CPU. Be sure that software guarantee to disable transmit and receive interrupt except timeout and error interrupts.

During DMA transfer, if an interrupt occurs, software must first read the *ULSR* to see if an error interrupt exists, then check the *UIIR* for the source of the interrupt, then disable DMA channel and read out all the error data from receive FIFO. Software re-set and re-enable DMA and data transfer by DMA will re-start.

If Receive Empty Time Out interrupt exists, read DMA DDA and DTC register， get current transfer location.

25.8.7 Slow IrDA Asynchronous Interface

Each UART supports slow infra-red (SIR) transmission and reception by setting *ISR.XMITIR* and *ISR.RCVEIR* to 1 (make sure the two bits are not set to 1 at the same time because SIR can't operate full-duplex). According to the IrDA 1.1, data rate is limited at a maximum value of 115.2Kbps.

In SIR transmit mode, the transmit pulse comes out at a rate of 3/16 (when the transmit data bit is zero); in SIR receive mode, the receiver must detect the 3/16 pulsed period to recognize a zero value (an active high or low pulse is demodulation to 0, and no pulse is demodulation to 1).

Compared to normal UART, there are some limitations to SIR, that is, each character is fixed to 8-bit data width, no parity and 1 stop bit and modem function is ignored. The IrDA 1.1 specifies

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

a minimum 10ms latency after an optical node ceases transmitting before its receiver recovers its receiving function and software must guarantee this delay.

In the IrDA 1.1 specification, communication must start up at the rate of 9600bps, but then allows the link to negotiate higher (or lower) data rates if supported by both ends. However, the communication rate will not automatically change. Change, if necessary, is performed by software.

25.8.8 For any frequency clock to use the UART

NOTE: if you don't set M register and *UACR* the UART work at normal mode with the specified frequencies. To use other frequency you should to set M register and *UACR* to right value.

1 The Improving

Following changes are made:

a One bit is composed by M CLK_{BR} cycles, which can be 4~1024.

b Some extra CLK_{BR} cycles can be inserted in some bits in one frame, so that like M has fraction.

For instance:

$CLK_{BR} = CLK_{DEV} / N$ N = 1, 2, …

$CLK_{BR} = CLK_{DEV} = 4MHz$

Band rate = 460800

In accurate

$M_a = 8.681$

We take

M = 8, with 8 extra cycles in every frame

A 12-bit register is used to indicate where to insert the extra cycles.

The first line is the time expected

The second line is the time actual

The third line is the time error

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

For transmission, in theory, the biggest error is half of CLK_{BR} cycle, which is 0.125us here.

2 To set UMR register

$CLK_{BR} = CLK_{DEV} / N$

$M_a = CLK_{BR}$/band rate

M is modem of M_a.

Write M to M register.

Considering the power and the robust quality, for M form 6 to 32 is you better select by set the UDLR.

The max error

$$\frac{0.5/CLK_{BR}}{M_a/CLK_{BR}} = 0.5/M_a < 0.5/M$$

M	4	8	16	32	64
error/W_{bit}	12.5%	6.25%	3.125%	1.56%	0.78%

3 To set UACR value

For each bit of it means:

0: means not to add additional cycle to the bit that UART is prepare to transmit or receive, in another word, you will to use M cycles to transmit or receive the bit

1: means to add additional cycle to the bit that UART is prepare to transmit or receive, in another word, you will to use M+1 cycles to transmit or receive the bit

To set *UACR* value you must ensure that the max error of each bit should be less than $0.5P_{BR}$.

For example: M_a-M =0.15; M+1-M_a=0.85;

Write 8 to *UMR*,

Write 0x408 to *UACR*

cycle/bit :	M,	M,	M,	M+1,	M,	M,	M,	M,	M,	M,	M+1,	M
UACR :	0	0	0	1	0	0	0	0	0	0	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

26 MMC/SD CE-ATA Controller(MSC)

26.1 Overview

The Multi Media Card (MMC) is a universal low cost mass storage and communication media that is designed to cover a wide area of applications such as electronic toys, organizers, PDAs, smart phones, and so on.

The Secure Digital (SD) card is an evolution of MMC. It is specifically designed to meet the security, capacity, performance, and environmental requirements inherent in newly emerging audio and video consumer electronic devices. The physical form factor, pin assignment, and data transfer protocol are forward compatible with the Multi Media Card with some additions. An SD card can be categorized as SD memory or SD I/O card, commonly known as SDIO. A memory card invokes a copyright protection mechanism that complies with the security of the SDMI standard and is faster and capable of higher memory capacity. The SDIO card provides high-speed data I/O with low-power consumption for mobile electronic devices.

For CE-ATA detail protocol , please referred to WWW.CE-ATA.ORG.

26.2 Features

- Fully compatible with the MMC System Specification version 4.2
- Support SD Specification 2.0
- Support SD I/O Specification 2.0 with 1 command channel and 4 data channels
- Maximum data rate is 50MBps
- Support MMC data width 1bit ,4bit
- Built-in programmable frequency divider for MMC/SD bus
- Built-in Special Descriptor DMA
- Multi-SD function support including multiple I/O and combined I/O and memory
- IRQ supported enable card to interrupt MMC/SD controller
- Single or multi block access to the card including erase operation
- Stream access to the MMC card
- Supports SDIO read wait, interrupt detection during 1-bit or 4-bit access
- Supports CE-ATA digital protocol commands
- Support Command Completion Signal and interrupt to CPU
- Command Completion Signal disable feature
- The maximum block length is 4096bytes

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

26.3 Block Diagram

Figure 26-1 MMC/SD Controller Block Diagram

26.4 Functional Description

All communication between system and cards is controlled by the MSC. The MSC sends commands of two type: broadcast and addressed (point-to-point) commands.

Broadcast commands are intended for all cards, command like “Go_Idle_State”, “Send_Op_Cond”, “All_Send_CID” and “Set_Relative_Addr” are using way of broadcasting. During Broadcast mode, all cards are in open-drain mode, to avoid bus contention.

After Broadcast commands “Set_Relative_Addr” issue, cards are enter standby mode, and Addressed command will be used from now on, in this mode, CMD/DAT will return to push-pull mode, to have maximum driving for maximum operation frequency.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

The MMC and the SD are similar product. Besides the 4x bandwidth and the built-in encryption, they are being programmed similarly.

The MMC/SD controller (MSC) is the interface between the software and the MMC/SD bus. It is responsible for the timing and protocol between the software and the MMC/SD bus. It consists of control and status registers, a 16-bit response FIFO that is 8 entries deep, and one 32-bit receive/transmit data FIFOs that are 16 entries deep. The registers and FIFOs are accessible by the software.

MSC also enable minimal data latency by buffering data and generating and checking CRCs.

26.4.1 MSC Reset

The MMC/SD controller (MSC) can be reset by a hardware reset or software reset. All registers and FIFO controls are set to their default values after any reset.

26.4.2 Voltage Validation

All cards shall be able to establish communication with the host using any operation voltage in the maximal allowed voltage range specified in this standard. However, the support minimum and maximum values for Vdd are defined in Operation Conditions register (OCR) and many not cover the whole range. Cards that store the CID and CSD data in the payload memory would be able to communicate these information only under data transfer Vdd conditions. That means if host and card have non compatible Vdd ranges, the card will not be able to complete the identification cycle, nor to send CSD data.

Therefore, a special command Send_Op_Cont (CMD1 for MMC), SD_Send_Op_Cont (CMD41 for SD Memory) and IO_Send_Op_Cont (CMD5 for SDIO) are designed to provide a mechanism to identify and reject cards which do not match the Vdd range desired by the host. This is accomplished by the host sending the required Vdd voltage window as the operand of this command. Cards which can not perform data transfer in the specified range must discard themselves from further bus operations and go into Inactive State. By omitting the voltage range in the command, the host can query each card and determine the common voltage range before sending out-of-range cards into the Inactive State. This query should be used if the host is able to select a common voltage range or if a notification to the application of non usable cards in the stack is desired.

26.4.3 Card Registry

Card registry on MMC and SD card are different.

For SD card, Identification process start at clock rate Fod, while CMD line output drives are push-pull drivers instead of open-drain. After the bus is activated the host will request the

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

cards to send their valid operation conditions. The response to ACMD41 is the operation condition register of the card. The same command shall be send to all of the new cards in the system. Incompatible cards are sent into Inactive State. The host then issue the command All_Send_CID (CMD2) to each card and get its unique card identification (CID) number. Card that is unidentified, that is, which is in Ready State, send its CID number as the response. After the CID was sent by the card it goes into Identification State. Thereafter, the host issues Send_Relative_Addr (CMD3) asks the card to publish a new relative card address (RCA), which is shorter that CID and which will be used to address the card in the future data transfer mode. Once the RCA is received the card state changes to the Stand-by State. At this point, if the host wants that the card will have another RCA number, it may ask the card to publish a new number by sending another Send_Relative_Addr command to the card. The last published RCA is the actual RCA of the card. The host repeats the identification process, that is, the cycles with CMD2 and CMD3 for each card in the system.

In MMC, the host starts the card identification process in open-drain mode with the identification clock rate Fod. The open drain driver stages on the CMD line allow parallel card operation during card identification. After the bus is active the host will request the cards to send their valid operation conditions (CMD1). The response to CMD1 is the 'wired or' operation on the condition restrictions of all cards in the system. Incompatible cards are sent into Inactive State. The host then issues the broadcast command All_Send_CID (CMD2), asking all cards for their unique card identification (CID) number. All unidentified cards, that is, those which are in Ready State, simultaneously start sending their CID numbers serially, while bit-wise monitoring their outgoing bit-stream. Those cards, whose outgoing CID bits do not match the corresponding bits on the command line in any one of the bit periods stop sending their CID immediately and must wait for the next identification cycle. Since CID is unique for each card, only one card can be successfully send its full CID to the host. This card then goes into Identification State. Thereafter, the host issues Set_Relative_Addr (CMD3) to assign to this card a relative card address (RCA). Once the RCA is received the card state changes to the Stand-by State, and the card does not react to further identification cycles, and its output switches from open-drain to push-pull. The host repeat the process, which is CM2 and CMD3, until the host receive time-out condition to recognize completion of the identification process.

26.4.4 Card Access

26.4.4.1 Block Access, Block Write and Block Read

During block write (CMD24-27) one or more blocks of data are transferred from the host to the card with a CRC appended to the end of each block by the host. A card supporting block write shall always be able to accept a block of data defined by WRITE_BL_LEN. If the CRC fails, the card shall indicate the failure on the DAT line; the transferred data will be discarded and not written, and all further transmitted blocks (in multiple block write mode) will be ignored.

Programming of the CID and CSD registers does not require a previous block length setting.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

The transferred data is also CRC protected. If a part of the CSD or CID register is stored in ROM, then this unchangeable part must match the corresponding part of the receive buffer. If this match fails, then the card will report an error and not change any register contents. Some cards may require long and unpredictable times to write a block of data. After receiving a block of data and completing the CRC check, the card will begin writing and hold the DAT line low if its write buffer is full and unable to accept new data from a new WRITE_BLOCK command. The host may poll the status of the card with a SEND_STATUS command (CMD13) at any time, and the card will respond with its status. The status bit READY_FOR_DATA indicates whether the card can accept new data or whether the write process is still in progress). The host may deselect the card by issuing CMD7 (to select a different card) which will displace the card into the Disconnect State and release the DAT line without interrupting the write operation. When reselecting the card, it will reactivate busy indication by pulling DAT to low if programming is still in progress and the write buffer is unavailable.

Block read is similar to stream read, except the basic unit of data transfer is a block whose maximizes is defined in the CSD (READ_BL_LEN). If READ_BL_PARTIAL is set, smaller blocks whose starting and ending address are entirely contained within one physical block (as defined by READ_BL_LEN) may also be transmitted. Unlike stream read, a CRC is appended to the end of each block ensuring data transfer integrity. CMD17 (READ_SINGLE_BLOCK) initiates a block read and after completing the transfer, the card returns to the Transfer state. CMD18 (READ_MULTIPLE_BLOCK) starts a transfer of several consecutive blocks. Blocks will be continuously transferred until a stop command is issued. If the host uses partial blocks whose accumulated length is not block aligned and block misalignment is not allowed, the card shall detect a block misalignment at the beginning of the first mis-aligned block, set the ADDRESS_ERROR error bit in the status register, abort transmission and wait in the Data State for a stop command.

26.4.4.2 Stream Access, Stream Write and Stream Read (MMC Only)

Stream write (CMD20) starts the data transfer from the host to the card beginning from the starting address until the host issues a stop command. Since the amount of data to be transferred is not determined in advance, CRC can not be used. If the end of the memory range is reached while sending data and no stop command has been sent by the host, all further transferred data is discarded.

There is a stream oriented data transfer controlled by READ_DAT_UNTIL_STOP (CMD11). This command instructs the card to send its payload, starting at a specified address, until the host sends a STOP_TRANSMISSION command (CMD12). The stop command has execution delay due to the serial command transmission. The data transfer stops after the end bit of the stop command. If the end of the memory range is reached while sending data and no stop command has been sent yet by the host, the contents of the further transferred payload is undefined.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

26.4.4.3 Erase, Group Erase and Sector Erase (MMC Only)

It is desirable to erase many sectors simultaneously in order to enhance the data throughput. Identification of these sectors is accomplished with the TAG_* commands. Either an arbitrary set of sectors within a single erase group, or an arbitrary selection of erase groups may be erase at one time, but not both together. That is, the unit of measure for determining an erase is either a sector or an erase group. If a set of sectors must be erased, all selected sectors must lie within the same erase group. To facilitate selection, a first command with the starting address is followed by a second command with the final address, and all sectors (or groups) within this range will be selected for erase.

26.4.4.4 Wide Bus Selection/Deselection

Wide Bus (4 bit bus width) operation mode may be selected / deselected using ACMD6. The default bus width after power up or GO_IDLE (CMD0) is 1 bit bus width. ACMD6 command is valid in 'trans state' only. That means the bus width may be changed only after a card was selected (CMD7).

26.4.4.5 Protection Management

Three write protect methods are supported in the host for Cards, Card internal write protect (Card's responsibility), Mechanical write protect switch (Host responsibility only) and Password protection card lock operation.

26.4.4.6 Card Internal Write Protection

Card data may be protected against either erase or write. The entire card may be permanently write protected by the manufacturer or content provider by setting the permanent or temporary write protect bits in the CSD. For cards which support write protection of groups of sectors by setting the WP_GRP_SIZE sectors as specified in the CSD), and the write protection may be changed by the application. The SET_WRITE_PROT command sets the write protection of the addressed write-protect group, and the CLR_WRITE_PROT command clears the write protection of the addressed write-protect group.

The SEND_WRITE_PROT command is similar to a single block read command. The card shall send a data block containing 32 write protection bits (representing 32 write protect groups starting at the specified address) followed by 16 CRC bits. The address field in the write protect commands is a group address in byte units. The card will ignore all LSB's below the group size.

26.4.4.7 Mechanical write protect switch

A mechanical sliding tablet on the side of the card will be used by the user to indicate that a given card is write protected or not. If the sliding tablet is positioned in such a way that the

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

window is open that means the card is write protected. If the window is close the card is not write protected.

A proper, matched, switch on the socket side will indicated to the host that the card is write protected or not. It is the responsibility of the host to protect the card. The position of the write protect switch is un-known to the internal circuitry of the card.

26.4.4.8 Password Protect

The password protection feature enables the host to lock a card while providing a password, which later will be used for unlocking the card. The password and its size is kept in an 128-bit PWD and 8-bit PWD_LEN registers, respectively. These registers are non-volatile so that a power cycle will not erase them.

Locked cards respond to (and execute) all commands in the basic command class (class 0) and “lock card” command class. Thus the host is allowed to reset, initialize, select, query for status, etc., but not to access data on the card. If the password was previously set (the value of PWD_LEN is not 0) will be locked automatically after power on. Similar to the existing CSD and CID register write commands the lock/unlock command is available in “trans-state” only. This means that it does not include an address argument and the card must be selected before using it. The card lock/unlock command has the structure and bus transaction type of a regular single block write command. The transferred data block includes all the required information of the command (password setting mode, PWD itself, card lock/unlock etc.). The following table describes the structure of the command data block.

Table 26-1 Command Data Block Structure

Byte #	Bit 7-4	Bit 3	Bit 2	Bit 1	Bit 0
0	Reserved	ERASE	LOCK_UNLOCK	CLR_PWD	SET_PWD
1	PWDS_LEN				
2	Password Data				
…					
PWDS_LEN + 1					

ERASE – 1 Defines Forced Erase Operation (all other bits shall be 0) and only the command byte is sent.

LOCK/UNLOCK – 1=Locks the card. 0=Unlock the card (note that it is valid to set this bit together with SET_PWD but it is not allowed to set it together with CLR_PWD).

CLR_PWD – 1=Clears PWD.

SET_PWD – 1=Set new password to PWD.

PWD_LEN – Defines the following password length (in bytes).

PWD – The password (new or currently used depending on the command).

The data block size shall be defined by the host before it send the card lock/unlock

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

command. This will allow different password sizes.

The following paragraphs define the various lock/unlock command sequences:

Lock command sequences:

1 Setting the Password.
   a Select a card (CMD7), if not previously selected already.
   b Define the block length (CMD16), given by the 8bit card lock/unlock mode, the 8 bits password size (in bytes), and the number of bytes of the new password. In case that a password replacement is done, then the block size shall consider that both passwords, the old and the new one, are sent with the command.
   c Send Card Lock/Unlock command with the appropriate data block size on the data line including 16-bit CRC. The data block shall indicate the mode (SET_PWD), the length (PWD_LEN) and the password itself. In case that a password replacement is done, then the length value (PWD_LEN) shall include both passwords, the old and the new one, and the PWD field shall include the old password (currently used) followed by the new password.
   d In case that the sent old password is not correct (not equal in size and content) then LOCK_UNLOCK_FAILED error bit will be set in the status register and the old password does not change. In case that PWD matches the sent old password then the given new password and its size will be saved in the PWD and PWD_LEN fields, respectively.

   NOTE:
   the password length register (PWD_LEN) indicates if a password is currently set. When it equals 0 there is no password set. If the value of PWD_LEN is not equal to zero the card will lock itself after power up. It is possible to lock the card immediately in the current power session by setting the LOCK/UNLOCK bit (while setting the password) or sending additional command for card lock.

2 Reset the password.
   a Select a card (CMD7), if not previously selected already.
   b Define the block length (CMD16), given by the 8-bit card lock/unlock mode, the 8-bit password size (in bytes), and the number of bytes of the currently used password.
   c Send the card lock/unlock command with the appropriate data block size on the data line including 16-bit CRC. The data block shall indicate the mode CLR_PWD, the length (PWD_LEN) and the password (PWD) itself (LOCK/UNLOCK bit is don't care). If the PWD and PWD_LEN is set to 0. If the password is not correct then the LOCK_UNLOCK_FAILED error bit will be set in the status register.

3 Locking a card.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

a Select a card (CMD7), if not previously selected already.

b Define the block length (CMD16), given by the 8-bit card lock/unlock mode, the 8-bit password size (in bytes), and the number of bytes of currently used password.

c Send the card lock/unlock command with the appropriate data block size on the data line including 16-bit CRC. The data block shall indicate the mode LOCK, the length (PWD_LEN) and the password (PWD) itself.

If the PWD content equals to the sent password then the card will be locked and the card-locked status bit will be set in the status register. If the password is not correct then LOCK_UNLOCK_FAILED error bit will be set in the status register.

NOTE:

it is possible to set the password and to lock the card in the same sequence. In such case the host shall perform all the required steps for setting the password (as described above) including the bit LOCK set while the new password command is sent. If the password was previously set (PWD_LEN is not 0), then the card will be locked automatically after power on reset. An attempt to lock a locked card or to lock a card that does not have a password will fail and the LOCK_UNLOCK_FAILED error bit will be set in the status register.

Unlock command sequences:

1 Unlocking the card.

a Select a card (CMD7), if not previously selected already.

b Define the block length (CMD16), given by the 8-bit card lock/unlock mode, the 8-bit password size (in bytes), and the number of bytes of the currently used password.

c Send the card lock/unlock command with the appropriate data block size on the data line including 16-bit CRC. The data block shall indicate the mode UNLOCK, the length (PWD_LEN) and the password (PWD) itself.

If the PWD content equals to the sent password then the card will be unlocked and the card-locked status bit will be cleared in the status register. If the password is not correct then the LOCK_UNLOCK_FAILED error bit will be set in the status register.

NOTE:

the unlocking is done only for the current power session. As long as the PWD is not cleared the card will be locked automatically on the next power up. The only way to unlock the card is by clearing the password. An attempt to unlock an unlocked card will fail and LOCK_UNLOCK_FAILED error bit will be set in the status register.

2 Forcing Erase.

In case that the user forgot the password (the PWD content) it is possible to erase all

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

the card data content along with the PWD content. This operation is called Forced Erase.

a Select a card (CMD7), if not previously selected already.

b Define the block length (CMD16) to 1 byte (8bit card lock/unlock command). Send the card lock/unlock command with the appropriate data block of one byte on the data line including 16-bit CRC. The data block shall indicate the mode ERASE (the ERASE bit shall be the only bit set).

If the ERASE bit is not the only bit in the data field then the LCOK_UNLOCK_FAILED error bit will be set in the status register and the erase request is rejected. If the command was accepted then ALL THE CARD CONTENT WILL BE ERASED including the PWD and PWD_LEN register content and the locked card will get unlocked.

An attempt to force erase on an unlocked card will fail and LOCK_UNLOCK_FAILED error bit will be set in the status register.

26.4.5 Card Status

The response format R1 contains a 32-bit field named card status. This field is intended to transmit the card's status information (which may be stored in a local status register) to the host. If not specified otherwise, the status entries are always related to the previous issued command.

Table below defines the different entries of the status. The type and clear condition fields in the table are abbreviate as follows:

Type:

E: Error bit.

S: Status bit..

R: Detected and set for the actual command response.

X: Detected and set during command execution. The host must poll the card by issuing the status command in order to read these bits.

Clear Condition:

A: According to the card current state.

B: Always related to the previous command. Reception of a valid command will clear it (with a delay of one command).

C: Clear by read.

Table 26-2 Card Status Description

Bits	Identifier	Type	Description	Clear Condition
31	OUT_OF_RAGE	E R	The command's argument was out	C

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

			of the allowed range for this card. 0: No Error 1: Error	
30	ADDRESS_ERROR	E R X	A misaligned address which did not match the block length was used in the command. 0: No Error 1: Error	C
29	BLOCK_LEN_ERROR	E R	The transferred block length is not allowed for this, or the number of transferred bytes does not match the block length. 0: No Error 1: Error	C
28	ERASE_SEQ_ERROR	E R	An error in the sequence of erase commands occurred. 0: No Error 1: Error	C
27	ERASE_PARAM	E X	An invalid selection of sectors or groups for erase occurred. 0: No Error 1: Error	C
26	WP_VIOLATION	E R X	Attempt to program a write protected block. 0: No Protected 1: Protected	C
25	CARD_IS_LOCKED	S X	When set, signals that the card is locked by the host. 0: Card unlocked 1: Card locked	A
24	LOCK_UNLOCK_FAILED	E R X	Set when a sequence or password error has been detected in lock/unlock card command or if there was an attempt to access a locked card. 0: No Error 1: Error	C
23	COM_CRC_ERROR	E R	The CRC check of the previous command failed. 0: No Error 1: Error	B
22	ILLEGAL_COMMAND	E R	Command not legal for the card	B

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

			state. 0: No Error 1: Error	
21	CARD_ECC_FAILED	E X	Card internal ECC was applied but failed to correct the data. 0: normal 1: failure	C
20	CC_ERROR	E R X	Internal card controller error. 0: No Error 1: Error	C
19	ERROR	E R X	A general or an unknown error occurred during the operation. 0: No Error 1: Error	C
18	UNDERRUN	E X	The card could not sustain data transfer in stream read mode. 0: No Error 1: Error	C
17	OVERRUN	E X	The card could not sustain data programming in stream write mode. 0: No Error 1: Error	C
16	CID/CSD_OVERWRITE	E R X	Can be either one of the following errors. 0: No Error 1: Error	C
15	WP_ERASE_SKIP	S X	Only partial address space was erased due to existing write protected blocks. 0: No Protected 1 : Protected	C
14	CARD_ECC_DISABLED	S X	The command has been executed without using the internal ECC. 0: enabled 1: disabled	A
13	ERASE_RESET	S R	An erase sequence was cleared before executing because an out of erase sequence command was received. 0: normal 1: set	C
12:9	CURRENT_STATE	S X	The state of the card when receiving	B

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

			the command. If the command execution causes a state change, it will be visible to the host in the response to the next command. The four bits are interpreted as binary coded number between 0 and 15. 0: idle 1: ready 2: identify 3: standby 4: transition 5: data 6: receive 7: program 8 : disable (9 – 15) : received	
8	READY_FOR_DATA	S X	Corresponds to buffer empty signaling on the bus. 0: No Ready 1: Ready	A
7:6	Reserved	-	-	-
5	APP_CMD	S R	The card will expect ACMD, or indication that the command has been interpreted as ACMD. 0: Disable 1: Enable	C
4:0	Reserved	-	-	-

26.4.6 SD Status

The SD status contains status bits that are related to the SD card proprietary features and may be used for future application specific usage. The size of the SD status is one data block of 512bit. The content of this register is transmitted to the Host over the DAT bus along with 16-bit CRC. The SD status is sent to the host over the DAT bus if ACMD13 is sent (CMD55 followed with CMD13). ACMD13 can be sent to a card only in tran_state (card is selected). SD status structure is described in below.

The same abbreviation for *type* and *clear condition* were used as for the Card Status above.

Table 26-3 SD Status Structure

Bits	Identifier	Type	Description	Clear Condition
511:510	DAT_BUS_WIDTH	S R	Shows the currently defined data	A

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

			bus width that was defined by SET_BUS_WIDTH command. 00: 1 (default) 01: Reserved 10: 4 bit width 11: Reserved	
509	SECURED_MODE	S R	Card is in Secured Mode of operation. 0: Not in the Mode 10: In the mode	A
508:496	Reserved.			
495:480	SD_CARD_TYPE	S R	All 0, is SD Memory cards.	A
479:448	SIZE_OF_PROTECTED_AREA	S R	Size of protected area.	A
447:312	Reserved.			
311:0	Reserved for manufacturer.			

26.4.7 SDIO

I/O access differs from memory in that the registers can be written and read individually and directly without a FAT file structure or the concept of blocks (although block access is supported). These registers allow access to the IO data, control of the IO function, and report on status or transfer I/O data to and from the host.

Each SDIO card may have from 1 to 7 functions plus one memory function built into it. A function is a self contained I/O device. I/O functions may be identical or completely different from each other. All I/O functions are organized as a collection of registers, and there is a maximum of 131,072 registers possible for each I/O function.

26.4.7.1 SDIO Interrupts

In order to allow the SDIO card to interrupt the host, and interrupt function is added to a pin on the SD interface. Pin number 8 which is used as DAT[1] when operating in the 4 bit SD mode is used to signal the card's interrupt to the host. The use of interrupt is optional for each card or function within a card. The SDIO interrupt is "level sensitive", that is, the interrupt line must be held active (low) until it is either recognized and acted upon by the host or de-asserted due to the end of the Interrupt Period. Once the host has serviced the interrupt, it is cleared via an IO write to the appropriate bit in the CCCR. The interrupt output of all SDIO cards is active low.

As Pin 8 of the card is shared between the IRQ and DAT[1] use in the 4 bit SD mode, and interrupt shall only be sent by the card and recognized by the host during a specific time. The time that a low on Pin 8 will be recognized as an interrupt is defined as the Interrupt Period. The host here will only sample the level of Pin 8 (DAT[1]/IRQ) into the interrupt detector during the Interrupt Period. At all other times, the host will ignore the level on Pin 8. Note that the

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Interrupt Period is applicable for both memory and IO operations. The definition of the Interrupt Period is different for operations with single block and multiple block data transfer.

26.4.7.2 SDIO Suspend/Resume

Within a multi-function SDIO or a Combo (Mix IO and Memory) card, there are multiple devices (I/O and memory) that must share access to the SD bus. In order to allow the sharing of access to the host among multiple devices, SDIO and combo cards can implement the optional concept of suspend/resume. In a card supports suspend/resume, the host may temporarily halt a data transfer operation to one function or memory (suspend) in order to free the bus for a higher priority transfer to a different function of memory. Once this higher-priority transfer is complete, the original transfer is re-started where it left off (resume). The host controller here is supported by all IO functions except zero, and the memory of a combo card, and can suspend multiple transactions and resume them in any order desired. IO function zero does not support suspend/resume.

The procedure used to perform the Suspend/Resume operation on the SD bus is:

- The host determines which function currently used the DAT[] line(s).
- The host requests the lower priority or slower transaction to suspend.
- The host checks for the transaction suspension to complete.
- The host begins the higher priority transaction.
- The host waits for the completion of the higher priority transaction.
- The host restores the suspended transaction.

26.4.7.3 SDIO Read Wait

The optional Read Wait (RW) operation is defined only for the SD 1-bit and 4-bit modes. The read wait operation allows a host to signal a card that it is doing a read multiple (CMD53) operation to temporarily stall the data transfer while allowing the host to send commands to any function within the SDIO device. To determine if a card supports the Read Wait protocol, the host must test capability bits in CCCR. The timing for Read Wait is base on the Interrupt Period.

26.4.7.4 Clock Control

The software should guarantee that the card identification process starts in open-drain mode with the clock rate fod (0 ~ 400khz). In addition, the software should also make the card into interrupt mode with fod (only for MMC). The commands that require fod are CMD0, CMD1, CMD2, CMD3, CMD5, CMD40 and ACMD41. In data transfer mode, the MSC controller can operate card with clock rate fpp (0 ~ 25Mhz).

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

26.4.7.5 Application Specified Command Handling

The MMC/SD system is designed to provide a standard interface for a variety applications types. In this environment it is anticipate that there will be a need for specific customers/applications features. To enable a common way of implementing these features, two types of generic commands are defined in the standard: Application Specific Command, ACMD, and General Command, GEN_CMD.

GEN_CMD, this command, when received by the card, will cause the card to interpret the following command as an application specific command, ACMD. The ACMD has the same structure as of regular MMC standard commands and it may have the same CMD number. The card will recognize it as ACMD by the fact that it appears after APP_CMD.

The only effect of the APP_CMD is that if the command index of the, immediately, following command has an ACMD overloading, the none standard version will used. If, as an example, a card has a definition for ACMD13 but not for ACMD7 then, if received immediately after APP_CMD command, Command 13 will be interpreted as the non standard ACMD13 but, command 7 as the standard CMD7.

In order to use one of the manufacturer specific ACMD's the host will:

1. Send APP_CMD. The response will have the APP_CMD bit (new status bit) set signaling to the host that ACMD is now expected.
2. Send the required ACMD. The response will have the APP_CMD bit set, indicating that the accepted command was interpreted as ACMD. If a non-ACMD is sent then it will be respected by the card as normal MMC command and the APP_CMD bit in the Card Status stays clear.

If a non valid command is sent (neither ACMD nor CMD) then it will be handled as a standard MMC illegal command error.

The bus transaction of the GEN_CMD is the same as the single block read or write commands (CMD24 or CMD17). The difference is that the argument denotes the direction of the data transfer (rather than the address) and the data block is not a memory payload data but has a vendor specific format and meaning.

The card shall be selected before sending CMD56. The data block size is the BLOCK_LEN that was defined with CMD16. The response to CMD56 will be R1b (card status + busy indication).

26.5 Pins Description

- MSC_CLK, output, host to card clock signal.
- MSC_CMD, inout, bidirectional command/response signal.
- MSC_DAT[3:0], inout, bidirectional data bus.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

26.6 Data Format Description

MSC0 and MSC1 supports two kinds of data bits width:1bits, 4bits.

Figure 26-2 msc data format

26.7 Register Description

Following chapter will describe the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. Register read/write attribute
   - R- Read only
   - W- Write only
   - RW- Read and Write
   - RCW- Read and Write, but Clear to 0 by Read
   - RSW- Read and Write, but Set to 1 by Read
   - RWC- Read and Write, Clear to 0 by Write 1, Write 0 has no effect
   - RWS- Read and Write, Set to 1 by Write 1, Write 0 has no effect
   - RC- Read only, and Clear to 0 by read
   - RS- Read only, and Set to 1 by read
3. Reset Value
   - 1 - reset to 1
   - 0 - reset to 0
   - ? - value unknown after reset

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

26.7.1 Register Memory Map

Table 26-4 Registers Memory Map Base Address

Name	Base	Description
MSC0	0x13450000	Address base of MSC0
MSC1	0x13460000	Address base of MSC1

The MMC-SD-CE_ATA controller is controlled by a set of registers that the application configures before every operation. The following table lists all the MSC registers.

Table 26-5 MSC Registers Map

Name	RW	Reset Value	Address Offset	Access Size
MSC_CTRL	RW	0x0000_0000	0x0000	32
MSC_STAT	R	0x??00_0040	0x0004	32
MSC_CLKRT	RW	0x0000_0000	0x0008	32
MSC_CMDAT	RW	0x0000_5000	0x000C	32
MSC_RESTO	RW	0x0000_0100	0x0010	32
MSC_RDTO	RW	0x00FF_FFFF	0x0014	32
MSC_BLKLEN	RW	0x0000_0000	0x0018	32
MSC_NOB	RW	0x0000_0000	0x001C	32
MSC_SNOB	R	0x0000_????	0x0020	32
MSC_IMASK	RW	0xFFFF_FFFF	0x0024	32
MSC_IFLG	RW	0x??00_2000	0x0028	32
MSC_CMD	RW	0x0000_0000	0x002C	32
MSC_ARG	RW	0x0000_0000	0x0030	32
MSC_RES	R	0x0000_????	0x0034	32
MSC_RXFIFO	R	0x????_????	0x0038	32
MSC_TXFIFO	W	0x????_????	0x003C	32
MSC_LPM	RW	0x0000_0000	0x0040	32
MSC_DMAC	RW	0x0000_0000	0x0044	32
MSC_DMANDA	RW	0x0000_0000	0x0048	32
MSC_DMADA	R	0x0000_0000	0x004C	32
MSC_DMALEN	R	0x0000_0000	0x0050	32
MSC_DMACMD	R	0x0000_0000	0x0054	32
MSC_CTRL2	RW	0x0080_0000	0x0058	32
MSC_RTCNT	R	0x0000_0000	0x005C	32

26.7.2 Register and Fields Description

26.7.2.1 MSC Control Register (MSC_CTRL,0x0000)

	MSC_CTRL	Base + 0x0000

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																SEND_CCSD	SEND_AD_CCSD	Reserved						EXIT_MULTIPLE	EXIT_TRANSFER	START_READ WAIT	STOP_READ WAIT	RESET	START_OP	CLOCK_CTRL	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect. read as zero.	R
15	SEND_CCSD	0: clear bit 1: Send Command Completion Signal Disable (CCSD) to CE_ATA device when set, host sends CCSD to CE_ATA device. Software set the bit only if current command is expecting CCS and interrupts are enabled in CE_ATA devices. Once the CCSD pattern is sent to device, host automatically clears the SEND_CCSD bit.	W
14	SEND_AS_CCSD	0: clear bit 1: send internally generated stop after sending CCSD to CE_ATA device When set, host automatically sends internally-generated STOP command(CMD12) to CE_ATA device. After sending CMD12, MSC_STAT. AUTO_CMD12_DONE is set and generates interrupt to CPU. After sending the CCSD, controller automatically clears the SEND_AS_CCSD bit.	W
13:8	Reserved	Writing has no effect. read as zero.	R
7	EXIT_MULTIPLE	If CMD12 or CMD52 (I/O abort) is to be sent to terminate multiple block read/write in advance, set this bit to 1. 0: No effect 1: Exit from multiple block read/write	W
6	EXIT_TRANSFER	**Only used for SDIO suspend/resume and MMC stream read.** For SDIO, after suspend is accepted, set this bit with 1. For MMC, after the data of the expected number are received, set this bit with 1. 0: No effect 1: Exit from multiple block read/write after suspend is accepted, or exit from stream read	W
5	START_READ WAIT	Only used for SDIO Read Wait. Start the Read Wait cycle. 0: No effect 1: Start Read Wait	W
4	STOP_READ WAIT	Only used for SDIO Read Wait. Stop the Read Wait cycle. 0: No effect	W

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		1: Start Read Wait	
3	RESET	Reset the MSC controller. 0: No effect 1: Reset the MSC controller	W
2	START_OP	This bit is used to start the new operation. When starting the clock, this bit can be 1. When stopping the clock, this bit can only be 0. 0: Do nothing 1: Start the new operation	W
1:0	CLOCK_CTRL	These bits are used to start or stop clock. 00: Do nothing 01: Stop MMC/SD clock 10: Start MMC/SD clock 11: Reserved	W

26.7.2.2 MSC Status Register (MSC_STAT,0x0004)

	MSC_STAT																															Base + 0x0004
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	AUTO_CMD12_DONE	Reserved		PIN_LEVEL					Reserved			BCE	BDE	BAE	BAR	DMAEND	IS_RESETTING	SDIO_INT_ACTIVE	PRG_DONE	DATA_TRAN_DONE	END_CMD_RES	DATA_FIFO_AFULL	IS_READ WAIT	CLK_EN	DATA_FIFO_FULL	DATA_FIFO_EMPTY	CRC_RES_ERR	CRC_READ_ERROR	CRC_WRITE_ERRO	R	TIME_OUT_RES	TIME_OUTREAD
RST	0	0	0	?	?	?	?	?	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bits	Name	Description	RW
31	AUTO_CMD12_DONE	Indicates that the stop command (CMD12) that is internally generated by controller has finished.	R
30:29	Reserved	Writing has no effect, read as zero.	R
28:24	PIN_LEVEL	MSC Interface Pin Level PIN_LEV[4:0] indicates the pin level of MSC_CMD, MSC_DAT[3:0] separately.	R
23:21	Reserved	Writing has no effect, read as zero.	R
20	BCE	Boot CRC error. 0: No boot CRC error occurs. 1: Boot CRC is not correct.	R
19	BDE	Boot data end. 0: No boot data or boot data is not finished. 1: Boot data is received completely.	R
18	BAE	Boot acknowledge is error.	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		0: No boot acknowledge is received or boot acknowledge is correct (decided by BAR) 1: The received boot acknowledge is not correct.	
17	BAR	Boot acknowledge received. 0: No boot acknowledge received. 1: Boot acknowledge received.	R
16	DMAEND	Indicates that the DMA has finished the current transfer.	R
15	IS_RESETTING	MSC is resetting after power up or MSC_CTRL[RESET] is written with 1. 0: Reset has been finished 1: Reset has not been finished	R
14	SDIO_INT_ACTIVE	Indicates whether an interrupt is detected at the SD I/O card. A separate acknowledge command to the card is required to clear this interrupt. 0: No interrupt detected 1: The interrupt from SDIO is detected	R
13	PRG_DONE	Indicates whether card has finished programming. 0: not finished 1: finished	R
12	DATA_TRAN_DONE	Indicates whether data transmission to card has completed. 0: not completed 1: completed	R
11	END_CMD_RES	Indicates whether command and response/no-response sequence have been completed 0: not completed 1: completed	R
10	DATA_FIFO_AFULL	Indicates whether the data FIFO is almost full. 0: The number of words in FIFO is less then 127. 1: The number of words in FIFO is equal to or great then 127	R
9	IS_READ WAIT	Indicates whether SDIO card has entered Read Wait State. 0: Card has not entered Read Wait 1: Card has entered Read Wait	R
8	CLK_EN	Clock enabled. 0: Clock is off 1: Clock is on	R
7	DATA_FIFO_FULL	Indicates whether the data FIFO is full. 0: Data FIFO is not full 1: Data FIFO is full	R
6	DATA_FIFO_EMPTY	Indicates whether data FIFO is empty.	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		0: Data FIFO is not empty 1: Data FIFO is empty	
5	CRC_RES_ERR	Response CRC error. 0: No error on the response CRC 1: CRC error occurred on the response	R
4	CRC_READ_ERROR	Read CRC error. 0: No error on received data 1: CRC error occurred on received data	R
3:2	CRC_WRITE_ERROR	Write CRC error. 00: No error on transmission of data 01: Card observed erroneous transmission of data 10: No CRC status is sent back 11: Reserved	R
1	TIME_OUT_RES	Response Time Out. 0: Card response has not timed out 1: Card response has time out	R
0	TIME_OUT_READ	Read time out. 0: Card read data has not timed out 1: Card read data has timed out	R

26.7.2.3 MSC Clock Rate Register (MSC_CLKRT,0x0008)

The MSC_CLKRT register specifies the frequency division of the MMC/SD bus clock. The software is responsible for setting this register.

	MSC_CLKRT																															Base + 0x0008
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																													CLK_RATE		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:3	Reserved	Writing has no effect, read as zero.	R
2:0	CLK_RATE	Clock rate. 000: DEV_CLK 001: 1/2 of DEV_CLK 010: 1/4 of DEV_CLK 011: 1/8 of DEV_CLK 100: 1/16 of DEV_CLK 101: 1/32 of DEV_CLK	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		110: 1/64 of DEV_CLK 111: 1/128 of DEV_CLK This field must be set to 0 when the controller works during normal writing or reading.	

26.7.2.4 MSC Command and Data Control Register (MSC_CMDAT,0x000C)

	MSC_CMDAT																															Base + 0x000C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CCS_EXPECTED	READ_CEATA	Reserved		DIS_BOOT	Reserved_0	EXP_BOOT_ACK	BOOT_MODE	Reserved					Reserved_0	SDIO_PDRT	AUTO_CMD12	RTRG		TTRG		IO_ABORT	BUS_WIDTH		Reserved	INIT	BUSY	STREAM_BLOCK	WRITE_READ	DATA_EN	RESPONSE_FORMAT		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	CCS_EXPECTED	0: interrupts are not enabled in CE-ATA device, or commands does not expect CCS from device 1: interrupts are enabled in CE_ATA device, or RW_BLK command expects command completion signal from device If the command expects Command Completion Signal (CCS) from the device, the software should set the control bit. It is auto cleared 0 by hardware.	RW
30	READ_CEATA	0: host is not performing read access (RW_BLK or RW_REG) towards CE_ATA device 1: host id performing read access (RW_BLK or RW_REG) towards CE_ATA device Software should set the bit to indicate that CE_ATA device is being accessed for read transfer. The bit is used to disable read data timeout indication while performing CE_ATA read transfers. It is auto cleared 0 by hardware.	RW
29:28	Reserved	Writing has no effect, read as zero.	R
27	DIS_BOOT	0: Do nothing 1: Stop boot operation DIS_BOOT should not be used with ENA_BOOT at the same time.	RW
26	Reserved_0	Inner usage, keep to 0.	RW
25	EXP_BOOT_ACK	Whether boot acknowledge pattern is expected or not	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		0: Boot acknowledge pattern is not expected 1: Boot acknowledge pattern is expected	
24	BOOT_MODE	Boot mode operation selection. 0: Ignore. 1: Alternative boot operation	RW
23:19	Reserved	Writing has no effect, read as zero.	R
18	Reserved_0	Inner usage, keep to 0.	RW
17	SDIO_PRDT	Determine whether SDIO interrupt is 2 cycle or extend more cycle when data block last is transferred. 0: more cycle (like single block) 1: exact 2 cycle	RW
16	AUTO_CMD12	This field controls use of auto command functions. 0: Auto CMD12 is disabled 1: MSC controller will issue CMD12 automatically after the last data block transfer is finished. when stop command has finished, it is auto cleared 0 by hardware.	RW
15:14	RTRG	Receive FIFO Trigger Value Select. These bits set the receive FIFO half-empty threshold value, when the number of transmit FIFO >= threshold value , RXFIFO_RD_REQ will be set to 1. 00: more than or equal to 16 01: more than or equal to 32 10: more than or equal to 64 11: more than or equal to 96	RW
13:12	TTRG	Transmit FIFO Trigger Value Select. These bits set the transmit FIFO half-empty threshold value, when the number of transmit FIFO < threshold value , TXFIFO_WR_REQ will be set to 1. 00: less than 16 01: less than 32 10: less than 64 11: less than 96	RW
11	IO_ABORT	Specifies the current command is used to abort data transfer. 0: Nothing 1: The current command is used to abort transfer It is auto cleared 0 by hardware.	WR
10:9	BUS_WIDTH	Specifies the width of the data bus. 00: 1-bit 01: Reserved 10: 4-bit	WR

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

8	Reserved	Writing has no effect, read as zero.	R
7	INIT	80 initialization clocks. 0: Issues command directly 1: Issues 80 clocks before command	W
6	BUSY	Specifies whether a busy signal is expected after the current command. This bit is for no data command/response transactions only. 0: Not expect a busy signal 1: Expects a busy signal. If the response is R1b, then set it	WR
5	STREAM_BLOCK	Stream mode. 0: Data transfer of the current command sequence is not in stream mode 1: Data transfer of the current command sequence is in stream mode	WR
4	WRITE_READ	Data Transfer Direction Selection. 0: Read (from card to host) 1: Write (from host to card)	RW
3	DATA_EN	Specifies whether the current command includes data transfer or not. It is also used to reset RX_FIFO and TX_FIFO. 0: Current command without data transfer 1: Current command with data transfer	RW
2:0	RESPONSE_FORMAT	Response Type Selection. 000: No response 001: Format R1 and R1b 010: Format R2 011: Format R3 100: Format R4 101: Format R5 110: Format R6 111: Format R7	RW

26.7.2.5 MSC Response Time Out Register (MSC_RESTO,0x0010)

	MSC_RESTO																															Base + 0x0010
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RES_TO																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:0	RES_TO	Specifies the maximum number of MSC_CLK clock cycles between the end bit of the command and the response from the SD card. The default value is 128.	RW

26.7.2.6 MSC Read Time Out Register (MSC_RDTO,0x0014)

	MSC_RDTO																															Base + 0x0014
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	READ_TO																															
RST	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Name	Description	RW
31:0	READ_TO	Specifies the maximum number of clocks between the command and when the MMC/SD host controller turns on the time-out error for the received data. The unit is MSC_CLK.	RW

26.7.2.7 MSC Block Size Register (MSC_BLKLEN,0x0018)

	MSC_BLKLEN																															Base + 0x0018
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																BLK_LEN															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Write has no effect, read as zero.	R
15:0	BLK_LEN	Specifies the number of bytes in a block, and is normally set to 0x200 for MMC/SD data transactions. The value Specified in the cards CSD.	RW

26.7.2.8 MSC Block Count Register (MSC_NOB,0x001C)

	MSC_NOB																															Base + 0x001C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Reserved																NOB															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Write has no effect, read as zero.	R
15:0	NOB	Specifies the number of blocks in a data transfer. One block is a possibility.	RW

26.7.2.9 MSC Successfully-transferred Blocks Count Register (MSC_SNOB,0x0020)

In block mode, the MSC_SNOB register records the number of successfully transferred blocks. If the last block has CRC error, this register also summaries it. It is used to query blocks for multiple block transfer.

	MSC_SNOB																															Base + 0x0020
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																MSC_SNOB															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:16	Reserved	Write has no effect, read as zero.	R
15:0	MSC_SNOB	Specify the number of successfully transferred blocks for a multiple block transfer.	R

26.7.2.10 MSC Interrupt Mask Register (MSC_IMASK,0x0024)

	MSC_IMASK																															Base + 0x0024
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	DMA_DATA_DONE	Reserved_1		PIN_LEVEL					WR_ALL_DONE	Reserved		BCE	BDE	BAE	BAR	DMAEND	AUTO_CMD12_DONE	DATA_FIFO_FULL	DATA_FIFO_EMP	CRC_RES_ERR	CRC_READ_ERR	CRC_WRITE_ERR	TIME_OUT_RES	TIME_OUT_READ	SDIO	TXFIFO_WR_REQ	RXFIFO_RD_REQ	Reserved		END_CMD_RES	PRG_DONE	DATA_TRAN_DONE
RST	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Name	Description	RW
31	DMA_DATA_DONE	Mask the interrupt DMA_DATA_DONE 0: Not masked 1: Masked	RW
30:29	Reserved_1	Inner usage, keep to 1.	RW
28:24	PIN_LEVEL	Mask the interrupt of PIN_LEVEL separately 0: Not masked 1: Masked	RW
23	WR_ALL_DONE	Mask the interrupt WR_ALL_DONE 0: Not masked 1: Masked	RW
22:21	Reserved	Writing has no effect, read as zero.	R
20	BCE	Boot CRC error. 0: Not masked 1: Masked	RW
19	BDE	Boot data end. 0: Not masked 1: Masked	RW
18	BAE	Mask the interrupt of BAE. 0: Not masked. 1: Masked.	RW
17	BAR	Mask the interrupt of BAR. 0: Not masked. 1: Masked.	RW
16	DMAEND	Mask the interrupt of DMA end. 0: Not masked. 1: Masked.	RW
15	AUTO_CMD12_DONE	Mask the interrupt AUTO_CMD12_DONE. 0: Not masked 1: Masked	RW
14	DATA_FIFO_FULL	0: Not masked 1: Masked	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

13	DATA_FIFO_EMP	0: Not masked 1: Masked	RW
12	CRC_RES_ERR	0: Not masked 1: Masked	RW
11	CRC_READ_ERR	0: Not masked 1: Masked	RW
10	CRC_WRITE_ERR	0: Not masked 1: Masked	RW
9	TIME_OUT_RES	0: Not masked 1: Masked	RW
8	TIME_OUT_READ	0: Not masked 1: Masked	RW
7	SDIO	Mask the interrupt from the SD I/O card. 0: Not masked 1: Masked	WR
6	TXFIFO_WR_REQ	Mask the Transmit FIFO write request interrupt. 0: Not masked 1: Masked	WR
5	RXFIFO_RD_REQ	Mask the Receive FIFO read request interrupt. 0: Not masked 1: Masked	WR
4:3	Reserved	Writing has no effect, read as zero.	R
2	END_CMD_RES	Mask the End command response interrupt. 0: Not masked 1: Masked	WR
1	PRG_DONE	Mask the Programming done interrupt. 0: Not masked 1: Masked	WR
0	DATA_TRAN_DONE	Mask the Data transfer done interrupt. 0: Not masked 1: Masked	WR

26.7.2.11 MSC Interrupt Flag Register (MSC_IFLG,0x0028)

The MSC_IFLG register shows the currently requested interrupt. The FIFO request interrupts, TXFIFO_WR_REQ, and RXFIFO_RD_REQ are masked off with the DMA function is used. The software is responsible for monitoring these bit in program I/O mode.

	MSC_IFLG																															Base + 0x0028
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	DMA_DATA_DONE	Reserved_0		PIN_LEVEL					WR_ALL_DONE	Reserved_0		BCE	BDE	BAE	BAR	DMAEND	AUTO_CMD12_DONE	DATA_FIFO_FULL	DATA_FIFO_EMP	CRC_RES_ERR	CRC_READ_ERR	CRC_WRITE_ERR	TIME_OUT_RES	TIME_OUT_READ	SDIO	TXFIFO_WR_REQ	RXFIFO_RD_REQ	Reserved		END_CMD_RES	PRG_DONE	DATA_TRAN_DONE
RST	0	0	0	?	?	?	?	?	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	DMA_DATA_DONE	This field will be set to 1 when DATA_TRAN_DONE and DMAEND are valid. 0: the interrupt is not detected 1: the interrupt is detected	RW
30:29	Reserved_0	Inner usage, keep to 0.	RW
28:24	PIN_LEVEL	Indicates PIN_LEVEL interrupt. 0: the interrupt is not detected 1: the interrupt is detected Write 1 to clear.	RWC
23	WR_ALL_DONE	This field will be set to 1 when DATA_TRAN_DONE, DMAEND and PRG_DONE are valid. 0: the interrupt is not detected 1: the interrupt is detected	RW
22:21	Reserved_0	Inner usage, keep to 0	R
20	BCE	Boot CRC error. 0: the interrupt is not detected 1: the interrupt is detected Write 1 to clear.	RWC
19	BDE	Boot data end. 0: the interrupt is not detected 1: the interrupt is detected Write 1 to clear.	RWC
18	BAE	Indicates the BAE interrupt. 0: the interrupt is not detected 1: the interrupt is detected Write 1 to clear.	RWC
17	BAR	Indicates the BAR interrupt. 0: the interrupt is not detected 1: the interrupt is detected Write 1 to clear.	RWC
16	DMAEND	Indicates the DMA end interrupt. 0: the interrupt is not detected 1: the interrupt is detected	RWC

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		Write 1 to clear.	
15	AUTO_CMD12_DONE	Indicates AUTO_CMD12_DONE interrupt. 0: the interrupt is not detected 1: the interrupt is detected Write 1 to clear.	RWC
14	DATA_FIFO_FULL	Indicate data FIFO is full interrupt. 0: the interrupt is not detected 1: the interrupt is detected	R
13	DATA_FIFO_EMP	Indicate data FIFO is empty interrupt. 0: the interrupt is not detected 1: the interrupt is detected	R
12	CRC_RES_ERR	Indicate response CRC error interrupt. 0: the interrupt is not detected 1: the interrupt is detected Write 1 to clear	RWC
11	CRC_READ_ERR	Indicate CRC read error interrupt. 0: the interrupt is not detected 1: the interrupt is detected Write 1 to clear	RWC
10	CRC_WRITE_ERR	Indicate CRC write error interrupt. 0: the interrupt is not detected 1: the interrupt is detected Write 1 to clear	RWC
9	TIME_OUT_RES	Indicate response time out interrupt. 0: the interrupt is not detected 1: the interrupt is detected Write 1 to clear	RWC
8	TIME_OUT_READ	Indicate read time out interrupt. 0: the interrupt is not detected 1: the interrupt is detected Write 1 to clear	RWC
7	SDIO	Indicates whether the interrupt from SDIO is detected. 0: The interrupt from SDIO is not detected 1: The interrupt from SDIO is detected	R
6	TXFIFO_WR_REQ	Transmit FIFO write request. Set if data FIFO becomes half empty. (the number of words is < 8) 0: No Request for data Write to MSC_TXFIFO 1: Request for data write to MSC_TXFIFO	R
5	RXFIFO_RD_REQ	Receive FIFO read request. Set if data FIFO becomes half full (the number of words is >= 8) or the entries in data FIFO are the last read data. 0: No Request for data read from MSC_RXFIFO	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		1: Request for data read from MSC_RXFIFO	
4:3	Reserved	Writing has no effect, read as zero.	R
2	END_CMD_RES	Indicates whether the command/response sequence has been finished. 0: The command/response sequence has not been finished 1: The command/response sequence has been finished Write 1 to clear.	RWC
1	PRG_DONE	Indicates whether card has finished programming. 0: Card has not finished programming and is busy 1: Card has finished programming and is no longer busy Write 1 to clear.	RWC
0	DATA_TRAN_DONE	Indicates whether data transfer is done. Note that for stream read/write, only when CMD12 (STOP_TRANS) has been sent, is this bit set. 0: Data transfer is not complete 1: Data transfer has completed or an error has occurred Write 1 to clear.	RWC

26.7.2.12 MSC Command Index Register (MSC_CMD,0x002C)

	MSC_CMD																															Base + 0x002C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										CMD_INDEX					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:6	Reserved	Writing has no effect, read as zero.	R
5:0	CMD_INDEX	Specifies the command index to be executed.	RW

26.7.2.13 MSC Command Argument Register (MSC_ARG,0x0030)

	MSC_ARG																															Base + 0x0030
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ARG																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

31:0	ARG	Specifies the argument for the current command.	RW

26.7.2.14 MSC Response FIFO Register (MSC_RES,0x0034)

The read-only MMC/SD Response FIFO register (RES_FIFO) holds the response sent back to the MMC/SD controller after every command. The size of this FIFO is 8 x 16-bit. The RES_FIFO does not contain the 7-bit CRC for the response. The Status for CRC checking and response time-out status is in the status register MSC_STAT.

The first half-word read from the response FIFO is the most significant half-word of the received response.

	MSC_RES																															Base + 0x0034
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																DATA															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	DATA	Contains the response to the command that is sent by the MMC/SD controller.	R

26.7.2.15 MSC Receive FIFO Port Register (MSC_RXFIFO,0x0038)

The MSC_RXFIFO is used to read the data from a card. It is read-only to the software, and is read on 32-bit boundary. The size of this FIFO is 128 x 32-bit.

	MSC_RXFIFO																															Base + 0x0038
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:0	DATA	One word of read data.	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

26.7.2.16 MSC Transmit FIFO Port Register (MSC_TXFIFO,0x003C)

The MSC_TXFIFO is used to write the data to a card. It is write-only to the software, and is written on 32-bit boundary. The size of this FIFO is 128 x 32-bit.

	MSC_TXFIFO																															Base + 0x003C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:0	DATA	One word of write data.	W

26.7.2.17 MSC Low Power Mode Register (MSC_LPM,0x0040)

The MSC_LPM is used to control whether MSC controller enters Low-Power Mode.

	MSC_LPM																															Base + 0x0040
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DRV_SEL		SMP_SEL	Reserved																												LPM
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:30	DRV_SEL	Drive clock selection 0: CMD and data are driven by MSC_CLK falling edge 1: CMD and data are driven by clock rising edge which is 1ns delayed by MSC_CLK 2: CMD and data are driven by clock rising edge which is 1/4 phase delayed by MSC_CLK 3: Reserved When this field is not zero, MSC_CLKRT.CLK_RATE must be set to 0.	RW
29	SMP_SEL	Sample clock selection 0: CMD and data are sampled by MSC_CLK rising edge 1: CMD and data are sampled by clock rising edge which is 1/4 or 1/2 phase delayed by MSC_CLK. When this field is 1, MSC_CLKRT.CLK_RATE must be set to 0.	
28:1	Reserved	Writing has no effect, read as zero.	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

0	LPM	Low Power Mode Enable 0: Disable low power mode 1: Enable low power mode Clock will stop when card in idle (should be normally set to only MMC and SD cards. For SDIO cards, if interrupts must be detected, clock should not be stopped) When software sets the bit, MSC clock can auto be stopped. **NOTE:** when set the bit, the clock start and stop can be not use.	RW

26.7.2.18 MSC DMA Control Register (MSC_DMAC,0x0044)

The MSC_DMAC register is used to control the DMA transfer.

	MSC_DMAC																															Base + 0x0044
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								MODE_SEL	AOFST		ALIGNEN	INCR		DMASEL	DMAEN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect, read as zero.	R
7	MODE_SEL	Transfer mode selection. 0: Do not specify the transfer length. This is the standard transfer. 1: Specify the transfer length. If this mode is selected, the transfer performance can be improved.	
6:5	AOFST	Address Offset. This field is effective only when ALIGNEN is 1b. 00b:The lowest 2 bit of the data transfer start address is 00b 01b: The lowest 2 bit of the data transfer start address is 01b 10b: The lowest 2 bit of the data transfer start address is 10b 11b: The lowest 2 bit of the data transfer start address is 11b	RW
4	ALIGNEN	Align Enable 0: Only word boundary data transfer is supported 1: Byte boundary data transfer is supported	RW
3:2	INCR	Burst type selection. The field only effects to special DMA in MSC controller. 2’b00: The burst type of DMA is INCR16. 2’b01: The burst type of DMA is INCR32. 2’b10: The burst type of DMA is INCR64.	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

1	DMASEL	One of supported DMA modes is selected. 0: Special DMA in MSC controller is used 1: Common DMA in DMAC controller is used	RW
0	DMAEN	DMA Function Enable 0: Disable DMA function 1:Enable DMA function	RW

26.7.2.19 MSC DMA Descriptor Address Register (MSC_DMANDA,0x0048)

	MSC_DMANDA																															Base + 0x0048
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	NDA																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	NDA	SDMA Next Descriptor Physical Address The SDMA will change the register when a descriptor is read in. It should be 4-word aligned.	RW

26.7.2.20 MSC DMA Data Address Register (MSC_DMADA,0x004C)

	MSC_DMADA																															Base + 0x004C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DA																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DA	SDMA Data Physical Address The data address of the current descriptor will be copied to this field. The SDMA will increment it during the data transfer automatically.	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

26.7.2.21 MSC DMA Data Length Register (MSC_DMALEN,0x0050)

	MSC_DMALEN																															Base + 0x0050
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LEN																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	LEN	SDMA Data Length to be Transferred Its unit is byte. The data length of the current descriptor will be copied to this field. The SDMA will decrement it during the data transfer automatically.	R

26.7.2.22 MSC DMA Command Register (MSC_DMACMD,0x0054)

	MSC_DMACMD																															Base + 0x0054
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IDI								ID								Reserved					OFFSET		ALIGN_EN	Reserved						ENDI	LINK
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:24	IDI	Identification of the Interrupt DMA. This field will copy the ID when a DMA transfer interrupt occurs. If the interrupt of DMA is disabled, the field will not change.	R
23:16	ID	Identification of Current DMA Transfer.	R
15:11	Reserved	It has no use in the current version.	R
10:9	OFFSET	Address Offset. This field is effective when ALIGN_EN is set to 1b. 00: data address[1:0] is 00b 01: data address[1:0] is 01b 10: data address[1:0] is 10b 11: data address[1:0] is 11b	R
8	ALIGN_EN	Address Align Enable.	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		This bit should be set to 1b if the data address is not word-aligned.	
7:2	Reserved	It has no use in the current version.	R
1	ENDI	Interrupt Enable for Current DMA Transfer End 0: Disable interrupt 1: Enable interrupt	R
0	LINK	Control the end of DMA Descriptor. 0: DMA will go to idle state after the current transmission is finished. The MSC_STAT.DMAEND will be set to 1b when the current read/write is finished. If the interrupt mask bit MSC_IMASK.DMAEND is 0b, the interrupt flag MSC_IFLG. DMAEND will be set to 1b also. 1: DMA will continue to fetch another descriptor.	R

26.7.2.23 MSC Control 2 Register (MSC_CTRL2,0x0058)

	MSC_CTRL2																															Base + 0x0058
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			PIP					Reserved_1	Reserved																		STPRM	Reserved_0	SMS		
RST	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:29	Reserved	Writing has no effect, read as zero.	R
28:24	PIP	Pin Level Interrupt Polarity 1: Interrupt can be trigged when pin level is high 0: Interrupt can be trigged when pin level is low	RW
23	Reserved_1	Inner usage, keep to 1.	RW
22:5	Reserved	Writing has no effect, read as zero.	R
4	STPRM	Stop Read Operation Mode Selection 0: Host can stop read operation during data transfer 1: Host only can stop read operation during block gap	RW
3	Reserved_0	Inner usage, keep to 0.	RW
2:0	SMS	Speed Mode Selection 000: Default speed 001: High speed 010: SDR12 011: SDR25 100: SDR50 Others: reserved	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

26.7.2.24 MSC RTFIFO Data Counter Register(MSC_RTCNT,0x005C)

	MSC_RTCNT																															Base + 0x005C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RTCNT																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	RTCNT	This field indicates how many data in word units are stored in RTFIFO.	R

26.8 Operation Flow

26.8.1 Data FIFOs

The controller FIFOs for the response tokens, received data, and transmitted data are MSC_RES, MSC_RXFIFO, and MSC_TXFIFO, respectively. These FIFOs are accessible by the software and are described in the following paragraphs.

26.8.1.1 Response FIFO (MSC_RES)

The response FIFO, MSC_RES, contains the response received from an MMC/SD card after a command is sent from the controller. MSC_RES is a read-only, 16-bit, and 8-entry deep FIFO.

The FIFO will hold all possible response lengths. Responses that are only one byte long are located on the LSB of the 16-bit entry in the FIFO. The first half-word read from the response FIFO is the most significant half-word of the received response. For example, if the response format is R1, then the response read from RES_FIFO is bit [47:32], bit[31:16], bit[15:0] and in the third half-word only the low 8-bit is effective response [15:8] and the high 8-bit is ignored. If the response format is R2, then the response read from MSC_RES is bit [135:8] and needs reading 8 times.

The FIFO does not contain the response CRC. The status of the CRC check is in the status register, MSC_STAT.

26.8.1.2 Receive/Transmit Data FIFO (MSC_RXFIFO/MSC_TXFIFO)

The receive data FIFO and transmit data FIFO share one 16-entry x 32-bit FIFO, because at one time data are only received or are only transmitted. If it is used to receive data, it is called MSC_RXFIFO and read-only. If it is used to transmit data, it is called MSC_TXFIFO and write-only.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Data FIFO and its controls are cleared to a starting state after a system reset or at the beginning of the operations which include data transfer. (MSC_CMDAT[DATA_EN] == 1)

If at any time MSC_RXFIFO becomes full and the data transmission is not complete, the controller turns the MSC_CLK off to prevent any overflows. When the clock is off, data transmission from the card stops until the clock is turned back on. After MSC_RXFIFO is not full, the controller turns the clock on to continue data transmission. The full status of the FIFO is registered in the MSC_STAT [DATA_FIFO_FULL] bit.

If at any time MSC_TXFIFO becomes empty and the data transmission is not complete, the controller turns the MSC_CLK off to prevent any under run. When the clock is off, data transmission to the card stops until the clock is turned back on. When MSC_TXFIFO is no longer empty, the controller automatically restarts the clock. The empty status of the FIFO is registered in the MSC_STAT [DATA_FIFO_EMPTY] bit.

The FIFO is readable on word (32-bit) boundaries. The max read/written number is 16 words. The controller can correctly process big-endian and little-endian data.

Because at the beginning of the operation which include data transfer (MSC_CMDAT [DATA_EN] == 1), Data FIFO and its controls are cleared, software should guarantee data in FIFO have been read/written before beginning a new command.

26.8.2 DMA and Program I/O

Software may communicate to the MSC controller via the DMA or program I/O. The SDMA and CDMA are supported at the same time. SDMA is the special DMA in MSC controller, while CDMA is the common DMA in DMAC controller.

26.8.2.1 Structure of SDMA Descriptor

SDMA is a descriptor DMA. And a descriptor can be linked to another one by the NDA until the LINK in the 4th word is set to 1b.

A SDMA descriptor includes 4 words.

Word 1: The physical address of the next SDMA descriptor.

Bits	Name	Description
31:0	NDA	Next descriptor physical address. It should be 4-word aligned.

Word 2: The system memory address where the data will be read from or stored to.

Bits	Name	Description

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

31:0	DA	Data Address.

Word 3: The length of data to be transferred.

Bits	Name	Description
31:0	LEN	Unit is byte.

Word 4: The command for the current SDMA.

Bits	Name	Description
31:24	Reserved	It has no use in the current version.
23:16	ID	Identification of Current DMA Transfer.
15:2	Reserved	It has no use in the current version.
1	ENDI	Interrupt Enable for Current DMA Transfer End 0: Disable interrupt 1: Enable interrupt
0	LINK	Control the end of DMA Descriptor. 0: DMA will continue to fetch another descriptor. 1: DMA will go to idle state after the current transfer. The MSC_STAT.DMAEND will be set to 1b when the current read/write is finished. If the interrupt mask bit MSC_IMASK.DMAEND is 0b, the interrupt flag MSC_IFLG. DMAEND will be set to 1b also.

26.8.2.2 Operation of SDMA

Step 1: Prepare the descriptor in system memory

Step 2: If the address is not word boundary, it is suggested to configure MSC_DMAC.ALIGNEN and MSC_DMAC.AOFST

Step 3: Write the descriptor address to MSC_DMANDA

Step 4: Configure MSC controller to read or write operation, e,g, set MSC_NOB, MSC_BLEN and MSC_CMDAT.WRITE_READ etc.

Step 5: If DMAEND interrupt is wanted, clear MSC_IMASK.DMAEND, otherwise, set this bit

Step 6: Select SDMA by setting MSC_DMAC.DMASEL to 0b

Step 7: Start DMA transfer by setting MSC_DMAC.DMAEN

Step 8: Waiting the DMAEND interrupt (if interrupt is used) or status (if interrupt is not used)

Step 9: Disable the SDMA by configuring MSC_DMAC.DMAEN to 0b

26.8.2.3 Operation of CDMA

To access MSC_RXFIFO/MSC_TXFIFO with the DMA, the software must program the DMA to read or write the FIFO with source port width 32-bit, destination port width 32-bit, transfer data size 32-byte, transfer mode single. For example, to write 64 bytes of data to the MSC_TXFIFO,

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

the software must program the DMA as follows:

```
DMA_DCTRn = 2              // Write 2 32-bytes (64 bytes)
DMA_DCCRn[SWDH] = 0        // source port width is 32-bit
DMA_DCCRn[DWDH] = 0        // destination port width is 32-bit
DMA_DCCRn[DS] = 4          // transfer data size is 32-byte
DMA_DCCRn[TM] = 4          // transfer mode is single
DMA_DCCRn[RDIL] = 0        // request detection interval length is 0
```

The number of 32-bytes should be calculated from the number of transferred bytes as follows:

The number of words = (The number of bytes + 31) / 32

If the number of transferred bytes is not the multiple of 4, the controller can correctly process endian.

The DMA trigger level is 8 words, that is to say, the DMA read trigger is when data words in MSC_RXFIFO is >= 8 and the DMA write trigger is when data words in MSC_TXFIFO is < 8. Software can also configure DMA registers based on requirements, but the above 32-byte transfer data size is most efficient.

26.8.2.4 Operation of Program I/O

With program I/O, the software waits for the MSC_IFLG [RXFIFO_RD_REQ] or MSC_IFLG [TXFIFO_WR_REQ] interrupts before reading or writing the respective FIFO.

NOTES:

1. The MSC_CMDAT [DMA_EN] bit must be set to a 1 to enable communication with the DMA and it must be set to a 0 to enable program I/O.
2. DMA can be enabled only after MSC_CMDAT is written, because MSC_CMDAT [DATA_EN] is used to reset TX/RXFIFO.

26.8.3 Start and Stop clock

The software stops the clock as follows:

1. Write MSC_CTRL with 0x01 to stop the MMC/SD bus clock.
2. Wait until MSC_STAT[CLK_EN] becomes zero.

To start the clock the software writes MSC_CTRL with 0x02.

26.8.4 Software Reset

Reset includes the MSC reset and the card reset.

The MSC reset is through MSC_CTRL [RESET] bit.

The card reset is to make the card into idle state. CMD0 (GO_IDLE_STATE) sets the MMC and SD memory cards into idle state. CMD52 (IO_RW_DIRECT, with argument 0x88000C08) reset the SD I/O card. The MMC/SD card are initialized with a default relative card address (RCA = 0x0001 for MMC and RCA = 0x0000 for SD) and with a default driver stage register setting (lowest speed, highest driving current capability).

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

The following registers must be set before the clock is started:

Step 1. Stop the clock.

Step 2. Set MSC_CTRL register to 0x08 to reset MSC.

Step 3. Wait while MSC_STAT [IS_RESETTING] is 1.

Step 4. Set MSC_CMD with CMD0.

Step 5. Update the MSC_CMDAT register as follows:

- a Write 0x0000 to MSC_CMDAT [RESPONSE_FORMAT].
- b Clear the MSC_CMDAT [DATA_EN] bit.
- c Clear the MSC_CMDAT [BUSY] bit.
- d Clear the MSC_CMDAT [INIT] bit.

Step 6. Start the clock.

Step 7. Start the operation. (write MSC_CTRL with 0x04)

Step 8. Wait for the END_CMD_RES interrupt.

Step 9. Set MSC_CMD with CMD52.

Step 10. Set MSC_ARG with 0x88000C08.

Step 11. Update the MSC_CMDAT register as follows:

- a Write 0x005 to MSC_CMDAT [RESPONSE_FORMAT].
- b Clear the MSC_CMDAT [DATA_EN] bit.
- c Clear the MSC_CMDAT [BUSY] bit.
- d Clear the MSC_CMDAT [INIT] bit.

Step 12. Start the operation.

Step 13. Wait for the END_CMD_RES interrupt.

26.8.5 Voltage Validation and Card Registry

At most 10 MMC and 1 SD (either SDMEM or SDIO) can be inserted MMC/SD bus at the same time, and their voltage validation and card registry steps are different, so the software should be programmed as follows:

Step 1. Check whether SDIO card is inserted.

Step 2. Check whether SDMEM card is inserted.

Step 3. Check whether MMC cards are inserted.

26.8.5.1 Check SDIO

The commands are sent as follows:

Step 1. (Optional) Send CMD52 (IO_RW_DIRECT) with argument 0x88000C08 to reset SDIO card.

Step 2. Send CMD5 (IO_SEND_OP_CMD) to validate voltage.

Step 3. If the response is correct and the number of IO functions > 0, then continue, else go to check SDMEM.

Step 4. If C-bit in the response is ready (the initialization has finished), go to 6.

Step 5. Send CMD5 (IO_SEND_OP_CMD) to validate voltage, then go to 4.

Step 6. If memory-present-bit in the response is true, then it is a combo card (SDIO +

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Memory), else it is only a SDIO card.

Step 7. If it is a combo card, go to check SDMEM to initialize the memory part.

Step 8. Send CMD3 (SET_RELATIVE_ADDR) to let the card publish a RCA. The RCA is returned from the response.

Step 9. If do not accept the new RCA, go to 8, else record the new RCA.

Step 10. Go to check MMC, because we can assure that there is no SDMEM card.

26.8.5.2 Check SDMEM

If there is no SDIO card or there is a combo card, continue to check SDMEM.

The commands are sent as follows:

Step 1. (Optional) Send CMD0 (GO_IDLE_STATE) to reset MMC and SDMEM card. This command has no response.

Step 2. Send CMD55. Here the default RCA 0x0000 is used for CMD55.

Step 3. If the response is correct (CMD55 has response), then continue, else go to check MMC.

Step 4. Send ACMD41 (SD_SEND_OP_CMD) to validate voltage (the general OCR value is 0x00FF8000).

Step 5. If the initialization has finished, go to 7. (The response is the OCR register and it includes a status information bit (bit [31]). This status bit is set if the card power up procedure has been finished. As long as the card is busy, the corresponding bit[31] is set to LOW.)

Step 6. Send CMD55 and ACMD41 to validate voltage, and then go to 5.

Step 7. Send CMD2 (ALL_SEND_CID) to get the card CID.

Step 8. Send CMD3 (SET_RELATIVE_ADDR) to let card publish a RCA. The RCA is returned from the response.

Step 9. If do not accept the new RCA, go to 8, else record the new RCA.

Step 10. Go to check MMC.

26.8.5.3 Check MMC

Because there may be several MMC card, so some steps (5 ~ 8) should be repeated several times.

The commands are sent as follows:

Step 1. Send CMD1 (SEND_OP_CMD) to validate voltage (the general OCR value is 0x00FF88000).

Step 2. If the response is correct, then continue, else go to 9.

Step 3. If the initialization has finished, go to 5. (The response is the OCR register and it includes a status information bit (bit [31]). This status bit is set if the card power up procedure has been finished. As long as the card is busy, the corresponding bit[31] is set to LOW.)

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Step 4. Send CMD1 (SEND_OP_CMD) to validate voltage, and then go to 3.
Step 5. Send CMD2 (ALL_SEND_CID) to get the card CID.
Step 6. If the response timeout occurs, go to 9.
Step 7. Send CMD3 (SET_RELATIVE_ADDR) to assign the card a RCA.
Step 8. If there are other MMC cards, then go to 5.
Step 9. Finish.

26.8.6 Single Data Block Write

In a single block write command, the following registers must be set before the operation is started:

Step 1. Set MSC_NOB register to 0x0001.
Step 2. Set MSC_BLKLEN to the number of bytes per block.
Step 3. Update the MSC_CMDAT register as follows:
- a Write 0x001 to MSC_CMDAT [RESPONSE_FORMAT].
- b Write 0x2 to MSC_CMDAT [BUS_WIDTH] if the card is SD, else clear it.
- c Set the MSC_CMDAT [DATA_EN] bit.
- d Set the MSC_CMDAT [WRITE_READ] bit.
- e Clear the MSC_CMDAT [STREAM_BLOCK] bit.
- f Clear the MSC_CMDAT [BUSY] bit.
- g Clear the MSC_CMDAT [INIT] bit.

Step 4. Start the operation.
Step 5. Write MSC_IMASK with some value to unmask the expected interrupts.

Then the software must perform the following steps:

Step 1. Wait for the MSC_IFLG [END_CMD_RES] interrupt.
Step 2. Wait for the MSC_IFLG [DATA_TRAN_DONE] interrupt.
At the same time write data to the MSC_TXFIFO and continue until all of the data have been written to the FIFO.
Step 3. Wait for MSC_IFLG [PROG_DONE] interrupt. This interrupt indicates that the card has finished programming. Certainly software may start another command sequence on a different card.
Step 4. Read the MSC_STAT register to verify the status of the transaction (i.e. CRC error status).

To address a different card, the software sends a select command to that card by sending a basic no data command and response transaction. To address the same card, the software must wait for MSC_IFLG [PROG_DONE] interrupt. This ensures that the card is not in the busy state.

In addition, CMD26 (PROGRAM_CID), CMD27 (PROGRAM_CSD), CMD42 (LOCK/UNLOCK), CMD56 (GEN_CMD: write) and CMD53 (single block write) operations are similar to single block write.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

26.8.7 Single Block Read

In a single block read command, the following registers must be set before the operation is started:

Step 1. Set MSC_NOB register to 0x0001.

Step 2. Set MSC_BLKLEN register to the number of bytes per block.

Step 3. Update the following bits in the MSC_CMDAT register:

- a Write 0x001 to MSC_CMDAT [RESPONSE_FORMAT].
- b Write 0x2 to MSC_CMDAT [BUS_WIDTH] if the card is SD, else clear it.
- c Set the MSC_CMDAT [DATA_EN] bit.
- d Clear the MSC_CMDAT [WRITE_READ] bit.
- e Clear the MSC_CMDAT [STREAM_BLOCK] bit.
- f Clear the MSC_CMDAT [BUSY] bit.
- g Clear the MSC_CMDAT [INIT] bit.

Step 4. Start the operation.

Step 5. Write MSC_IMASK with some value to unmask the expected interrupts.

Then the software must perform the following steps:

Step 1. Wait for the MSC_IFLG [END_CMD_RES] interrupt.

Step 2. Wait for the MSC_IFLG [DATA_TRAN_DONE] interrupt.
At the same time read data from the MSC_RXFIFO as data becomes available in the FIFO, and continue reading until all data is read from the FIFO.

Step 3. Read the MSC_STAT register to verify the status of the transaction (i.e. CRC error status).

In addition, CMD30 (SEND_WRITE_PROT), ACMD13 (SD_STATUS), CMD56 (GEN_CMD-read), ACMD51 (SEND_SCR) and CMD53 (single block read) are similar to single block read.

26.8.8 Multiple Block Write

The multiple block write mode is similar to the single block write mode, except that multiple blocks of data are transferred. Each block is the same length. All the registers are set as they are for the single block write, except that the MSC_NOB register is set to the number of blocks to be written.

The multiple block write mode also requires a stop transmission command, CMD12, after the data is transferred to the card. After the MSC_IFLG [DATA_TRAN_DONE] interrupt occurs, the software must program the controller register to send a stop data transmission command.

If multiple block write with pre-defined block count (refer to MMC spec v-3.3) is used, CMD12 should not be sent.

For SDIO card, CMD53 (multiple block write) is also similar, but when IO abort (CMD52) is

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

sent, MSC_CMDAT [IO_ABORT] should be 1.

Table 26-6 How to stop multiple block write

Operation	Stop condition	Software processing
Open-ended or SDIO infinite	After write MSC_NOB blocks	1 Wait for DATA_TARN_DONE interrupt. 2 Send CMD12 or CMD52. (IO abort) 3 Wait for END_CMD_RES and PRG_DONE interrupt.
Open-ended or SDIO infinite	Stop writing in advance (not write MSC_NOB blocks)	1 Set MSC_CTRL [EXIT_MULTIPLE]. 2 Wait for DATA_TRAN_DONE interrupt. 3 Send CMD12 or CMD52. (IO abort) 4 Wait for END_CMD_RES and PRG_DONE interrupt.
Predefined block or SDIO finite	After writing MSC_NOB blocks	1 Wait for DATA_TRAN_DONE interrupt.
Predefined block or SDIO finite	Stop writing in advance (not write MSC_NOB blocks)	1 Set MSC_CTRL [EXIT_MULTIPLE]. 2 Wait for DATA_TRAN_DONE interrupt. 3 Send CMD12 or CMD52. (IO abort) 4 Wait for END_CMD_RES and PRG_DONE interrupt.

26.8.9 Multiple Block Read

The multiple blocks read mode is similar to the single block read mode, except that multiple blocks of data are transferred. Each block is the same length. All the registers are set as they are for the single block read, except that the MSC_NOB register is set to the number of blocks to be read.

The multiple blocks read mode requires a stop transmission command, CMD12, after the data from the card is received. After the MSC_IFLG [DATA_TRAN_DONE] interrupt has occurred, the software must program the controller registers to send a stop data transmission command. If multiple block read with pre-defined block count (refer to MMC spec v-3.3) is used, CMD12 should not be sent.

For SDIO card, CMD53 (multiple block read) is also similar, but when IO abort (CMD52) is sent, MSC_CMDAT [IO_ABORT] should be 1.

Table 26-7 How to stop multiple block read

Operation	Stop condition	Software processing
Open-ended or SDIO infinite	After reading MSC_NOB blocks	1 Wait for DATA_TRAN_DONE interrupt. 2 Send CMD12 or CMD52. (IO abort)

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		3 Wait for END_CMD_RES interrupt.
Open-ended or SDIO infinite	Stop reading in advance (not write MSC_NOB blocks)	1 Set MSC_CTRL [EXIT_MULTIPLE]. 2 Wait for DATA_TRAN_DONE interrupt. 3 Send CMD12 or CMD52. (IO abort) 4 Wait for END_CMD_RES interrupt.
Predefined block or SDIO finite	After reading MSC_NOB blocks	1 Wait for DATA_TRAN_DONE interrupt.
Predefined block or SDIO finite	Stop reading in advance (not write MSC_NOB blocks)	1 Set MSC_CTRL [EXIT_MULTIPLE]. 2 Wait for DATA_TRAN_DONE interrupt. 3 Send CMD12 or CMD52. (IO abort) 4 Wait for END_CMD_RES interrupt.

26.8.10 Stream Write (MMC)

In a stream write command, the following registers must be set before the operation is started:

1. Update MSC_CMDAT register as follows:
   - a Write 0x001 to the MSC_CMDAT [RESPONSE_FORMAT].
   - b Clear the MSC_CMDAT [BUS_WIDTH] because only MMC support stream write.
   - c Set the MSC_CMDAT [DATA_EN] bit.
   - d Set the MSC_CMDAT [WRITE_READ] bit.
   - e Set the MSC_CMDAT [STREAM_BLOCK] bit.
   - f Clear the MSC_CMDAT [BUSY] bit.
   - g Clear the MSC_CMDAT [INIT] bit.
2. Start the operation.
3. Write MSC_IMASK with some value to unmask the expected interrupts.

Then the software must perform the following steps:

1. Wait for the MSC_IFLG [END_CMD_RES] interrupt.
2. Write data to the MSC_TXFIFO and continue until all of the data is written to the Data FIFO.
3. Stop clock. Wait until MSC_STAT[CLK_EN] becomes 0. The clock must be stopped.
4. Set the command registers for a stop transaction command (CMD12) and other registers.
5. Start the clock and start the operation.
6. Wait for the MSC_IFLG [END_CMD_ERS] interrupt.
7. Wait for the MSC_IFLG [DATA_TRAN_DONE] interrupt.
8. Wait for the MSC_IFLG [PRG_DONE] interrupt. This interrupt indicates that the card has finished programming. Certainly software may start another command sequence on a different card.
9. Read the MSC_STAT register to verify the status of the transaction.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

To address a different card, the software must send a select command to that card by sending a basic no data command and response transaction. To address the same card, the software must wait for MSC_IFLG [PRG_DONE] interrupt. This ensures that the card is not in the busy state.

If partial blocks are allowed (if CSD parameter WRITE_BL_PARTIAL is set) the data stream can start and stop at any address within the card address space, otherwise it shall start and stop only at block boundaries. If WRITE_BL_PARTIAL is not set, 16 more stuff bytes need to be written after the useful written data, otherwise only write the useful written data.

26.8.11 Stream Read (MMC)

In a stream read command, the following registers must be set before the operation is turned on:

1. Update the MSC_CMDAT register as follows:
   a. Write 0x01 to the MSC_CMDAT [RESPONSE_FORMAT].
   b. Clear the MSC_CMDAT [BUS_WIDTH] because only MMC support stream read.
   c. Clear the MSC_CMDAT [WRITE_READ] bit.
   d. Set the MSC_CMDAT [STREAM_BLOCK] bit.
   e. Clear the MSC_CMDAT [BUSY] bit.
   f. Clear the MSC_CMDAT [INIT] bit.
2. Start the operation.
3. Write MSC_IMASK with some value to unmask the expected interrupts.

Then the software must perform the following steps:

1. Wait for the MSC_IFLG [END_CMD_RES] interrupt.
2. Read data from the MSC_RXFIFO and continue until all of the expected data has been read from the FIFO.
3. Write MSC_CTRL [EXIT_TRANSER] with 1. If MSC_STAT[DATA_FIFO_FULL] is 1, then read MSC_RXFIFO to make it not full. Because if data FIFO is full, MSC_CLK is stopped. Here, the data FIFO contains useless data.
4. Set the command registers for a stop transaction command (CMD12) and send it. There is no need to stop the clock.
5. Wait for the MSC_IFLG [END_CMD_RES].
6. Wait for the MSC_IFLG [DATA_TRAN_DONE] interrupt.
7. Read the MSC_STAT register to verify the status of the transaction.

26.8.12 Erase, Select/Deselect and Stop

For CMD7 (SELECT/DESELECT_CARD), CMD12 (STOP_TRANSMISSION) and CMD38 (ERASE), the following registers must be set before the operation is started:

1. Update the MSC_CMDAT register as follows:
   a. Write 0x01 to the MSC_CMDAT [RESPONSE_FORMAT].

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

b Clear the MSC_CMDAT [DATA_EN] bit.
c Clear the MSC_CMDAT [WRITE_READ] bit.
d Clear the MSC_CMDAT [STREAM_BLOCK] bit.
e Set the MSC_CMDAT [BUSY] bit.
f Clear the MSC_CMDAT [INIT] bit.

2 Start the operation.
3 Write MSC_IMASK with some value to unmask the expected interrupts.

Then the software must perform the following steps:

1 Wait for the MSC_IFLG [END_CMD_RES] interrupt.
2 Wait for the MSC_IFLG [PRG_DONE] interrupt. If CMD12 is sent to terminate data read operation, then there is no need to wait for MSC_IFLG [PRG_DONE] interrupt. This interrupt indicates that the card has finished programming. Certainly software may start another command sequence on a different card.

26.8.13 SDIO Suspend/Resume

The actual suspend/resume steps are as follows:

1 During data transfer, send CMD52 to require suspend. BR and RAW flag should be 1.
2 If BS flag in the response is 0, then suspend has been accepted and goto 4.
3 Send CMD52 to query card status. R flag should be 1. Go to 2.
4 Write MSC_CTRL [EXIT_TRANSFER] with 1.
5 Wait for the MSC_IFLG [DATA_TRAN_DONE] interrupt.
6 Read MSC_NOB, MSC_SNOB and etc, save them into variables.
7 Set registers for high priority transfer and start it.
8 Wait until high priority transfer is finished.
9 Restore registers from variables, but MSC_NOB should be (MSC_NOB – MSC_SNOB).
10 Send CMD52 to require resume. FSx should be resumed function number.

26.8.14 SDIO Read Wait

The actual Read Wait steps are as follows:

1 During multiple block read, read MSC_SNOB. If MSC_SNOB is nearby or equal to MSC_NOB, no need to use Read Wait.
2 Write MSC_CTRL [START_READ WAIT] with 1.
3 Wait until MSC_STAT [IS_READ WAIT] becomes 1.
4 Send CMD52 to query card status.
5 Write MSC_CTRL [STOP_READ WAIT] with 1.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

26.8.15 Operation and Interrupt

The software can use polling-status method to operate the MMC/SD card, but this is not the proposed method, because its performance is very low. The proposed method is to use interrupt. Generally there are fixed necessary steps to finish each command. The steps are as follows:

1. (Optional) Stop clock. Poll CLK_EN.
2. Fill the registers (MSC_CMD, MSC_CMDAT, MSC_ARG, MSC_CLKRT, and etc).
3. (Optional) Start clock.
4. Start the operation. Wait for the MSC_IFLG [END_CMD_RES] interrupt.
5. Wait for the MSC_IFLG [DATA_TRAN_DONE] interrupt.
6. Send STOP_TRANS (CMD12) or I/O abort (CMD52). Wait for the MSC_IFLG [END_CMD_ERS] interrupt.
7. Wait for the MSC_IFLG [DATA_TRAN_DONE] interrupt.
8. Wait for the MSC_IFLG [PRG_DONE] interrupt.

26.9 Index

Table 26-8 Description of Proprietary Vocabulary

Name	Description
Block	A number of bytes, basic data transfer unit
CID	Card Identification number register
CRC	Cyclic Redundancy Check
CSD	Card specific Data register
OCR	Operation Conditions Register
Open-drain	A logical interface operation mode. An external resistor or current source is used to pull the interface level to HIGH, the internal transistor pushes it to LOW.
Push-pull	A logical interface operation mode, a complementary pair of transistors is used to push the interface level to High or Low

Table 26-9 The mapping between Commands and Steps

Index	Abbreviation	1	2	3	4	5	6	7	8	Comments
CMD0	GO_IDLE_STATE	Y	Y	Y	Y					
CMD1	SEND_OP_COND	Y	Y	Y	Y					
CMD2	ALL_SEND_CID	Y	Y	Y	Y					
CMD3	SET_RELATIVE_ADDR	Y	Y	Y	Y					
CMD4	SET_DSR	Y	Y	Y	Y					
CMD7	SELECT/DSELECT_CARD	Y	Y	Y	Y				Y	
CMD9	SEND_CID	Y	Y	Y	Y					
CMD10	SEND_CSD	Y	Y	Y	Y					
CMD11	READ_DAT_UNTIL_STOP	Y	Y	Y	Y		Y	Y		

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

CMD12	STOP_TRANSMISSION	Y	Y	Y	Y				Y	
CMD13	SEND_STATUS	Y	Y	Y	Y					
CMD15	GO_INACTIVE_STATE	Y	Y	Y	Y					
CMD16	SET_BLOCKLEN	Y	Y	Y	Y					
CMD17	READ_SINGLE_BLOCK	Y	Y	Y	Y	Y				
CMD18	READ_MULTIPLE_BLOCK	Y	Y	Y	Y	Y	Y			Open-ended
CMD18	READ_MULTIPLE_BLOCK	Y	Y	Y	Y	Y				Predefine blocks
CMD20	WRITE_DAT_UNTIL_STOP	Y	Y	Y	Y		Y	Y	Y	
CMD23	SET_BLOCK_COUNT	Y	Y	Y	Y					
CMD24	WRITE_SINGLE_BLOCK	Y	Y	Y	Y	Y			Y	
CMD25	WRITE_MULTIPLE_BLOCK	Y	Y	Y	Y	Y	Y		Y	Open-ended
CMD25	WRITE_MULTIPLE_BLOCK	Y	Y	Y	Y	Y			Y	Predefine blocks
CMD26	PROGRAM_CID	Y	Y	Y	Y	Y			Y	
CMD27	PROGRAM_CSD	Y	Y	Y	Y	Y			Y	
CMD28	SET_WRITE_PROT	Y	Y	Y	Y				Y	
CMD29	CLR_WRITE_PROT	Y	Y	Y	Y				Y	
CMD30	SEND_WRITE_PROT	Y	Y	Y	Y	Y				
CMD32	ERASE_WR_BLOCK_START	Y	Y	Y	Y					
CMD33	ERASE_WR_BLOCK_END	Y	Y	Y	Y					
CMD35	ERASE_GROUP_START	Y	Y	Y	Y					
CMD36	ERASE_GROUP_END	Y	Y	Y	Y					
CMD38	ERASE	Y	Y	Y	Y				Y	
CMD39	FAST_IO	Y	Y	Y	Y					
CMD40	GO_IRQ_STATE	Y	Y	Y	Y					
CMD42	LOCK/UNLOCK	Y	Y	Y	Y	Y			Y	
CMD55	APP_CMD	Y	Y	Y	Y					
CMD56	GEN_CMD	Y	Y	Y	Y	Y				Read
CMD56	GEN_CMD	Y	Y	Y	Y	Y			Y	Write
ACMD6	SET_BUS_WIDTH	Y	Y	Y	Y					
ACMD13	SD_STATUS	Y	Y	Y	Y	Y				
ACMD22	SEND_NUM_WR_BLOCKS	Y	Y	Y	Y					
ACMD23	SET_WR_BLOCK_COUNT	Y	Y	Y	Y					
ACMD41	SD_SEND_OP_COND	Y	Y	Y	Y					
ACMD42	SET_CLR_CARD_DETECT	Y	Y	Y	Y					
ACMD51	SEND_SCR	Y	Y	Y	Y	Y				

Note:

For stream read/write, STOP_CMD is sent after finishing data transfer. For write, STOP_CMD is with the last six bytes. For read, STOP_CMD is sent after receiving data and card sends some data which MSC ignores.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

27 ON-THE-GO Controller(OTG)

27.1 Overview

This chapter describes the USB On-The-Go (OTG) implemented in the processor.
The Universal Serial Bus (USB) supports serial data exchanges between a host computer and a variety of simultaneously accessible portable peripherals. Many of these portable devices would benefit a lot from being able to communicate to each other over the USB interface. And OTG make this possible. An OTG device can plays the role of both host and device.
Familiarity with the Universal Serial Bus Specification, Revision 1.1 and OTG supplement are necessary to fully understand the material contained in this section.

27.2 Features

- Complies with the USB 2.0 standard for high-speed (480 Mbps) functions and with the *On-The-Go* supplement to the USB 2.0 specification
- Operates either as the function controller of a high- /full-speed USB peripheral or as the host/peripheral in point-to-point or multi-point communications with other USB functions
- Supports Session Request Protocol (SRP) and Host Negotiation Protocol (HNP)
- UTMI+ Level 3 Transceiver Interface
- Soft connect/disconnect
- 16 Endpoints
- Supports control, interrupt, ISO and bulk transfer

27.3 Functional Description

The OTG is a Dual-Role Device(DRD) controller that supports both device and host functions and complies fully with the On-The-Go Supplement to the USB 2.0 Specification ,Revision 1.3a and Revision 2.0.It can also be configured as a host-only or device-only controller , fully compliant with the USB 2.0 Specification.

27.4 Pins Description

DRV_VBUS：PC17,USB 5-V Signal.
Function: This is the USB 5-V supply. A charge pump external to USB2.0 picoPHY must provide power to this pin. The nominal voltage for this pin is 5V. If VBUS is not used ,leave it floating.

27.5 Data Format Description

Support UTMI 8/16 for the USB-Phy Interface.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

27.6 Register Desciption

Following chapter will describe the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. Register read/write attribute
   R- Read only
   W- Write only
   RW- Read and Write
   RCW- Read and Write, but Clear to 0 by Read
   RSW- Read and Write, but Set to 1 by Read
   RWC- Read and Write, Clear to 0 by Write 1, Write 0 has no effect
   RWS- Read and Write, Set to 1 by Write 1, Write 0 has no effect
   RC- Read only, and Clear to 0 by read
   RS- Read only, and Set to 1 by read
3. Reset Value
   1 - reset to 1
   0 - reset to 0
   ? - value unknown after reset

27.6.1 Register Memory Map

Table 27-1 Registers Memory Map Base Address

Name	Base	Description
OTG	0x13500000	Address base of OTG

The On-The-Go Controller is controlled by a set of registers that the application configures before every operation. The following table lists all the registers.

Table 27-2 On-The-Go（OTG） Registers Map

Name	RW	Reset Value	Address Offset	Access Size
GOTGCTL	RW	0x0???_0000	0x000	32
GOTGINT	RW	0x0000_0000	0x004	32
GAHBCFG	RW	0x0000_0000	0x008	32
GUSBCFG	RW	0x0?00_140?	0x00C	32
GRSTCTL	RW	0x8000_0000	0x010	32
GINTSTS	RW	0x0400_0020	0x014	32
GINTMSK	RW	0x0000_0000	0x018	32
GRXSTSR	R	0x0000_0000	0x01C	32
GRXSTSP	R	0x0000_0000	0x020	32
GRXFSIZ	RW	0x0000_????	0x024	32
GNPTXFSIZ	RW	0x????_????	0x028	32
GNPTXSTS	RW	0x00??_????	0x02C	32

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

GHWCFG1	R	0x????_????	0x044	32
GHWCFG2	R	0x????_????	0x048	32
GHWCFG3	R	0x????_????	0x04C	32
GHWCFG4	R	0x????_?0??	0x050	32
GDFIFOCFG	RW	0x????_????	0x05C	32
HPTXFSIZ	RW	0x????_????	0x100	32
DIEPTXFn	RW	0x????_????	0x104+n*0x4	32
HCFG	RW	0x0000_0200	0x400	32
HFIR	RW	0x0000_EA60	0x404	32
HFNUM	R	0x0000_3FFF	0x408	32
HPTXSTS	R	0x00??_????	0x410	32
HAINT	R	0x0000_0000	0x414	32
HAINTMAK	RW	0x0000_0000	0x418	32
HPRT	RW	0x0000_0000	0x440	32
HCCHARn	RW	0x0000_0000	0x500+n*0x20	32
HCSPLTn	RW	0x0000_0000	0x504+n*0x20	32
HCINTn	RW	0x0000_0000	0x508+n*0x20	32
HCINTMSKn	RW	0x0000_0000	0x50c+n*0x20	32
HCTSIZn	RW	0x0000_0000	0x510+n*0x20	32
HCDMAn	RW	0x0000_0000	0x514+n*0x20	32
HCDMABn	R	0x????_????	0x51C+n*0x20	32
DCFG	RW	0x0820_0000	0x800	32
DCTL	RW	0x0000_0002	0x804	32
DSTS	R	0x0000_0002	0x808	32
DIEPMSK	RW	0x0000_0000	0x810	32
DOEPMSK	RW	0x0000_0000	0x814	32
DAINT	R	0x0000_0000	0x818	32
DAINTMSK	RW	0x0000_0000	0x81C	32
DTKNQR1	R	0x0000_0000	0x820	32
DTKNQR2	R	0x0000_0000	0x824	32
DTKNQR3	R	0x0000_0000	0x830	32
DTKNQR4	R	0x0000_0000	0x834	32
DVBUSDIS	RW	0x0000_????	0x828	32
DVBUSPULSE	RW	0x0000_0???	0x82C	32
DTHRCTL	RW	0x0810_0020	0x830	32
DIEPEMPMSK	RW	0x0000_0000	0x834	32
DEACHINT	R	0x0000_0000	0x838	32
DEACHINTMSK	RW	0x0000_0000	0x83C	32
DIEPEACHMSKn	RW	0x0000_0000	0x840	32
DOEPEACHMSKn	RW	0x0000_0000	0x844	32
DIEPCTL0	RW	0x0000_8000	0x900	32

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

DOEPCTL0	RW	0x0000_8000	0xB00	32
DIEPCTLn/DOEPCTLn	RW	0x0000_0000	0x900/0xB00+n*0x20	32
DIEPINTn/DOEPINTn	RW	0x0000_0080	0x908/0xB08+n*0x20	32
DIEPTSIZ0/DOEPTSIZ0	RW	0x0000_0000	0x910/0xB10	32
DIEPTSIZn/DOEPTSIZn	RW	0x0000_0000	0x910/0xB10+n*0x20	32
DIEPDMAn/DOEPDMAn	RW	0x????_????	0x914/0xB14+n*0x20	32
DIEPDMABn/DOEPDMABn	R	0x????_????	0x91C/0xB1C+n*0x20	32
DTXFSTSn	R	0x0000_0000	0x918	32

27.6.2 Register and Fields Description

27.6.2.1 Control and Status Register (GOTGCTL,0x000)

	GOTGCTL																															Base + 0x000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				chirpen	MultValIdBc					Reserved	OTGVer	BSesVld	ASesVld	DbncTime	ConIDSts	Reserved				DevHNPEn	HstSetHNPEn	HNPReq	HstNegScs	BvalidOvVa	BvalidOvEn	AvalidOvVal	AvalidOvEn	VbvalidOvVal	VbvalidOvEn	SesReq	SesReqScs
RST	0	0	0	0	0	?	?	?	?	?	0	0	?	?	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	Mode	R/W
31:26	Reserved	Host and Device	R
27	Chirp On Enable (ChirpEn) This bit when programmed to 1'b1 results in the core asserting chirp_on before sending an actual Chirp "K" signal on USB. This bit is present only if OTG_BC_SUPPORT = 1.If OTG_BC_SUPPORT!=1, this bit is a reserved bit.	Device only	RW
26:22[1]	Multi Valued ID pin (MultValIdBc) Battery Charger ACA inputs in the following order: Bit 26 - rid_float. Bit 25 - rid_gnd Bit 24 - rid_a Bit 23 - rid_b Bit 22 - rid_c These bits are valid only if OTG_BC_SUPPORT=1, otherwise they are reserved.	Host and Device	R
21	Reserved	Host and Device	R
20	OTG Version (OTGVer) Indicates the OTG revision. 1'b0: OTG Version 1.3. In this version the core supports Data line pulsing and VBus pulsing for SRP.	Host and Device	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	1'b1: OTG Version 2.0. In this version the core supports only Data line pulsing for SRP.		
19	B-Session Valid (BSesVld) Indicates the Device mode transceiver status. 1'b0: B-session is not valid. 1'b1: B-session is valid. In OTG mode, you can use this bit to determine if the device is connected or disconnected. **Note:** If you do not enable OTG features (such as SRP and HNP), the read reset value will be 1.The vbus assigns the values internally for non- SRP or non-HNP configurations. In case of OTG_MODE=0, the reset value of this bit is 1'b0.	Device only	R
18	A-Session Valid (ASesVld) Indicates the Host mode transceiver status. 1'b0: A-session is not valid 1'b1: A-session is valid **Note:** If you do not enable OTG features (such as SRP and HNP), the read reset value will be 1.The vbus assigns the values internally for non- SRP or non-HNP configurations. In device mode, this bit is reserved.	Host only	R
17	Long/Short Debounce Time (DbncTime) Indicates the debounce time of a detected connection. 1'b0: Long debounce time, used for physical connections (100 ms + 2.5 μs) 1'b1: Short debounce time, used for soft connections (2.5 μs)	Host only	R
16	Connector ID Status (ConIDSts) Indicates the connector ID status on a connect event. 1'b0: The DWC_otg core is in A-Device mode 1'b1: The DWC_otg core is in B-Device mode	Host and Device	R
15:12	Reserved	Host and Device	R
11	Device HNP Enabled (DevHNPEn) The application sets this bit when it successfully receives a SetFeature.SetHNPEnable command from the connected USB host. 1'b0: HNP is not enabled in the application 1'b1: HNP is enabled in the application	Device Only OTG configura tions	RW
10	Host Set HNP Enable (HstSetHNPEn) The application sets this bit when it has successfully enabled HNP (using the SetFeature.SetHNPEnable command) on the connected device. 1'b0: Host Set HNP is not enabled 1'b1: Host Set HNP is enabled	Device Only OTG configura tions	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

9	HNP Request (HNPReq) The application sets this bit to initiate an HNP request to the connected USB host. The application can clear this bit by writing a 0 when the Host Negotiation Success Status Change bit in the OTG Interrupt register (GOTGINT.HstNegSucStsChng) is set. The core clears this bit when the HstNegSucStsChng bit is cleared. 1'b0: No HNP request 1'b1: HNP request	Device Only OTG configura tions	RW
8	Host Negotiation Success (HstNegScs) The core sets this bit when host negotiation is successful. The core clears this bit when the HNP Request (HNPReq) bit in this register is set. 1'b0: Host negotiation failure 1'b1: Host negotiation success	Device only	R
7	B-Peripheral Session Valid OverrideValue (BvalidOvVal) This bit is used to set the Override value for Bvalid signal when GOTGCTL.BvalidOvEn is set. 1'b0: Bvalid value is 1'b0 when GOTGCTL.BvalidOvEn = 1. 1'b1: Bvalid value is 1'b1 when GOTGCTL.BvalidOvEn = 1.	Device only	RW
6	B-Peripheral Session Valid Override Enable (BvalidOvEn) This bit is used to enable/disable the software to override the Bvalid signal using the GOTGCTL.BvalidOvVal. 1'b1: Internally Bvalid received from the PHY is overridden with GOTGCTL.BvalidOvVal. 1'b0: Override is disabled and Bvalid signal from the respective PHY selected is used internally by the core.	Device only	RW
5	A-Peripheral Session Valid OverrideValue (AvalidOvVal) This bit is used to set the Override value for Avalid signal when GOTGCTL.AvalidOvEn is set. 1'b0: Avalid value is 1'b0 when GOTGCTL.AvalidOvEn = 1. 1'b1: Avalid value is 1'b1 when GOTGCTL.AvalidOvEn = 1.	Host only	RW
4	A-Peripheral Session Valid Override Enable (AvalidOvEn) This bit is used to enable/disable the software to override the Avalid signal using the GOTGCTL.AvalidOvVal. 1'b1: Internally Avalid received from the PHY is overridden with GOTGCTL.AvalidOvVal. 1'b0: Override is disabled and Avalid signal from the respective PHY is used internally by the core.	Host only	RW
3	VBUS Valid OverrideValue (VbvalidOvVal) This bit is used to set the Override value for vbus valid signal when GOTGCTL.VbusvalidOvEn is set.	Host only	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	1'b0: vbusvalid value is 1'b0 when GOTGCTL.VbvalidOvEn = 1. 1'b1: vbusvalid value is 1'b1 when GOTGCTL.VbvalidOvEn = 1.		
2	VBUS Valid Override Enable (VbvalidOvEn) This bit is used to enable/disable the software to override the vbus-valid signal using the GOTGCTL.vbvalidOvVal. 1'b1: The vbus-valid signal received from the PHY is overridden with GOTGCTL.vbvalidOvVal. 1'b0: Override is disabled and avalid signal from the respective PHY is used internally by the core.	Host only	RW
1	Session Request (SesReq) The application sets this bit to initiate a session request on the USB. The application can clear this bit by writing a 0 when the Host Negotiation Success Status Change bit in the OTG Interrupt register (GOTGINT.HstNegSucStsChng) is set. The core clears this bit when the HstNegSucStsChng bit is cleared. If you use the USB 1.1 Full-Speed Serial Transceiver interface to initiate the session request, the application must wait until the VBUS discharges to 0.2 V, after the B-Session Valid bit in this register (GOTGCTL.BSesVld) is cleared. This discharge time varies between different PHYs and can be obtained from the PHY vendor. 1'b0: No session request 1'b1: Session request	Device only	RW
0	Session Request Success (SesReqScs) The core sets this bit when a session request initiation is successful. 1'b0: Session request failure 1'b1: Session request success	Device only	R

Note:

[1]. bits [26:22]: configurable. The reset value is unknown if OTG_BC_ SUPPORT=1 and 0 otherwise.

27.6.2.2 Interrupt Register (GOTGINT,0x004)

	GOTGINT																															Base + 0x004
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved												MVIC	DbnceDone	ADevTOUTCh		Reserved						HstNegSucStsChng	SesReqSucStsChng	Reserved					SesEndDet	Reserved	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Description	Mode	R/W
31:21	Reserved	Host and Device	R
20	Multi-Valued input changed (MVIC) This bit when set indicates that there is a change in the value of at least one ACA pin value. This bit is present only if OTG_BC_SUPPORT = 1, otherwise it is reserved.	Host and Device	RW[1]
19	Debounce Done (DbnceDone) The core sets this bit when the debounce is completed after the device connect. The application can start driving USB reset after seeing this interrupt. This bit is only valid when the HNP Capable or SRP Capable bit is set in the Core USB Configuration register (GUSBCFG.HNPCap or GUSBCFG.SRPCap, respectively).	Host Only	RW[2]
18	A-Device Timeout Change (ADevTOUTChg) The core sets this bit to indicate that the A-device has timed out while waiting for the B-device to connect.	Host and Device	RW[3]
17	Host Negotiation Detected (HstNegDet) The core sets this bit when it detects a host negotiation request on the USB.	Host and Device	RW[4]
16:10	Reserved	Host and Device	R
9	Host Negotiation Success Status Change (HstNegSucStsChng) The core sets this bit on the success or failure of a USB host negotiation request. The application must read the Host Negotiation Success bit of the OTG Control and Status register (GOTGCTL.HstNegScs) to check for success or failure.	Host and Device	RW[5]
8	Session Request Success Status Change (SesReqSucStsChng) The core sets this bit on the success or failure of a session request. The application must read the Session Request Success bit in the OTG Control and Status register (GOTGCTL.SesReqScs) to check for success or failure.	Host and Device	RW[6]
7:3	Reserved	Host and Device	R
2	Session End Detected (SesEndDet) The core sets this bit when the utmisrp_bvalid signal is deasserted.	Device only	RW[7]
1:0	Reserved	Host and Device	R

Note:

[1]~[7]: This bits will operate with Self set , Write clear function.

27.6.2.3 AHB Configuration Register (GAHBCFG,0x008)

	GAHBCFG																															Base + 0x008
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Reserved								AHBSingle	NotiAllDmaWrit	RemMemSupp	Reserved												PTxFEmpLvl	NPTxFEmpLvl	Reserved	DMAEn	HBstLen				GlbIntrMsk
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	Mode	R/W
31:24	Reserved	Host and Device	R
23	AHB Single Support (AHBSingle) This bit when programmed supports Single transfers for the remaining data in a transfer when the DWC_otg core is operating in DMA mode. 1'b0: This is the default mode. When this bit is set to 1'b0, the remaining data in the transfer is sent using INCR burst size. 1'b1: When set to 1'b1, the remaining data in a transfer is sent using Single burst size. Note: if this feature is enabled, the AHB RETRY and SPLIT transfers still have INCR burst type. Enable this feature when the AHB Slave connected to the DWC_otg core does not support INCR burst (and when Split, and Retry transactions are not being used in the bus).	Host and Device	RW
22	Notify All Dma Write Transactions (NotiAllDmaWrit) This bit is programmed to enable the System DMA Done functionality for all the DMA write Transactions corresponding to the Channel/Endpoint. This bit is valid only when GAHBCFG.RemMemSupp is set to 1. GAHBCFG.NotiAllDmaWrit = 1 HS OTG core asserts int_dma_req for all the DMA write transactions on the AHB interface along with int_dma_done, chep_last_transact and chep_number signal informations. The core waits for sys_dma_done signal for all the DMA write transactions in order to complete the transfer of a particular Channel/Endpoint. GAHBCFG.NotiAllDmaWrit = 0 HS OTG core asserts int_dma_req signal only for the last transaction of DMA write transfer corresponding to a particular Channel/Endpoint. Similarly, the core waits for sys_dma_done signal only for that transaction of DMA write to complete the transfer of a particular Channel/Endpoint.	Host and Device	RW
21	Remote Memory Support (RemMemSupp)	Host and Device	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	This bit is programmed to enable the functionality to wait for the system DMA Done Signal for the DMA Write Transfers. GAHBCFG.RemMemSupp=1 The int_dma_req output signal is asserted when HS OTG DMA starts write transfer to the external memory. When the core is done with the Transfers it asserts int_dma_done signal to flag the completion of DMA writes from HS OTG. The core then waits for sys_dma_done signal from the system to proceed further and complete the Data Transfer corresponding to a particular Channel/Endpoint. GAHBCFG.RemMemSupp=0 The int_dma_req and int_dma_done signals are not asserted and the core proceeds with the assertion of the XferComp interrupt as soon as the DMA write transfer is done at the HS OTG Core Boundary and it doesn't wait for the sys_dma_done signal to complete the DATA transfers.		
20:9	Reserved	Host and Device	R
8	Periodic TxFIFO Empty Level (PTxFEmpLvl) Indicates when the Periodic TxFIFO Empty Interrupt bit in the Core Interrupt register (GINTSTS.PTxFEmp) is triggered. This bit is used only in Slave mode. 1'b0: GINTSTS.PTxFEmp interrupt indicates that the Periodic TxFIFO is half empty 1'b1: GINTSTS.PTxFEmp interrupt indicates that the Periodic TxFIFO is completely empty	Host only	RW
7	Non-Periodic TxFIFO Empty Level (NPTxFEmpLvl) This bit is used only in Slave mode. In host mode and with Shared FIFO with device mode, this bit indicates when the Non-Periodic TxFIFO Empty Interrupt bit in the Core Interrupt register (GINTSTS.NPTxFEmp) is triggered. With dedicated FIFO in device mode, this bit indicates when IN endpoint Transmit FIFO empty interrupt (DIEPINTn.TxFEmp) is triggered. Host mode and with Shared FIFO with device mode: 1'b0: GINTSTS.NPTxFEmp interrupt indicates that the Non-Periodic TxFIFO is half empty 1'b1: GINTSTS.NPTxFEmp interrupt indicates that the Non-Periodic TxFIFO is completely empty Dedicated FIFO in device mode: 1'b0: DIEPINTn.TxFEmp interrupt indicates that the IN Endpoint TxFIFO is half empty 1'b1: DIEPINTn.TxFEmp interrupt indicates that the IN Endpoint TxFIFO is completely empty	Host and Device	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

6	Reserved	Host and Device	R
5	DMA Enable (DMAEn) 1'b0: Core operates in Slave mode 1'b1: Core operates in a DMA mode	Host and Device	RW
4:1	Burst Length/Type (HBstLen) This Bits is used in both External and Internal DMA modes. In External DMA mode, these bits appear on dma_burst[3:0] ports, which can be used by an external wrapper to interface the External DMA Controller interface to Synopsys DW_ahb_dmac or ARM PrimeCell. External DMA Mode — defines the DMA burst length in terms of 32-bit words: 4'b0000: 1 word 4'b0001: 4 words 4'b0010: 8 words 4'b0011: 16 words 4'b0100: 32 words 4'b0101: 64 words 4'b0110: 128 words 4'b0111: 256 words Others: Reserved Internal DMA Mode — AHB Master burst type: 4'b0000 Single 4'b0001 INCR 4'b0011 INCR4 4'b0101 INCR8 4'b0111 INCR16 Others: Reserved Slave Mode: Only single burst is supported.	Host and Device	RW
0	Global Interrupt Mask (GlblIntrMsk) The application uses this bit to mask or unmask the interrupt line assertion to itself. Irrespective of this bit's setting, the interrupt status registers are updated by the core. 1'b0: Mask the interrupt assertion to the application. 1'b1: Unmask the interrupt assertion to the application.	Host and Device	RW

27.6.2.4 USB Configuration Register (GUSBCFG,0x00C)

	GUSBCFG																															Base + 0x00C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Txpacket	ForceDevMode	ForceHstMode	TxEndDelay	IC_USBTrafCtl	C_USBCap	ULIPPectDis	IndiPass	IndiComp	TermSelDLPulse	ULPIExtVbusIndicator	ULPIExtVbusDrv	ULPIClkSusM	ULPIAutoRes	ULPIFsLs	OtgI2CSel	PhyLPwrClkSel	Reserved	USBTrdTim				HNPCap	SRPCap	DDRSel	PHYSel	FSIntf	ULPI_UTMI_Sel	PHYIf	TOutCal		
RST	0	0	0	0	0	?	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	?	0	0	0

Bits	Description	Mode	R/W
31	Corrupt Tx packet(Txpacket) This bit is for debug purposes only. Never set this bit to 1.	Host and Device	W
30	Force Device Mode (ForceDevMode) Writing a 1 to this bit forces the core to device mode irrespective of utmiotg_iddig input pin. 1'b0: Normal Mode 1'b1: Force Device Mode After setting the force bit, the application must wait at least 25 ms before the change to take effect. When the simulation is in scale down mode, waiting for 500 µs is sufficient.	Host and Device	RW
29	Force Host Mode (ForceHstMode) Writing a 1 to this bit forces the core to host mode irrespective of utmiotg_iddig input pin. 1'b0: Normal Mode 1'b1: Force Host Mode After setting the force bit, the application must wait at least 25 ms before the change to take effect. When the simulation is in scale down mode, waiting for 500 µs is sufficient.	Host and Device	RW
28	Tx End Delay (TxEndDelay) Writing a 1 to this bit enables the TxEndDelay timers in the core as per the section 4.1.5 on Opmode of the USB 2.0 Transceiver Macrocell Interface (UTMI) version 1.05. 1'b0: Normal mode 1'b1: Introduce Tx end delay timers	Device Only	RW
27	IC_USB TrafficPullRemove Control (IC_USBTrafCtl) When this bit is set, pullup/pulldown resistors are detached from the USB during traffic signaling, per section 6.3.4 of the IC_USB specification. This bit is invalid.	Device	RW
26	IC_USB-Capable (IC_USBCap) The application uses this bit to control the DWC_otg core's IC_USB capabilities.	Host and Device	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	1'b0: IC_USB PHY Interface is not selected. 1'b1: IC_USB PHY Interface is selected. This bit is set to 1'b0 and the bit is read only.		
25	ULPI Interface Protect Disable (ULIPPectDis) Controls circuitry built into the PHY for protecting the ULPI interface when the link tri-states STP and data. Any pull-ups or pull-downs employed by this feature can be disabled. 1'b0: Enables the interface protect circuit 1'b1: Disables the interface protect circuit This bit is reserved and read-only.	Host only	R
24	Indicator Pass Through(IndiPass) Controls wether the Complement Output is qualified with the Internal Vbus Valid comparator before being used in the Vbus State in the RX CMD. Please refer to the ULPI Specification for more detail. 1'b0: Complement Output signal is qualified with the Internal VbusValid comparator. 1'b1: Complement Output signal is not qualified with the Internal VbusValid comparator. This bit is reserved and read-only.	Host Only	R
23	Indicator Complement(IndiComp) Controls the PHY to invert the ExternalVbusIndicator input signal, generating the Complement Output. Please refer to the ULPI Specification for more detail 1'b0: PHY does not invert ExternalVbusIndicator signal 1'b1: PHY does invert ExternalVbusIndicator signal This bit is reserved and read-only.	Host Only	R
22	TermSel DLine Pulsing Selection (TermSelDLPulse) This bit selects utmi_termselect to drive data line pulse during SRP. 1'b0: Data line pulsing using utmi_txvalid (default). 1'b1: Data line pulsing using utmi_termsel.	Device Only	RW
21	ULPI External VBUS Indicator (ULPIExtVbusIndicator) This bit indicates to the ULPI PHY to use an external VBUS over-current indicator. 1'b0: PHY uses internal VBUS valid comparator. 1'b1: PHY uses external VBUS valid comparator. This bit is invalid.	Host Only	RW
20	ULPI External VBUS Drive (ULPIExtVbusDrv)	Host Only	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	This bit selects between internal or external supply to drive 5V on VBUS, in ULPI PHY. 1'b0: PHY drives VBUS using internal charge pump (default). 1'b1: PHY drives VBUS using external supply. This bit is invalid.		
19	ULPI Clock SuspendM (ULPIClkSusM) This bit sets the ClockSuspendM bit in the Interface Control register on ULPI PHY. 1'b0: PHY powers down internal clock during suspend. 1'b1: PHY does not power down internal clock. This bit is invalid.	Host and Device	RW
18	ULPI Auto Resume (ULPIAutoRes) This bit sets the AutoResume bit in the Interface Control register on the ULPIPHY. 1'b0: PHY does not use AutoResume feature. 1'b1: PHY uses AutoResume feature. This bit is invalid.	Host and Device	RW
17	ULPI FS/LS Select (ULPIFsLs) The application uses this bit to select the FS/LS serial interface for the ULPI PHY. This bit is valid only when the FS serial transceiver is selected on the ULPI PHY. 1'b0: ULPI interface 1'b1: ULPI FS/LS serial interface	Host and Device	RW
16	UTMIFS or I2C Interface Select (OtgI2CSel) The application uses this bit to select the I2C interface. 1'b0: UTMI USB 1.1 Full-Speed interface for OTG signals 1'b1: I 2C interface for OTG signals This bit is writable only if I 2C and UTMIFS were specified for Enable I2C Interface	Host and Device	R/RW
15	PHY Low-Power Clock Select (PhyLPwrClkSel) Selects either 480-MHz or 48-MHz (low-power) PHY mode. In FS and LS modes, the PHY can usually operate on a 48-MHz clock to save power. 1'b0: 480-MHz Internal PLL clock 1'b1: 48-MHz External Clock In 480 MHz mode, the UTMI interface operates at either 60 or 30-MHz, depending upon whether 8- or 16-bit data width is selected. In 48-MHz mode, the UTMI interface operates at 48 MHz in FS and LS modes. This bit drives the utmi_fsls_low_power core output signal, and is valid only for UTMI+ PHYs.	Host and Device	RW
14	Reserved	Host and Device	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

13:10	USB Turnaround Time (USBTrdTim) Sets the turnaround time in PHY clocks. Specifies the response time for a MAC request to the Packet FIFO Controller (PFC) to fetch data from the DFIFO (SPRAM). This must be programmed to 4'h5: When the MAC interface is 16-bit UTMI+. 4'h9: When the MAC interface is 8-bit UTMI+. Note: The values above are calculated for the minimum AHB frequency of 30 MHz. USB turnaround time is critical for certification where long cables and 5-Hubs are used, so if you need the AHB to run at less than 30 MHz, and if USB turnaround time is not critical, these bits can be programmed to a larger value.	Device Only	RW
9	HNP-Capable (HNPCap) The application uses this bit to control the DWC_otg core's HNP capabilities. 1'b0: HNP capability is not enabled. 1'b1: HNP capability is enabled. This bit is writable only if an HNP mode was specified for Mode of operation in coreConsultant (parameter OTG_MODE). Otherwise, reads return 0. If HNP functionality is disabled by the software, the OTG signals on the PHY domain must be tied to the appropriate values.	Host and Device	R/RW
8	SRP-Capable (SRPCap) The application uses this bit to control the DWC_otg core SRP capabilities. If the core operates as a non-SRP-capable B-device, it cannot request the connected A-device (host) to activate VBUS and start a session. 1'b0: SRP capability is not enabled. 1'b1: SRP capability is enabled. If SRP functionality is disabled by the software, the OTG signals on the PHY domain must be tied to the appropriate values.	Host and Device	RW
7	ULPI DDR Select (DDRSel) The application uses this bit to select a Single Data Rate (SDR) or Double Data Rate (DDR) or ULPI interface. 1'b0: Single Data Rate ULPI Interface, with 8-bit-wide data bus 1'b1: Double Data Rate ULPI Interface, with 4-bit-wide data bus This bit is invalid.	Host and Device	RW
6	USB 2.0 High-Speed PHY or USB 1.1 Full-Speed Serial Transceiver Select (PHYSel) The application uses this bit to select either a high-speed UTMI+ or ULPI PHY, or a full-speed transceiver. 1'b0: USB 2.0 high-speed UTMI+ or ULPI PHY	Host and Device	R/RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	1'b1: USB 1.1 full-speed serial transceiver This bit is always 0, with Read Only access.		
5	Full-Speed Serial Interface Select (FSIntf) The application uses this bit to select either a unidirectional or bidirectional USB 1.1 full-speed serial transceiver interface. 1'b0: 6-pin unidirectional full-speed serial interface 1'b1: 3-pin bidirectional full-speed serial interface This bit is always 0, with Read Only access.	Host and Device	R/RW
4	ULPI or UTMI+ Select (ULPI_UTMI_Sel) The application uses this bit to select either a UTMI+ interface or ULPI Interface. 1'b0: UTMI+ Interface 1'b1: ULPI Interface This bit takes effect only if GUSBCFG.PHYSel = 1'b0.	Host and Device	R/RW
3	PHY Interface (PHYIf) The application uses this bit to configure the core to support a UTMI+ PHY with an 8- or 16-bit interface. When a ULPI PHY is chosen, this must be set to 8-bit mode. 1'b0: 8 bits 1'b1: 16 bits This bit is writable only if UTMI+ and ULPI were selected in coreConsultant configuration (parameter = 2). Otherwise, this bit returns the value for the power-on interface selected during configuration.	Host and Device	R/RW
2:0	HS/FS Timeout Calibration (TOutCal) The number of PHY clocks that the application programs in this Bits is added to the high-speed/full-speed interpacket timeout duration in the core to account for any additional delays introduced by the PHY. This can be required, because the delay introduced by the PHY in generating the line state condition can vary from one PHY to another. The USB standard timeout value for high-speed operation is 736 to 816 (inclusive) bit times. The USB standard timeout value for full-speed operation is 16 to 18 (inclusive) bit times. The application must program this Bits based on the speed of enumeration. The number of bit times added per PHY clock are: High-speed operation: One 30-MHz PHY clock = 16 bit times One 60-MHz PHY clock = 8 bit times Full-speed operation: One 30-MHz PHY clock = 0.4 bit times One 60-MHz PHY clock = 0.2 bit times One 48-MHz PHY clock = 0.25 bit times	Host and Device	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Using the HS as an example, if you set ToutCal to '001' you add one 30MHz PHY clock or 16 bit times. If you set ToutCal to '010' you add two 30MHz PHY clocks or 32 bit times, and so on. The 3 bits allow you to add up to 7 PHY clocks, and the number of bit times depend on the speed, and the PHY clock you are using.		

27.6.2.5 Reset Register (GRSTCTL,0x010)

	GRSTCTL																															Base + 0x010
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	AHBIdle	DMAReq	Reserved																			DMAReq					TxFFlsh	RxFFlsh	INTknQFlsh	FrmCntrRst	Reserved	CSftRst
RST	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	Mode	R/W
31	AHB Master Idle (AHBIdle) Indicates that the AHB Master State Machine is in the IDLE condition.	Host and Device	R
30	DMA Request Signal (DMAReq) Indicates that the DMA request is in progress. Used for debug.	Host and Device	R
29:11	Reserved	Host and Device	R
10:6	TxFIFO Number (TxFNum) This is the FIFO number that must be flushed using the TxFIFO Flush bit. This Bits must not be changed until the core clears the TxFIFO Flush bit. 5'h0: Non-periodic TxFIFO flush in Host mode Non-periodic TxFIFO flush in device mode when in shared FIFO operation Tx FIFO 0 flush in device mode when in dedicated FIFO mode 5'h1: Periodic TxFIFO flush in Host mode Periodic TxFIFO 1 flush in Device mode when in shared FIFO operation TXFIFO 1 flush in device mode when in dedicated FIFO mode 5'h2: Periodic TxFIFO 2 flush in Device mode when in shared FIFO operation	Host and Device	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	TXFIFO 2 flush in device mode when in dedicated FIFO mode ... 5'hF: Periodic TxFIFO 15 flush in Device mode when in shared FIFO operation TXFIFO 15 flush in device mode when in dedicated FIFO mode 5'h10: Flush all the transmit FIFOs in device or host mode.		
5	TxFIFO Flush (TxFFlsh) This bit selectively flushes a single or all transmit FIFOs, but cannot do so if the core is in the midst of a transaction. The application must write this bit only after checking that the core is neither writing to the TxFIFO nor reading from the TxFIFO. Verify using these registers: Read—NAK Effective Interrupt ensures the core is not reading from the FIFO. Write—GRSTCTL.AHBIdle ensures the core is not writing anything to the FIFO. Flushing is normally recommended when FIFOs are re-configured or when switching between Shared FIFO and Dedicated Transmit FIFO operation. FIFO flushing is also recommended during device endpoint disable. The application must wait until the core clears this bit before performing any operations. This bit takes eight clocks to clear, using the slower clock of phy_clk or hclk.	Host and Device	RW[1]
4	RxFIFO Flush (RxFFlsh) The application can flush the entire RxFIFO using this bit, but must first ensure that the core is not in the middle of a transaction. The application must only write to this bit after checking that the core is neither reading from the RxFIFO nor writing to the RxFIFO. The application must wait until the bit is cleared before performing any other operations. This bit requires 8 clocks (slowest of PHY or AHB clock) to clear.	Host and Device	RW[2]
3	IN Token Sequence Learning Queue Flush (INTknQFlsh) This bit is valid only if OTG_EN_DED_TX_FIFO = 0. The application writes this bit to flush the IN Token Sequence Learning Queue.	Device Only	RW[3]
2	Host Frame Counter Reset (FrmCntrRst) The application writes this bit to reset the (micro)frame number counter inside the core. When the (micro)frame counter is reset,	Host Only	RW[4]

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	the subsequent SOF sent out by the core has a (micro)frame number of 0.		
1	Reserved	Host and Device	R
0	Core Soft Reset (CSftRst) Resets the hclk and phy_clock domains as follows: Clears the interrupts and all the CSR registers except the following register bits: PCGCCTL.RstPdwnModule PCGCCTL.GateHclk PCGCCTL.PwrClmp GUSBCFG.DDRSel GUSBCFG.PHYSel GUSBCFG.FSIntf GUSBCFG.ULPI_UTMI_Sel GUSBCFG.PHYIf HCFG.FSLSPclkSel DCFG.DevSpd DCTL.SftDiscon GGPIO GUSBCFG.TxEndDelay GUSBCFG.TermSelDLPulse GUSBCFG.ULPIClkSusM GUSBCFG.ULPIAutoRes GUSBCFG.ULPIFsLs GPWRDN GADPCTL All module state machines (except the AHB Slave Unit) are reset to the IDLE state, and all the transmit FIFOs and the receive FIFO are flushed. Any transactions on the AHB Master are terminated as soon as possible, after gracefully completing the last data phase of an AHB transfer. Any transactions on the USB are terminated immediately. When Hibernation or ADP feature is enabled, the PMU module is not reset by the Core Soft Reset. The application can write to this bit any time it wants to reset the core. This is a self-clearing bit and the core clears this bit after all the necessary logic is reset in the core, which can take several clocks, depending on the current state of the core. Once this bit is cleared software must wait at least 3 PHY clocks before doing any access to the PHY domain (synchronization delay). Software must also must check that bit 31 of this register is 1 (AHB Master is IDLE) before starting any operation.	Host and Device	RW[5]

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Typically software reset is used during software development and also when you dynamically change the PHY selection bits in the USB configuration registers listed above. When you change the PHY, the corresponding clock for the PHY is selected and used in the PHY domain. Once a new clock is selected, the PHY domain has to be reset for proper operation.		

***Notes*:**

[1]~[5]: This bits will operate with Write set , self clear function.

27.6.2.6 Interrupt Register (GINTSTS,0x014)

	GINTSTS																															Base + 0x014
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WkUpInt	SessReqInt	DisconnInt	ConIDStsChng	LPM_Int	PTxFEmp	HChInt	PrtInt	ResetDet	FetSusp	incompIP	incomplSOIN	OEPInt	IEPInt	EPMis	RstrDoneInt	EOPF	ISOOutDrop	EnumDone	USBRst	USBSusp	ErlySusp	I2CINT	ULPICKINT	GOUTNakEff	GINNakEff	NPTxFEmp	RxFLvl	Sof	OTGInt	ModeMis	CurMod
RST	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Description	Mode	R/W
31	Resume/Remote Wakeup Detected Interrupt (WkUpInt) Wakeup Interrupt during Suspend(L2) or LPM(L1) state. During Suspend(L2): Device Mode - This interrupt is asserted only when Host Initiated Resume is detected on USB. Host Mode - This interrupt is asserted only when Device Initiated Remote Wakeup is detected on USB. During LPM(L1): Device Mode - This interrupt is asserted for either Host Initiated Resume or Device Initiated Remote Wakeup on USB. Host Mode - This interrupt is asserted for either Host Initiated Resume or Device Initiated Remote Wakeup on USB.	Host and Device	RW[1]
30	Session Request/New Session Detected Interrupt (SessReqInt) In Host mode, this interrupt is asserted when a session request is detected from the device. In Host mode, this interrupt is asserted when a session request is detected from the device. In Device mode, this interrupt is asserted when the utmisrp_bvalid signal goes high. For more information on how to use this interrupt, see "FIFO RAM Allocation" in the Programming Guide.	Host and Device	RW[2]

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

29	Disconnect Detected Interrupt (DisconnInt) This interrupt is asserted when a device disconnect is detected.	Host Only	RW[3]
28	Connector ID Status Change (ConIDStsChng) This interrupt is asserted when there is a change in connector ID status.	Host and Device	RW[4]
27	LPM Transaction Received Interrupt (LPM_Int) Device Mode - This interrupt is asserted when the device receives an LPM transaction and responds with a non-ERRORed response. Host Mode - This interrupt is asserted when the device responds to an LPM transaction with a non-ERRORed response or when the host core has completed LPM transactions for the programmed number of times (GLPMCFG.RetryCnt). This Bits is valid only if the Core LPM Configuration register's LPM- Capable (LPMCap) Bits is set to 1 and the User HW Config3 register's OTG_ENABLE_LPM bit is set to 1.	Host and Device	RW[5]
26	Periodic TxFIFO Empty (PTxFEmp) This interrupt is asserted when the Periodic Transmit FIFO is either half or completely empty and there is space for at least one entry to be written in the Periodic Request Queue. The half or completely empty status is determined by the Periodic TxFIFO Empty Level bit in the Core AHB Configuration register (GAHBCFG.PTxFEmpLvl).	Host Only	R
25	Host Channels Interrupt (HChInt) The core sets this bit to indicate that an interrupt is pending on one of the channels of the core (in Host mode). The application must read the Host All Channels Interrupt (HAINT) register to determine the exact number of the channel on which the interrupt occurred, and then read the corresponding Host Channel-n Interrupt (HCINTn) register to determine the exact cause of the interrupt. The application must clear the appropriate status bit in the HCINTn register to clear this bit.	Host Only	R
24	Host Port Interrupt (PrtInt) The core sets this bit to indicate a change in port status of one of the DWC_otg core ports in Host mode. The application must read the Host Port Control and Status (HPRT) register to determine the exact event that caused this interrupt. The application must clear the appropriate status bit in the Host Port Control and Status register to clear this bit.	Host Only	R
23	Reset Detected Interrupt (ResetDet) The core sets this status bit in device mode when reset is detected on the USB in L2 Suspend state.	Device Only	RW[6]

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	This bit is valid only when the core is Device Mode and is operating in Partial Power-Down, or Clock Gating modes of Suspend. This bit is not valid when device is in Hibernation mode of Suspend.		
22	Data Fetch Suspended (FetSusp) This interrupt is valid only in DMA mode. This interrupt indicates that the core has stopped fetching data for IN endpoints due to the unavailability of TxFIFO space or Request Queue space. This interrupt is used by the application for an endpoint mismatch algorithm. For example, after detecting an endpoint mismatch, the application: Sets a global non-periodic IN NAK handshake Disables In endpoints Flushes the FIFO Determines the token sequence from the IN Token Sequence Learning Queue Re-enables the endpoints Clears the global non-periodic IN NAK handshake If the global non-periodic IN NAK is cleared, the core has not yet fetched data for the IN endpoint, and the IN token is received: the core generates an "IN token received when FIFO empty" interrupt. The OTG then sends the host a NAK response. To avoid this scenario, the application can check the GINTSTS.FetSusp interrupt, which ensures that the FIFO is full before clearing a global NAK handshake. Alternatively, the application can mask the "IN token received when FIFO empty" interrupt when clearing a global IN NAK handshake.	Device Only	RW[7]
21	Incomplete Periodic Transfer (incomplP) In Host mode, the core sets this interrupt bit when there are incomplete periodic transactions still pending which are scheduled for the current microframe. Incomplete Isochronous OUT Transfer (incompISOOUT) The Device mode, the core sets this interrupt to indicate that there is at least one isochronous OUT endpoint on which the transfer is not completed in the current microframe. This interrupt is asserted along with the End of Periodic Frame Interrupt (EOPF) bit in this register.	Host only Device only	RW[8]

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

20	Incomplete Isochronous IN Transfer (incompISOIN) The core sets this interrupt to indicate that there is at least one isochronousIN endpoint on which the transfer is not completed in the current microframe. This interrupt is asserted along with the End of Periodic Frame Interrupt (EOPF) bit in this register. Note: This interrupt is not asserted in Scatter/Gather DMA mode.	Device only	RW[9]
19	OUT Endpoints Interrupt (OEPInt) The core sets this bit to indicate that an interrupt is pending on one of the OUT endpoints of the core (in Device mode). The application must read the Device All Endpoints Interrupt (DAINT) register to determine the exact number of the OUT endpoint on which the interrupt occurred, and then read the corresponding Device OUT Endpoint-*n* Interrupt (DOEPINTn) register to determine the exact cause of the interrupt. The application must clear the appropriate status bit in the corresponding DOEPINTn register to clear this bit.	Device only	R
18	IN Endpoints Interrupt (IEPInt) The core sets this bit to indicate that an interrupt is pending on one of the IN endpoints of the core (in Device mode). The application must read the Device All Endpoints Interrupt (DAINT) register to determine the exact number of the IN endpoint on which the interrupt occurred, and then read the corresponding Device IN Endpoint-*n* Interrupt (DIEPINTn) register to determine the exact cause of the interrupt. The application must clear the appropriate status bit in the corresponding DIEPINTn register to clear this bit.	Device only	R
17	Endpoint Mismatch Interrupt (EPMis) Note: This interrupt is valid only in shared FIFO operation. ndicates that an IN token has been received for a non-periodic endpoint, but the data for another endpoint is present in the top of the Non-periodic Transmit FIFO and the IN endpoint mismatch count programmed by the application has expired.	Device only	RW[10]
16	Restore Done Interrupt (RstrDoneInt) The core sets this bit to indicate that the restore command after Hibernation was completed by the core. The core continues from Suspended state into the mode dictated by PCGCCTL.RestoreMode bits. This bit is valid only when Hibernation feature is enabled (OTG_EN_PWROPT=2)	Host and Device mode	RW[11]
15	End of Periodic Frame Interrupt (EOPF) Indicates that the period specified in the Periodic Frame Interval	Device only	RW[12]

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	bits of the Device Configuration register (DCFG.PerFrInt) has been reached in the current microframe.		
14	Isochronous OUT Packet Dropped Interrupt (ISOOutDrop) The core sets this bit when it fails to write an isochronous OUT packet into the RxFIFO because the RxFIFO does not have enough space to accommodate a maximum packet size packet for the isochronous OUT endpoint.	Device only	RW[13]
13	Enumeration Done (EnumDone) The core sets this bit to indicate that speed enumeration is complete. The application must read the Device Status (DSTS) register to obtain the enumerated speed.	Device only	RW[14]
12	USB Reset (USBRst) The core sets this bit to indicate that a reset is detected on the USB.	Device only	RW[15]
11	USB Suspend (USBSusp) The core sets this bit to indicate that a suspend was detected on the USB. The core enters the Suspended state when there is no activity on the utmi_linestate signal for an extended period of time.	Device only	RW[16]
10	Early Suspend (ErlySusp) The core sets this bit to indicate that an Idle state has been detected on the USB for 3 ms.	Device only	RW[17]
9	I^2C Interrupt (I2CINT) The core sets this interrupt when I^2C access is completed on the I^2C interface. This Bits is used only if the I^2C interface was enabled. Otherwise, reads return 0.	Host and Device	RW[18]
8	ULPI Carkit Interrupt (ULPICKINT) This Bits is used only if the Carkit interface was enabled. Otherwise, reads return 0.	Host and Device	RW[19]
7	Global OUT NAK Effective (GOUTNakEff) Indicates that the Set Global OUT NAK bit in the Device Control register (DCTL.SGOUTNak), set by the application, has taken effect in the core. This bit can be cleared by writing the Clear Global OUT NAK bit in the Device Control register (DCTL.CGOUTNak).	Device only	R
6	Global IN Non-Periodic NAK Effective (GINNakEff) Indicates that the Set Global Non-periodic IN NAK bit in the Device Control register (DCTL.SGNPInNak), set by the application, has taken effect in the core. That is, the core has sampled the Global IN NAK bit set by the application. This bit can be cleared by clearing the Clear Global Non- periodic IN NAK bit in the Device Control register (DCTL.CGNPInNak).	Device only	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	This interrupt does not necessarily mean that a NAK handshake is sent out on the USB. The STALL bit takes precedence over the NAK bit.		
5	Non-Periodic TxFIFO Empty (NPTxFEmp) This interrupt is valid only when OTG_EN_DED_TX_FIFO = 0. This interrupt is asserted when the Non-periodic TxFIFO is either half or completely empty, and there is space for at least one entry to be written to the Non-periodic Transmit Request Queue. The half or completely empty status is determined by the Non-periodic TxFIFO Empty Level bit in the Core AHB Configuration register (GAHBCFG.NPTxFEmpLvl).	Host and Device	R
4	RxFIFO Non-Empty (RxFLvl) Indicates that there is at least one packet pending to be read from the RxFIFO.	Host and Device	R
3	Start of (micro)Frame (Sof) In Host mode, the core sets this bit to indicate that an SOF (FS), micro-SOF (HS), or Keep-Alive (LS) is transmitted on the USB. The application must write a 1 to this bit to clear the interrupt. In Device mode, in the core sets this bit to indicate that an SOF token has been received on the USB. The application can read the Device Status register to get the current (micro)frame number. This interrupt is seen only when the core is operating at either HS or FS. Note: This register may return 1'b1 if read immediately after power on reset. If the register bit reads 1'b1 immediately after power on reset it does not indicate that an SOF has been sent (in case of host mode) or SOF has been received (in case of device mode). The read value of this interrupt is valid only after a valid connection between host and device is established. If the bit is set after power on reset the application can clear the bit.	Host and Device	RW[20]
2	OTG Interrupt (OTGInt) The core sets this bit to indicate an OTG protocol event. The application must read the OTG Interrupt Status (GOTGINT) register to determine the exact event that caused this interrupt. The application must clear the appropriate status bit in the GOTGINT register to clear this bit.	Host and Device	R
1	Mode Mismatch Interrupt (ModeMis) The core sets this bit when the application is trying to access: A Host mode register, when the core is operating in Device mode A Device mode register, when the core is operating in Host mode The register access is completed on the AHB with an OKAY response, but is ignored by the core internally and does not	Host and Device	RW[21]

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	affect the operation of the core.		
0	Current Mode of Operation (CurMod) Indicates the current mode. 1'b0: Device mode 1'b1: Host mode	Host and Device	R

Note:

[1]~[21]: **This bits will operate with Write set , self clear function.**

27.6.2.7 Interrupt Mask Register (GINTMSK,0x018)

	GINTMSK																															Base + 0x018
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WkUpInt	SessReqInt	DisconnInt	ConIDStsChng	LPM_Int	PTxFEmp	HChInt	PrtInt	ResetDet	FetSusp	incomplP	incomplSOIN	OEPInt	IEPInt	EPMis	RstrDoneInt	EOPF	ISOOutDrop	EnumDone	USBRst	USBSusp	ErlySusp	I2CINT	ULPICKINT	GOUTNakEff	GINNakEff	NPTxFEmp	RxFLvl	Sof	OTGInt	ModeMis	CurMod
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	Mode	R/W
31	Resume/Remote Wakeup Detected Interrupt Mask (WkUpIntMsk)	Host and Device	RW
30	Session Request/New Session Detected Interrupt Mask (SessReqIntMsk)	Host and Device	RW
29	Disconnect Detected Interrupt Mask (DisconnIntMsk)	Host Only	RW
28	Connector ID Status Change Mask (ConIDStsChngMsk)	Host and Device	RW
27	LPM Transaction Received Interrupt Mask (LPM_IntMsk)	Host and Device	RW
26	Periodic TxFIFO Empty Mask (PTxFEmpMsk)	Host Only	RW
25	Host Channels Interrupt Mask (HChIntMsk)	Host Only	RW
24	Host Port Interrupt Mask (PrtIntMsk)	Host Only	RW
23	Reset Detected Interrupt Mask (ResetDetMsk)	Device Only	RW
22	Data Fetch Suspended Mask (FetSuspMsk)	Device Only	RW
21	Incomplete Periodic Transfer Mask (incomplPMsk) Incomplete Isochronous OUT Transfer Mask (incompISOOUTMsk)	Host only Device only	RW
20	Incomplete Isochronous IN Transfer Mask (incompISOINMsk) This bit is enabled only when device periodic endpoints are enabled in Dedicated TxFIFO mode.	Device only	RW
19	OUT Endpoints Interrupt Mask (OEPIntMsk)	Device only	RW
18	IN Endpoints Interrupt Mask (IEPIntMsk)	Device only	RW
17	Endpoint Mismatch Interrupt Mask (EPMisMsk)	Device only	RW
16	Restore Done Interrupt Mask (RstrDoneIntMsk)	Host and Device	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	This Bits is valid only when Hibernation feature is enabled (OTG_EN_PWROPT=2).	mode	
15	End of Periodic Frame Interrupt Mask (EOPFMsk)	Device only	RW
14	Isochronous OUT Packet Dropped Interrupt Mask (ISOOutDropMsk)	Device only	RW
13	Enumeration Done Mask (EnumDoneMsk)	Device only	RW
12	USB Reset Mask (USBRstMsk)	Device only	RW
11	USB Suspend Mask (USBSuspMsk)	Device only	RW
10	Early Suspend Mask (ErlySuspMsk)	Device only	RW
9	I^2C Interrupt Mask (I2CIntMsk)	Host and Device	RW
8	ULPI Carkit Interrupt Mask (ULPICKINTMsk) I^2C Carkit Interrupt Mask (I2CCKINTMsk)	Host and Device	RW
7	Global OUT NAK Effective Mask (GOUTNakEffMsk)	Device only	RW
6	Global Non-periodic IN NAK Effective Mask (GINNakEffMsk)	Device only	RW
5	Non-periodic TxFIFO Empty Mask (NPTxFEmpMsk)	Host and Device	RW
4	Receive FIFO Non-Empty Mask (RxFLvlMsk)	Host and Device	RW
3	Start of (micro)Frame Mask (SofMsk)	Host and Device	RW
2	OTG Interrupt Mask (OTGIntMsk)	Host and Device	RW
1	Mode Mismatch Interrupt Mask (ModeMisMsk)	Host and Device	RW
0	Reserved	Host and Device	R

27.6.2.8 Receive Status Debug Read/Status Read and Pop Registers (GRXSTSR/GRXSTSP)

when host mode:

	GRXSTSR/GRXSTSP																															Base + 0x01C/Base + 0x020
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved											PktSts				DPID	BCnt												ChNum			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:21	Reserved	R
20:17	Packet Status (PktSts) 4'b0010: IN data packet received 4'b0011: IN transfer completed (triggers an interrupt) 4'b0101: Data toggle error (triggers an interrupt) 4'b0111: Channel halted (triggers an interrupt)	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Others: Reserved	
16:15	Data PID (DPID) Indicates the Data PID of the received packet	R
14:4	Byte Count (BCnt) Indicates the byte count of the received IN data packet.	R
3:0	Channel Number (ChNum) Indicates the channel number to which the current received packet belongs.	R

when device mode:

	GRXSTSR/GRXSTSP																															
																		Base + 0x01C/Base + 0x020														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved							FN				PktSts				DPID	BCnt												EPNum			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:25	Reserved	R
24:21	Frame Number (FN) This is the least significant 4 bits of the (micro)frame number in which the packet is received on the USB. This Bits is supported only when isochronous OUT endpoints are supported.	R
20:17	Packet Status (PktSts) Indicates the status of the received packet 4'b0001: Global OUT NAK (triggers an interrupt) 4'b0010: OUT data packet received 4'b0011: OUT transfer completed (triggers an interrupt) 4'b0100: SETUP transaction completed (triggers an interrupt) 4'b0110: SETUP data packet received Others: Reserved	R
16:15	Data PID (DPID) Indicates the Data PID of the received OUT data packet 2'b00: DATA0 2'b10: DATA1 2'b01: DATA2 2'b11: MDATA	R
14:4	Byte Count (BCnt) Indicates the byte count of the received data packet.	R
3:0	Endpoint Number (EPNum) Indicates the endpoint number to which the current received packet belongs.	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

27.6.2.9 Receive FIFO Size Register (GRXFSIZ,0x024)

	GRXFSIZ																															Base + 0x024
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																RxFDep															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Description	R/W
31:16	Reserved	R
15:0	RxFIFO Depth (RxFDep) This value is in terms of 32-bit words. Minimum value is 16 Maximum value is 3648.	RW

27.6.2.10 Non-Periodic Transmit FIFO Size Register (GNPTXFSIZ,0x028)

	GNPTXFSIZ																															Base + 0x028
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	NPTxFDep																NPTxFStAddr															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Description	R/W
31:16	Non-periodic TxFIFO Depth (NPTxFDep) For host mode, this Bits is always valid. For Device mode, this Bits is invalid. This value is in terms of 32-bit words. Minimum value is 16 Maximum value is 3648	R/RW
15:0	Non-periodic Transmit RAM Start Address (NPTxFStAddr) For host mode, this Bits is always valid. This Bits contains the memory start address for Non-periodic Transmit FIFO RAM. The application can write a new value in this Bits. Programmed values must not exceed the power-on value set	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

27.6.2.11 Non-Periodic Transmit FIFO/Queue Status Register (GNPTXSTS,0x02C)

	GNPTXSTS																															Base + 0x02C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	NPTxQTop								NPTxQSpcAvail								NPTxFSpcAvail															
RST	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Description	R/W
31:24	Top of the Non-periodic Transmit Request Queue (NPTxQTop) Entry in the Non-periodic Tx Request Queue that is currently being processed by the MAC. Bits [30:27]: Channel/endpoint number Bits [26:25]: 2'b00: IN/OUT token 2'b01: Zero-length transmit packet (device IN/host OUT) 2'b10: PING/CSPLIT token 2'b11: Channel halt command Bit [24]: Terminate (last entry for selected channel/endpoint)	R
23:16	Non-periodic Transmit Request Queue Space Available (NPTxQSpcAvail) Indicates the amount of free space available in the Non-periodic Transmit Request Queue. This queue holds both IN and OUT requests in Host mode. Device mode has only IN requests. 8'h0: Non-periodic Transmit Request Queue is full 8'h1: 1 location available 8'h2: 2 locations available n : n locations available (0⩽n⩽8) Others: Reserved	R
15:0	Non-periodic TxFIFO Space Avail (NPTxFSpcAvail) Indicates the amount of free space available in the Non-periodic TxFIFO. Values are in terms of 32-bit words. 16'h0: Non-periodic TxFIFO is full 16'h1: 1 word available 16'h2: 2 words available 16'h*n*: *n* words available (where 0⩽n⩽32,768) 16'h8000: 32,768 words available Others: Reserved	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

27.6.2.12 User HW Config1 Register (GHWCFG1,0x044)

	GHWCFG1																															Base + 0x044
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	epdir																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Description	R/W
31:0	Endpoint Direction (epdir) This 32-bit Bits uses two bits per endpoint to determine the endpoint direction. Endpoint Bits [31:30]: Endpoint 15 direction Bits [29:28]: Endpoint 14 direction ... Bits [3:2]: Endpoint 1 direction Bits[1:0]: Endpoint 0 direction (always BIDIR) Direction 2'b00: BIDIR (IN and OUT) endpoint 2'b01: IN endpoint 2'b10: OUT endpoint 2'b11: Reserved This Bits is configured using "Name: OTG_EP_DIR_1(n)".	R

27.6.2.13 User HW Config2 Register (GHWCFG2,0x048)

	GHWCFG2																															Base + 0x048
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	otgenicusb	TknQDepth					PTxQDepth		NPTxQDepth		Reserved	MultiProcIntrpt	DynFifoSizing	PerioSupport	NumHstChnl				NumDevEps				FSPhyType		HSPhyType		SingPnt	OtgArch		OtgMode		
RST	?	?	?	?	?	?	?	?	?	?	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Description	R/W
31	OTG_ENABLE_IC_USB(otgenicusb) IC_USB mode specified for mode of operation (parameter OTG_ENABLE _IC_USB) in coreConsultant. To choose IC_USB_MODE, both OTG_FSPHY_INTERFACE and OTG_ENABLE_IC_USB must be 1.	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

30:26	Device Mode IN Token Sequence Learning Queue Depth (TknQDepth) Range: 0-30 This Bits is configured using "Name: OTG_TOKEN_QUEUE_DEPTH".	R
25:24	Host Mode Periodic Request Queue Depth (PTxQDepth) 2'b00: 2 2'b01: 4 2'b10: 8 2'b11: 16 This Bits is configured using parameter "Name: OTG_PERIO_TX_QUEUE_DEPTH"	R
23:22	Non-periodic Request Queue Depth (NPTxQDepth) 2'b00: 2 2'b01: 4 2'b10: 8 Others: Reserved This Bits is configured using parameter "Name: OTG_NPERIO_TX_QUEUE_DEPTH".	R
21	Reserved	R
20	Multi Processor Interrupt Enabled (MultiProcIntrpt) 1'b0: No 1'b1: Yes This Bits is configured using parameter "Name: OTG_MULTI_PROC_INTRPT".	R
19	Dynamic FIFO Sizing Enabled (DynFifoSizing) 1'b0: No 1'b1: Yes This Bits is configured using parameter "Name: OTG_DFIFO_DYNAMIC".	R
18	Periodic OUT Channels Supported in Host Mode (PerioSupport) 1'b0: No 1'b1: Yes This Bits is configured using parameter "Name: OTG_EN_PERIO_HOST".	R
17:14	Number of Host Channels (NumHstChnl) Indicates the number of host channels supported by the core in Host mode. The range of this Bits is 0-15: 0 specifies 1 channel, 15 specifies 16 channels. This Bits is configured using parameter "Name: OTG_NUM_HOST_CHAN".	R
13:10	Number of Device Endpoints (NumDevEps) Indicates the number of device endpoints supported by the core in Device mode in addition to control endpoint 0. The range of this Bits is 1-15. This Bits is configured using parameter "Name: OTG_NUM_EPS".	R
9:8	Full-Speed PHY Interface Type (FSPhyType) 2'b00: Full-speed interface not supported 2'b01: Dedicated full-speed interface 2'b10: FS pins shared with UTMI+ pins 2'b11: FS pins shared with ULPI pins This Bits is configured using parameter "Name: OTG_FSPHY_INTERFACE".	R
7:6	High-Speed PHY Interface Type (HSPhyType)	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	2'b00: High-Speed interface not supported 2'b01: UTMI+ 2'b10: ULPI 2'b11: UTMI+and ULPI This Bits is configured using parameter "Name: OTG_HSPHY_INTERFACE".	
5	Point-to-Point (SingPnt) 1'b0: Multi-point application (hub and split support) 1'b1: Single-point application (no hub and no split support) This Bits is configured using parameter "Name: OTG_SINGLE_POINT".	R
4:3	Architecture (OtgArch) 2'b00: Slave-Only 2'b01: External DMA 2'b10: Internal DMA Others: Reserved This Bits is configured using parameter "Name: OTG_ARCHITECTURE".	R
2:0	Mode of Operation (OtgMode) 3'b000: HNP- and SRP-Capable OTG (Host and Device) 3'b001: SRP-Capable OTG (Host and Device) 3'b010: Non-HNP and Non-SRP Capable OTG (Host and Device) 3'b011: SRP-Capable Device 3'b100: Non-OTG Device 3'b101: SRP-Capable Host 3'b110: Non-OTG Host Others: Reserved This Bits is configured using parameter "Name: OTG_MODE".	R

27.6.2.14 User HW Config3 Register (GHWCFG3,0x04C)

																																	Base + 0x04C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DfifoDepth																OTG_ENABLE_LPM	OTG_BC_SUPPORT	OTG_ENABLE_HSIC	OTG_ADP_SUPPORT	RstType	OptFeature	VndctlSupt	I2CIntSel	OtgEn	PktSizeWidth			XferSizeWidth			
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Description	R/W
31:16	DFIFO Depth (DfifoDepth minus EP_LOC_CNT) This value is in terms of 32-bit words. Minimum value is 32	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Maximum value is 32,768 This Bits is configured using parameter "Name: OTG_DFIFO_DEPTH" and EP_LOC_CNT. For more information on EP_LOC_CNT, see "Endpoint Information Controller (EPINFO_CTL)".	
15	OTG_ENABLE_LPM LPM mode specified for Mode of Operation (parameter OTG_ENABLE_LPM) in coreConsultant configuration.	R
14	OTG_BC_SUPPORT This bit indicates the HS OTG controller support for Battery Charger. 0 - No Battery Charger Support 1 - Battery Charger support present.	R
13	OTG_ENABLE_HSIC HSIC mode specified for Mode of Operation in coreConsultant configuration (parameter OTG_ENABLE_HSIC). Value Range: 0-1 1: HSIC-capable with shared UTMI PHY interface 0: Non-HSIC-capable Parameter Name: OTG_ENABLE_HSIC Dependencies: OTG_HSPHY_INTERFACE Default: Non-HSIC-capable	R
12	OTG_ADP_SUPPORT This bit indicates whether ADP logic is present within or external to the HS OTG controller 0 - No ADP logic present with HS OTG controller 1- ADP logic is present along with HS OTG controller.	R
11	Reset Style for Clocked always Blocks in RTL (RstType) 1'b0: Asynchronous reset is used in the core 1'b1: Synchronous reset is used in the core This Bits is configured using parameter "Name: OTG_SYNC_RESET_TYPE".	R
10	Optional Features Removed (OptFeature) Indicates whether the User ID register, GPIO interface ports, and SOF toggle and counter ports were removed for gate count optimization by enabling Remove Optional Features? during coreConsultant configuration. 1'b0: No 1'b1: Yes This Bits is configured using parameter "Name: OTG_RM_OPT_FEATURES".	R
9	Vendor Control Interface Support (VndctlSupt) 1'b0: Vendor Control Interface is not available on the core. 1'b1: Vendor Control Interface is available. This Bits is configured using parameter "Name: OTG_VENDOR_CTL_INTERFACE".	R
8	I^2C Selection (I2CIntSel) 1'b0: I 2C Interface is not available on the core.	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	1'b1: I 2C Interface is available on the core. This Bits is configured using parameter "Name: OTG_I2C_INTERFACE".	
7	OTG Function Enabled (OtgEn) The application uses this bit to indicate the DWC_otg core's OTG capabilities. 1'b0: Not OTG capable 1'b1: OTG Capable This Bits is configured using parameter "Name: OTG_MODE".	R
6:4	Width of Packet Size Counters (PktSizeWidth) 3'b000: 4 bits 3'b001: 5 bits 3'b010: 6 bits 3'b011: 7 bits 3'b100: 8 bits 3'b101: 9 bits 3'b110: 10 bits Others: Reserved This Bits is configured using parameter "Name: OTG_PACKET_COUNT_WIDTH".	R
3:0	Width of Transfer Size Counters (XferSizeWidth) 4'b0000: 11 bits 4'b0001: 12 bits ... 4'b1000: 19 bits Others: Reserved This Bits is configured using parameter "Name: OTG_TRANS_COUNT_WIDTH".	R

27.6.2.15 User HW Config4 Register (GHWCFG4,0x050)

	GHWCFG4																															Base + 0x050
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SGDMA	SGDMACFG	INEps				DedFifoMode	SessEndFltr	BValidFltr	AValidFltr	VBusValidFltr	IddgFltr	NumCtlEps				PhyDataWidth		Reserved								AhbFreq	enPartPwrDn	NumDevPerioEps			
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	0	?	?	?	?	?	?

Bits	Description	R/W
31	Scatter/Gather DMA(SGDMA) 1'b1: Dynamic configuration This Bits is configured using parameter "Name: OTG_EN_DESC_DMA" .	R
30	Scatter/Gather DMA configuration(SGDMACFG) 1'b0: Non-Scatter/Gather DMA configuration	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	1'b1: Scatter/Gather DMA configuration This Bits is configured using parameter "Name: OTG_EN_DESC_DMA".	
29:26	Number of Device Mode IN Endpoints Including Control Endpoints (INEps) Range 0 -15 0:1 IN Endpoint 1:2 IN Endpoints .... 15:16 IN Endpoints This Bits is configured using parameter "Name: OTG_NUM_IN_EPS".	R
25	Enable Dedicated Transmit FIFO for device IN Endpoints (DedFifoMode) 1'b0: Dedicated Transmit FIFO Operation not enabled. 1'b1: Dedicated Transmit FIFO Operation enabled. This Bits is configured using parameter "Name: OTG_EN_DED_TX_FIFO".	R
24	session_end Filter Enabled (SessEndFltr) 1'b0: No filter 1'b1: Filter This Bits is configured using parameter "Name: OTG_EN_SESSIONEND_FILTER"	R
23	"b_valid" Filter Enabled (BValidFltr) 1'b0: No filter 1'b1: Filter This Bits is configured using parameter "Name: OTG_EN_B_VALID_FILTER".	R
22	"a_valid" Filter Enabled (AValidFltr) 1'b0: No filter 1'b1: Filter This Bits is configured using parameter "Name: OTG_EN_A_VALID_FILTER".	R
21	"vbus_valid" Filter Enabled (VBusValidFltr) 1'b0: No filter 1'b1: Filter This Bits is configured using parameter "Name: OTG_EN_VBUSVALID_FILTER".	R
20	"iddig" Filter Enable (IddgFltr) 1'b0: No filter 1'b1: Filter This Bits is configured using parameter "Name: OTG_EN_IDDIG_FILTER".	R
19:16	Number of Device Mode Control Endpoints in Addition to Endpoint 0 (NumCtlEps) Range: 0-15 This Bits is configured using parameter "Name: OTG_NUM_CRL_EPS".	R
15:14	UTMI+ PHY/ULPI-to-Internal UTMI+ Wrapper Data Width (PhyDataWidth) When a ULPI PHY is used, an internal wrapper converts ULPI to UTMI+. 2'b00: 8 bits 2'b01: 16 bits 2'b10: 8/16 bits, software selectable Others: Reserved	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	This Bits is configured using parameter "Name: OTG_HSPHY_DWIDTH".	
13:6	Reserved	R
6	Enable Hibernation 1'b0: Hibernation feature not enabled 1'b1: Hibernation feature enabled This Bits is configured using parameter "Name: OTG_EN_PWROPT".	R
5	Minimum AHB Frequency Less Than 60 MHz (AhbFreq) 1'b0: No 1'b1: Yes This Bits is configured using parameter "Name: OTG_MIN_AHB_FREQ_LESSTHAN_60".	R
4	Enable Partial Power Down(enPartPwrDn) 1'b0: Partial Power Down Not Enabled 1'b1: Partial Power Down Enabled This Bits is configured using parameter "Name: OTG_EN_PWROPT".	R
3:0	Number of Device Mode Periodic IN Endpoints (NumDevPerioEps) Range: 0-15 This Bits is configured using parameter "Name: OTG_NUM_PERIO_EPS".	R

27.6.2.16 DFIFO Software Config Register (GDFIFOCFG,0x05C)

	GDFIFOCFG																															Base + 0x05C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EPInfoBaseAddr																GDFIFOCfg															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Description	Mode	R/W
31:16	EPInfoBaseAddr This Bits provides the start address of the EP info controller.	Host and Device	RW
15:0	GDFIFOCfg This Bits is for dynamic programming of the DFIFO Size. This value takes effect only when the application programs a non zero value to this register. The value programmed must conform to the guidelines described in "FIFO RAM Allocation" in the Programming Guide. The DWC_otg core does not have any corrective logic if the FIFO sizes are programmed incorrectly.	Host and Device	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

27.6.2.17 Host Periodic Transmit FIFO Size Register (HPTXFSIZ,0x100)

	HPTXFSIZ																															Base + 0x100
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PTxFSize																PTxFStAddr															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Description	R/W
31:16	**Host Periodic TxFIFO Depth (PTxFSize)** **This value is in terms of 32-bit words.** **Minimum value is 16** **Maximum value is 3648**	**RW**
15:0	**Host Periodic TxFIFO Start Address (PTxFStAddr)** **The power-on reset value of this register is the sum of the Largest Rx Data FIFO Depth and Largest Non-periodic Tx Data FIFO Depth specified .These parameters are:** **In shared FIFO operation:-** **OTG_RX_DFIFO_DEPTH(3648) + OTG_TX_NPERIO_DFIFO_DEPTH(1024)** **In dedicated FIFO mode:-** **OTG_RX_DFIFO_DEPTH(3648) + OTG_TX_HNPERIO_DFIFO_DEPTH(3648)**	**R/RW**

27.6.2.18 Device IN Endpoint Transmit FIFO Size Register: (DIEPTXFn,0x104+(FIFO_num - 1)*0x04)

	DIEPTXFn																															Base + 0x104+(FIFO_num - 1)*0x4
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	INEPnTxFDep																INEPnTxFStAddr															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Description	R/W
31:16	IN Endpoint TxFIFO Depth (INEPnTxFDep) This value is in terms of 32-bit words. Minimum value is 16 Maximum value is 3648	RW
15:0	IN Endpoint FIFO*n* Transmit RAM Start Address (INEPnTxFStAddr) This Bits contains the memory start address for IN endpoint Transmit FIFOn (0 < n	R/RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	<= 15). The power-on reset value of this register is calculated according to the following formula: OTG_RX_DFIFO_DEPTH + SUM of OTG_TX_DINEP_DFIFO_DEPTH_'x' (where x = 0 to n - 1) If at POR the calculated value (C) exceeds 65535, then the Reset value becomes Reset Value(A) = (C - 65536). Example: If start address of IN endpoint FIFO 1 is OTG_RX_DFIFO_DEPTH + OTG_TX_DINEP_DFIFO_DEPTH_ 0 and start address of IN endpoint FIFO 2 is OTG_RX_DFIFO_DEPTH + OTG_TX_DINEP_DFIFO_DEPTH_ 0 + OTG_TX_DINEP_DFIFO_DEPTH_ 1.	

27.6.2.19 Host Configuration Register (HCFG,0x400)

	HCFG																															Base + 0x400
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ModeChTimEn	Reserved				PerSchedEna	FrListEn		DescDMA	Reserved							ResValid								Ena32KHzS	Reserved				FSLSSupp	FSLSPclkSel	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31	Mode Change Ready Timer Enable (ModeChTimEn) This bit is used to enable or disable the host core to wait for 200 PHY clock cycles at the end of Resume to change the opmode signal to the PHY to 00 after Suspend or LPM. 1'b0: The Host core waits for either 200 PHY clock cycles or a linestate of SE0 at the end of resume to change the opmode from 2'b10 to 2'b00. 1'b1: The Host core waits only for a linestate of SE0 at the end of resume to change the opmode from 2'b10 to 2'b00.	RW
30:27	Reserved	R
26	Enable Periodic Scheduling (PerSchedEna) Applicable in Scatter/Gather DMA mode only. Enables periodic scheduling within the core. Initially, the bit is reset. The core will not process any periodic channels. As soon as this bit is set, the core will get ready to start scheduling periodic channels. In non Scatter/Gather DMA mode, this bit is reserved.	RW
25:24	Frame List Entries (FrListEn). The value in the register specifies the number of entries in the Frame list. This Bits is valid only in Scatter/Gather DMA mode. 2'b00: 8 Entries 2'b01:16 Entries	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	2'b10: 32 Entries 2'b11: 64 Entries In modes other than Scatter/Gather DMA mode, these bits are reserved.	
23	Enable Scatter/gather DMA in Host mode (DescDMA) When the Scatter/Gather DMA option selected during configuration of the RTL, the application can set this bit during initialization to enable the Scatter/Gather DMA operation. NOTE: This bit must be modified only once after a reset. The following combinations are available for programming: GAHBCFG.DMAEn=0, HCFG.DescDMA=0 => Slave mode GAHBCFG.DMAEn=0, HCFG.DescDMA=1 => Invalid GAHBCFG.DMAEn=1, HCFG.DescDMA=0 => Buffered DMA mode GAHBCFG.DMAEn=1, HCFG.DescDMA=1 => Scatter/Gather DMA mode In non Scatter/Gather DMA mode, this bit is reserved.	RW
22:16	Reserved	RW
15:8	Resume Validation Period (ResValid) This Bits is effective only when HCFG.Ena32KHzS is set. It controls the resume period when the core resumes from suspend. The core counts the ResValid number of clock cycles to detect a valid resume when this is set.	RW
7	Enable 32-KHz Suspend Mode (Ena32KHzS) This bit can only be set if the USB 1.1 Full-Speed Serial Transceiver Interface has been selected. If USB 1.1 Full-Speed Serial Transceiver Interface has not been selected, this bit must be zero. When the USB 1.1 Full-Speed Serial Transceiver Interface is chosen and this bit is set, the core expects the 48-MHz PHY clock to be switched to 32 KHz during a suspend.	RW
6:3	Reserved	R
2	FS- and LS-Only Support (FSLSSupp) The application uses this bit to control the core's enumeration speed. Using this bit, the application can make the core enumerate as a FS host, even if the connected device supports HS traffic. Do not make changes to this Bits after initial programming. 1'b0: HS/FS/LS, based on the maximum speed supported by the connected device 1'b1: FS/LS-only, even if the connected device can support HS	RW
1:0	FS/LS PHY Clock Select (FSLSPclkSel) When the core is in FS Host mode 2'b00: Internal PHY clock is running at 30/60 MHZ (For UTMI+/ULPI PHY Interfaces) 2'b01: Internal PHY clock is running at 48MHZ (For 1.1 FS transceiver Interface) Others: Reserved When the core is in LS Host mode 2'b00: Internal PHY clock is running at 30/60 MHZ (For UTMI+/ULPI PHY Interfaces) 2'b10: Internal PHY clock is running at 6 MHZ and the external clock is running at 48MHZ. When you select a 6 MHz clock during LS Mode, you must do a soft reset	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	(for 1.1 FS transceiver Interface) Others: Reserved Notes: When Core in FS mode, the internal and external clocks have the same frequency. When Core in LS mode, If FSLSPclkSel = 2'b00: Internal and external clocks have the same frequency If FSLSPclkSel = 2'b10: Internal clock is divided by eight version of external 48 MHz clock (utmifs_clk).	

27.6.2.20 Host Frame Interval Register (HFIR,0x404)

	HFIR																															Base + 0x404
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved															HFIRRldCtrl	FrInt															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0	0	0

Bits	Description	R/W
31:17	Reserved	R
16	Reload Control (HFIRRldCtrl) This bit allows dynamic reloading of the HFIR register during runtime. 1'b0: The HFIR cannot be reloaded dynamically 1'b1: the HFIR can be dynamically reloaded during runtime. This bit needs to be programmed during initial configuration and its value must not be changed during runtime.	RW
15:0	Frame Interval (FrInt) The value that the application programs to this Bits specifies the interval between two consecutive SOFs (FS) or micro-SOFs (HS) or Keep-Alive tokens (LS). This Bits contains the number of PHY clocks that constitute the required frame interval. The default value set in this Bits for a FS operation when the PHY clock frequency is 60 MHz. The application can write a value to this register only after the Port Enable bit of the Host Port Control and Status register (HPRT.PrtEnaPort) has been set. If no value is programmed, the core calculates the value based on the PHY clock specified in the FS/LS PHY Clock Select Bits of the Host Configuration register (HCFG.FSLSPclkSel). 125 μs * (PHY clock frequency for HS) 1 ms * (PHY clock frequency for FS/LS)	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

27.6.2.21 Host Frame Number/Frame Time Remaining Register (HFNUM,0x408)

	HFNUM																															Base + 0x408
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FrRem																FrNum															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Description	R/W
31:16	Frame Time Remaining (FrRem) Indicates the amount of time remaining in the current microframe (HS) or frame (FS/LS), in terms of PHY clocks. This Bits decrements on each PHY clock. When it reaches zero, this Bits is reloaded with the value in the Frame Interval register and a new SOF is transmitted on the USB.	R
15:0	Frame Number (FrNum) This Bits increments when a new SOF is transmitted on the USB, and is reset to 0 when it reaches 16'h3FFF.	R

27.6.2.22 Host Periodic Transmit FIFO/Queue Status Register (HPTXSTS,0x410)

	HPTXSTS																															Base + 0x410
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PTxQTop								PTxQSpcAvail								PTxFSpcAvail															
RST	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Description	R/W
31:24	Top of the Periodic Transmit Request Queue (PTxQTop) This indicates the entry in the Periodic Tx Request Queue that is currently being processes by the MAC. This register is used for debugging. Bit [31]: Odd/Even (micro)frame 1'b0: send in even (micro)frame 1'b1: send in odd (micro)frame Bits [30:27]: Channel/endpoint number Bits [26:25]: Type	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	2'b00: IN/OUT 2'b01: Zero-length packet 2'b10: CSPLIT 2'b11: Disable channel command Bit [24]: Terminate (last entry for the selected channel/endpoint)	
23:16	Periodic Transmit Request Queue Space Available (PTxQSpcAvail) Indicates the number of free locations available to be written in the Periodic Transmit Request Queue. This queue holds both IN and OUT requests. 8'h0: Periodic Transmit Request Queue is full 8'h1: 1 location available 8'h2: 2 locations available n : n locations available (0 ≤n ≤16) Others: Reserved	R
15:0	Periodic Transmit Data FIFO Space Available (PTxFSpcAvail) Indicates the number of free locations available to be written to in the Periodic TxFIFO. Values are in terms of 32-bit words 16'h0: Periodic TxFIFO is full 16'h1: 1 word available 16'h2: 2 words available 16'hn: n words available (where 0 ≤n ≤32,768) 16'h8000: 32,768 words available Others: Reserved	R

27.6.2.23 Host All Channels Interrupt Register (HAINT,0x414)

	HAINT																															Base + 0x414
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																HAINT															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:16	Reserved	R
15:0	Channel Interrupts (HAINT) One bit per channel: Bit 0 for Channel 0, bit 15 for Channel 15	R

27.6.2.24 Host All Channels Interrupt Mask Register (HAINTMSK,0x418)

	HAINTMSK	Base + 0x418

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																HAINTMsk															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:16	Reserved	R
15:0	Channel Interrupt Mask (HAINTMsk) One bit per channel: Bit 0 for channel 0, bit 15 for channel 15	RW

27.6.2.25 Host Port Control and Status Register (HPRT,0x440)

	HPRT																															Base + 0x440
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved													PrtSpd		PrtTstCtl				PrtPwr	PrtLnSts		Reserved	PrtRst	PrtSusp	PrtRes	PrtOvrCurrChng	PrtOvrCurrAct	PrtEnChng	PrtEna	PrtConnDet	PrtConnSts
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:19	Reserved	R
18:17	Port Speed (PrtSpd) Indicates the speed of the device attached to this port. 2'b00: High speed 2'b01: Full speed 2'b10: Low speed 2'b11: Reserved	R
16:13	Port Test Control (PrtTstCtl) The application writes a nonzero value to this Bits to put the port into a Test mode, and the corresponding pattern is signaled on the port. 4'b0000: Test mode disabled 4'b0001: Test_J mode 4'b0010: Test_K mode 4'b0011: Test_SE0_NAK mode 4'b0100: Test_Packet mode 4'b0101: Test_Force_Enable Others: Reserved	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	For more information on moving the DWC_otg host core into test mode, see "Moving the Host Core to Test Mode" on page 89.	
12	Port Power (PrtPwr) The application uses this Bits to control power to this port (write 1'b1 to set to 1'b1 and write 1'b0 to set to 1'b0), and the core can clear this bit on an over current condition. 1'b0: Power off 1'b1: Power on	R
11:10	Port Line Status (PrtLnSts) Indicates the current logic level USB data lines Bit [10]: Logic level of D+ Bit [11]: Logic level of D-	R
9	Reserved	R
8	Port Reset (PrtRst) When the application sets this bit, a reset sequence is started on this port. The application must time the reset period and clear this bit after the reset sequence is complete. 1'b0: Port not in reset 1'b1: Port in reset To start a reset on the port, the application must leave this bit set for at least the minimum duration mentioned below, as specified in the USB 2.0 specification, Section 7.1.7.5. The application can leave it set for another 10 ms in addition to the required minimum duration, before clearing the bit, even though there is no maximum limit set by the USB standard. High speed: 50 ms Full speed/Low speed: 10 ms	RW
7	Port Suspend (PrtSusp) The application sets this bit to put this port in Suspend mode. The core only stops sending SOFs when this is set. To stop the PHY clock, the application must set the Port Clock Stop bit, which asserts the suspend input pin of the PHY. The read value of this bit reflects the current suspend status of the port. This bit is cleared by the core after a remote wakeup signal is detected or the application sets the Port Reset bit or Port Resume bit in this register or the Resume/Remote Wakeup Detected Interrupt bit or Disconnect Detected Interrupt bit in the Core Interrupt register (GINTSTS.WkUpInt or GINTSTS.DisconnInt, respectively). 1'b0: Port not in Suspend mode 1'b1: Port in Suspend mode	RW[1]
6	Port Resume (PrtRes) The application sets this bit to drive resume signaling on the port. The	RW[2]

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	core continues to drive the resume signal until the application clears this bit. If the core detects a USB remote wakeup sequence, as indicated by the Port Resume/Remote Wakeup Detected Interrupt bit of the Core Interrupt register (GINTSTS.WkUpInt), the core starts driving resume signaling without application intervention and clears this bit when it detects a disconnect condition. The read value of this bit indicates whether the core is currently driving resume signaling. 1'b0: No resume driven 1'b1: Resume driven When LPM is enabled and the core is in the L1 (Sleep) state, setting this bit results in the following behavior: The core continues to drive the resume signal until a pre-determined time specified in the GLPMCFG.HIRD_Thres[3:0] Bits. If the core detects a USB remote wakeup sequence, as indicated by the Port L1 Resume/Remote L1 Wakeup Detected Interrupt bit of the Core Interrupt register (GINTSTS.L1WkUpInt), the core starts driving resume signaling without application intervention and clears this bit at the end of the resume. The read value of this bit indicates whether the core is currently driving resume signaling. 1'b0: No resume driven 1'b1: Resume driven	
5	Port Overcurrent Change (PrtOvrCurrChng) The core sets this bit when the status of the Port Overcurrent Active bit (bit 4) in this register changes.	RW[3]
4	Port Overcurrent Active (PrtOvrCurrAct) Indicates the overcurrent condition of the port. 1'b0: No overcurrent condition 1'b1: Overcurrent condition	R
3	Port Enable/Disable Change (PrtEnChng) The core sets this bit when the status of the Port Enable bit [2] of this register changes.	RW[4]
2	Port Enable (PrtEna) A port is enabled only by the core after a reset sequence, and is disabled by an overcurrent condition, a disconnect condition, or by the application clearing this bit. The application cannot set this bit by a register write. It can only clear it to disable the port. This bit does not trigger any interrupt to the application. 1'b0: Port disabled 1'b1: Port enabled	RW[5]
1	Port Connect Detected (PrtConnDet)	RW[6]

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	The core sets this bit when a device connection is detected to trigger an interrupt to the application using the Host Port Interrupt bit of the Core Interrupt register (GINTSTS.PrtInt). The application must write a 1 to this bit to clear the interrupt.	
0	Port Connect Status (PrtConnSts) 0: No device is attached to the port. 1: A device is attached to the port.	R

Note:

[1], [2]: **This bits will operate with Write set , self clear function.**

[3], [4], [6]: **This bits will operate with Self set , Write clear function.**

[5]: **This bits will operate with Write clear or read clear function.**

27.6.2.26 Host Channel-n Characteristics Register (HCCHARn,0x500+n*0x20)

	HCCHARn																															Base + 0x500+n*0x20
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ChEna	ChDis	OddFrm	DevAddr	DevAddr						EC		EPType		LSpdDev	Reserved	EPDir	EPNum				MPS										
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31	Channel Enable (ChEna) When Scatter/Gather mode is enabled 1'b0: Indicates that the descriptor structure is not yet ready. 1'b1: Indicates that the descriptor structure and data buffer with data is setup and this channel can access the descriptor. When Scatter/Gather mode is disabled This Bits is set by the application and cleared by the OTG host. 1'b0: Channel disabled 1'b1: Channel enabled	RW[1]
30	Channel Disable (ChDis) The application sets this bit to stop transmitting/receiving data on a channel, even before the transfer for that channel is complete. The application must wait for the Channel Disabled interrupt before treating the channel as disabled.	RW[2]
29	Odd Frame (OddFrm) This Bits is set (reset) by the application to indicate that the OTG host must perform a transfer in an odd (micro)frame. This Bits is applicable for only periodic (isochronous and interrupt) transactions.	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	1'b0: Even (micro)frame 1'b1: Odd (micro)frame This Bits is not applicable for Scatter/Gather DMA mode and need not be programmed by the application and is ignored by the core.	
28:22	Device Address (DevAddr) This Bits selects the specific device serving as the data source or sink.	RW
21:20	Multi Count (MC) / Error Count (EC) When the Split Enable bit of the Host Channel-n Split Control register (HCSPLTn.SpltEna) is reset (1'b0), this Bits indicates to the host the number of transactions that must be executed per microframe for this periodic endpoint. For non periodic transfers, this Bits is used only in DMA mode, and specifies the number packets to be fetched for this channel before the internal DMA engine changes aubitration. 2'b00: Reserved This Bits yields undefined results. 2'b01: 1 transaction 2'b10: 2 transactions to be issued for this endpoint per microframe 2'b11: 3 transactions to be issued for this endpoint per microframe When HCSPLTn.SpltEna is set (1'b1), this Bits indicates the number of immediate retries to be performed for a periodic split transactions on transaction errors. This Bits must be set to at least 2'b01.	RW
19:18	Endpoint Type (EPType) Indicates the transfer type selected. 2'b00: Control 2'b01: Isochronous 2'b10: Bulk 2'b11: Interrupt	RW
17	Low-Speed Device (LSpdDev) This Bits is set by the application to indicate that this channel is communicating to a low-speed device. The application must program this bit when a low speed device is connected to the host through an FS HUB. The HS OTG Host core uses this Bits to drive the XCVR_SELECT signal to 2'b11 while communicating to the LS Device through the FS hub. **Note:** In a peer to peer setup, the HS OTG Host core ignores this bit even if it is set by the application software.	RW
16	Reserved	R
15	Endpoint Direction (EPDir) Indicates whether the transaction is IN or OUT. 1'b0: OUT 1'b1: IN	RW
14:11	Endpoint Number (EPNum) Indicates the endpoint number on the device serving as the data source or sink.	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

10:0	Maximum Packet Size (MPS) Indicates the maximum packet size of the associated endpoint.	RW

Note:

[1], [2]: **This bits will operate with Write set , self clear function.**

27.6.2.27 Host Channel-n Split Control Register (HCSPLTn,0x504+n*0x20)

	HCSPLTn																															
																																Base + 0x504+n*0x20
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SpltEna	Reserved														CompSplt	XactPos		HubAddr							PrtAddr						
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31	Split Enable (SpltEna) The application sets this Bits to indicate that this channel is enabled to perform split transactions.	RW
30:17	Reserved	R
16	Do Complete Split (CompSplt) The application sets this Bits to request the OTG host to perform a complete split trsnsaction.	RW
15:14	Transaction Position (XactPos) This Bits is used to determine whether to send all, first, middle, or last payloads with each OUT transaction. 2'b11: All. This is the entire data payload is of this transaction (which is less than or equal to 188 bytes). 2'b10: Begin. This is the first data payload of this transaction (which is larger than 188 bytes). 2'b00: Mid. This is the middle payload of this transaction (which is larger than 188 bytes). 2'b01: End. This is the last payload of this transaction (which is larger than 188 bytes).	RW
13:7	Hub Address (HubAddr) This Bits holds the device address of the transaction translator's hub.	RW
6:0	Port Address (PrtAddr) This Bits is the port number of the recipient transaction translator.	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

27.6.2.28 Host Channel-n Interrupt Register (HCINTn,0x508+n*0x20)

	HCINTn																															Base + 0x508+n*0x20
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																		DESC_LST_ROLLIntr	XCS_XACT_ERR	BNAIntr	DataTglErr	FrmOvrun	BblErr	XactErr	NYET	ACK	NAK	STALL	AHBErr	ChHltd	XferCompl
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:14	Reserved	R
13	Descriptor rollover interrupt (DESC_LST_ROLLIntr) This bit is valid only when Scatter/Gather DMA mode is enabled. The core sets this bit when the corresponding channel's descriptor list rolls over. For non Scatter/Gather DMA mode, this bit is reserved.	RW[1]
12	Excessive Transaction Error (XCS_XACT_ERR) This bit is valid only when Scatter/Gather DMA mode is enabled. The core sets this bit when 3 consecutive transaction errors occurred on the USB bus. XCS_XACT_ERR will not be generated for Isochronous channels. For non Scatter/Gather DMA mode, this bit is reserved.	RW[2]
11	BNA (Buffer Not Available) Interrupt (BNAIntr) This bit is valid only when Scatter/Gather DMA mode is enabled. The core generates this interrupt when the descriptor accessed is not ready for the Core to process. BNA will not be generated for Isochronous channels. For non Scatter/Gather DMA mode, this bit is reserved.	RW[3]
10	Data Toggle Error (DataTglErr) In Scatter/Gather DMA mode, the interrupt due to this bit is masked in the core.	RW[4]
9	Frame Overrun (FrmOvrun) In Scatter/Gather DMA mode, the interrupt due to this bit is masked in the core	RW[5]
8	Babble Error (BblErr) In Scatter/Gather DMA mode, the interrupt due to this bit is masked in the core.	RW[6]
7	Transaction Error (XactErr) Indicates one of the following errors occurred on the USB. CRC check failure Timeout Bit stuff error False EOP	RW[7]

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	In Scatter/Gather DMA mode, the interrupt due to this bit is not set.	
6	NYET Response Received Interrupt (NYET) In Scatter/Gather DMA mode, the interrupt due to this bit is masked in the core.	RW[8]
5	ACK Response Received/Transmitted Interrupt (ACK) In Scatter/Gather DMA mode, the interrupt due to this bit is masked in the core.	RW[9]
4	NAK Response Received Interrupt (NAK) In Scatter/Gather DMA mode, the interrupt due to this bit is masked in the core.	RW[10]
3	STALL Response Received Interrupt (STALL) In Scatter/Gather DMA mode, the interrupt due to this bit is masked in the core.	RW[11]
2	AHB Error (AHBErr) This is generated only in DMA mode when there is an AHB error during AHB read/write. The application can read the corresponding channel's DMA address register to get the error address.	RW[12]
1	Channel Halted (ChHltd) In non Scatter/Gather DMA mode, it indicates the transfer completed abnormally either because of any USB transaction error or in response to disable request by the application or because of a completed transfer. In Scatter/Gather DMA mode, this indicates that transfer completed due to any of the following EOL being set in descriptor AHB error Excessive transaction errors In response to disable request by the application Babble Stall	RW[13]
0	Transfer Completed (XferCompl) For Scatter/Gather DMA mode, it indicates that current descriptor processing got completed with IOC bit set in its descriptor. In non Scatter/Gather DMA mode, it indicates that Transfer completed normally without any errors.	RW[14]

Note:

[1], [2]: **This bits will operate with Self set , write clear function.**

27.6.2.29 Host Channel-n Interrupt Mask Register (HCINTMSKn,0x50C+n*0x20)

	HCINTMSKn	**Base + 0x50C+n*0x20**

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																		ROLLIntrMsk	Reserved	BNAIntrMsk	DataTglErrMsk	DataTglErrMsk	BblErrMsk	XactErrMsk	NyetMsk	AckMsk	NakMsk	StallMsk	AHBErrMsk	ChHltdMsk	XferComplMsk
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:14	Reserved	R
13	Descriptor rollover interrupt Mask register (DESC_LST_ROLLIntrMsk) This bit is valid only when Scatter/Gather DMA mode is enabled. In non Scatter/Gather DMA mode, this bit is reserved.	RW
12	Reserved	R
11	BNA (Buffer Not Available) Interrupt mask register (BNAIntrMsk) This bit is valid only when Scatter/Gather DMA mode is enabled. In non Scatter/Gather DMA mode, this bit is reserved	RW
10	Data Toggle Error Mask (DataTglErrMsk) This bit is not applicable in Scatter/Gather DMA mode.	R
9	Frame Overrun Mask (FrmOvrunMsk) This bit is not applicable in Scatter/Gather DMA mode.	RW
8	Babble Error Mask (BblErrMsk) This bit is not applicable in Scatter/Gather DMA mode.	RW
7	Transaction Error Mask (XactErrMsk) This bit is not applicable in Scatter/Gather DMA mode	RW
6	NYET Response Received Interrupt Mask (NyetMsk) This bit is not applicable in Scatter/Gather DMA mode.	RW
5	ACK Response Received/Transmitted Interrupt Mask (AckMsk) This bit is not applicable in Scatter/Gather DMA mode.	RW
4	NAK Response Received Interrupt Mask (NakMsk) This bit is not applicable in Scatter/Gather DMA mode.	RW
3	STALL Response Received Interrupt Mask (StallMsk) This bit is not applicable in Scatter/Gather DMA mode.	RW
2	AHB Error Mask (AHBErrMsk) Note: This bit is only accessible when OTG_ARCHITECTURE = 2	RW
1	Channel Halted Mask (ChHltdMsk)	RW
0	Transfer Completed Mask (XferComplMsk)	RW

27.6.2.30 Host Channel-n Transfer Size Register (HCTSIZn,0x510+n*0x20)

	HCTSIZn																															Base + 0x510+n*0x20
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Reserved	Pid		Reserved													NTD								SCHED_INFO							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	**Description**	**R/W**
31	Reserved	R
30:29	PID (Pid) The application programs this Bits with the type of PID to use for the initial transaction. The host maintains this Bits for the rest of the transfer. 2'b00: DATA0 2'b01: DATA2 2'b10: DATA1 2'b11: MDATA (non-control)	RW
28:16	Reserved	R
15:8	NTD (Number of Transfer Descriptors) (Non Isochronous) This value is in terms of number of descriptors. Maximum number of descriptor that can be present in the list is 64. The values can be from 0 to 63. 0 - 1 descriptor. 63 - 64 descriptors This Bits indicates the total number of descriptors present in that list. The core will wrap around after servicing NTD number of descriptors for that list. (Isochronous) This Bits indicates the number of descriptors present in that list.µframe The possible values for FS are 1 - 2 descriptors 3 - 4 descriptors 7 - 8 descriptors 15 - 16 descriptors 31 - 32 descriptors 63 - 64 descriptors The possible values for HS are 7 - 8 descriptors 15 - 16 descriptors 31 - 32 descriptors 63 - 64 descriptors 127 - 128 descriptors 255 - 256 descriptors	RW
7:0	SCHED_INFO (Schedule information) Every bit in this 8 bit register indicates scheduling for that microframe. Bit 0 indicates scheduling for 1st microframe and bit 7 indicates scheduling for 8th	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	microframe in that frame. A value of 8'b11111111 indicates that the corresponding interrupt channel is scheduled to issue a token every microframe in that frame. A value of 8'b10101010 indicates that the corresponding interrupt channel is scheduled to issue a token every alternate microframe starting with second microframe. Note that this Bits is applicable only for periodic (Isochronous and Interrupt) channels.	

In Non-Scatter/Gather mode, HCTSIZn is defined as follows:

	HCTSIZn																															**Base + 0x510+n*0x20**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DoPng	Pid		PktCnt										XferSize																		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	**Description**	**R/W**
31	Do Ping (DoPng) This bit is used only for OUT transfers. Setting this Bits to 1 directs the host to do PING protocol. Note: Do not set this bit for IN transfers. If this bit is set for IN transfers it disables the	RW
30:29	PID (Pid) The application programs this Bits with the type of PID to use for the initial transaction. The host maintains this Bits for the rest of the transfer. 2'b00: DATA0 2'b01: DATA2 2'b10: DATA1 2'b11: MDATA (non-control)/SETUP (control)	RW
28:19	Packet Count (PktCnt) This Bits is programmed by the application with the expected number of packets to be transmitted (OUT) or received (IN). The host decrements this count on every successful transmission or reception of an OUT/IN packet. Once this count reaches zero, the application is interrupted to indicate normal completion.	RW
18:0	Transfer Size (XferSize) For an OUT, this Bits is the number of data bytes the host sends during the transfer. For an IN, this Bits is the buffer size that the application has Reserved for the transfer. The application is expected to program this Bits as an integer multiple of the maximum packet size for IN transactions (periodic and non-periodic).	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

27.6.2.31 Host Channel-n DMA Address Register (HCDMAn, ,0x514+n*0x20)

Buffer DMA Mode:

	HCDMAn																															Base + 0x514+n*0x20
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DMAAddr																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:0	DMA Address (DMAAddr) This Bits holds the start address in the external memory from which the data for the endpoint must be fetched or to which it must be stored. This register is incremented on every AHB transaction.	RW

Descriptor DMA Mode：

	HCDMAn																															Base +0x514+n*0x20
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DMAAddr																							CTD						Reserved		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:9 (Non Isoc)	DMA Address (DMAAddr) Non-Isochronous: This Bits holds the start address of the 512 bytes page. The first descriptor in the list should be located in this address. The first descriptor may be or may not be ready. The core starts processing the list from the CTD value. Isochronous: This Bits holds the address of the 2*(nTD+1) bytes of locations in which the isochronous descriptors are present where N is based on nTD as per Table below 31:N | N-1:3 | 2:0 Base Address | Offset | 000	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	HS ISOC nTD N 7 6 15 7 31 8 63 9 127 10 255 11 FS ISOC nTD N 1 4 3 5 7 6 15 7 31 8 63 9	
8:3 (Non Isoc)	Current Transfer Desc (CTD): Non Isochronous: This value is in terms of number of descriptors. The values can be from 0 to 63. 0 - 1 descriptor. 63- 64 descriptors. This Bits indicates the current descriptor processed in the list. This Bits is updated both by application and the core. For example, if the application enables the channel after programming CTD=5, then the core will start processing the 6th descriptor. The address is obtained by adding a value of (8bytes*5=) 40(decimal) to DMAAddr. Isochronous: CTD for isochronous is based on the current frame/µframe value. Need to be set to zero by application.	RW
2:0	Reserved	R

27.6.2.32 Host Channel-n DMA Buffer Address Register (HCDMABn,0x51C+n*0x20)

	HCDMABn																															Base + 0x51C+n*0x20
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	buffer_address																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Description	R/W
31:0	Holds the current buffer address. This register is updated as and when the data transfer for the corresponding end point is in progress. This register is present only in Scatter/Gather DMA mode. Otherwise this Bits is reserved.	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

27.6.2.33 Host Frame List Base Address Register (HFLBAddr,0x51C+n*0x20)

	HFLBAddr																															Base + 0x41C+n*0x20
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	flarm_list																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:0	The starting address of the Frame list. This register is used only for Isochronous and Interrupt Channels.	RW

27.6.2.34 Device Configuration Register (DCFG,0x800)

	DCFG																															Base + 0x800
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ResValid						PerSchIntvl		DescDMA	EPMisCnt					Reserved				EnDevOutNak	PerFrInt		DevAddr							Ena32KHzS	NZStsOUTHShk	DevSpd	
RST	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:26	Resume Validation Period (ResValid) This Bits controls the period when the core resumes from a suspend. When this bit is set, the core counts for the ResValid number of clock cycles to detect a valid resume. This Bits is effective only when DCFG.Ena32KHzSusp is set.	RW
25:24	Periodic Scheduling Interval (PerSchIntvl) PerSchIntvl must be programmed only for Scatter/Gather DMA mode. Description: This Bits specifies the amount of time the Internal DMA engine must allocate for fetching periodic IN endpoint data. Based on the number of periodic endpoints, this value must be specified as 25,50 or 75% of (micro)frame. When any periodic endpoints are active, the internal DMA engine allocates the specified amount of time in fetching periodic IN endpoint data. When no periodic endpoints are active, then the internal DMA engine services non-periodic endpoints, ignoring this Bits. After the specified time within a (micro)frame, the DMA switches to fetching for non-	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	periodic endpoints. 2'b00: 25% of (micro)frame. 2'b01: 50% of (micro)frame. 2'b10: 75% of (micro)frame. 2'b11: Reserved.	
23	Enable Scatter/Gather DMA in Device mode (DescDMA). When the Scatter/Gather DMA option selected during configuration of the RTL, the application can set this bit during initialization to enable the Scatter/Gather DMA operation. NOTE: This bit must be modified only once after a reset. The following combinations are available for programming: GAHBCFG.DMAEn=0,DCFG.DescDMA=0 => Slave mode GAHBCFG.DMAEn=0,DCFG.DescDMA=1 => Invalid GAHBCFG.DMAEn=1,DCFG.DescDMA=0 => Buffered DMA mode GAHBCFG.DMAEn=1,DCFG.DescDMA=1 => Scatter/Gather DMA mode	RW
22:18	IN Endpoint Mismatch Count (EPMisCnt) This Bits is valid only in shared FIFO operation. The application programs this filed with a count that determines when the core generates an Endpoint Mismatch interrupt (GINTSTS.EPMis). The core loads this value into an internal counter and decrements it. The counter is reloaded whenever there is a match or when the counter expires. The width of this counter depends on the depth of the Token Queue.	RW
17:14	Reserved	R
13	Enable Device OUT NAK (EnDevOutNak) This bit enables setting NAK for Bulk OUT endpoints after the transfer is completed when the core is operating in Device Descriptor DMA mode. 1'b0: The core does not set NAK after Bulk OUT transfer complete 1'b1: The core sets NAK after Bulk OUT transfer complete This bit is valid only when OTG_EN_DESC_DMA == 1'b1	RW
12:11	Periodic Frame Interval (PerFrInt) Indicates the time within a (micro)frame at which the application must be notified using the End Of Periodic Frame Interrupt. This can be used to determine if all the isochronous traffic for that (micro)frame is complete. 2'b00: 80% of the (micro)frame interval 2'b01: 85% 2'b10: 90% 2'b11: 95%	RW
10:4	Device Address (DevAddr) The application must program this Bits after every SetAddress control command.	RW
3	Enable 32-KHz Suspend Mode (Ena32KHzS) When the USB 1.1 Full-Speed Serial Transceiver Interface is chosen and this bit is set, the core expects the 48-MHz PHY clock to be switched to 32 KHz during a	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	suspend. This bit can only be set if USB 1.1 Full-Speed Serial Transceiver Interface has been selected. If USB 1.1 Full-Speed Serial Transceiver Interface has not been selected, this bit must be zero.	
2	Non-Zero-Length Status OUT Handshake (NZStsOUTHShk) The application can use this Bits to select the handshake the core sends on receiving a nonzero-length data packet during the OUT transaction of a control transfer's Status stage. 1'b1: Send a STALL handshake on a nonzero-length status OUT transaction and do not send the received OUT packet to the application. 1'b0: Send the received OUT packet to the application (zero-length or nonzero-length) and send a handshake based on the NAK and STALL bits for the endpoint in the Device Endpoint Control register.	RW
1:0	Device Speed (DevSpd) Indicates the speed at which the application requires the core to enumerate, or the maximum speed the application can support. However, the actual bus speed is determined only after the chirp sequence is completed, and is based on the speed of the USB host to which the core is connected. 2'b00: High speed (USB 2.0 PHY clock is 30 MHz or 60 MHz) 2'b01: Full speed (USB 2.0 PHY clock is 30 MHz or 60 MHz) 2'b10: Low speed (USB 1.1 FS transceiver clock is 48 MHz) 2'b11: Full speed (USB 1.1 FS transceiver clock is 48 MHz)	RW

27.6.2.35 Device Control Register (DCTL,0x804)

	DCTL																															Base + 0x804
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved														EnContOnBNA	NakOnBble	IgnrFrmNum	GMC		Reserved	PWROnPrgDone	CGOUTNak	SGOUTNak	CGNPInNak	SGNPInNak	TstCtl			GOUTNakSts	GNPINNakSts	SftDiscon	RmtWkUpSig
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Description	R/W
31:18	Reserved	R
17	Enable Continue on BNA (EnContOnBNA) This bit enables the DWC_otg core to continue on BNA for Bulk OUT endpoints. With this feature enabled, when a Bulk OUT endpoint receives a BNA interrupt the core starts processing the descriptor that caused the BNA interrupt after the endpoint re-enables the endpoint. 1'b0: After receiving BNA interrupt, the core disables the endpoint. When the	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	endpoint is re-enabled by the application, the core starts processing from the DOEPDMA descriptor. 1'b1: After receiving BNA interrupt, the core disables the endpoint. When the endpoint is re-enabled by the application, the core starts processing from the descriptor that received the BNA interrupt. This bit is valid only when OTG_EN_DESC_DMA == 1'b1. It is a one-time programmable after reset bit like any other DCTL register bits.	
16	Set NAK automatically on babble (NakOnBble). The core sets NAK automatically for the endpoint on which babble is received.	RW
15	Ignore frame number for isochronous endpoints (IgnrFrmNum) Slave Mode (GAHBCFG.DMAEn=0): This bit is not valid in Slave mode and should not be programmed to 1.Non-Scatter/Gather DMA mode (GAHBCFG.DMAEn=1,DCFG.DescDMA=0): This bit is not used when Threshold mode is enabled and should not be programmed to 1. In non-Scatter/Gather DMA mode, the application receives transfer complete interrupt after transfers for multiple (micro)frames are completed. When Scatter/Gather DMA mode is disabled, this Bits is used by the application to enable periodic transfer interrupt. The application can program periodic endpoint transfers for multiple (micro)frames. 0: Periodic transfer interrupt feature is disabled; the application must program transfers for periodic endpoints every (micro)frame 1: Packets are not flushed when an ISOC IN token is received for an elapsed frame. The core ignores the frame number, sending packets as soon as the packets are ready, and the corresponding token is received. This Bits is also used by the application to enable periodic transfer interrupts. Scatter/Gather DMA Mode (GAHBCFG.DMAEn=1,DCFG.DescDMA=1): This bit is not applicable to high-speed, high-bandwidth transfers and should not be programmed to 1. In addition, this bit is not used when Threshold mode is enabled and should not be programmed to 1. 0: The core transmits the packets only in the frame number in which they are intended to be transmitted. 1: Packets are not flushed when an ISOC IN token is received for an elapsed frame. The core ignores the frame number, sending packets as soon as the packets are ready, and the corresponding token is received. When this bit is set, there must be only one packet per descriptor.	RW
14:13	Global Multi Count (GMC) GMC must be programmed only once after initialization. Applicable only for Scatter/Gather DMA mode. This indicates the number of packets to be serviced for that end point before moving to the next end point. It is only for non- periodic end points. 2'b00: Invalid.	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	2'b01: 1 packet. 2'b10: 2 packets. 2'b11: 3 packets. The value of this Bits automatically changes to 2'h1 when DCFG.DescDMA is set to 1. When Scatter/Gather DMA mode is disabled, this Bits is reserved and reads 2'b00.	
12	Reserved	R
11	Power-On Programming Done (PWROnPrgDone) The application uses this bit to indicate that register programming is completed after a wake-up from Power Down mode.	W
10	Clear Global OUT NAK (CGOUTNak) A write to this Bits clears the Global OUT NAK.	W
9	Set Global OUT NAK (SGOUTNak) A write to this Bits sets the Global OUT NAK. The application uses this bit to send a NAK handshake on all OUT endpoints. The application must set the this bit only after making sure that the Global OUT NAK Effective bit in the Core Interrupt Register (GINTSTS.GOUTNakEff) is cleared.	W
8	Clear Global Non-periodic IN NAK (CGNPInNak) A write to this Bits clears the Global Non-periodic IN NAK.	W
7	Set Global Non-periodic IN NAK (SGNPInNak) A write to this Bits sets the Global Non-periodic IN NAK.The application uses this bit to send a NAK handshake on all non-periodic IN endpoints. The core can also set this bit when a timeout condition is detected on a non-periodic endpoint in shared FIFO operation. The application must set this bit only after making sure that the Global IN NAK Effective bit in the Core Interrupt Register (GINTSTS.GINNakEff) is cleared.	W
6:4	Test Control (TstCtl) 3'b000: Test mode disabled 3'b001: Test_J mode 3'b010: Test_K mode 3'b011: Test_SE0_NAK mode 3'b100: Test_Packet mode 3'b101: Test_Force_Enable Others: Reserved	RW
3	Global OUT NAK Status (GOUTNakSts) 1'b0: A handshake is sent based on the FIFO Status and the NAK and STALL bit settings. 1'b1: No data is written to the RxFIFO, irrespective of space availability. Sends a NAK handshake on all packets, except on SETUP transactions. All isochronous OUT packets are dropped.	W
2	Global Non-periodic IN NAK Status (GNPINNakSts)	W

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	1'b0: A handshake is sent out based on the data availability in the transmit FIFO. 1'b1: A NAK handshake is sent out on all non-periodic IN endpoints, irrespective of the data availability in the transmit FIFO.	
1	Soft Disconnect (SftDiscon) The application uses this bit to signal the DWC_otg core to do a soft disconnect. As long as this bit is set, the host does not see that the device is connected, and the device does not receive signals on the USB. The core stays in the disconnected state until the application clears this bit. The minimum duration for which the core must keep this bit set is specified in Table 27-3. 1'b0: Normal operation. When this bit is cleared after a soft disconnect, the core drives the phy_opmode_o signal on the UTMI+ to 2'b00, which generates a device connect event to the USB host. When the device is reconnected, the USB host restarts device enumeration. 1'b1: The core drives the phy_opmode_o signal on the UTMI+ to 2'b01, which generates a device disconnect event to the USB host. Note: This bit can be also used for ULPI/FS Serial interfaces. Note: This bit is not impacted by a soft reset.	RW
0	Remote Wakeup Signaling (RmtWkUpSig) When the application sets this bit, the core initiates remote signaling to wake the USB host. The application must set this bit to instruct the core to exit the Suspend state. As specified in the USB 2.0 specification, the application must clear this bit 1-15 ms after setting it.If LPM is enabled and the core is in the L1 (Sleep) state, when the application sets this bit, the core initiates L1 remote signaling to wake up the USB host. The application must set this bit to instruct the core to exit the Sleep state. As specified in the LPM specification, the hardware automatically clears this bit 50 µs ($T_{L1DevDrvResume}$) after being set by the application. The application must not set this bit when GLPMCFG bRemoteWake from the previous LPM transaction is zero.	RW

Table 27-3 Minimum Duration for Soft Disconnect

Operating Speed	Device state	Minimum Duration
High Speed	Suspend	1ms+2.5us
High Speed	Idle	3ms+2.5us
High Speed	Not Idle or Suspend	125us
Full Speed/Low Speed	Suspend	1ms+2.5us
Full Speed/Low Speed	Idle	2.5us
Full Speed/Low Speed	Not Idle or Suspend	2.5us

27.6.2.36 Device Status Register (DSTS,0x808)

	DSTS																															Base + 0x808
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Reserved										SOFFN														Reserved				ErrticErr	EnumSpd		SuspSts
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	**Description**	**R/W**
31:22	Reserved	R
21:8	Frame or Microframe Number of the Received SOF (SOFFN) When the core is operating at high speed, this Bits contains a microframe number. When the core is operating at full or low speed, this Bits contains a frame number. Note: This register may return a non zero value if read immediately after power on reset. In case the register bit reads non zero immediately after power on reset it does not indicate that SOF has been received from the host. The read value of this interrupt is valid only after a valid connection between host and device is established.	R
7:4	Reserved	R
3	Erratic Error (ErrticErr) The core sets this bit to report any erratic errors (phy_rxvalid_i/phy_rxvldh_i or phy_rxactive_i is asserted for at least 2 ms, due to PHY error) seen on the UTMI+. Due to erratic errors, the DWC_otg core goes into Suspended state and an interrupt is generated to the application with Early Suspend bit of the Core Interrupt register (GINTSTS.ErlySusp). If the early suspend is asserted due to an erratic error, the application can only perform a soft disconnect recover.	R
2:1	Enumerated Speed (EnumSpd) Indicates the speed at which the DWC_otg core has come up after speed detection through a chirp sequence. 2'b00: High speed (PHY clock is running at 30 or 60 MHz) 2'b01: Full speed (PHY clock is running at 30 or 60 MHz) 2'b10: Low speed (PHY clock is running at 48 MHz, internal phy_clk at 6 MHz) 2'b11: Full speed (PHY clock is running at 48 MHz) Low speed is not supported for devices using a UTMI+ PHY.	R
0	Suspend Status (SuspSts) In Device mode, this bit is set as long as a Suspend condition is detected on the USB. The core enters the Suspended state when there is no activity on the utmi_linestate signal for an extended period of time. The core comes out of the suspend: When there is any activity on the utmi_linestate signal When the application writes to the Remote Wakeup Signaling bit in the Device Control register (DCTL.RmtWkUpSig).	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

27.6.2.37 Device IN Endpoint Common Interrupt Mask Register (DIEPMSK,0x810)

	DIEPMSK																															Base + 0x810
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																		NAKMsk	NAKMsk			BNAInIntrMsk	TxfifoUndrnMsk	Reserved	INEPNakEffMsk	INTknEPMisMsk	INTknTXFEmpMsk	TimeOUTMsk	AHBErrMsk	EPDisbldMsk	XferComplMsk
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:14	Reserved	R
13	NAK interrupt Mask (NAKMsk)	RW
12:10	Reserved	R
9	BNA Interrupt Mask (BNAInIntrMsk) This bit is valid only when Device Descriptor DMA is enabled.	RW
8	Fifo Underrun Mask (TxfifoUndrnMsk)	RW
7	Reserved	R
6	IN Endpoint NAK Effective Mask (INEPNakEffMsk)	RW
5	IN Token received with EP Mismatch Mask (INTknEPMisMsk)	RW
4	IN Token Received When TxFIFO Empty Mask (INTknTXFEmpMsk)	RW
3	Timeout Condition Mask (TimeOUTMsk) (Non-isochronous endpoints)	RW
2	AHB Error Mask (AHBErrMsk)	RW
1	Endpoint Disabled Interrupt Mask (EPDisbldMsk)	RW
0	Transfer Completed Interrupt Mask (XferComplMsk)	RW

27.6.2.38 Device OUT Endpoint Common Interrupt Mask Register (DOEPMSK,0x814)

	DOEPMSK																															Base + 0x814
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																	NYETMsk	NAKMsk	BbleErrMsk	Reserved		BnaOutIntrMsk	OutPktErrMsk	Reserved	Back2BackSETup	Reserved	OUTTknEPdisMsk	SetUPMsk	AHBErrMsk	EPDisbldMsk	XferComplMsk
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Description	R/W
31:15	Reserved	R
14	NYET Interrupt Mask (NYETMsk)	RW
13	NAK Interrupt Mask (NAKMsk)	RW
12	Babble Interrupt Mask (BbleErrMsk)	RW
11:10	Reserved	R
9	BNA interrupt Mask (BnaOutIntrMsk)	RW
8	OUT Packet Error Mask (OutPktErrMsk)	RW
7	Reserved	R
6	Back-to-Back SETUP Packets Received Mask (Back2BackSETup) Applies to control OUT endpoints only.	RW
5	Reserved	R
4	OUT Token Received when Endpoint Disabled Mask (OUTTknEPdisMsk) Applies to control OUT endpoints only.	RW
3	SETUP Phase Done Mask (SetUPMsk) Applies to control endpoints only.	RW
2	AHB Error (AHBErrMsk)	RW
1	Endpoint Disabled Interrupt Mask (EPDisbldMsk)	RW
0	Transfer Completed Interrupt Mask (XferComplMsk)	RW

27.6.2.39 Device All Endpoints Interrupt Register (DAINT,0x818)

	DAINT																															Base + 0x818
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OutEPInt																InEpInt															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:16	OUT Endpoint Interrupt Bits (OutEPInt) One bit per OUT endpoint: Bit 16 for OUT endpoint 0, bit 31 for OUT endpoint 15	R
15:0	IN Endpoint Interrupt Bits (InEpInt) One bit per IN Endpoint: Bit 0 for IN endpoint 0, bit 15 for endpoint 15	R

27.6.2.40 Device All Endpoints Interrupt Mask Register (DAINTMSK,0x81C)

	DAINTMSK	Base + 0x81C

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OutEpMsk																InEpMsk															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:16	OUT EP Interrupt Mask Bits (OutEpMsk) One per OUT Endpoint: Bit 16 for OUT EP 0, bit 31 for OUT EP 15 The value of this Bits depends on the number of OUT endpoints that are configured.	RW
15:0	IN EP Interrupt Mask Bits (InEpMsk) One bit per IN Endpoint: Bit 0 for IN EP 0, bit 15 for IN EP 15 The value of this Bits depends on the number of IN endpoints that are configured.	RW

27.6.2.41 Device IN Token Sequence Learning Queue Read Register 1 (DTKNQR1,0x820)

	DTKNQP1																															Base + 0x820
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EPTkn																								WrapBit	Reserved		INTknWPtr				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:8	Endpoint Token (EPTkn) Four bits per token represent the endpoint number of the token: Bits [31:28]: Endpoint number of Token 5 Bits [27:24]: Endpoint number of Token 4 ..... Bits [15:12]: Endpoint number of Token 1 Bits [11:8]: Endpoint number of Token 0	R
7	Wrap Bit (WrapBit) This bit is set when the write pointer wraps. It is cleared when the learning queue is cleared.	R
6:5	Reserved	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

4:0	IN Token Queue Write Pointer (INTknWPtr)	R

27.6.2.42 Device IN Token Sequence Learning Queue Read Register 2 (DTKNQR2,0x824)

	DTKNQR2																															Base + 0x824
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EPTkn																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:0	Endpoint Token (EPTkn) Four bits per token represent the endpoint number of the token: Bits [31:28]: Endpoint number of Token 13 Bits [27:24]: Endpoint number of Token 12 ..... Bits [7:4]: Endpoint number of Token 7 Bits [3:0]: Endpoint number of Token 6	R

27.6.2.43 Device IN Token Sequence Learning Queue Read Register 3 (DTKNQR3,0x830)

	DTKNQR3																															Base + 0x830
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EPTkn																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:0	Endpoint Token (EPTkn) Four bits per token represent the endpoint number of the token: Bits [31:28]: Endpoint number of Token 21 Bits [27:24]: Endpoint number of Token 20 ..... Bits [7:4]: Endpoint number of Token 15 Bits [3:0]: Endpoint number of Token 14	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

27.6.2.44 Device IN Token Sequence Learning Queue Read Register 4 (DTKNQR4,0x834)

	DTKNQR4																															Base + 0x834
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EPTkn																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:0	Endpoint Token (EPTkn) Four bits per token represent the endpoint number of the token: Bits [31:28]: Endpoint number of Token 29 Bits [27:24]: Endpoint number of Token 28 ..... Bits [7:4]: Endpoint number of Token 23 Bits [3:0]: Endpoint number of Token 22	R

27.6.2.45 Device VBUS Discharge Time Register (DVBUSDIS,0x828)

	DVBUSDIS																															Base + 0x828
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																DVBUSDis															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Description	R/W
31:16	Reserved	R
15:0	Device VBUS Discharge Time (DVBUSDis) Specifies the VBUS discharge time after VBUS pulsing during SRP. This value equals: VBUS discharge time in PHY clocks / 1,024 The value you use depends whether the PHY is operating at 30 MHz (16-bit data width) or 60 MHz (8-bit data width). Depending on your VBUS load, this value can need adjustment. The reset value is :	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	PHY CLK 30MHz :0x0B8F PHY CLK 60MHz :0x17D7	

27.6.2.46 Device VBUS Pulsing Time Register (DVBUSPULSE,0x82C)

	DVBUSPULSE																															Base + 0x82C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				DVBUSPulse											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Description	R/W
31:12	Reserved	R
11:0	Device VBUS Pulsing Time (DVBUSPulse) Specifies the VBUS pulsing time during SRP. This value equals: VBUS pulsing time in PHY clocks / 1,024 The value you use depends whether the PHY is operating at 30 MHz (16-bit data width) or 60 MHz (8-bit data width). The reset value is : PHY CLK 30MHz :0x2C6 PHY CLK 60MHz :0x5B8	RW

27.6.2.47 Device Threshold Control Register (DTHRCTL,0x830)

	DTHRCTL																															Base + 0x830
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				ArbPrkEn	Reserved	RxThrLen									RxThrEn	Reserved			AHBThrRatio		TxThrLen									ISOThrEn	NonISOThrEn
RST	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Description	R/W
31:28	Reserved	R
27	Arbiter Parking Enable (ArbPrkEn) This bit controls internal DMA arbiter parking for IN endpoints. When thresholding is enabled and this bit is set to one, then the arbiter parks on the IN endpoint for which there is a token received on the USB. This is done to avoid getting into underrun	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	conditions. By default the parking is enabled.	
26	Reserved	R
25:17	Receive Threshold Length (RxThrLen) This Bits specifies Receive thresholding size in DWORDS. This Bits also specifies the amount of data received on the USB before the core can start transmitting on the AHB. The threshold length has to be at least eight DWORDS. The recommended value for ThrLen is to be the same as the programmed AHB Burst Length (GAHBCFG.HBstLen).	RW
16	Receive Threshold Enable (RxThrEn) When this bit is set, the core enables thresholding in the receive direction. Note: Synopsys recommends that you do not enable RxThrEn, because it may cause issues in the RxFIFO especially during error conditions such as RxError and Babble.	RW
15:13	Reserved	R
12:11	AHB Threshold Ratio (AHBThrRatio) These bits define the ratio between the AHB threshold and the MAC threshold for the transmit path only. The AHB threshold always remains less than or equal to the USB threshold, because this does not increase overhead. Both the AHB and the MAC threshold must be DWORD-aligned. The application needs to program TxThrLen and the AHBThrRatio to make the AHB Threshold value DWORD aligned. If the AHB threshold value is not DWORD aligned, the core might not behave correctly. When programming the TxThrLen and AHBThrRatio, the application must ensure that the minimum AHB threshold value does not go below 8 DWORDS to meet the USB turnaround time requirements.	RW
10:2	Transmit Threshold Length (TxThrLen) This Bits specifies Transmit thresholding size in DWORDS. This Bits also forms the MAC threshold and specifies the amount of data, in bytes, to be in the corresponding endpoint transmit FIFO before the core can start a transmit on the USB. When the value of AHBThrRatio is 2'h00, the threshold length must be at least 8 DWORDS. If the AHBThrRatio is nonzero, the application must ensure that the AHB threshold value does not go below the recommended 8 DWORDs. This Bits controls both isochronous and non-isochronous IN endpoint thresholds. The recommended value for ThrLen is to be the same as the programmed AHB Burst Length (GAHBCFG.HBstLen).	RW
1	ISO IN Endpoints Threshold Enable. (ISOThrEn) When this bit is set, the core enables thresholding for isochronous IN endpoints.	RW
0	Non-ISO IN Endpoints Threshold Enable. (NonISOThrEn) When this bit is set, the core enables thresholding for Non Isochronous IN endpoints.	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

27.6.2.48 Device IN Endpoint FIFO Empty Interrupt Mask Register(DIEPEMPMSK,0x834)

	DIEPEMPMSK																															Base + 0x834
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																InEpTxfEmpMsk															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:16	Reserved	R
15:0	IN EP Tx FIFO Empty Interrupt Mask Bits (InEpTxfEmpMsk) These bits acts as mask bits for DIEPINTn. TxFEmp interrupt One bit per IN Endpoint: Bit 0 for IN endpoint 0 ... Bit 15 for endpoint 15	RW

27.6.2.49 Device Each Endpoint Interrupt Register (DEACHINT,0x838)

	DEACHINT																															Base + 0x838
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EchOutEPInt																EchInEpInt															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:16	OUT Endpoint Interrupt Bits (EchOutEPInt) One bit per OUT endpoint: Bit 16 for OUT endpoint 0 ... Bit 31 for OUT endpoint 15	R
15:0	IN Endpoint Interrupt Bits (EchInEpInt) One bit per IN Endpoint: Bit 0 for IN endpoint 0 ... Bit 15 for IN endpoint 15	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

27.6.2.50 Device Each Endpoint Interrupt Register Mask (DEACHINTMSK,0x83C)

	DEACHINTMSK																															Base + 0x83C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EchOutEPInt																EchInEpInt															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:16	OUT EP Interrupt Mask Bits (EchOutEpMsk) One per OUT Endpoint: Bit 16 for IN endpoint 0 ... Bit 31 for IN endpoint 15	RW
15:0	IN EP Interrupt Mask Bits (EchInEpMsk) One bit per IN Endpoint: Bit 0 for IN endpoint 0 ... Bit 15 for IN endpoint 15	RW

27.6.2.51 Device Each In Endpoint-n Interrupt Register (DIEPEACHMSKn,0x840)

	DIEPEACHMSKn																															Base + 0x840
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																		NAKMsk	Reserved			BNAInIntrMsk	TxfifoUndrnMsk	Reserved	INEPNakEffMsk	INTknEPMisMsk	INTknTXFEmpMsk	TimeOUTMsk	AHBErrMsk	EPDisbldMsk	XferComplMsk
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:14	Reserved	R
13	NAK interrupt Mask (NAKMsk)	RW
12:10	Reserved	R
9	BNA interrupt Mask (BNAInIntrMsk)	RW
8	Fifo Under run Mask (TxfifoUndrnMsk)	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

7	Reserved	R
6	IN Endpoint NAK Effective Mask (INEPNakEffMsk)	RW
5	IN Token received with EP Mismatch Mask (INTknEPMisMsk)	RW
4	IN Token Received When TxFIFO Empty Mask (INTknTXFEmpMsk)	RW
3	Timeout Condition Mask (TimeOUTMsk) (Non-isochronous endpoints)	RW
2	AHB Error Mask (AHBErrMsk)	RW
1	Endpoint Disabled Interrupt Mask (EPDisbldMsk)	RW
0	Transfer Completed Interrupt Mask (XferComplMsk)	RW

27.6.2.52 Device Each Out Endpoint-n Interrupt Register (DOEPEACHMSKn,0x880+n*0x4)

	DOEPEACHMSKn																															Base + 0x880+n*0x4
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																	NYETMsk	NAKMsk	BbleErrMsk	Reserved		BnaOutIntrMsk	OutPktErrMsk	Reserved	Back2BackSETup	Reserved	OUTTknEPdisMsk	SetUPMsk	AHBErrMsk	EPDisbldMsk	XferComplMsk
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:15	Reserved	R
14	NYET interrupt Mask (NYETMsk)	RW
13	NAK interrupt Mask (NAKMsk)	RW
12	Babble interrupt Mask (BbleErrMsk)	RW
11:10	Reserved	R
9	BNA interrupt Mask (BnaOutIntrMsk)	RW
8	OUT Packet Error Mask (OutPktErrMsk)	RW
7	Reserved	R
6	Back-to-Back SETUP Packets Received Mask (Back2BackSETup) Applies to control OUT endpoints only.	RW
5	Reserved	R
4	OUT Token Received when Endpoint Disabled Mask (OUTTknEPdisMsk) Applies to control OUT endpoints only.	RW
3	SETUP Phase Done Mask (SetUPMsk) Applies to control endpoints only.	RW
2	AHB Error (AHBErrMsk)	RW
1	Endpoint Disabled Interrupt Mask (EPDisbldMsk)	RW
0	Transfer Completed Interrupt Mask (XferComplMsk)	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

27.6.2.53 Device Control IN Endpoint 0 Control Register (DIEPCTL0,0x900)

	DIEPCTL0																															Base + 0x900
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EPEna	EPDis	Reserved		SNAK	CNAK	TxFNum				Stall	Reserved	EPType		NAKSts	Reserved	USBActEP	NextEp				Reserved									MPS	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31	Endpoint Enable (EPEna) When Scatter/Gather DMA mode is enabled, for IN endpoints this bit indicates that the descriptor structure and data buffer with data ready to transmit is setup. When Scatter/Gather DMA mode is disabled—such as in buffer-pointer based DMA mode—this bit indicates that data is ready to be transmitted on the endpoint. The core clears this bit before setting the following interrupts on this endpoint: Endpoint Disabled Transfer Completed	RW[1]
30	Endpoint Disable (EPDis) The application sets this bit to stop transmitting data on an endpoint, even before the transfer for that endpoint is complete. The application must wait for the Endpoint Disabled interrupt before treating the endpoint as disabled. The core clears this bit before setting the Endpoint Disabled Interrupt. The application must set this bit only if Endpoint Enable is already set for this endpoint. This bit is valid only when DMA mode is enabled.	RW[2]
29:28	Reserved	R
27	Set NAK (SNAK) A write to this bit sets the NAK bit for the endpoint. Using this bit, the application can control the transmission of NAK handshakes on an endpoint. The core can also set this bit for an endpoint after a SETUP packet is received on that endpoint.	W
26	Clear NAK (CNAK) A write to this bit clears the NAK bit for the endpoint.	W
25:22	TxFIFO Number (TxFNum) For Shared FIFO operation, this value is always set to 0, indicating that control IN endpoint 0 data is always written in the Non-Periodic Transmit FIFO. For Dedicated FIFO operation, this value is set to the FIFO number that is assigned to IN Endpoint 0.	RW
21	STALL Handshake (Stall) The application can only set this bit, and the core clears it, when a SETUP token is received for this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT	RW[3]

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	NAK is set along with this bit, the STALL bit takes priority.	
20	Reserved	R
19:18	Endpoint Type (EPType) Hardcoded to 00 for control.	R
17	NAK Status (NAKSts) Indicates the following: 1'b0: The core is transmitting non-NAK handshakes based on the FIFO status 1'b1: The core is transmitting NAK handshakes on this endpoint. When this bit is set, either by the application or core, the core stops transmitting data, even if there is data available in the TxFIFO. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake.	R
16	Reserved	R
15	USB Active Endpoint (USBActEP) This bit is always set to 1, indicating that control endpoint 0 is always active in all configurations and interfaces.	R
14:11	Next Endpoint (NextEp) Applies to non-periodic IN endpoints only. Indicates the endpoint number to be fetched after the data for the current endpoint is fetched. The core can access this Bits, even when the Endpoint Enable (EPEna) bit is not set. This Bits is not valid in Slave mode. Note: This Bits is valid only for Shared FIFO operations.	RW
10:2	Reserved	R
1:0	Maximum Packet Size (MPS) Applies to IN and OUT endpoints. The application must program this Bits with the maximum packet size for the current logical endpoint.	RW

Note:

[1], [2], [3]: This bits will operate with Write set , self clear function.

27.6.2.54 Device Control OUT Endpoint 0 Control Register (DOEPCTL0,0xB00)

	DOEPCTL																															Base + 0xB00
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EPEna	EPDis	Reserved		SNAK	CNAK	Reserved				Stall	Snp	EPType		NAKSts	Reserved	USBActEP	Reserved													MPS	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

31	Endpoint Enable (EPEna) When Scatter/Gather DMA mode is enabled, for OUT endpoints this bit indicates that the descriptor structure and data buffer to receive data is setup. When Scatter/Gather DMA mode is disabled—(such as for buffer-pointer based DMA mode)—this bit indicates that the application has allocated the memory to start receiving data from the USB. The core clears this bit before setting any of the following interrupts on this endpoint: SETUP Phase Done Endpoint Disabled Transfer Completed Note: In DMA mode, this bit must be set for the core to transfer SETUP data packets into memory.	RW[1]
30	Endpoint Disable (EPDis) The application cannot disable control OUT endpoint 0.	R
29:28	Reserved	R
27	Set NAK (SNAK) A write to this bit sets the NAK bit for the endpoint. Using this bit, the application can control the transmission of NAK handshakes on an endpoint. The core can also set bit on a Transfer Completed interrupt, or after a SETUP is received on the endpoint.	W
26	Clear NAK (CNAK) A write to this bit clears the NAK bit for the endpoint.	W
25:22	Reserved	R
21	STALL Handshake (Stall) The application can only set this bit, and the core clears it, when a SETUP token is received for this endpoint. If a NAK bit or Global OUT NAK is set along with this bit, the STALL bit takes priority. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake.	RW[2]
20	Snoop Mode (Snp) This bit configures the endpoint to Snoop mode. In Snoop mode, the core does not check the correctness of OUT packets before transferring them to application memory.	RW
19:18	Endpoint Type (EPType) Hardcoded to 2'b00 for control.	R
17	NAK Status (NAKSts) Indicates the following: 1'b0: The core is transmitting non-NAK handshakes based on the FIFO status. 1'b1: The core is transmitting NAK handshakes on this endpoint. When either the application or the core sets this bit, the core stops receiving data, even if there is space in the RxFIFO to accommodate the incoming packet. Irrespective of this bit's setting, the core always responds to SETUP data packets with	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	an ACK handshake.	
16	Reserved	R
15	USB Active Endpoint (USBActEP) This bit is always set to 1, indicating that a control endpoint 0 is always active in all configurations and interfaces.	R
14:2	Reserved	R
1:0	Maximum Packet Size (MPS) The maximum packet size for control OUT endpoint 0 is the same as what is programmed in control IN Endpoint 0. 2'b00: 64 bytes 2'b01: 32 bytes 2'b10: 16 bytes 2'b11: 8 bytes	R

Note:

[1], [2]: This bits will operate with Write set , self clear function.

27.6.2.55 Device Endpoint-n Control Register (DIEPCTLn/DOEPCTLn, 0x900/0xB00+n*0x20)

	DIEPCTLn/DOEPCTLn																Base + 0x900/0xB00+n*0x20															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EPEna	EPDis	SetD1PID	SetD0PID	SNAK	CNAK	TxFNum				Stall	Snp	EPType		NAKSts	DPID	USBActEP	NextEp				MPS										
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31	Endpoint Enable (EPEna) Applies to IN and OUT endpoints. When Scatter/Gather DMA mode is enabled, For IN endpoints this bit indicates that the descriptor structure and data buffer with data ready to transmit is setup. For OUT endpoint it indicates that the descriptor structure and data buffer to receive data is setup. When Scatter/Gather DMA mode is enabled—such as for buffer-pointer based DMA mode: For IN endpoints, this bit indicates that data is ready to be transmitted on the endpoint. For OUT endpoints, this bit indicates that the application has allocated the memory to start receiving data from the USB. The core clears this bit before setting any of the following interrupts on this endpoint.	RW[1]

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	SETUP Phase Done Endpoint Disabled Transfer Completed Note: For control endpoints in DMA mode, this bit must be set to be able to transfer SETUP data packets in memory.	
30	Endpoint Disable (EPDis) Applies to IN and OUT endpoints. The application sets this bit to stop transmitting/receiving data on an endpoint, even before the transfer for that endpoint is complete. The application must wait for the Endpoint Disabled interrupt before treating the endpoint as disabled. The core clears this bit before setting the Endpoint Disabled interrupt. The application must set this bit only if Endpoint Enable is already set for this endpoint.	RW[2]
29	Set DATA1 PID (SetD1PID) Applies to interrupt/bulk IN and OUT endpoints only. Writing to this Bits sets the Endpoint Data PID (DPID) Bits in this register to DATA1. This Bits is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode. Set Odd (micro)frame (SetOddFr) Applies to isochronous IN and OUT endpoints only. Writing to this Bits sets the Even/Odd (micro)frame (EO_FrNum) Bits to odd (micro)frame. This Bits is not applicable for Scatter/Gather DMA mode.	W W
28	Set DATA0 PID (SetD0PID) Applies to interrupt/bulk IN and OUT endpoints only. Writing to this Bits sets the Endpoint Data PID (DPID) Bits in this register to DATA0. This Bits is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode. In non-Scatter/Gather DMA mode: Set Even (micro)frame (SetEvenFr) Applies to isochronous IN and OUT endpoints only. Writing to this Bits sets the Even/Odd (micro)frame (EO_FrNum) Bits to even (micro) frame. When Scatter/Gather DMA mode is enabled, this Bits is reserved. The frame number in which to send data is in the transmit descriptor structure. The frame in which to receive data is updated in receive descriptor structure.	W
27	Set NAK (SNAK) Applies to IN and OUT endpoints. A write to this bit sets the NAK bit for the endpoint. Using this bit, the application can control the transmission of NAK handshakes on an endpoint. The core can also set this bit for OUT endpoints on a Transfer Completed interrupt, or after a SETUP is received on the endpoint.	W

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

26	Clear NAK (CNAK) Applies to IN and OUT endpoints. A write to this bit clears the NAK bit for the endpoint.	W
25:22	TxFIFO Number (TxFNum) *Shared FIFO Operation*—non-periodic endpoints must set this bit to zero. Periodic endpoints must map this to the corresponding Periodic TxFIFO number. 4'h0: Non-Periodic TxFIFO Others: Specified Periodic TxFIFO.number Note: An interrupt IN endpoint can be configured as a non-periodic endpoint for applications such as mass storage. The core treats an IN endpoint as a non-periodic endpoint if the TxFNum Bits is set to 0. Otherwise, a separate periodic FIFO must be allocated for an interrupt IN endpoint, and the number of this FIFO must be programmed into the TxFNum Bits. Configuring an interrupt IN endpoint as a non-periodic endpoint saves the extra periodic FIFO area. *Dedicated FIFO Operation*—these bits specify the FIFO number associated with this endpoint. Each active IN endpoint must be programmed to a separate FIFO number. This Bits is valid only for IN endpoints.	RW
21	STALL Handshake (Stall) Applies to non-control, non-isochronous IN and OUT endpoints only. The application sets this bit to stall all tokens from the USB host to this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Only the application can clear this bit, never the core. Applies to control endpoints only. The application can only set this bit, and the core clears it, when a SETUP token is received for this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake.	RW RW[3]
20	Snoop Mode (Snp) Applies to OUT endpoints only. This bit configures the endpoint to Snoop mode. In Snoop mode, the core does not check the correctness of OUT packets before transferring them to application memory.	RW
19:18	Endpoint Type (EPType) Applies to IN and OUT endpoints. This is the transfer type supported by this logical endpoint. 2'b00: Control 2'b01: Isochronous 2'b10: Bulk 2'b11: Interrupt	RW
17	NAK Status (NAKSts) Applies to IN and OUT endpoints.	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Indicates the following: 1'b0: The core is transmitting non-NAK handshakes based on the FIFO status. 1'b1: The core is transmitting NAK handshakes on this endpoint. When either the application or the core sets this bit: The core stops receiving any data on an OUT endpoint, even if there is space in the RxFIFO to accommodate the incoming packet. For non-isochronous IN endpoints: The core stops transmitting any data on an IN endpoint, even if there data is available in the TxFIFO. For isochronous IN endpoints: The core sends out a zero-length data packet, even if there data is available in the TxFIFO. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake.	
16	Endpoint Data PID (DPID) Applies to interrupt/bulk IN and OUT endpoints only. Contains the PID of the packet to be received or transmitted on this endpoint. The application must program the PID of the first packet to be received or transmitted on this endpoint, after the endpoint is activated. The applications use the SetD1PID and SetD0PID Bitss of this register to program either DATA0 or DATA1 PID. 1'b0: DATA0 1'b1: DATA1 This Bits is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode. Even/Odd (Micro)Frame (EO_FrNum) In non-Scatter/Gather DMA mode: Applies to isochronous IN and OUT endpoints only. Indicates the (micro)frame number in which the core transmits/receives isochronous data for this endpoint. The application must program the even/odd (micro) frame number in which it intends to transmit/receive isochronous data for this endpoint using the SetEvnFr and SetOddFr Bitss in this register. 1'b0: Even (micro)frame 1'b1: Odd (micro)frame When Scatter/Gather DMA mode is enabled, this Bits is reserved. The frame number in which to send data is provided in the transmit descriptor structure. The frame in which data is received is updated in receive descriptor structure.	R
15	USB Active Endpoint (USBActEP) Applies to IN and OUT endpoints. Indicates whether this endpoint is active in the current configuration and interface. The core clears this bit for all endpoints (other than EP 0) after detecting a USB reset. After receiving the SetConfiguration and SetInterface commands, the application must program endpoint registers accordingly and set this bit.	RW[4]
14:11	Next Endpoint (NextEp)	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Applies to non-periodic IN endpoints only. Indicates the endpoint number to be fetched after the data for the current endpoint is fetched. The core can access this Bits, even when the Endpoint Enable (EPEna) bit is low. This Bits is not valid in Slave mode operation. Note: This Bits is valid only for Shared FIFO operations.	
10:0	Maximum Packet Size (MPS) Applies to IN and OUT endpoints. The application must program this Bits with the maximum packet size for the current	RW

Note:[1]~[2]: This bits will operate with Write set , self clear function.

27.6.2.56 Device Endpoint-n Interrupt Register (DIEPINTn/DOEPINTn, 0x908/0xB08+n*0x20)

	DIEPINTn/DOEPINTn																															Base + 0x908/0xB08+n*0x20
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																	NYETIntrpt	NAKIntrpt	BbleErrIntrpt	PktDrpSts	Reserved	BNAIntr	TxfifoUndrn	TxFEmp	INEPNakEff	INTknEPMis	INTknTXFEmp	TimeOUT	AHBErr	EPDisbld	XferCompl
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:15	Reserved	R
14	NYET interrupt (NYETIntrpt) The core generates this interrupt when a NYET response is transmitted for a non isochronous OUT endpoint.	RW[1]
13	NAK interrupt (NAKIntrpt) The core generates this interrupt when a NAK is transmitted. In case of isochronous IN endpoints the interrupt gets generated when a zero length packet is transmitted due to unavailability of data in the TXFifo.	RW[2]
12	BbleErr (Babble Error) interrupt (BbleErrIntrpt) The core generates this interrupt when babble is received for the endpoint.	RW[3]
11	PktDrpSts (Packet Dropped Status) This bit indicates to the application that an ISOC OUT packet has been dropped. This bit does not have an associated mask bit and does not generate an interrupt. **Dependency**: This bit is valid in non Scatter/Gather DMA mode when periodic transfer interrupt feature is selected.	RW[4]
10	Reserved	R
9	BNA (Buffer Not Available) Interrupt (BNAIntr) The core generates this interrupt when the descriptor accessed is not ready for the Core to process, such as Host busy or DMA done.	RW[5]

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Dependency: This bit is valid only when Scatter/Gather DMA mode is enabled.	
8	FIFO Underrun (TxfifoUndrn) Applies to IN endpoints only The core generates this interrupt when it detects a transmit FIFO underrun condition for this endpoint. **Dependency**: This interrupt is valid only when both of the following conditions are true: Parameter OTG_EN_DED_TX_FIFO=1 Thresholding is enabled OUT Packet Error (OutPktErr) Applies to OUT endpoints only This interrupt is asserted when the core detects an overflow or a CRC error for an OUT packet. **Dependency**: This interrupt is valid only when both of the following conditions are true: Parameter OTG_EN_DED_TX_FIFO=1 Thresholding is enabled.	RW[6] RW[7]
7	Transmit FIFO Empty (TxFEmp) This bit is valid only for IN Endpoints This interrupt is asserted when the TxFIFO for this endpoint is either half or completely empty. The half or completely empty status is determined by the TxFIFO Empty Level bit in the Core AHB Configuration register (GAHBCFG.NPTxFEmpLvl)).	R
6	N Endpoint NAK Effective (INEPNakEff) This bit should be cleared by writing a 1'b1 before writing a 1'b1 to corresponding DIEPCTLn.CNAK. The interrupt indicates that the IN endpoint NAK bit set by the application has taken effect in the core. This interrupt does not guarantee that a NAK handshake is sent on the USB. A STALL bit takes priority over a NAK bit. This bit is applicable only when the endpoint is enabled. Back-to-Back SETUP Packets Received (Back2BackSETup) Applies to Control OUT endpoints only. This bit indicates that the core has received more than three back-to-back SETUP packets for this particular endpoint. This bit is not valid in Slave mode.	RW[8] RW[9]
5	IN Token Received with EP Mismatch (INTknEPMis) Applies to non-periodic IN endpoints only. Indicates that the data in the top of the non-periodic TxFIFO belongs to an endpoint other than the one for which the IN token was received. This interrupt is asserted on the endpoint for which the IN token was received. Status Phase Received For Control Write (StsPhseRcvd) This interrupt is valid only	RW[10]

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	for Control OUT endpoints and only in Scatter Gather DMA mode. This interrupt is generated only after the core has transferred all the data that the host has sent during the data phase of a control write transfer, to the system memory buffer. The interrupt indicates to the application that the host has switched from data phase to the status phase of a Control Write transfer. The application can use this interrupt to ACK or STALL the Status phase, after it has decoded the data phase. This is applicable only in case of Scatter Gather DMA mode.	
4	IN Token Received When TxFIFO is Empty (INTknTXFEmp) Indicates that an IN token was received when the associated TxFIFO (periodic/non-periodic) was empty. This interrupt is asserted on the endpoint for which the IN token was received. OUT Token Received When Endpoint Disabled (OUTTknEPdis) Indicates that an OUT token was received when the endpoint was not yet enabled. This interrupt is asserted on the endpoint for which the OUT token was received.	RW[11]
3	Timeout Condition (TimeOUT) In shared TX FIFO mode, applies to non-isochronous IN endpoints only. In dedicated FIFO mode, applies only to Control IN endpoints. In Scatter/Gather DMA mode, the TimeOUT interrupt is not asserted. Indicates that the core has detected a timeout condition on the USB for the last IN token on this endpoint. SETUP Phase Done (SetUp) Applies to control OUT endpoints only. Indicates that the SETUP phase for the control endpoint is complete and no more back-to-back SETUP packets were received for the current control transfer. On this interrupt, the application can decode the received SETUP data packet.	RW[12]
2	AHB Error (AHBErr) Applies to IN and OUT endpoints. This is generated only in Internal DMA mode when there is an AHB error during an AHB read/write. The application can read the corresponding endpoint DMA address register to get the error address.	RW[13]
1	Endpoint Disabled Interrupt (EPDisbld) Applies to IN and OUT endpoints. This bit indicates that the endpoint is disabled per the application's request.	RW[14]
0	Transfer Completed Interrupt (XferCompl) Applies to IN and OUT endpoints. When Scatter/Gather DMA mode is enabled For IN endpoint this Bits indicates that the requested data from the descriptor is moved from external system memory to internal FIFO. For OUT endpoint this Bits indicates that the requested data from the internal FIFO is	RW[15]

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	moved to external system memory. This interrupt is generated only when the corresponding endpoint descriptor is closed, and the IOC bit for the corresponding descriptor is set. When Scatter/Gather DMA mode is disabled, this Bits indicates that the programmed transfer is complete on the AHB as well as on the USB, for this endpoint.	

Note:

[1]~[15]: This bits will operate with Self set , Write clear function.

27.6.2.57 Device Endpoint 0 Transfer Size Register (DIEPTSIZ0/DOEPTSIZ0,0x910/0xB10)

	DIEPTSIZ0/DOEPTSIZ0																															Base + 0x910/0xB10
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved											PktCnt		Reserved												XferSize						
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:21	Reserved	R
20:19	Packet Count (PktCnt) Indicates the total number of USB packets that constitute the Transfer Size amount of data for endpoint 0. This Bits is decremented every time a packet (maximum size or short packet) is read from the TxFIFO.	RW
18:7	Reserved	R
6:0	Transfer Size (XferSize) Indicates the transfer size in bytes for endpoint 0. The core interrupts the application only after it has exhausted the transfer size amount of data. The transfer size can be set to the maximum packet size of the endpoint, to be interrupted at the end of each packet. The core decrements this Bits every time a packet from the external memory is written to the TxFIFO.	RW

27.6.2.58 Device Endpoint-n Transfer Size Register (DIEPTSIZn/DOEPTSIZn, 0x910/0xB10+n*0x20)

	DIEPTSIZn/DOEPTSIZn																															Base + 0x910/0xB10+n*0x20
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Reserved	MC		PktCnt									XferSize																		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31	Reserved	R
30:29	Multi Count (MC) Applies to IN endpoints only. For periodic IN endpoints, this Bits indicates the number of packets that must be transmitted per microframe on the USB. The core uses this Bits to calculate the data PID for isochronous IN endpoints. 2'b01: 1 packet 2'b10: 2 packets 2'b11: 3 packets For non-periodic IN endpoints, this Bits is valid only in Internal DMA mode. It specifies the number of packets the core must fetch for an IN endpoint before it switches to the endpoint pointed to by the Next Endpoint Bits of the Device Endpoint-*n* Control register (DIEPCTLn.NextEp). Received Data PID (RxDPID) Applies to isochronous OUT endpoints only. This is the data PID received in the last packet for this endpoint. 2'b00: DATA0 2'b01: DATA2 2'b10: DATA1 2'b11: MDATA SETUP Packet Count (SUPCnt) Applies to control OUT Endpoints only. This Bits specifies the number of back-to-back SETUP data packets the endpoint can receive. 2'b01: 1 packet 2'b10: 2 packets 2'b11: 3 packets	RW R R RW
28:19	Packet Count (PktCnt) Indicates the total number of USB packets that constitute the Transfer Size amount of data for this endpoint (PktCnt = XferSize / MPS). IN Endpoints: This Bits is decremented every time a packet (maximum size or short	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	packet) is read from the TxFIFO. OUT Endpoints: This Bits is decremented every time a packet (maximum size or short packet) is written to the RxFIFO.	
18:0	Transfer Size (XferSize) This Bits contains the transfer size in bytes for the current endpoint. The transfer size (XferSize) = Sum of buffer sizes across all descriptors in the list for the endpoint. In Buffer DMA, the core only interrupts the application after it has exhausted the transfer size amount of data. The transfer size can be set to the maximum packet size of the endpoint, to be interrupted at the end of each packet. IN Endpoints: The core decrements this Bits every time a packet from the external memory is written to the TxFIFO. OUT Endpoints: The core decrements this Bits every time a packet is read from the RxFIFO and written to the external memory.	RW

27.6.2.59 Device Endpoint-n DMA Address Register (DIEPDMAn/DOEPDMAn, 0x914/0xB14+n*0x20)

	DIEPDMAnDOEPDMAn																															
																	Base + 0x914/0xB14+n*0x20															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DMAAddr																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Description	R/W
31:0	DMA Address (DMAAddr) Holds the start address of the external memory for storing or fetching endpoint data. Note: For control endpoints, this Bits stores control OUT data packets as well as SETUP transaction data packets. When more than three SETUP packets are received back-to-back, the SETUP data packet in the memory is overwritten. This register is incremented on every AHB transaction. The application can give only a DWORD-aligned address. When Scatter/Gather DMA mode is not enabled, the application programs the start address value in this Bits. When Scatter/Gather DMA mode is enabled, this Bits indicates the base pointer for the descriptor list.	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

27.6.2.60 Device Endpoint-n DMA Buffer Address Register (DIEPDMABn/DOEPDMABn, 0x91C/0xB1C+n*0x20)

	DIEPDMABn/DOEPDMABn																															
																	Base + 0x91C/0xB1C+n*0x20															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DMABufferAddr																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Description	R/W
31:0	DMA Buffer Address (DMABufferAddr) Holds the current buffer address.This register is updated as and when the data transfer for the corresponding end point is in progress. This register is present only in Scatter/Gather DMA mode. Otherwise this Bits is reserved.	R

27.6.2.61 Device IN Endpoint Transmit FIFO Status Register (DTXFSTSn,0x918)

	DTXFSTSn																															
																	Base + 0x918															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																INEPTxFSpcAvail															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:16	Reserved.	R
15:0	IN Endpoint TxFIFO Space Avail (INEPTxFSpcAvail) Indicates the amount of free space available in the Endpoint TxFIFO. Values are in terms of 32-bit words. 16'h0: Endpoint TxFIFO is full 16'h1: 1 word available 16'h2: 2 words available 16'hn: n words available (where 0≤n≤32,768) 16'h8000: 32,768 words available Others: Reserved	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

27.6.3 PHY Register Memory Map

Table 27-4 Registers Memory Map Base Address

Name	Base	Description
OTGPHY	0x10078000	Address base of OTGPHY

Table 27-5 OTGPHY Registers Map

Address Offset	RW	Reset Value	Access Size
0x30	RW	0x09	8
0x40	RW	0x49	8
0x44	RW	0x08	8
0x48	RW	0x0E	8
0x60	RW	0x03	8
0x64	RW	0xE0	8
0x68	RW	0xF8	8
0x78	RW	0x00	8
0xA0	RW	0xF0	8
0x100	RW	0x40	8
0x104	RW	0x00	8
0x108	RW	0x00	8
0x10C	RW	0x00	8
0x110	RW	0x00	8
0x114	RW	0x00	8
0x11C	RW	0xB5	8
0x120	RW	0x52	8
0x124	RW	0x00	8

27.6.4 PHY Register and Fields Description

27.6.4.1 PHY Register 0x30

									Base + 0x030
Bit		7	6	5	4	3	2	1	0
		Reserved					EnPrEm		

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

RST		0	0	0	0	1	0	0	1

Bits	Description	R/W
7:3	Reserved.	R
2:0	EnPrEm Enables pre-emphasis under certain circumstances in order to compensate for excessive capacitive loading on D+ / D-. This tends to increase the slew rate. **3'b001**: enable pre-emphasis during SOF and EOP **3'b010**: enable pre-emphasis during chirp **3'b100**: enable pre-emphasis in non-chirp state **3'b111**: always enable pre-emphasis All other combinations are reserved	RW

27.6.4.2 PHY Register 0x40

		Base + 0x040							
Bit		7	6	5	4	3	2	1	0
		Reserved	HBPrEm	TxHSPrEm			Reserved		
RST		0	1	0	0	1	0	0	1

Bits	Description	R/W
7	Reserved	R
6	HBPrEm, half bit pre_emphasize enable, active high	RW
5:3	TxHSPrEm Tx HS pre_emphasize strength config. **3'b111** represents the strongest **3'b000** represents the weakest	RW
2:0	Reserved	R

27.6.4.3 PHY Register 0x44

		Base + 0x044							
Bit		7	6	5	4	3	2	1	0
		RxClkP			Reserved				

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

RST		0	0	0	0	1	0	0	0

Bits	Description	R/W
7:5	RxClkP Manually set the Rx Clock phase select. these bits will tune the HS RX path sample timing between digital and analog inside PHY: **3'b000**:represents the earliest phase **3'b111**:represents the latest phase The delay associated with each step is 256ps	RW
4:0	Reserved	R

27.6.4.4 PHY Register 0x48

		Base + 0x048							
Bit		7	6	5	4	3	2	1	0
		Reserved					TxClkP		
RST		0	0	0	0	1	1	1	0

Bits	Description	R/W
7:3	Reserved	R
2:0	TxClkP Manually set the Tx Clock phase select. These bits will tune the HS TX path sample timing between digital and analog inside PHY: **3'b000** represents the earliest phase **3'b111** represents the latest phase The delay associated with each step is 256ps	RW

27.6.4.5 PHY Register 0x60

		Base + 0x060							
Bit		7	6	5	4	3	2	1	0
		Reserved						HsDisDeTri	
RST		0	0	0	0	0	0	1	1

Bits	Description	R/W

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

7:2	Reserved	R
1:0	HsDisDeTri[3:2] HsDisDeTri[3:0] is {0x60[1:0], 0x68[0], 0x64[7]} HOST disconnects detection trigger point. Only valid in host mode. Allows compensation for package and board level parasitic which tend to drop in the input voltage. All other combinations reserved 4’b0000: 625mV 4’b0001: 675mV 4’b0010: 612.5mV 4’b0011: 575mV 4’b0100: 550mV 4’b0101: 600mV 4’b0110: 537.5mV 4’b0111: 500mV 4’b1000: 600mV 4’b1001: 650mV 4’b1010: 587.5mV 4’b1011: 550mV 4’b1100: 575mV 4’b1101: 625mV(default) 4’b1110: 562.5mV 4’b1111: 525mV	RW

27.6.4.6 PHY Register 0x64

		Base + 0x064							
Bit	7	6	5	4	3	2	1	0	
	HsDisDeTri	RxSqTri				Reserved			
RST	1	1	1	0	0	0	0	0	

Bits	**Description**	**R/W**
7	HsDisDeTri[0] HsDisDeTri[3:0] is {0x60[1:0], 0x68[0], 0x64[7]} Detail reference 0x60[1:0]	RW
6:3	RxSqTri Rx squelch trigger point configures. Allows tuning of the squelch trigger point in order to compensate for package and board level parasitic. 4b’0000 : 112.5mv 4b’0001 : 150mv	

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	4b'0010 : 87.5mv 4b'0011 : 162.5mv 4b'0100 : 100mv 4b'0101 : 137.5mv 4b'0110 : 75mv 4b'0111 : 150mv 4b'1000 : 125mv 4b'1001 : 162.5mv 4b'1010 : 100mv 4b'1011 : 175mv 4b'1100 : 150mv(default) 4b'1101 : 187.5mv 4b'1110 : 125mv 4b'1111 : 200mv	
2:0	Reserved	R

27.6.4.7 PHY Register 0x68

									Base + 0x068
Bit	7	6	5	4	3	2	1	0	
	Reserved							HsDisDeTri	
RST	1	1	1	1	1	0	0	0	

Bits	Description	R/W
7:1	Reserved	R
0	HsDisDeTri[1] HsDisDeTri[3:0] is {0x60[1:0], 0x68[0], 0x64[7]} Detail reference 0x60[1:0]	RW

27.6.4.8 PHY Register 0x78

									Base + 0x078
Bit	7	6	5	4	3	2	1	0	
	Reserved		IOHighZ	Reserved					
RST	0	0	0	0	0	0	0	0	

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Description	R/W
7:6	Reserved	R
5	IOHighZ set IO high Z state , active high	RW
4:0	Reserved	R

27.6.4.9 PHY Register 0xA0

									Base + 0x0A0
Bit	7	6	5	4	3	2	1	0	
	Reserved				BgOutVol		Reserved		
RST	1	1	1	1	0	0	0	0	

Bits	Description	R/W
7:4	Reserved	R
3:2	BgOutVol BG output reference voltage adjust. It can control the whole output reference voltage and current of bg.	RW
1:0	Reserved	R

27.6.4.10 PHY Register 0x100

									Base + 0x100
Bit	7	6	5	4	3	2	1	0	
	Reserved		PLLfb	DcpDetected	CpDetected	Reserved		DpAttached	
RST	0	1	0	0	0	0	0	0	

Bits	Description	R/W
7:6	Reserved	R
5	PLLfb PLL feedback divider ratio option	R
4	DcpDetected Dedicated Charging Port detected successfully	R
3	CpDetected	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Charging Port detected successfully (Dedicated Charging Port or Charging Downstream Port)	
2:1	Reserved	R
0	DpAttached assert DP pin connect successfully	R

27.6.4.11 PHY Register 0x104

									Base + 0x104
Bit	7	6	5	4	3	2	1	0	
	IdmSink	IdpSrc	Rdmpdwn	VdpSrc	IdpSink	VdmSrc	ousbplldecn	ousbpllincz	
RST	0	0	0	0	0	0	0	0	

Bits	Description	R/W
7	uda_Idm_sink_en	RW
6	uda_Idp_src_en	RW
5	uda_Rdm_pdwn_en	RW
4	uda_vdp_src_en	RW
3	uda_Idp_sink_en	RW
2	uda_vdm_src_en	RW
1	uda_ousbplldecn	RW
0	uda_ousbpllincz	RW

27.6.4.12 PHY Register 0x108

									Base + 0x108
Bit	7	6	5	4	3	2	1	0	
	Reserved			ChirpBypass	VbusDetPd	VbusValid	Reserved		
RST	0	0	0	0	0	0	0	0	

Bits	Description	R/W
7:5	Reserved	R
4	ChirpBypass bypass squelch trigger point configure in chirp modes , active high	RW
3	VbusDetPd	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	vbus voltage level detection function power down, active high	
2	VbusValid force output vbus_valid asserted, active high	RW
1:0	Reserved	R

27.6.4.13 PHY Register 0x10C

									Base + 0x10C
Bit	7	6	5	4	3	2	1	0	
	ForceBse	ForceAse	BseRefTune			AseRefTune			
RST	0	0	0	0	0	0	0	0	

Bits	Description	R/W
7	ForceBse force output B_sessionvalid asserted, active high	RW
6	ForceAse force output A_sessionvalid asserted, active high	RW
5:3	BseRefTune B_sessionvalid reference tuning	RW
2:0	AseRefTune A_sessionvalid reference tuning	RW

27.6.4.14 PHY Register 0x110

									Base + 0x110
Bit	7	6	5	4	3	2	1	0	
	Reserved	ForceSeEnd	VbusRefTune			SeEndTune			
RST	0	0	0	0	0	0	0	0	

Bits	Description	R/W
7	Reserved	R
6	ForceSeEnd force output session_end asserted, active high	RW
5:3	VbusRefTune vbus_valid reference tuning	RW
2:0	SeEndTune	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	session_end reference tuning	

27.6.4.15 PHY Register 0x114

									Base + 0x114
Bit	7	6	5	4	3	2	1	0	
	Reserved							BalClockEn	
RST	0	0	0	0	0	0	0	0	

Bits	Description	R/W
7:1	Reserved	R
0	BalClockEn clk12m, clk48m, clk60m enable signal ,active high	RW

27.6.4.16 PHY Register 0x11C

									Base + 0x11C
Bit	7	6	5	4	3	2	1	0	
	HSRecvBias	DisDetBias		ODTTune					
RST	1	0	1	1	0	1	0	1	

Bits	Description	R/W
7	HSRecvBias HS receiver bias current tunning register	RW
6:5	DisDetBias disconnect detector bias current tunning register	RW
4:0	ODTTune 45ohm HS ODT value tuning & FS/LS driver strength tuning 5’b11111: smallest HS ODT value & largest FS/LS driver strength and fastest FS/LS slew rate 5’b10000: biggest HS ODT value & smallest FS/LS driver strength and slowest FS/LS slew rate	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

27.6.4.17 PHY Register 0x120

									Base + 0x120
Bit	7	6	5	4	3	2	1	0	
	Reserved		HSDriSlew			SqDetBias		HSTransDig	
RST	0	1	0	1	0	0	1	0	

Bits	Description	R/W
7:6	Reserved	R
5:3	HSDriSlew HS driver slew rate tunning	RW
2:1	SqDetBias Squelch detector bias current tunning register	RW
0	HSTransDig HS receiver can receive HS data and transmit it to digital.	RW

27.6.4.18 PHY Register 0x124

									Base + 0x124
Bit	7	6	5	4	3	2	1	0	
	Reserved			HSEyeTune			Reserved		
RST	0	0	0	0	0	0	0	0	

Bits	Description	R/W
7:5	Reserved	R
5:3	HSEyeTune HS eye height tuning **3'b000**: 400mv(default) **3'b001**: 475mv **3'b010**: 350mv **3'b011**: 500mv **3'b100**: 412.5mv **3'b101**: 425mv **3'b110**: 437.5mv **3'b111**: 450mv	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

1:0	Reserved	R

27.7 PHY VBUS attention

PHY VBUS port support 5V connections and 0.6 voltage divided connections. If use 5V connections , the voltage-comparator mode need to set 5V mode.

Table 27-6 PHY VBUS compare mode

Voltage mode	PHY Registers	Register Value
5V mode	0x10C.BseRefTune	0x5
	0x10C.AseRefTune	0x5
	0x110.VbusRefTune	0x5
	0x110.SeEndTune	0x5
0.6 voltage divided mode(**default**)	0x10C.BseRefTune	0x0
	0x10C.AseRefTune	0x0
	0x110.VbusRefTune	0x0
	0x110.SeEndTune	0x0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

28 SC_HASH HDL

28.1 Overview

- HASH digest algorithm
- HASH engine: SHA and MD5
- SHA1 fully referring to *RFC-3174* standard
- MD5 fully referring to *RFC-1321* standard

28.2 Feature

- AHB2 slave interface;
- AHB2 master interface;
- SHA core: support SHA 160/224/256/384/512bit digest;

Name	Vertion	Input Data Lenth	Output Data Lenth	Cycle	BPS
SHA1	160	512*n	160	88	73Mbyte/ (200MHz)
SHA2	224	512*n	224	64	
	256	512*n	256	64	
	384	1024*n	384	97	
	512	1024*n	512	97	
MD5		512*n	128	79	81Mbyte/ (200MHz)

28.3 Registers

Following chapter will descript the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. Register read/write attribute

   R - Read only

   W - Write only

   RW - read and write

   RCW - read and write, but clear to 0 by read

   RSW - read and write, but set to 1 by read

   RWC - read and write, clear to 0 by write 1, write 0 has no effect

   RWS - read and write, set to 1 by write 1, write 0 has no effect

   RC - read only, and clears to 0 by read

   RS - read only, and set to 1 by read

   SPEC - special access method, relate to its description

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

3. Reset Value

1 - Reset to 1

0 - reset to 0

? - Value unknown after reset

28.3.1 Register Memory Map

Table 28-1 Registers Memory Map-Address Base

Name	Base	Description
HASH	0x13470000	HASH registers memory map address

Table 28-2 HASH registers description

Name	Description	Reset Value	Address offset	Access Size
HSCR	HASH control register	0x30000000	0x0000	32
HSSR	HASH status register	0x00000000	0x0004	32
HSINTM	HASH interrupt mask register	0x00000000	0x0008	32
HSSA	HASH DMA source address	0x00000000	0x000c	32
HSTC	HASH DMA transfer count	0x00000000	0x0010	32
HSDI	HASH data input	0x00000000	0x0014	32
HSDO	HASH data output	0x00000000	0x0018	32

28.3.2 Hash Ctrl Register (HSCR)

	HSCR																															BASE+0x0000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PS				Reserved																			DORVS	DIRVS	DMAS	DMAE	INIT	SEL			EN
RST	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:28	PS	Page Size, don't set these bits, and keep them default value. 0: don't care 1: 1 KB 2: 2 KB 3: 4 KB(default) 4: 8 KB 5: 16 KB	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

27:7	Reserved	Writing has no effect, read as zero.	R
8	DORVS	**Data output reveres**: big-end <> little-end If output data is odata[31:0] 0: the result is odata[31:0]; 1:the result is {odata[7:0],odata[15:8],odata[23:16],odata[31:24]}; In MD5 mode, this bit should set to 1 before data input.	WR
7	DIRVS	**Data input reveres**: big-end ~ little-end If input data is idata[31:0] 0: the result is idata[31:0]; 1:the result is {idata[7:0],idata[15:8],idata[23:16],idata[31:24]}; In SHA mode, this bit should be set to 1 before data input.	WR
6	DMAS	**DMA Start** This bit is cleared automatically by hardware and always read as 0.	RWS
5	DMAE	**DMA Enable**	WR
4	INIT	**Initial module for a New Round:** HASH Process Initial. This bit is cleared automatically by hardware and always read as 0. **NOTE:** ONLY a new round of hash begin this bit may set to 1.	RWS
3:1	SEL	**Hash Algorithm Selection :** 000: MD5 001: SHA1 010: SHA224 011: SHA256 100: SHA384 101: SHA512 110: Reserved 111: Reserved	WR
0	EN	**Hash Enable:** 1: Hash Enable 0: Hash Disable	WR

28.3.3 Hash Status Register (HSSR)

	HSCR																															BASE+0x0004	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														MRD	ORD
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:2	Reserved	Writing has no effect, read as zero.	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

1	MRD	**Multi Hash Round Done: the HSDO is valid** MRD ONLY for DMA read access done ; Set 1 to clear	RWC
0	ORD	**ONE Hash Round Done: the HSDO is valid** ORD for CPU read access done as usual ; Set 1 to clear	RWC

28.3.4 Hash Interrupt Mask Register (HSINTM)

	HSCR																															BASE+0x0008
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														MR_INT_M	OR_INT_M
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:2	Reserved	Writing has no effect, read as zero.	R
1	MR_INT_M	**MRD Interrupt Mask** 1: Interrupt Enable 0: Interrupt Mask(default)	WR
0	OR_INT_M	**ORD Interrupt Mask** 1: Interrupt Enable 0: Interrupt Mask(default)	WR

28.3.5 Hash DMA Source Address (HSSA)

	HSSA																															BASE+0x000C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SA																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	SA	**Source physical address for DMA use.**	WR

28.3.6 Hash Transfer Count (HSTC)

	HSTC																															BASE+0x0010
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	TC																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	TC	**Transfer Count:** Number of Blocks(**1Block == 512bit**)	WR

28.3.7 Hash Data Input Register (HSDI)

	HSDI																															BASE+0x0014
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DIN																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DIN	**Data Input:** Only support Word write	W

28.3.8 Hash Data Output Register (HSDO)

	HSDO																															BASE+0x0018
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DOUT																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DOUT	Data Output : Only support word read MD5: 128bit SHA1:160bit SHA224:224bit SHA256:256bit SHA384:384bit SHA512:512bit	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

28.4 Software User Guide

28.4.1 HASH running flow

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

28.4.2 Example of MD5

MD5("abc") = 0x900150983cd24fb0d6963f7d28e17f72;

MD5 ("") = d41d8cd98f00b204e9800998ecf8427e

MD5 ("a") = 0cc175b9c0f1b6a831c399e269772661

MD5 ("abc") = 900150983cd24fb0d6963f7d28e17f72

MD5 ("message digest") = f96b697d7cb7938d525a2f31aaf161d0

MD5 ("abcdefghijklmnopqrstuvwxyz") = c3fcd3d76192e4007dfb496cca67e13b

MD5 ("ABCDEFGHIJKLMNOPQRSTUVWXYZabcdefghijklmnopqrstuvwxyz0123456789")
=
d174ab98d277d9f5a5611c2c9f419d9f

MD5 ("12345678901234567890123456789012345678901234567890123456789012345678901234567890") = 57edf4a22be3c955ac49da2e2107b67a

use Linux command md5sum。

```
> md5sum -t file.txt
Note: if the original text is "abc" the actual text is "abc<LF>";
<LF> = 0x0a;
```


Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

file.txt

abc

28.4.3 Example of SHA1

SHA1("abc") = a9993e36 47068 16a ba3e2571 7850c26c 9cd0d89d

SHA1("abcdbcdecdefdefgefghfghighijhijkijkljklmklmnlmnomnopnopq") = 84983e44 1c3bd26e baae4aa1 f95129e5 e54670f1

SHA1 consists of 1,000,000 repetitions of the character " a " = 34aa973c d4c4daa4 f61eeb2b dbad2731 6534016f

28.4.4 Test Vectors

SHA1

Text: "abc"

Input: 80636261 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 18000000

output: a9993e36 4706816a ba3e2571 7850c26c 9cd0d89d

MD5

Text: "abc"

Input: 80636261 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000018 00000000

output: 90015098 3cd24fb0 d6963f7d 28e17f72

28.5 AHB Interface

28.5.1 AHB Slave Interface

System Signal			
Port Name	**IO**	**Width**	**Note**
clk	Input	1	Clock input
rst_n	Intput	1	Reset, active low
For Internal Module			
Port Name	**IO**	**Width**	**Note**
wr	output	1	Ahb bus write enable for internal module
wr_addr	output	5	Ahb bus write addr for internal module
wr_dat	output	32	Write 32bit data to internal module
rd	output	1	Ahb bus read enable for internal module

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

rd_addr	output	5	Ahb bus read addr for internal module
rd_data	input	32	Read 32bit data from internal module
For AHB Slave Interface			
Port Name	**IO**	**Width**	**Note**
haddr	input	32	
htran	input	2	
hwrite	input	1	
hburst	input	3	Single access ONLY
hsize	input	3	Word access ONLY
hsel	input	1	
hwdata	input	32	
hready	input	1	
hready_local	output	1	
hresp_local	output	2	MUST be AHB_OKAY = 2'b00
hrdata_local	output	32	

28.5.2 AHB Master Interface

System Signal			
Port Name	**IO**	**Width**	**Note**
clk	Input	1	Clock input
rst_n	Input	1	Reset, active low
For Internal Module			
Port Name	**IO**	**Width**	**Note**
start	Input	1	Start signal
done	output	1	Current access done
wr_rd	input	1	1: write data 0: read data
cmd	Input	2	Number of Words 00:INCR4 01:INCR16 10:INCR16x2

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

mas_wr_req	output	1	Master read data valid, combination logic output
mas_wr_dat	input	32	Master trans 32bit internal data to AHB, register input
mas_rd_req	output	1	Master read data valid, register output
mas_rd_dat	output	32	Master read 32bit data, and trans to internal module, register output
For AHB Master Interface			
Port Name	**IO**	**Width**	**Note**
haddr	Output	10	
htran	Output	2	
hwrite	Output	1	
hburst	Output	3	Support INCR4,INCR16
hsize	Output	3	Word access ONLY
hsel	Output	1	
hwdata	Output	32	
hready	Input	1	

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

29 AES

29.1 Overview

- AES: Advanced Encryption Standard
- Fully referring to *Rijdael_fips_197* standard
- AES Engine: AES-128/192/256
- 128/192/256 bits key for AES Encryption and Decryption supported
- ECB and CBC mode supported
- Internal DMA mode supported
- Clear bit supported to clear keys, data and IV for security concern

29.2 AES engine

- 128 bits data for Encryption and Decryption
- 128/192/256 bits Key
- 128 bits IV (initial vector) for CBC mode
- ECB and CBC mode

Figure 29-1 ECB mode encoding

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Figure 29-2 ECB mode decoding

Figure 29-3 CBC mode encoding

Figure 29-4 CBC mode decoding

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

29.3 Registers

Following chapter will descript the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. Register read/write attribute
   R - Read only
   W - Write only
   RW - read and write
   RCW - read and write, but clear to 0 by read
   RSW - read and write, but set to 1 by read
   RWC - read and write, clear to 0 by write 1, write 0 has no effect
   RWS - read and write, set to 1 by write 1, write 0 has no effect
   RC - read only, and clears to 0 by read
   RS - read only, and set to 1 by read
   SPEC - special access method, relate to its description
3. Reset Value
   1 - Reset to 1
   0 - reset to 0
   ? - Value unknown after reset

29.3.1 Register Memory Map

Table 29-1 Registers Memory Map-Address Base

Name	Base	Description
AES	0x13430000	AES registers memory map address

Table 29-2 AES registers description

Name	Description	Reset Value	Address offset	Access Size
ASCR	AES control register	0x30000000	0x0000	32
ASSR	AES status register	0x00000000	0x0004	32
ASINTM	AES interrupt mask register	0x00000000	0x0008	32
ASSA	AES DMA source address	0x00000000	0x000c	32
ASDA	AES DMA destine address	0x00000000	0x0010	32
ASTC	AES DMA transfer count	0x00000000	0x0014	32
ASDI	AES data input	0x00000000	0x0018	32
ASDO	AES data output	0x00000000	0x001c	32
ASKY	AES key input	0x00000000	0x0020	32
ASIV	AES IV input	0x00000000	0x0024	32

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

29.3.2 AES Control Register (ASCR)

	ASCR																															BASE+0x0000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PS				RESERVED																ENDIAN	CLR	DMAS	DMAE	KEYL		MODE	DECE	AESS	KEYS	INIT_IV	EN
RST	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:28	PS	Page Size, don't set these bits, and keep them default value. 0: don't care 1: 1 KB 2: 2 KB 3: 4 KB(default) 4: 8 KB 5: 16 KB	RW
27:12	Reserved	Writes to these bits have no effect and always read as 0.	R
11	ENDIAN	0: little-endian data input 1: big-endian data input	RW
10	CLR	Clear the IV & KEYs: This bit MUST be set by two reasons : (1)After CBC mode decoding; (2)Clear IV/KEYs/Input Data/Output Data for security concern ;	RWS
9	DMAS	DMA Start	RWS
8	DMAE	DMA Enable	RW
7:6	KEYL	Selects the key size mode according to the following list: • 2'b00 value selects 128 bit key length, • 2'b01 value selects 192 bit key length, • 2'b10 value selects 256 bit key length This value should not change during operation of the core unless the key mode is changed and key expansion is restarted.	RW
5	MODE	AES mode select bit 0: ECB mode selected 1: CBC mode selected	RW
4	DECE	AES encrypts/decrypts select bit 0: Encrypts input data 1: Decrypts input data	RW
3	AESS	AES Start ONLY valid when DMAE==0, Means a round of AES process start. After ASIV and ASDI write, set AESS by software.	RWS
2	KEYS	Key Expansion Start: Key expansion start command.	RWS

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

1	INIT_IV	AES IV Initial After a new ASIV be written, INIT MUST be set by software to indicate a new round of CBC mode process will be start.	RWS
0	EN	AES enable 0: Disable AES 1: Enable AES	WR

29.3.3 AES Status Register (ASSR)

	ASSR																															BASE+0x0004
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																													DMAD	AESD	KEYD
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:3	Reserved	Writing has no effect, read as zero.	R
2	DMAD	**1: DMA mode encryption/decryption done** **0: DMA mode encryption/decryption not done** Set 1 to clear after reading this bit, writing 0 has no effect	RWC
1	AESD	**1: CPU mode encryption/decryption Done** **0: CPU mode encryption/decryption not done** Set 1 to clear after reading this bit, writing 0 has no effect	RWC
0	KEYD	**1: Key Expansion done** **0: Key Expansion not done** Set 1 to clear after reading this bit, writing 0 has no effect	RWC

29.3.4 AES Interrupt Mask Register (ASINTM)

	ASINTM																															BASE+0x0008
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																													DMA_INT_M	AES_INT_M	KEY_INT_M
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:3	Reserved	Writing has no effect, read as zero.	R
2	DMA_INT_M	**DMA Done Interrupt Mask** 1: Interrupt Enable	WR

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		0: Interrupt Mask(default)	
1	AES_INT_M	**AES Done Interrupt Mask** 1: Interrupt Enable 0: Interrupt Mask(default)	WR
0	KEY_INT_M	**KEY Expansion Done Interrupt Mask** 1: Interrupt Enable 0: Interrupt Mask(default)	WR

29.3.5 AES DMA Source Address (ASSA)

	ASSA																															BASE+0x000c
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SA																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	SA	**Source physical address for DMA mode**	WR

29.3.6 AES DMA Destination Address (ASDA)

	ASDA																															BASE+0x0010
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DA																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DA	**Destination Physical Address for DMA mode**	WR

29.3.7 AES Transfer Count (ASTC)

	ASTC																															BASE+0x0014
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TC																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:0	TC	**Transfer Count:** Number of Blocks(**1Block == 128bit**)	WR

29.3.8 AES Data Input Register (ASDI)

	ASDI																															BASE+0x0018
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DIN																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DIN	**Data Input:** Only support Word write The minimum data unit of AES algorithms is 128-bit. Software should ensure that the number of data to process is **n*128** (bit). The write data flow is {DIN_1st, DIN_2ed, DIN_3rd, DIN_4th}; ASDI can ONLY be acceded by word-write.	W

29.3.9 AES Data Output Register (ASDO)

	ASDO																															BASE+0x001C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DOUT																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DOUT	**Data Output FIFO** The minimum data unit of AES algorithms is 128-bit. Software should ensure that the number of data to process is **n*128** (bit). The read data flow is { DOUT_1st, DOUT_2ed, DOUT_3rd , DOUT_4th}; DOUT can **ONLY** be acceded by word-read, writing has no effect.	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

29.3.10 AES KEY FIFO (ASKY)

	ASKY																															BASE+0x0020
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ASKY																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	ASKY	AES Key register The key(AES128) data flow is { KEY_1st, KEY_2ed, KEY_3rd , KEY_4th }; The key(AES192) data flow is { KEY_1st, KEY_2ed, KEY_3rd , KEY_4th, KEY_5th, KEY_6th }; The key(AES256) data flow is { KEY_1st, KEY_2ed, KEY_3rd , KEY_4th, KEY_5th, KEY_6th, KEY_7th, KEY_8th }; ASKY can **ONLY** be acceded by word-write, read as 0	W

29.3.11 AES IV FIFO (ASIV)

	ASIV																															BASE+0x0024
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ASIV																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	ASIV	Initial Vector register The IV data flow is { IV_1st, IV_2ed, IV_3rd, IV_4th }; ASIV can **ONLY** be acceded by word-write, read as 0	W

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

29.4 Software User Guide

Running flow:

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Example for software

Test Vectors:

128bit Key: 0x2b7e1516 28aed2a6 abf71588 09cf4f3c

IV: NULL

Data Input: 0x3243f6a8 885a308d 313198a2 e0370734

Encoding Output: 0x3925841d 02dc09fb dc118597 196a0b32

128bit Key: 0x2b7e1516 28aed2a6 abf71588 09cf4f3c

IV: 0x00010203 04050607 08090a0b 0c0d0e0f

Data Input: 0x6bc1bee2 2e409f96 e93d7e11 7393172a

Encoding Output: 0x7649abac 8119b246 cee98e9b 12e9197d

192bit Key: 0x00010203 04050607 08090a0b 0c0d0e0f 10111213 14151617

IV: NULL

Data Input: 0x00112233 44556677 8899aabb ccddeeff

Encoding Output: 0xdda97ca4 864cdfe0 6eaf70a0 0ec07191

256bit Key: 0x00010203 04050607 08090a0b 0c0d0e0f 10111213 14151617
18191a1b 1c1d1e1f

IV: NULL

Data Input: 0x00112233 44556677 8899aabb ccddeeff

Encoding Output: 0x8ea2b7ca 516745bf eafc4990 4b496089

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

30 Digital True Random Number Generator （DTRNG）

30.1 Overview

DTRNG(Digital True Random Number Generator) is used to provide true random number encryption seed for system.

30.2 Features

- Pure digital logic circuits
- True random number
- APB bus configure Register
- Interrupt mode and no interrupt mode

30.3 Block Diagram

Figure 30-1 DTRNG Block Diagram

30.4 Register Description

Following chapter will describe the functions of all software accessible registers.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Conventions:

1. Register Address = Base + Address offset
2. Register read/write attribute
   - R- Read only
   - W- Write only
   - RW- Read and Write
   - RCW- Read and Write, but Clear to 0 by Read
   - RSW- Read and Write, but Set to 1 by Read
   - RWC- Read and Write, Clear to 0 by Write 1, Write 0 has no effect
   - RWS- Read and Write, Set to 1 by Write 1, Write 0 has no effect
   - RC- Read only, and Clear to 0 by read
   - RS- Read only, and Set to 1 by read
3. Reset Value
   - 1 - reset to 1
   - 0 - reset to 0
   - ? - value unknown after reset

30.4.1 Register Memory Map

Table 30-1 Registers Memory Map Base Address

Name	Base	Description
DTRNG	0x10072000	DTRNG

Table 30-2 DTRNG Registers Map

Name	RW	Reset Value	Address Offset	Access Size
DTRNG_CFG	RW	0x03FF0800	0x00	32
DTRNG_RANDOMNUM	RW	0x00000000	0x04	32
DTRNG_STAT	RW	0x00000000	0x08	32

30.4.2 Register and Fields Description

30.4.2.1 DTRNG CONFIG Register（DTRNG_CFG,0x00）

	DTRNG_CFG																															0x0000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved						line9_en	line8_en	line7_en	line6_en	line5_en	line4_en	line3_en	line2_en	line1_en	line0_en	Reserved			rdy_clr	int_mask	div_num										gen_en
RST	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:26	Reserved	Writing has no effect. Read as zero.	R
25	line9_en	The enable of inverter9 1:enable the inverter 0: Disable the inverter	RW
24	line8_en	The enable of inverter8 1:enable the inverter 0: Disable the inverter	RW
23	line7_en	The enable of inverter7 1:enable the inverter 0: Disable the inverter	RW
22	line6_en	The enable of inverter6 1:enable the inverter 0: Disable the inverter	RW
21	line5_en	The enable of inverter5 1:enable the inverter 0: Disable the inverter	RW
20	line4_en	The enable of inverter4 1:enable the inverter 0: Disable the inverter	RW
19	line3_en	The enable of inverter3 1:enable the inverter 0: Disable the inverter	RW
18	line2_en	The enable of inverter2 1:enable the inverter 0: Disable the inverter	RW
17	line1_en	The enable of inverter1 1:enable the inverter 0: Disable the inverter	RW
16	line0_en	The enable of inverter0 1:enable the inverter 0:Disable the inverter	RW
15:13	Reserved	Writing has no effect. Read as zero.	R
12	rdy_clr	Ready clear signal: 1.Clear the interrupt 0.Normal work	RW
11	int_mask	The DTRNG interupt mask signal 1:mask the interupt 0:not mask the interupt	RW
10:1	div_num	The divder of pclk	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		The f(clk)=f(pclk)/(div_num+1) ;	
0	gen_en	The enable signal of DTRNG 1:enable the DTRNG 0:disable the DTRNG	RW

30.4.2.2 DTRNG RANDOM NUMBER REGISTER(DTRNG_RANDOMNUM,0x04)

	DTRNG_RANDOMNUM																															0x0004
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	random_num																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	random_num	The random from DTRNG	R

30.4.2.3 DTRNG STATUS REGISTER(DTRNG_STAT,0x08)

	DTRNG_STAT																															0x0008
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															random_rdy
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect. Read as zero.	R
0	random_rdy	The random data generate ready signal When READ: 1.The random data generate ready; 0. No random data generate ready;	R

30.5 Operation Flow

Interrupt mode:

1.configure DTRNG_CFG.div_num, the f(dtrng_clk) = f(pclk)/(1+div_num);

2.Enable the DTRNG, configure DTRNG_CFG.gen_en to ‘1’ ;

3.Wait interupt;

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

4.Read the random data from DTRNG_RANDOMNUM register
5.Clear the interupt, set DTRNG_CFG.rdy_clr to‘1’, then clear DTRNG_CFG.rdy_clr to‘0’;

Cpu mode:

1.configure DTRNG_CFG.div_num, the f(dtrng_clk) = f(pclk)/(1+div_num);
2.Enable the DTRNG, configure DTRNG_CFG.gen_en to‘1’;
3.Read DTRNG_STAT.random_rdy until DTRNG_STAT.random_rdy is '1'
4.Read the random data from DTRNG_RANDOMNUM register
5.Clear the ramdom_rdy, set DTRNG_CFG.rdy_clr to‘1’, the clear DTRNG_CFG.rdy_clr to ‘0’.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

31 Fast Ethernet Media Access Controller (MAC)

31.1 Overview

The processor contains one Fast Ethernet media access controller (MAC), each capable of supporting 10/100Mbps Ethernet. The MAC provides the interface between the host application and the PHY layer through RMII(Reduced Medium Independent Interface). The PHY layer device is external to the processor.

31.2 Features

- 10, 100Mbps data transfer rates with the following PHY interfaces:
  - RMII interface to communicate with an external Fast Ethernet PHY
- Full-duplex operation:
  - IEEE 802.3x flow control automatic transmission of zero-quanta Pause frame on flow control input de-assertion
  - forwarding of received Pause frames to the user application
- Half-duplex operation:
  - CSMA/CD Protocol support
  - Frame bursting and frame extension in 100 Mbps half-duplex operation
- Preamble and start of frame data (SFD) insertion in Transmit path
- Preamble and SFD deletion in the Receive path
- Automatic CRC and pad generation controllable on a per-frame basis
- Automatic Pad and CRC Stripping options for receive frames
- Flexible address filtering modes, such as:
  - Up to 31 additional 48-bit perfect (DA) address filters with masks for each byte
  - 64-bit Hash filter for multicast and unicast (DA) addresses
  - Option to pass all multicast addressed frames
  - Promiscuous mode to pass all frames without any filtering for network monitoring
  - Pass all incoming packets (as per filter) with a status report
- Support Standard or Jumbo Ethernet frames with up to 2 KB of size
- IEEE 802.1Q VLAN tag detection for reception frames
- MDIO master interface for PHY device configuration and management
- CRC replacement, Source Address field insertion or replacement, and VLAN insertion, replacement, and deletion in transmitted frames with per-frame control
- Programmable watchdog timeout limit in the receive path
- Detect remote wake-up frames and AMD magic packets

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

31.3 Block Diagram

Figure 31-1 GMAC Block Diagram

31.4 Functional Description

The MAC enables a host to transmit and receive data over Ethernet in compliance with the IEEE 802.3-2008 standard. The MAC is a configurable product that can be optimized for gate count and latency to meet the application requirements. You can use the MAC in number of applications such as switches and network interface cards.

31.5 Pins Description

Table 31-1 GMAC pin description

Pin	I/O	Description
PHY_CLK	Output	External PHY clock Function: The PHY_CLK is provide for External GMAC PHY, and the frequency is 50MHz
REF_CLK	Input	RMII reference clock. The frequency is 50MHz whenever at 100-Mbps or at 10-Mbps
RX_DV	Input	PHY Receive Data Valid Function: This signal is driven by PHY and has multiple functions depending on which PHY interface is selected: RMII: Contains the crs and data valid information of the receive interface. Synchronous to: REF_CLK
RXD [1:0]	Input	PHY Receive Data Function: This is a bundle of two data signals

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		received from the PHY: RMII: Bits [1:0] provide the RMII receive data. The validity of the data is qualified with phy_rxdv_o. Synchronous to: REF_CLK
TX_EN	Output	PHY Transmit Data Enable Function: This signal is driven by the MAC and has multiple functions depending on which PHY interface is selected: RMII: When high, indicates that valid data is being transmitted on the phy_txd bus. Synchronous to: REF_CLK
TXD [1:0]	Output	PHY Transmit Data Function: This is a group of two transmit data signals driven by the MAC. RMII: Bits [1:0] provide the RMII transmit data. The validity of the data is qualified with phy_txen_o. Synchronous to: REF_CLK
MDC	Output	Management Data Clock Function: The maximum frequency of this clock is 2.5 MHz. This clock is generated from the GMAC HCLK through a clock divider.
MDIO	I/O	MDIO is the bidirectional data signal between the MAC and the PHY that is clocked by MDC.

31.6 Data Format Description

For RMII mode , the data width is 2bits.

31.7 Register Description

Following chapter will describe the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. Register read/write attribute
   R- Read only
   W- Write only
   RW- Read and Write
   RCW- Read and Write, but Clear to 0 by Read
   RSW- Read and Write, but Set to 1 by Read
   RWC- Read and Write, Clear to 0 by Write 1, Write 0 has no effect
   RWS- Read and Write, Set to 1 by Write 1, Write 0 has no effect
   RC- Read only, and Clear to 0 by read
   RS- Read only, and Set to 1 by read
3. Reset Value
   1 - reset to 1

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

0 - reset to 0

? - value unknown after reset

31.7.1 Register Memory Map

Table 31-2 Registers Memory Map Base Address

Name	Base	Description
GMAC	0x134B0000	Address base of GMAC

The GMAC is controlled by a set of registers that the application configures before every operation. The following table lists all the registers.

Table 31-3 GMAC Registers Map

Name	RW	Reset Value	Address Offset	Access Size
DMA_BMR	RW	0x0002_0101	0x1000	32
DMA_TPDR	RW	0x0000_0000	0x1004	32
DMA_RPDR	RW	0x0000_0000	0x1008	32
DMA_RDLAR	RW	0x0000_0000	0x100C	32
DMA_TDLAR	RW	0x0000_0000	0x1010	32
DMA_SR	RW	0x0000_0000	0x1014	32
DMA_OMR	RW	0x0000_0000	0x1018	32
DMA_IER	RW	0x0000_0000	0x101C	32
DMA_MFOCR	RC	0x0000_0000	0x1020	32
DMA_RIWTR	RW	0x0000_0000	0x1024	32
DMA_AHBSR	R	0x0000_0000	0x102C	32
MAC_CR	RW	0x0000_0000	0x0000	32
MAC_FFR	RW	0x0000_0000	0x0004	32
MAC_HTHR	RW	0x0000_0000	0x0008	32
MAC_HTLR	RW	0x0000_0000	0x000C	32
GMII_AR	RW	0x0000_0000	0x0010	32
GMII_DR	RW	0x0000_0000	0x0014	32
MAC_FCR	RW	0x0000_0000	0x0018	32
MAC_VTR	RW	0x0000_0000	0x001C	32
MAC_DR	R	0x0000_0000	0x0024	32
LPI_CSR	RW	0x0000_0000	0x0030	32
LPI_TCR	RW	0x03E8_0000	0x0034	32
MAC_ISR	R	0x0000_0000	0x0038	32
MAC_IMR	RW	0x0000_0000	0x003C	32
MAC_A0HR	RW	0x8000_FFFF	0x0040	32
MAC_A0LR	RW	0xFFFF_FFFF	0x0044	32
MAC_A1HR	RW	0x0000_FFFF	0x0048	32
MAC_A1LR	RW	0xFFFF_FFFF	0x004C	32

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

MAC_WTR	RW	0x0000_0000	0x00DC	32

31.7.2 Register and Fields Description

31.7.2.1 DMA Bus Mode Register(DMA_BMR,0x1000)

	DMA_BMR																															Base + 0x1000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RIB	Reserved	PRWG		TXPR	MB	AAL	PLBx8	USP	RPBL						FB	PR	PBL							ATDS	DSL					DA	SWR
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Bits	Name	Description	R/W
31	RIB	Rebuild INCRx Burst When this bit is set high and the AHB master gets an EBT (Retry, Split, or Losing bus grant), the AHB master interface rebuilds the pending beats of any burst transfer initiated with INCRx. The AHB master interface rebuilds the beats with a combination of specified bursts with INCRx and SINGLE. By default, the AHB master interface rebuilds pending beats of an EBT with an unspecified (INCR) burst.	RW
30	Reserved	Writing has no effect. Read as zero.	R
29:28	PRWG	Channel Priority Weights This Bits sets the priority weights for Channel 0 during the round-robin arbitration between the DMA channels for the system bus. 00: The priority weight is 1. 01: The priority weight is 2. 10: The priority weight is 3. 11: The priority weight is 4	RW
27	TXPR	Transmit Priority When set, this bit indicates that the transmit DMA has higher priority than the receive DMA during arbitration for the system-side bus.	RW
26	MB	Mixed Burst When this bit is set high and the FB bit is low, the AHB master interface starts all bursts of length more than 16 with INCR (undefined burst), whereas it reverts to fixed burst transfers (INCRx and SINGLE) for burst length of 16 and less.	RW
25	AAL	Address-Aligned Beats When this bit is set high and the FB bit is equal to 1, the AHB interface	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		generates all bursts aligned to the start address LS bits. If the FB bit is equal to 0, the first burst (accessing the start address of data buffer) is not aligned, but subsequent bursts are aligned to the address.	
24	PBLx8	PBLx8 Mode When set high, this bit multiplies the programmed PBL value (Bits [22:17] and Bits[13:8]) eight times. Therefore, the DMA transfers the data in 8, 16, 32, 64, 128, and 256 beats depending on the PBL value.	RW
23	USP	Use Separate PBL When set high, this bit configures the Rx DMA to use the value configured in Bits [22:17] as PBL. The PBL value in Bits [13:8] is applicable only to the Tx DMA operations. When reset to low, the PBL value in Bits [13:8] is applicable for both DMA engines.	RW
22:17	RPBL	Rx DMA PBL This Bits indicates the maximum number of beats to be transferred in one Rx DMA transaction. This is the maximum value that is used in a single block Read or Write. The Rx DMA always attempts to burst as specified in the RPBL bit each time it starts a Burst transfer on the host bus. You can program RPBL with values of 1, 2, 4, 8, 16, and 32. Any other value results in undefined behavior. This Bits is valid and applicable only when USP is set high.	RW
16	FB	Fixed Burst This bit controls the AHB master interface performs fixed burst transfers or not. When set, the AHB interface uses only SINGLE, INCR4, INCR8, or INCR16 during start of the normal burst transfers. When reset, the AHB interface uses SINGLE and INCR burst transfer operations.	RW
15:14	PR	Priority Ratio These bits control the priority ratio in the weighted round-robin arbitration between the Rx DMA and Tx DMA. These bits are valid only when Bit 1 (DA) is reset. The priority ratio is Rx:Tx or Tx:Rx depending on whether Bit 27 (TXPR) is reset or set. 00: The Priority Ratio is 1:1. 01: The Priority Ratio is 2:1. 10: The Priority Ratio is 3:1. 11: The Priority Ratio is 4:1.	RW
13:8	PBL	Programmable Burst Length These bits indicate the maximum number of beats to be transferred in one DMA transaction. This is the maximum value that is used in a single block Read or Write. The DMA always attempts to burst as specified in PBL each time it starts a Burst transfer on the host bus. PBL can be programmed with permissible values of 1, 2, 4, 8, 16, and 32. Any other	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		value results in undefined behavior. When USP is set high, this PBL value is applicable only for Tx DMA transactions. If the number of beats to be transferred is more than 32, then perform the following steps: 1. Set the PBLx8 mode. 2. Set the PBL. For example, if the maximum number of beats to be transferred is 64, then first set PBLx8 to 1 and then set PBL to 8. The PBL values have the following limitation: The maximum number of possible beats (PBL) is limited by the size of the Tx FIFO and Rx FIFO in the MTL layer and the data bus width on the DMA. The FIFO has a constraint that the maximum beat supported is half the depth of the FIFO, except when specified.	
7	ATDS	Alternate Descriptor Size When set, the size of the alternate descriptor increases to 32 bytes (8 DWORDS). This is required when the IPC Full Checksum Offload Engine (Type 2) is enabled in the receiver. The enhanced descriptor is not required if the IPC Full Checksum Offload Engine (Type 2) features are not enabled. In such case, you can use the 16 bytes descriptor to save 4 bytes of memory. IPC Full Checksum Offload Engine (Type 2) feature Otherwise, this bit is reserved and is read-only. When reset, the descriptor size reverts back to 4 DWORDs (16 bytes). This bit preserves the backward compatibility for the descriptor size. In versions prior to 3.50a, the descriptor size is 16 bytes for both normal and enhanced descriptors.	RW
6:2	DSL	Descriptor Skip Length This bit specifies the number of Word, Dword, or Lword (depending on the 32-bit, 64-bit, or 128-bit bus) to skip between two unchained descriptors. The address skipping starts from the end of current descriptor to the start of next descriptor. When the DSL value is equal to zero, the descriptor table is taken as contiguous by the DMA in Ring mode.	RW
1	DA	DMA Arbitration Scheme This bit specifies the arbitration scheme between the transmit and receive paths of Channel 0. 0: Weighted round-robin with Rx:Tx or Tx:Rx The priority between the paths is according to the priority specified in Bits [15:14] (PR) and priority weights specified in Bit 27 (TXPR). 1: Fixed priority The transmit path has priority over receive path when Bit 27 (TXPR) is set. Otherwise, receive path has priority over the transmit path.	RW
0	SWR	Software Reset	RW[1]

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		When this bit is set, the MAC DMA Controller resets the logic and all internal registers of the MAC. It is cleared automatically after the reset operation is complete in all of the GMAC clock domains. Before reprogramming any register of the GMAC, you should read a zero (0) value in this bit. Note: The Software reset function is driven only by this bit. Bit 0 of Register 64 (Channel 1 Bus Mode Register) or Register 128 (Channel 2 Bus Mode Register) has no impact on the Software reset function. The reset operation is completed only when all resets in all active clock domains are de-asserted. Therefore, it is essential that all PHY inputs clocks (applicable for the selected PHY interface) are present for the software reset completion. The time to complete the software reset operation depends on the frequency of the slowest active clock.	

Note:

1. Only support RMII mode
2. [1]:Write Set, self clear

31.7.2.2 DMA Transmit Poll Demand Register(DMA_TPDR,0x1004)

	DMA_TPDR																															Base+ 0x1004
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TPD																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	TPD	Transmit Poll Demand When these bits are written with any value, the DMA reads the current descriptor to which the Register 18 (Current Host Transmit Descriptor Register) is pointing. If that descriptor is not available (owned by the Host), the transmission returns to the Suspend state and Bit 2 (TU) of Register 5 (Status Register) is asserted. If the descriptor is available, the transmission resumes.	RW

Note:

Only support RMII mode

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

31.7.2.3 DMA Receive Poll Demand Register(DMA_RPDR,0x1008)

	DMA_RPDR																															Base + 0x1008
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RPD																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	RPD	Receive Poll Demand When these bits are written with any value, the DMA reads the current descriptor to which the Register 19 (Current Host Receive Descriptor Register) is pointing. If that descriptor is not available (owned by the Host), the reception returns to the Suspended state and Bit 7 (RU) of Register 5 (Status Register) is asserted. If the descriptor is available, the Rx DMA returns to the active state.	RW

Note:

Only support RMII mode

31.7.2.4 DMA Receive Descriptor List Address Register(DMA_RDLAR,0x100C)

	DMA_RDLAR																															Base + 0x100C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RDESLA																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	RDESLA	Start of Receive List This Bits contains the base address of the first descriptor in the Receive Descriptor list. The LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width are ignored and internally taken as all-zero by the DMA. Therefore, these LSB bits are read-only (RO).	RW

Note:

Only support RMII mode

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

31.7.2.5 DMA Transmit Descriptor List Address Register(DMA_TDLAR,0x1010)

	DMA_TDLAR																															Base + 0x1010
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TDESLA																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	TDESLA	Start of Transmit List This Bits contains the base address of the first descriptor in the Transmit Descriptor list. The LSB bits (1:0, 2:0, 3:0) for 32-bit, 64-bit, or 128-bit bus width are ignored and are internally taken as all-zero by the DMA. Therefore, these LSB bits are read-only (RO).	RW

Note:

Only support RMII mode

31.7.2.6 DMA Status Register(DMA_SR,0x1014)

	DMA_BMR																															Base + 0x1014
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	GLPLL/GTMSI	TTI	GPI	GMI	GLI	EB			TS			RS			NIS	AIS	ERI	FBI	Reserved		ETI	RWT	RPS	RU	RI	UNF	OVF	TJT	TU	TPS	TI
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31	Reserved	Writing has no effect, read as zero.	R
30	GLPII OR GTMSI	GLPII: GMAC LPI Interrupt (for Channel 0) This bit indicates an interrupt event in the LPI logic of the GMAC. To reset this bit to 1'b0, the software must read the corresponding registers in the gmac to get the exact cause of the interrupt and clear its source. **Note:** GLPII status is given only in Channel 0 DMA register and is applicable only when the Energy Efficient Ethernet feature is enabled. GTMSI: GMAC TMS Interrupt (for Channel 1 and Channel 2)	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		This bit indicates an interrupt event in the traffic manager and scheduler logic of gmac. To reset this bit, the software must read the corresponding registers (Channel Status Register) to get the exact cause of the interrupt and clear its source.	
29	TTI	Reserved	R
28	GPI	GMAC PMT Interrupt This bit indicates an interrupt event in the PMT module of the gmac. The software must read the PMT Control and Status Register in the MAC to get the exact cause of interrupt and clear its source to reset this bit to 1'b0. The interrupt signal from the gmac subsystem is high when this bit is high.	R
27	GMI	GMAC MMC Interrupt This bit reflects an interrupt event in the MMC module of the GMAC. The software must read the corresponding registers in the GMAC to get the exact cause of the interrupt and clear the source of interrupt to make this bit as 1'b0. The interrupt signal from the gmac subsystem is high when this bit is high. This bit is applicable only when the MAC Management Counters (MMC) are enabled. Otherwise, this bit is reserved.	R
26	GLI	GMAC Line Interface Interrupt When set, this bit reflects any of the following interrupt events in the GMAC interfaces: RGMII: Link change event To identify the exact cause of the interrupt, the software must first read Bit 11 and Bits[2:0] of Register 14 (Interrupt Status Register) and then to clear the source of interrupt (which also clears the GLI interrupt), read any of the following corresponding registers: PCS (TBI, RTBI, or SGMII): Register 49 (AN Status Register) RGMII: Register 54 (RGMII Control and Status Register) General Purpose Input (GPI): Register 56 (General Purpose IO Register)	R
25:23	EB	Error Bits This Bits indicates the type of error that caused a Bus Error, for example, error response on the AHB interface. This Bits is valid only when Bit 13 (FBI) is set. This Bits does not generate an interrupt. 0 0 0: Error during Rx DMA Write Data Transfer 0 1 1: Error during Tx DMA Read Data Transfer 1 0 0: Error during Rx DMA Descriptor Write Access 1 0 1: Error during Tx DMA Descriptor Write Access 1 1 0: Error during Rx DMA Descriptor Read Access 1 1 1: Error during Tx DMA Descriptor Read Access **Note:** 001 and 010 are reserved.	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

22:20	TS	Transmit Process State This Bits indicates the Transmit DMA FSM state. This Bits does not generate an interrupt. 3'b000: Stopped; Reset or Stop Transmit Command issued 3'b001: Running; Fetching Transmit Transfer Descriptor 3'b010: Running; Waiting for status 3'b011: Running; Reading Data from host memory buffer and queuing it to transmit buffer (Tx FIFO) 3'b100: Reserved for future use 3'b101: Reserved for future use 3'b110: Suspended; Transmit Descriptor Unavailable or Transmit Buffer Underflow 3'b111: Running; Closing Transmit Descriptor	R
19:17	RS	Receive Process State This Bits indicates the Receive DMA FSM state. This Bits does not generate an interrupt. 3'b000: Stopped: Reset or Stop Receive Command issued 3'b001: Running: Fetching Receive Transfer Descriptor 3'b010: Reserved for future use 3'b011: Running: Waiting for receive packet 3'b100: Suspended: Receive Descriptor Unavailable 3'b101: Running: Closing Receive Descriptor 3'b110: TIME_STAMP write state 3'b111: Running: Transferring the receive packet data from receive buffer to host memory	R
16	NIS	Normal Interrupt Summary Normal Interrupt Summary bit value is the logical OR of the following bits when the corresponding interrupt bits are enabled in Register 7 (Interrupt Enable Register): Register 5[0]: Transmit Interrupt Register 5[2]: Transmit Buffer Unavailable Register 5[6]: Receive Interrupt Register 5[14]: Early Receive Interrupt Only unmasked bits (interrupts for which interrupt enable is set in Register 7) affect the Normal Interrupt Summary bit. This is a sticky bit and must be cleared (by writing 1 to this bit) each time a corresponding bit, which causes NIS to be set, is cleared.	RW[1]
15	AIS	Abnormal Interrupt Summary Abnormal Interrupt Summary bit value is the logical OR of the following when the corresponding interrupt bits are enabled in Register 7 (Interrupt Enable Register): Register 5[1]: Transmit Process Stopped Register 5[3]: Transmit Jabber Timeout	RW[2]

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		Register 5[4]: Receive FIFO Overflow Register 5[5]: Transmit Underflow Register 5[7]: Receive Buffer Unavailable Register 5[8]: Receive Process Stopped Register 5[9]: Receive Watchdog Timeout Register 5[10]: Early Transmit Interrupt Register 5[13]: Fatal Bus Error Only unmasked bits affect the Abnormal Interrupt Summary bit. This is a sticky bit and must be cleared (by writing 1 to this bit) each time a corresponding bit, which causes AIS to be set, is cleared.	
14	ERI	Early Receive Interrupt This bit indicates that the DMA filled the first data buffer of the packet. This bit is cleared when the software writes 1 to this bit or Bit 6 (RI) of this register is set (whichever occurs earlier).	RW[3]
13	FBI	Fatal Bus Error Interrupt This bit indicates that a bus error occurred, as described in Bits [25:23]. When this bit is set, the corresponding DMA engine disables all of its bus accesses.	RW[4]
12:11	Reserved	Writing has no effect, read as zero.	R
10	ETI	Early Transmit Interrupt This bit indicates that the frame to be transmitted is fully transferred to the MTL Transmit FIFO.	RW[5]
9	RWT	Receive Watchdog Timeout When set, this bit indicates that the Receive Watchdog Timer expired while receiving the current frame and the current frame is truncated after the watchdog timeout.	RW[6]
8	RPS	Receive Process Stopped This bit is asserted when the Receive Process enters the Stopped state.	RW[7]
7	RU	Receive Buffer Unavailable This bit indicates that the host owns the Next Descriptor in the Receive List and the DMA cannot acquire it. The Receive Process is suspended. To resume processing Receive descriptors, the host should change the ownership of the descriptor and issue a Receive Poll Demand command. If no Receive Poll Demand is issued, the Receive Process resumes when the next recognized incoming frame is received. This bit is set only when the previous Receive Descriptor is owned by the DMA.	RW[8]
6	RI	Receive Interrupt This bit indicates that the frame reception is complete. When reception is complete, the Bit 31 of RDES1 (Disable Interrupt on	RW[9]

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		Completion) is reset in the last Descriptor, and the specific frame status information is updated in the descriptor. The reception remains in the Running state.	
5	UNF	Transmit Underflow This bit indicates that the Transmit Buffer had an Underflow during frame transmission. Transmission is suspended and an Underflow Error TDES0[1] is set.	RW[10]
4	OVF	Receive Overflow This bit indicates that the Receive Buffer had an Overflow during frame reception. If the partial frame is transferred to the application, the overflow status is set in RDES0[11].	RW[11]
3	TJT	Transmit Jabber Timeout This bit indicates that the Transmit Jabber Timer expired, which happens when the frame size exceeds 2,048 (10,240 bytes when the Jumbo frame is enabled). When the Jabber Timeout occurs, the transmission process is aborted and placed in the Stopped state. This causes the Transmit Jabber Timeout TDES0[14] flag to assert.	RW[12]
2	TU	Transmit Buffer Unavailable This bit indicates that the host owns the Next Descriptor in the Transmit List and the DMA cannot acquire it. Transmission is suspended. Bits[22:20] explain the Transmit Process state transitions. To resume processing Transmit descriptors, the host should change the ownership of the descriptor by setting TDES0[31] and then issue a Transmit Poll Demand command.	RW[13]
1	TPS	Transmit Process Stopped This bit is set when the transmission is stopped.	RW[14]
0	TI	Transmit Interrupt This bit indicates that the frame transmission is complete. When transmission is complete, Bit 31 (OWN) of TDES0 is reset, and the specific frame status information is updated in the descriptor.	RW[15]

Note:

1. Only support RMII mode
2. [1]~[15]:This bits will operate with Self set, read clear function.

31.7.2.7 DMA Operation Mode Register(DMA_OMR,0x1018)

	DMA_OMR																															Base + 0x1018
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Reserved					DT	RSF	DFF	Reserved		TSF	FTF	Reserved			TTC			ST	RFD		RFA		EFC	FEF	FUF	DGF	RTC		OSF	SR	Reserved
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:27	Reserved	Writing has no effect, read as zero.	R
26	DT	Disable Dropping of TCP/IP Checksum Error Frames When this bit is set, the MAC does not drop the frames which only have errors detected by the Receive Checksum Offload engine. Such frames do not have any errors (including FCS error) in the Ethernet frame received by the MAC but have errors only in the encapsulated payload. When this bit is reset, all error frames are dropped if the FEF bit is reset. If the IPC Full Checksum Offload Engine (Type 2) is disabled, this bit is reserved (RO with value 1'b0).	RW
25	RSF	Receive Store and Forward When this bit is set, the MTL reads a frame from the Rx FIFO only after the complete frame has been written to it, ignoring the RTC bits. When this bit is reset, the Rx FIFO operates in the cut-through mode, subject to the threshold specified by the RTC bits.	RW
24	DFF	Disable Flushing of Received Frames When this bit is set, the Rx DMA does not flush any frames because of the unavailability of receive descriptors or buffers as it does normally when this bit is reset.	RW
23:22	Reserved	Writing has no effect, read as zero.	R
21	TSF	Transmit Store and Forward When this bit is set, transmission starts when a full frame resides in the MTL Transmit FIFO. When this bit is set, the TTC values specified in Bits [16:14] are ignored. This bit should be changed only when the transmission is stopped.	RW
20	FTF	Flush Transmit FIFO When this bit is set, the transmit FIFO controller logic is reset to its default values and thus all data in the Tx FIFO is lost or flushed. This bit is cleared internally when the flushing operation is complete. The Operation Mode register should not be written to until this bit is cleared. The data which is already accepted by the MAC transmitter is not flushed. It is scheduled for transmission and results in underflow and runt frame transmission. Note:	RW[1]

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		The flush operation is complete only when the Tx FIFO is emptied of its contents and all the pending Transmit Status of the transmitted frames are accepted by the host. In order to complete this flush operation, the PHY transmit clock is required to be active.	
19:17	Reserved	Writing has no effect, read as zero.	R
16:14	TTC	Transmit Threshold Control These bits control the threshold level of the MTL Transmit FIFO. Transmission starts when the frame size within the MTL Transmit FIFO is larger than the threshold. In addition, full frames with a length less than the threshold are also transmitted. These bits are used only when Bit 21 (TSF) is reset. ▪ 000: 64 ▪ 001: 128 ▪ 010: 192 ▪ 011: 256 ▪ 100: 40 ▪ 101: 32 ▪ 110: 24 ▪ 111: 16	RW
13	ST	Start or Stop Transmission Command When this bit is set, transmission is placed in the Running state, and the DMA checks the Transmit List at the current position for a frame to be transmitted. Descriptor acquisition is attempted either from the current position in the list, which is the Transmit List Base Address set by Register 4 (Transmit Descriptor List Address Register), or from the position retained when transmission was stopped previously. If the DMA does not own the current descriptor, transmission enters the Suspended state and Bit 2 (Transmit Buffer Unavailable) of Register 5 (Status Register) is set. The Start Transmission command is effective only when transmission is stopped. If the command is issued before setting Register 4 (Transmit Descriptor List Address Register), then the DMA behavior is unpredictable. When this bit is reset, the transmission process is placed in the Stopped state after completing the transmission of the current frame. The Next Descriptor position in the Transmit List is saved, and it becomes the current position when transmission is restarted. To change the list address, you need to program Register 4 (Transmit Descriptor List Address Register) with a new value when this bit is reset. The new value is considered when this bit is set again. The stop transmission command is effective only when the transmission of the current frame is complete or the transmission is in the Suspended state.	RW
12:11	RFD	Threshold for Deactivating Flow Control (in half-duplex and full-duplex	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		modes) These bits control the threshold (Fill-level of Rx FIFO) at which the flow control is de-asserted after activation. ▪00: Full minus 1 KB, that is, FULL — 1 KB ■ 01: Full minus 2 KB, that is, FULL — 2 KB ■ 10: Full minus 3 KB, that is, FULL — 3 KB ■ 11: Full minus 4 KB, that is, FULL — 4 KB The de-assertion is effective only after flow control is asserted. If the Rx FIFO is 8 KB or more, an additional Bit (RFD_2) is used for more threshold levels as described in Bit 22. These bits are reserved and read-only when the Rx FIFO depth is less than 4 KB.	
10:9	RFA	Threshold for Activating Flow Control (in half-duplex and full-duplex modes) These bits control the threshold (Fill level of Rx FIFO) at which the flow control is activated. ▪00: Full minus 1 KB, that is, FULL—1KB. ▪01: Full minus 2 KB, that is, FULL—2KB. ▪10: Full minus 3 KB, that is, FULL—3KB. ▪11: Full minus 4 KB, that is, FULL—4KB. These values are applicable only to Rx FIFOs of 4 KB or more and when Bit 8 (EFC) is set high. If the Rx FIFO is 8 KB or more, an additional Bit (RFA_2) is used for more threshold levels as described in Bit 23. These bits are reserved and read-only when the depth of Rx FIFO is less than 4 KB.	RW
8	EFC	Enable HW Flow Control When this bit is set, the flow control signal operation based on the fill-level of Rx FIFO is enabled. When reset, the flow control operation is disabled. This bit is not used (reserved and always reset) when the Rx FIFO is less than 4 KB.	RW
7	FEF	Forward Error Frames When this bit is reset, the Rx FIFO drops frames with error status (CRC error, collision error, GMII_ER, giant frame, watchdog timeout, or overflow). However, if the start byte (write) pointer of a frame is already transferred to the read controller side (in Threshold mode), then the frame is not dropped. When the FEF bit is set, all frames except runt error frames are forwarded to the DMA. If the Bit 25 (RSF) is set and the Rx FIFO overflows when a partial frame is written, then the frame is dropped irrespective of the FEF bit setting. However, if the Bit 25 (RSF) is reset and the Rx FIFO overflows when a partial frame is written, then a partial frame may be forwarded to the DMA. **Note:** When FEF bit is reset, the giant frames are dropped if the giant frame status is given in Rx Status in the following configurations: The IP checksum engine (Type 1) and full checksum offload engine (Type 2) are not selected.	RW
6	FUF	Forward Undersized Good Frames When set, the Rx FIFO forwards Undersized frames (that is, frames with no Error and length less than 64 bytes) including pad-bytes and CRC. When reset, the Rx FIFO drops all frames of less than 64 bytes, unless a frame is already transferred because of the lower value of Receive	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		Threshold, for example, RTC = 01.	
5	DGF	Drop Giant Frames When set, the MAC drops the received giant frames in the Rx FIFO, that is, frames that are larger than the computed giant frame limit. When reset, the MAC does not drop the giant frames in the Rx FIFO.	RW
4:3	RTC	Receive Threshold Control These two bits control the threshold level of the MTL Receive FIFO. Transfer (request) to DMA starts when the frame size within the MTL Receive FIFO is larger than the threshold. In addition, full frames with length less than the threshold are automatically transferred. The value of 11 is not applicable if the configured Receive FIFO size is 128 bytes. These bits are valid only when the RSF bit is zero, and are ignored when the RSF bit is set to 1. ▪ 00: 64 ▪ 01: 32 ▪ 10: 96 ▪ 11: 128	RW
2	OSF	Operate on Second Frame When this bit is set, it instructs the DMA to process the second frame of the Transmit data even before the status for the first frame is obtained.	RW
1	SR	Start or Stop Receive When this bit is set, the Receive process is placed in the Running state. The DMA attempts to acquire the descriptor from the Receive list and processes the incoming frames. The descriptor acquisition is attempted from the current position in the list, which is the address set by the Register 3 (Receive Descriptor List Address Register) or the position retained when the Receive process was previously stopped. If the DMA does not own the descriptor, reception is suspended and Bit 7 (Receive Buffer Unavailable) of Register 5 (Status Register) is set. The Start Receive command is effective only when the reception has stopped. If the command is issued before setting Register 3 (Receive Descriptor List Address Register), the DMA behavior is unpredictable. When this bit is cleared, the Rx DMA operation is stopped after the transfer of the current frame. The next descriptor position in the Receive list is saved and becomes the current position after the Receive process is restarted. The Stop Receive command is effective only when the Receive process is in either the Running (waiting for receive packet) or in the Suspended state. **Note:** For information about how to pause the transmission, see "Stopping and Starting Transmission".	RW
0	-	Reserved	R

Note:

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Only support RMII mode

31.7.2.8 DMA Interrupt Enable Register(DMA_IER,0x101C)

	DMA_IER																															Base + 0x101C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved															NIE	AIE	ERE	FBEE	Reserved		ETE	RWE	RSE	RUE	RIE	UNE	OVE	TJE	TUE	TSE	TIE
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:17	Reserved	Writing has no effect, read as zero.	R
16	NIE	Normal Interrupt Summary Enable When this bit is set, normal interrupt summary is enabled. When this bit is reset, normal interrupt summary is disabled. This bit enables the following interrupts in Register 5 (Status Register): ▪ Register 5[0]: Transmit Interrupt ▪ Register 5[2]: Transmit Buffer Unavailable ▪ Register 5[6]: Receive Interrupt ▪ Register 5[14]: Early Receive Interrupt	RW
15	AIE	Abnormal Interrupt Summary Enable When this bit is set, abnormal interrupt summary is enabled. When this bit is reset, the abnormal interrupt summary is disabled. This bit enables the following interrupts in Register 5 (Status Register): ▪ Register 5[1]: Transmit Process Stopped ▪ Register 5[3]: Transmit Jabber Timeout ▪ Register 5[4]: Receive Overflow ▪ Register 5[5]: Transmit Underflow ▪ Register 5[7]: Receive Buffer Unavailable ▪ Register 5[8]: Receive Process Stopped ▪ Register 5[9]: Receive Watchdog Timeout ▪ Register 5[10]: Early Transmit Interrupt ▪ Register 5[13]: Fatal Bus Error	RW
14	ERE	Early Receive Interrupt Enable When this bit is set with Normal Interrupt Summary Enable (Bit 16), the Early Receive Interrupt is enabled. When this bit is reset, the Early Receive Interrupt is disabled.	RW
13	FBEE	Fatal Bus Error Enable When this bit is set with Abnormal Interrupt Summary Enable (Bit 15),	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		the Fatal Bus Error Interrupt is enabled. When this bit is reset, the Fatal Bus Error Enable Interrupt is disabled.	
12:11	Reserved	Writing has no effect, read as zero.	R
10	ETE	Early Transmit Interrupt Enable When this bit is set with an Abnormal Interrupt Summary Enable (Bit 15), the Early Transmit Interrupt is enabled. When this bit is reset, the Early Transmit Interrupt is disabled.	RW
9	RWE	Receive Watchdog Timeout Enable When this bit is set with Abnormal Interrupt Summary Enable (Bit 15), the Receive Watchdog Timeout Interrupt is enabled. When this bit is reset, the Receive Watchdog Timeout Interrupt is disabled.	RW
8	RSE	Receive Stopped Enable When this bit is set with Abnormal Interrupt Summary Enable (Bit 15), the Receive Stopped Interrupt is enabled. When this bit is reset, the Receive Stopped Interrupt is disabled.	RW
7	RUE	Receive Buffer Unavailable Enable When this bit is set with Abnormal Interrupt Summary Enable (Bit 15), the Receive Buffer Unavailable Interrupt is enabled. When this bit is reset, the Receive Buffer Unavailable Interrupt is disabled.	RW
6	RIE	Receive Interrupt Enable When this bit is set with Normal Interrupt Summary Enable (Bit 16), the Receive Interrupt is enabled. When this bit is reset, the Receive Interrupt is disabled.	RW
5	UNE	Underflow Interrupt Enable When this bit is set with Abnormal Interrupt Summary Enable (Bit 15), the Transmit Underflow Interrupt is enabled. When this bit is reset, the Underflow Interrupt is disabled.	RW
4	OVE	Overflow Interrupt Enable When this bit is set with Abnormal Interrupt Summary Enable (Bit 15), the Receive Overflow Interrupt is enabled. When this bit is reset, the Overflow Interrupt is disabled.	RW
3	TJE	Transmit Jabber Timeout Enable When this bit is set with Abnormal Interrupt Summary Enable (Bit 15), the Transmit Jabber Timeout Interrupt is enabled. When this bit is reset, the Transmit Jabber Timeout Interrupt is disabled.	RW
2	TUE	Transmit Buffer Unavailable Enable When this bit is set with Normal Interrupt Summary Enable (Bit 16), the Transmit Buffer Unavailable Interrupt is enabled. When this bit is reset, the Transmit Buffer Unavailable Interrupt is disabled.	RW
1	TSE	Transmit Stopped Enable When this bit is set with Abnormal Interrupt Summary Enable (Bit 15), the Transmission Stopped Interrupt is enabled. When this bit is reset,	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		the Transmission Stopped Interrupt is disabled.	
0	TIE	Transmit Interrupt Enable When this bit is set with Normal Interrupt Summary Enable (Bit 16), the Transmit Interrupt is enabled. When this bit is reset, the Transmit Interrupt is disabled.	RW

Note:

Only support RMII mode

31.7.2.9 DMA Missed Frame and Buffer Overflow Counter Register(DMA_MFOCR,0x1020)

	DMA_MFOCR																															Base + 0x1020
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			OVFCNTOVF	MISCNTOVF											MISCNTOVF	MISFRMCNT															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:29	Reserved	Writing has no effect, read as zero.	R
28	OVFCNTOVF	Overflow Bit for FIFO Overflow Counter This bit is set every time the Overflow Frame Counter (Bits[27:17]) overflows, that is, the Rx FIFO overflows with the overflow frame counter at maximum value. In such a scenario, the overflow frame counter is reset to all-zeros and this bit indicates that the rollover happened.	RC[1]
27:17	OVFFRMCNT	Overflow Frame Counter This Bits indicates the number of frames missed by the application. This counter is incremented each time the MTL FIFO overflows. The counter is cleared when this register is read with mci_be_i[2] at 1'b1.	RC[2]
16	MISCNTOVF	Overflow Bit for Missed Frame Counter This bit is set every time Missed Frame Counter (Bits[15:0]) overflows, that is, the DMA discards an incoming frame because of the Host Receive Buffer being unavailable with the missed frame counter at maximum value. In such a scenario, the Missed frame counter is reset to all-zeros and this bit indicates that the rollover happened.	RC[3]
15:0	MISFRMCNT	Missed Frame Counter This Bits indicates the number of frames missed by the controller because of the Host Receive Buffer being unavailable. This counter is incremented each time the DMA discards an incoming frame. The	RC[4]

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		counter is cleared when this register is read with mci_be_i[0] at 1'b1.	

Note:1. Only support RMII mode

2. [1]~[4]:This bits will operate with Self set, read clear function.

31.7.2.10 DMA Receive Interrupt Watchdog Timer Register(DMA_RIWTR,0x1024)

	DMA_BMR																															Base + 0x1024
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								RIWT							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:8	Reserved	Writing has no effect, read as zero.	R
7:0	RIWT	RI Watchdog Timer Count This bit indicates the number of system clock cycles multiplied by 256 for which the watchdog timer is set. The watchdog timer gets triggered with the programmed value after the Rx DMA completes the transfer of a frame for which the RI status bit is not set because of the setting in the corresponding descriptor RDES1[31]. When the watchdog timer runs out, the RI bit is set and the timer is stopped. The watchdog timer is reset when the RI bit is set high because of automatic setting of RI as per RDES1[31] of any received frame.	RW

Note:Only support RMII mode

31.7.2.11 DMA AHB State Register(DMA_AHBSR,0x102C)

	DMA_AHBSR																															Base + 0x102C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															AXWHSTS
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:1	Reserved	Writing has no effect, read as zero.	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

0	AXWHSTS	AHB Master Status	R

Note:Only support RMII mode

31.7.2.12 MAC Configuration Register(MAC_CR,0x0000)

	MAC_CR																															Base + 0x0000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	SARC			TWOKPE	Reserved	CST	TC	WD	JD	BE	JE	IFG			DCRS	PS	FES	DO	LM	DM	IPC	DR	LUD	ACS	BL		DC	TE	RE	PRELEN	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31	Reserved	Writing has no effect, read as zero.	R
30:28	SARC	Source Address Insertion or Replacement Control This Bits controls the source address insertion or replacement for all transmitted frames. Bit 30 specifies which MAC Address register (0 or 1) is used for source address insertion or replacement based on the values of Bits [29:28]: 2'b0*x*: The input signals mti_sa_ctrl_i and ati_sa_ctrl_i control the SA Bits generation. 2'b10: If Bit 30 is set to 0, the MAC inserts the content of the MAC Address 0 registers (registers 16 and 17) in the SA Bits of all transmitted frames. If Bit 30 is set to 1 and the Enable MAC Address Register 1 option is selected during core configuration, the MAC inserts the content of the MAC Address 1 registers (registers 18 and 19) in the SA Bits of all transmitted frames. 2'b11: If Bit 30 is set to 0, the MAC replaces the content of the MAC Address 0 registers (registers 16 and 17) in the SA Bits of all transmitted frames. If Bit 30 is set to 1 and the Enable MAC Address Register 1 option is selected during core configuration, the MAC replaces the content of the MAC Address 1 registers (registers 18 and 19) in the SA Bits of all transmitted frames. **Note:** Changes to this Bits take effect only on the start of a frame. If you write this register Bits when a frame is being transmitted, only the subsequent frame can use the updated value, that is, the current frame does not use the updated value.	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		These bits are reserved and RO when the Enable SA, VLAN, and CRC Insertion on TX feature is not selected during core configuration.	
27	TWOKPE	IEEE 802.3as Support for 2K Packets When set, the MAC considers all frames, with up to 2,000 bytes length, as normal packets. When Bit 20 (JE) is not set, the MAC considers all received frames of size more than 2K bytes as Giant frames. When this bit is reset and Bit 20 (JE) is not set, the MAC considers all received frames of size more than 1,518 bytes (1,522 bytes for tagged) as Giant frames. When Bit 20 is set, setting this bit has no effect on Giant Frame status. For more information about how the setting of this bit and Bit 20 impact the Giant frame status.	RW
26	Reserved	Writing has no effect, read as zero.	RW
25	CST	CRC Stripping for Type Frames When this bit is set, the last 4 bytes (FCS) of all frames of Ether type (Length/Type Bits greater than or equal to 1,536) are stripped and dropped before forwarding the frame to the application. This function is not valid when the IP Checksum Engine (Type 1) is enabled in the MAC receiver. This function is valid when Type 2 Checksum Offload Engine is enabled. **Note:** For information about how the settings of Bit 7 (ACS) and this bit impact the frame length.	RW
24	TC	Transmit Configuration in RGMII When set, this bit enables the transmission of duplex mode, link speed, and link up or down information to the PHY in the RGMI port. When this bit is reset, no such information is driven to the PHY.	RW
23	WD	Watchdog Disable When this bit is set, the MAC disables the watchdog timer on the receiver. The MAC can receive frames of up to 16,384 bytes. When this bit is reset, the MAC does not allow a receive frame which more than 2,048 bytes (10,240 if JE is set high) or the value programmed in Register 55 (Watchdog Timeout Register). The MAC cuts off any bytes received after the watchdog limit number of bytes.	RW
22	JD	Jabber Disable When this bit is set, the MAC disables the jabber timer on the transmitter. The MAC can transfer frames of up to 16,384 bytes. When this bit is reset, the MAC cuts off the transmitter if the application sends out more than 2,048 bytes of data (10,240 if JE is set high) during transmission.	RW
21	BE	Frame Burst Enable When this bit is set, the MAC allows frame bursting during transmission	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		in the GMII half-duplex mode. This bit is reserved (and RO) in the 10/100 Mbps only or full-duplex-only configurations.	
20	JE	Jumbo Frame Enable When this bit is set, the MAC allows Jumbo frames of 9,018 bytes (9,022 bytes for VLAN tagged frames) without reporting a giant frame error in the receive frame status.	RW
19:17	IFG	Inter-Frame Gap These bits control the minimum IFG between frames during transmission. 000: 96 bit times 001: 88 bit times 010: 80 bit times ... 111: 40 bit times In the half-duplex mode, the minimum IFG can be configured only for 64 bit times (IFG = 100). Lower values are not considered. In the 1000-Mbps mode, the minimum IFG supported is 80 bit times.	RW
16	DCRS	Disable Carrier Sense During Transmission When set high, this bit makes the MAC transmitter ignore the (G)MII CRS signal during frame transmission in the half-duplex mode. This request results in no errors generated because of Loss of Carrier or No Carrier during such transmission. When this bit is low, the MAC transmitter generates such errors because of Carrier Sense and can even abort the transmissions. This bit is reserved (and RO) in the full-duplex-only configurations.	RW
15	PS	Port Select This bit selects the Ethernet line speed. 0: For 1000 Mbps operations 1: For 10 or 100 Mbps operations In 10 or 100 Mbps operations, this bit, along with FES bit, selects the exact line speed. In the 10/100 Mbps-only (always 1) or 1000 Mbps-only (always 0) configurations, this bit is read-only with the appropriate value. In default 10/100/1000 Mbps configuration, this bit is R_W.	RW
14	FES	Speed This bit selects the speed in the MII, RMII, RGMII or GMII interface: 0: 10 Mbps 1: 100 Mbps	RW
13	DO	Disable Receive Own When this bit is set, the MAC disables the reception of frames when the TXEN is asserted in the half-duplex mode. When this bit is reset, the MAC receives all packets that are given by the PHY while transmitting.	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		This bit is not applicable if the MAC is operating in the full-duplex mode. This bit is reserved (RO with default value) if the MAC is configured for the full-duplex-only operation.	
12	LM	Loopback Mode When this bit is set, the MAC operates in the loopback mode at GMII or MII. The (G)MII Receive clock input (RX_CLK) is required for the loopback to work properly, because the Transmit clock is not looped-back internally.	RW
11	DM	Duplex Mode When this bit is set, the MAC operates in the full-duplex mode where it can transmit and receive simultaneously. This bit is RO with default value of 1'b1 in the full-duplex-only configuration.	RW
10	IPC	Checksum Offload When this bit is set, the MAC calculates the 16-bit one's complement of the one's complement sum of all received Ethernet frame payloads. It also checks whether the IPv4 Header checksum (assumed to be bytes 25-26 or 29-30 (VLAN- tagged) of the received Ethernet frame) is correct for the received frame and gives the status in the receive status word. The MAC also appends the 16-bit checksum calculated for the IP header datagram payload (bytes after the IPv4 header) and appends it to the Ethernet frame transferred to the application (when Type 2 COE is deselected). When this bit is reset, this function is disabled. When Type 2 COE is selected, this bit, when set, enables the IPv4 header checksum checking and IPv4 or IPv6 TCP, UDP, or ICMP payload checksum checking. When this bit is reset, the COE function in the receiver is disabled and the corresponding PCE and IP HCE status bits are always cleared.	RW
9	DR	Disable Retry When this bit is set, the MAC attempts only one transmission. When a collision occurs on the GMII or MII interface, the MAC ignores the current frame transmission and reports a Frame Abort with excessive collision error in the transmit frame status. When this bit is reset, the MAC attempts retries based on the settings of the BL Bits (Bits [6:5]). This bit is applicable only in the half-duplex mode and is reserved (RO with default value) in the full-duplex-only configuration.	RW
8	LUD	Link Up or Down This bit indicates whether the link is up or down during the transmission of configuration in the RGMI: 0: Link Down 1: Link Up	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

7	ACS	Automatic Pad or CRC Stripping When this bit is set, the MAC strips the Pad or FCS Bits on the incoming frames only if the value of the length Bits is less than 1,536 bytes. All received frames with length Bits greater than or equal to 1,536 bytes are passed to the application without stripping the Pad or FCS Bits. When this bit is reset, the MAC passes all incoming frames, without modifying them, to the Host. **Note:** For information about how the settings of Bit 23 (CST) and this bit impact the frame length.	RW
6:5	BL	Back-Off Limit The Back-Off limit determines the random integer number (r) of slot time delays (4,096 bit times for 1000 Mbps and 512 bit times for 10/100 Mbps) for which the MAC waits before rescheduling a transmission attempt during retries after a collision. This bit is applicable only in the half-duplex mode and is reserved (RO) in the full-duplex-only configuration. 00: k= min (*n*, 10) 01: k = min (*n*, 8) 10: k = min (*n*, 4) 11: k = min (*n*, 1) where *n* = retransmission attempt. The random integer *r* takes the value in the range $0 \leq r < 2^k$	RW
4	DC	Deferral Check When this bit is set, the deferral check function is enabled in the MAC. The MAC issues a Frame Abort status, along with the excessive deferral error bit set in the transmit frame status, when the transmit state machine is deferred for more than 24,288 bit times in the 10 or 100 Mbps mode. If the MAC is configured for 1000 Mbps operation or if the Jumbo frame mode is enabled in the 10 or 100 Mbps mode, the threshold for deferral is 155,680 bits times. Deferral begins when the transmitter is ready to transmit, but it is prevented because of an active carrier sense signal (CRS) on GMII or MII. The defer time is not cumulative. For example, if the transmitter defers for 10,000 bit times because the CRS signal is active and then the CRS signal becomes inactive, the transmitter transmits and collision happens. Because of collision, the transmitter needs to back off and then defer again after back off completion. In such a scenario, the deferral timer is reset to 0 and it is restarted. When this bit is reset, the deferral check function is disabled and the MAC defers until the CRS signal goes inactive. This bit is applicable only in the half-duplex mode and is reserved (RO) in the full-duplex-only configuration.	RW
3	TE	Transmitter Enable When this bit is set, the transmit state machine of the MAC is enabled for	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		transmission on the GMII or MII. When this bit is reset, the MAC transmit state machine is disabled after the completion of the transmission of the current frame, and does not transmit any further frames.	
2	RE	Receiver Enable When this bit is set, the receiver state machine of the MAC is enabled for receiving frames from the GMII or MII. When this bit is reset, the MAC receive state machine is disabled after the completion of the reception of the current frame, and does not receive any further frames from the GMII or MII.	RW
1:0	PRELEN	Preamble Length for Transmit frames These bits control the number of preamble bytes that are added to the beginning of every Transmit frame. The preamble reduction occurs only when the MAC is operating in the full-duplex mode. 2'b00: 7 bytes of preamble 2'b01: 5 bytes of preamble 2'b10: 3 bytes of preamble 2'b11: Reserved	RW

Note:Only support RMII mode

31.7.2.13 MAC Frame Filter Register(MAC_FFR,0x0004)

	MAC_FFR																															Base + 0x0004
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RA	Reserved														VTFE	Reserved					HPF	SAF	SAIF	PCF		DBF	PM	DAIF	HMC	HUC	PR
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31	RA	Receive All When this bit is set, the MAC Receiver module passes all received frames, irrespective of whether they pass the address filter or not, to the Application. The result of the SA or DA filtering is updated (pass or fail) in the corresponding bits in the Receive Status Word. When this bit is reset, the Receiver module passes only those frames to the Application that pass the SA or DA address filter.	RW
30:17	Reserved	Writing has no effect, read as zero.	R
16	VTFE	VLAN Tag Filter Enable When set, this bit enables the MAC to drop VLAN tagged frames that do not match the VLAN Tag comparison. When reset, the MAC forwards all frames irrespective of the match status of the VLAN Tag.	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

15:11	Reserved	Writing has no effect, read as zero.	RW
10	HPF	Hash or Perfect Filter When this bit is set, it configures the address filter to pass a frame if it matches either the perfect filtering or the hash filtering as set by the HMC or HUC bits. When this bit is low and the HUC or HMC bit is set, the frame is passed only if it matches the Hash filter.	RW
9	SAF	Source Address Filter Enable When this bit is set, the MAC compares the SA Bits of the received frames with the values programmed in the enabled SA registers. If the comparison fails, the MAC drops the frame. When this bit is reset, the MAC forwards the received frame to the application with updated SAF bit of the Rx Status depending on the SA address comparison. **Note:** According to the IEEE specification, Bit 47 of the SA is reserved and set to 0. However, in gmac, the MAC compares all 48 bits. The software driver should take this into consideration while programming the MAC address registers for SA.	RW
8	SAIF	SA Inverse Filtering When this bit is set, the Address Check block operates in inverse filtering mode for the SA address comparison. The frames whose SA matches the SA registers are marked as failing the SA Address filter. When this bit is reset, frames whose SA does not match the SA registers are marked as failing the SA Address filter.	RW
7:6	PCF	Pass Control Frames These bits control the forwarding of all control frames (including unicast and multicast Pause frames). 00: MAC filters all control frames from reaching the application. 01: MAC forwards all control frames except Pause frames to application even if they fail the Address filter. 10: MAC forwards all control frames to application even if they fail the Address Filter. 11: MAC forwards control frames that pass the Address Filter. The following conditions should be true for the Pause frames processing: Condition 1: The MAC is in the full-duplex mode and flow control is enabled by setting Bit 2 (RFE) of Register 6 (Flow Control Register) to 1. Condition 2: The destination address (DA) of the received frame matches the special multicast address or the MAC Address 0 when Bit 3 (UP) of the Register 6 (Flow Control Register) is set. Condition 3: The Type Bits of the received frame is 0x8808 and the OPCODE Bits is 0x0001. **Note:** This Bits should be set to 01 only when the Condition 1 is true, that	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		is, the MAC is programmed to operate in the full-duplex mode and the RFE bit is enabled. Otherwise, the Pause frame filtering may be inconsistent. When Condition 1 is false, the Pause frames are considered as generic control frames. Therefore, to pass all control frames (including Pause frames) when the full-duplex mode and flow control is not enabled, you should set the PCF Bits to 10 or 11 (as required by the application).	
5	DBF	Disable Broadcast Frames When this bit is set, the AFM module blocks all incoming broadcast frames. In addition, it overrides all other filter settings. When this bit is reset, the AFM module passes all received broadcast frames.	RW
4	PM	Pass All Multicast When set, this bit indicates that all received frames with a multicast destination address (first bit in the destination address Bits is '1') are passed. When reset, filtering of multicast frame depends on HMC bit.	RW
3	DAIF	DA Inverse Filtering When this bit is set, the Address Check block operates in inverse filtering mode for the DA address comparison for both unicast and multicast frames. When reset, normal filtering of frames is performed.	RW
2	HMC	Hash Multicast When set, MAC performs destination address filtering of received multicast frames according to the hash table. When reset, the MAC performs a perfect destination address filtering for multicast frames, that is, it compares the DA Bits with the values programmed in DA registers.	RW
1	HUC	Hash Unicast When set, MAC performs destination address filtering of unicast frames according to the hash table. When reset, the MAC performs a perfect destination address filtering for unicast frames, that is, it compares the DA Bits with the values programmed in DA registers.	RW
0	PR	Promiscuous Mode When this bit is set, the Address Filter module passes all incoming frames irrespective of the destination or source address. The SA or DA Filter Fails status bits of the Receive Status Word are always cleared when PR is set.	RW

Note:

Only support RMII mode

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

31.7.2.14 MAC Hash Table High Register(MAC_HTHR,0x0008)

	MAC_HTHR																															Base + 0x0008
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	HTH																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	HTH	Hash Table High This Bits contains the upper 32 bits of the Hash table.	RW

Note:

Only support RMII mode

31.7.2.15 MAC Hash Table Low Register(MAC_HTLR,0x000C)

	MAC_HTLR																															Base + 0x000C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	HTL																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	HTL	Hash Table Low This Bits contains the lower 32 bits of the Hash table.	RW

Note:

Only support RMII mode

31.7.2.16 GMII Address Register(GMII_AR,0x0010)

	GMII_AR																															Base + 0x0010
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																PA					GR					CR				GW	GB

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:16	Reserved	Writing has no effect, read as zero.	R
15:11	PA	Physical Layer Address This Bits indicates which of the 32 possible PHY devices are being accessed.	RW
10:6	GR	GMII Register These bits select the desired GMII register in the selected PHY device.	RW
5:2	CR	CSR Clock Range The CSR Clock Range selection determines the frequency of the MDC clock according to the CSR clock frequency used in your design. The suggested range of CSR clock frequency applicable for each value (when Bit[5] = 0) ensures that the MDC clock is approximately between the frequency range 1.0 MHz-2.5 MHz. 0000: The CSR clock frequency is 60-100 MHz and the MDC clock frequency is CSR clock/42. 0001: The CSR clock frequency is 100-150 MHz and the MDC clock frequency is CSR clock/62. 0010: The CSR clock frequency is 20-35 MHz and the MDC clock frequency is CSR clock/16. 0011: The CSR clock frequency is 35-60 MHz and the MDC clock frequency is CSR clock/26. 0100: The CSR clock frequency is 150-250 MHz and the MDC clock frequency is CSR clock/102. 0101: The CSR clock frequency is 250-300 MHz and the MDC clock is CSR clock/124. 0110, 0111: Reserved When Bit 5 is set, you can achieve higher frequency of the MDC clock than the frequency limit of 2.5 MHz (specified in the IEEE Std 802.3) and program a clock divider of lower value. For example, when CSR clock is of 100 MHz frequency and you program these bits as 1010, then the resultant MDC clock is of 12.5 MHz which is outside the limit of IEEE 802.3 specified range. Program the following values only if the interfacing chips support faster MDC clocks. 1000: CSR clock/4 1001: CSR clock/6 1010: CSR clock/8 1011: CSR clock/10	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		1100: CSR clock/12 1101: CSR clock/14 1110: CSR clock/16 1111: CSR clock/18	
1	GW	GMII Write When set, this bit indicates to the PHY that this is a Write operation using the GMII Data register. If this bit is not set, it indicates that this is a Read operation, that is, placing the data in the GMII Data register.	RW
0	GB	GMII Busy This bit should read logic 0 before writing to Register 4 and Register 5. During a PHY or RevMII register access, the software sets this bit to 1'b1 to indicate that a Read or Write access is in progress. Register 5 is invalid until this bit is cleared by the MAC. Therefore, Register 5 (GMII Data) should be kept valid until the MAC clears this bit during a PHY Write operation. Similarly for a read operation, the contents of Register 5 are not valid until this bit is cleared. The subsequent read or write operation should happen only after the previous operation is complete. Because there is no acknowledgment from the PHY to MAC after a read or write operation is completed, there is no change in the functionality of this bit even when the PHY is not present.	RW[1]

Note:1. Only support RMII mode

2. [1]:This bits will operate with Write set, read clear function.

31.7.2.17 GMII Data Register(GMII_DR,0x0014)

	GNII_DR																															Base + 0x0014
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																GD															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	GD	GMII Data This Bits contains the 16-bit data value read from the PHY after a Management Read operation or the 16-bit data value to be written to the PHY before a Management Write operation.	RW

Note:

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Only support RMII mode

31.7.2.18 MAC Flow Control Register(MAC_FCR,0x0018)

	MAC_FCR																															Base+ 0x0018
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PT																Reserved								DZPQ	Reserved	PLT		UP	RFE	TFE	FCP/PBA
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:16	PT	Pause Time This Bits holds the value to be used in the Pause Time Bits in the transmit control frame. If the Pause Time bits is configured to be double-synchronized to the (G)MII clock domain, then consecutive writes to this register should be performed only after at least four clock cycles in the destination clock domain.	RW
15:8	Reserved	Writing has no effect, read as zero.	R
7	DZPQ	Disable Zero-Quanta Pause When this bit is set, it disables the automatic generation of the Zero-Quanta Pause frames on the de-assertion of the flow-control signal from the FIFO layer (MTL or external sideband flow control signal sbd_flowctrl_i/mti_flowctrl_i). When this bit is reset, normal operation with automatic Zero-Quanta Pause frame generation is enabled.	RW
6	Reserved	Writing has no effect, read as zero.	R
5:4	PLT	Pause Low Threshold This Bits configures the threshold of the Pause timer at which the input flow control signal mti_flowctrl_i (or sbd_flowctrl_i) is checked for automatic retransmission of the Pause frame. The threshold values should be always less than the Pause Time configured in Bits[31:16]. For example, if PT = 100H (256 slot-times), and PLT = 01, then a second Pause frame is automatically transmitted if the mti_flowctrl_i signal is asserted at 228 (256 - 28) slot times after the first Pause frame is transmitted. The following list provides the threshold values for different values: 00: The threshold is Pause time minus 4 slot times (PT - 4 slot times). 01: The threshold is Pause time minus 28 slot times (PT - 28 slot	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		times). 10: The threshold is Pause time minus 144 slot times (PT - 144 slot times). 11: The threshold is Pause time minus 256 slot times (PT - 256 slot times). The slot time is defined as the time taken to transmit 512 bits (64 bytes) on the GMII or MII interface.	
3	UP	Unicast Pause Frame Detect A pause frame is processed when it has the unique multicast address specified in the IEEE Std 802.3. When this bit is set, the MAC can also detect Pause frames with unicast address of the station. This unicast address should be as specified in the MAC Address0 High Register and MAC Address0 Low Register. When this bit is reset, the MAC only detects Pause frames with unique multicast address. **Note:** The MAC does not process a Pause frame if the multicast address of received frame is different from the unique multicast address.	RW
2	RFE	Receive Flow Control Enable When this bit is set, the MAC decodes the received Pause frame and disables its transmitter for a specified (Pause) time. When this bit is reset, the decode function of the Pause frame is disabled.	RW
1	TFE	Transmit Flow Control Enable In the full-duplex mode, when this bit is set, the MAC enables the flow control operation to transmit Pause frames. When this bit is reset, the flow control operation in the MAC is disabled, and the MAC does not transmit any Pause frames. In the half-duplex mode, when this bit is set, the MAC enables the backpressure operation. When this bit is reset, the backpressure feature is disabled.	RW
0	FCB_BPA	Flow Control Busy or Backpressure Activate This bit initiates a Pause frame in the full-duplex mode and activates the backpressure function in the half-duplex mode if the TFE bit is set. In the full-duplex mode, this bit should be read as 1'b0 before writing to the Flow Control register. To initiate a Pause frame, the Application must set this bit to 1'b1. During a transfer of the Control Frame, this bit continues to be set to signify that a frame transmission is in progress. After the completion of Pause frame transmission, the MAC resets this bit to 1'b0. The Flow Control register should not be written to until this bit is cleared. In the half-duplex mode, when this bit is set (and TFE is set), then backpressure is asserted by the MAC. During backpressure, when	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		the MAC receives a new frame, the transmitter starts sending a JAM pattern resulting in a collision. This control register bit is logically ORed with the mti_flowctrl_i input signal for the backpressure function. When the MAC is configured for the full-duplex mode, the BPA is automatically disabled.	

Note:

Only support RMII mode

31.7.2.19 MAC VLAN Tag Register(MAC_VTR,0x001C)

	MAC_VTR																															Base + 0x001C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved												VTHM	ESVL	VTIM	ETV	VL															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:20	Reserved	Writing has no effect, read as zero.	R
19	VTHM	VLAN Tag Hash Table Match Enable When set, the most significant four bits of the VLAN tag's CRC are used to index the content of Register 354 (VLAN Hash Table Register). A value of 1 in the VLAN Hash Table register, corresponding to the index, indicates that the frame matched the VLAN hash table. When Bit 16 (ETV) is set, the CRC of the 12-bit VLAN Identifier (VID) is used for comparison whereas when ETV is reset, the CRC of the 16-bit VLAN tag is used for comparison. When reset, the VLAN Hash Match operation is not performed.	RW
18	ESVL	nable S-VLAN When this bit is set, the MAC transmitter and receiver also consider the S-VLAN (Type = 0x88A8) frames as valid VLAN tagged frames.	RW
17	VTIM	VLAN Tag Inverse Match Enable When set, this bit enables the VLAN Tag inverse matching. The frames that do not have matching VLAN Tag are marked as matched. When reset, this bit enables the VLAN Tag perfect matching. The frames with matched VLAN Tag are marked as matched.	RW
16	ETV	Enable 12-Bit VLAN Tag Comparison	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		When this bit is set, a 12-bit VLAN identifier is used for comparing and filtering instead of the complete 16-bit VLAN tag. Bits [11:0] of VLAN tag are compared with the corresponding Bits in the received VLAN-tagged frame. Similarly, when enabled, only 12 bits of the VLAN tag in the received frame are used for hash-based VLAN filtering. When this bit is reset, all 16 bits of the 15th and 16th bytes of the received VLAN frame are used for comparison and VLAN hash filtering.	
15:0	VL	VLAN Tag Identifier for Receive Frames This Bits contains the 802.1Q VLAN tag to identify the VLAN frames and is compared to the 15th and 16th bytes of the frames being received for VLAN frames. The following list describes the bits of this Bits: Bits [15:13]: User Priority Bit 12: Canonical Format Indicator (CFI) or Drop Eligible Indicator (DEI) Bits[11:0]: VLAN tag's VLAN Identifier (VID) Bits When the ETV bit is set, only the VID (Bits[11:0]) is used for comparison. If VL (VL[11:0] if ETV is set) is all zeros, the MAC does not check the fifteenth and 16th bytes for VLAN tag comparison, and declares all frames with a Type Bits value of 0x8100 or 0x88a8 as VLAN frames.	RW

Note:Only support RMII mode

31.7.2.20 MAC Debug Register(MAC_DR,0x0024)

	MAC_DR																															Base + 0x0024
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved							TXFSTS	Reserved	TWCST	TRCSTS		TXPAUSED	TFCSTS		TPESTS	Reserved						RXFSTS		Reserved	RPCSTS		RWCSTS	Reserved	RFCFCSTS	RPESTS	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:25	Reserved	Writing has no effect, read as zero.	R
24	TXFSTS	MTL Tx FIFO Not Empty Status When high, this bit indicates that the MTL Tx FIFO is not empty and some data is left for transmission.	R
23	Reserved	Writing has no effect, read as zero.	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

22	TWCSTS	MTL Tx FIFO Write Controller Status When high, this bit indicates that the MTL Tx FIFO Write Controller is active and is transferring data to the Tx FIFO.	R
21:20	TRCSTS	MTL Tx FIFO Read Controller Status This Bits indicates the state of the Tx FIFO Read Controller: ▪ 00: IDLE state ▪ 01: READ state (transferring data to the MAC transmitter) ▪ 10: Waiting for Tx Status from the MAC transmitter ▪ 11: Writing the received Tx Status or flushing the Tx FIFO	R
19	TXPAUSED	MAC Transmitter in Pause When high, this bit indicates that the MAC transmitter is in the Pause condition (in the full-duplex-only mode) and hence does not schedule any frame for transmission.	R
18:17	TFCSTS	MAC Transmit Frame Controller Status This Bits indicates the state of the MAC Transmit Frame Controller module: 00: IDLE state 01: Waiting for status of previous frame or IFG or backoff period to be over 10: Generating and transmitting a Pause frame (in the full-duplex mode) 11: Transferring input frame for transmission	R
16	TPESTS	MAC GMII or MII Transmit Protocol Engine Status When high, this bit indicates that the MAC GMII or MII transmit protocol engine is actively transmitting data and is not in the IDLE state.	R
15:10	Reserved	Writing has no effect, read as zero.	R
9:8	RXFSTS	MTL Rx FIFO Fill-Level Status This Bits gives the status of the fill-level of the Rx FIFO: ▪ 00: Rx FIFO Empty ▪ 01: Rx FIFO fill-level below flow-control deactivate threshold ▪ 10: Rx FIFO fill-level above flow-control activate threshold ▪ 11: Rx FIFO Full	R
7	Reserved	Writing has no effect, read as zero.	R
6:5	RRCSTS	MTL Rx FIFO Read Controller State This Bits gives the state of the Rx FIFO read Controller: ▪ 00: IDLE state ▪ 01: Reading frame data ▪ 10: Reading frame status ▪ 11: Flushing the frame data and status	R
4	RWCSTS	MTL Rx FIFO Write Controller Active Status When high, this bit indicates that the MTL Rx FIFO Write Controller is	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		active and is transferring a received frame to the FIFO.	
3	Reserved	Writing has no effect, read as zero.	R
2:1	RFCFCSTS	MAC Receive Frame FIFO Controller Status When high, this Bits indicates the active state of the small FIFO Read and Write controllers of the MAC Receive Frame Controller Module.	R
0	RPESTS	MAC GMII or MII Receive Protocol Engine Status When high, this bit indicates that the MAC GMII or MII receive protocol engine is actively receiving data and not in IDLE state.	R

Note:

Only support RMII mode

31.7.2.21 LPI Control and Status Register(LPI_CSR,0x0030)

	LPI_CSR																															Base + 0x0030
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved												LPITXA	PLSEN	PLS	LPIEN	Reserved						RLPIST	TLPIST	Reserved				RLPIES	RLPIEN	TLPIES	TLPIEN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:20	Reserved	Writing has no effect, read as zero.	R
19	LPITXA	LPI TX Automate This bit controls the behavior of the MAC when it is entering or coming out of the LPI mode on the transmit side. If the LPITXA and LPIEN bits are set to 1, the MAC enters the LPI mode only after all outstanding frames (in the core) and pending frames (in the application interface) have been transmitted. The MAC comes out of the LPI mode when the application sends any frame for transmission or the application issues a TX FIFO Flush command. In addition, the MAC automatically clears the LPIEN bit when it exits the LPI state. If TX FIFO Flush is set in Bit 20 of Register 6 (Operation Mode Register), when the MAC is in the LPI mode, the MAC exits the LPI mode. When this bit is 0, the LPIEN bit directly controls behavior of the MAC when it is entering or coming out of the LPI mode.	R
18	PLSEN	PHY Link Status Enable This bit enables the link status received on the RGMII receive paths to be used for activating the LPILS TIMER. When set, the MAC uses the link-status bits of Register 54 (RGMII	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		Control and Status Register) and Bit 17 (PLS) for the LPI LS Timer trigger. When cleared, the MAC ignores the link-status bits of Register 54 and takes only the PLS bit.	
17	PLS	PHY Link Status This bit indicates the link status of the PHY. The MAC Transmitter asserts the LPI pattern only when the link status is up (okay) at least for the time indicated by the LPI LS TIMER. When set, the link is considered to be okay (up) and when reset, the link is considered to be down.	RW
16	LPIEN	LPI Enable When set, this bit instructs the MAC Transmitter to enter the LPI state. When reset, this bit instructs the MAC to exit the LPI state and resume normal transmission. This bit is cleared when the LPITXA bit is set and the MAC exits the LPI state because of the arrival of a new packet for transmission.	RW[1]
15:10	Reserved	Writing has no effect, read as zero.	R
9	RLPIST	Receive LPI State When set, this bit indicates that the MAC is receiving the LPI pattern on the GMII or MII interface.	R
8	TLPIST	Transmit LPI State When set, this bit indicates that the MAC is transmitting the LPI pattern on the GMII or MII interface.	R
7:4	Reserved	Writing has no effect, read as zero.	R
3	RLPIEX	Receive LPI Exit When set, this bit indicates that the MAC Receiver has stopped receiving the LPI pattern on the GMII or MII interface, exited the LPI state, and resumed the normal reception. This bit is cleared by a read into this register. **Note:** This bit may not get set if the MAC stops receiving the LPI pattern for a very short duration, such as, less than 3 clock cycles of HCLK clock.	R[2]
2	RLPIEN	Receive LPI Entry When set, this bit indicates that the MAC Receiver has received an LPI pattern and entered the LPI state. This bit is cleared by a read into this register. **Note:** This bit may not get set if the MAC stops receiving the LPI pattern for a very short duration, such as, less than 3 clock cycles of HCLK clock.	R[3]
1	TLPIEX	Transmit LPI Exit When set, this bit indicates that the MAC transmitter has exited the LPI state after the user has cleared the LPIEN bit and the LPI TW Timer has expired. This bit is cleared by a read into this register.	R[4]

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

0	TLPIEN	Transmit LPI Entry When set, this bit indicates that the MAC Transmitter has entered the LPI state because of the setting of the LPIEN bit. This bit is cleared by a read into this register.	R[5]

Note:

1. Only support RMII mode
2. [1]:This bits will operate with Self clear function.
3. [2]~[5]: This bits will operate with Self set , read clear function.

31.7.2.22 LPI Timers Control Register(LPI_TCR,0x0034)

	LPI_TCR																															Base + 0x0034
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved						LST										TWT															
RST	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:26	Reserved	Writing has no effect, read as zero.	R
25:16	LST	LPI LS TIMER This Bits specifies the minimum time (in milliseconds) for which the link status from the PHY should be up (OKAY) before the LPI pattern can be transmitted to the PHY. The MAC does not transmit the LPI pattern even when the LPIEN bit is set unless the LPI LS Timer reaches the programmed terminal count. The default value of the LPI LS Timer is 1000 (1 sec) as defined in the IEEE standard.	RW
15:0	TWT	LPI TW TIMER This Bits specifies the minimum time (in microseconds) for which the MAC waits after it stops transmitting the LPI pattern to the PHY and before it resumes the normal transmission. The TLPIEX status bit is set after the expiry of this timer.	RW

Note:

Only support RMII mode

31.7.2.23 MAC Interrupt Status Register(MAC_ISR,0x0038)

	MAC_ISR																															Base + 0x0038
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Reserved																				GPIIS	LPIIS	Reserved		MMCRXIPIS	MMCTXIS	MMCRXIS	MMCIS	PMTIS	Reserved		RGMII
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:12	Reserved	Writing has no effect, read as zero.	R
11	GPIIS	GPI Interrupt Status When the GPIO feature is enabled, this bit is set when any active event (LL or LH) occurs on the GPIS Bits (Bits [3:0]) of Register 56 (General Purpose IO Register) and the corresponding GPIE bit is enabled. This bit is cleared on reading lane 0 (GPIS) of Register 56 (General Purpose IO Register). When the GPIO feature is not enabled, this bit is reserved.	R
10	LPIIS	LPI Interrupt Status When the Energy Efficient Ethernet feature is enabled, this bit is set for any LPI state entry or exit in the MAC Transmitter or Receiver. This bit is cleared on reading Bit 0 of Register 12 (LPI Control and Status Register). In all other modes, this bit is reserved.	R
9:8	Reserved	Writing has no effect, read as zero.	R
7	MMCRXIPIS	MMC Receive Checksum Offload Interrupt Status This bit is set high when an interrupt is generated in the MMC Receive Checksum Offload Interrupt Register. This bit is cleared when all the bits in this interrupt register are cleared.	R
6	MMCTXIS	MMC Transmit Interrupt Status This bit is set high when an interrupt is generated in the MMC Transmit Interrupt Register. This bit is cleared when all the bits in this interrupt register are cleared.	R
5	MMCRXIS	MMC Receive Interrupt Status This bit is set high when an interrupt is generated in the MMC Receive Interrupt Register. This bit is cleared when all the bits in this interrupt register are cleared.	R
4	MMCIS	MMC Interrupt Status This bit is set high when any of the Bits [7:5] is set high and cleared only when all of these bits are low.	R
3	PMTIS	PMT Interrupt Status This bit is set when a magic packet or remote wake-up frame is received in the power-down mode (see Bits 5 and 6 in the PMT	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		Control and Status Register). This bit is cleared when both Bits[6:5] are cleared because of a read operation to the PMT Control and Status register.	
2:1	Reserved	Writing has no effect, read as zero.	R
0	RGMII	RGMII Interrupt Status This bit is set because of any change in value of the Link Status of RGMII interface.	R

Note:

Only support RMII mode

31.7.2.24 MAC Interrupt Mask Register(MAC_IMR,0x003C)

	MAC_IMR																															Base + 0x003C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																					LPIIM	Reserved						PMTIM	PCSANCIM	PCSLCHGIM	RGMII
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:11	Reserved	Writing has no effect, read as zero.	R
10	LPIIM	LPI Interrupt Mask When set, this bit disables the assertion of the interrupt signal because of the setting of the LPI Interrupt Status bit in Register 14 (Interrupt Status Register).	RW
9:4	Reserved	Writing has no effect, read as zero.	R
3	PMTIM	PMT Interrupt Mask When set, this bit disables the assertion of the interrupt signal because of the setting of PMT Interrupt Status bit in Register 14 (Interrupt Status Register).	RW
2	PCSANCIM	PCS AN Completion Interrupt Mask When set, this bit disables the assertion of the interrupt signal because of the setting of PCS Auto-negotiation complete bit in Register 14 (Interrupt Status Register).	RW
1	PCSLCHGIM	PCS Link Status Interrupt Mask When set, this bit disables the assertion of the interrupt signal because of the setting of the PCS Link-status changed bit in Register 14 (Interrupt Status Register).	RW
0	RGMII	RGMII Interrupt Mask When set, this bit disables the assertion of the interrupt signal	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		because of the setting of the RGMII Interrupt Status bit in Register 14 (Interrupt Status Register).	

31.7.2.25 MAC Address0 High Register(MAC_A0HR,0x0040)

	MAC_A0HR																															Base + 0x0040
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	AE	Reserved															ADDRHI															
RST	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Name	Description	R/W
31	AE	Address Enable This bit is always set to 1.	R
30:16	Reserved	Writing has no effect, read as zero.	R
15:0	ADDRHI	MAC Address0 [47:32] This Bits contains the upper 16 bits (47:32) of the first 6-byte MAC address. The MAC uses this Bits for filtering the received frames and inserting the MAC address in the Transmit Flow Control (Pause) Frames.	RW

Note:

Only support RMII mode

31.7.2.26 MAC Address0 LOW Register(MAC_A0LR,0x0044)

	MAC_A0LR																															Base + 0x0044
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ADDRLO																															
RST	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Name	Description	R/W
31:0	ADDRLO	MAC Address0 [31:0] This Bits contains the lower 32 bits of the first 6-byte MAC address. This is used by the MAC for filtering the received frames and inserting	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		the MAC address in the Transmit Flow Control (Pause) Frames.	

Note:

Only support RMII mode

31.7.2.27 MAC Address1 High Register(MAC_A1HR,0x0048)

	MAC_A1HR																															Base + 0x0048
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	AE	SA	MBC						Reserved								ADDRHI															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Name	Description	R/W
31	AE	Address Enable When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering.	RW
30	SA	Source Address When this bit is set, the MAC Address1[47:0] is used to compare with the SA bits of the received frame. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA Bits of the received frame.	RW
29:24	MBC	Mask Byte Control These bits are mask control bits for comparison of each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: Bit 29: Register 18[15:8] Bit 28: Register 18[7:0] Bit 27: Register 19[31:24] ... Bit 24: Register 19[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.	RW
23:16	Reserved	Writing has no effect, read as zero.	R
15:0	ADDRHI	MAC Address1 [47:32] This Bits contains the upper 16 bits (47:32) of the second 6-byte MAC	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		address.	

Note:

Only support RMII mode

31.7.2.28 MAC Address1 LOW Register(MAC_A1LR,0x004C)

	MAC_A1LR																															Base + 0x004C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ADDRLO																															
RST	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Name	Description	R/W
31:0	ADDRLO	MAC Address1 [31:0] This Bits contains the lower 32 bits of the second 6-byte MAC address. The content of this Bits is undefined until loaded by the Application after the initialization process.	RW

Note: Only support RMII mode

31.7.2.29 MAC Watchdog Timeout Register(MAC_WTR,0x00DC)

	MAC_WTR																															Base + 0x00DC
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved															PWE	Reserved		WTO													
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:17	Reserved	Writing has no effect, read as zero.	R
16	PWE	Programmable Watchdog Enable When this bit is set and Bit 23 (WD) of Register 0 (MAC Configuration Register) is reset, the WTO Bits (Bits[13:0]) is used as watchdog timeout for a received frame. When this bit is cleared, the watchdog timeout for a received frame is controlled by the setting of Bit 23 (WD) and Bit 20 (JE) in Register 0 (MAC Configuration Register).	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

15:14	Reserved	Writing has no effect, read as zero.	R
13:0	WTO	Watchdog Timeout When Bit 16 (PWE) is set and Bit 23 (WD) of Register 0 (MAC Configuration Register) is reset, this Bits is used as watchdog timeout for a received frame. If the length of a received frame exceeds the value of this Bits, such frame is terminated and declared as an error frame. **Note:** When Bit 16 (PWE) is set, the value in this Bits should be more than 1,522 (0x05F2). Otherwise, the IEEE Std 802.3-specified valid tagged frames are declared as error frames and are dropped.	RW

Note:

Only support RMII mode

31.8 Operation Flow

Figure 31-2 GMAC configure flow

Note: Only support RMII mode.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

32 Controller Area Network (CAN)

32.1 Overview

The CAN 2.0B IP is a stand-alone Controller Area Network (CAN) protocol controller. It supports CAN 2.0B standard and the maximal bit rate is 1 Mb/s. It is capable of transmitting and receiving standard and extended message frames. It includes the double-buffer transmit buffers and 64-byte receive FIFO with 4 ID acceptance filtering and message management. The MCU communication is implemented via the AHB-Lite and DMA function.

32.2 Features

- Support CAN 2.0B protocol in ISO-11898-1:2003
- Arbitration Bit Rate up to 1Mbps
- Support CAN 2.0A Standard 11-bit and CAN 2.0B Extended 29-bit ID
- 8-byte Transmit Double Buffer
- Built-in 4-byte SRAM as Receive FIFO for maximal 4 received frames
- Four Receive Acceptance ID Filters and Mask
- Bus Error Handling and Auto-Recovery
- Listen-Only mode
- Self-Test mode
- Self-Loop Test Mode

32.3 Brief Introduction

The Controller Area Network (CAN) is a serial asynchronous bus allowing multi-master communications. The CAN bus uses a single terminated twisted pair with maximum data rate of 1Mbps. Typical length of the bus can be up to 40 meters. One unusual aspect of the CAN protocol is its message based nature. Nodes on the bus do not have specific address instead the messages have unique identifiers which are used for determining its priority. Each node depending on its functionality transmits specific types of messages and also responds to specific related messages. CAN is especially popular in connecting electronic control modules, sensors, actuators in automotive and industrial applications because its simple bus structure and fault-tolerant capability from extensive error checking.

The physical media of typical CAN bus is a twisted pair terminated with 120Ohm on both ends. The twisted pair has two signals, CANH and CANL. CANH and CANL forms a 5V pseudo differential signal thus have reliable transmissions even under high noise environment. There are two possible logic states on the bus. Dominant state (logic 0) is when CANH is actively pulled to 5V and CANL is actively pulled to 0V. Recessive state (logic 1) is when the bus is not actively driven and both CANH and CANL are pulled toward 2.5V by the termination resistors. The bus also exhibits the wire-AND characteristics, that is bus is in recessive state if only if all nodes are recessive, and bus is in dominant state if one or more nodes are dominant. Because of this pseudo differential nature, it is possible to maintain correct data transmission even if one of the wires is broken. To drive the CAN bus, typically an external transceiver is used to

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

provide isolated drive.

Figure 32-1 CAN Bus

The CAN protocol is a modified version of Carrier Sense Multiple Access/Collision Avoidance (CSMA/CA) similar to Ethernet. If two nodes are trying to send at the same time, instead of collision avoidance, the ID field of message will resolve itself which allows the higher priority message to continue and lower priority message been postponed. The typical standard CAN frame format and extended format are shown in the following.

Figure 32-2 SFF and EFF

The frame starts with a bit 0 of Start of Frame (SOF), and followed by an 11-bit ID field. Because the dominant state transmitted by one node will overwrite any other nodes transmitting recessive state, the message ID with lowest number will win the bus arbitration. After arbitration, RTR bit indicate whether this is a transmit message (RTR=0), or a Remote Transmission Request (RTR=1) message. R1 and R0 are two reserve bits which should both be 0. The Data Length Code (DLC) indicates the byte count of following data. DLC must be less than 9. After data field, a 15-bit CRC is appended, and a CRC delimiter is the last bit of CRC field. The receive node will acknowledge the successful reception by sending 0 during the ACK slot. An ACK delimiter and along with minimum 7 bit time of EOF field is ensured for the bus to enter into bus IDLE state. And a minimum 3 BT (typically implemented as 7 BT) of recessive state and bus IDLE state should be used for inter-frame spacing.

The message format can be further categorized into standard (SFF) or extended format (EFF). The difference in SFF and EFF is in IDE bit. If IDE=dominant, the message is SFF, and if

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

IDE=recessive, the message is EFF. The extended format provides 29-bit ID addressing whit the additional 18 bit ID following the IDE bit. In terms of purpose of message, the message can be considered as either data frame or remote frame. A data frame carries data sent by the transmitter to receivers (plural here). A remote frame is transmitted by a node to request other nodes to respond with data frame using same message ID. Both data frame and remote frame can take either standard or extended format.

CAN bus uses NRZ coding. To ensure enough edges for synchronization, Bit-Stuffing is used. An opposite polarity bit is inserted after 5 consecutive bits of the same level. Bit-Stuffing starts with SOF and ends with CRC (before CRC delimiter). The initial falling edge of SOF provides a hard synchronization on the start of the message.

CAN bus include many error checking mechanisms to ensure reliable operations. This includes CRC checking built-in in the message frame. CRC is calculated over the non-stuffed bit stream data starting with SOF and ends with last bit of data field. In case of CRC mismatch, the frame is discarded, and ACK bit is not responded. Nodes on the bus will also detect frame format error, bit stuffing errors. All these error been detected, a node will transmit an error frame. The error frame consists of 6 consecutive dominant bits as error flag and may be extended to 12 bits when multiple nodes are responding to the same error. This violation of bit-stuffing (more than 5 consecutive same bits) will ensure all nodes on the bus will detect the error and the error flag thus might be further extended up 12 bit times by those nodes detecting the same error. After error flag, the error frame is terminated with minimum 3 bit time of recessive state as error delimiter. Another special frame with the same format as error frame is the overload frame which is sent by a receiving node in response to a remote request message when this node cannot meet the response requirement. Overload frame is also sent by nodes when detecting a violation of frame intermission rule (each frame must be separated by 3 bit time of recessive bits).

There are three fundamental states for error handling in each CAN node. This is shown in the following state diagram. REC is receive error count, and TEC is transmit error count.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Figure 32-3 Error State

The node is in normal operation when in Error Active state. In this state, the node can send all frames including active error flag with six consecutive 'dominant' bits. When error count reaches 127, it enters Error Passive states, and the node can send all frames and passive error flag with six consecutive 'recessive' bits. When error count exceeds 255, the node enters Bus Off state and is isolated from the bus. This mechanism ensures a faulty node does cause bus dead-lock. The exit of Bus Off state can only be done by re-initialization or if auto recovery is enabled when 128 occurrence of 11 consecutive recessive bit.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

32.4 Block Diagram

Figure 32-4 CAN 2.0B Block Diagram

32.5 Pin Description

Table 32-1 CAN 2.0B PinsDescription

Name	I/O	Description
rx_i	I	CAN RX input from CAN transceiver
tx_o	O	CAN TX output to CAN transceiver

32.6 Register Description

Following chapter will descript the functions of all software accessible registers.

Conventions:

5. Register Address = Base + Address offset
6. The registers can be read and written by AHB2 bus
7. Register read/write attribute

R - Read only

W - Write only

RW - read and write

RCW - read and write, but clear to 0 by read

RSW - read and write, but set to 1 by read

RWC - read and write, clear to 0 by write 1, write 0 has no effect

RWS - read and write, set to 1 by write 1, write 0 has no effect

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

RC - read only, and clear to 0 by read

RS - read only, and set to 1 by read

SPEC - special access method, relate to its description

8. Reset Value

1 - reset to 1

0 - reset to 0

? - value unknown after reset

32.6.1 Registers Mapping

Table 32-2 Registers Memory Map Base Address

Name	Base	Description
CAN0	0x13560000	Address base of CAN0
CAN1	0x13570000	Address base of CAN1

Table 32-3 CAN Memory Map-Address Offset

Name	Addr Offset	Description	RW	Reset
CANMODE	0x00	CAN mode configuration register	RW	0x1
CANCMD	0x04	CAN command register	W	0x0
CANSTAT	0x08	CAN status register	R	0x11C
CANINT	0x0C	CAN interrupt flag and enable register	RW	0x0
CANBTR	0x10	CAN bus timing register	RW	0x6701
CANFLT	0x18	CAN filter register	RW	0xF
CANERR	0x1C	CAN error information register	RW	0x6000
CANAFID0	0x20	CAN acceptance filter0 ID	RW	0x0
CANAFMK0	0x24	CAN acceptance filter0 MASK	RW	0x0
CANAFID1	0x28	CAN acceptance filter1 ID	RW	0x0
CANAFMK1	0x2C	CAN acceptance filter1 MASK	RW	0x0
CANAFID2	0x30	CAN acceptance filter2 ID	RW	0x0
CANAFMK2	0x34	CAN acceptance filter2 MASK	RW	0x0
CANAFID3	0x38	CAN acceptance filter3 ID	RW	0x0
CANAFMK3	0x3C	CAN acceptance filter3 MASK	RW	0x0
CANTFIR	0x40	CAN transmit frame information register	RW	0x0
CANTXID	0x44	CAN transmit identifier register	RW	0x0
CANTXDATA0	0x48	CAN transmit DATA 0 register	RW	0x0
CANTXDATA1	0x4C	CAN transmit DATA 1 register	RW	0x0
CANRFIR	0x90	CAN receive frame information register	R	0x0
CANRXID	0x94	CAN receive identifier register	R	0x0
CANRXDATA0	0x98	CAN receive DATA 0 register	R	0x0
CANRXDATA1	0x9C	CAN receive DATA 1 register	R	0x0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

CANSL	0xFC	CAN self-loop register	RW	0x0

32.6.2 Register and Fields Description

32.6.2.1 Configuration, Control and Status Registers

32.6.2.1.1 CAN Mode Configuration Register (CANMODE, 0x00)

	CANMODE																															Base + 0x00
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																	RXCNT4	TXAR	Reserved			SLEEP	DMAEN	Reserved				ERAR	STE	LOM	RSTM
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Name	Description	RW
31:15	Reserved	Writing has no effect, read as zeros.	R
14	RXCNT4	RX entry count is always 4 words. Set RXCNT4 to 1 to indicate that RX entry count is always 4 words. This register can only be modified in reset mode (RSTM=1).	RW
13	TXAR	TX auto request. Set TXAR to 1 to indicate that request a transmission when access CANTXDATA1. This register can only be modified in reset mode (RSTM=1).	RW
12:10	Reserved	Writing has no effect, read as zeros.	R
9	SLEEP	SLEEP Mode Set SLEEP to 1 to indicate that CAN Controller is going to enter the SLEEP mode. This register is used to enable the CAN bus wakeup detector. Hardware will clear this register automatically when detect the rx_i falling edge from CAN transceiver. Meanwhile, if the WKIE is set, the WKI interrupt will be issued. In order to detect the valid wakeup signal from CAN bus, this register shall be programed during CAN bus idle (rx_i is voltage high). This register can only be modified in reset mode (RSTM=1).	RW
8	DMAEN	RX DMA Mode Enable DMAEN=1 enable RX DMA mode DMAEN=0 disable RX DMA mode This register can only be modified in reset mode (RSTM=1).	RW
7:4	Reserved	Writing has no effect, read as zeros.	R
3	ERAR	Error Auto Recovery ERAR=1 will allow auto recovery from bus off state	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		When this bit is set, auto recovery from Bus Off state to Error Active state is enabled. The auto recovery condition is met when 128 occurrences of bus-free time (11 consecutive 'recessive' bits) is received. When exiting the Bus Off state, TEC and REC are cleared to 0 by hardware if ERAR=1. ERAR=0 for disable the auto recovery function. If ERAR=0, software must clear REC and TEC to exit of Bus Off state to Error Active state. Please note in the entry of Bus Off state, if ERAR=0, RSTM will be set by hardware, so modification of REC and TEC is allowed. After clearing REC and TEC, the software must also clear RSTM bit to return to normal operation. This register can only be modified in reset mode (RSTM=1).	
2	STE	Self-Test Enable STE=1 enables self-test mode. When STE=1, the only difference from normal operation mode is that all ACK errors are ignored. STE=0 for normal mode operation This register can only be modified in reset mode (RSTM=1)	RW
1	LOW	Listen-Only Mode LOM=1 will set the CAN controller as listen-only mode When LOM=1, CAN controller will work in Listen-Only mode. In this mode, the CAN controller will only perform receiver functions and does not engage any transmission (including ACK signaling). All other functions can be used like in Operating mode. In this mode, the error counters are stopped at the current value and message transmission is not possible. But when detecting bus error, listen-only mode will still transmit error frame. LOM=0 for normal mode operation This register can only be modified in reset mode (RSTM=1).	RW
0	RSTM	Reset Mode RSTM=1 will force the CAN Controller into rest mode regardless of other setting, and will initialize all state machine. It does not affect the register contents. RSTM defaults to 1 after system reset. RSTM is set to 1 by hardware when entering into Bus-Off state if ERAR=0. RSTM must be cleared to 0 to allow the CAN Controller into normal operation. Please note RSTM must be set to 1 first in order to modify the other registers in CANMODE. The write cycle of RSTM must be preceding the modification cycles of PHYOFF, ERAR, STE, and LOM	RW

32.6.2.1.2 CAN Command Register (CANCMD, 0x04)

	CANCMD																															**Base + 0x04**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Reserved																									CTB	OFR	SRR	CDO	RRB	AT	TR
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:7	Reserved	Writing has no effect, read as zeros.	R
6	CTB	Clear Transmit Buffer Set CTB=1 will cancel the unexecuted Transmit Request (TR) command and release the transmit buffer for any message revision. This command is only valid when the transmit buffer is occupied by an unsent message with TBS=0. This bit is self-cleared by hardware when TBS is set. Since CTB is only cancel the unexecuted transmission in the transmit buffer, the extra AT command is necessary to abort the pending transmission in CAN MAC controller if you are going to abort all transmissions.	W
5	OFR	Overload Frame Request OFR=1 will request transmitting an overload frame. The overload frame is transmitted the first bit time of next expected INTERMISSION. This bit is self-cleared by hardware after the overload frame is transmitted. Since the overload frame will be transmitted regardless of the bus condition, no interrupt is generated at the completion.	W
4	SRR	Self Receive Request SRR=1 will result a message be transmitted and received simultaneously. Upon self reception request command, a message is transmitted and simultaneously received if the acceptance filter is set to the corresponding identifier. This command is used mainly for self test of the controller. If STE=1 which enables the self test mode, the transmit and receive can be successful without other nodes present. This bit is self cleared by hardware when transmit and receive operations are completed and both transmit and receive interrupts will be generated. SRR is only valid when both CTB=0 and TR=0.	W
3	CDO	Clear Data Overrun CDO=1 will clear data overrun status bit. This command bit is used to clear the data overrun condition indicated by the data overrun status bit. This command bit is self cleared by hardware.	W
2	RRB	Release Receive Buffer After reading the contents of the receive buffer, the CPU can release this memory space in the RX-FIFO by setting the Release Receive Buffer bit to logic 1. This may result in another message becoming immediately available within the receive buffer. If there is no other message available,	W

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		the Receive Buffer Status (RBS) bit is reset. RRB is relevant only when DMAEN=0.	
1	AT	Abort Transmitting AT=1 will abort the any pending transmission request. AT does not stop an on-going message transmission. But the next transmission attempt will be aborted. The completion of the abortion will cause TCS=1 in CANSTAT register. AT should be used only for aborting a message transmission with errors (mostly in ACK error). As AT can not guarantee to stop an on-going message transmission, the software should check Bus Error Flag (BEI) bit and Arbitration Lost Flag (ALI) when TCS=1. TCS=1 can be resulted by either abortion or success of transmission. If BEI=0 and ALI=0, then the message is sent successfully even abort command is issued. Otherwise the transmission was actually aborted because of bus error or arbitration lost.	W
0	TR	Transmit Request TR=1 will start the transmit process of the message in the transmit buffer. While setting TR =1, the message in the transmit buffer including CANTFIR, CANTXID will be delivered to CAN MAC controller for transmit process if the CAN bus was idle. When the message is delivered to CAN MAC controller, the transmit buffer will be free for next message from CPU. Meanwhile the TBS and the TBI will be set to notice Users. TR is only valid when CTB=0.	W

32.6.2.1.3 CAN Status Register (CANSTAT, 0x08)

	CANSTAT																															Base + 0x08
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																							TBF	BOS	ES	TR	RS	TCS	TBS	DOS	RBS
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:9	Reserved	Writing has no effect, read as zeros.	R
8	TBF	Transmit Buffer Free TBF=1 indicates the transmit buffer is free and a new message can be written. TBF=0 indicates the transmit buffer is locked and the content in the transmit buffer is either waiting for transmission or in the process of being transmitted. And no new message could be written.	R
7	BOS	Bus Off State Status	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		BOS=1 indicates the CAN controller is in the Bus Off State. BOS=0 indicates the CAN controller is involved in bus activities. Bus Off state is defined in the error handling state diagram. Possible exit of Bus Off state is by Bus Auto recovery, or by writing a value less than 255 into TEC under reset mode.	
6	ES	Error Status ES=1 indicates at least one of the error counters has reached or exceeded the warning limit defined by the CANEWLR. ES=0 indicates warning limits are not exceeded. Errors detected during reception or transmission will affect the error counters according to the CAN 2.0B protocol specification. ES is set when at least one of the error counters has reached or exceeded the warning limit setting (CANEWLR). An error warning interrupt is generated, if enabled. The default value of CANEWLR after hardware reset is 0x60.	R
5	TS	Transmit Status TS=1 indicates CAN controller is transmitting a message.	R
4	RS	Receive Status RS=1 indicates CAN controller is receiving a message. If both TS and RS are 0, the CAN controller is idle.	R
3	TCS	Transmit Complete Status TCS=1 indicates last requested message transmission has been successfully completed. TCS is cleared to 0 when TR or SRR command is issued. And TCS is set to 1 by hardware when the message is sent successfully. TCS remains to be 0 during the message transmission, and TCS is set to 1 by hardware if the message is sent successfully. Please note TCS=1 can also be resulted by AT command.	R
2	TBS	Transmit Buffer Status TBS=1 indicates the transmit buffer is free and a new message can be written. TBS=0 indicates the transmit buffer is locked and the content in the transmit buffer is either waiting for transmission or in the process of being transmitted. And no new message could be written.	R
1	DOS	Data Overrun Status DOS=1 indicates a received message was lost due to RX-FIFO overrun. The overrun interrupt is generated with DOI flag set. DOS must be cleared by setting CDO (Clear Data Overrun) command bit or by setting to reset mode.	R
0	RBS	Receive Buffer Status RBS=1 indicates one or more valid messages are available in RX-FIFO. RBS is cleared when the RX-FIFO is empty.	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

32.6.2.1.4 CAN Interrupt Register (CANINT, 0x0C)

	CANINT																															Base + 0x0C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				OFIE	TBIE	DMAIE	WKIE	BEIE	ALIE	EPIE	BOIE	DOIE	EIT	TIE	RIE	Reserved				OFI	TBI	DMAI	WKI	BEi	ALI	EPI	BOI	DOI	EI	TI	RI
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:28	Reserved	Writing has no effect, read as zeros.	R
27	OFIE	Overload Frame Interrupt Enable	RW
26	TBIE	Transmit Buffer Free Interrupt Enable	RW
25	DMAIE	RX DMA Complete Interrupt Enable	RW
24	WKIE	Wake Up Interrupt Enable	RW
23	BEIE	Bus Error Interrupt Enable	RW
22	ALIE	Arbitration Lost Interrupt Enable	RW
21	EPIE	Error Passive Interrupt Enable	RW
20	BOIE	Bus Off Interrupt Enable	RW
19	DOIE	Data Overrun Interrupt Enable	RW
18	EIE	Error Warning Interrupt Enable	RW
17	TIE	Transmit Interrupt Enable	RW
16	RIE	Receive Interrupt Enable	RW
15:12	Reserved	Writing has no effect, read as zeros.	R
11	OFI	Overload Frame Interrupt Flag OFI is set when CAN controller detects or issues an overload frame on the CAN-bus. OFI is cleared when read. OFIE bit must be set to enable OFI function.	R
10	TBI	Transmit Buffer Free Interrupt Flag TBI is set when Transmit Buffer is free for new message. The transmit buffer including CANTFIR and CANTXID are double buffers. TBS and TBI indicate the transmit buffer is free to accept a new message from CPU. TBI is cleared when read. TBIE bit must be set to enable TBI function.	R
9	DMAI	RX DMA Complete Interrupt Flag DMAI is set when receive dma_finsih signal under RX DMA mode. DMAI is cleared when read. Both DMAEN and DMAIE must be set to enable DMAI function.	R
8	WKI	Wake Up Interrupt Flag WKI is set when the CAN controller detects a dominant bit on the CAN-bus	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		in the SLEEP mode (SLEEP=1). WKI is cleared when read. Both WKIE and SLEEP bit must be set to enable the WKI function. This interrupt can notice and wake up the controller from CAN-bus.	
7	BEI	Bus Error Interrupt Flag BEI is set when the CAN controller detects error(s) on the CAN-bus. The error types include format error, bit stuff error, bit error (when data or CRC transmitted does not match with received), CRC error, and ACK error. The BEIE bit must be set to enable the BEI function.	R
6	ALI	Arbitration Lost Interrupt ALI is set when a message was not sent successfully due to loss of arbitration. The ALIE bit must be set to enable the ALI function.	R
5	EPI	Error Passive Interrupt EPI is set when the CAN controller enters the error passive state, or the CAN controller is already in the error passive state and enters the error active state. EPIE bit must be set to enable EPI function.	R
4	BOI	Bus Off State Interrupt BOI is set when the CAN controller in the bus off state or equivalently BOS=1. Since BOI and BOS is 1 whenever in Bus Off state, the software must take care to disable BOIE when entering BOI ISR and then correct the BOS status otherwise the interrupt will occur indefinitely. BOIE bit must be set to enable BOI function.	R
3	DOI	Data Overrun Interrupt DOI is set when a received message was lost due to RX-FIFO overrun. The function is equivalently when DOS changes from 0 to 1. DOIE bit must be set to enable DOI function. DOI is cleared when read.	R
2	EI	Error Warning Interrupt EI is set on when REC or TEC is greater or equal to the CANEWLR setting or equivalently when ES changes from 0 to 1. EIE bit must be set to enable EI function.	R
1	TI	Transmit Interrupt TI is set whenever the transmit buffer becomes free or equivalently the transmission of the message has finished and TBS changes from 0 to 1. TIE bit must be set to enable TI function.	R
0	RI	Receive Interrupt RI is set when a new message has been put into the RX-FIFO by the CAN controller. RI is cleared when read. RIE bit must be set to enable RI function.	R

32.6.2.1.5 CAN Bus Timing Register (CANBTR, 0x10)

	CANBTR																															**Base + 0x10**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Reserved1																SAW	TSEG2[2-0]			TSEG1				SJW[1-0]		CANCS[5-0]					
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	1	1	0	0	1	1	1	0	0	0	0	0	0	0	1

Bits	Name	Description	RW
31:7	Reserved	Writing has no effect, read as zeros.	R
15	SAW	SAW=1 will use triple-sampling method. The triple-sampling method uses three instances between TSEG1 and TSEG2 as show in the following timing diagram. The data is determined by the majority of the sampled results. SAM=0 will use single-sample method. The single-sampling occurs at the time instance between TSEG1 and TSEG2.	RW
14:12	TSEG2[2-0]	TSEG2[2-0] defines the bit time component 2. TSEG2 = TSEG2[2-0] + 1.	RW
11:8	TSEG1[3-0]	TSEG1[3-0] defines the bit time component 1. TSEG1 = TSEG1[3-0] + 1.	RW
7:6	SJW[1-0]	Synchronization Jump Length This defines the maximum adjustment in TQCLK period units for re-synchronization. The receiver uses the falling edges to determine the physical delay of the network. The synchronization is achieved by inserting a delay compensation segment in the bit time after SYNC SEG and thus also delays the sampling points of the local receiver. SJW[1-0]+1 is used to set the maximum allowed delay segment in TQCLK period.	RW
5:0	CANCS[5-0]	CANCS[5-0] defines the CAN Controller Clock The CAN controller clock TQCLK = CANCLK/(CANCS[5-0]+1). This defines the CAN Time Quanta (TQCLK) from the CAN system clock.	RW

A CAN bit time is partitioned by TQCLK periods as the following diagram. The first CAN TQCLK period is used for edge synchronization, and TSEG1 is used for defining the sampling edge. For SAM=0, the sampling edge is the first edge of TSEG2. For SAM=1, the sampling edges are the last two edges of TSEG1, and the first edge of TSEG2. For typical CAN bus design, TSEG1 and TSEG2 is organized for sampling at the last two quanta (period of TQCLK).

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Figure 32-5 Timing Diagram

CAN baud rate is thus can be calculated as TQCLK/((TSEG2[2-0]+1)+(TSEG1[3-0]+1)+1). Or in terms of CANCLK,CANCLK/(CANCS[5-0]+1)/{(TSEG2[2-0]+1)+(TSEG1[3-0]+1)+1}. Also note, with re-synchronization, a delay compensation segment is inserted between SYNC SEG and TSEG1. The maximum length of delay compensation segment is limited by SJW[1-0].

32.6.2.1.6 CAN Filter Register (CANFLT, 0x18)

There are four Acceptance Filters for message ID matching.

CANFLT.FTER0 ~ CANFLT.FTER3 control the enabling of each filter and multiple filters.

CANFLT.FTER0 ~ CANFLT.FTER3 can be modified only in reset mode(CANMODE.RSTM=1) and appears as read-only in normal operating mode.

CANFLT.FMS[0] ~ CANFLT.FMS[3] are read-only and the corresponding match bit is set to 1 when a match condition occurs for the acceptance filer.

CANFLT.ALC0 ~ CANFLT.ALC4 are read only and report the bit locations of a lost arbitration when transmitting a message.

	CANFLT																															**Base + 0x18**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved1											ALC4	ALC3	ALC2	ALC1	ALC0	Reserved				FMS[3]	FMS[2]	FMS[1]	FMS[0]	Reserved				FTER3	FTER2	FTER1	FTER0
RST	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Bits	Name	Description	RW
31:21	Reserved	Writing has no effect, read as zeros.	R
20	ALC4	These bits are read only and report the bit locations of a lost arbitration when transmitting a message. The following table defines the corresponding relationship.	R
19	ALC3		R
18	ALC2		R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

17	ALC1		R
16	ALC0		R
15:12	Reserved	Writing has no effect, read as zeros.	R
11	FMS[3]	Acceptance Filter 3 Match Status FSM[3]=1 Acceptance Filter 3 match FSM[3]=0 Acceptance Filter 3 not match	R
10	FMS[2]	Acceptance Filter 2 Match Status FSM[2]=1 Acceptance Filter 2 match FSM[2]=0 Acceptance Filter 2 not match	R
9	FMS[2]	Acceptance Filter 1 Match Status FSM[1]=1 Acceptance Filter 1 match FSM[1]=0 Acceptance Filter 1 not match	R
8	FMS[0]	Acceptance Filter 0 Match Status FSM[0]=1 Acceptance Filter 0 match FSM[0]=0 Acceptance Filter 0 not match	R
7:4	Reserved	Writing has no effect, read as zeros.	R
3	FTER3	Acceptance Filter 3 Enable FTER3=1 enables Acceptance Filter 3	RW
2	FTER2	Acceptance Filter 2 Enable FTER2=1 enables Acceptance Filter 2	RW
1	FTER1	Acceptance Filter 1Enable FTER1=1 enables Acceptance Filter 1	RW
0	FTER0	Acceptance Filter 0 Enable FTER0=1 enables Acceptance Filter 0	RW

Table 32-4 Bit Locations of a Lost Arbitration when Transmission

Bits					Decimal Value	Description
ALC4	ALC3	ALC2	ALC1	ALC0		
0	0	0	0	0	0	Arbitration lost in bit ID28
0	0	0	0	1	1	Arbitration lost in bit ID27
0	0	0	1	0	2	Arbitration lost in bit ID26
0	0	0	1	1	3	Arbitration lost in bit ID25
0	0	1	0	0	4	Arbitration lost in bit ID24
0	0	1	0	1	5	Arbitration lost in bit ID23
0	0	1	1	0	6	Arbitration lost in bit ID22
0	0	1	1	1	7	Arbitration lost in bit ID21
0	1	0	0	0	8	Arbitration lost in bit ID20
0	1	0	0	1	9	Arbitration lost in bit ID19

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits					Decimal Value	Description
ALC4	ALC3	ALC2	ALC1	ALC0		
0	1	0	1	0	10	Arbitration lost in bit ID18
0	1	0	1	1	11	Arbitration lost in bit SRTR (Note 1)
0	1	1	0	0	12	Arbitration lost in bit IDE
0	1	1	0	1	13	Arbitration lost in bit ID17 (Note 2)
0	1	1	1	0	14	Arbitration lost in bit ID16 (Note 2)
0	1	1	1	1	15	Arbitration lost in bit ID15 (Note 2)
1	0	0	0	0	16	Arbitration lost in bit ID14 (Note 2)
1	0	0	0	1	17	Arbitration lost in bit ID13 (Note 2)
1	0	0	1	0	18	Arbitration lost in bit ID12 (Note 2)
1	0	0	1	1	19	Arbitration lost in bit ID11 (Note 2)
1	0	1	0	0	20	Arbitration lost in bit ID10 (Note 2)
1	0	1	0	1	21	Arbitration lost in bit ID9 (Note 2)
1	0	1	1	0	22	Arbitration lost in bit ID8 (Note 2)
1	0	1	1	1	23	Arbitration lost in bit ID7 (Note 2)
1	1	0	0	0	24	Arbitration lost in bit ID6 (Note 2)
1	1	0	0	1	25	Arbitration lost in bit ID5 (Note 2)
1	1	0	1	0	26	Arbitration lost in bit ID4 (Note 2)
1	1	0	1	1	27	Arbitration lost in bit ID3 (Note 2)
1	1	1	0	0	28	Arbitration lost in bit ID2 (Note 2)
1	1	1	0	1	29	Arbitration lost in bit ID1 (Note 2)
1	1	1	1	0	30	Arbitration lost in bit ID0 (Note 2)
1	1	1	1	1	31	Arbitration lost in bit RTR (Note 2)

Note 1: Bit RTR for standard frame messages.

Note 2: Extended frame messages only.

On arbitration lost, the corresponding arbitration lost interrupt is generated. At the same time, the current bit position of the bit stream processor is captured into the Arbitration Lost Capture register. The content in this register is locked until the software read out its contents. The capture mechanism is then activated again. The corresponding interrupt flag located in the interrupt register is cleared during the read access to the interrupt flag register. A new arbitration lost interrupt is not possible until the arbitration lost capture register is read out. The following diagram shows the bit locations of the arbitration lost. And an ALC=0x08 is shown as an example, where arbitration lost is detected when outputting a recessive bit but receiving a dominant bit at ID20.

32.6.2.1.7 CAN Error Register (CANERR, 0x1C)

CANERR[7:0] are read-only and always keep the last error status on CAN bus.

CANERR[15:8] set the warning limit for the error counter.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

CANERR[23:16] denote receive error count.

CANERR[31:24] denote transmit error count.

	CANERR																															Base + 0x1C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CANTEC[7-0]								CANREC[7-0]								CANEWLR[7-0]								ERRC[1]	ERRC[0]	DIR	SEG[4]	SEG[3]	SEG[2]	SEG[1]	SEG[0]
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:24	CANTEC[7-0]	**These bits denote transmit error count.** These bits are modifiable in reset mode (CANMODE.RSTM = 1) and appear as read-only in normal operating mode. CANTEC contains the current error count, and is initialized as 0 after hardware rest. If a bus-off event occurs, the transmit error counter is initialized to 128 if auto-recovery is not enabled. The software can just use the reset mode to allow recovery to the normal error-active state.	RW
23:16	CANREC[7-0]	**These bits denote receive error count.** This register are modifiable in reset mode (CANMODE.RSTM=1) and appears as read-only in normal operating mode. CANREC contains the current error count. When the controller enters bus-off state, CANREC is re-initialized as 0, and during bus-off, the writing to CANREC has no effect.	RW
15:8	CANEWLR[7-0]	**These bits denote error warning limit.** These bits are modifiable in reset mode (CANMODE.RSTM=1) and appears as read-only in normal operating mode. These bits set the warning limit for the error counter. When CANREC or CANTEC value exceed CANEWLR value, an error warning interrupt is generated, and the EI flag is set in the interrupt flag register. CANEWLF defaults to 0x60 after hardware reset.	RW
7	ERRC[1]	Error Code.	R
6	ERRC[0]	These two bits reflect the error type as defined in the following table.	R

ERRC[1]	ERRC[0]	Descriptions
0	0	Bit error
0	1	Form error

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		1	0	Stuff error	
		1	1	Other types of error	
5	DIR	Direction of Transfer Error DIR=1 means errors occurred during reception DIR=0 means errors occurred during transmission			R
4	SEG[4]	Error Locations. The following table defines the function.			R
3	SEG[3]				R
2	SEG[2]				R
1	SEG[1]				R
0	SEG[0]				R

Table 32-5 Error Locations

SEG[4-0]					Function
0	0	0	1	1	Start of frame
0	0	0	1	0	ID28 to ID21
0	0	1	1	0	ID20 toID18
0	0	1	0	0	Bit SRTR
0	0	1	0	1	Bit IDE
0	0	1	1	1	ID17 to ID13
0	1	1	1	1	ID12 to ID5
0	1	1	1	0	ID4 to ID0
0	1	1	0	0	Bit RTR
0	1	1	0	1	Reserved bit 1
0	1	0	0	1	Reserved bit 0
0	1	0	1	1	Data length code
0	1	0	1	0	Data field
0	1	0	0	0	CRC sequence
1	1	0	0	0	CRC delimiter
1	1	0	0	1	Acknowledge slot
1	1	0	1	1	Acknowledge delimiter
1	1	0	1	0	End of frame
1	0	0	1	0	Intermission
1	0	0	0	1	Active error flag
1	0	1	1	0	Passive error flag
1	0	0	1	1	Tolerate dominant bits (Note)
1	0	1	1	1	Error delimiter

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

SEG[4-0]					Function
1	1	1	0	0	Overload flag

Note: Any node tolerates up to 7 consecutive 'dominant' bits after send Active Error Flag, Passive Error Flag or Overload Flag.

If a bus error occurs, the corresponding bus error interrupt is generated. At the same time, the current position of the bit stream processor is captured into the CANERR[7:0]. The content in these bits are locked until the software read out its content. A new bus error capture is prohibited until CANERR[7:0] is read. The capture mechanism is then activated again. The corresponding interrupt flag located in the interrupt flag register is cleared by reading of the interrupt flag register.

32.6.2.2 Transmit Buffer

The global layout of the transmit buffer in XFR is shown in figure below. The transmit buffer contains 13-bytes of XFR space can be in the form of Standard Frame Format (SFF) or Extended Frame Format (EFF) configuration.

Standard Format Frame	
B+040h	TX Frame Information
B+044h	TX Identifier[10:0]
B+048h	TX Data 3 - TX Data 0
B+04Ch	TX Data 7 - TX Data 4

Extended Format Frame	
B+040h	TX Frame Information
B+044h	TX Identifier[28:0]
B+048h	TX Data 3 - TX Data 0
B+04Ch	TX Data 7 - TX Data 4

Figure 32-6 Transmit Buffer

The transmit buffer layout is subdivided into descriptor and data fields where the first byte of the descriptor field is the frame information byte (frame information). It describes the frame format (SFF or EFF), remote or data frame and the data length. Four identifier bytes for both SFF and EFF messages follow. But only the lower 11 bits in the four identifier bytes are valid for SFF and the upper 21 bits are invalid. For EFF, the lower 29 bits in the four identifier bytes are valid and the upper 3 bits are invalid. The data field contains up to eight data bytes.

32.6.2.2.1 CAN Transmit Frame Information Register (CANTFIR, 0x40)

	CANTFIR																															Base + 0x40
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								FF	RTR	Reserved	Reseved	DLC[3]	DLC[2]	DLC[1]	DLC[0]
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect, read as zeros.	R
7	FF	Frame Format FF=1 indicates Extended format frame FF=0 indicates Standard format frame	RW
6	RTR	Remote Frame Transmit Request RTR=1 indicates remote frame RTR=0 indicates regular data frame	RW
5:4	Reserved	Writing has no effect, read as zeros.	R
3	DLC[3]	Data Byte Count = DLC[3-0] The number of bytes in the data field of a message is coded by the data length code. At the start of a remote frame transmission the data length code is not considered due to the RTR bit being logic 1 (remote). This forces the number of transmitted/received data bytes to be 0. Nevertheless, the data length code must be specified correctly to avoid bus errors, if two CAN controllers start a remote frame transmission with the same identifier simultaneously. The numbers of data bytes by the DLC is defined by the following table.	RW
2	DLC[2]		
1	DLC[1]		
0	DLC[0]		

Table 32-6 Coding of the numbers of data bytes by the DLC

Frames	Data length code				Number of data bytes
	DLC3	DLC2	DLC1	DLC0	
Classical Frames	0	0	0	0	0
	0	0	0	1	1
	0	0	1	0	2
	0	0	1	1	3
	0	1	0	0	4
	0	1	0	1	5
	0	1	1	0	6
	0	1	1	1	7
	1	0 or 1	0 or 1	0 or 1	8

In standard Frame Format (SFF) the identifier consists of 11 bits (ID.10 to ID.0) and in Extended Frame Format (EFF) messages the identifier consists of 29 bits (ID.28 to ID.0). ID.28 is the most significant bit, which is transmitted first on the bus during the arbitration process. The identifier acts as the message's name and is used for bus arbitration and used in a receiver for acceptance filtering. The smaller the binary value of the identifier is, the higher the priority is. This is due to the larger number of leading dominant bits during arbitration. Also please note the R0, R1 and SRR bits in the SFF and EFF are transmitted as R0=R1=0 and SRR=1.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

32.6.2.2.2 CAN Transmit Identifier Register (CANTXID, 0x44)

	CANTXID																															Base + 0x44
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			CANTXID																												
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:29	Reserved	Writing has no effect, read as zeros.	R
28:0	CANTXID	For SFF ID, CANTXID[10:0] = ID[10:0], CANTXID[31:11] is not used. For EFF ID, CANTXID[28:0] = ID[28:0], CANTXID[31:29] is not used.	RW

32.6.2.2.3 CAN Transmit Data Register0/1 (CANTXDATA0/1, 0x48/0x4C)

Data field registers is mapping to address Base+0x48 to Base+0x4C. The number of transferred data bytes is defined by the data length code. The first bit transmitted is the most significant bit of data byte 0 at address Base+0x48/0x4C.

	CANTXDATA0/1																															Base + 0x48/0x4C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CANTXDATA																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	CANTXDATA	The data to be send,.	RW

32.6.2.3 Acceptance Filter

There are four Acceptance Filters for matching with the ID of a message on the bus. Each filter can be enabled or disabled independently. Each acceptance filter is consisted of 1 ID register and corresponding ID Mask register to mask the match comparing the specific bit in the ID. The layout of the ID registers corresponding to forming ID28 to ID0 for SFF and EFF are the same as Transmit ID registers. Please note the ID registers only define the ID and do not define the frame type, therefore it is possible a value in the ID registers corresponding to two

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

possible matches for SFF and EFF separately. The software should check if unintended accepted ID is possible for another frame type. For the Filter's Mask register, when mask bit is 0 the corresponding bit is compared for matching, and when the mask bit is 1 the corresponding bit is ignored. All Acceptance Filter ID registers and Mask register can only be modified in the reset mode, and appear as read-only in normal operating mode.

32.6.2.3.1 CAN Acceptance Filter ID0/1/2/3(CANAFID0/1/2/3, 0x20,/28/30/38)

	CANAFID0/1/2/3																															Base + 0x20/28/30/38
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			CANAFID																												
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:29	Reserved	Writing has no effect, read as zeros.	R
28:0	CANAFID	The register can only be modified in the reset mode, and appear as read-only in normal operating mode.	RW

32.6.2.3.2 CAN Acceptance Filter Mask0/1/2/3(CANAFMK0/1/2/3, 0x24/2C/34/3C)

	CANAFMK0/1/2/3																															Base + 0x24/2C/34/3C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			CANAFMK																												
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:29	Reserved	Writing has no effect, read as zeros.	R
28:0	CANAFMK	The register can only be modified in the reset mode, and appear as read-only in normal operating mode.	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

32.6.2.4 Receive Buffer

There is a 64-byte SRAM as Receive FIFO (RX-FIFO). Each received frame can contain up to 16 bytes when data length is 8 bytes. So the RX-FIFO can store maximally 4 unread received frames.

Under the RX DMA mode (DMAEN=1), the DMA controller will always issue the dma_req to transfer the receive frame to the DMA host. When receive the dma_finish with dma_ack, the memory space of current frame will be released.

LOCATION	DESCRIPTION	31 24	23 16	15 8	7 0
*B + 0x90	ACP FILTER INFO	0x00	0 1 0 0 Filter Stat[3-0]	0x00	FF RTR 0 0 DLC[3-0]
*B + 0x94	ID	000 ID [28 – 0]			
*B + 0x98	** RX DATA	RX DATA 3 [7-0]	RX DATA 2 [7-0]	RX DATA 1 [7-0]	RX DATA 0 [7-0]
*B + 0x9C		RX DATA 7 [7-0]	RX DATA 6 [7-0]	RX DATA 5 [7-0]	RX DATA 4 [7-0]

*B = Base Address

** RX DATA valid data length is defined by DLC[3-0] and RTR

Figure 32-7 Receive Buffer

32.6.2.4.1 CAN Receive Frame Information Register(CANRFIR, 0x90)

	CANRFIR																															Base + 0x90
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved												RXFMS[3]	RXFMS[2]	RXFMS[1]	RXFMS[0]	Reserved								FF	RTR	Reserved	Reseved	DLC[3]	DLC[2]	DLC[1]	DLC[0]
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:20	Reserved	Writing has no effect, read as zeros.	R
19	RXFMS[3]	Acceptance Filter 3 Match Status RXFSM[3]=1 Acceptance Filter 3 match RXFSM[3]=0 Acceptance Filter 3 not match	R
18	RXFMS[2]	Acceptance Filter 2 Match Status RXFSM[2]=1 Acceptance Filter 2 match RXFSM[2]=0 Acceptance Filter 2 not match	R
17	RXFMS[1]	Acceptance Filter 1 Match Status RXFSM[1]=1 Acceptance Filter 1 match RXFSM[1]=0 Acceptance Filter 1 not match	R
16	RXFMS[0]	Acceptance Filter 0 Match Status RXFSM[0]=1 Acceptance Filter 0 match RXFSM[0]=0 Acceptance Filter 0 not match	R
15:8	Reserved	Writing has no effect, read as zeros.	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

7	FF	Frame Format FF=1 indicates Extended format frame FF=0 indicates Standard format frame	R
6	RTR	Remote Frame Transmit Request RTR=1 indicates remote frame RTR=0 indicates regular data frame	R
5:4	Reserved	Writing has no effect, read as zeros.	R
3	DLC[3]	Data Byte Count = DLC[3-0] The number of bytes in the data field of a message is coded by the data length code. At the start of a remote frame transmission the data length code is not considered due to the RTR bit being logic 1 (remote). This forces the number of transmitted/received data bytes to be 0. Nevertheless, the data length code must be specified correctly to avoid bus errors, if two CAN controllers start a remote frame transmission with the same identifier simultaneously.	R
2	DLC[2]		
1	DLC[1]		
0	DLC[0]		

In standard Frame Format (SFF) the identifier consists of 11 bits (ID.10 to ID.0) and in Extended Frame Format (EFF) messages the identifier consists of 29 bits (ID.28 to ID.0). ID.28 is the most significant bit, which is transmitted first on the bus during the arbitration process. The identifier acts as the message's name and is used for bus arbitration and used in a receiver for acceptance filtering. The smaller the binary value of the identifier is, the higher the priority is. This is due to the larger number of leading dominant bits during arbitration. Also please note the R0, R1 and SRR bits in the SFF and EFF are transmitted as R0=R1=0 and SRR=1.

32.6.2.4.2 CAN Receive Identifier Register (CANRXID, 0x94)

	CANRXID																															**Base + 0x94**
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CANRXID																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	CANRXID	For SFF ID, CANRXID[10:0] = ID[10:0], CANRXID[31:11] is not used. For EFF ID, CANRXID[28:0] = ID[28:0], CANRXID[31:29] is not used.	R

32.6.2.4.3 CAN Receive Data Register0/1(CANRXDATA0/1, 0x98/0x9C)

Data field registers is mapping to address Base+0x98 to Base+0x9C. The number of received

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

data bytes is defined by the data length code.

	CANRXDATA0/1																															Base + 0x98/0x9C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CANRXDATA																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	CANRXDATA	The data received.	R

32.6.2.5 CAN Self-Loop Register (CANSL, 0xFC)

	CANSLF																															Base + 0xFC
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IPRESET						CANTXOFF	CANSLEN	Reserved				CANSLKEY[3-0]				Reserved															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	IPRESET	CAN 2.0B IP Reset. This bit can be programed only when Self-Loop Security Key is unlocked in reset mode (RSTM=1). Setting IPRESET=1 will generate an internal reset signal to initiate all registers and all mechanisms in the CAN controller. IPRESET is cleared automatically.	RW
30:26	Reserved	Writing has no effect, read as zeros	R
25	CANTXOFF	CAN TX Off. This bit can be programed only when Self-Loop Security Key is unlocked in reset mode (RSTM=1). CANTXOFF = 1 Force tx_o always output logical high to CAN transceiver. CANTXOFF = 0 tx_o is normal function to CAN transceiver.	RW
24	CANSLEN	CAN Self-Loop Test Mode. This bit can be programmed only when Self-Loop Security Key is	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

		unlocked in reset mode(RSTM=1), CANSLEN=1 Enable CAN Self-Loop Test Mode. CANSLEN=0 Disable CAN Self-Loop Test Mode.	
23:20	Reserved	Writing has no effect, read as zeros	R
19:16	CANSLKEY[3-0]	CANSLKEY[3-0] is used to protect the CANSLEN and can only be modified in reset mode (RSTM=1). Writing 0x6 into CANSLKEY[3-0] can unlock the access of CANSLEN.	W
15:0	Reserved	Writing has no effect, read as zeros	R

32.7 Basic Operations

The basic function of CAN controller will be discussed in this section. The following chapter will describe the advanced functions of CAN controller. To communicate with other nodes on the CAN-bus, CAN controller must be configured properly as described.

Following diagram is the flowchart of basic communication.

Figure 32-8 CAN basic communication

32.7.1 System Configuration

Following system configurations must be done under reset mode (RSTM=1).

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

32.7.1.1 Enter Reset Mode

Some registers are writable only in reset mode such as Bus Timing registers and Acceptance Filter registers etc., so we must write these registers in the reset mode. Then the CAN controller must quit reset mode when these registers are configured properly to make the controller work.

32.7.1.2 Baud Rate Setting

The baud rate in the CAN-bus is determined by the two registers CANBTR0 and CANBTR1. The following example explains how to calculate the baud rate of 1Mbps assuming system clock is 120MHz, and CANBTR0=09h CANBTR1=45h. Then the TQ1_CLK is CANCLK/(CANCS[5-0]+1) = 120MHz/10 = 12MHz. Thus each time quanta (TQ1) is 83.33nsec. Then the one CAN bit time (BT) of arbitration phase is (1 + (TSEG1+1) + (TSEG2+1)) x 83.33 nsec = (1 + 5 + 6) x 83.33 nsec = 1usec. As the result the CAN bus baud rate of arbitration phase is 1Mbps.

32.7.1.3 Setting of Acceptance Filter

With the help of the acceptance filter, the CAN controller can receive proper frames from CAN-bus only when the identifier bits of the received frames are equal to the predefined ones within the acceptance filter registers. The acceptance filter is defined by the Acceptance Code Registers (ACR) and the Mask Code Registers (MCR). The bit patterns of frames to be received are defined within the Acceptance Code registers. The corresponding mask code registers allow define certain bit positions to be ‘don’t care’. After hardware reset, all the Acceptance Code registers and Mask Code registers are cleared.

There are 4 groups of acceptance filter. We must enable at least one group of filter previously. Each group of filter has 4 Acceptance Code bits and 4 Mask Code bits. Acceptance code 3 register is the highest byte in the Acceptance Code; the Acceptance code 0 register is the lowest byte in the Acceptance Code. Mask code 3 register is the highest byte in the Mask Code and Mask Code 0 register is the lowest byte in the Mask Code.

When received message is standard format frame, the lower 11 bits of the Acceptance Code and the Mask Code are valid. When received message is extended format frame, the lower 29 bits of the Acceptance Code and the Mask Code are valid.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Figure 32-9 Setting Acceptance Filter

Figure 32-10 Extended Frame

Extended frame: if an extended format frame is received, the complete identifier including the RTR bit is used for acceptance filtering. For a successful reception of a message, all single bit comparisons have to signal acceptance. It should be noted that the 3 most significant bits of ACR3 and MCR3 are not used. In order to be compatible with future products these bit should be ‘don’t care’ by setting MCR3.7, MCR3.6 and MCR3.5 to logic 1.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Figure 32-11 Standard Frame

Standard frame: if a standard format frame message is received, the completely identifier are used for acceptance filtering. For a successful reception of a frame, all single bit comparisons have to signal acceptance. Note that ACR3, MCR3, ACR2, MCR2 and the 5 most significant bits of ACR1 and MCR1 are not used. In order to be compatible with future products, these unused bits in Mask Code registers should be programmed to be 'don't care' by setting these bits to logic 1.

32.7.1.4 Enter Operation Mode

After all system configurations are done, we must enter Operation Mode by setting RSTM to zero. In the meanwhile, the CAN controller enters the idle state waiting for transmitting and receiving frames.

32.7.2 Transmitting a Frame

You must write transmit buffer to send a frame to CAN-bus, then set the transmit request bit to logic 1. The controller will wait for the bus idle and sends the frame to the bus. For example, CAN will send a standard format frame to CAN-bus. Frame identifier is 0x123, the data have a length of 8 and the data are 0x11, 0x22, 0x33, 0x44, 0x55, 0x66, 0x77 and 0x88. Following the below steps:

- Write 0x8 to CANTFIR;
- Write 0x123 to CANTXID;
- Write 0x44332211 to CANTXDATA0;
- Write 0x88776655 to CANTXDATA1;
- Write 0x1 to CANCMD;

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

If the transmission completed successfully, the Transmit Interrupt (TI) will be set. If there is any error happened, the Bus Error Interrupt (BEI) will be set and the present frame will be retransmitted after the error frame. User can check the CANERR[7:0] for the detailed error condition and can abort the unsuccessful transmission by setting Abort Transmitting (AT) command.

32.7.3 Receive a Frame

Only the frame which ID passed the Acceptance Filter can be received by controller. When CAN controller receives a frame successfully and the Receive Interrupt Enable (RIE) is enabled, the Receive Interrupt (RI) bit will be set logic 1.

If RX DMA mode (DMAEN) is disable, MCU is informed by the receive interrupt and reads out the data in the receive buffer, then releases the receive buffer. Please pay special attention here that the data must be read before releasing receive buffer, because the value in the receive buffer has changed after releasing receive buffer.

If RX DMA mode (DMAEN) is enable, the DMA request (dma_req) will be active and start the DMA protocol. When complete the DMA protocol by receiving dma_finish, the receive buffer is released and the RX DMA Complete Interrupt (DMAI) will be set to logic 1.

32.8 Test Modes

32.8.1 Self Test Mode

Enable the STE bit in CANMODE[2] will enable the self-test mode .The self-test mode is of the CAN control is the same normal operation mode except all ACK errors are ignored. This allows the software to initiate a “self receive request” command. Upon this command, a message is transmitted to the bus and will be treated as successfully transmitted without check the ACK flag. The transmitted message is also received by the sending CAN controller if the ID field matches with the acceptance filter.

32.8.2 Self Receive Request

Enable the SRR in CANCMD[4] will result a message be transmitted and received simultaneously. Upon Self Receive Request command, a message is transmitted and simultaneously received if the acceptance filter is set to the corresponding identifier. This command is used mainly for self test of the controller. If STE=1 which enables the Self Test Mode, the transmit and receive can be successful without other nodes present.

When transmit and receive operations are completed and both transmit and receive interrupts will be generated. The software shall read and verify the received data from RX-FIFO. Then set the Release Receive Buffer (RRB) command to release the memory space.

32.8.3 Self-loop Test Mode

The software can then check the correctness of the received message and perform loop-back test. The loop-back can be done by shorting CANTX and CANRX, or can be done through the external transceiver on the actual CAN bus. When loop back from the bus, the CAN bus needs to be properly terminated to ensure correct electrical level for normal bus operation.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Figure 32-12 CAN Self-Loop

32.8.4 Self Test Example

32.8.4.1 Step 1

In Reset Mode (RSTM=1), unlock the CANSLKEY then enable CAN Self-Loop Test Mode and set CANTXOFF to bypass the external CAN Transceiver.

32.8.4.2 Step 2

Enable Self Test Mode (STE=1) to ignore all ACK errors.

32.8.4.3 Step 3

In Reset Mode (RSTM=1), configure all bit rate timing registers, operation setting registers and RX acceptance filters same as normal operation. In order to read and compare the TX/RX data by MCU, the RX DMA Mode (DMAEN) shall be disable.

32.8.4.4 Step 4

Enter normal operation mode (RSTM=0), enable both Transmit Interrupt (TIE) and Receive Interrupt (RIE). Program the test ID and Data into the Transmit Buffers then enable Self Receive Request (SRR) command to start the transmit and receive.

32.8.4.5 Step 5

When can_irq is issued, software shall read out the received data from the Receive Buffer and compare with the transmitted data.

32.8.5 Bit Time Configuration Suggestion

In the general application, recommend assigning both SJW[1-0] a non-zero value, such as 0x1 or 0x2. Following tables are the examples of bit time configuration under 80Mhz and 16MHz CANCLK frequency. In real CAN system, these setting shall be readjusted with transceiver's timing.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

32.8.5.1 CANCLK = 24MHz

Table 32-7 CANCLK = 24MHz

Bit Rate	Normal bit time configuration		
	CANCS[5-0]	TSEG2[2-0]	TSEG1[3=0]
1 Mbps	0	7	14
500 Kbps	1	7	14

32.8.5.2 CANCLK = 80MHz

Table 32-8 CANCLK=80MHz

Bit Rate	Normal bit time configuration		
	CANCS[5-0]	TSEG2[2-0]	TSEG1[3=0]
1 Mbps	3	5	12
500 Kbps	7	5	12

32.8.5.3 CANCLK = 16MHz

Table 32-9 CANCLK=16MHz

Bit Rate	Normal bit time configuration		
	CANCS[5-0]	TSEG2[2-0]	TSEG1[3=0]
1 Mbps	0	4	9
500 Kbps	1	4	9

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

33 CDBUS

33.1 OVERVIEW

CDBUS is a protocol for Asynchronous Serial Communication, it has a 3-bytes header: [src_addr, dst_addr, data_len], then user data, and finally 2 bytes of CRC. (Same as MODBUS CRC.)

It's suitable for one-to-one communication, e.g. UART or RS-232. In this case, the address for each side are usually carefully selected and fixed, e.g: [0x55, 0xaa, data_len, ...], and the backward is: [0xaa, 0x55, data_len, ...].

The CDBUS protocol is more valuable for bus communication, e.g. RS-485, M-LVDS or Single Line UART. In this case, it supports multi nodes，full-duplex, multicast, unicast, broadcast and so on.

33.2 Features

- Support multiple modes: arbitration mode(CDBUS-A), break sync mode(CDBUS-BS), full-duplex and half-duplex.
- Two pages for receive and one page for transmit, 256 bytes one page.
- The maximum user data len is 253 bytes.
- Loop back mode for testing.
- Support dual baud rate, maximum rate can greater than 10Mbps.

33.3 Block Diagram

Figure 33-1 CDBUS Block Diagram

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

33.4 Arbitration Mode(CDBUS-A)

- It introduces an arbitration mechanism that automatically avoids conflicts like the CAN bus.
- Support dual baud rate, provide high speed communication, maximum rate can greater than 10Mbps. The baud rate , in the data phase is up to:sys_freq / 3. (e.g. 50 Mbps for 150 MHz sys_freq.)
- Supports unicast, multicast and broadcast.
- The maximum user data size is 253 bytes.
- Hardware packing, unpacking, verification and filtering, save your time and CPU usage.
- Backward compatible with traditional RS-485 hardware (The arbitration function still works).

The protocol timing example, include only one user data byte:

(You can set the length of time to enter idle and wait to send.)

Tips:

When a high-priority node needs to send unimportant data, you can dynamically increase the send wait time (TX_PERMIT_LEN).

33.5 Break Sync Mode(CDBUS-BS)

In CDBUS-A mode, if the low-speed part takes a lot of time, it will be a communication efficiency bottleneck.

In this case, single-rate peer-to-peer bus communication can be implemented by CDBUS-BS mode:

- The TX_PERMIT_LEN parameter is configured differently for different nodes, and the difference needs to be large enough to avoid conflicts.
- If any node has pending tx frame before TX-permit point, then start send at the TX-permit point.
- Or wait until the idle time exceeds MAX_IDLE_LEN, then send a break character to bring the bus out of idle state.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

The CDBUS-BS mode is suitable for high-speed applications with few nodes, and it is also suitable for software implementation.

33.6 Pin Description

Table 33-1 CDBUS Pins Description

Name	I/O	Description
TX_EN	Output	Enable output
TX	Output	Transmit data
RX	Input	Receive data

33.7 Registers Description

33.7.1 Instructions

Following chapter will descript the functions of all software accessible registers.

Conventions:

17. Register Address = Base + Address offset
18. The registers can be read and written by AHB2 bus.
19. Register read/write attribute
    - ✧ R - Read only
    - ✧ W - Write only
    - ✧ RW - read and write
    - ✧ RCW - read and write, but clear to 0 by read
    - ✧ RSW - read and write, but set to 1 by read

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

- ✧ RWC - read and write, clear to 0 by write 1, write 0 has no effect
- ✧ RWS - read and write, set to 1 by write 1, write 0 has no effect
- ✧ RC - read only, and clear to 0 by read
- ✧ RS - read only, and set to 1 by read
- ✧ SPEC - special access method, relate to its description

20. Reset Value
    - 1 - reset to 1
    - 0 - reset to 0
    - ? - value unknown after reset

33.7.2 Map

The CDBUS's registers map base address is 0x13550000.

The CDBUS is controlled by a set of registers that the application configures before every operation. The following table lists all the registers.

Table 33-2 CDBUS Registers Map

Name	Reset Value	Address Offset	Description	RW
VERSION	0x0000_000C	0x00	Hardware verison	R
SETTING	0x0000_0010	0x04	Configs	RW
IDLE_WAIT_LEN	0x0000_000A	0x08	How long to enter idle	RW
TX_PERMIT_LEN	0x0000_0014	0x0C	How long to allow sending	RW
MAX_IDLE_LEN	0x0000_00C8	0x10	Max idle for BS mode	RW
TX_PRE_LEN	0x0000_0001	0x14	Active TX_EN before TX	RW
FILTER	0x0000_00FF	0x18	Set to local address	RW
DIV_LS	0x0000_015A	0x1C	Low-speed rate setting	RW
DIV_HS	0x0000_015A	0x20	High-speed rate setting	RW
INT_FLAG	0x0000_0020	0x24	Status	R
INT_MASK	0x0000_0000	0x28	Interrupt mask	RW
RX_CTRL	0x????_????	0x2C	Rx control	W
TX_CTRL	0x????_????	0x30	Tx control	W
FILTER_M	0x0000_FFFF	0x38	Multicast filters	RW
TX_FIFO	0x????_????	0x100	Write Tx page	W
RX_FIFO	0x????_????	0x500	Write Rx page.	R
SELF_TEST	0x0000_0000	0x900	loopback tx to rx	RW

33.7.3 Register and Fields Description

33.7.3.1 CDBUS VERSION Register(CDVER, 0x0000)

	VER	**BASE+0x0000**

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								VER							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect, read as zero.	R
7:0	VER	Hardware version.	R

33.7.3.2 CDBUS SETTING Register(CDSET, 0x0004)

	SET																															
																	BASE+0x0004															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																									MODE			NOT_DROP	USER_CRC	TX_INVERT	TX_PUSH_PULL
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Name	Description	RW
31:7	Reserved	Writing has no effect, read as zero.	R
6:4	MODE	Supported mode selected. Only one mode can be selected one time. SET[6:4] / Description(MODE) / Remark 000 / Traditional half-duplex mode. / 100 / Full duplex mode. / 010 / Break sync mode.(CDBUS-BS) / 001 / Enable arbitration.(CDBUS-A) / defalt value	RW
3	NOT_DROP	Save broken frame.	RW
2	USER_CRC	Crc maintained by user.	RW
1	TX_INVERT	Invert tx output.	RW
0	TX_PUSH_PULL	Enable push-pull output for tx and tx_en pin.	RW

33.7.3.3 CDBUS IDLE_WAIT_LEN Register(CDIWL, 0x0008)

	IWL																															
																	BASE+0x0008															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Reserved																								IWL							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect, read as zero.	R
7:0	IWL	How long to enter bus idle.	RW

33.7.3.4 CDBUS TX_PERMIT_LEN Register(CDTPERL, 0x000C)

	CDTPERL																															BASE+0x000C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								TPERL							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect, read as zero.	R
7:0	TPERL	How long to allow to send data.	RW

33.7.3.5 CDBUS MAX_IDLE_LEN Register(CDMIL, 0x0010)

	CDMIL																															BASE+0x0010
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																						MIL									
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect, read as zero.	R
9:0	MIL	Max idle wait time for CDBUS-BS mode. **NOTE:** (1) For receiving, the CDIWL.IWL can not be set to 0. (2) For transmitting, the CDTPERL.TPERL must be smaller than CDIWL.MIL. (3) For transmitting, the CDTPERL.TPERL must be greater than CDIWL.IWL of the receiver.	RW

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

33.7.3.6 CDBUS TX_PRE_LEN Register(CDTPREL, 0x0014)

	TPERL																															BASE+0x0014
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														TPREL	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Name	Description	RW
31:2	Reserved	Writing has no effect, read as zero.	R
1:0	TPREL	Active TX_EN before TX. Not used in CDBUS-A mode.	RW

33.7.3.7 CDBUS FILTER Register(CDFIL, 0x0018)

	CDFIL																															BASE+0x0018
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								FIL							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect, read as zero.	R
7:0	FIL	Set as local address.	RW

33.7.3.8 CDBUS DIV_LS Register(CDDIVLS, 0x001C)

	CDDIVL																															BASE+0x001C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																DIVLS															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	1	0	1	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	DIVLS	Set low-speed rate. low-speed rate = sys_freq / (DIVLS + 1);	RW

33.7.3.9 CDBUS DIV_HS Register(CDDIVHS, 0x0020)

	CDDIVHS																															BASE+0x0020
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Reserved																DIVHS															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	1	0	1	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	DIVHS	Set high-speed rate. high-speed rate = sys_freq / (DIVHS + 1); **NOTE:** 1.If not used dual rate, set the same value as DIVLS. 2.The minimum value is 2.	RW

NOTE:

In CDSUB-A mode:

When sys_freq = 150Mhz, the maxmum of high-speed rate is 50Mbps, the maxmum of low-speed rate recommended is no more than 1Mbps.

33.7.3.10 CDBUS INT_FLAG Register(CDIFLG, 0x0024)

	CDIFLG																															BASE+0x0024
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								TX_ERROR	TX_CD	TX_PENDING	RX_ERROR	Reserved	RX_BREAK	RX_PENDING	BUS_IDLE
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect, read as zero.	R
7	TX_ERROR	1: Tx error: tx is 0 but rx is 1.	R
6	TX_CD	1: Tx collision detected.	R
5	TX_PENDING	1: Tx page released by hardware and data can be send by set CDTCTRL.START_TX to 1.	R
4	RX_ERROR	1：Rx error: frame broken.	R
3	Reserved	Writing has no effect, read as zero.	R
2	RX_BREAK	1: Receive break character.	R
1	RX_PENDING	1: Rx page ready for read.	R
0	BUS_IDLE	1: Bus in idle mode.	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

33.7.3.11 CDBUS INT_MASK Register(CDIMSK, 0x0028)

	CDIMSK																															BASE+0x0028
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								TE_MSK	TCD_MSK	TP_MSK	RE_MSK	Reserved	RB_MSK	RP_MSK	IDLE_MSK
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect, read as zero.	R
7	TE_MSK	Mask of TX_ERROR 1: generate interrupt 0: interrupt is masked	RW
6	TCD_MSK	Mask of TX_CD 1: generate interrupt 0: interrupt is masked	RW
5	TP_MSK	Mask of TX_PENDING 1: generate interrupt 0: interrupt is masked. **NOTE:** After set CDTCTRL.START_TX to 1, set this bit to 1. And when receive the TX_PENDING flag and no more data need to send, set this bit to 0 immediately.	RW
4	RE_MSK	Mask of RX_ERROR 1: generate interrupt 0: interrupt is masked	RW
3	Reserved	Writing has no effect, read as zero.	R
2	RB_MSK	Mask of RX_BREAK 1: generate interrupt 0: interrupt is masked. **NOTE:** In CDBUS-BS mode, it suggest that set this bit to 0 to avoid receive the RX_BREAK flag triggered by hardware frequently	RW
1	RP_MSK	Mask of RX_PENDING 1: generate interrupt 0: interrupt is masked	RW
0	IDLE_MSK	Mask of BUS_IDLE 1: generate interrupt 0: interrupt is masked	RW

NOTE:

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Output of irq = ((CDIFLG & CDIMSK) != 0).

33.7.3.12 CDBUS RX_CTRL Register(CDRCTRL, 0x002C)

	CDRCTRL																															BASE+0x002C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										CLR_RBREAK	RST_RX_BLK	CLR_RERR	Reserved	SW_RX_PAGE	Reserved
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:6	Reserved	Writing has no effect, read as zero.	R
5	CLR_RBREAK	Clear RX_BREAK flag.	W
4	RST_RX_BLK	Reset Rx block. The rx page is forced change to the first page after set this bit to 1.	W
3	CLR_RERR	Clear RX_ERROR flag.	W
2	Reserved	Writing has no effect, read as zero.	R
1	SW_RX_PAGE	Switch Rx page.	W
0	Reserved	Writing has no effect, read as zero.	R

33.7.3.13 CDBUS TX_CTRL Register(CDTCTRL, 0x0030)

	CDTCTRL																															BASE+0x0030
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										SEND_BK	ABORT_TX	CLR_TERR	CLR_TCD	START_TX	Reserved
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:6	Reserved	Writing has no effect, read as zero.	R
5	SEND_BK	Send break character.	W
4	ABORT_TX	Abort Tx.	W
3	CLR_TERR	Clear TX_ERROR flag.	W
2	CLR_TCD	Clear TX_CD flag.	W
1	START_TX	Start to send data.	W
0	Reserved	Writing has no effect, read as zero.	R

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

33.7.3.14 CDBUS FILTER_M Register(CDFILM, 0x38)

	CDFILM																															BASE+0x0038
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																FILTER_2								FILTER_1							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:8	FILTER_2	Multicast filter2.	RW
7:0	FILTER_1	Multicast filter1.	RW

NOTE:

The default value 0xFF of CDFILM.FILTER_x means not available.

For CDBUS-A mode：

SRC_ADDR	DST_ADDR	CDFIL.FIL	CDFILM.FILTER_x(x=1,2)	Receive or drop	Remarks
not care	not care	255	not care	Receive	Promiscuous mode
=CDFIL.FIL	not care	!=255	not care	Drop	Avoid loopback
!=CDFIL.FIL	255	not care	not care	Receive	Broadcast
!=CDFIL.FIL	!=255	not care	any=DST_ADDR	Receive	Multicast
!=CDFIL.FIL	!=255	=DST_ADDR	not care	Receive	Unicast
not care	!=255	!=DST_ADDR	any !=DST_ADDR	Drop	

33.7.3.15 CDBUS TX_FIFO Register(CDTFIFO, 0x100)

	CDTFIFO																															BASE+0x0100
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TX_FIFO																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:0	TX_FIFO	The trasmit data register.	W

33.7.3.16 CDBUS RX_FIFO Register(CDRFIFO, 0x500)

	CDRFIFO																															BASE+0x0200
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

	RX_FIFO																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	RX_FIFO	The receved data register.	R

33.7.3.17 CDBUS SELFTEST Register(CDSELT, 0x900)

	CDDIVHS																BASE+0x0020															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															SELF_TEST
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect, read as zero.	R
0	SELF_TEST	Loopback tx to rx.	RW

33.8 Operation guide

Assume that the sys_freq is 150Mhz, using CDBUS-A mode:

- SRC_ADDR = 0xA
- DST_ADDR = 0xB
- data_len = 4
- user data: 0x1, 0x2, 0x3 and x04.

33.8.1 Set sys_seq

(1) Set CLKGR1.CDBUS of cpm module to 0 to ungate the clock for cdbus.

(2) Write 0x6000_0003 to CDBUSCDR to choose MPLL and set sys_seq(cdbus_clk) to 150Mhz.

(3) Wait until CDBUSCDR.CDBUS_BUSY changes to 0.

33.8.2 Init cdbus

(1) Write 0x11 to CDSET.

(2) Write 0x95 to CDDIVLS to set the low-speed rate to 1Mbps.

(3) Write 0xE to CDDIVHS to set the high-speed rate to 10Mbs.

(4) If you want to save time for transmission, please refer to the note of CDMIL

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

register(0x0010).

33.8.3 Send data

(19) Write 0xA to CDFIL to config the filter as “Avoid loopback”.
(20) Write 0x01040B0A to CDTFIFO.
(21) Write 0x40302 to CDTFIFO.
(22) Set CDTCTRL. START_TX to 1 to start to send data.
(23) Set CDIMSK. TP_MSK to 1 to unmask the CDIFLG.TX_PENDING.
(24) If no more data needs to be send, set CDIMSK. TP_MSK to 0 when the CDIFLG.TX_PENDING is 1.

33.8.4 Receive data

(1) Write 0xB to CDFIL to config the filter.
(2) Wait until the CDIFLG.RX_PENDING changed to 1.
(3) Read data from RXFIFO.

33.9 Software Notes

BS 模式下如果波特率设置为 50Mhz，数据长度第一帧为 253bytes，第二帧 1bytes，第三帧 1bytes 那么接收很容易出现 overrun 的情况。

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Section 7

BOOT

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

34 Boot Read Only Memory(BOOTROM)

34.1 Overview

This chapter describes the startup bootrom ways, including SFC MSC0 NOR USB start modes and boot procedure.

The X1600 contains an internal 20KB bootrom. The CPU boots from the bootrom after reset.

34.2 Boot Select

The boot sequence of the X1600 is controlled by boot_sel [1:0]. The configuration is shown as follow:

Table 34-1 Boot Configuration of X1600

boot_sel[1:0]	Boot method
0 0	MSC0@PC(17-22)
0 1	SFC0@PC(17-22)
1 0	NOR
1 1	USB

34.3 Boot Procedure

After reset, the boot program on the internal boot ROM executes as follows:

Disable all interrupts, prepare the program running environment.

Read and save efuse values, the values to determine whether to set MSC 4bit transmission data, MSC wait status, gpio HI-Z, hide USB device information, USB eye diagram.

Initialize clock and read boot_sel[1:0] to determine the boot method.

1. If it is boot from MMC/SD card at MSC0, the boot program loads the 26KB data from MMC/SD card to cache and jump to it. The clock 187.5Khz (MSC_CDR=12M, DEV_CLK=12M/64) is used initially. When reading data, the clock 12Mhz is used. If the msc_bus_width_4 efuse value is set to 1, the function pins MSC_D0, MSC_D1, MSC_D2, MSC_D3 are initialized for 4bit data transmission, otherwise, only the MSC_D0 data bus is used.

2. If it is boot from USB, a block of code will be received through USB cable connected with host PC and be stored in cache. Then branch to this area in cache.

3. If it is boot from SPI nor/nand at SFC, its function pins SFC_CLK, SFC_CE, SFC_DR, SFC_DT, SFC_WP, SFC_HOL are initialized, the boot program loads the spl size bytes code from nor/nand to cache and jump to it.

4. If it is boot from NOR Flash, the boot program jump to nor and run directory.

NOTE: The bootrom of x1600 occupies 36KB of cache, its address is from 0x80000000 to 0x80009000.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

34.4 Block Diagram

After reset, the boot program on the internal boot ROM is executed as shown in the boot sequence Block Diagram:

Figure 34-1 Boot sequence diagram of X1600

34.5 SPL Structure

For some special requirement, SPL(Second Program Loader) data needs to contain different information according to the different boot modes. The basic structure as shown below. SC_Boot KEY (1.5K) use for security boot, SPL signature is used to store some information for kinds of boot (512B), and SPL.text (not more than24K,and 512 byte aligned) is real code segment. The first 4k bytes of cache address space is used for stack and data space. all the boot model must jump to 0x80001000 to execute SPL code and all the boot model contains the SPL structure show as Figure 1 -2. Every boot model has its unique SPL signature,Introduces the SPL signature structure behind.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Figure 34-2 The basic SPL structure diagram

34.6 SPL Paramaters

In order to support variable length of SPL size and increase the loading speed by changing the clock frequency. The SPL parameter is created to accomplish this function. This mechanism is only used for SFC/SD/MMC boot, and this mechanism is optional.

Parameters in a storage space in a certain structure is placed, and the size is 256 bytes .When sd card boot, the parameters will be placed at 17K + 256 space.

Table 34-2 **SPL parameters structure**

Offset	0x1 : 0x0	0x3 : 0x2	0x7 : 0x4	0xb : 0x8	0xf : 0xc
0x00	INGE		SPL length	CPU freq	Reserved
0x10	NAND Timing[0]		NAND Timing[1]	NAND Timing[2]	NAND Timing[3]
0x20	Desc[0].saddr	Desc[0].paddr	Desc[0].value	Desc[0].poll_h	Desc[0].poll_l

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

0x30	Desc[1].saddr	Desc[1].paddr	Desc[1].value	Desc[1].poll_h	Desc[1].poll_l
0x40	Desc[2].saddr	Desc[2].paddr	Desc[2].value	Desc[2].poll_h	Desc[2].poll_l
…	…	…	…	…	…
0xf0	Desc[13].saddr	Desc[13].paddr	Desc[13].value	Desc[13].poll_h	Desc[13].poll_l

Domain in SPL parameter structure:

INGE：

SPL Params ID，must store ‘I’ ‘N’ ‘G’ ‘E’, if this area is not store “INGE”,bootrom will use default params to boot.

SPL length：

The length of SPL in bytes, and must be 512 byte aligned. the size of SPL must be not more than 24K.

CPU freq：

Cpu frequency conversion value in HZ.

NAND Timing[0~3]：

After frequency conversion, the timing parameters of NAND.

```
struct {
        unsigned set_rw:8;
        unsigned wait_rw:8;
        unsigned hold_rw:8;
        unsigned set_cs:8;
        unsigned wait_cs:8;
        unsigned trr:8;
        unsigned tedo:8;
        unsigned trpre:8;
        unsigned twpre:8;
        unsigned tds:8;
        unsigned tdh:8;
        unsigned twpst:8;
        unsigned tdqsre:8;
        unsigned trhw:8;
        unsigned t1:8;
        unsigned t2:8;
    };
```

Descriptor：

A maximum of 14 groups descriptor, each descriptor is used to configure an cpm register. The content of descriptor definition is as follows:

Saddr: Set Value Addr(This is lower 16 bits address , th higher 16bit address is

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

0xb000).

paddr: Polling Value Addr(This is lower 16 bits address , th higher 16bit address is 0xb000).

value: The configuration value of the “saddr” register

poll_h: Polling high bit mask(32bit).

poll_l: Polling low bit mask(32bit).

Figure 34-3 SPL configuration change Procedure

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

34.7 MSC Boot Specification

The MSC boot program will load 26KB code starting at address 0x4400 from MMC/SD card to cache. First the boot determine data transfer width through the efuse value, if 1 bit width initializes MSC_D0, MSC_CLK, MSC_CMD as function pins, if 4 bits width initializes MSC_D0, MSC_D1, MSC_D2, MSC_D3, MSC_CLK, MSC_CMD as function pins. Then the boot program sends CMD55 to test if it‘s SD or MMC card and initializes the card. At last it loads 26KB code from the card to cpu cache and branches to execute the code.
When initializing the card, the clock of 187.5Khz (MSC_CDR=12M, DEV_CLK=12M/64) is used. And when reading data, the clock of 12Mhz is used.

The procedure of the X1600 MMC/SD boot is shown as follow:

Figure 34-4 Typical Procedure of MSC0 boot

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

34.8 SFC boot Specification

When boot_sel[1:0] is selected as SFC boot, CPU will goes into SFC boot, AT first cpu fetch a 16 bytes flag information table(The first 16 bytes in SPL signature)from the SPI device. CPU check the flag table to decide the SPI address length , SPI device type(NOR flash or NAND flash), receive code length and the crc7 check data. SFC_boot detailed process shown “SFC Boot Procedure”

Note: Any irregularity in boot steps, SPI_boot will disable SFC controller and jump to MSC0 boot.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Figure 34-5 SFC Boot Procedure

SPI-NOR BOOT:

When SPI NOR flash by General-Purpose I/O Port-A 1,2,3,4 pin. In SPI NOR flash address 0x0~0xF, this space will store 16 bytes that agreed SPI boot flag.

The SPI boot flag information table and procedure of the X1600 SPI NOR boot is shown as follow:

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Table 34-3 SPI NOR flash boot flag informations(in spl signature)

Addr	0x0	0x1	0x2	0x3	0x4	0x5	0x6	0x7
Detail	0x06	0x05	0x04	0x03	0x02	0x55	0xaa	0x55
Addr	0x8	0x9	0xa	0xb	0xc	0xd	0xe	0xf
Detail	0xaa	0x00	0x00	0x00	Len(LSB)	Len(MSB)	0x00	0x00

Explain:

0x00~0x04 :Must store 0x06,0x05,0x04,0x03,0x02
These part is used for cpu to decide the spi address length
0X05~0X08 :Must not be 0x55,0xAA,0x55,0xAA.
Magic code，device use this code decided whether is spi-nor flash boot
0x09~0x0b :Don't care.
0x0C~0x0D :The length of copy data.
0x0E~0X0F :Don't care.

SPI-NAND BOOT:

When SPI NAND flash by General-Purpose I/O Port-A 1,2,3,4 pin. Like spi nor flash, in spi NAND flash address 0x0~0xF, this space will store 16 bytes that agreed SPI_boot flag.
The SPI_boot flag information table and procedure of theX1600 SPI NAND boot is shown as follow:

Table 34-4 SPI NAND flash boot flag informations(in spl signature)

Addr	0x0	0x1	0x2	0x3	0x4	0x5	0x6	0x7
Detail	0x06	0x05	0x04	0x03	0x02	0x55	0xaa	0x55
Addr	0x8	0x9	0xa	0xb	0xc	0xd	0xe	0xf
Detail	0x00	Crc7	ppb	bpp	Len(LSB)	Len(MSB)	Env_crc	Head_crc

Explain:

0x00~0x04 :Must store 0x06,0x05,0x04,0x03,0x02
These part is used for cpu to decide the spi address length
0X05~0X08 :Must not be 0x55,0xAA,0x55,0x00.
Magic code，device use this code decided whether is spi-nand flash boot
0x09 :The copy code’s crc7 value .
0x0a :The pages per block of SPI Nand, the value is X/32, for example, the pages

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

per block is 64, then ppb is 64/32=2.

0x0B :The bytes per page of SPI Nand, the value is X/1024, for example, the bytes per page is 2048, then bpp is 2048/1024=2.

0x0C~0x0D :The length of copy data.

0x0E :The env data code's crc7 value .

0X0F :The first fifteen byte flags code's crc7 value .

34.9 USB Boot Specification

When boot_sel[1:0] is selected as USB boot, the internal boot ROM downloads user program from the USB port to internal cache and branches to the internal cache to execute the program.

X1600 supports the external main crystal whose frequency is 24MHz.
The boot program supports both high-speed (480MHz) and full-speed (12MHz) transfer modes.
The boot program uses the following two transfer types.

Table 34-5 **Transfer Types Used by the Boot Program**

Transfer Type	Description
Control Transfer	Used for transmitting standard requests and vendor requests.
Bulk Transfer	Used for responding to vendor requests and transmitting a user program.

The following figure shows an overview of the USB communication flow.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Figure 34-6 USB Communication Flow

The vendor ID and product ID for the USB boot device are 0xa108 and 0xEAEF respectively. The Configuration for USB is for Control Endpoint 0 with Max Packet Size equals 64 bytes, Bulk IN at Endpoint 1 with Max Packet Size equals 512 bytes in high-speed and 64 bytes in full-speed, Bulk OUT at Endpoint 1 with Max Packet Size equals 512 bytes in high-speed and 64 bytes in full-speed.

The USB boot program provides six vendor requests through control endpoint for user to download/upload data to/from device, and to branch to a target address to execute user program. The six vendor requests are VR_GET_CPU_INFO (0x00), VR_SET_DATA_ADDRESS (0x01), VR_SET_DATA_LENGTH (0x02), VR_FLUSH_CACHES (0x03), VR_PROGRAM_START1 (0x04) and VR_PROGRAM_START2 (0x05). User program is transferred through Bulk IN or Bulk OUT endpoint.

When X1600 is reset with boot_sel[1:0] equals 11b, the internal boot ROM will switch to USB boot mode and wait for USB requests from host. After connecting the USB device port to host, host will recognize the connection of a USB device, and start device enumeration. After finishing the device enumeration, user can send VR_GET_CPU_INFO (0x00) to query the device CPU information. If user wants to download/upload a program to/from device, two vendor requests VR_SET_DATA_ADDRESS (0x01) and VR_SET_DATA_LENGTH (0x02) should be sent first to tell the device the address and length in byte of the subsequent

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

transferring data. Then data can be transferred through bulk-out/bulk-in endpoint. After this first stage program has been transferred to device, user can send vendor request VR_PROGRAM_START1 (0x04) to let the CPU to execute the program. This first stage program must not greater than 20KB and is normally used to init GPIO and SDRAM of the target board. At the end of the first stage program, it can return back to the internal boot ROM by jumping to ra ($31) register. Thus user can download a new program to the SDRAM of the target board like the first stage, and send vendor request VR_FLUSH_CACHES (0x03) and VR_PROGRAM_START2 (0x05) to let the CPU to execute the new program. Next figure is the typical procedure of USB boot.

Figure 34-7 Typical Procedure of USB Boot

Following tables list all the vendor requests that USB boot program supports:

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

Table 34-6 Vendor Request 0 Setup Command Data Structure

Offset	Field	Size	Value	Description
0	bmRequestType	1	40H	D7 0: Host to Device. D6-D5 2: Vendor. D4-D0 0: Device.
1	bRequest	1	00H	VR_GET_CPU_INFO: get CPU information.
2	wValue	2	0000H	Not in used.
4	wIndex	2	0000H	Not in used.
6	wLength	2	0008H	8 bytes.

Table 34-7 Vendor Request 1 Setup Command Data Structure

Offset	Field	Size	Value	Description
0	bmRequestType	1	40H	D7 0: Host to Device. D6-D5 2: Vendor. D4-D0 0: Device.
1	bRequest	1	01H	VR_SET_DATA_ADDRESS: set address for next bulk-in/bulk-out transfer.
2	wValue	2	xxxxH	MSB (bit[31:16]) of the data address.
4	wIndex	2	xxxxH	LSB (bit[15:0]) of the data address.
6	wLength	2	0000H	Not in used.

Table 34-8 Vendor Request 2 Setup Command Data Structure

Offset	Field	Size	Value	Description
0	bmRequestType	1	40H	D7 0: Host to Device. D6-D5 2: Vendor. D4-D0 0: Device.
1	bRequest	1	02H	VR_SET_DATA_LENGTH: set length in byte for next bulk-in/bulk-out transfer.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

2	wValue	2	xxxxH	MSB (bit[31:16]) of the data length.
4	wIndex	2	xxxxH	LSB (bit[15:0]) of the data length.
6	wLength	2	0000H	Not in used.

Table 34-9 Vendor Request 3 Setup Command Data Structure

Offset	Field	Size	Value	Description
0	bmRequestType	1	40H	D7 0: Host to Device. D6-D5 2: Vendor. D4-D0 0: Device.
1	bRequest	1	02H	VR_SET_DATA_LENGTH: set length in byte for next bulk-in/bulk-out transfer.
2	wValue	2	xxxxH	MSB (bit[31:16]) of the data length.
4	wIndex	2	xxxxH	LSB (bit[15:0]) of the data length.
6	wLength	2	0000H	Not in used.

Table 34-10 Vendor Request 4 Setup Command Data Structure

Offset	Field	Size	Value	Description
0	bmRequestType	1	40H	D7 0: Host to Device. D6-D5 2: Vendor. D4-D0 0: Device.
1	bRequest	1	04H	VR_PROGRAM_START1: transfer data from D-Cache to I-Cache and branch to address in I-Cache. **NOTE:** After downloading program from host to device for the first time, you can only use this request to start the program. Since the USB boot program will download data to D-Cache after reset. This request will transfer data from D-Cache to I-Cache and execute the program in I-Cache.
2	wValue	2	xxxxH	MSB (bit[31:16]) of the program entry point.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.

4	wIndex	2	xxxxH	LSB (bit[15:0]) of the program entry point.
6	wLength	2	0000H	Not in used.

Table 34-11 Vendor Request 5 Setup Command Data Structure

Offset	Field	Size	Value	Description
0	bmRequestType	1	40H	D7 0: Host to Device. D6-D5 2: Vendor. D4-D0 0: Device.
1	bRequest	1	05H	VR_PROGRAM_START2: branch to target address directly.
2	wValue	2	xxxxH	MSB (bit[31:16]) of the program entry point.
4	WIndex	2	xxxxH	LSB (bit[15:0]) of the program entry point.
6	WLength	2	0000H	Not in used.

Copyright © 2005-2021 Ingenic Semiconductor Co., Ltd. All rights reserved.