Project Polyphony
Zedboard Implementation

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Revision History

Rev.	Date	Author	Description
0.9	2020/06/30	Kenji Ishimaru	First Release
0.91	2020/07/16	Kenji Ishimaru	Terminology changed: master to initiator, slave to target

Contents

1 Introduction

The 3D system consists of hardware Rasterizer (polyphony IP Core) and Cortex-A9 CPU. The Cortex-A9 processes application program, 3D graphics API middleware, and Geometry Engine. The system occupies only one CPU out of 2 CPUs.

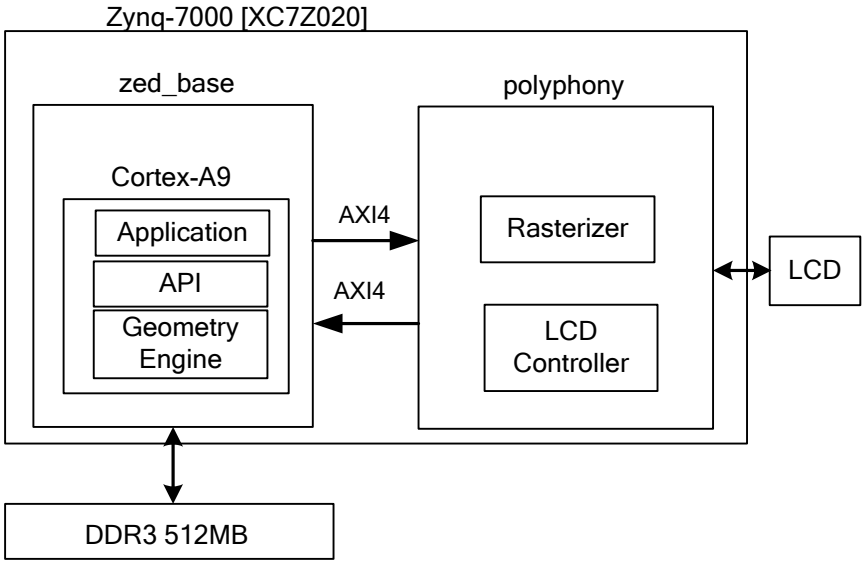

Figure 1 System Architecture

Table 1 System Overview

System	Development System	ZedBoard
	FPGA	Zynq-7020
	Feature	3D Video System
	Memory	DDR3 512MB
	Video Out	Analog VGA(DSUB)
	OS	None(Bear-metal)
Processor (Software process)	Function	Application 3D Geometry Engine (One Cortex-A9 of 2 is used)
	Cortex-A9 Frequency	666MHz
	DDR3 Frequency	533MHz(Data Rate: 1066MHz)
Programmable Logic (Hardware Process)	Function	3D Rasterizer LCD Controller (VGA Size)
	Logic Frequency	66MHz/25MHz(VGA)
	Interface	AXI4 Target : 32-bit x 1 (M_AXI_GP0) AXI4 Initiator: 64-bit x 1 (S_AXI_ACP)

2 Architecture

The software Geometry Engine reads 3D model data from DDR3 memory, then transform them to 2D vertices. The transformed vertices are stored in DDR3 memory. The rasterizer reads transformed 2D vertices from DDR3 memory and generates pixels. The generated pixels are stores in frame buffers in DDR3 memory.

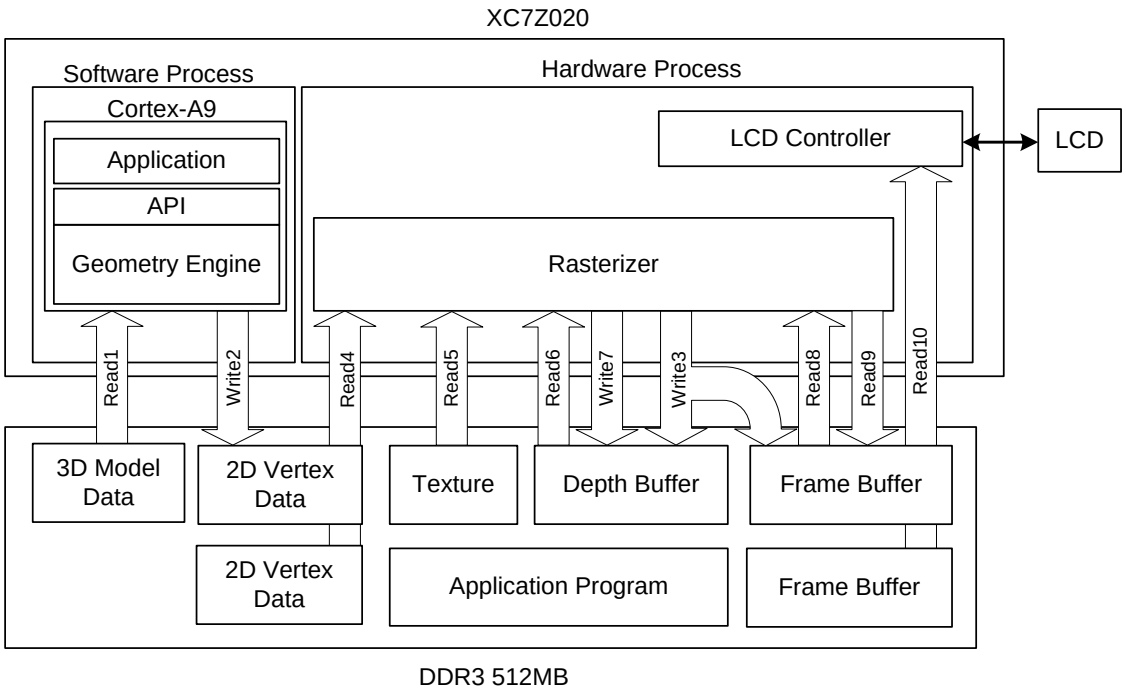

Figure 2 Memory Accesses

3 Operation

3D rendering consists of 3 main processes, Geometry Processing, Pixel Processing, and LCD Display. Each process runs in parallel. If the elapsed time of a process exceeds one frame interval (16ms), double buffer swapping is extended to the next frame interval.

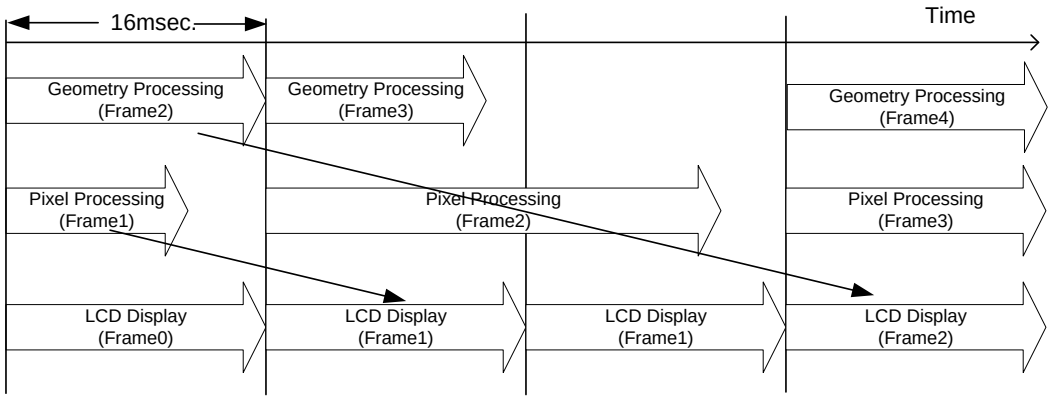

Figure 3 Frame Processing

4 Register and Memory Mapping

DDR3 main memory is mapped from 0000_0000h to 1FFF_FFFFh. Polyphony registers are mapped from 4000_0000h to 4000_03FFh(1kB) in M_AXI_GP0 area.

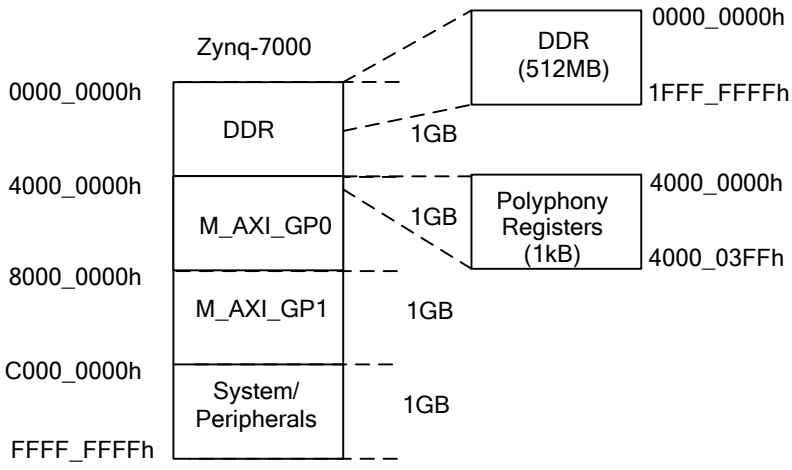

Figure 4 Memory Map

Table 2 Memory Map

Address Range	CPU/S_AXI_ACP	Notes
0000_0000h to 0003_FFFFh	DDR/OCM	DDR3 512MB is mapped at
0004_0000h to 3FFF_FFFFh	DDR	
4000_0000 h to 7FF_FFFFh	Polyphony Registers	M_AXI_GP0 area is mapped at 4000_0000h to 4000_03FFh
8000_0000h to BFFF_FFFFh	(Reserved)	Reserved area
C000_0000h to DFFF_FFFFh	(Reserved)	Reserved area
E000_0000 to FFFF_FFFF	Zynq System Register/ Peripheral/On-Chip Memory	Zynq system registers