Polyphony IP Core Specification

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Revision History

Rev.	Date	Author	Description
0.9	2020/06/30	Kenji Ishimaru	First Release

Contents

1 Introduction

Polyphony is a real-time 3D graphics rendering IP Core. The IP Core reads 3D triangle vertices from memory, then rasterizes them to 2D pixels. Note that this IP Core does not have hardware Geometry Engine. Polyphony requires software Geometry Engine, or other hardware Geometry Engine.

1 - 1 Features

- RTL Design
  - Design Language: Verilog
  - Clock Domain: 2 clocks(main clock and video clock)
  - Independent from any vendor specific module
- Interface
  - 32-bit AXI4 Slave Channel x1 (register configuration)
  - 64-bit AXI4 Master Channel x 1 (memory access)
- 3D Graphics Rasterizer
  - Display list DMAC
  - Rendering image size:　640 x 480(VGA)
  - Texture: 1 unit, bi-linear filtering
  - Anti-Aliasing: Quincunx
- LCD Conroller
  - VGA size

Note:
This IP Core does NOT have Hardware Geometry Engine.

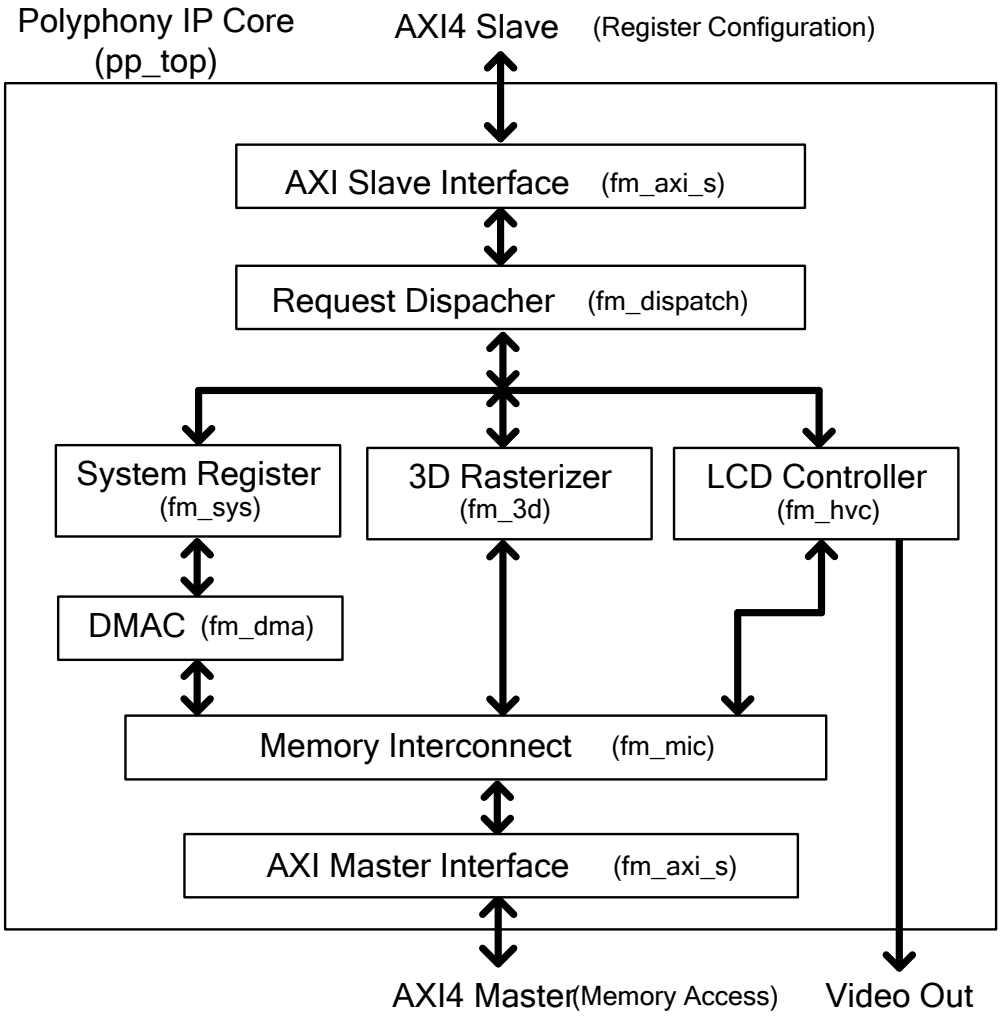


Figure 1 Interface and Internal Architecture

1 - 2 System Requirement

The real-time 3D graphics system would require additional system resources (Table 1).

Resource	Purpose
Processor	3D scene control, IP Core control(register configuration), Geometry Engine(vertex transformation, lighting)
Memory	The storage for 3D scene object and frame buffers

Table 1 Additional system resources

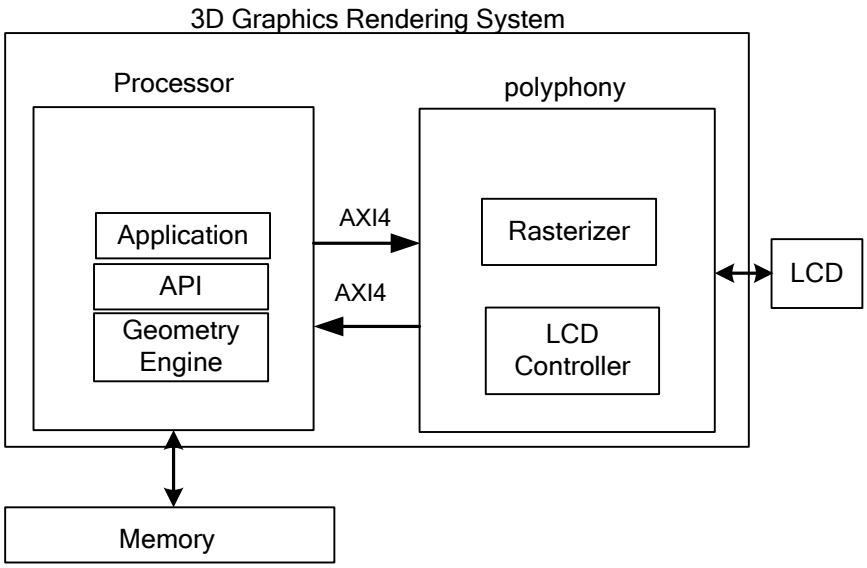


Figure 2 Polyphony 3D system implementation example

2 Architecture

The IP Core contains eight sub-modules.

- AXI Slave Interface
- AXI Master Interface
- Register Access Dispatcher
- System Register
- DMAC
- Memory Interconnect
- LCD Controller
- Rasterizer

2 - 1 AXI Slave Interface

AXI Slave Interface converts AXI4 protocol to Polyphony internal register access protocol.

2 - 2 AXI Master Interface

AXI Master Interface converts Polyphony internal memory access transfer to AXI4 protocol.

2 - 3 Register Access Dispatcher

Register Access Dispatcher dispatches internal resister access from AXI Slave Interface to sub-modules depending on the access destination address.

2 - 4 System Register

System Register contains Polyphony system registers. Rasterizer configuration registers are stored in Rasterizer module.

2 - 5 DMAC

DMAC(Direct Memory Acces Controller) fills memory by specified values. DMAC is used to clear frame buffer and depth buffer.

2 - 6 Memory Interconenct

Polyphony has three master memory accesses internally. The modules that require master memory access are DMAC, Rasterizer, and LCD Controller. When multiple modules require master memory access simultaneously,

Memory Interconnect selects one memory access from the simultaneous master accesses depending on the internal access priority setting.

2 - 7 LCD Controller

LCD Controller reads rendered pixels from frame buffer, and then outputs those pixels at VGA pixel clock timing. LCD Controller contains on-the-fly Quincunx anti-aliasing filter.

2 - 8 Rasterizer

Rasterizer fetches triangle vertices from memory and generates pixels from those triangles. Rasterizer contains five sub-modules (Figure 3).

Module Name	Instance Name	Description
fm_3d_cu	u_3d_cu	Rasterizer control module
fm_3d_ru	u_3d_ru	Triangle rasterizer
fm_3d_tu	u_3d_tu	Texture unit
fm_3d_pu	u_3d_pu	Pixel unit
fm_3d_mu	u_3d_mu	Memory access cache unit

Table 2 Rasterizer(fm_3d) sub-modules

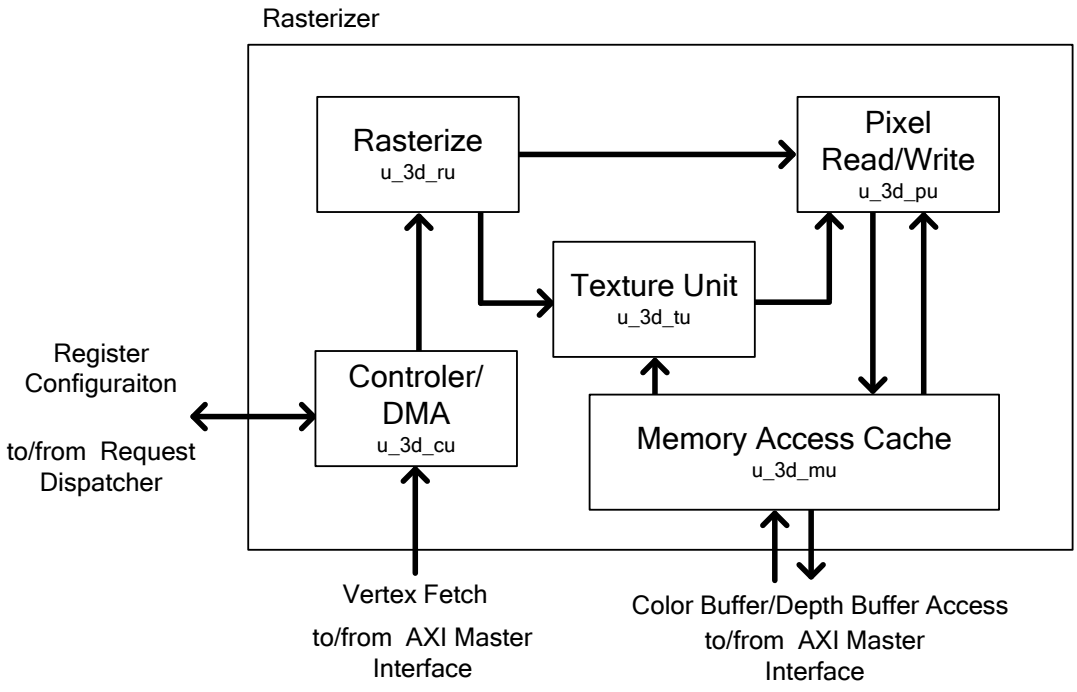


Figure 3 Rasterizer internal modules

3 Operation

3 - 1 Overview

From the user side view, a single 3D-object drawing requires the following steps:

1. Vertex generation (by software Geometry Engine)
2. Register setup
3. Start rendering
4. Wait interrupt

If there are multiple objects (data arrays) in a 3D scene, repeat the drawing steps from No.1 to No.4 for the number of data arrays.

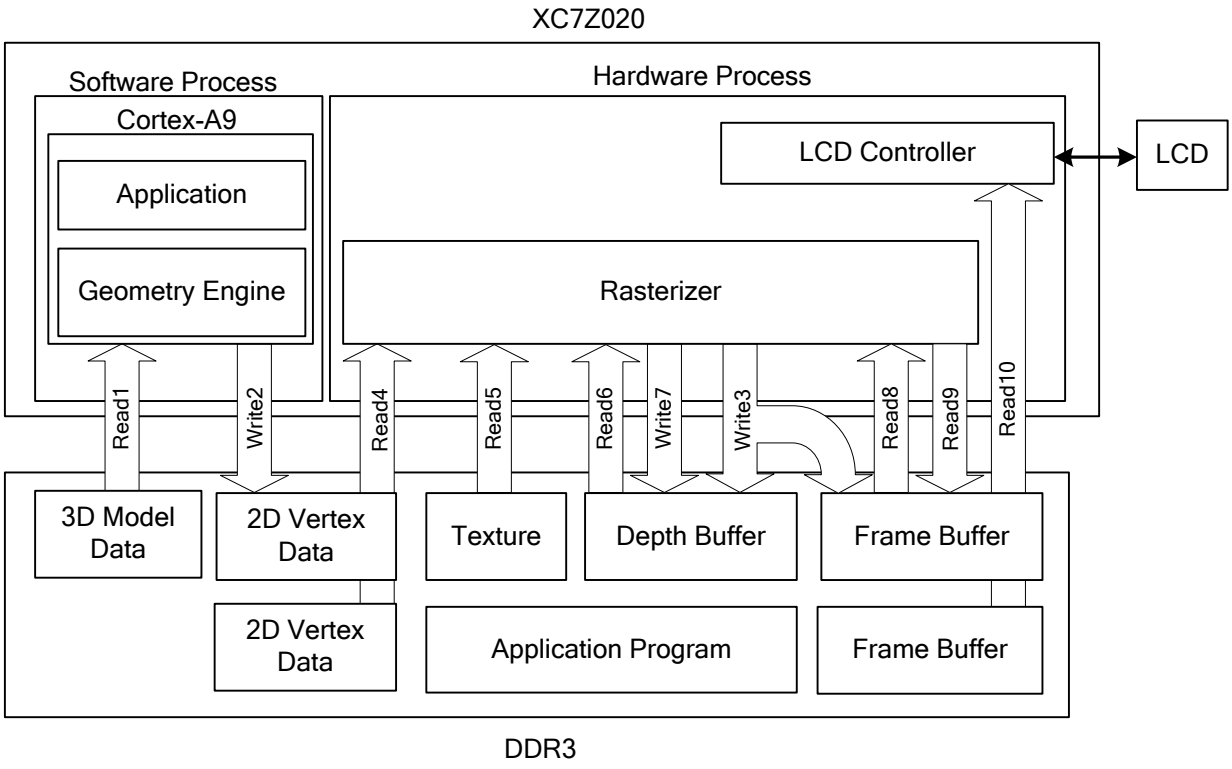


Figure 4 A single draw operations

3 - 2 Traiangle Data

To render trianlges for a scene frame, Polyphony requires triangle data and reqister-setting commands stored in the system memory. The triange data contains 2D-projected vertex arrays. The data format of the vertices are IEEE single precision floating-point number. The IP Core only supports 3-vertex triangle array. The register commans are stored in the registers and control subsequent triangle data processing.

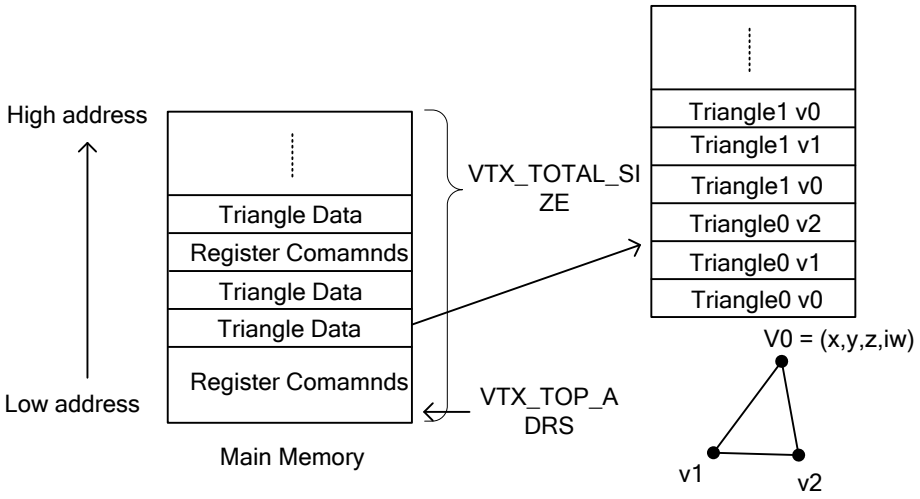
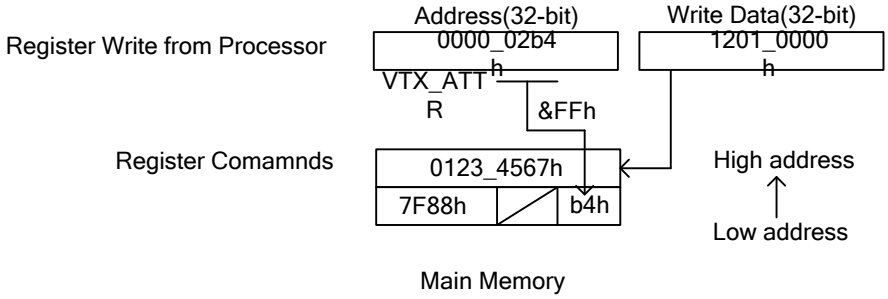


Figure 5 Vertex Array

3 - 2 - 1 Register Commands

Register Commans



3 - 2 - 2 Triangles

One vertex has x,y and z elements, and does not have w element.

3 - 3 Register Setup

Before start rendering, the following register configurations are required.

Category	Related Registers	Description
Screen Size	FSCR_W FSCR_H ISCR_W_M1 ISCR_H_M1 ISCR_W	Screen width and height
Vertex DMA	VDMA_ADDR VDMA_SIZE	DMA start address and size
Matrix transformation	MAT_EMT00-33	Model-View-Projection Matrix elements
Culling	GEO_CTR[8] GEO_CTR[16]	On/Off and clock-wise
Frame Buffer	FB_ADDR	Frame buffer address
Line Color	RAS_CTR[7:0]	Rasterize line color
Result Image	RAS_CTR[8]	Screen Y-flip On/Off

Table 3 Register Setup

3 - 4 Start Rendering

To start rendering, write 1 to GET_CTR[0].
After starting rendering, the IP Core reads current draw arrays from VDMA_ADDR, then writes rasterized pixels to FB_ADDR.

3 - 5 Interrupt Handling

When the current rendering is finished, INT_CTR[0] status is set to 1.
INT_CTR[0] status shows finish status in the following situation:
- Geometry Engine finished all vertices read
- All state machines in the IP Core modules are in IDLE state.

If INT_CTR[8] is 0, the interrupt also notifies to the processor that current rendering is finished.

4 Registers

4 - 1 Overview

Table 4 Polyphony Registers

Name	Register Address (Byte Address)	Description
VIDEO_START	0x00	Display Controller Control
FB0_OFFSET	0x04	Frame Buffer0 Offset Address
FB1_OFFSET	0x08	Frame Buffer1 Offset Address
FB0_MS_OFFSET	0x0C	Anti-Alias Multi Sample Buffer0 Offset
FB1_MS_OFFSET	0x10	Anti-Alias Multi Sample Buffer1 Offset
COLOR_MODE	0x14	Color Mode
AXI_MASTER_CONFIG	0x18	AXI Master Configuration
INT_STATUS	0x20	Interrupt Status
INT_CLEAR	0x24	Interrupt Clear Register
INT_MASK	0x28	Interrupt Mask Register
FRONT_BUFFER	0x2C	Front/Back Buffer Status
DMA_TOP_ADRS0	0x30	DMA Start Address0
DMA_TOP_ADRS1	0x34	DMA Start Address1
DMA_TOP_ADRS2	0x38	DMA Start Address2
DMA_TOP_ADRS3	0x3C	DMA Start Address3
DMA_BE_LENGTH	0x40	DMA Size/Be
DMA_WD0	0x44	DMA Write Data0/1
DMA_WD1	0x48	DMA Write Data2/3
DMA_CTRL	0x4C	DMA Control
RASTER_CTRL	0x200	Raster Start
RASTER_CACHE_CTRL	0x204	Cache Control
VTX_TOP_ADRS	0x208	Vertex Buffer Top Address
VTX_TOTAL_SIZE	0x20C	Vertex Total Transfer Size
NUM_OF_TRIANGLES	0x210	Number of Triangles
NUM_OF_ELEMENTS	0x214	Number of Elements
VTX_DMA_CTRL	0x218	Vertex DMA Control
TEX_OFFSET	0x220	Texture0 Buffer Offset

TEX_WIDTH_M1	0x224	Texture0 Width-1 (floating format)
TEX_HEIGHT_M1	0x228	Texture1 Height-1 (floating format)
TEX_WIDTH_UI	0x22C	Texture1 Width (unsigned format)
TEX_CONFIG	0x234	Texture0 Configuration format
TEX_ENABLE	0x258	Texture0 Enable
TEX_BLEND_ENABLE	0x278	Texture0 Blend Enable
SCREEN_MODE	0x280	Screen Mode
COLOR_OFFSET	0x284	Color Buffer Offset
COLOR_MS_OFFSET	0x288	Multi Sample Buffer Offset
DEPTH_OFFSET	0x28C	Depth Buffer Offset
DEPTH_MS_OFFSET	0x290	Depth Multi Sample Buffer Offset
BLEND_OPERATION	0x294	Blend Operation
DEPTH_TEST	0x2AC	Depth Test
COLOR_MASK	0x2B0	Color Masking
VTX_ATTR	0x2B4	Attribute Configuration
VTX0_X	0x340	Vertex0 X
VTX0_Y	0x344	Vertex0 Y
VTX0_Z	0x348	Vertex0 Z
VTX0_IW	0x34C	Vertex0 IW (1/W)
VTX0_P00	0x350	Vertex0 Attribute0 0
VTX0_P01	0x354	Vertex0 Attribute0 1
VTX0_P02	0x358	Vertex0 Attribute0 2
VTX0_P03	0x35C	Vertex0 Attribute0 3
VTX0_P10	0x360	Vertex0 Attribute1 0
VTX0_P11	0x364	Vertex0 Attribute1 1
VTX0_P12	0x368	Vertex0 Attribute1 2
VTX0_P13	0x36C	Vertex0 Attribute1 3
VTX1_X	0x380	Vertex1 X
VTX1_Y	0x384	Vertex1 Y
VTX1_Z	0x388	Vertex1 Z
VTX1_IW	0x38C	Vertex1 IW (1/W)
VTX1_P00	0x390	Vertex1 Attribute0 0
VTX1_P01	0x394	Vertex1 Attribute0 1
VTX1_P02	0x398	Vertex1 Attribute0 2
VTX1_P03	0x39C	Vertex1 Attribute0 3

VTX1_P10	0x3A0	Vertex1 Attribute1 0
VTX1_P11	0x3A4	Vertex1 Attribute1 1
VTX1_P12	0x3A8	Vertex1 Attribute1 2
VTX1_P13	0x3AC	Vertex1 Attribute1 3
VTX2_X	0x3C0	Vertex2 X
VTX2_Y	0x3C4	Vertex2 Y
VTX2_Z	0x3C8	Vertex2 Z
VTX2_IW	0x3CC	Vertex2 IW (1/W)
VTX2_P00	0x3D0	Vertex2 Attribute0 0
VTX2_P01	0x3D4	Vertex2 Attribute0 1
VTX2_P02	0x3D8	Vertex2 Attribute0 2
VTX2_P03	0x3DC	Vertex2 Attribute0 3
VTX2_P10	0x3E0	Vertex2 Attribute1 0
VTX2_P11	0x3E4	Vertex2 Attribute1 1
VTX2_P12	0x3E8	Vertex2 Attribute1 2
VTX2_P13	0x3EC	Vertex2 Attribute1 3

4 - 2 VIDEO_START

Bits	R/W	POR	Description
31:17	Reserved		
16	RW	0	Buffer Blend mode for anaglyph 0: Disable 1: Enable This flag works with AA filter configurations. bit9:8 = 2'b11
15:11	Reserved		
10:8	RW	0	Bit10 for debugging (LA trigger control) Bit9 Filter control 0: Normal output
7:1	Reserved		
0	RW	0	Display Controller Start 0: Stop 1: Start

4-3 FB0_OFFSET

Bits	R/W	POR	Description
31:20	RW	Unkown	Frame Buffer0 top address
19:0	R	0	Always 0

FB0_ADDR is a 32-bit byte address value. The address specifies the top of frame buffer address. The lowest 20 bits are not configurable (fixed as 0).

4-4 FB1_OFFSET

Bits	R/W	POR	Description
31:20	RW	Unkown	Frame Buffer1 top address
19:0	R	0	Always 0

FB1_ADDR is a 32-bit byte address value. The address specifies the top of frame buffer address. The lowest 20 bits are not configurable (fixed as 0).

4-5 FB0_MS_OFFSET

Bits	R/W	POR	Description
31:20	RW	Unkown	Anti-Alias Multi Sample Buffer1 top address
19:0	R	0	Always 0

FB0_MS_ADDR is a 32-bit byte address value. The address specifies the top of frame buffer address. The lowest 20 bits are not configurable (fixed as 0).

4-6 FB1_MS_OFFSET

Bits	R/W	POR	Description
31:20	RW	Unkown	Anti-Alias Multi Sample Buffer1 top address
19:0	R	0	Always 0

FB1_MS_ADDR is a 32-bit byte address value. The address specifies the top of frame buffer address. The lowest 20 bits are not configurable (fixed as 0).

4-7 COLOR_MODE

Bits	R/W	POR	Description
31:2	Reserved		
1:0	RW	0	11 = 8:8:8:8

			10 = 4:4:4:4 01 = 5:5:5:1 00 = 5:6:5

4-8 AXI_MASTER_CONFIG

Bits	R/W	POR	Description
31:0	Reserved		

4-9 INT_STATUS

Bits	R/W	POR	Description
31:17	Reserved		
16	RW	0	Vertex transfer DMA status 1 = Finished 0 = IDLE or not finished
8	RW	0	DMA status 1 = DMA is finished 0 = DMA is not finished, or IDLE
0	RW	0	V-sync status. 1 = In V-sync period 0 = Not in V-sync period

4-10 INT_CLEAR

Bits	R/W	POR	Description
31:1	Reserved		
0	RW	0	V-sync interrupt is clear when the bit is set. V-sync interrupt is also clear automatically when V-sync term is finished.

4-11 INT_MASK

Bits	R/W	POR	Description
31:1	Reserved		
2	RW	0	Vertex transfer DMA interrupt mask 1 = Mask 0 = Enable
1	RW	0	DMA interrupt mask 1 = Mask 0 = Enable
0	RW	0	V-sync interrupt mask 1 = Mask 0 = Enable

4-12 FRONT_BUFFER

Bits	R/W	POR	Description
31:1	Reserved		
0	RW	0	This specifies current frame buffer displayed on LCD 1 = Frame Buffer1 is displaying 0 = Frame Buffer0 is displaying

4-13 DMA_TOP_ADRS0-3

Bits	R/W	POR	Description
31:12	RW	Unknown	DMA0 Top Address
11:0	R	0	Always 0

4-14 DMA_BE_LENGTH

Bits	R/W	POR	Description
31:16	Reserved		
27:24	RW	Unknown	Byte enable
23:18	Reserved		
17:0	RW	Unknown	DMA transfer size.(32bit)

4-15 DMA_WD0,1

Bits	R/W	POR	Description
31:0	RW	Unknown	DMA Write data

4-16 DMA_CTRL

Bits	R/W	POR	Description
31:9	Reserved		
8	RW	0	DMA interrupt end flag
7:4	RW	00	DMA mode Bit4 : DMA0 enable Bit5: DMA1 enable Bit6: DMA2 enable Bit7: DMA3 enable
3:1	Reserved		
0	RW	0	DMA start 1 = In DMA processing 0 = Idle

4-17 RASTER_CTRL

Bits	R/W	POR	Description
31:19	Reserved		
18	R	0	Pixel Unit Idle
17	R	0	Texture Unit Idle
16	R	0	Raster Unit Idle
15:9	Reserved		
8	RW	0	0: Normal rendering 1: Anti-aliasing mode
7:1	Reserved		
0	RW	0	Start triangle rasterize. 1 = In processing 0 = Idle or finished

4-18 RASTER_CACHE_CTRL

Bits	R/W		POR	Description
31:9	Reserved			
8	RW		0	Color cache flush 1 = In cache flush processing 0 = Idle or cache flush finished
7:1	Reserved			
0	RW		0	Cache tag initialization. Color/Depth/Texture caches 1 = cache tag initialization

4-19 VTX_TOP_ADRS

Bits	R/W	POR	Description
31:16	RW	Unkown	Vertex Buffer Top Address
15:0	R	0	Always 0

4-20 VTX_TOTAL_SIZE

Bits	R/W	POR	Description
31:21	Reserved		
20:0	RW	Unkown	Vertex size to be transfered

4-21 NUM_OF_TRIANGLES

Bits	R/W	POR	Description
31:21	Reserved		
15:0	RW	Unkown	Number of triangles to be transferred

4-22 NUM_OF_ELEMENTS

Bits	R/W	POR	Description
31:5	Reserved		
4:0	RW	Unkown	Number of elements in one vertex

4-2 3 VTX_DMA_CTRL

Bits	R/W	POR	Description
31:9	Reserved		
8	RW	0	DMA interrupt end flag
7:1	Reserved		
0	RW	0	DMA start 1 = In DMA processing 0 = Idle

4-2 4 TEX_OFFSET

Bits	R/W	POR	Description
31:20	RW	Unkown	Texture Top Address
19:0	Reserved		

4-2 5 TEX_WIDTH_M1

Bits	R/W	POR	Description
31:22	Reserved		
21: 0	RW	Unkown	Texture Width-1 (22-bit floating point format)

4-2 6 TEX_HEIGHT_M1

Bits	R/W	POR	Description
31:22	Reserved		
21: 0	RW	Unkown	Texture Height -1(22-bit floating point format)

4-2 7 TEX_WIDTH_UI

Bits	R/W	POR	Description
31:22	Reserved		
21: 0	RW	Unkown	Texture Height -1(unsigned integer format)

4-28 TEX_CONFIG

Bits	R/W	POR	Description
31:11	Reserved		
10: 8	RW	0	Texture Color Mode 100 = ETC 011 = 8:8:8:8 010 = 4:4:4:4 001 = 5:5:5:1 000 = 5:6:5
7:0	Reserved		

4-29 TEX_ENABLE

Bits	R/W	POR	Description
31:2	Reserved		
0	RW	0	Texture enable 0 = disable 1 = enable

4-30 TEX_BLEND_ENABLE

Bits	R/W	POR	Description
31:2	Reserved		
0	RW	0	Texture and primary color blend enable 0 = disable 1 = enable

4-3 1 SCREEN_MODE

Bits	R/W	POR	Description
31:9	Reserved		
8	RW	0	Buffer Offset. This is for anaglyph rendering 1=Multi-Sample Buffer (Both Color and Depth) 0=Normal Buffer
7:2	Reserved		
0	RW	0	Screen Vertical Flip 1=Flip 0=Normal

4-3 2 COLOR_OFFSET

Bits	R/W	POR	Description
31:20	RW	Unkown	Color Buffer address offset
19:0	Reserved		

4-3 3 COLOR_MS_OFFSET

Bits	R/W	POR	Description
31:20	RW	Unkown	Color buffer (multi-sample)address offset
19:0	Reserved		

4-3 4 DEPTH_OFFSET

Bits	R/W	POR	Description
31:20	RW	Unkown	Depth buffer address offset
19:0	Reserved		

4-3 5 DEPTH_MS_OFFSET

Bits	R/W	POR	Description
31:20	RW	Unkown	Depth buffer (multi-sample)address offset
19:0	Reserved		

4-36 BLEND_OPERATION

Bits	R/W	POR	Description
31:28	Reserved		
27:24	RW	0	Destination blending factor. Same as source
23:20	Reserved		
19:16	RW	0	Source blending factor 14 = SRC_ALPHA_SATURATE 13 = ONE_MINUS_CONSTANT_ALPHA 12 = CONSTANT_ALPHA 11 = ONE_MINUS_CONSTANT_COLOR 10 = CONSTANT_COLOR 9 = ONE_MINUS_DST_ALPHA 8 = DST_ALPHA 7 = ONE_MINUS_SRC_ALPHA 6 = SRC_ALPHA 5 = ONE_MINUS_DST_COLOR 4 = DST_COLOR 3 = ONE_MINUS_SRC_COLOR 2 = SRC_COLOR 1 = ONE 0 = ZERO
15:9	Reserved		
10:8	RW	0	Blend Equation 5 = ADD_SCREEN 4 = MAX 3 = MIN 2 = REV_SUB 1 = SUB 0 = ADD
7:1	Reserved		
0	RW	0	Color Blend enable 1 = enable 0 = disable

4-37 DEPTH_TEST

Bits	R/W	POR	Description
31:28	Reserved		
31:19	Reserved		
18:16	RW	0	Depth function 7 = ALWAYS 6 = GEQUAL 5= NOTEQUAL 4 = GREATER 3 = LEQUAL 2 = EQUAL 1 = LESS 0 = NEVER
15:9	Reserved		
8	RW	0	Depth mask 1 = read and write buffer 0 = read-only buffer
7:1	Reserved		
0	RW	0	Depth test enable 1 = enable 0 = disable

4-38 VTX_ATTR

Bits	R/W	POR	Description
31:30	Reserved		
29:28	RW	0	Attribute1 size 00 = no element 01 = 1 element 10 = 2 elements(U/V) 11 = 3 elements(R,G,B)
27:26	Reserved		
25:24	RW	0	Attribute1 kind 00 = Primary Color 10 = Texture0
23:17	Reserved		
16	RW	0	Attribute1 enable 1 = enable 0 = disable
15:14	Reserved		
13:12	RW	0	Attribute0 size 00 = no element 01 = 1 element 10 = 2 elements(U/V) 11 = 3 elements(R,G,B)
11:10	Reserved		
9:8	RW	0	Attribute0 kind 00 = Primary Color 10 = Texture0
7:1	Reserved		
0	RW	0	Attribute0 enable 1 = enable 0 = disable

5 IO Ports

5 - 1 Clock&Reset

Name	Bits	Direction	Description
clk_core	1	In	Main clock
clk_v	1	In	Video clock
rst_x	1	In	Async reset

5 - 2 Interrupt

Name	Bits	Direction	Description
o_int	1	Out	Interrupt Out, level

5 - 3 AXI4 Slave

5 - 3 - 1 Write Address Channel

Name	Bits	Direction	Description
i_awvalid_s	1	In	Valid write address channel transfer indicator
i_awaddr_s[31:0]	32	In	The address of the first transfer in a write transaction
i_awburst_s[1:0]	2	In	Address changes between each transfer in a write transaction
i_awcache_s[3:0]	4	In	Write transaction progress through a system
i_awid_s[3:0]	4	In	Identification tag for a read transaction
i_awlen_s[3:0]	4	In	The exact number of data transfers in a write transaction
i_awlock_s[1:0]	2	In	The atomic characteristics of a write transaction
i_awprot_s[2:0]	3	In	Protection attributes of a write transaction
i_awsize_s[2:0]	3	In	The number of bytes in each data transfer in a write transaction
o_awready_s	1	Out	Write address channel transfer acceptance

5 - 3 - 2 Write Data Channel

Name	Bits	Direction	Description
i_wvalid_s	1	In	Valid write data indicator
i_wstrb_s[3:0]	4	In	Write data strobe
i_wid_s[3:0]	4	In	Identification tag for write data
i_wdata_s[31:0]	32	In	Write data
i_wlast_s	1	In	Last write data transfer indicator
o_wready_s	1	Out	Write data acceptance

5 - 4 Write Response Channel

Name	Bits	Direction	Description
o_bvalid_s	1	Out	Valid write response channel transfer indicator
o_bid_s[3:0]	4	Out	Identification tag for a write response
o_bresp_s[1:0]	2	Out	The status of a write transaction
i_bready_s	1	In	Write response acceptance

5 - 4 - 1 Read Address Channel

Name	Bits	Direction	Description
i_arvalid_s	1	In	Valid Write data acceptance indicator
i_araddr_s[31:0]	32	In	The address of the first transfer in a read transaction
i_arburst_s[1:0]	2	In	Address changes between each transfer in a read transaction
i_arcache_s[3:0]	4	In	Read transaction progress through a system
i_arid_s[3:0]	4	In	Identification tag for a read transaction
i_arlen_s[3:0]	4	In	The exact number of data transfers in a read transaction
i_arlock_s[1:0]	2	In	The atomic characteristics of a read transaction
i_arprot_s[2:0]	3	In	Protection attributes of a read transaction

i_arsize_s[2:0]	3	In	The number of bytes in each data transfer in a read transaction
o_arready_s	1	Out	Read data acceptance acceptance

5 - 4 - 2 Read Data Channel

Name	Bits	Direction	Description
o_rvalid_s	1	Out	Valid read channel transfer indicator
o_rid_s[3:0]	4	Out	Identification tag for read data and response
o_rdata_s[31:0]	32	Out	Read data
o_rlast_s	1	Out	Last read data indicator
i_rready_s	1	In	Read data acceptance

5 - 5 AXI4 Master

5 - 5 - 1 Write Channel

Name	Bits	Direction	Description
o_awvalid_m	1	Out	Valid write address channel transfer indicator
o_awaddr_m[31:0]	32	Out	The address of the first transfer in a write transaction
o_awburst_m[1:0]	2	Out	Address changes between each transfer in a write transaction
o_awcache_m[3:0]	4	Out	Write transaction progress through a system
o_awid_m[3:0]	4	Out	Identification tag for a write transaction
o_awlen_m[4:0]	5	Out	The exact number of data transfers in a write transaction
o_awlock_m[1:0]	2	Out	The atomic characteristics of a write transaction
o_awprot_m[2:0]	3	Out	Protection attributes of a write transaction
o_awsize_m[2:0]	3	Out	The number of bytes in each data

			transfer in a write transaction
o_awuser_m[4:0]	5	Out	User-defined extension for the write address channel
i_awready_m	1	In	Read address channel transfer acceptance

5 - 5 - 2 Write Data Channel

Name	Bits	Direction	Description
o_wvalid_m	1	Out	Valid write channel transfer indicator
o_wstrb_m[7:0]	8	Out	Wrie data strobe
o_wid_m[3:0]	4	Out	Identification tag for write data
o_wdata_m[63:0]	64	Out	Write data
o_wlast_m	1	Out	Last data indicator
i_wready_m	1	In	Write data acceptance

5 - 5 - 3 Write Response Channel

Name	Bits	Direction	Description
i_bvalid_m	1	In	Valid write response channel transfer indicator
i_bid_m[3:0]	4	In	Identification tag for a write response
i_bresp_m[1:0]	2	In	The status of a write transaction
o_bready_m	1	Out	Write response acceptance

5 - 5 - 4 Read Address Channel

Name	Bits	Direction	Description
o_arvalid_m	1	Out	Valid read address channel transfer indicator
o_araddr_m[31:0]	32	Out	The address of the first transfer in a read transaction
o_arburst_m[1:0]	2	Out	Address changes between each transfer in a read transaction
o_arcache_m[3:0]	4	Out	Read transaction progress through a

			system
o_arid_m[3:0]	4	Out	Identification tag for a read transaction
o_arlen_m[4:0]	5	Out	The exact number of data transfers in a read transaction
o_arlock_m[1:0]	2	Out	The atomic characteristics of a read transaction
o_arprot_m[2:0]	3	Out	Protection attributes of a read transaction
o_arsize_m[2:0]	3	Out	The number of bytes in each data transfer in a read transaction
o_aruser_m[4:0]	5	Out	User-defined extension for the read address channel
i_arready_m	1	In	Read address channel transfer acceptance

Read Data Channel

Name	Bits	Direction	Description
i_rvalid_m	1	In	Valid read channel transfer indicator
i_rid_m[3:0]	4	In	Identification tag for read data and response
i_rdata_m[63:0]	64	In	Read data
i_rlast_m	1	In	Last read data indicator
o_rready_m	1	Out	Read data acceptance

5 - 6 Video

Name	Bits	Direction	Description
o_hsync_x	1	Out	H-sync
o_vsync_x	1	Out	V-sync
o_vr[7:0]	8	Out	Red color
o_vg[7:0]	8	Out	Green color
o_vb[7:0]	8	Out	Blue color

6 Internal Floating Point Format

Rasterizer uses 22-bit floating-point format number internally. The format has 1-bit sign, 7-bit exponent and 16-bit mantissa. Note that 16-bit mantissa contains explicit one integer bit. It is not same as IEEE floating format, their format does not have implicit integer bit. The explicit integer bit reduces fraction resolution, but it has several advantages, when the intermediate successive floating point calculation in hardware.

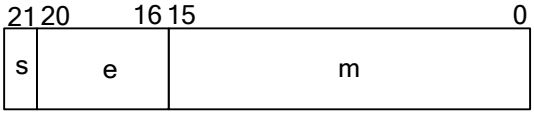


Figure 6 22-bit floating point format

$$\text{Value} = -1^{s} \times \text{m} \times 2^{e-15}$$

Bias = 15(Fh)
m = 1.15(1bit integer, 15bit fraction part)

s	e	m	Value
0	0x0f	0x8000	1.0
0	0x1f	0xffff	131071.0(positive max. number)
0	0x0e	0x8000	0.5
0	0x0e	0xc000	0.75
0	0x0d	0x8000	0.25
0	0x02	0x8000	0.000122
0	0x01	0x8000	0.000061
0	0x00	0x8000	0.000031(denormal)
0	0x00	0x0000	0
1	0xf	0x8000	-1.0
1	0x1f	0xffff	-131071.0.0
1	0xe	0x800	-0.5
1	0xe	0x800	-0.75
1	0x1	0x800	-0.000061
1	0x0	0x800	-0.000031(denormal)

Table 5 22-bit floating-point value example

Biased e	Actual exponent	Biased e	Actual exponent
0x1f	2^{16}	0x0f	2^{0}
0x1e	2^{15}	0x0e	2^{-1}
0x1d	2^{14}	0x0d	2^{-2}
0x1c	2^{13}	0x0c	2^{-3}
0x1b	2^{12}	0x0b	2^{-4}
0x1a	2^{11}	0x0a	2^{-5}
0x19	2^{10}	0x09	2^{-6}
0x18	2^{9}	0x08	2^{-7}
0x17	2^{8}	0x07	2^{-8}
0x16	2^{7}	0x06	2^{-9}
0x15	2^{6}	0x05	2^{-10}
0x14	2^{5}	0x04	2^{-11}
0x13	2^{4}	0x03	2^{-12}
0x12	2^{3}	0x02	2^{-13}
0x11	2^{2}	0x01	2^{-14}
0x10	2^{1}	0x00	Denormal Number

Table 6 Biased exponent and actual exponent