

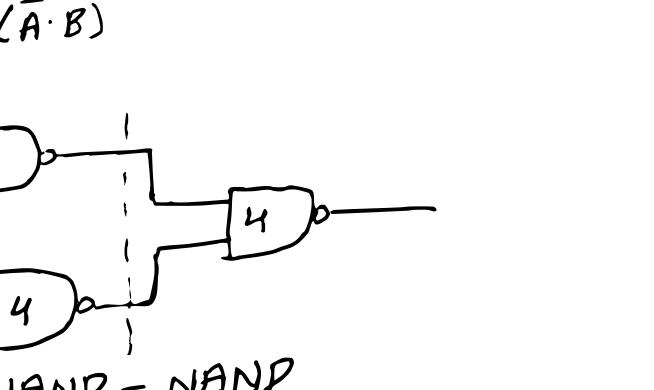
Universality

Truth table

A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

$$C = A \cdot \bar{B} + \bar{A} \cdot B$$

SOP \rightarrow Sum of Products

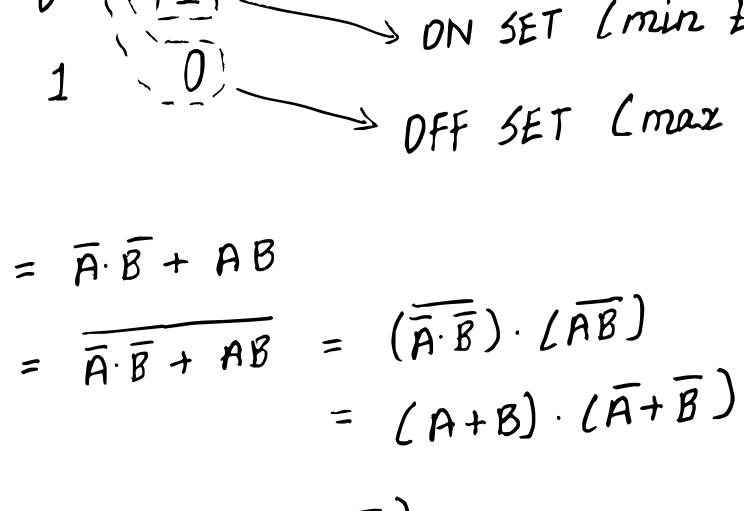


$$C = A \cdot \bar{B} + \bar{A} \cdot B$$

AND-OR

$$C = \bar{C} = \overline{A \cdot \bar{B} + \bar{A} \cdot B}$$

$$= (\overline{A \cdot \bar{B}}) \cdot (\overline{\bar{A} \cdot B})$$



NAND - NAND

TRUTH-TABLE \rightarrow SOP \rightarrow Optimize \rightarrow SOP
 (Boolean Algebra) \rightarrow (AND-OR) \rightarrow (NAND-NAND)

A	B	Z	2^n bits
m_0 0 0 1 \overline{D}			
m_1 0 1 1 $\overline{1}$			
m_2 1 0 1 $\overline{1}$			
m_3 1 1 0 $\overline{0}$			

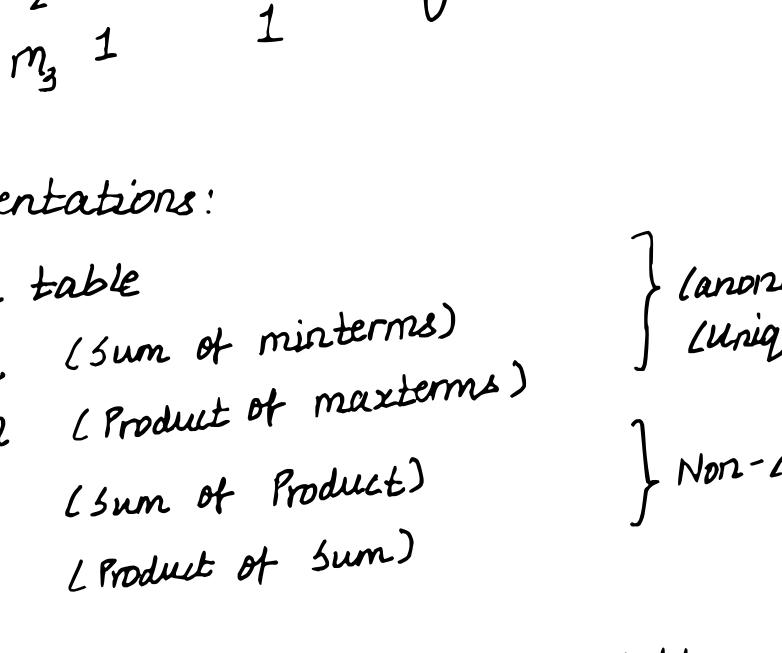
$$Z = A \cdot \bar{B} + \bar{A} \cdot B \quad (\text{SOP})$$

$$Z = \overline{\overline{A \cdot \bar{B} + \bar{A} \cdot B}} = (\overline{\overline{A \cdot \bar{B}}}) \cdot (\overline{\overline{\bar{A} \cdot B}})$$

$$= (A+B) \cdot (\bar{A}+\bar{B})$$

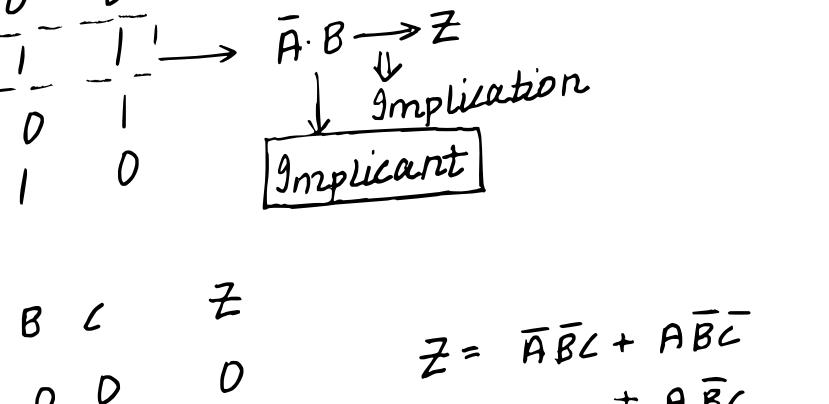
$$\therefore Z = (A+B)(\bar{A}+\bar{B})$$

\hookrightarrow Product of Sum (POS)



$$Z = (A+B) \cdot (\bar{A}+\bar{B})$$

$$\bar{Z} = (\overline{A+B}) \cdot (\overline{\bar{A}+\bar{B}}) = (\overline{A+B}) + (\overline{\bar{A}+\bar{B}})$$



Representations:

Truth table

SOM (Sum of minterms)

POM (Product of maxterms)

SOP (Sum of Product)

POS (Product of Sum)

} Canonical (unique)

} Non-canonical

minterms \rightarrow product of all variables
 (Intersection \rightarrow min.)

maxterms \rightarrow sum of all variables
 (Union \rightarrow max.)

$$A \ B \ Z$$

$$0 \ 0 \ 0 \ \overline{D}$$

$$\overline{0} \ \overline{1} \ \overline{1} \ \overline{1}$$

$$1 \ 0 \ 1 \ \overline{1}$$

$$1 \ 1 \ 0 \ \overline{0}$$

$$1 \ 1 \ 1 \ \overline{1}$$

$$Z = \bar{A} \cdot \bar{B} \cdot \bar{C} + A \cdot \bar{B} \cdot \bar{C}$$

$$+ A \cdot \bar{B} \cdot C$$

$$+ A \cdot B \cdot \bar{C}$$

$$+ A \cdot B \cdot C$$

\hookrightarrow SOM & SOP

$$Z = A + \bar{B} \cdot \bar{C}$$

\hookrightarrow SOP but not SOM

n inputs

$A \cdot B \cdot C \rightarrow 0\text{-implicant} \Rightarrow n-D \text{ literals}$

$\bar{B} \cdot C \rightarrow 1\text{-implicant} \Rightarrow n-1 \text{ literals}$

$A \rightarrow 2\text{-implicant} \Rightarrow n-2 \text{ literals}$

Literals \rightarrow variables in either normal form or complement form

($A, \bar{A} \rightarrow$ different literals)

Representations:

TRUTH TABLE

S0m

PDM2

SOP

POS

} Canonical

} Non-Canonical

Cost (min # switches):

$$Z = AB + CD$$

$$= \overline{AB} \cdot \overline{CD}$$

AND-OR

No. of literals + No. of product terms

4 + 2

$$(4+2) \times 2 = 12$$

CMOS

Optimization:

KARNAUGH (BELL LAB)

Graphical Method

A	Z
0	1
1	1

$$Z = 1$$

A D 1
1 1 → 0-implicant

$$Z = A + \bar{A}$$

= 1// → 1-implicant

A	B	Z
0	0	1
0	1	1
1	0	0
1	1	0

$$Z = \bar{A}\bar{B} + \bar{A}B$$

$$Z = \bar{A}(\bar{B} + B) = \bar{A} \cdot 1$$

$$\underline{Z = \bar{A}}$$

A	0	1
0	1	0
1	1	0

$$Z = \bar{A}\bar{B} + \bar{A}B$$

$$Z = \bar{A}(\bar{B} + B) = \bar{A} \cdot 1$$

$$\underline{Z = \bar{A}}$$

$$Z = \bar{B}$$

Pair 1-implicant

00	01	11	10
1	0	0	(1)

$$Z = \bar{B}$$

Pair 1-implicant

00	01	11	10
1	1	1	1

$$Z = 1$$

$$Z = A + \bar{A} = 1$$

A	D	1
0	1	1
1	1	1

$$Z = \bar{B}$$

2-implicant Quad

AB	00	01	11	10
0	1	1	1	1
1	1	1	1	1

$$Z = 1$$

$$Z = A + \bar{A} = 1$$

AB	00	01	11	10
0	1	1	1	1
1	1	1	1	1

$$Z = 1$$

$$Z = A + \bar{A} = 1$$

AB	00	01	11	10
0	1	1	1	1
1	1	1	1	1

$$Z = 1$$

$$Z = A + \bar{A} = 1$$

AB	00	01	11	10
0	1	1	1	1
1	1	1	1	1

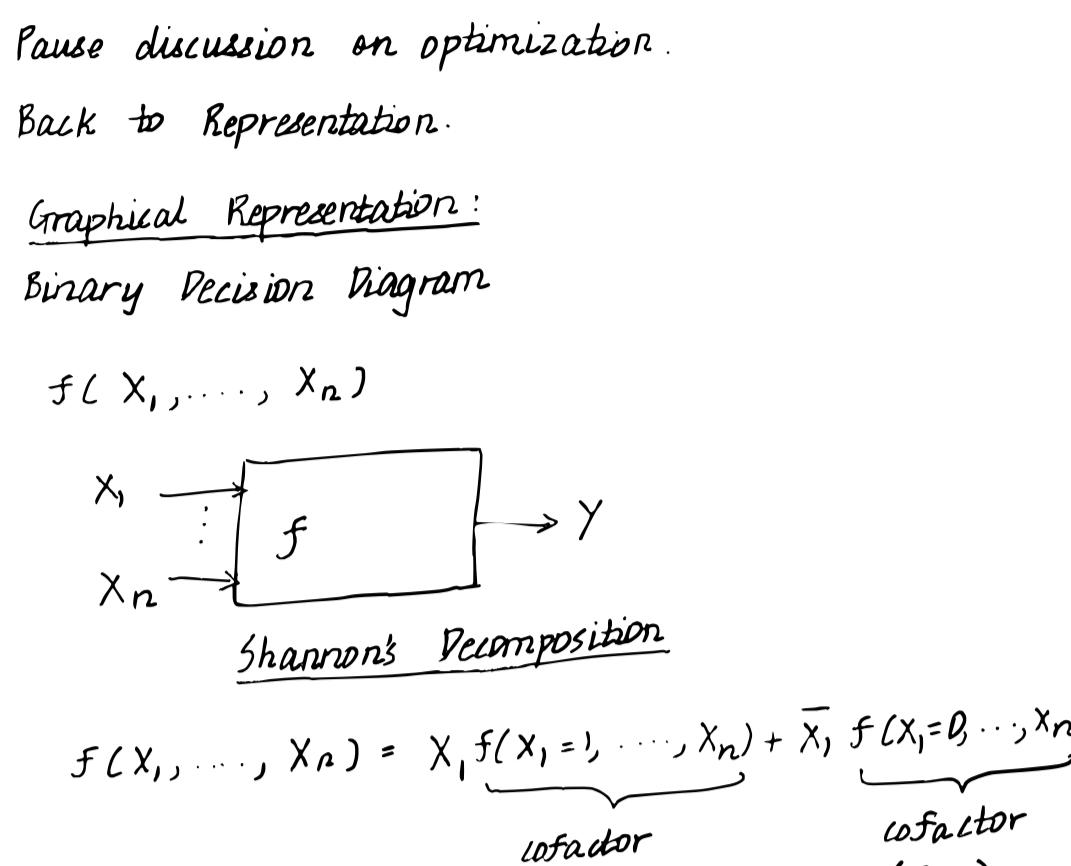
$$Z = 1$$

$$Z = A + \bar{A} = 1$$

Representation:

- | | | |
|----------------|---|---------------|
| 1. Truth Table | } | Canonical |
| 2. SDM | | |
| 3. PDM | } | Non-canonical |
| 4. SDP | | |
| 5. PDS | | |

K-map



EPI —

RPI X

SPI ← optimization ← Patrick's Method

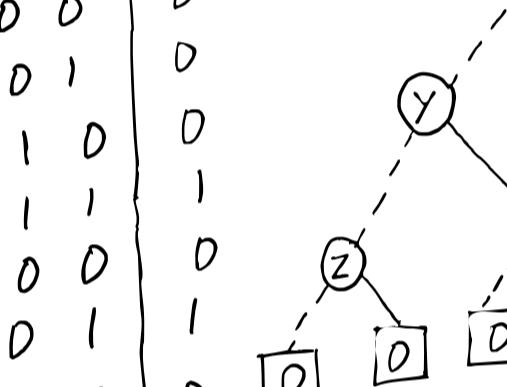
Pause discussion on optimization.

Back to Representation.

Graphical Representation:

Binary Decision Diagram

$$f(x_1, \dots, x_n)$$

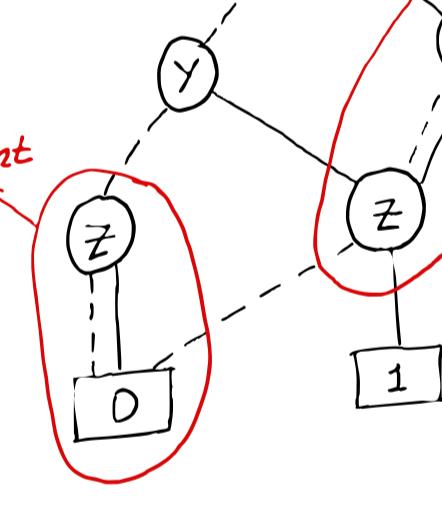


Shannon's Decomposition

$$f(x_1, \dots, x_n) = x_1 \underbrace{f(x_1=1, \dots, x_n)}_{\text{ufactor}} + \bar{x}_1 \underbrace{f(x_1=0, \dots, x_n)}_{\text{cofactor}} (f_{\bar{x}_1})$$

$$\therefore f(x_1, x_2, \dots, x_n) = x_1 f_{x_1} + \bar{x}_1 f_{\bar{x}_1}$$

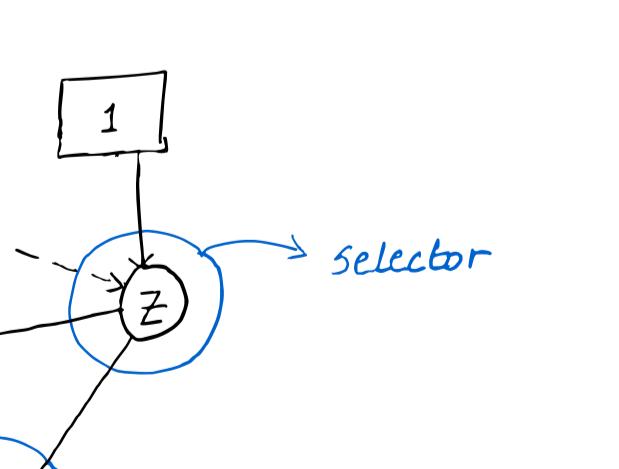
$\equiv x_1 f_{x_1} \oplus \bar{x}_1 f_{\bar{x}_1}$ (if A, B are orthogonal, $A+B \equiv A \oplus B$)



and so on...

example:

X	Y	Z	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1



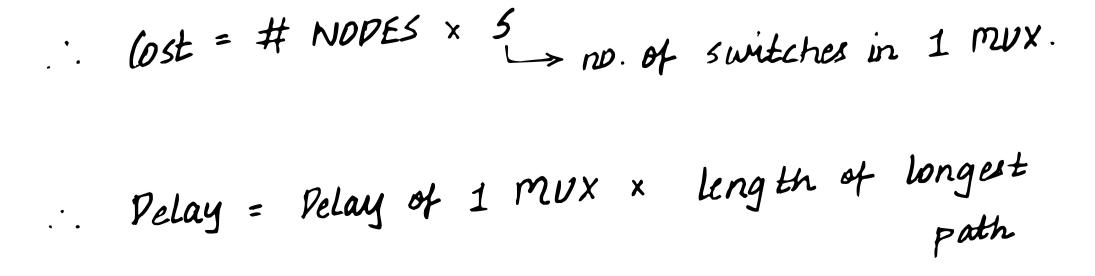
\hookrightarrow Ordered Binary Decision Tree

But this has many redundancies:

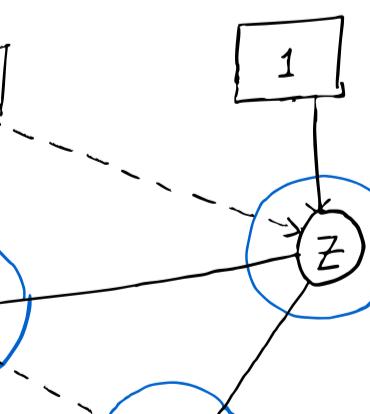
→ Only 2 bits required for 0,1.

$$(No. \text{ of nodes} = 2^n - 1 + 2 = 2^n + 1)$$

→ Isomorphic nodes can be merged together.



\hookrightarrow Redundant nodes can be eliminated.



Reduced Ordered Binary Decision Diagram (ROBDD)

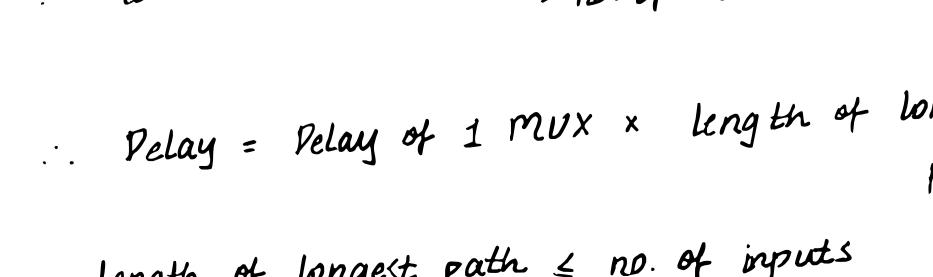
(Not a tree anymore)

(ROBDD)

ROBDD is canonical.

→ Can be used to verify equivalence of two functions.

→ Can be directly used for synthesis of circuit.



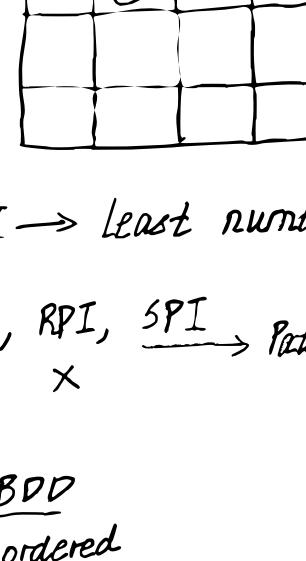
selector → can be replaced by 2:1 MUX.

$\therefore \text{lost} = \# \text{ NODES} \times 5 \rightarrow \text{no. of switches in 1 MUX.}$

$\therefore \text{Delay} = \text{Delay of 1 MUX} \times \text{length of longest path}$

length of longest path \leq no. of inputs

K-Map:



PI \rightarrow Least number of literals

EPI, RPI, SPI \rightarrow Patrick's Method

RDBDD
ordered
① Binary Decision Tree $\rightarrow (2^{N+1} - 1 \text{ nodes})$

② 3 Reduction Rules
 $f_1 = f_2$ \downarrow Directed Acyclic Graph
RDBDD (Canonical)

Uses:
① Verification
 $f_1 = f_2$

(Adder \rightarrow linear growth)
(Multiplier \rightarrow exponential growth)

② Synthesis

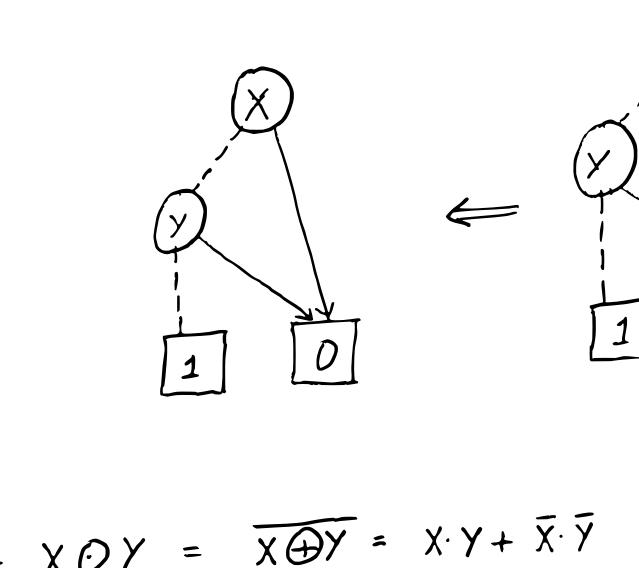
$$f_1(x_1, x_2, \dots, x_i, \dots, x_n) = x_i f_{1x_i} + \bar{x}_i f_{1\bar{x}_i}$$

$$f_2(x_1, x_2, \dots, x_i, \dots, x_n) = x_i f_{2x_i} + \bar{x}_i f_{2\bar{x}_i}$$

$$f_1 + f_2 = x_i (f_{1x_i} + f_{2x_i}) + \bar{x}_i (f_{1\bar{x}_i} + f_{2\bar{x}_i})$$

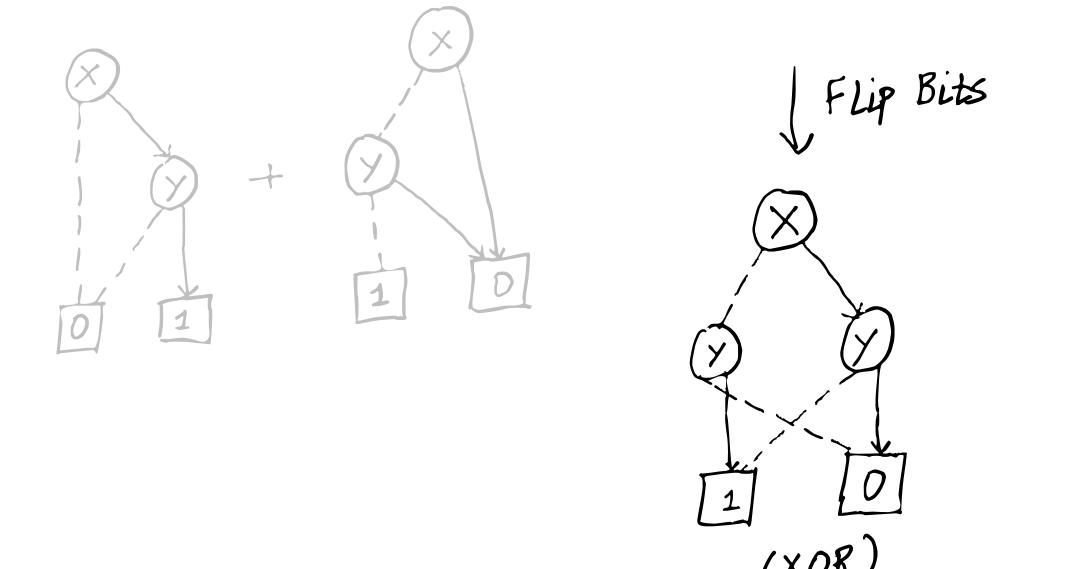
$$f_1 \cdot f_2 = x_i (f_{1x_i} f_{2x_i}) + \bar{x}_i (f_{1\bar{x}_i} f_{2\bar{x}_i})$$

$$\therefore f_1 \cdot \text{op. } f_2 = x_i (f_{1x_i} \cdot \text{op. } f_{2x_i}) + \bar{x}_i (f_{1\bar{x}_i} \cdot \text{op. } f_{2\bar{x}_i})$$



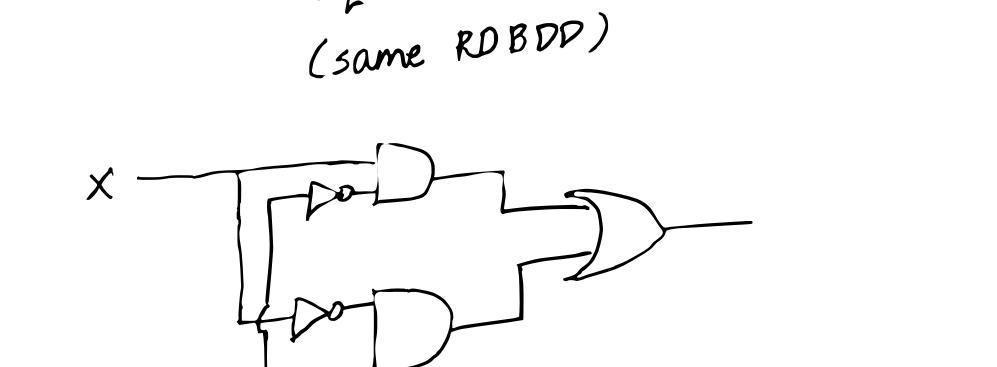
$$F_1 = \bar{x}, F_2 = \bar{y}$$

$$F = F_1 \cdot F_2 \quad (x > y)$$



$$F = x \oplus y = \bar{x} \oplus \bar{y} = x \cdot y + \bar{x} \cdot \bar{y}$$

$$(XNDR)$$



$$\therefore x \oplus y:$$

equivalent to
(same RDBDD)

Representation:

TRUTH TABLE	} CANONICAL
SOP	
PDM	
RDBDD	
SDP	} NON-CANONICAL
POS	

RM \leftarrow Reed Muller Decomposition

Shannon's Decomposition:

$$f(x_1, x_2, \dots, x_n) = x_i f_{x_i} + \bar{x}_i f_{\bar{x}_i}$$
$$= x_i f_{x_i} \oplus \bar{x}_i f_{\bar{x}_i}$$

Positive Davis Decomposition:

$$f(x_1, x_2, \dots, x_n) = f_{\bar{x}_i} \oplus x_i (f_{\bar{x}_i} \oplus f_{x_i})$$

↓
ALL literals un-complemented.
pure form

$$f(x_1, \dots, x_n) = f_{x_i} \oplus \bar{x}_i (f_{\bar{x}_i} \oplus f_{x_i})$$

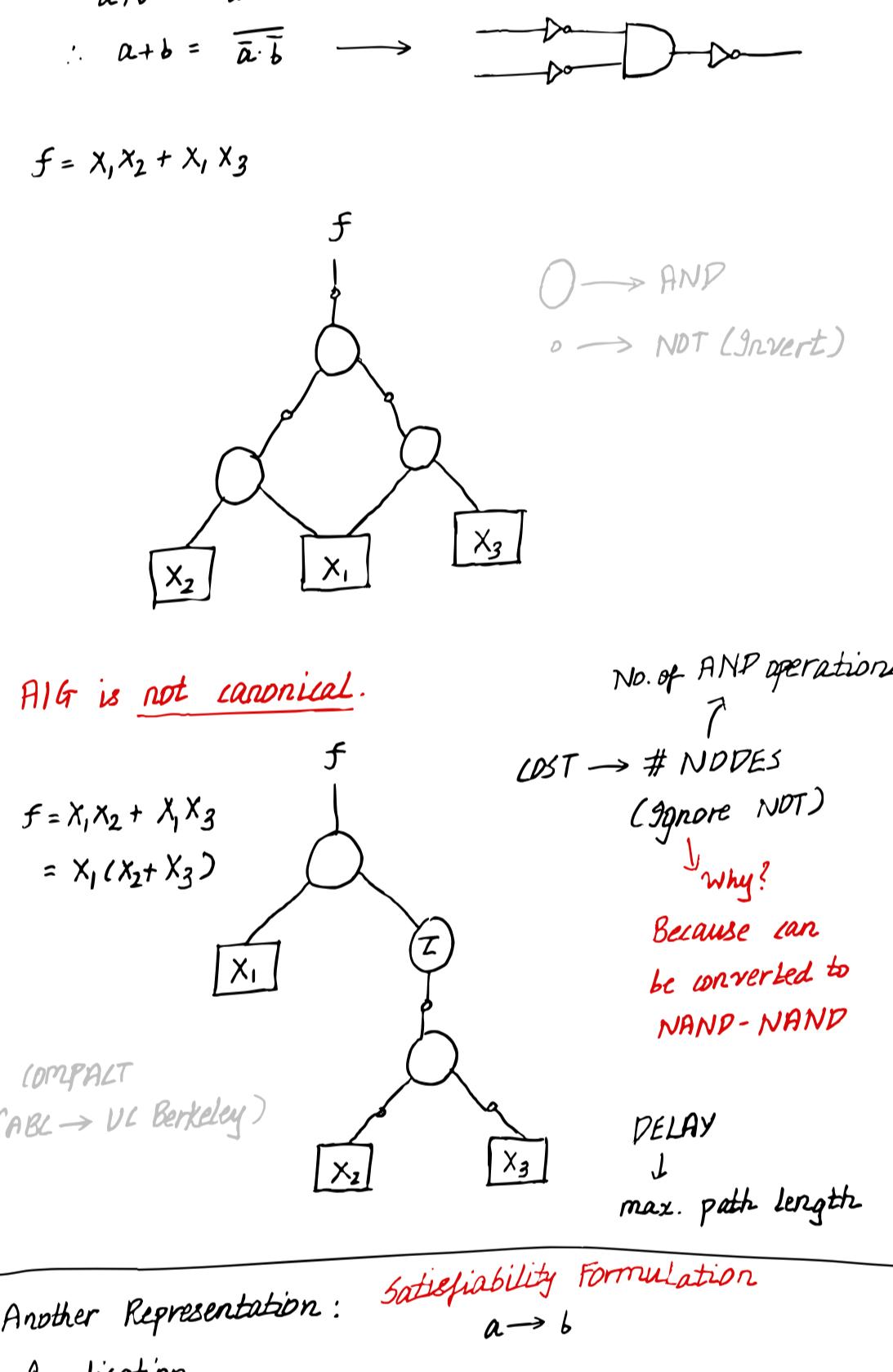
↓
ALL literals complemented.

$$f = x_i f_{x_i} \oplus \bar{x}_i f_{\bar{x}_i} \quad \boxed{\bar{x}_i = 1 \oplus x_i}$$
$$= x_i f_{x_i} \oplus (1 \oplus x_i) f_{\bar{x}_i}$$
$$= x_i f_{x_i} \oplus f_{\bar{x}_i} \oplus x_i f_{\bar{x}_i}$$
$$= f_{\bar{x}_i} \oplus x_i (f_{x_i} \oplus f_{\bar{x}_i})$$
$$f_{x_i} = f_{x_i \bar{x}_j} \oplus x_j (f_{x_i x_j} \oplus f_{x_i \bar{x}_j})$$
$$f_{\bar{x}_i} = f_{\bar{x}_i \bar{x}_j} \oplus x_j (f_{\bar{x}_i x_j} \oplus f_{\bar{x}_i \bar{x}_j})$$
$$f(x_1, x_2, \dots, x_n) = a_0 \oplus a_1 x_1 \oplus a_2 x_2 \oplus a_3 x_3 \dots$$

REED MULLER REPRESENTATION \rightarrow $\oplus a_{n+1} x_1 x_2 \oplus a_{n+2} x_1 x_3 \dots$
 $\oplus a_r x_1 x_2 x_3 \oplus a_{r+1} x_1 x_2 x_4$
 $\oplus \dots \dots \oplus a_m x_1 x_2 \dots x_n$

where $a_i \in \{0, 1\}$.

\therefore Only AND, XDR Gates needed



$f(a, b, c) = ac + bc$

$$f_a = c + bc = c$$

$$f_{\bar{a}} = bc$$

$$\therefore f = f_{\bar{a}} \oplus a (f_{\bar{a}} \oplus f_a)$$
$$= bc \oplus a(bc \oplus c)$$
$$= bc \oplus ac \oplus abc$$

$$f(a, b) = ab + \bar{a}\bar{b}$$

$$f_{\bar{a}} = \bar{b}$$

$$f_a = b$$

$$\therefore f = f_{\bar{a}} \oplus a(f_{\bar{a}} \oplus f_a)$$
$$= \bar{b} \oplus a(\bar{b} \oplus b)$$
$$= \bar{b} \oplus a$$
$$= 1 \oplus b \oplus a$$

REED MULLER REPRESENTATION
CANNOT HAVE COMPLEMENTED LITERALS.

$$f_{\bar{b}} = \bar{a} = 1 \oplus a$$

$$f_b = a$$

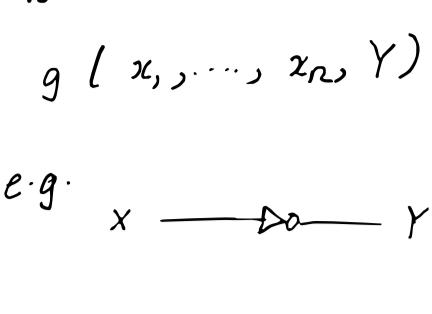
$$\therefore f = f_{\bar{b}} \oplus b(f_{\bar{b}} \oplus f_b)$$

$$= 1 \oplus a \oplus b(1 \oplus a \oplus b)$$

$$= 1 \oplus a \oplus b$$

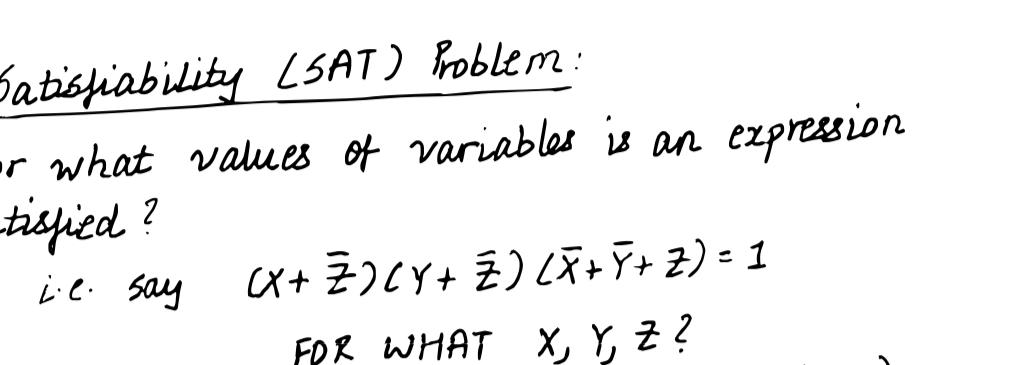
$$= 1 \oplus b \oplus a$$

Satisfiability Formulation:



$$g(x_1, \dots, x_n, Y)$$

e.g. $x \rightarrow y \Rightarrow (x+y)(\bar{x}+\bar{y}) = 1$



Conjunctive Normal Form (CNF)

conjunction of disjunctions

SOP
↓
Disjunctive Normal form (DNF)

Satisfiability (SAT) Problem:

For what values of variables is an expression satisfied?

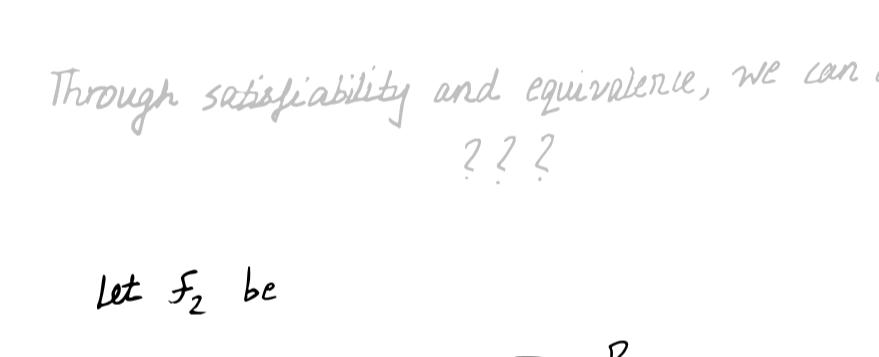
i.e. say $(x+\bar{z})(y+\bar{z})(\bar{x}+\bar{y}+z) = 1$

FOR WHAT x, y, z ?

$(1, 1, 1)$ works here)

Equivalence Checking:

To check if two functions are equivalent or not, we can use XDR.



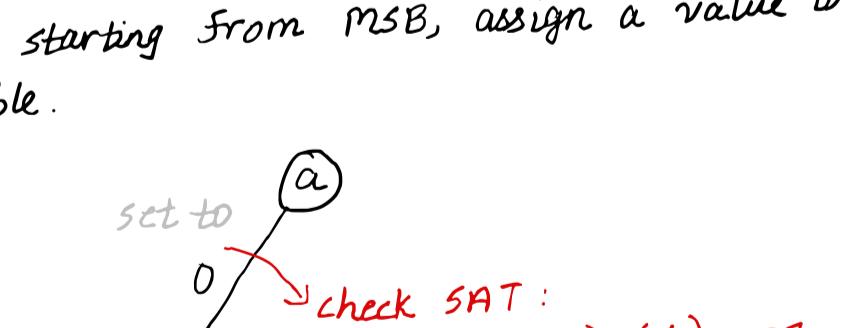
If $f_1 = f_2$, $f_1 \oplus f_2 = 0$ X

Thus, if we find even 1 x for which $f_1 \oplus f_2 = 1$, we can say that the two functions are not equivalent.

i.e. If we find a solution to the SAT problem for $f_1 \oplus f_2$, then f_1, f_2 are not equivalent.

e.g. Let $f_1 = \bar{A}B + A\bar{B} = K$

↓



SAT problem for f_1 :

$$G_1 : (B+\bar{D})(\bar{B}+D) = 1$$

+ 2

$$G_2 : (A+C)(\bar{A}+\bar{C}) = 1$$

+ 3

$$G_3 : (\bar{A}+\bar{D}+E)(A+\bar{E})(D+\bar{E}) = 1$$

+ 3

$$G_4 : (\bar{B}+\bar{C}+F)(B+F)(C+\bar{F}) = 1$$

+ 3

$$G_5 : (E+F+\bar{G})(\bar{E}+G)(\bar{F}+G) = 1$$

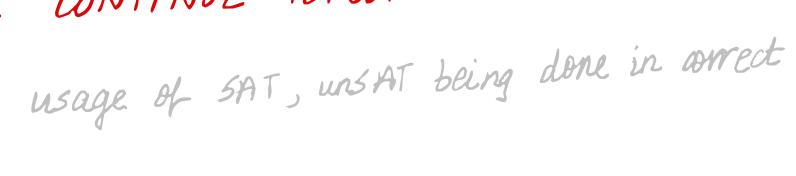
13 clauses

$$G_1 \cdot G_2 \cdot G_3 \cdot G_4 \cdot G_5 = 1$$

$$\underbrace{\quad}_{\text{13 clauses}} = 1$$

Through satisfiability and equivalence, we can debug a circuit.
???

Let f_2 be



SAT problem:

$$G_1 \cdot G_2 \cdot G_3 \cdot G_4 = 1$$

each has 3 clauses

$$\rightarrow 4 \times 3 = 12 \text{ clauses}$$

Continuity ???

Solving SAT problem: DPLL Method :

Davis-Putnam \leftarrow DP \rightarrow introduced

Logemann-Loveland \leftarrow LL \rightarrow Refined ???

based on backtracking.

what? Let's see.

let's learn through an example:

say $(a+\bar{c})(b+\bar{c})(\bar{a}+\bar{b}+c) = 1$ is our SAT problem.

let's set an order, say $a > b > c$.

Now, starting from MSB, assign a value to each variable.

If it would have been unSAT, we would have backtracked to b, then to a until we would have exhausted all possibilities.

\hookrightarrow i.e. Worst Case Backtracking: 2^n for n variables.

can we improve this?

WILL CONTINUE TOMORROW

Q.] Is usage of SAT, unsAT being done in correct context?

Representation:

Truth Table

SOP

PDM

RDBDD

RM

SOP

POS

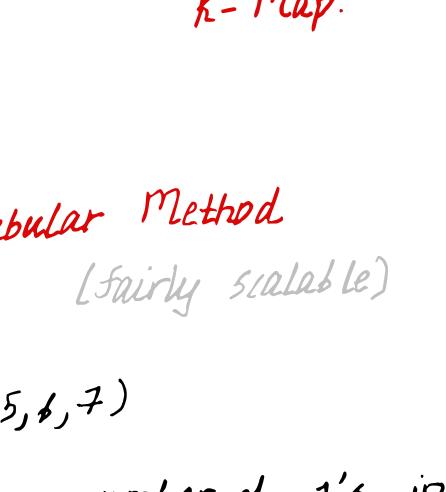
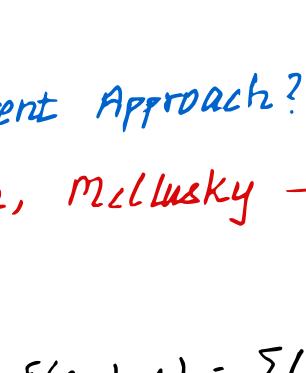
ALG

Canonical

Non-canonical

Optimization:

K-Map



Metric \rightarrow Cost : $\min \{ \# \text{ literals} + \# \text{ terms} \}$

Delay : $\min \{ \max \{ \# \text{ literals in a term} \} + \# \text{ terms} \}$

Power : similar to cost

can be visualized till 6 variables (3D),
 beyond that, it is difficult. \leftarrow Limitation of K-Map.

Different Approach?

Quinn, McClusky \rightarrow Tabular Method

(Fairly scalable)

$$\text{e.g. } f(a, b, c) = \sum(0, 1, 3, 5, 6, 7)$$

Place numbers with same number of 1's in the same group.

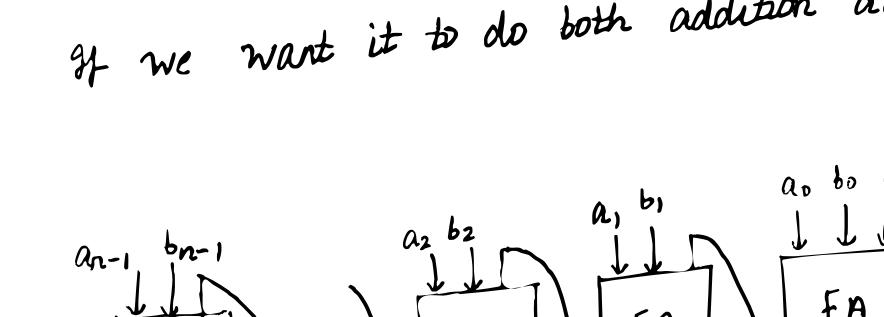
GD	0	000	(0, 1)	00 -	PI ₂
G ₁	1	001	(1, 3)	0 - 1	(1, 3, 5, 7) - - 1
G ₂	3	011	(1, 5)	- 0 1	(1, 5, 3, 7) - - 1
	5	101	(3, 7)	- 1 1	
	6	110	(5, 7)	1 - 1	
G ₃	7	111	(6, 7)	1 1 -	PI ₁

Pairing only possible between adjacent groups i.e.

(G₀, G₁), (G₁, G₂) & (G₂, G₃)

All unpaired groupings \rightarrow PI_s

$$\therefore f(a, b, c) = PI_1 + PI_2 + PI_3 \\ = c + \bar{a}\bar{b} + ab$$



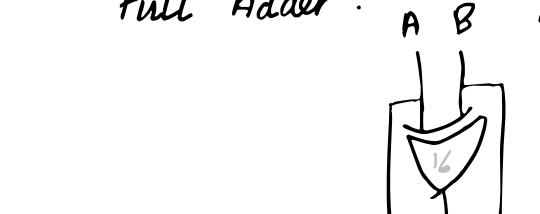
EPI (because of 0)
 remove these minterms

EPI because of 6

If you get SPI : Patrick's Method

or

Integer Linear Programming (ILP)



What we have done?

\rightarrow How to Represent

\rightarrow How to Minimize

\rightarrow How to check equivalence

Arithmetic functions :

- ADDITION

- SUBTRACTION

- MULTIPLICATION

- DIVISION

Addition:

(1-bit adder)

Now, what if we want to add

A $a_{n-1} a_{n-2} \dots a_0, a_0$

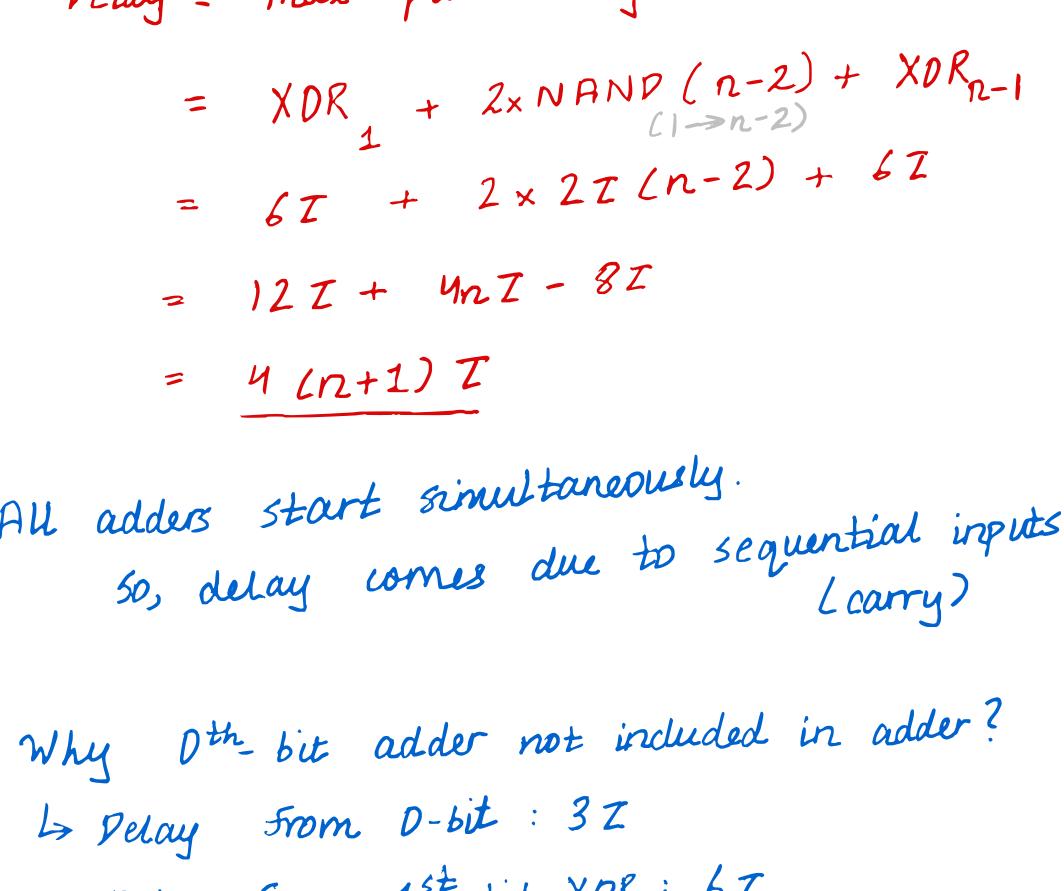
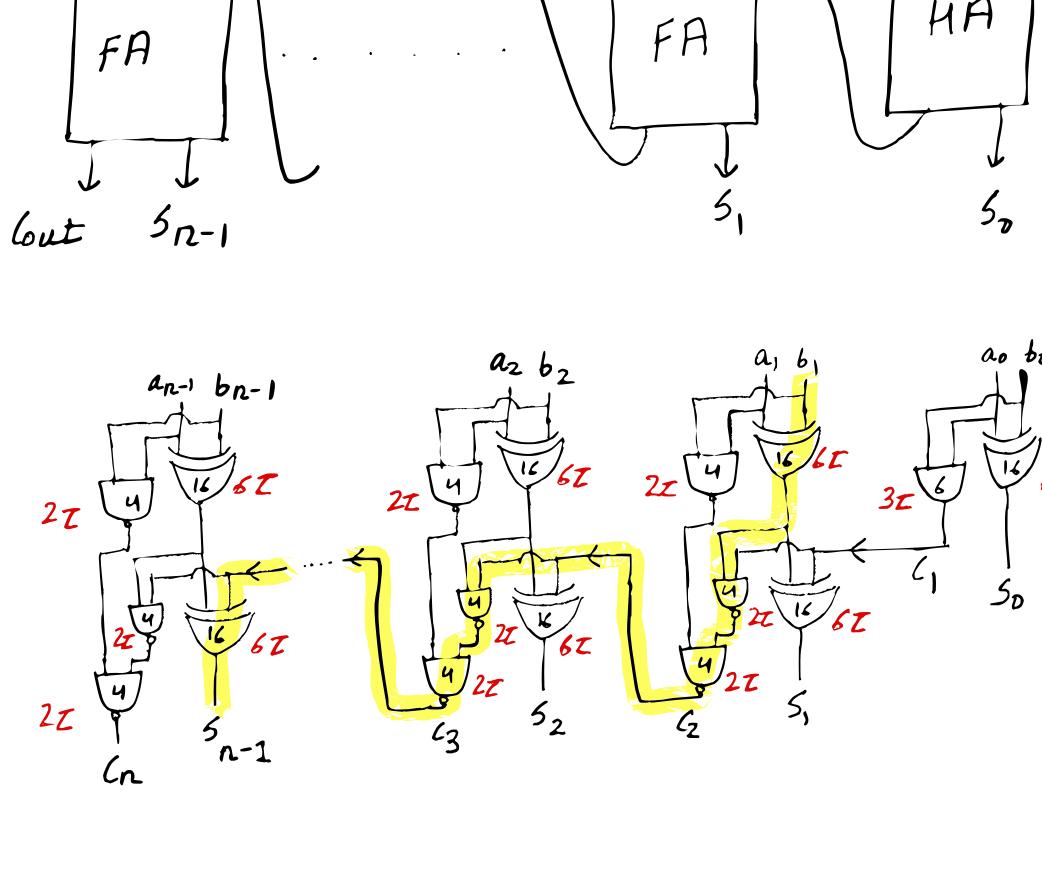
B $b_{n-1} b_{n-2} \dots b_1, b_0$

i.e. n-bit addition

If we want it to do both addition and subtraction,

ADDERS:

RIPPLE CARRY ADDER (RCA)



$$\text{total cost} = 22 + 44(n-1)$$

Delay = max. path length

$$\begin{aligned}
 &= XDR_1 + 2 \times \underset{(1 \rightarrow n-2)}{\text{NAND}}(n-2) + XDR_{n-1} \\
 &= 6T + 2 \times 2T(n-2) + 6T \\
 &= 12T + 4nT - 8T \\
 &= \underline{4(n+1)T}
 \end{aligned}$$

All adders start simultaneously.

So, delay comes due to sequential inputs.
(carry)

Why 0th-bit adder not included in adder?

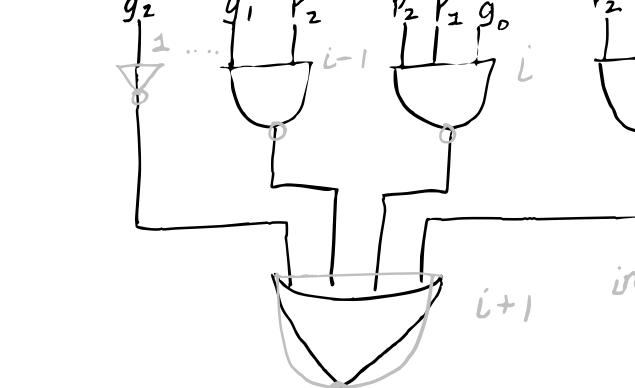
↳ Delay from 0-bit : 3T

Delay from 1st-bit XOR : 6T

We take max.

XOR :

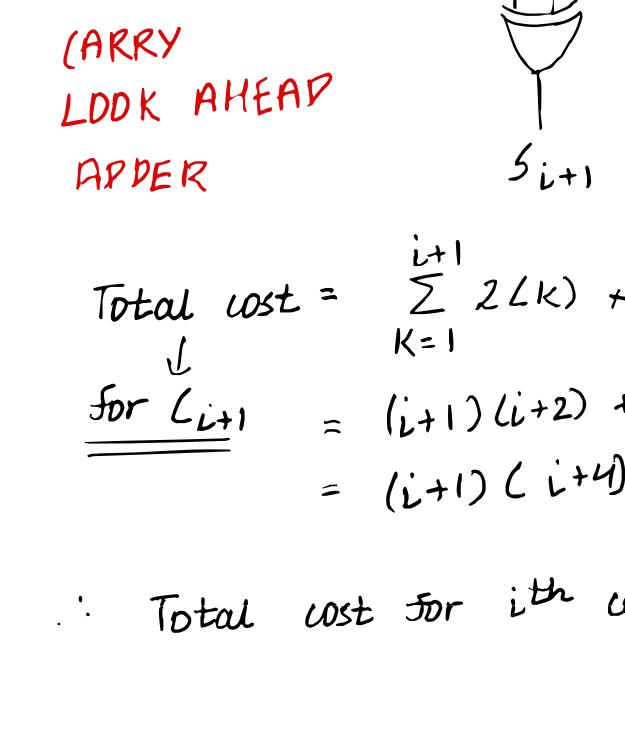
delay : 6T



Can we reduce delay?

Yes, why wait for cin to come when we can calculate it ourselves?

$$\begin{array}{r}
 \text{cin} \quad 0 \ 0 \ 0 \ 0 \ 0 \ 1 \ 1 \ 1 \\
 a_i \quad 0 \ 0 \ 1 \ 1 \ 0 \ 0 \ 1 \ 1 \\
 b_i \quad 0 \ 1 \ 0 \ 1 \ 0 \ 1 \ 0 \ 1 \\
 \hline
 l_0 \quad 0 \ 0 \ 0 \ 1 \ 0 \ 1 \ 1 \ 1
 \end{array}$$



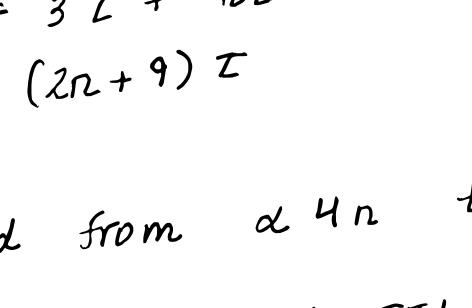
$$\therefore c_{i+1} = g_i + p_i c_i$$

$$\therefore c_1 = g_0 + c_0 p_0 \rightarrow (In case of adder \rightarrow l_0 = 0)$$

$$c_2 = g_1 + c_1 p_1$$

$$= g_1 + (g_0 + c_0 p_0) p_1$$

$$= g_1 + p_1 g_0 + p_1 p_0 c_0$$



(ARRY LOOK AHEAD ADDER)

$$s_{i+1} = l_{i+1} \oplus a_{i+1} \oplus b_{i+1}$$

$$\text{Total cost} = \sum_{k=1}^{i+1} 2L(k) + 2(i+1)$$

$$\text{for } l_{i+1} = (i+1)(i+2) + 2(i+1)$$

$$= (i+1)(i+4)$$

$$\therefore \text{Total cost for } i^{\text{th}} \text{ cell} = 2XDR + l_{i+1}$$

$$= 2 \times 16 + (i+1)(i+4)$$

$$= 32 + (i+1)(i+4)$$

$$g_i = a_i * b_i \rightarrow \text{cost} : 6$$

$$p_i = a_i + b_i \rightarrow \text{cost} : 6$$

$$n g_i \text{ and } n p_i \rightarrow 6n + 6n = \underline{12n}$$

$$\begin{aligned}
 \therefore \text{Delay} &= 3T + (i+1)T + (i+1)T + 6T \\
 &\downarrow \quad \text{AND} \quad \text{OR} \quad XDR \\
 \text{from } p_i & \\
 \text{For } i^{\text{th}} \text{ cell.} &
 \end{aligned}$$

But we only take max.

→ for (n-1)th cell

$$\therefore \text{Delay} = 3T + nT + nT + 6T$$

$$= (2n+9)T$$

Delay reduced from $\propto 4n$ to $\propto 2n$.

Earlier, TTL was used, in TTL, delay does not depend on no. of inputs. Thus, delay was fixed to 3T for above circuit → considered very fast.

But now, with CMOS, we lost that advantage.

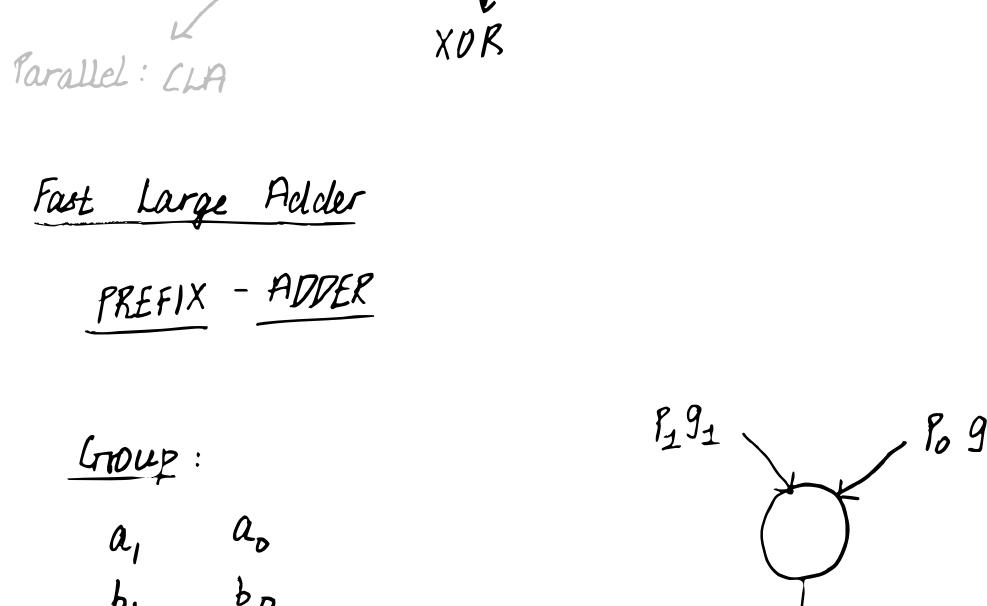
ADDER

- RLA \rightarrow slowest $\propto 4n$
- CLA \rightarrow $\propto 2n$
↑
(CMOS)

Fast for TTL/BJT

↓

Delay \propto # of levels



Fast Large Adder

PREFIX - ADDER

Group :

$$\begin{array}{cc} a_1 & a_0 \\ b_1 & b_0 \end{array} \quad \rightarrow g_0 = a_0 \cdot b_0$$

$$g_1 = a_1 \cdot b_1 \quad P_0 = a_0 \oplus b_0$$

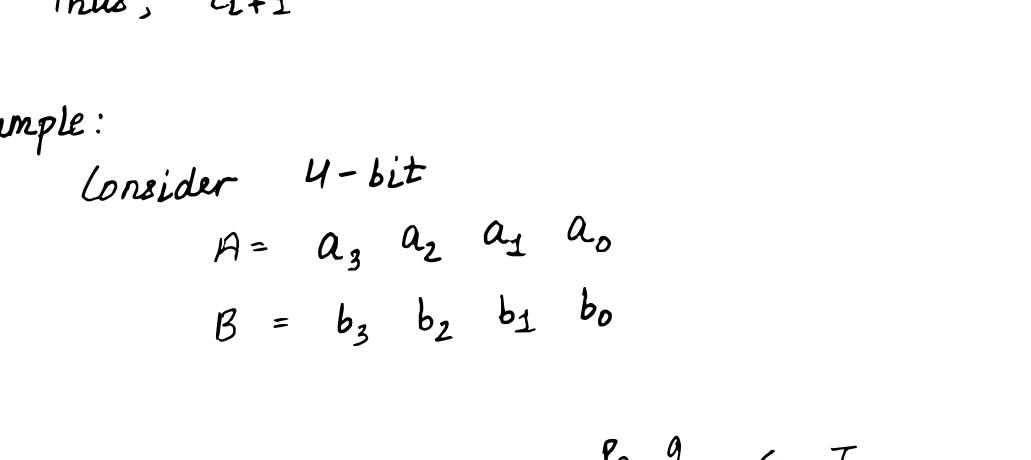
$$P_1 = a_1 \oplus b_1$$

$$P_1 g_1 \quad P_0 g_0$$

$$G[1:0] = g_1 + P_1 g_0$$

$$P[1:0] = P_1 \cdot P_0$$

Instead of making a group of all like in CLA,
make smaller groups (say, of two).



$$\therefore S_i = c_i \oplus a_i \oplus b_i$$

$$c_{i+1} = G[i:k] + P[i:k] \cdot c_k$$

We have c_0 ,

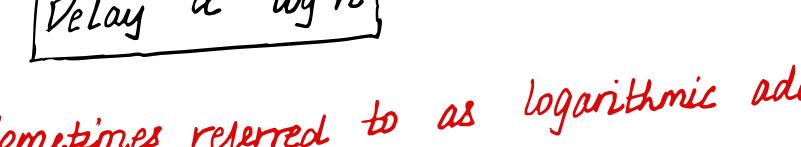
$$\text{Thus, } c_{i+1} = G[i:0] + P[i:0] c_0$$

example:

Consider 4-bit

$$A = a_3 \ a_2 \ a_1 \ a_0$$

$$B = b_3 \ b_2 \ b_1 \ b_0$$



$$\therefore \text{Delay} = \underbrace{T_1 + T_2 + T_3}_{\text{constant}} + \underbrace{\log n}_{\text{no. of levels (max.)}}$$

$$\therefore \boxed{\text{Delay} \propto \log n}$$

Sometimes referred to as logarithmic adder.

Other architectures:

→ BRENT-KUNG

1960

→ $2 \log n$ levels

Depth

Midsem Practice:

Distributivity:

$$a(b+c) = ab + ac$$

$$\star a + bc = (a+b) \cdot (a+c)$$

Thm:

absorption

$$a + \bar{a}b = (a+\bar{a})(a+b) = \underline{a+b}$$

$$a \cdot (\bar{a}+b) = a \cdot \bar{a} + a \cdot b = \underline{ab}$$

consensus

$$\begin{aligned}
 & ab + \bar{a}c + bc \\
 &= (a + \bar{a}c + bc)(b + \bar{a}c + bc) \\
 &= (a+c)(\bar{a}c + b) \\
 &= (a+c)(b+c)(\bar{a}+b) \\
 &=
 \end{aligned}$$

$$(ab + \bar{a}c + b) \subset ab + \bar{a}c + c$$

$$(b + \bar{a}c) \subset ab + c$$

$$(b + \bar{a}c)(ab + c) = ab + bc + \bar{a}c$$

$$\boxed{
 \begin{aligned}
 ab + a'c + b &\leftarrow ab + a'c + abc + a'b'c' \\
 &= ab + a'c
 \end{aligned}
 \text{bc}(a+a')
 }$$

consensus:

$$ab + a'c + bc = ab + a'c$$

$$(a+b)(a+c) / b+c = (a+b)(a'+c)$$

$$\text{cost: } \begin{cases} \text{no. of literals} + \text{no. of product terms} \\ 2 \times [\text{no. of literals} + \text{no. of product terms}] \end{cases}$$

$$AB + CD$$

$$[4 + 2] \times 2 = 6 \times 2 = 12$$

$$AB + AC + BC$$

$$[3 + 2] \times 2 = 5 \times 2 = 10 ?$$

$$AB + CD$$

$$[1 + 3] \times 2 = 4 \times 2 = 10$$

$$AB + AC + BC$$

$$[3 + 3] \times 2 = 12 ?$$

$$AB + AC + BC$$

$$[3 + 3] \times 2 = 12 ?$$

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$$[3 + 3] \times 2 = 12 ?$$
</div

EE224 midem

2]

AB	CD	DD	00	01	11	10
DD	1		1	1		1
DI	1	1				1
			1	1		
			1	1		1

$$\begin{aligned}
 f &= \bar{A} \bar{C} \bar{D} \\
 &+ \bar{A} B \bar{C} \\
 &+ \bar{A} \bar{B} C \\
 &+ \bar{A} C \bar{D} \\
 &+ A B D \\
 &+ A \bar{B} C \\
 &+ A \bar{B} \bar{D}
 \end{aligned}$$

3]

$$\begin{aligned}
 f(A, B, C) &= A'B' + A'C + BC + AB \\
 &= A'C + AB + BC + A'B' \\
 &\text{or} \\
 &A'B' + CB + A'C + AB
 \end{aligned}$$

A	B	C	00	01	11	10
0	1	1	1	1	1	1
1	1	1				

$$A'B', AB \rightarrow EP I$$

Q. 4]

n variables

$$a_1, a_2, a_3, \dots, a_n$$

$$0 \quad 0 \quad 0 \quad \dots \quad 0$$

$$0 \quad 0 \quad 0 \quad \dots \quad 1$$

$$\vdots \quad \vdots \quad \vdots \quad \ddots \quad \vdots$$

$$1 \quad 1 \quad 1 \quad \dots \quad 1$$

For each row of the table,

$$\text{define } m_i = \prod_j \hat{a}_j$$

where \hat{a}_j can be a_j or \bar{a}_j depending on the value 1 or 0 respectively.

$$\text{define } M_i = \sum_j m_j$$

In sum form,

$$f = \sum_k m_k$$

$$\bar{m}_i = 1's \text{ complement of } \hat{a}_j$$

$$\therefore \bar{m}_i = M_{2^n-1-i}$$

$$\text{If } f = \sum_{k \in S} m_k$$

$$\bar{f} = \left(\sum_{k \in S} \bar{m}_k \right)$$

$$\therefore \bar{f} = \prod_{k \in S} \bar{m}_k$$

$$= \prod_{k \in S} M_{2^n-1-i}$$

$$Y = \bar{B}C + BD$$

$$F = \bar{Y} A$$

$$F = (\bar{B}C + BD) A$$

$$= (B + \bar{C})(\bar{B} + \bar{D})(A)$$

$$= (AB + A\bar{C})(\bar{B} + \bar{D})$$

$$= ABD + A\bar{B}\bar{C} + A\bar{C}\bar{D}$$

$$= A(B\bar{D} + \bar{B}\bar{C} + \bar{C}\bar{D})$$

By consensus theorem,

$$F = A(B\bar{D} + \bar{B}\bar{C})$$

$$\text{NDT} \rightarrow A=1, B=0$$

$$\text{Input } C \rightarrow f = \bar{z}$$

$$\text{AND} \rightarrow ABCD$$

$$A(CBD) \rightarrow A(\bar{B}\bar{C} + \bar{B}\bar{D})$$

$$A(\bar{B}\bar{C} + \bar{B}\bar{D}) \rightarrow A(\bar{B}\bar{C} + \bar{B}\bar{D})$$

$$A(\bar{B}\bar{C} + BD + CD)$$

$$Y = \bar{A}\bar{B} = AB$$

$$A + \bar{A}B = A + B$$

$$A(\bar{A} + B) = AB$$

$$\text{XOR}(w, x, y, z) = w \oplus x \oplus y \oplus z$$

w	x	y	z	XOR
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

$$\text{XOR}(w, x, y, z) = w \oplus x \oplus y \oplus z$$

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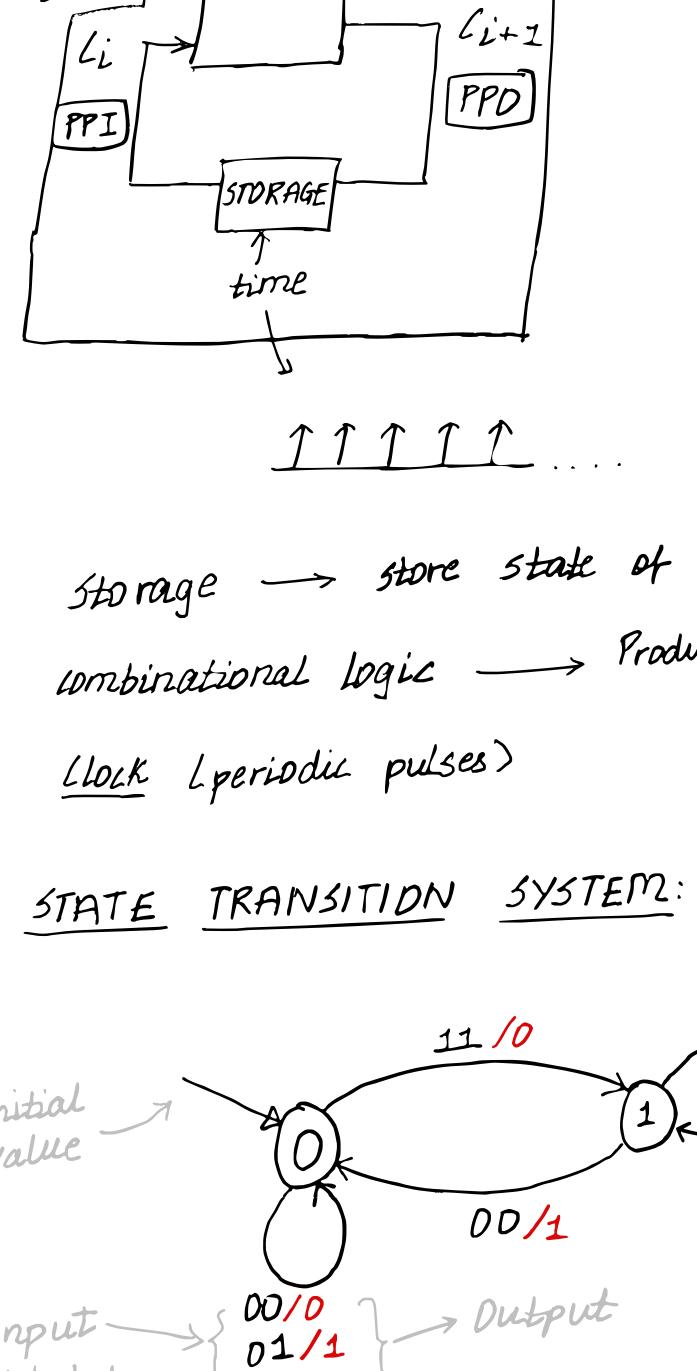
$$\text{XOR}(w, x, y, z) = w \oplus x \oplus y \oplus z$$

$$\text{XOR}(w, x, y, z) = w \oplus x \oplus y \oplus z$$

$$\text{XOR}(w, x, y, z) = w \oplus x \oplus y \oplus z$$

$$\text{XOR}(w, x, y, z) = w \oplus x$$

SERIAL ADDER

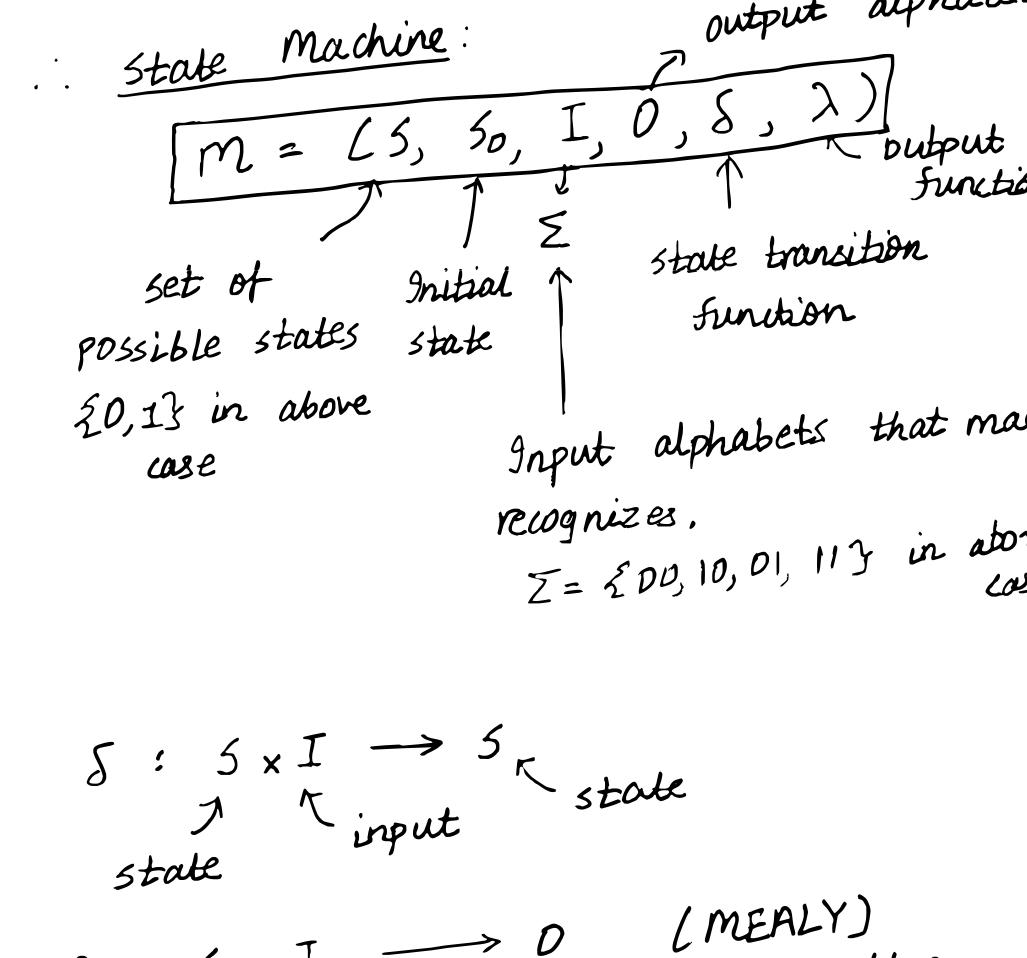


Storage → store state of the system

combinational logic → produce PO & PPD

Clock (periodic pulses)

STATE TRANSITION SYSTEM:



STATE TRANSITION DIAGRAM / GRAPH (STG)

PS	NS			
	00	01	10	11
0	0	0	0	1
1	0	1	1	1

PS	Output (Sum)			
	00	01	10	11
0	0	1	1	0
1	1	0	0	1

∴ $\delta : S \times I \rightarrow S$ state

state input

$\lambda : S \times I \rightarrow O$ (MEALY) machine

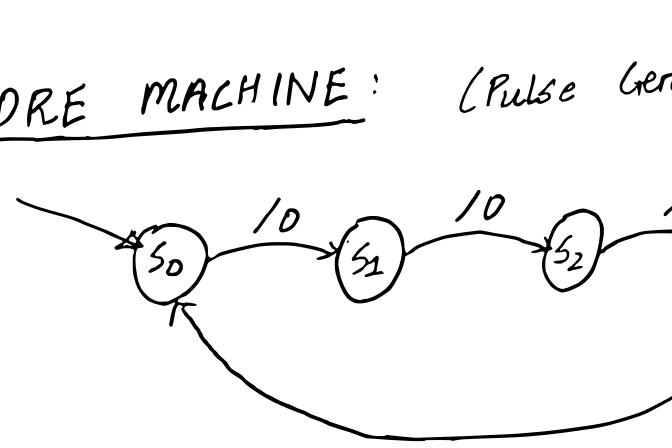
state input

$S \rightarrow O$ (MOORE) machine

state output

does not depend on input.

MEALY MACHINE: (Serial adder)



VHDL process:

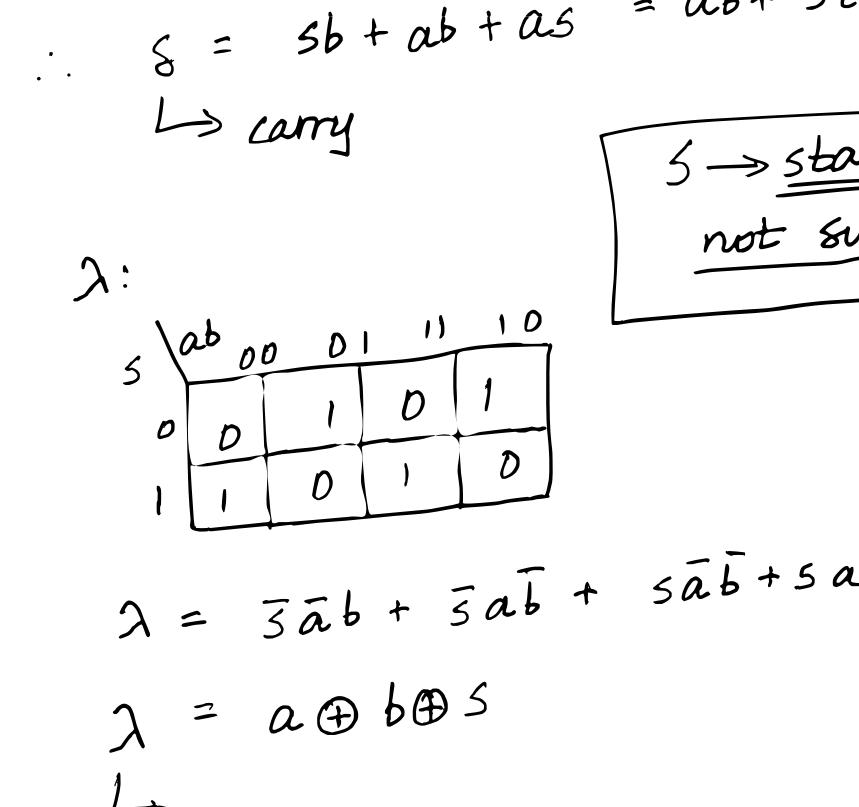
if (CLK = 1) then } partially specified behaviour
 $q \leftarrow d$ } behaviour

Here's where VHDL, Verilog or any other HDLs get ambiguous.

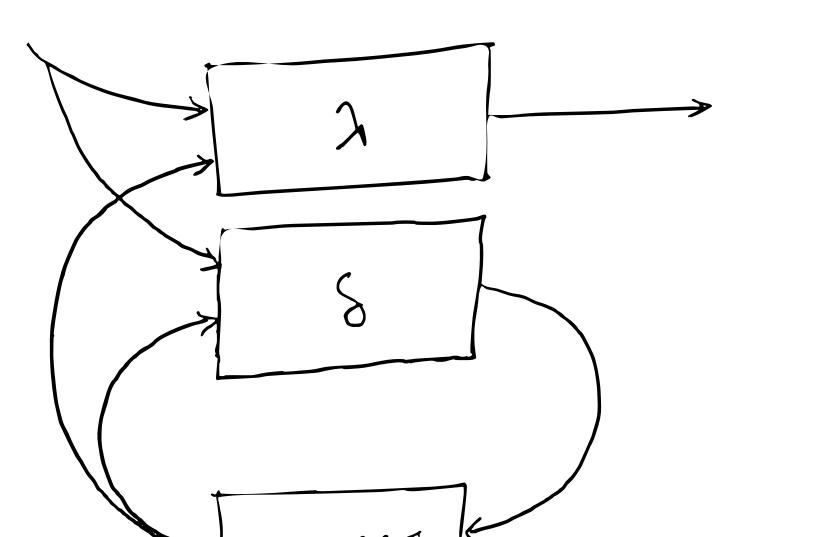
In this case, synthesizer will synthesize to default value; in most cases, default value retains previous value.

combinational logic behaviour needs to be fully specified.

MOORE MACHINE: (Pulse Generator)



Counter: (mod 4 counter)



$S = \{S_0, S_1, S_2, S_3\}$

$\delta, (\lambda \rightarrow (z_1, z_2))$

$\lambda = 3\bar{a}\bar{b} + \bar{a}\bar{b} + \bar{a}\bar{b} + \bar{a}\bar{b}$

$\lambda = a \oplus b \oplus s$

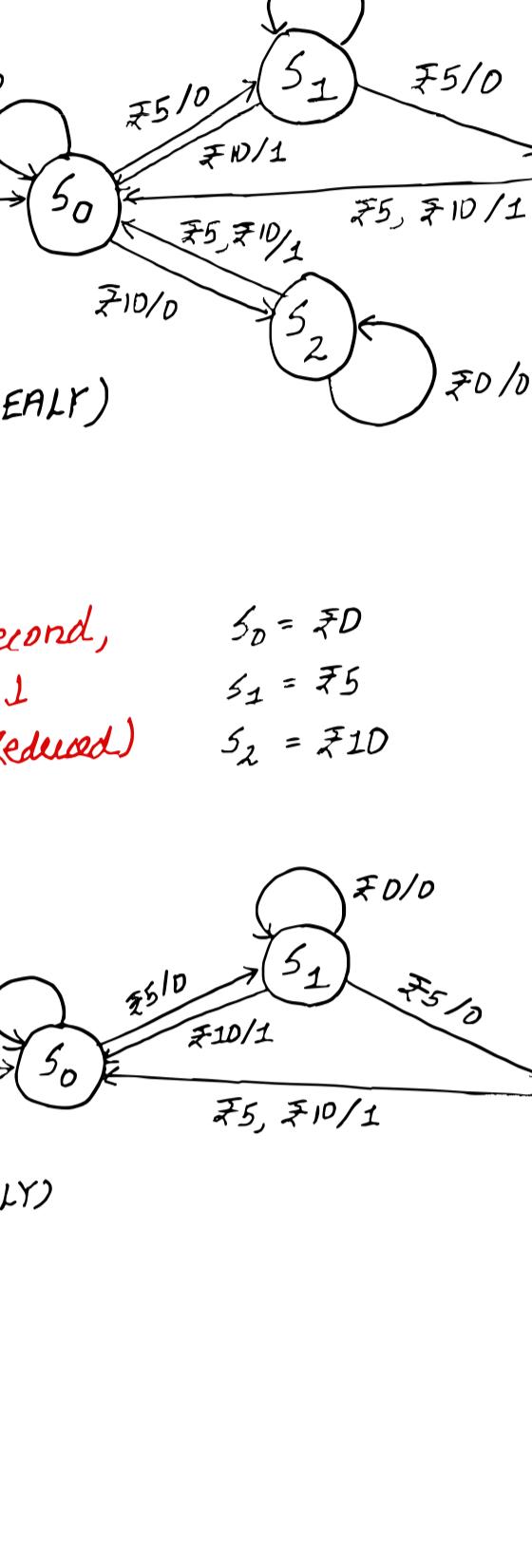
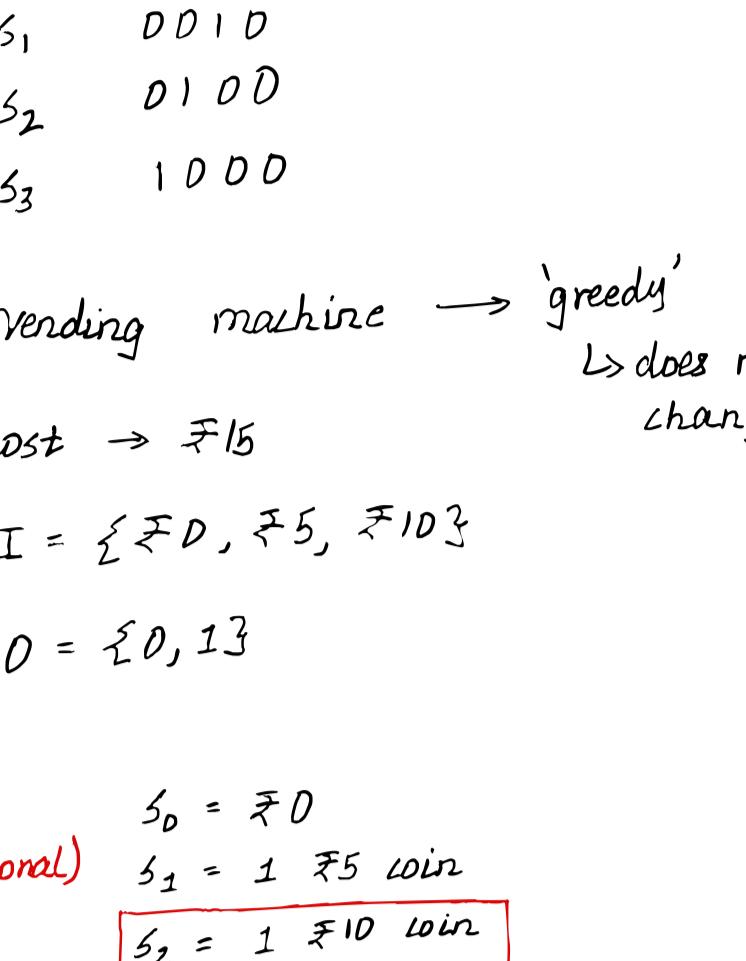
$\lambda = \bar{a} \oplus \bar{b} \oplus s$

$$M = (S, S_0, I, D, \delta, \lambda)$$

$\delta : S \times I \rightarrow S$
STATE TRANSITION FUNCTION

$\lambda : S \times I \rightarrow O$ (MEALY)
 $S \rightarrow O$ (MOORE)

STATE TRANSITION GRAPH



e.g. one-hot encoding

↳ 'n' states → n bits

$$S_0 \quad 0001$$

$$S_1 \quad 0010$$

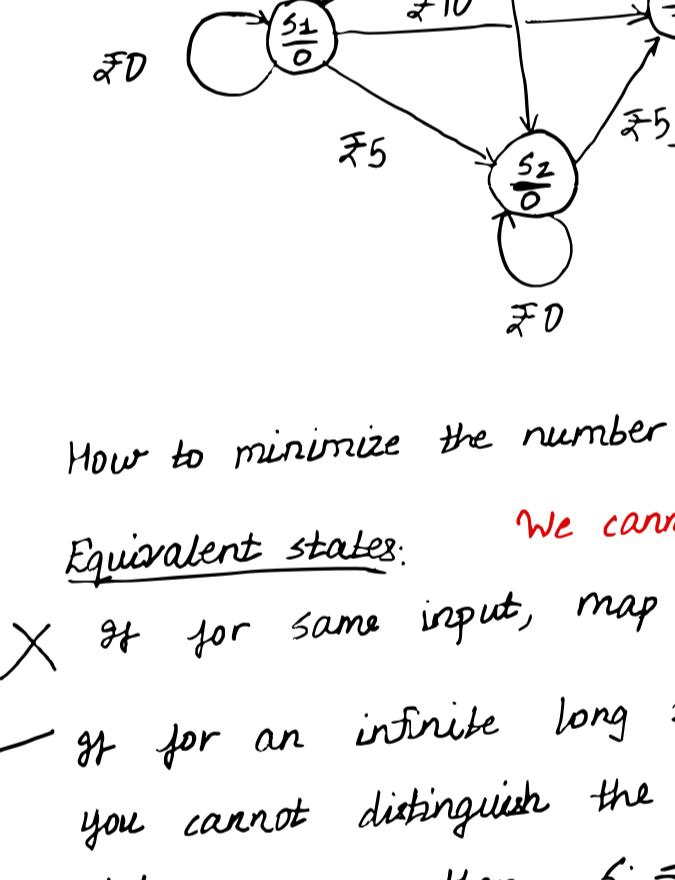
$$S_2 \quad 0100$$

$$S_3 \quad 1000$$

e.g. vending machine → 'greedy'
↳ does not have change
cost → ₹15

$$I = \{\text{₹}0, \text{₹}5, \text{₹}10\}$$

$$O = \{0, 1\}$$



Second, ↓ (Reduced)

$$S_0 = \text{₹}0$$

$$S_1 = \text{₹}5$$

$$S_2 = \text{₹}10$$

$$S_3 = \text{₹}15$$

$$S_4 = 1 \text{ ₹}5, 1 \text{ ₹}10 \text{ coin}$$

$$S_5 = 2 \text{ ₹}5 \text{ coins}$$

$$S_6 = 2 \text{ ₹}5, 1 \text{ ₹}10 \text{ coins}$$

$$S_7 = 1 \text{ ₹}10, 1 \text{ ₹}5 \text{ coins}$$

$$S_8 = 1 \text{ ₹}10, 2 \text{ ₹}5 \text{ coins}$$

$$S_9 = 2 \text{ ₹}10 \text{ coins}$$

$$S_{10} = 2 \text{ ₹}10, 1 \text{ ₹}5 \text{ coin}$$

$$S_{11} = 2 \text{ ₹}10, 2 \text{ ₹}5 \text{ coins}$$

$$S_{12} = 3 \text{ ₹}5 \text{ coins}$$

$$S_{13} = 3 \text{ ₹}5, 1 \text{ ₹}10 \text{ coin}$$

$$S_{14} = 3 \text{ ₹}5, 2 \text{ ₹}5 \text{ coins}$$

$$S_{15} = 4 \text{ ₹}5 \text{ coins}$$

$$S_{16} = 4 \text{ ₹}5, 1 \text{ ₹}10 \text{ coin}$$

$$S_{17} = 4 \text{ ₹}5, 2 \text{ ₹}5 \text{ coins}$$

$$S_{18} = 5 \text{ ₹}5 \text{ coins}$$

$$S_{19} = 5 \text{ ₹}5, 1 \text{ ₹}10 \text{ coin}$$

$$S_{20} = 5 \text{ ₹}5, 2 \text{ ₹}5 \text{ coins}$$

$$S_{21} = 6 \text{ ₹}5 \text{ coins}$$

$$S_{22} = 6 \text{ ₹}5, 1 \text{ ₹}10 \text{ coin}$$

$$S_{23} = 6 \text{ ₹}5, 2 \text{ ₹}5 \text{ coins}$$

$$S_{24} = 7 \text{ ₹}5 \text{ coins}$$

$$S_{25} = 7 \text{ ₹}5, 1 \text{ ₹}10 \text{ coin}$$

$$S_{26} = 7 \text{ ₹}5, 2 \text{ ₹}5 \text{ coins}$$

$$S_{27} = 8 \text{ ₹}5 \text{ coins}$$

$$S_{28} = 8 \text{ ₹}5, 1 \text{ ₹}10 \text{ coin}$$

$$S_{29} = 8 \text{ ₹}5, 2 \text{ ₹}5 \text{ coins}$$

$$S_{30} = 9 \text{ ₹}5 \text{ coins}$$

$$S_{31} = 9 \text{ ₹}5, 1 \text{ ₹}10 \text{ coin}$$

$$S_{32} = 9 \text{ ₹}5, 2 \text{ ₹}5 \text{ coins}$$

$$S_{33} = 10 \text{ ₹}5 \text{ coins}$$

$$S_{34} = 10 \text{ ₹}5, 1 \text{ ₹}10 \text{ coin}$$

$$S_{35} = 10 \text{ ₹}5, 2 \text{ ₹}5 \text{ coins}$$

$$S_{36} = 11 \text{ ₹}5 \text{ coins}$$

$$S_{37} = 11 \text{ ₹}5, 1 \text{ ₹}10 \text{ coin}$$

$$S_{38} = 11 \text{ ₹}5, 2 \text{ ₹}5 \text{ coins}$$

$$S_{39} = 12 \text{ ₹}5 \text{ coins}$$

$$S_{40} = 12 \text{ ₹}5, 1 \text{ ₹}10 \text{ coin}$$

$$S_{41} = 12 \text{ ₹}5, 2 \text{ ₹}5 \text{ coins}$$

$$S_{42} = 13 \text{ ₹}5 \text{ coins}$$

$$S_{43} = 13 \text{ ₹}5, 1 \text{ ₹}10 \text{ coin}$$

$$S_{44} = 13 \text{ ₹}5, 2 \text{ ₹}5 \text{ coins}$$

$$S_{45} = 14 \text{ ₹}5 \text{ coins}$$

$$S_{46} = 14 \text{ ₹}5, 1 \text{ ₹}10 \text{ coin}$$

$$S_{47} = 14 \text{ ₹}5, 2 \text{ ₹}5 \text{ coins}$$

$$S_{48} = 15 \text{ ₹}5 \text{ coins}$$

$$S_{49} = 15 \text{ ₹}5, 1 \text{ ₹}10 \text{ coin}$$

$$S_{50} = 15 \text{ ₹}5, 2 \text{ ₹}5 \text{ coins}$$

$$S_{51} = 16 \text{ ₹}5 \text{ coins}$$

$$S_{52} = 16 \text{ ₹}5, 1 \text{ ₹}10 \text{ coin}$$

$$S_{53} = 16 \text{ ₹}5, 2 \text{ ₹}5 \text{ coins}$$

$$S_{54} = 17 \text{ ₹}5 \text{ coins}$$

$$S_{55} = 17 \text{ ₹}5, 1 \text{ ₹}10 \text{ coin}$$

$$S_{56} = 17 \text{ ₹}5, 2 \text{ ₹}5 \text{ coins}$$

$$S_{57} = 18 \text{ ₹}5 \text{ coins}$$

$$S_{58} = 18 \text{ ₹}5, 1 \text{ ₹}10 \text{ coin}$$

$$S_{59} = 18 \text{ ₹}5, 2 \text{ ₹}5 \text{ coins}$$

$$S_{60} = 19 \text{ ₹}5 \text{ coins}$$

$$S_{61} = 19 \text{ ₹}5, 1 \text{ ₹}10 \text{ coin}$$

$$S_{62} = 19 \text{ ₹}5, 2 \text{ ₹}5 \text{ coins}$$

$$S_{63} = 20 \text{ ₹}5 \text{ coins}$$

$$S_{64} = 20 \text{ ₹}5, 1 \text{ ₹}10 \text{ coin}$$

$$S_{65} = 20 \text{ ₹}5, 2 \text{ ₹}5 \text{ coins}$$

$$S_{66} = 21 \text{ ₹}5 \text{ coins}$$

$$S_{67} = 21 \text{ ₹}5, 1 \text{ ₹}10 \text{ coin}$$

$$S_{68} = 21 \text{ ₹}5, 2 \text{ ₹}5 \text{ coins}$$

$$S_{69} = 22 \text{ ₹}5 \text{ coins}$$

$$S_{70} = 22 \text{ ₹}5, 1 \text{ ₹}10 \text{ coin}$$

$$S_{71} = 22 \text{ ₹}5, 2 \text{ ₹}5 \text{ coins}$$

$$S_{72} = 23 \text{ ₹}5 \text{ coins}$$

$$S_{73} = 23 \text{ ₹}5, 1 \text{ ₹}10 \text{ coin}$$

$$S_{74} = 23 \text{ ₹}5, 2 \text{ ₹}5 \text{ coins}$$

$$S_{75} = 24 \text{ ₹}5 \text{ coins}$$

$$S_{76} = 24 \text{ ₹}5, 1 \text{ ₹}10 \text{ coin}$$

$$S_{77} = 24 \text{ ₹}5, 2 \text{ ₹}5 \text{ coins}$$

$$S_{78} = 25 \text{ ₹}5 \text{ coins}$$

$$S_{79} = 25 \text{ ₹}5, 1 \text{ ₹}10 \text{ coin}$$

$$S_{80} = 25 \text{ ₹}5, 2 \text{ ₹}5 \text{ coins}$$

$$S_{81} = 26 \text{ ₹}5 \text{ coins}$$

$$S_{82} = 26 \text{ ₹}5, 1 \text{ ₹}10 \text{ coin}$$

$$S_{83} = 26 \text{ ₹}5, 2 \text{ ₹}5 \text{ coins}$$

$$S_{84} = 27 \text{ ₹}5 \text{ coins}$$

$$S_{85} = 27 \text{ ₹}5, 1 \text{ ₹}10 \text{ coin}$$

$$S_{86} = 27 \text{ ₹}5, 2 \text{ ₹}5 \text{ coins}$$

$$S_{87} = 28 \text{ ₹}5 \text{ coins}$$

$$S_{88} = 28 \text{ ₹}5, 1 \text{ ₹}10 \text{ coin}$$

$$S_{89} = 28 \text{ ₹}5, 2 \text{ ₹}5 \text{ coins}$$

$$S_{90} = 29 \text{ ₹}5 \text{ coins}$$

$$S_{91} = 29 \text{ ₹}5, 1 \text{ ₹}10 \text{ coin}$$

$$S_{92} = 29 \text{ ₹}5, 2 \text{ ₹}5 \text{ coins}$$

$$S_{93} = 30 \text{ ₹}5 \text{ coins}$$

$$S_{94} = 30 \text{ ₹}5, 1 \text{ ₹}10 \text{ coin}$$

$$S_{95} = 30 \text{ ₹}5, 2 \text{ ₹}5 \text{ coins}$$

$$S_{96} = 31 \text{ ₹}5 \text{ coins}$$

$$S_{97} = 31 \text{ ₹}5, 1 \text{ ₹}10 \text{ coin}$$

$$S_{98} = 31 \text{ ₹}5, 2 \text{ ₹}5 \text{ coins}$$

<math

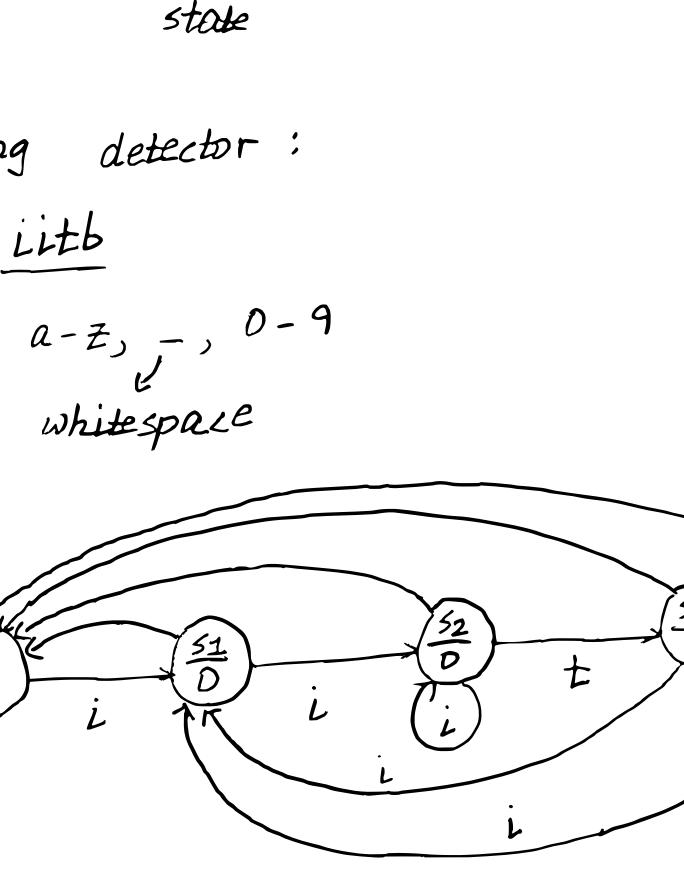
$$M = (S, S_0, I, D, \delta, \lambda)$$

$$\delta : S \times I \rightarrow S$$

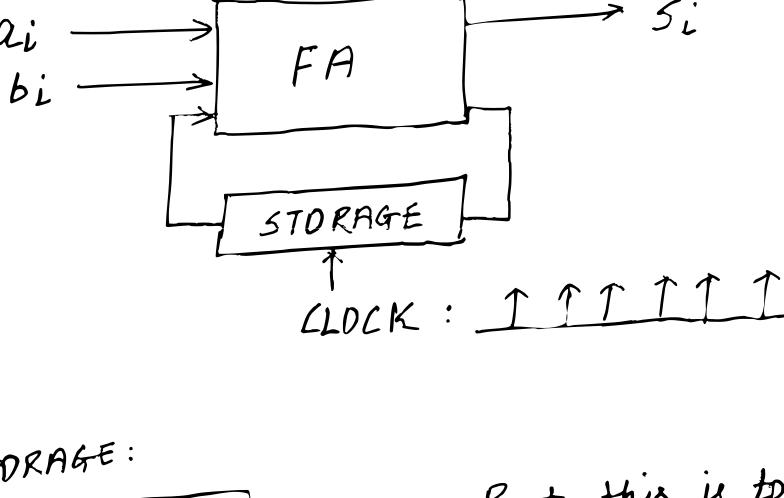
$$\lambda : S \times I \rightarrow O \quad (\text{Mealy})$$

$$S \rightarrow O \quad (\text{Moore})$$

Always, no. of states : Mealy < Moore



Counter:



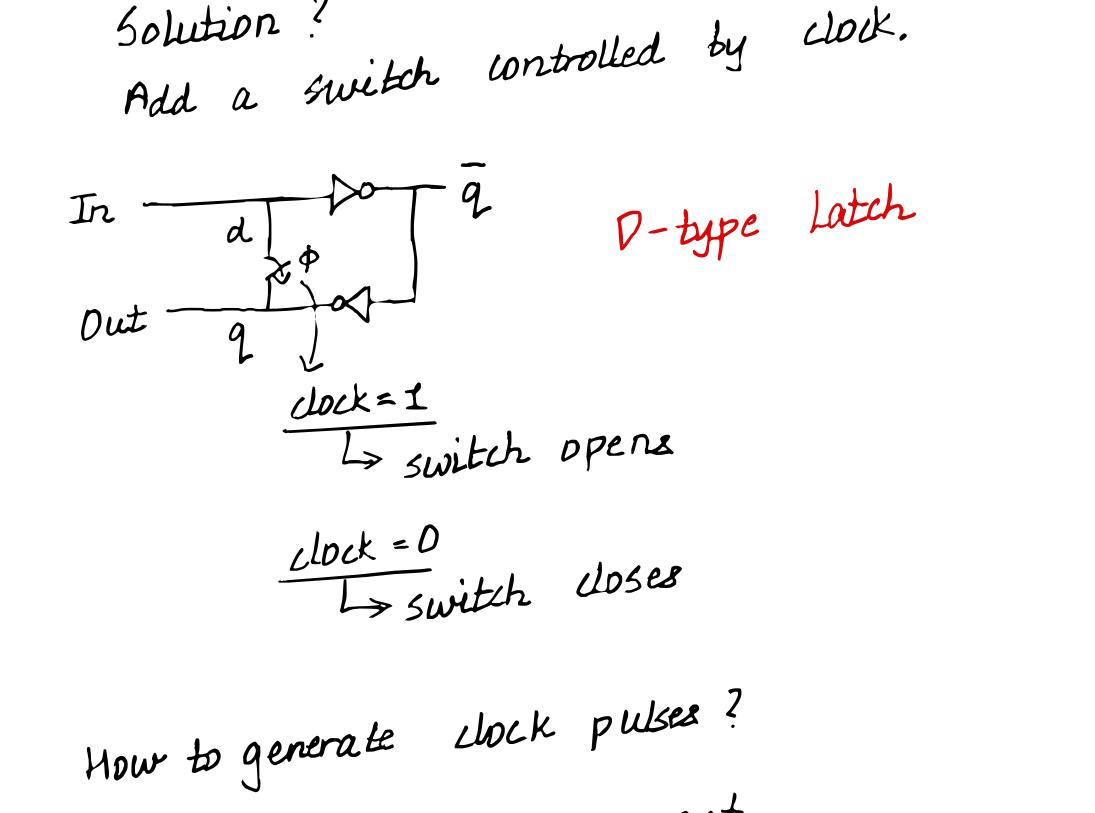
$\log_2 4 = 2$ bits required to store the state

String detector:

litsb

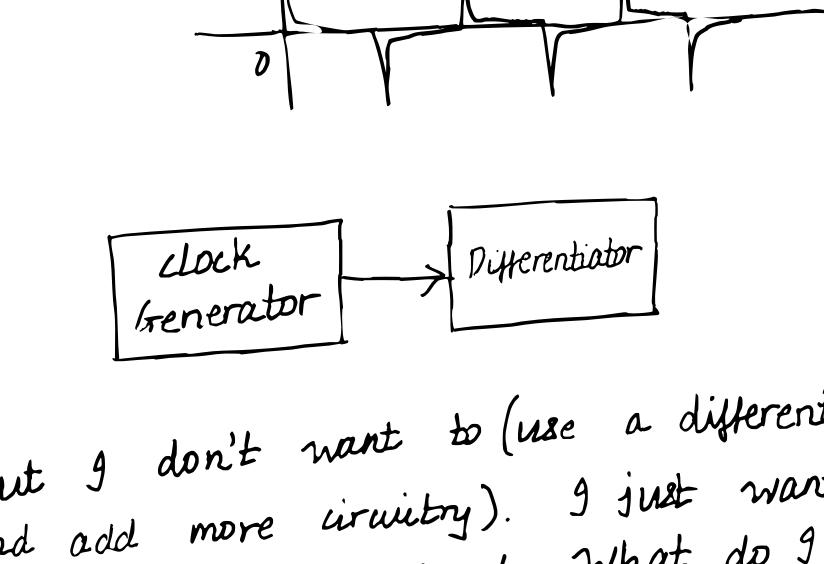
$$I = a-z, -, 0-9$$

whitespace

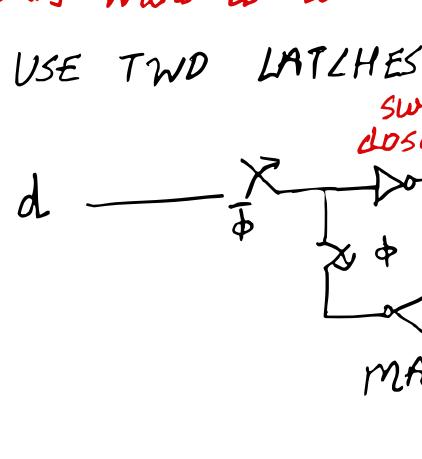


String matching \rightarrow compilers
using FSM or finite automata

ceil ($\log_2 5$) = 3 bits to store states
(3 storage elements)

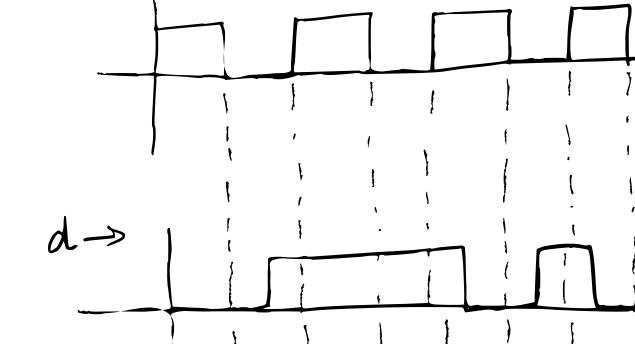


But when input changes, it becomes unstable:



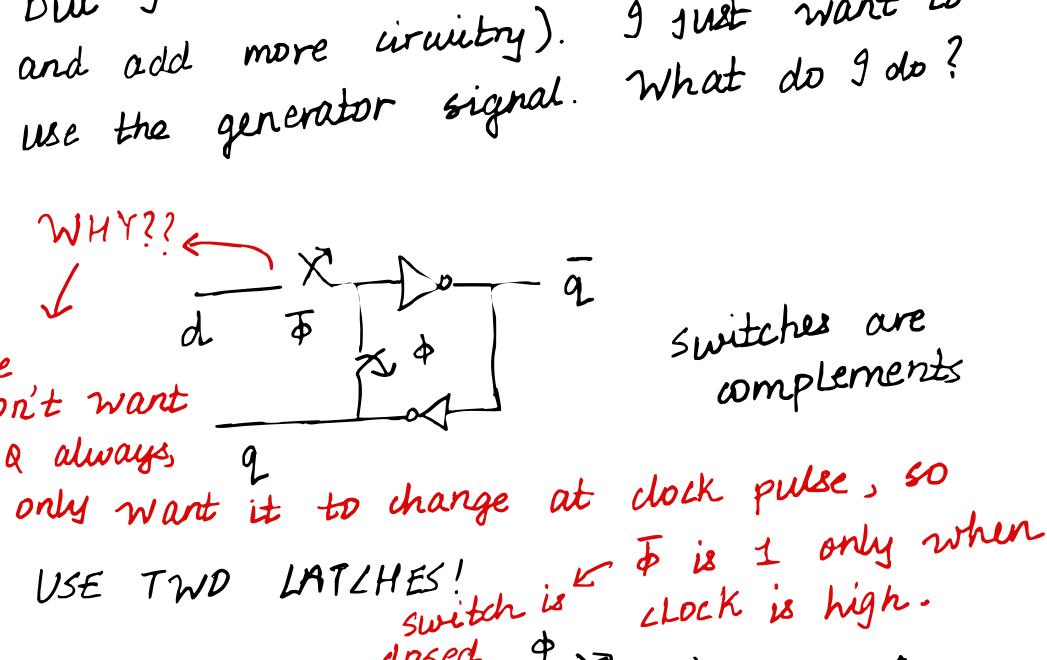
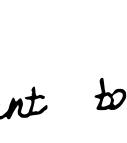
ONE OF THE CHEAPEST STORAGE ELEMENTS

Solution?
Add a switch controlled by clock.

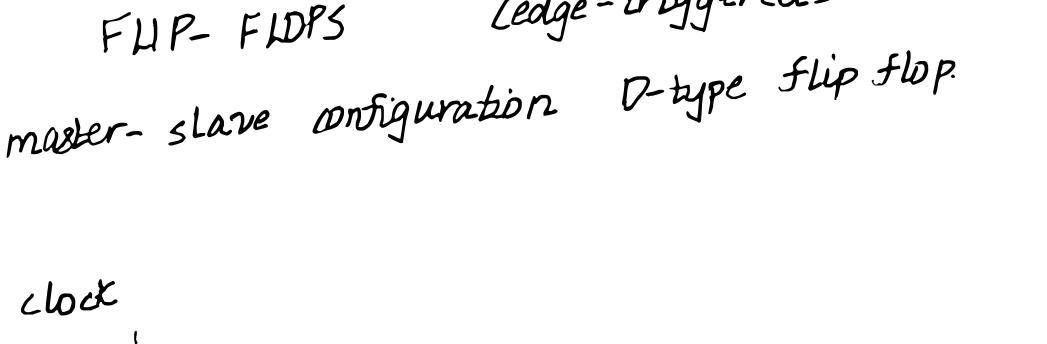


FLIP-FLOPS (edge-triggered)
master-slave configuration D-type flip flop.

NEGATIVE EDGE-TRIGGERED?



NEGATIVE EDGE-TRIGGERED?



NEGATIVE EDGE-TRIGGERED?

