IITB_CPU DESIGN DOCUMENTATION

EE224 Course Project

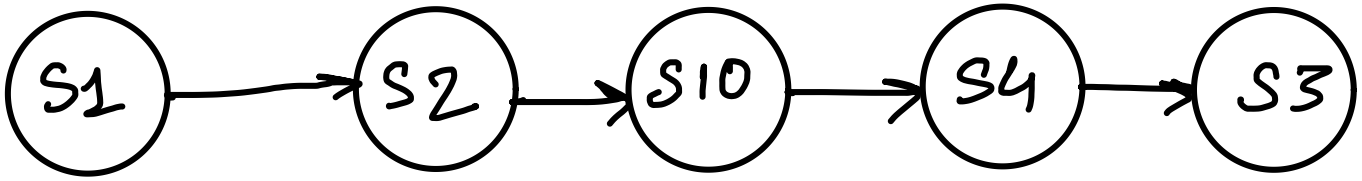
Team ID: 29

Members:

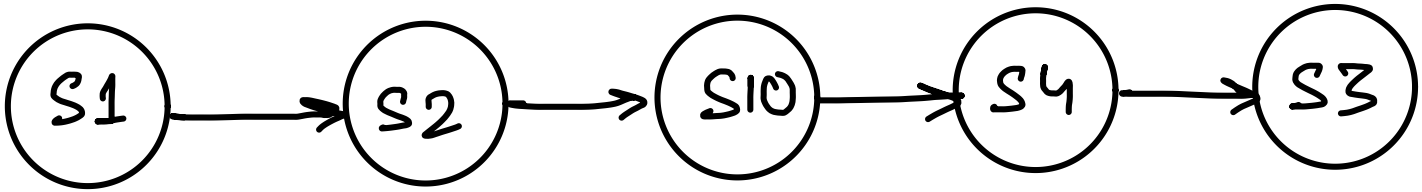
- 22B1238 - Saumya Dharmesh Shah
- 22B1235 – Himanshi Shende
- 22B0651 – Yug Pashupatinath Agarwal
- 22B3979 – Prerna Khobragade

FSM

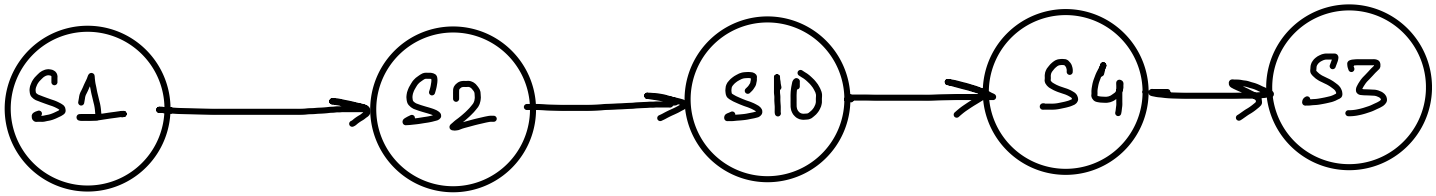
ADD:



SUB:



MUL:



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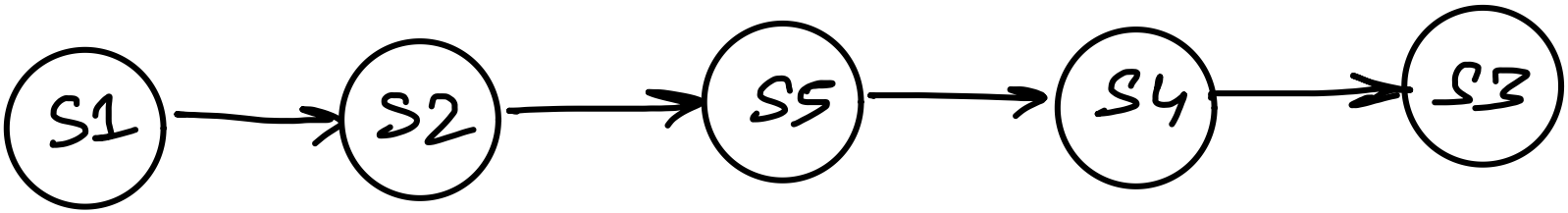
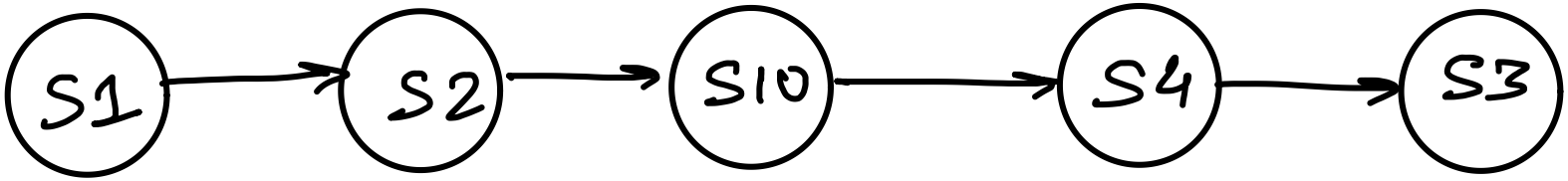
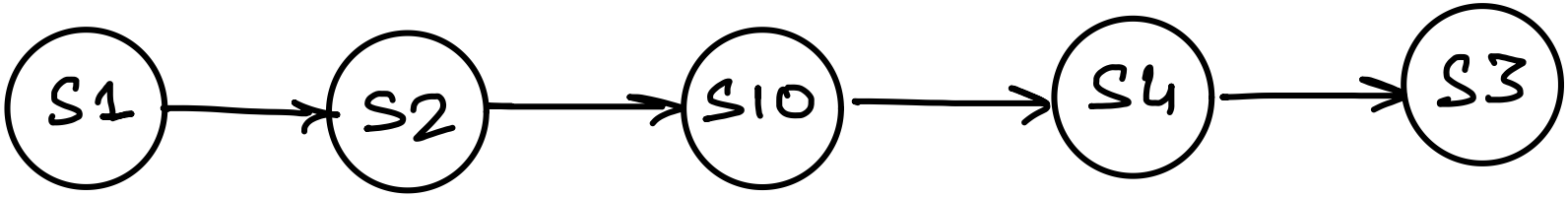


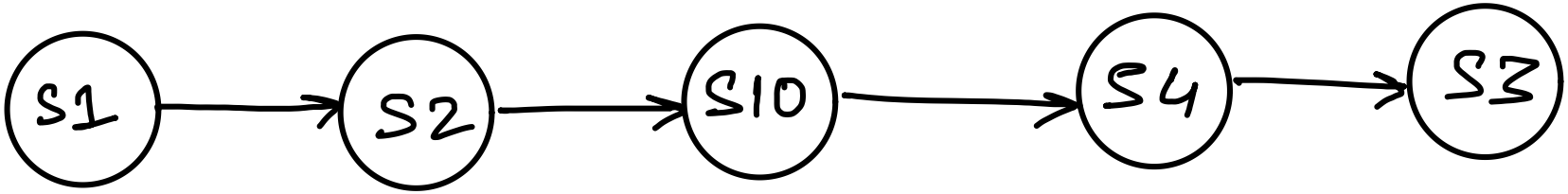
AND:



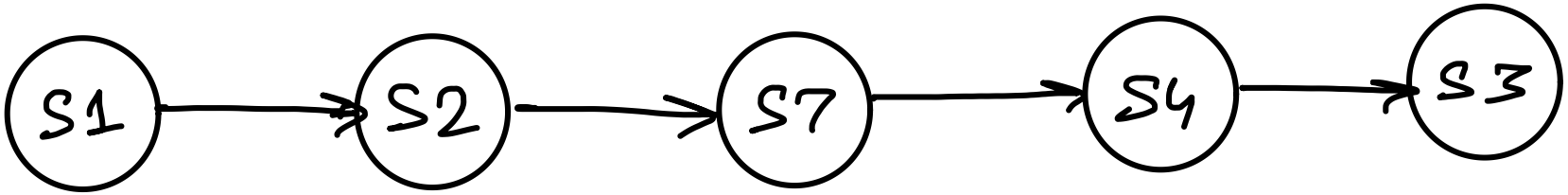
ORA:



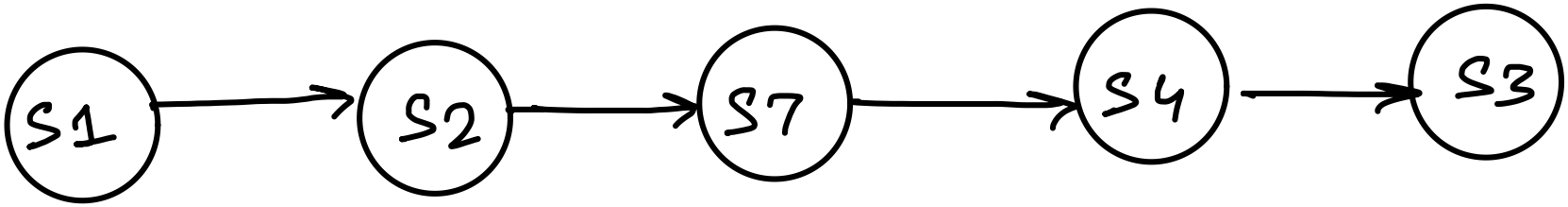
IMP:



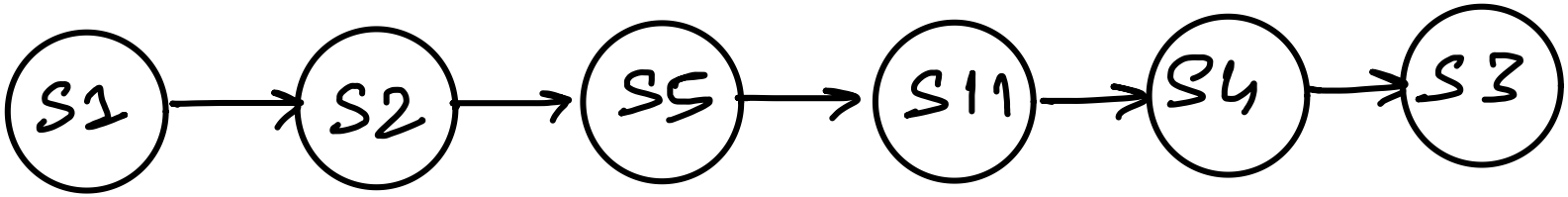
LHI:



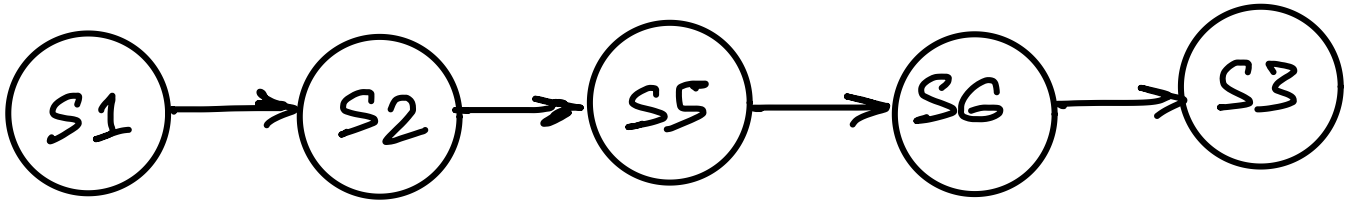
LLI:



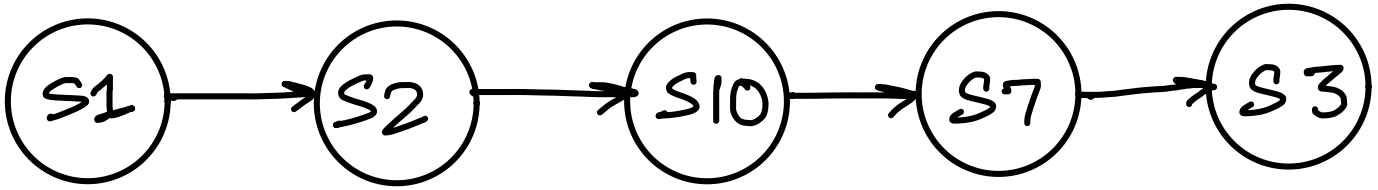
LW:



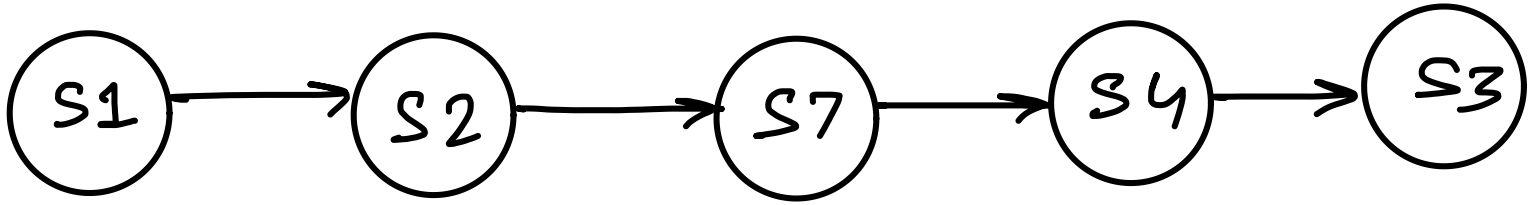
SW:



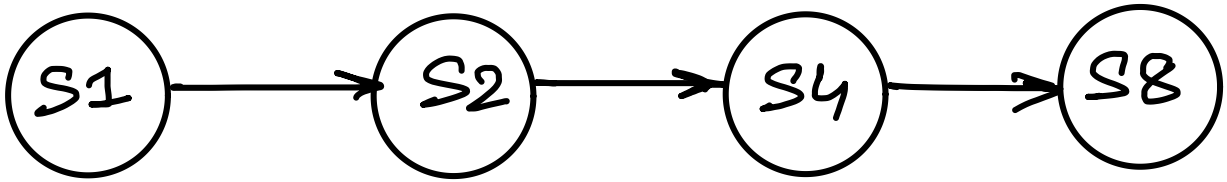
BEQ:



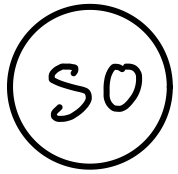
JAL:



JLR:



FLOWCHARTS AND CONTROLS



IP → Mem A1

Mem D1 → IR

	S0
MEM_R	0
MEM_W	0
IR_W	0
IP_W	0
RF_W	0
T1_W	0
T2_W	0
T3_W	0
sel_ALU(2)	0
sel_ALU(1)	0
sel_ALU(0)	0
sel_shift(1)	0
sel_shift(0)	0
S_IP	0
S_MA1	0
S_RA3(1)	0
S_RA3(0)	0
S1_RD3	0
S_AA	"00"
S_AB(2)	0
S_AB(1)	0
S_AB(0)	0
S_T3(1)	0
S_T3(0)	0
S_S1	0

S1

$IR_{9-11} \rightarrow RF\_A1$

$IR_{6-8} \rightarrow RF\_A2$

$RF\_D1 \rightarrow T1$

$RF\_D2 \rightarrow T2$

	S1
MEM_R	1
MEM_W	0
IR_W	1
IP_W	0
RF_W	0
T1_W	0
T2_W	0
T3_W	0
sel_ALU(2)	0
sel_ALU(1)	0
sel_ALU(0)	0
sel_shift(1)	0
sel_shift(0)	0
S_IP	0
S_MA1	0
S_RA3(1)	0
S_RA3(0)	0
S1_RD3	0
S_AA	"00"
S_AB(2)	0
S_AB(1)	0
S_AB(0)	0
S_T3(1)	0
S_T3(0)	0
S_S1	0

S2

al_A → ALU_A

al_B → ALU_B

ALU_C → al_C

ALU_Z → Z

ALU_ca → C

	S2
MEM_R	0
MEM_W	0
IR_W	0
IP_W	0
RF_W	0
T1_W	1
T2_W	1
T3_W	0
sel_ALU(2)	0
sel_ALU(1)	0
sel_ALU(0)	0
sel_shift(1)	0
sel_shift(0)	0
S_IP	0
S_MA1	0
S_RA3(1)	0
S_RA3(0)	0
S1_RD3	0
S_AA	"00"
S_AB(2)	0
S_AB(1)	0
S_AB(0)	0
S_T3(1)	0
S_T3(0)	0
S_S1	0

S3

X → RF_A3

Y → RF_D3

	S3
MEM_R	0
MEM_W	0
IR_W	0
IP_W	1
RF_W	0
T1_W	0
T2_W	0
T3_W	0
sel_ALU(2)	0
sel_ALU(1)	0
sel_ALU(0)	0
sel_shift(1)	0
sel_shift(0)	0
S_IP	0
S_MA1	0
S_RA3(1)	0
S_RA3(0)	0
S1_RD3	0
S_AA	"00"
S_AB(2)	(X3)(X2)(not X1)(not X0)(Z)
S_AB(1)	(X3)(X2)(not X1)(X0)
S_AB(0)	0
S_T3(1)	0
S_T3(0)	0
S_S1	0

S4

T1 ⟶ ALU_A

IR_{0-5} ⟶ SEG_in

SEG_out ⟶ ALU_B

ALU_C ⟶ T3

	S4
MEM_R	0
MEM_W	0
IR_W	0
IP_W	0
RF_W	1
T1_W	0
T2_W	0
T3_W	0
sel_ALU(2)	0
sel_ALU(1)	0
sel_ALU(0)	0
sel_shift(1)	0
sel_shift(0)	0
S_IP	0
S_MA1	0
S_RA3(1)	r (not X(1)))) xor (X(3) and (not X(2)) and X(
S_RA3(0)	(X(3) and X(1) and (not X(0)))) and not (X(3
S1_RD3	X(3) and X(2)
S_AA	"00"
S_AB(2)	0
S_AB(1)	0
S_AB(0)	0
S_T3(1)	0
S_T3(0)	0
S_S1	0

S5

T3 ⟶ Mem_A2

T2 ⟶ Mem_D2

	S5
MEM_R	0
MEM_W	0
IR_W	0
IP_W	0
RF_W	0
T1_W	0
T2_W	0
T3_W	1
sel_ALU(2)	0
sel_ALU(1)	0
sel_ALU(0)	0
sel_shift(1)	0
sel_shift(0)	0
S_IP	0
S_MA1	0
S_RA3(1)	0
S_RA3(0)	0
S1_RD3	0
S_AA	"10"
S_AB(2)	0
S_AB(1)	1
S_AB(0)	1
S_T3(1)	0
S_T3(0)	0
S_S1	0

S6

$IR_{0-8} \longrightarrow ZE9\_in$

$ZE9\_out \rightarrow shift\_in$

$Shift\_out \rightarrow T3$

	S6
MEM_R	0
MEM_W	1
IR_W	0
IP_W	0
RF_W	0
T1_W	0
T2_W	0
T3_W	0
sel_ALU(2)	0
sel_ALU(1)	0
sel_ALU(0)	0
sel_shift(1)	0
sel_shift(0)	0
S_IP	0
S_MA1	0
S_RA3(1)	0
S_RA3(0)	0
S1_RD3	0
S_AA	"00"
S_AB(2)	0
S_AB(1)	0
S_AB(0)	0
S_T3(1)	0
S_T3(0)	0
S_S1	0

S7

T2 → IP

	S7
MEM_R	0
MEM_W	0
IR_W	0
IP_W	0
RF_W	0
T1_W	0
T2_W	0
T3_W	1
sel_ALU(2)	0
sel_ALU(1)	0
sel_ALU(0)	0
sel_shift(1)	d (not X(2)) and (r
sel_shift(0)	X(2)
S_IP	0
S_MA1	0
S_RA3(1)	0
S_RA3(0)	0
S1_RD3	0
S_AA	"00"
S_AB(2)	0
S_AB(1)	0
S_AB(0)	0
S_T3(1)	1
S_T3(0)	0
S_S1	0

S8

TP → ALU_A

IR_{0-5} → SEG_in

SEG_out → shift_in

al_b → ALU-B

ALU_C → IP

	S8
MEM_R	0
MEM_W	0
IR_W	0
IP_W	1
RF_W	0
T1_W	0
T2_W	0
T3_W	0
sel_ALU(2)	0
sel_ALU(1)	0
sel_ALU(0)	0
sel_shift(1)	0
sel_shift(0)	0
S_IP	1
S_MA1	0
S_RA3(1)	0
S_RA3(0)	0
S1_RD3	0
S_AA	"00"
S_AB(2)	0
S_AB(1)	0
S_AB(0)	0
S_T3(1)	0
S_T3(0)	0
S_S1	0

S10

al_A → ALU_A

al_B → ALU_B

ALU_C → T3

ALU_Z → Z

ALU_ca → C

	S10
MEM_R	0
MEM_W	0
IR_W	0
IP_W	0
RF_W	0
T1_W	0
T2_W	0
T3_W	1
sel_ALU(2)	X(2) and not (X(3) and X(2) and (not X(1)) and (not X(0)))
sel_ALU(1)	X(1) or (X(3) and X(2) and (not X(1)) and (not X(0)))
sel_ALU(0)	(X(2) or X(1)) and X(0)
sel_shift(1)	0
sel_shift(0)	0
S_IP	0
S_MA1	0
S_RA3(1)	0
S_RA3(0)	0
S1_RD3	0
S_AA	"01"
S_AB(2)	0
S_AB(1)	0
S_AB(0)	1
S_T3(1)	0
S_T3(0)	0
S_S1	0

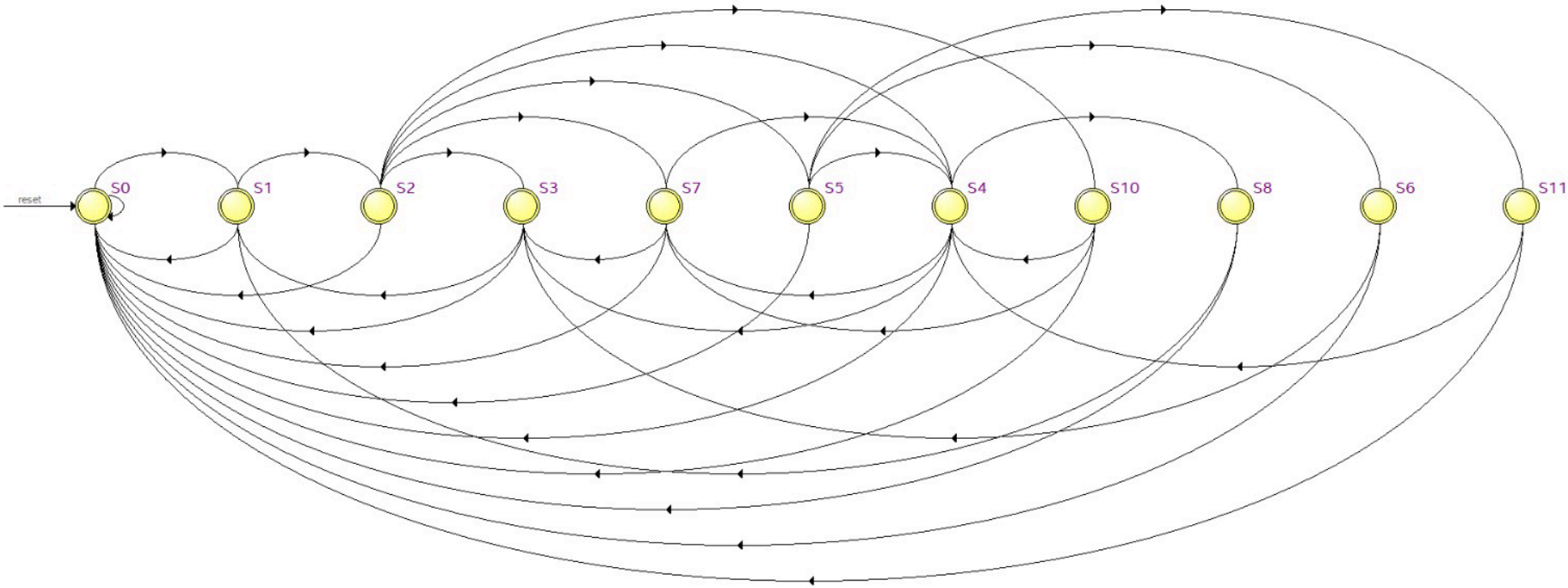
S11

T3 → Mem_A1

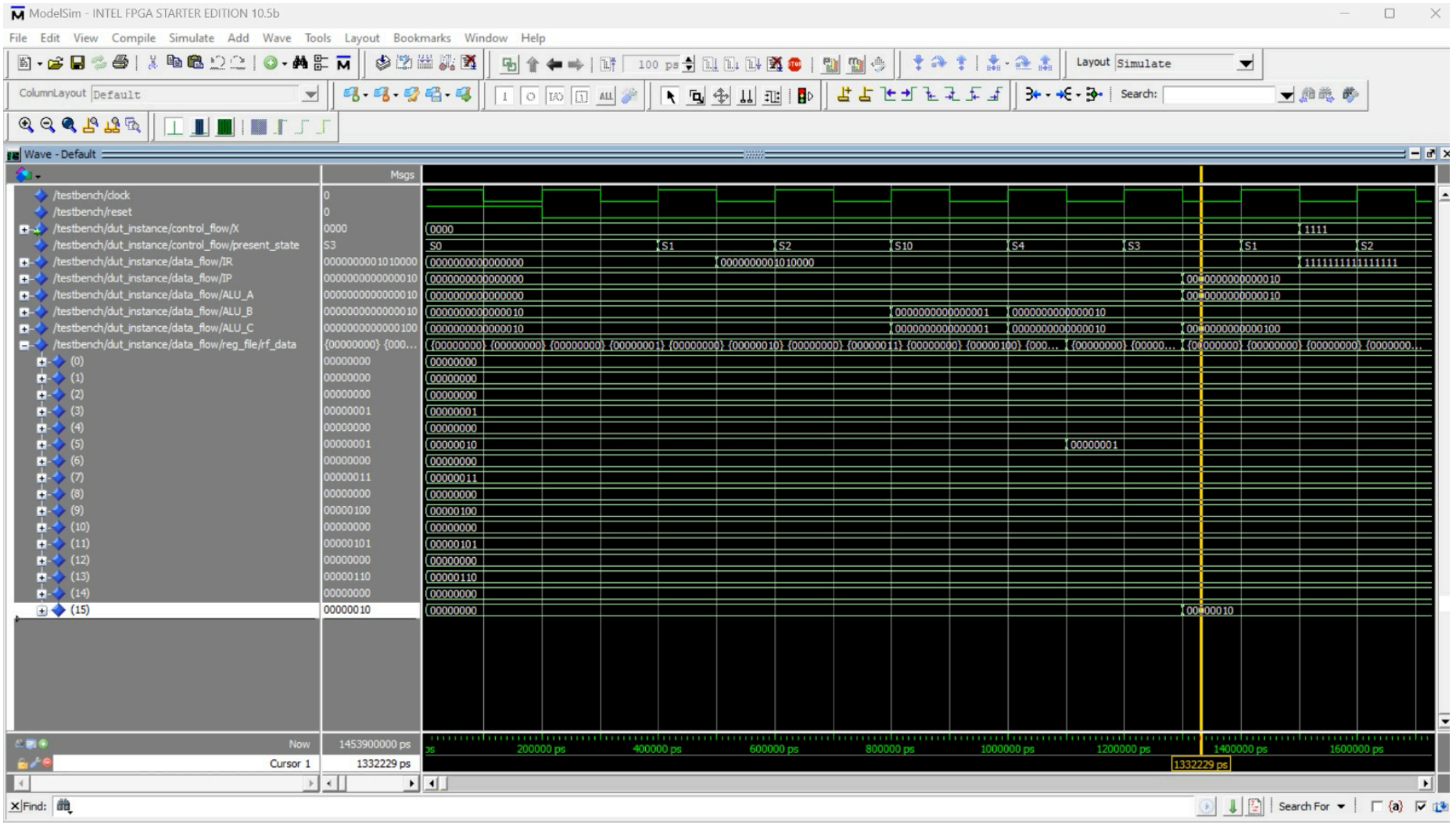
Mem D1 → T3

	S11
MEM_R	0
MEM_W	1
IR_W	0
IP_W	0
RF_W	0
T1_W	0
T2_W	0
T3_W	1
sel_ALU(2)	0
sel_ALU(1)	0
sel_ALU(0)	0
sel_shift(1)	0
sel_shift(0)	0
S_IP	0
S_MA1	1
S_RA3(1)	0
S_RA3(0)	0
S1_RD3	0
S_AA	"00"
S_AB(2)	0
S_AB(1)	0
S_AB(0)	0
S_T3(1)	0
S_T3(0)	1
S_S1	0

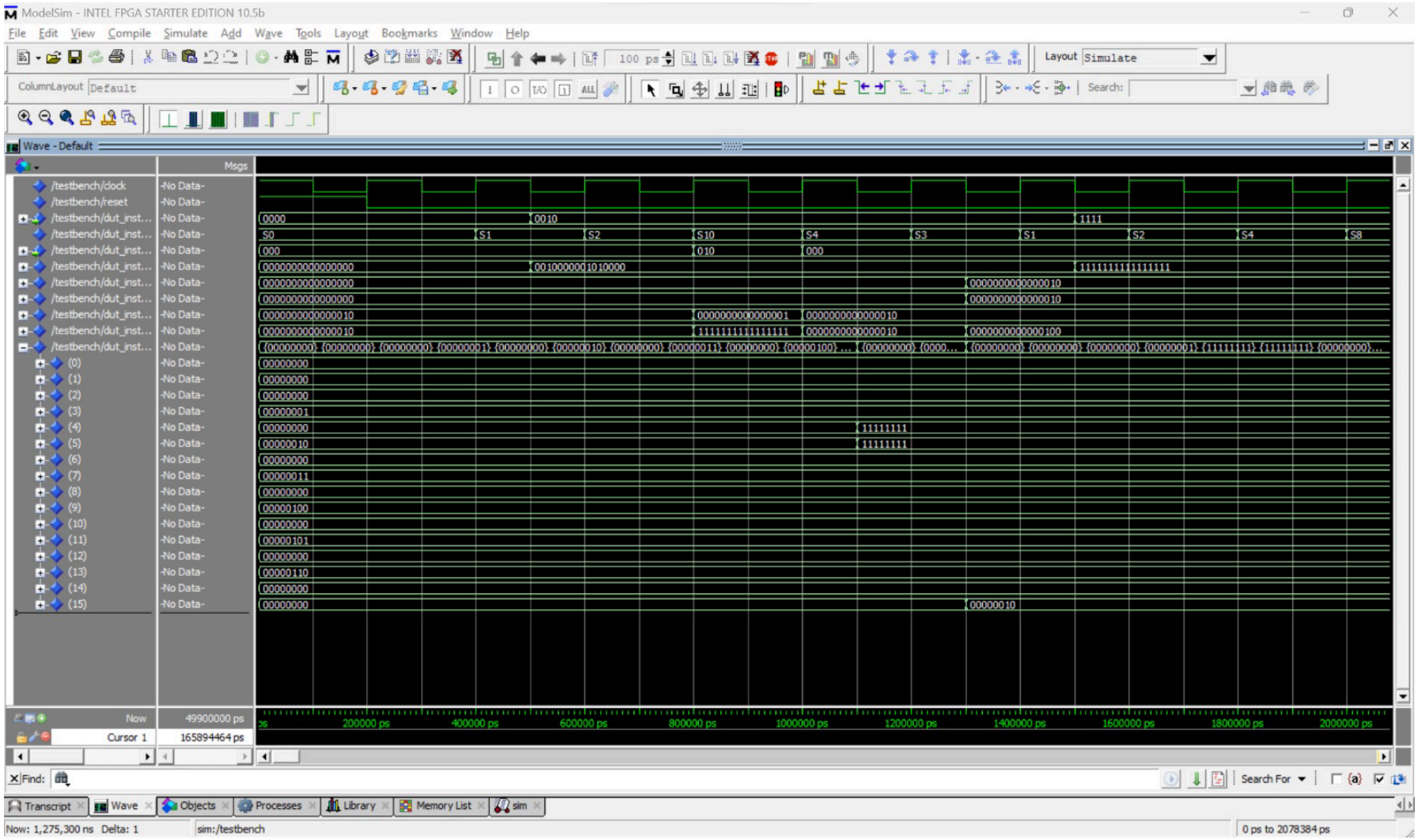
STATE DIAGRAM



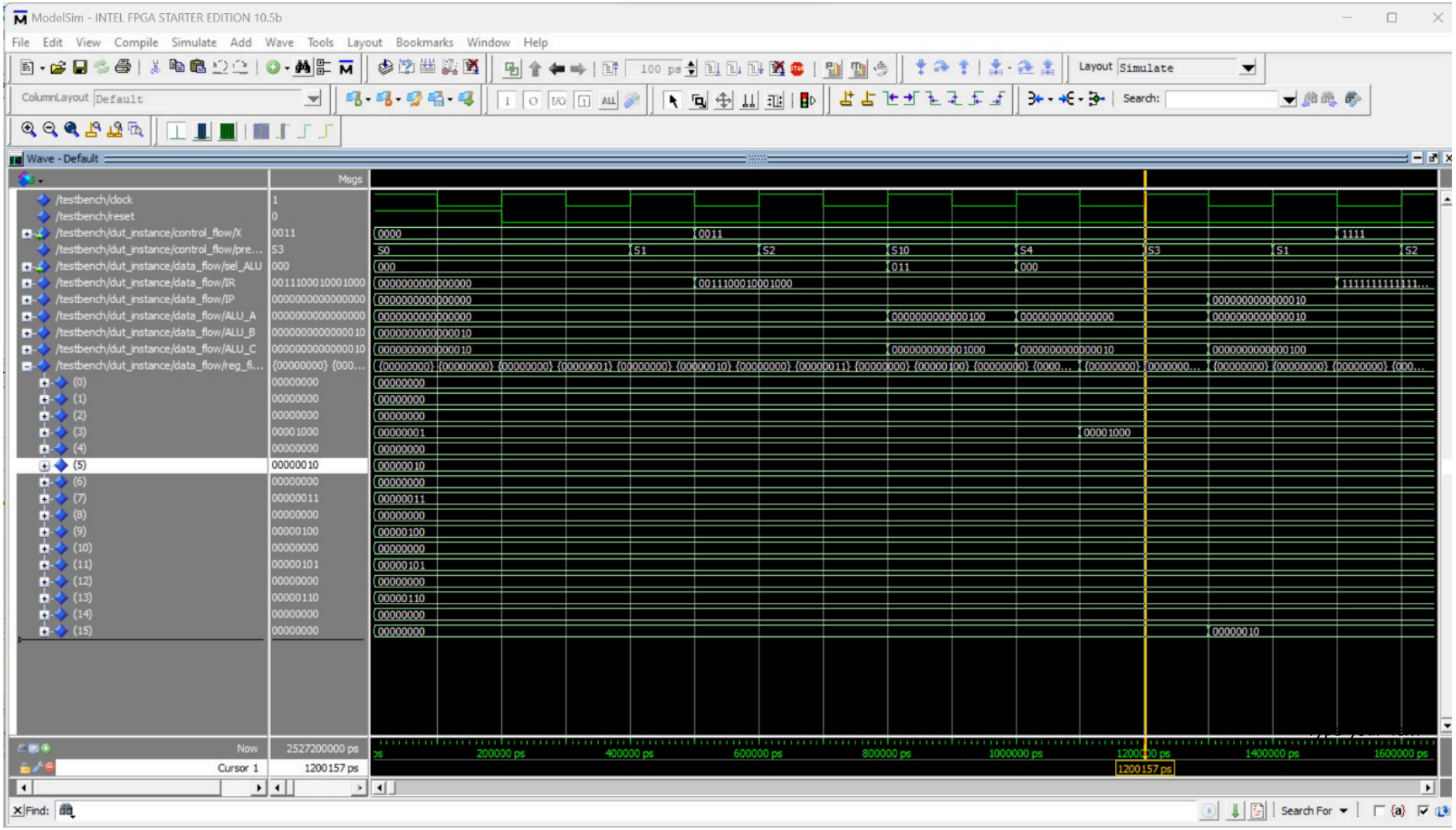
Simulations: ADD 000 001 010



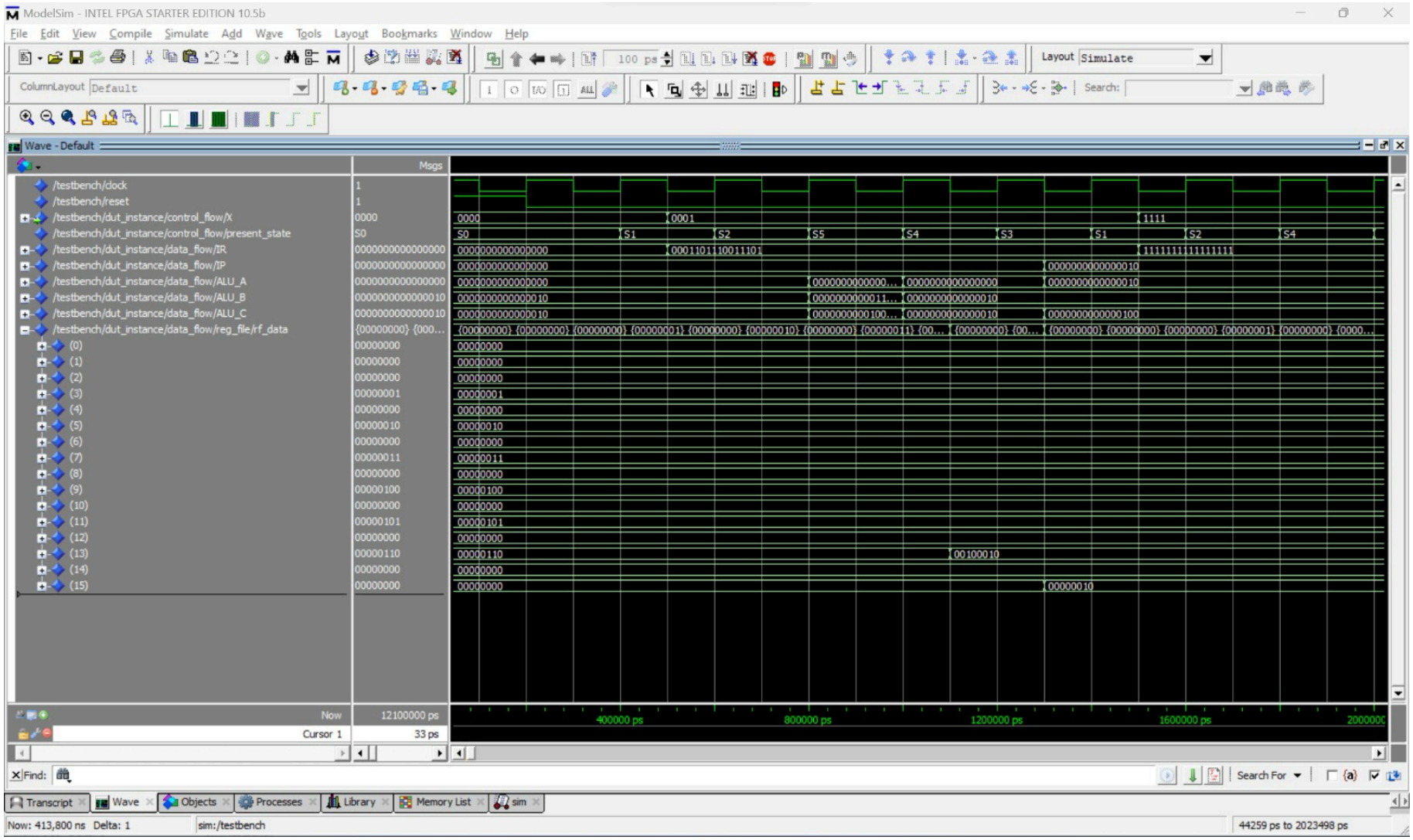
Simulations: SUB000 001 010



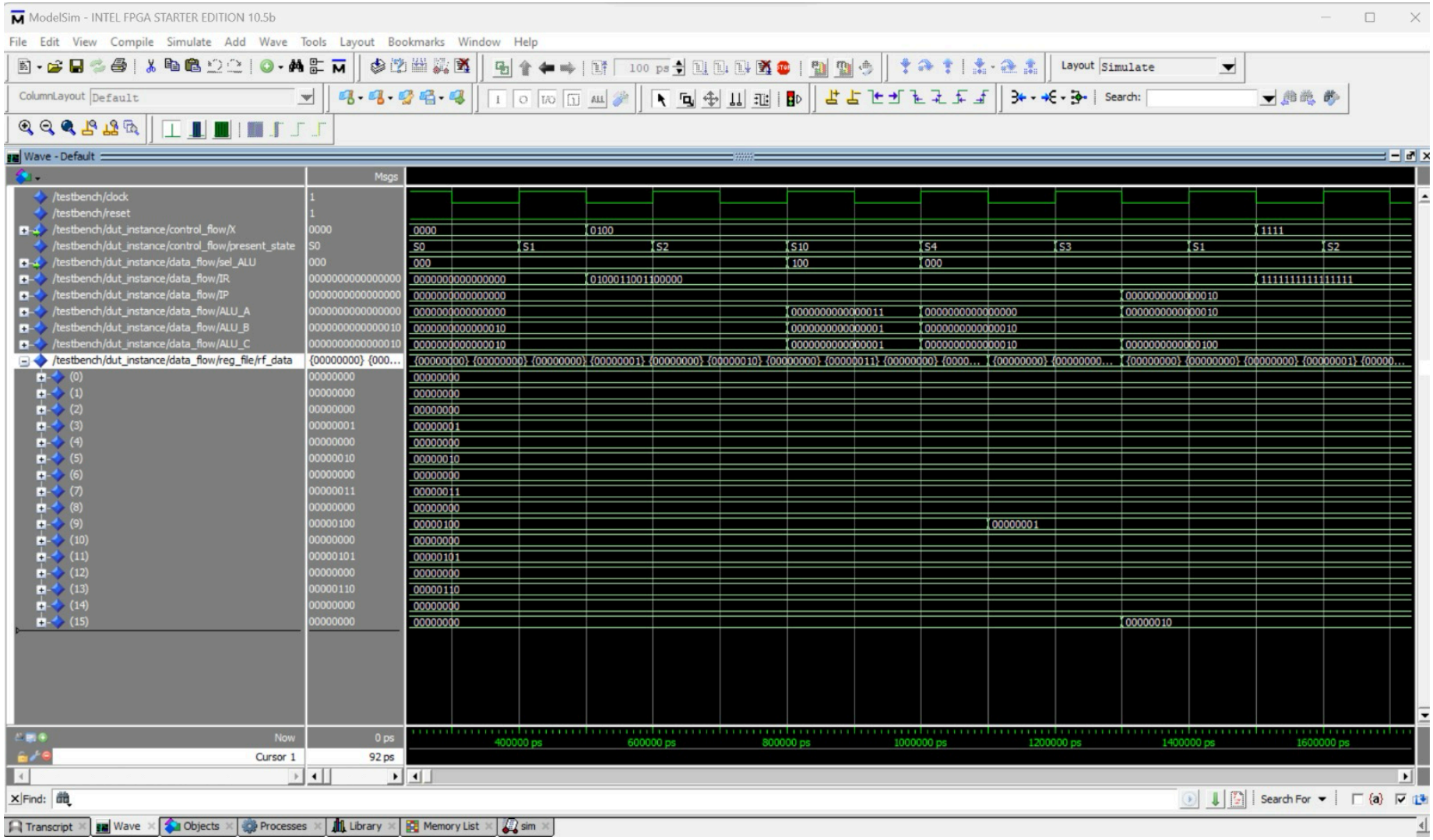
Simulations: MUL 100 010 001



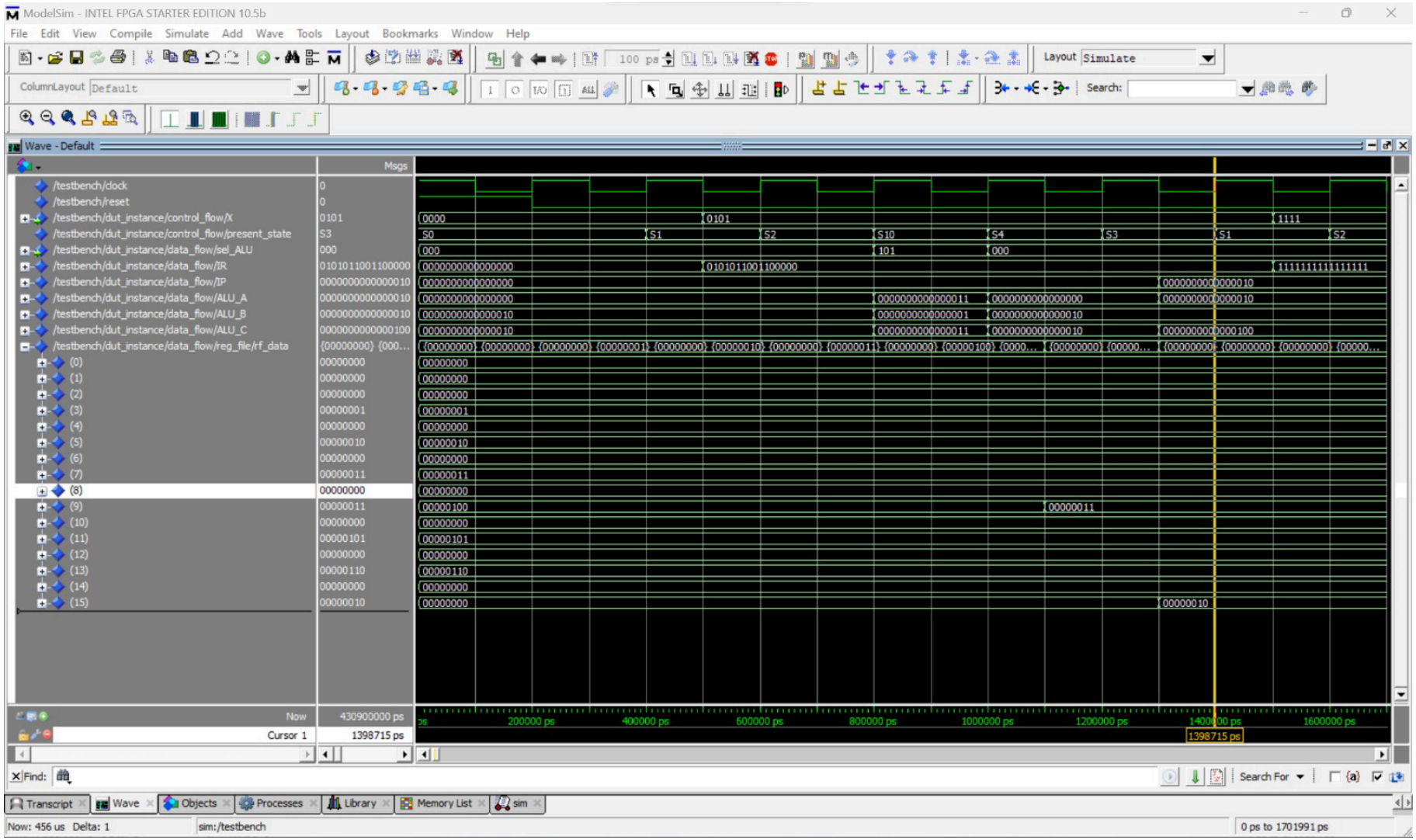
Simulations: ADI 101 110 011101



Simulations: AND 011 001 100

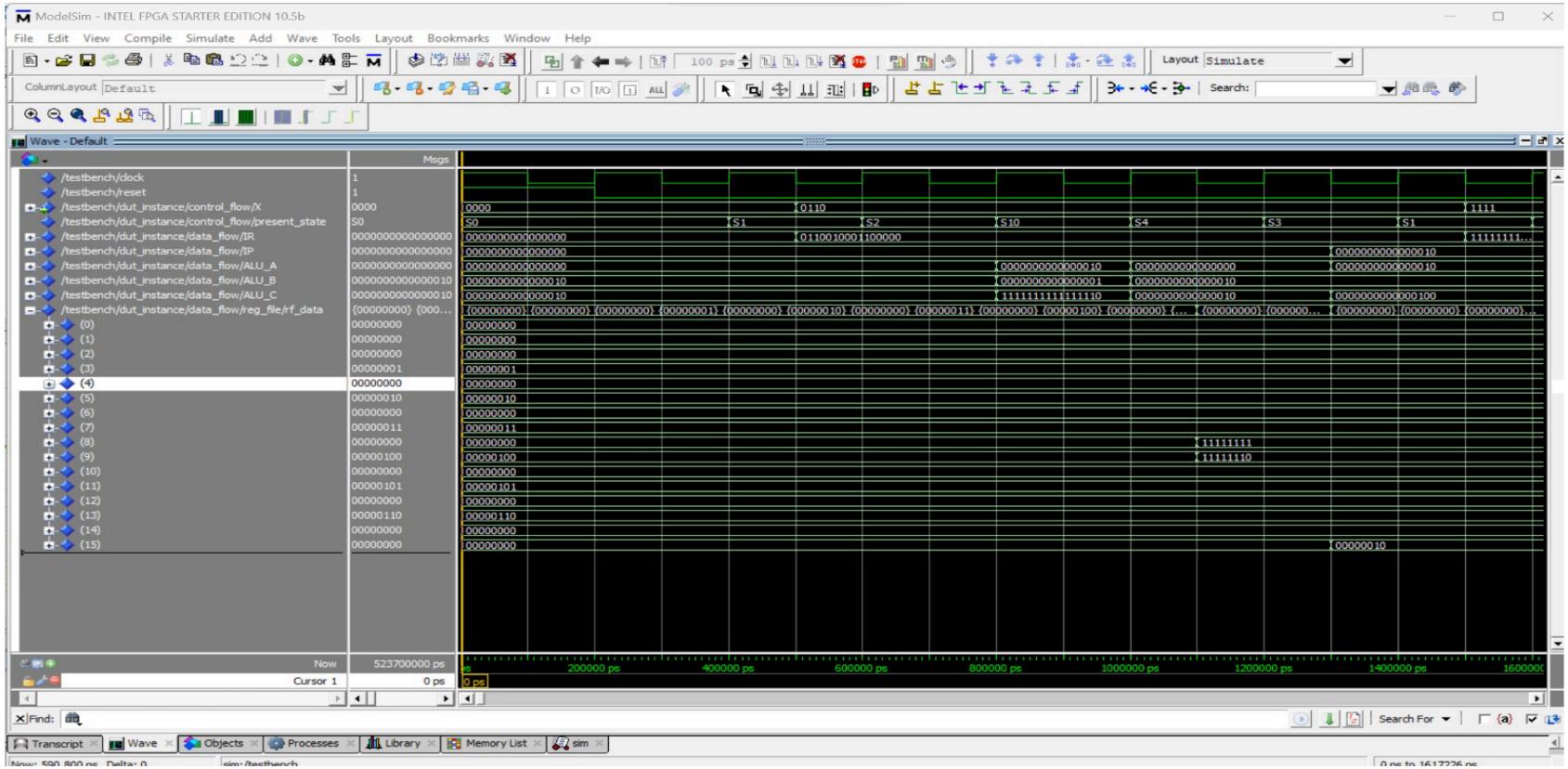


Simulations: ORA011 001 100

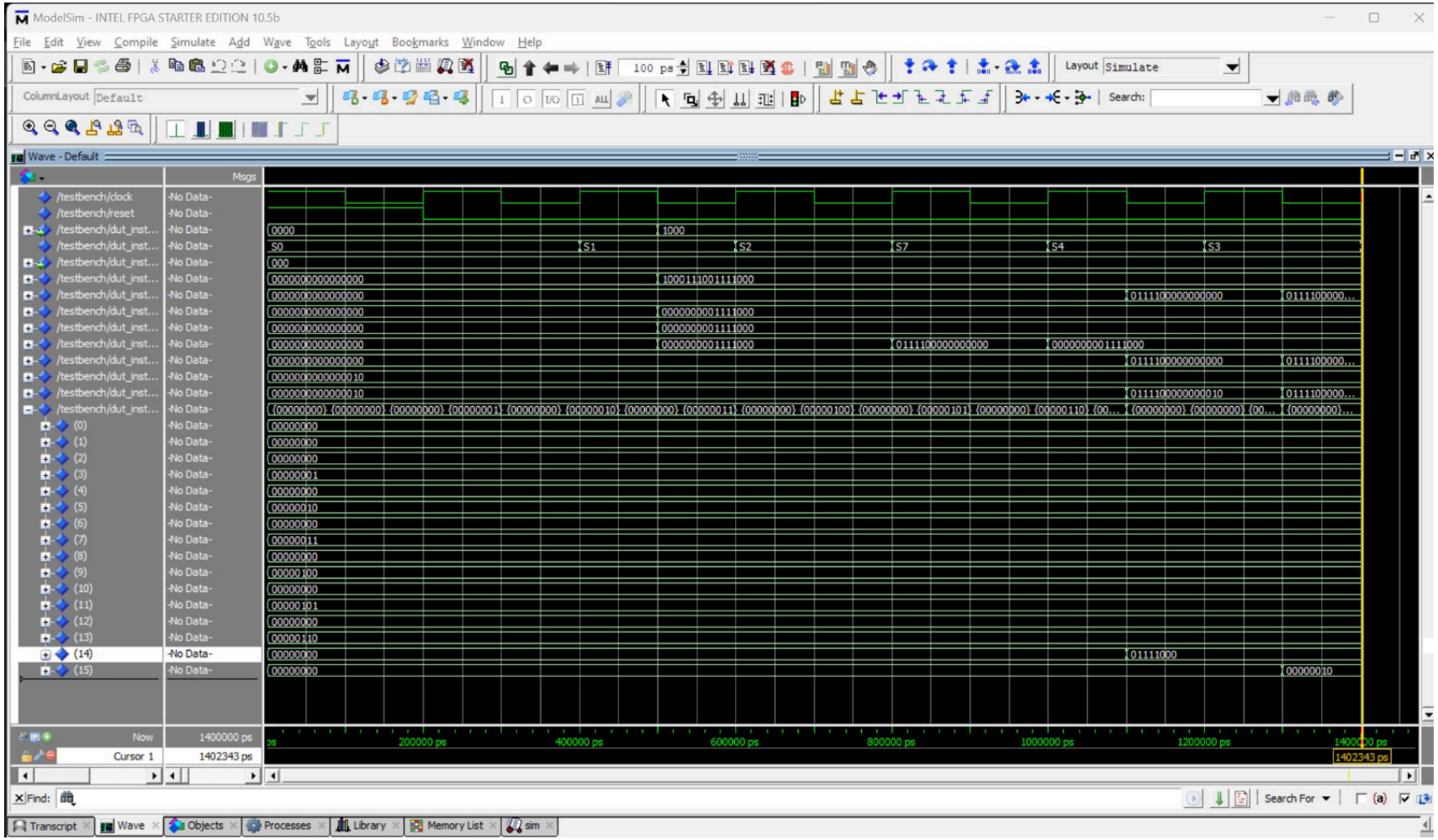


Simulations: IMP 010 001 100

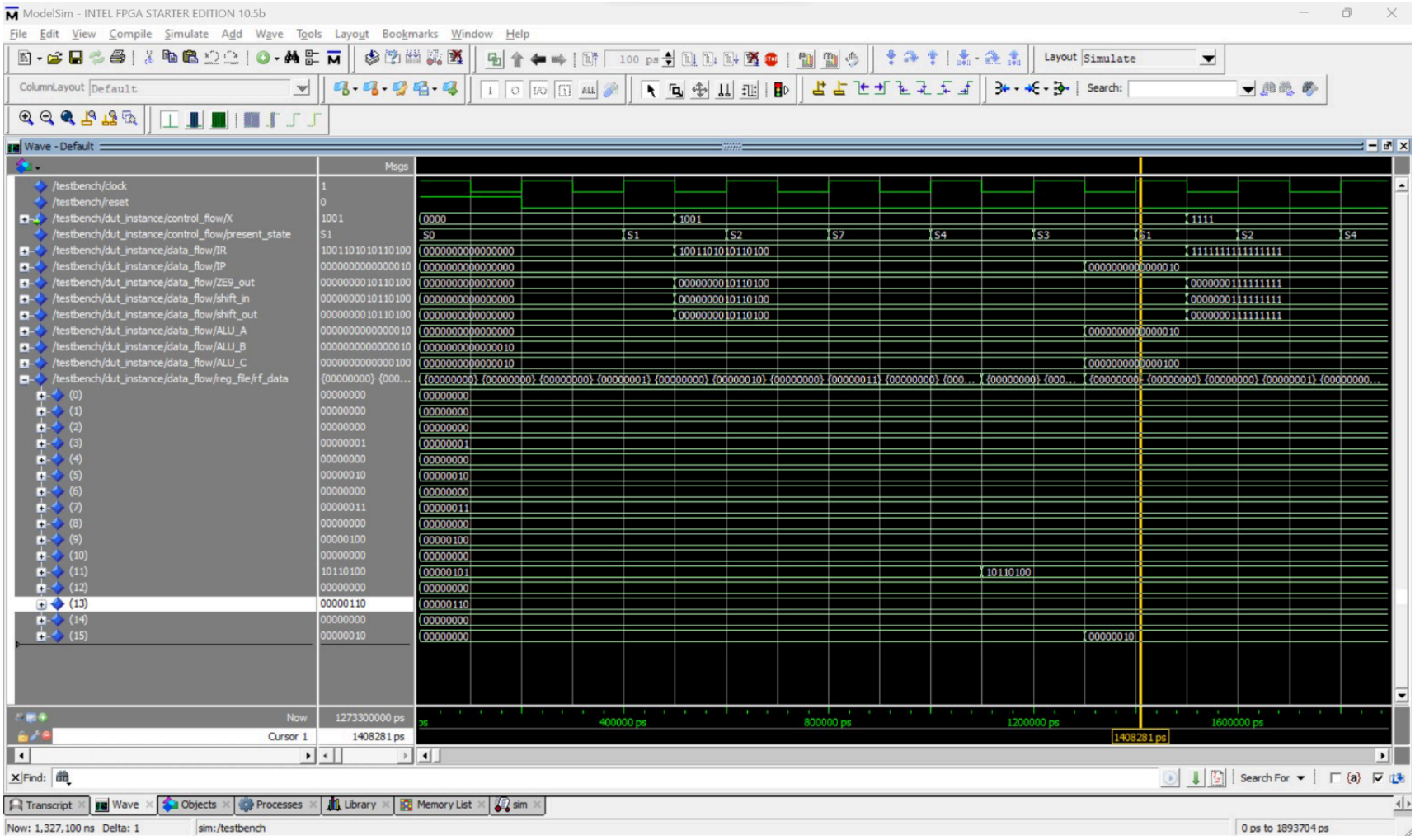
```
C:\Windows\System32\cmd.e
Microsoft Windows [Version 10.0.22621.2715]
(c) Microsoft Corporation. All rights reserved.

C:\Users\sdsha\OneDrive\Desktop\HAY_IMAGINARY_SUPERHUMANS\Testbench>python3 instruction_generator.py
Enter your Assembly Code:
IMP 010 001 100

C:\Users\sdsha\OneDrive\Desktop\HAY_IMAGINARY_SUPERHUMANS\Testbench>
```



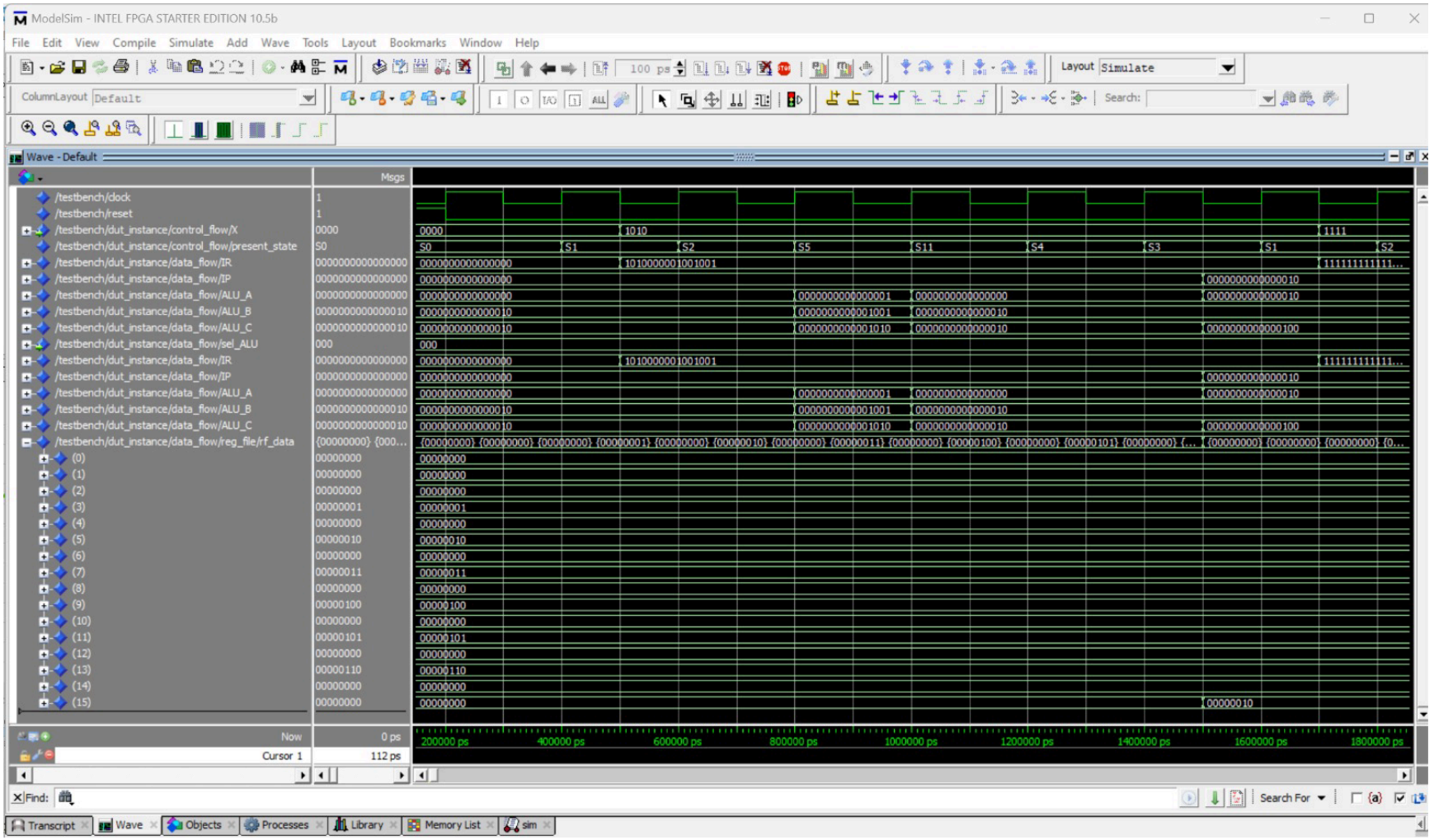
Simulations: LHI 111 01111000



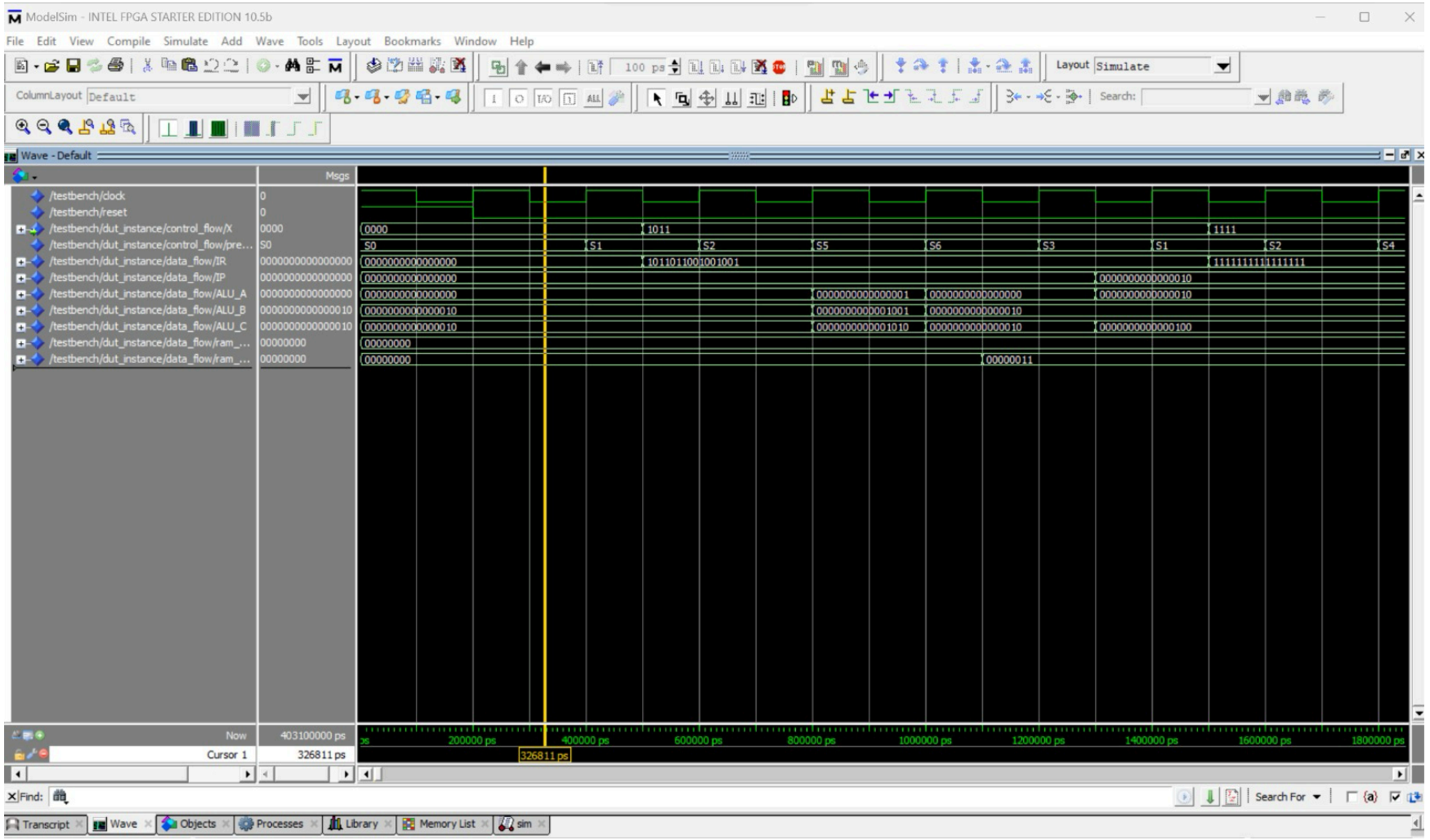
Simulations: LLI 101 10110100



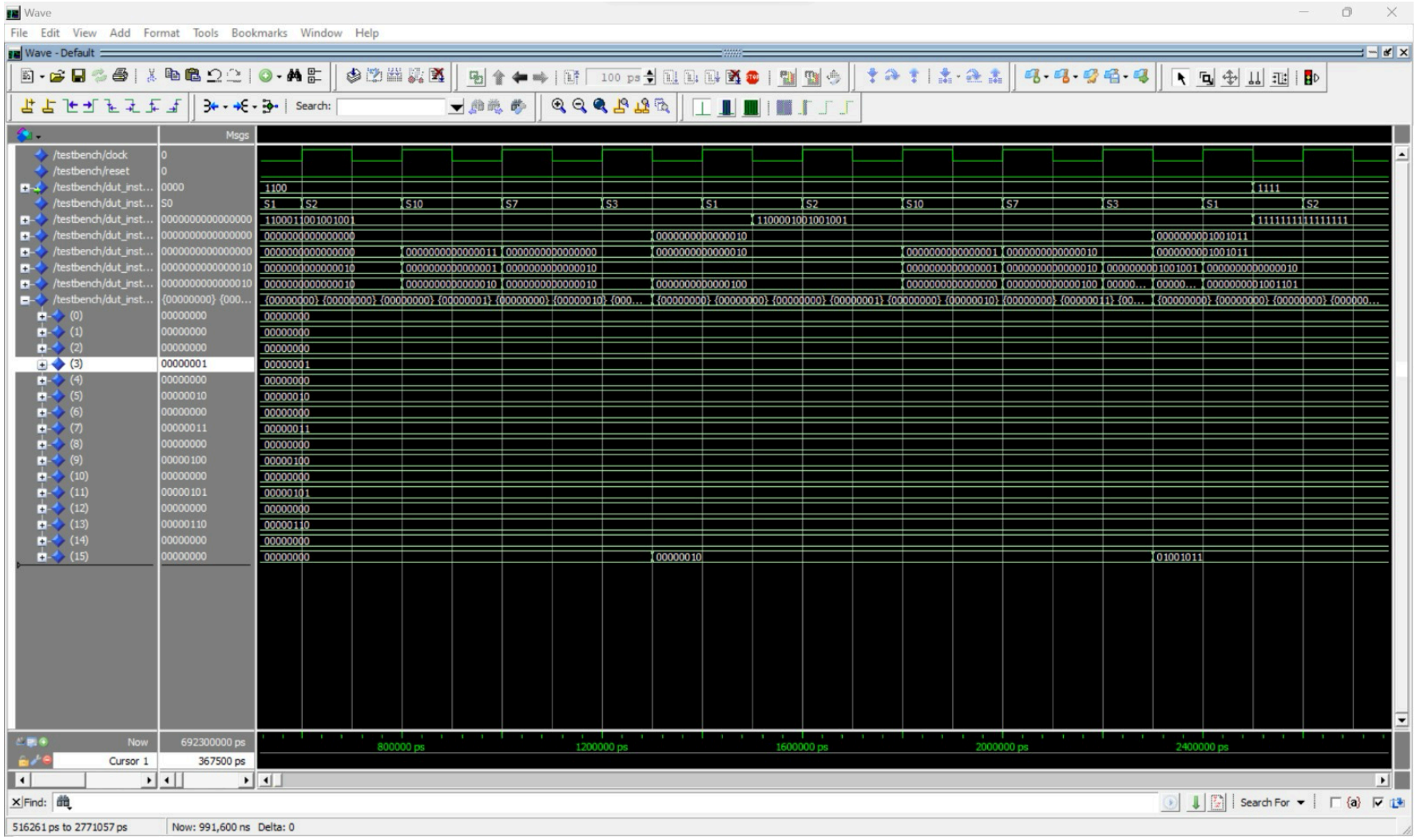
Simulations: LW000 001 001001



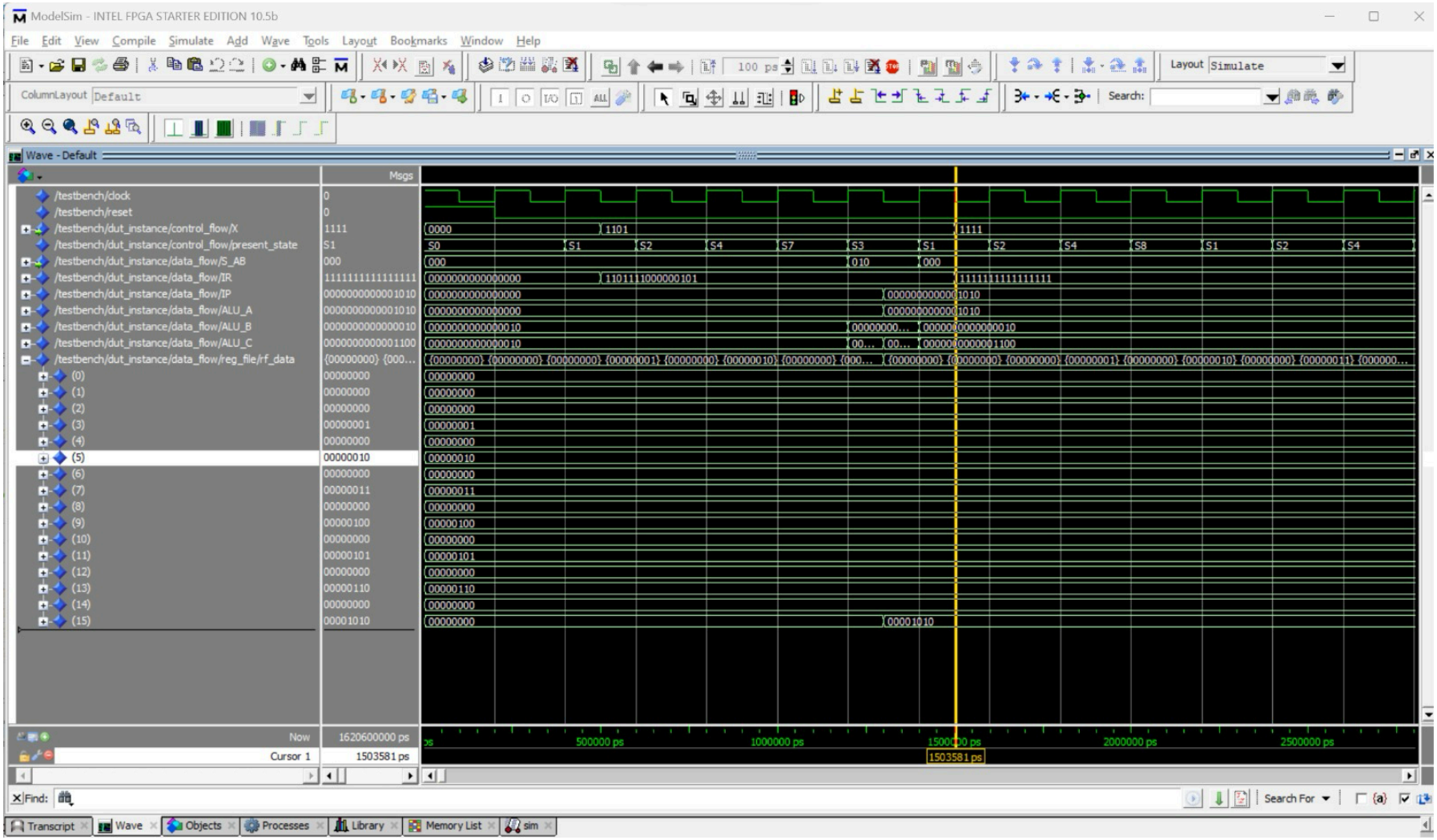
Simulations: SW 011 001 001001



Simulations: BEQ 011 001 001001 BEQ 001 001 001001



Simulations: JAL 111 00000101



Simulations: JLR 110 101