# EE224 PROJECT DESIGN DOCUMENT

## Problem Statement :

Design a computing system, IITB-CPU, whose instruction set architecture is provided. Use VHDL as HDL to implement. IITB-CPU is a 16-bit very simple computer developed for the teaching purpose. The IITB-CPU is an 8-register, 16-bit computer system, i.e., it can process 16 bits at a time. It should use point-to-point communication infrastructure.

## Group Members:


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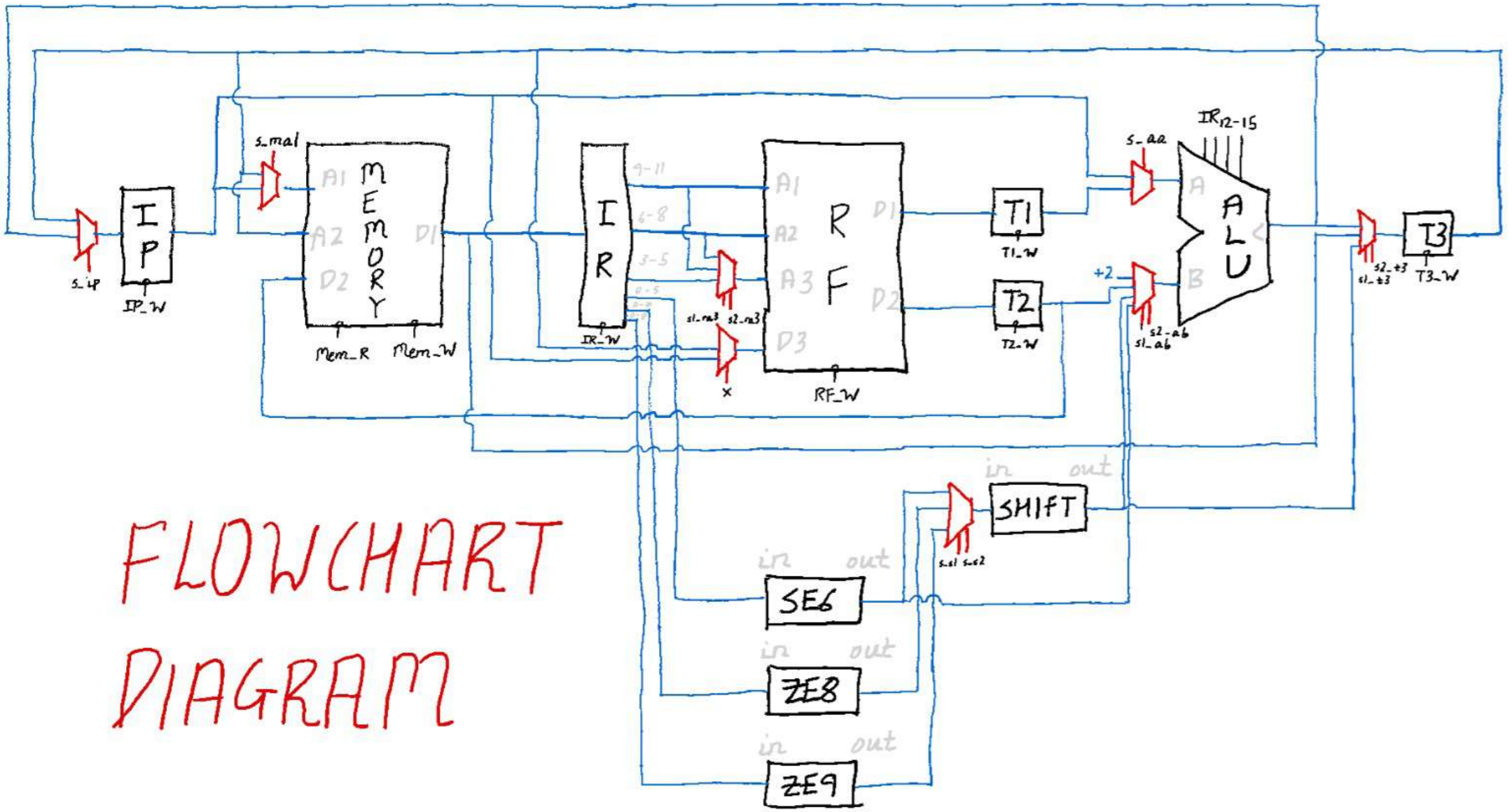
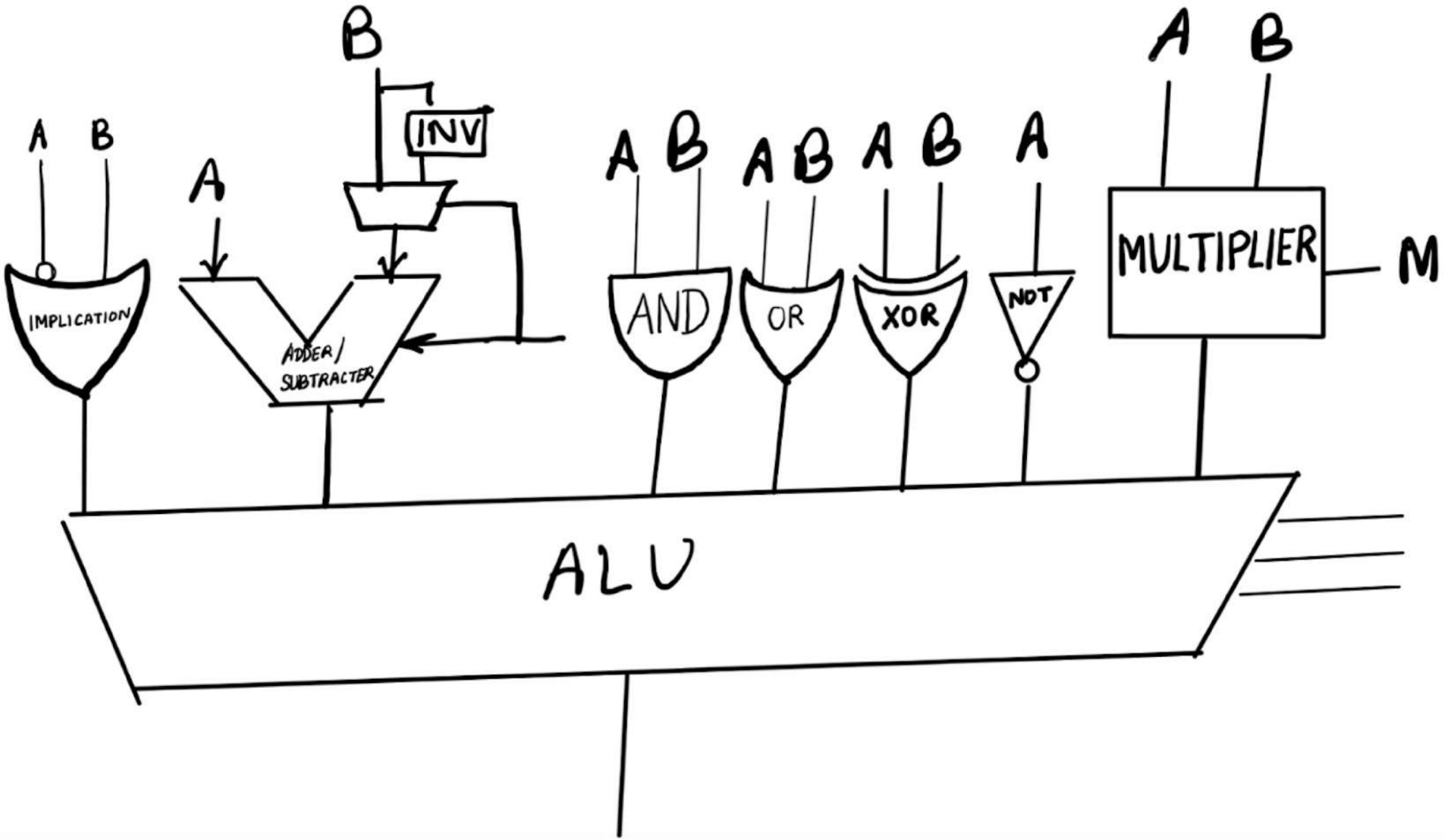
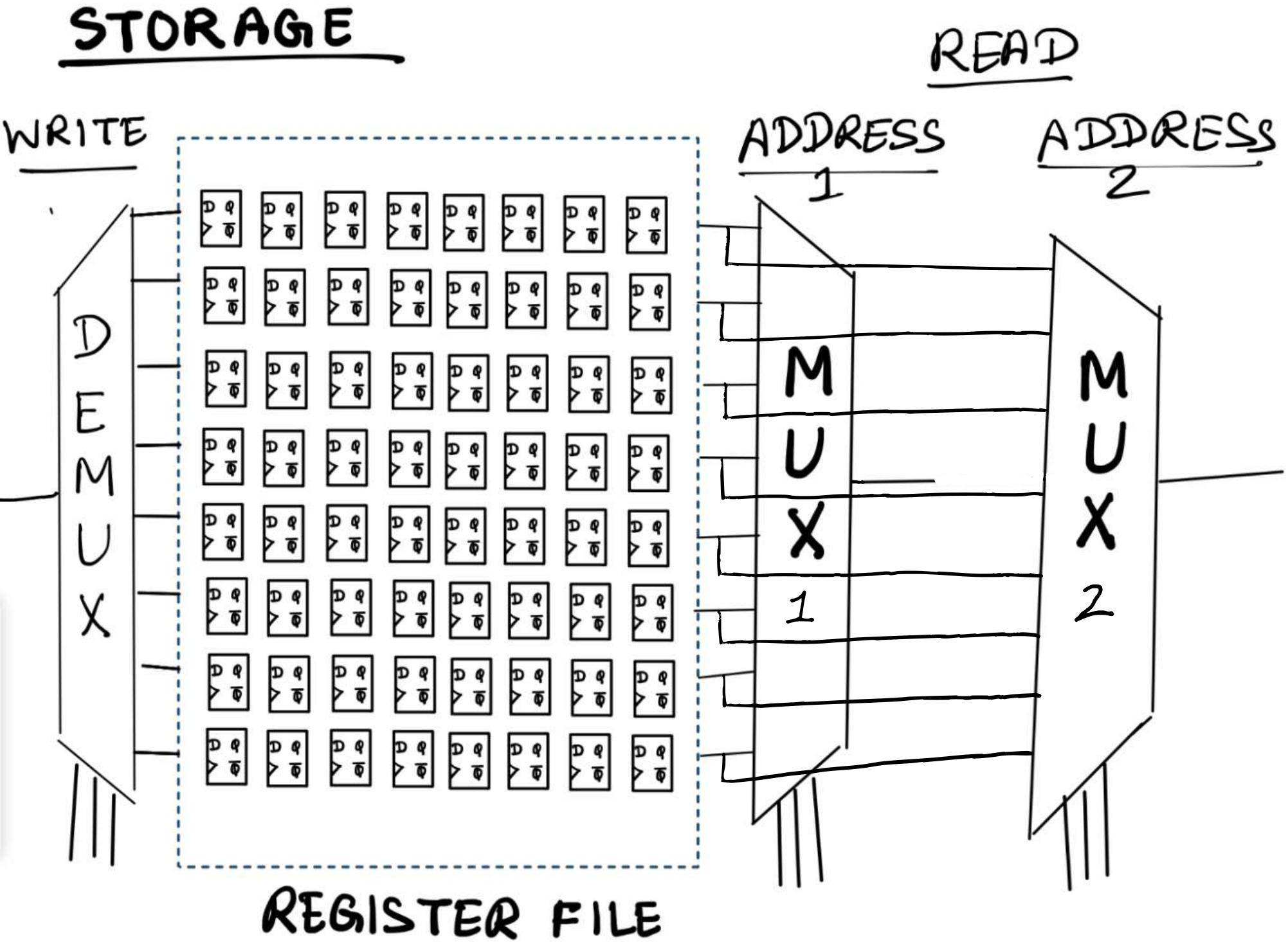

FLOWCHART
DIAGRAM
IP
IP_W
s_ip
s_mal
MEMORY
A1
A2
D2
D1
Mem_R
Mem_W
IR
IR_W
9-11
6-8
3-5
0-2
s1_ra3
s2_ra3
x
RF
A1
A2
A3
D1
D2
D3
RF_W
T1
T1_W
T2
T2_W
s_aa
+2
s2_ab
s1_ab
ALU
A
B
C
IR12-15
s2_t3
s1_t3
T3
T3_W
in
out
SHIFT
s_s1
s_s2
SE6
ZE8
ZE9


A
B
IMPLICATION
A
B
INV
ADDER/
SUBTRACTER
A
B
AND
A
B
OR
A
B
XOR
A
NOT
A
B
MULTIPLIER
M
ALU


STORAGE
READ
WRITE
ADDRESS 1
ADDRESS 2
DEMUX
MUX 1
MUX 2
REGISTER FILE

ADD SUB AND ORA IMP MUL

S1 → S2 → S3 → S4

S1 :

IP → Mem_A1

Mem_D1 → IR

S2 :

$IR_{9-11}$ → RF_A1

$IR_{6-8}$ → RF_A2

RF_D1 → T1

RF_D2 → T2

S3 :

T1 → ALU_A

T2 → ALU_B

ALU_C → T3

S4 :

T3 → RF_D3

X → RF_A3

IP → ALU_A

+2 → ALU_B

ALU_C → IP

ADI

S1 → S2 → S5 → S4

S1 :

IP → Mem_A1

Mem_D1 → IR

S2 :

$IR_{9-11}$ → RF_A1

$IR_{6-8}$ → RF_A2

RF_D1 → T1

RF_D2 → T2

S5 :

T1 → ALU_A

$IR_{0-5}$ → SEG_in

SEG_out → ALU_B

ALU_C → T3

S4 :

T3 → RF_D3

X → RF_A3

IP → ALU_A

+2 → ALU_B

ALU_C → IP

LW:

S1 ⟶ S2 ⟶ S5 ⟶ S6 ⟶ S4

S1:

IP ⟶ Mem_A1

Mem_D1 ⟶ IR

S2:

$IR_{9-11}$ ⟶ RF_A1

$IR_{6-8}$ ⟶ RF_A2

RF_D1 ⟶ T1

RF_D2 ⟶ T2

S5

T1 ⟶ ALU_A

$IR_{0-5}$ ⟶ SE6_in

SE6_out ⟶ ALU_B

ALU_C ⟶ T3

S6:

T3 ⟶ Mem_A1

Mem_D1 ⟶ T3

S4:

T3 ⟶ RF_D3

X ⟶ RF_A3

IP ⟶ ALU_A

+2 ⟶ ALU_B

ALU_C ⟶ IP.

SW

S1 ⟶ S2 ⟶ S5 ⟶ S7

S1 :

IP ⟶ Mem_A1

Mem_D1 ⟶ IR

S2 :

$IR_{9-11}$ ⟶ RF_A1

$IR_{6-8}$ ⟶ RF_A2

RF_D1 ⟶ T1

RF_D2 ⟶ T2

S5 :

T1 ⟶ ALU_A

$IR_{0-5}$ ⟶ SEG_in

SEG_out ⟶ ALU_B

ALU_C ⟶ T3

S7 :

T3 ⟶ Mem_A2

T2 ⟶ Mem_D2

IP ⟶ ALU_A

+2 ⟶ ALU-B

ALU_C ⟶ IP

LHI , LLI

S1 ⟶ S2 ⟶ S8 ⟶ S4

S1 :

IP ⟶ Mem_A1

Mem_D1 ⟶ IR

S2 :

$IR_{9-11}$ ⟶ RF_A1

$IR_{6-8}$ ⟶ RF_A2

RF_D1 ⟶ T1

RF_D2 ⟶ T2

S8 :

$IR_{0-7}$ ⟶ ZE8_in

ZE8_out ⟶ Shift_in

Shift_out ⟶ T3

S4 :

T3 ⟶ RF_D3

X ⟶ RF_A3

IP ⟶ ALU_A

+2 ⟶ ALU_B

ALU_C ⟶ IP

JAL

S1 → S2 → S9 → S10

S1 :

IP → Mem_A1

Mem_D1 → IR

S2 :

$IR_{9-11}$ → RF_A1

$IR_{6-8}$ → RF_A2

RF_D1 → T1

RF_D2 → T2

S9 :

$IR_{9-11}$ → RF_A3

IP → RF_D3

S10 :

$IR_{0-7}$ → ZE8_in

ZE8_out → Shift_in

Shift_out → ALU_B

IP → ALU_A

ALU_C → IP

JLR

S1 ⟶ S2 ⟶ S9 ⟶ S11

S1 :

IP ⟶ Mem_A1

Mem_D1 ⟶ IR

S2 :

$IR_{9-11}$ ⟶ RF_A1

$IR_{6-8}$ ⟶ RF_A2

RF_D1 ⟶ T1

RF_D2 ⟶ T2

S9 :

$IR_{9-11}$ ⟶ RF_A3

IP ⟶ RF_D3

S11

T2 ⟶ IP

BEQ.

S1 ⟶ S2 ⟶ S12 ⟶ S13

S1 :

IP ⟶ Mem_A1

Mem_D1 ⟶ IR

S2 :

$IR_{9-11}$ ⟶ RF_A1

$IR_{6-8}$ ⟶ RF_A2

RF_D1 ⟶ T1

RF_D2 ⟶ T2

S12

T1 ⟶ ALU_A

T2 ⟶ ALU_B

ALU_Z ⟶ Z

S13 :

IP ⟶ ALU_A

$IR_{0-5}$ ⟶ SE6_in

SE6_out ⟶ Shift_in

if (Z=1)

Shift_out ⟶ ALU_B

else

+2 ⟶ ALU_B

ALU_C ⟶ IP

# Finite State Machine:
# (FSM)