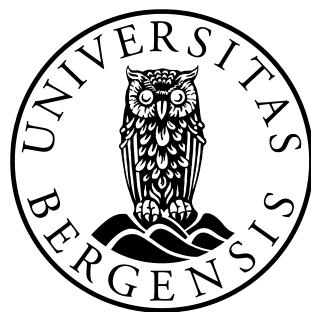


Radiation Testing of RCU2 Electronics

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Abstract

In Geneva in Switzerland we can find the largest particles accelerator ever built called Large Hadron Collider (LHC). The LHC is placed 100 meter below ground level in a 27 km long tunnel where four experiment areas are located, one of these experiment is A Large Ion Collider Experiment (ALICE). ALICE is built to study a matter known as Quark-gluons plasma, which will be generated under collisions of heavy ions. LHC is currently shutdown for maintenance and preparation for even higher energies. This period called Long Shutdown 1 (LS1), started January 2013 and will last until the end of 2014.

ALICE comprises of several sub-detectors, one of these are Time Projection Chamber (TPC), which is the main tracking device of ALICE. For LS1 it has been decided that a upgrade should be performed on the Readout Control Unit (RCU), which controls the readout in the TPC. The new RCU, named RCU2, will increase the present readout rate by a factor of up to 2.6, and will be more immune to radiation induced errors.

For the RCU2 design we introduces new components, where some of these hasn't been tested for radiation tolerance. The work presented through this thesis comprises of irradiation tests of these components, and the preparation process before radiation tests. The tested components consist of power regulators, bus transceivers, limiting amplifier, multiplexer/demultiplexer, buffer, comparator, Current Shunt Monitor and the RCU2's main FPGA, the Microsemi SF2 M2S050-FG896. The tests performed consist mostly of test for accumulative effects, but also test for Single Even Effect (SEE) will be performed for some of the components. The parts of the SF2 that were tested are SRAM, PLLs and Logic Element.

The radiation tests has been executed at Oslo Cyclotron Laboratory (OCL) in Oslo Norway, with a proton beam of 25 and 28 MeV and at The Svedberg Laboratory (TSL) in Uppsala Sweden, with a proton beam of 170 MeV.

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Acronyms

CERN	European Council for Nuclear Research
ALICE	A Large Ion Collider Experiment
OCL	Oslo Cyclotron Laboratory
DUT	Device Under Test
RCU	Readout Control Unit
LHC	Large Hadron Collider
FEE	Front End Electronic
FEC	Front End Card
FPGA	Field Programmable Gate Array
SEE	Single Even Effect
SEU	Single Event Upset
SET	Single Event Transient
SEL	Single Event Latchup
IC	Integrated Circuit
PCB	Printed Circuit Board
LVDS	Low-Voltage Differential Signaling
DAQ	Data Acquisition
SF2	SmartFusion2
CML	Current-Mode Logic
TPC	Time Projection Chamber
SRAM	Static Random Access Memory
TID	Total Ionizing Dose
ADC	Analog to Digital Converter
LET	Linear Energy Transfer
SoC	System On a Chip
CMOS	Complementary Metal Oxide Semiconductor
DCS	Control System board

SIU	Source Interface Unit
TSL	The Svedberg Laboratory
MSS	Microcontroller SubSystem
WSR	Windowed Shift Register

Chapter 1

Introduction

At CERN (European Council for Nuclear Research) in Switzerland there are being conducted experiment on fundamental structure of the universe. This is done by accelerating particles up to an energy level of 4 TeV per proton, and then collide with other particles on the same energy level. The largest accelerator is called Large Hadron Collider (LHC), and is the largest particle accelerator ever built, installed in a 27 km long tunnel. Particles are accelerated in both direction in the LHC. When the particles has reached high enough energy, particles from opposite directions are made to crash at 4 experiment areas, one of these is called ALICE (A Large Ion Collider Experiment). ALICE is built to study a matter known as Quark-gluons plasma [1], which will be generated under collisions of heavy ions. ALICE consists of several sub-detectors with different functionality. TPC is one of these, and is the main tracking detector placed closes to the beam-line, see section 2. Under a collision high particles will be generated, and will also pose a risk to the electronics used. It is therefore of highest importance to test everything that are planned to be used in the experiment for radiation.

One of the main boards used in the TPC detector is the Readout Control Unit (RCU). Now there has been decided that a new RCU shall be made, namely the RCU2. Because of the radiation level in the LHC, every active component used in the design of the RCU2 has to be tested for radiation to be sure that it won't fail when it is installed in the TPC detector.

1.1 How to Test

The radiation tests done through this work is mainly test for accumulative effects. Accumulative effects are effects caused by the total radiation of a component, and

are measured by the functionality and power consumption of the component, see section 3.4.2 for more information.

Previous research has been done on the radiation level in ALICE [2] and [15], and are used to decide if the tested components can be used or not.

Test for SEEs like Single Event Upset (SEU), Single Event Transient (SET) and Single Event Latchup (SEL) on a Microsemi SmartFusion2 (SF2) System On a Chip (SoC) Field Programmable Gate Array (FPGA) have also been performed.

1.2 About This Work

I started working on the RCU2-project in the autumn of 2013. Already before I started working, the design and the schematic layout for the RCU2 was basically finished. In the design process components that was already tested or are proven to be radiation hard was used when possible, but such components weren't always available. So my work in the project has been to do irradiation tests on components for the RCU2 design which didn't have any record of being radiation tested before.

The Integrated Circuits (ICs) which I have tested consist of: SoC FPGA, power regulators, bus transceivers, limiting amplifier, multiplexer/demultiplexer, buffer, comparator and Current Shunt Monitor. In order to investigate the radiation tolerance of these circuits, I had to first acquire good knowledge of radiation induced effect that may occur in such devices. I also needed to study these components to be able to find a reasonable test methodology. Further, I had to familiarize myself with CAD tools such as *expedition PCB* and *DXdesigner* and programming and developing environments like Libero and labVIEW in order to develop a sufficient hardware and software based test setup for the components.

The RCU2's main FPGA the Microsemi SF2, has been the main focus through this work. That is because this component will be hard to replace, and a functional failure on this one, may set the whole RCU2 out of function. The radiation effects that were tested on for SF2 are, SRAM blocks for SEU, logic elements for SEU and SET, and in general SEL. These effects can be read about in section 3.4.1.

The irradiation test was executed in four periods, three times at OCL with a proton beam of 28 MeV and 25 MeV where all components have been tested, and one time at TSL with a proton beam of 170 MeV, where only the SF2 SoC FPGA was tested. A SF2 starter-kit was used when designing test for this IC, and test code was written in VHDL and C. To be able to detect SEL the current on the FPGA had to be measured. Therefore a current measurement board was made for that task.

To summarize, this work has been consisting of practical work like making Printed Circuit Boards (PCBs), writing test code in VHDL, making labVIEW programs and making test codes in C. It has also consisting on getting the necessary knowledge of the components tested, learning to program in VHDL and C, as well as learning to use the tools and programs for the different tasks.

Chapter 2

ALICE Experiment

Since 1954 physicists at European Council for Nuclear Research (CERN) have studied the nucleus and its structure to find the fundamental structure of the universe. CERN is the world largest research center for nuclear and particle physics, and has a total of 21 member states. One of the biggest attractions at CERN is the Large Hadron Collider (LHC), which is a circular particle accelerator placed in a 27 km long tunnel around 100 meters beneath ground level. This is the last accelerator in a chain of up to 7 (depending on which particle to accelerate), see picture 2.0.1, where the particles gradually accelerate to higher and higher energies, up to their maximum energy of 4 TeV and speed close to the speed of light. When particles has reached this energy level accelerated particles from opposite direction are made to collide inside 4 different experiment areas, where one of these is called A Large Ion Collider Experiment (ALICE), see figure 2.0.2.

The ALICE detector is a heavy ion detector. Its main purpose is to study a state of matter called quark-gluon plasma which will be generated when heavy ions collides. Under the collisions a temperature 100 000 times higher than the temperature of the sun is generated. There is then high enough energy to split the protons and neutrons, and achieve a plasma of unbound quarks and gluons, and that is called quark-gluon plasma.

All ordinary matter in today's universe is made up of atoms. Each atom contains a nucleus composed of protons and neutrons (except hydrogen, which has no neutrons), surrounded by a cloud of electrons. Protons and neutrons are in turn made of quarks bound together by other particles called gluons. No quark has ever been observed in isolation: the quarks, as well as the gluons, seem to be bound permanently together and confined inside composite particles, such as protons and neutrons.

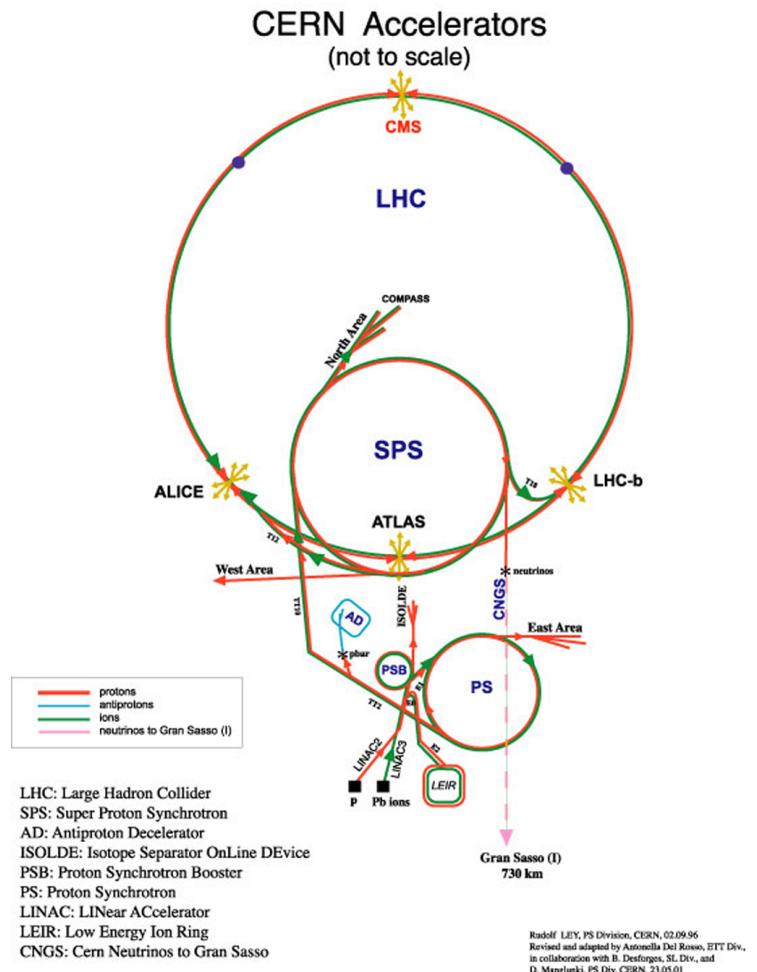


Figure 2.0.1: CERN accelerators [3]

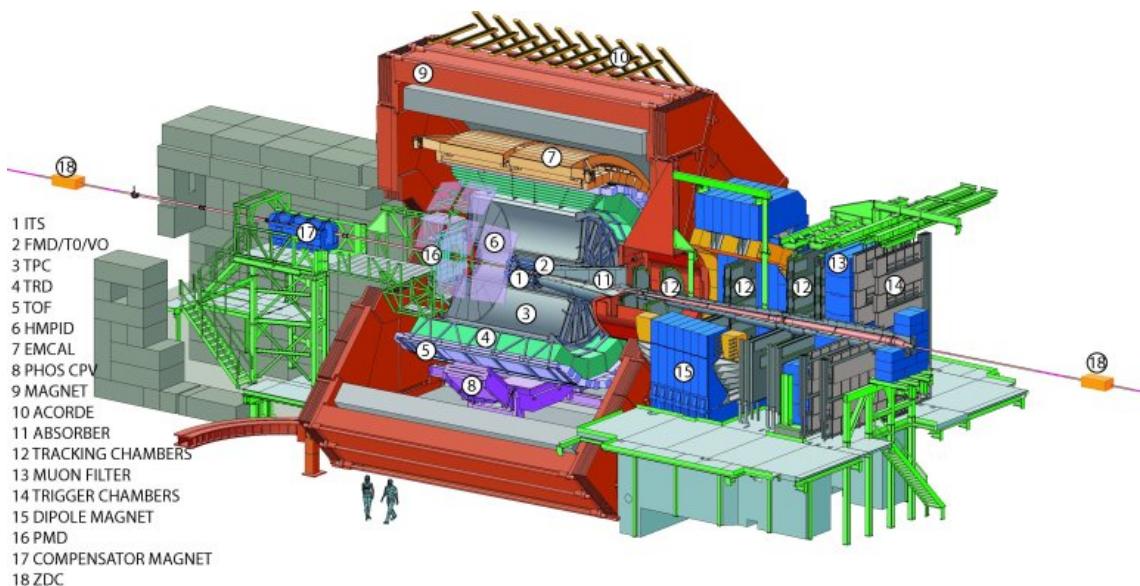


Figure 2.0.2: Layout of the ALICE experiment [4]

2.1 The Time Projection Chamber TPC

The ALICE detector comprises several sub-detectors, where one of these is the Time Projection Chamber (TPC). The TPC is the main tracking detector of ALICE. The functions of TPC are tracking particles, measure the charged particles momentum and identification of particles. A drawing of the TPC can be seen in figure 2.1.1. The TPC detector has a cylindrical shape, with an inner radius of 85 cm and outer radius of 250 cm, and has an overall length of 510 cm. The detector is made up of a large cylindrical field cage, filled with 88 m^3 of 90% Ne gas and 10% CO_2 gas. A high voltage electrode is placed in the center of the detector, dividing the TPC into two drift regions, and making an electric field between electrode and the two end plates. When a charged particle is generated inside the detector, the gas inside the cage will be ionized. The free electrons and the ions will then drift in the electric field between the high voltage electrode and the two end plates. At the end-plates we find the Readout Chamber which is divided into 18 trapezoidal sectors, where each sector is again divided into the inner and outer chamber. In the readout chamber, there are a total of 560 000 readout pads.

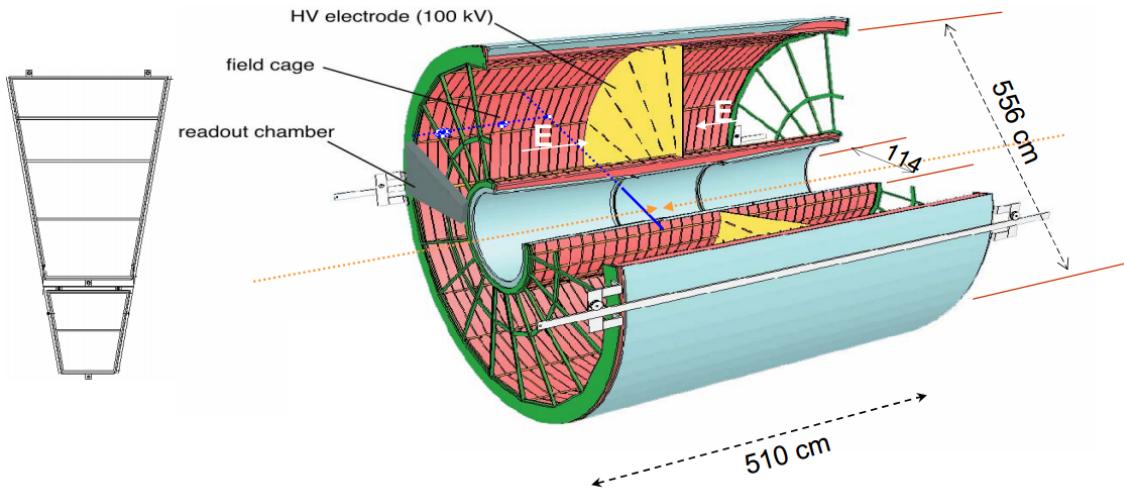


Figure 2.1.1: Layout of the TPC [4]

2.2 The TPC Front End electronics FEE

Each of the 36 sections (2×18) are also divided into 6 readout partitions, that is 2 in the inner chamber and 4 in the outer chamber. There are a total of 216 RCU connected to a total of 4356 Front End Card (FEC) which is connected to all of the 560 000 readout pads, and all together this sums up the Front End Electronic (FEE), see figure 2.2.1. In short, the task of the FEE is to read out the charge received at the readout pads, process it and send useful data to a computer.

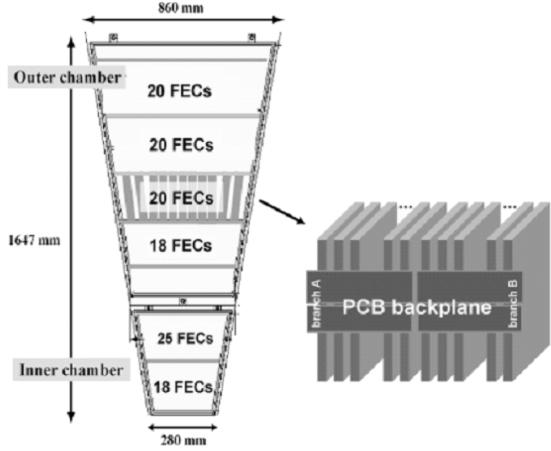


Figure 2.2.1: A TPC sector. Showing how FEC is placed [5]

2.2.1 Front End Card FEC

A current signal given by one of the pads, is sent into a Front End Card (FEC) which consist of three basic functional units, see block diagram in figure 2.2.2. The first unit is a charge sensitive amplifier/shaper called PASA, the second unit is a 10-bit 10 MHz low-power Analog to Digital Converter (ADC) and the last unit is a digital circuit that performs the baseline subtraction, tail cancellation, zero-suppression¹, formatting and buffering. The ADC and the digital unit together constitute the so called ALTRO chip. There are 16 PASA chips and 16 ALTRO chips on the FEC, the PASA chip is connected to 16 readout pads each, which gives a total of 128 readout pads for each FEC.

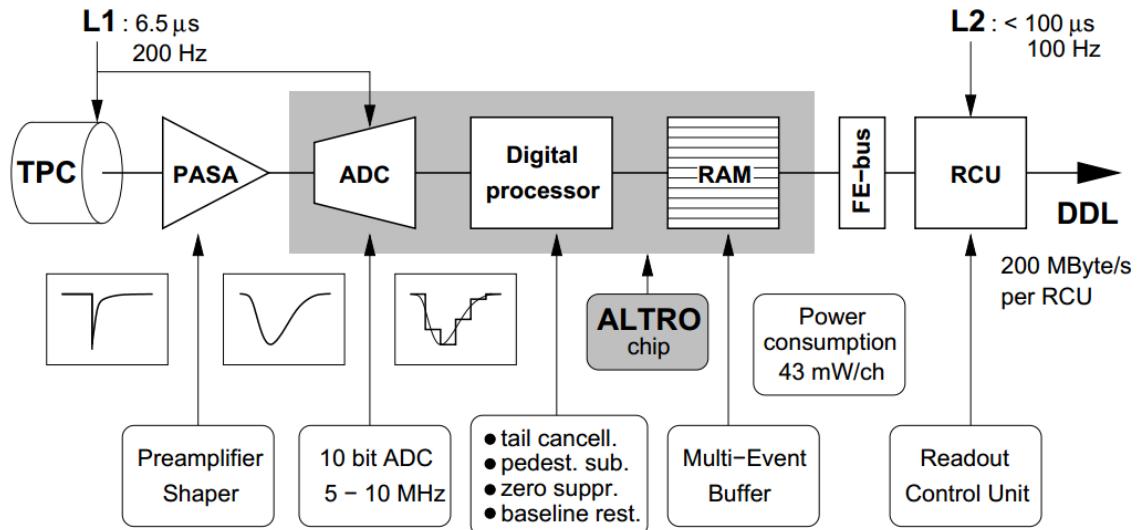


Figure 2.2.2: Block diagram of the Front End Card [4]

¹Zero Compressions means that signal below a given threshold will be filtered away.

2.2.2 Readout Control Unit RCU

One Readout Control Unit (RCU) is connected to one row of FECs (up to 25 pieces), through a backplane², see figure 2.2.1. The RCU task is to control the entire Front End Electronic (FEE) all the way from the readout pads through the FECs, and out to a Data Acquisition (DAQ) System. The RCU consist of three separated boards which are the Motherboard board, the Control System board (DCS) board and the Source Interface Unit (SIU) board. Most of the RCU functions are controlled by the Xilinx Virtex-II Pro FPGA. This FPGA are controlling the readout process of the TPC detector. It is also responsible for moving data from the FECs to the Source Interface Unit (SIU) board, where data is transmitted via an optical link to the Data Acquisition system, where data is stored and is made accessible for analysis.

The Xilinx Virtex-II Pro is a Static Random Access Memory (SRAM) based FPGA. SRAM cells are vulnerable for Single Event Upsets (SEUs), see section 3.4.1. Therefore a flash based FPGA, Actel ProASIC is used to monitor the SRAM memory and reprogram/reconfigure if an error occurs.

The DCS board is basically an embedded computer running Linux. This board is connected through an Ethernet link to a computer on the outside of the ALICE detector. Through it, we are even able to upgrade and reprogram the FPGAs of the RCU. So even though the hardware is inaccessible after it has been mounted in the TPC, the SIUs board gives some kind of flexibility. In addition, it has an optical interface, receiving the clock and trigger information from the Timing, Trigger and Control system, also called TTC.

2.2.3 RCU2

Why Upgrade RCU

LHC is currently shutdown for maintenance and preparation for even higher energies. This period, called Long Shutdown 1 (LS1), lasts until end of 2014. The present TPC readout electronics will be a limiting factor with the foreseen readout rate for the next run period (run2). The bus between RCU and FECs is not able to read all data for high occupancy events, like Pb-Pb collisions. In addition stability issues related to SEU on the SRAM based FPGA have been observed with the present setup. 9 % of the run time had to be stopped because of errors in the TPC readout electronics.

²A backplane is a PCB board, that connects Front End Cards to a Readout Control Unit. This is used instead of cables to get a more stability, and to keep things in place.

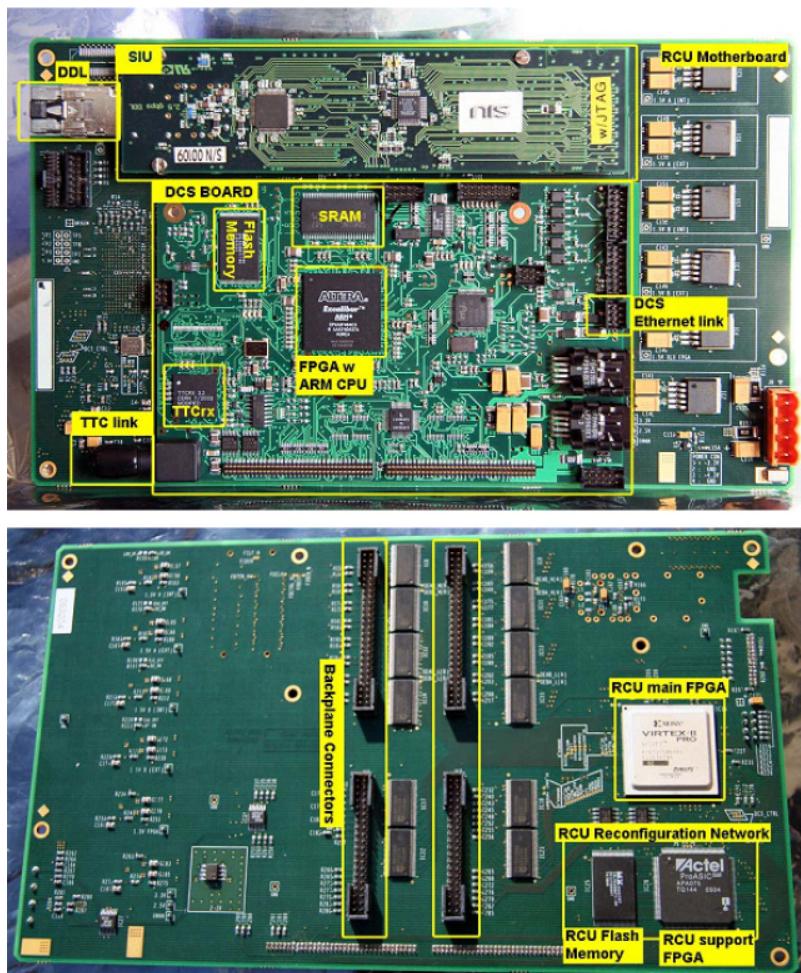


Figure 2.2.3: The Readout Control Unit top side and bottom side [5]

The new Readout Control Unit, the RCU2

The main challenge with making the RCU2 was to develop a solution that gives the needed performance improvement, and at the same time was feasible within the limited time-frame. Therefore some of the old infrastructure has to be reused, like cables for Ethernet, Trigger and power and the cooling envelops.

The main difference between the RCU2 and RCU1 is that the main FPGA, the Xilinx Virtex-II Pro, has been replaced by a Microsemi SmartFusion2 (SF2) System On a Chip (SoC) FPGA M2S050-FG896. This is a flash-based³ FPGA which has SEU immune configuration memory, as well as several other radiation tolerance measures implemented [6]. It also comes with a Microcontroller Subsystem which is based on a hardcore ARM Cortex-M3 microcontroller. On Microcontroller Subsystem we are able to build a Linux system, which replace the functionality of the Control System board (DCS)-card. The ProASIC was also not need as a reconfiguration FPGA anymore, but will still be used as a radiation monitor, this part of the RCU2 is now called RadMon, and consists of a ProASIC and SRAM chips. Another issue encountered in the design was that the TTCrx chip that was used for handling the clock and trigger signal on RCU1 was out of stuck and obsolete. This is being replaced by an optical receiver and a limiting amplifier. The limiting amplifier has been tested in this thesis, see section 4.2.7.

One of the limits with the old setup was that the bus between RCU and FECs was to slow. This was fixed by dividing the readout into 4 sections instead of 2, which effectively doubled the readout speed. Therefore all of the backplanes had to be redesigned and replaced.

³Flash-based FPGA means that configuration registers is saved in flash memory cells. Compared to SRAM-based FPGA where configuration is saved in SRAM cells, flash-based FPGA is much more tolerant against radiation.

Chapter 3

Radiation and Radiation effect on Semiconductor Devices

Radiation and radiation effects are a known challenge when designing electronics which are going to be used at CERN. There is therefore of highest importance to know about these effect, how they affect the electronics, how much damage they can cause and how we can protect and prevent the radiation effect to do damage.

This chapter is based on references [7], [8], [9], [10] and [11] if not otherwise stated.

3.1 Interaction of Radiation with Matter

Radiation is defined as a process which energy in the form of energetic particles or electromagnetic waves is transmitted through a medium or space. Radiation is normally divided into two categories, which are *Charged radiation* and *Neutral radiation*.

Charged radiation consist of charged particles like protons (p), alpha (α) and beta (β) particles and heavier ions. Neutral radiation consist of neutral particles like neutrons (n) and photons from gamma (γ) and X-rays. Particles which interact with a material will deposit some or all of its energy in the interaction, and can either interact with atoms, electrons, nucleus or the particles inside a nuclei. How much energy is deposited and which of these a particle will interact with is depended on the energy, mass, the charge of the particle and what material it interacts with. One of the main differences between charged particle and neutral particle is that charged particles will be affected by the Coulomb force, which is the attraction or

repulsion of particles or objects because of their electric charge. In the next sections we will look more closely on how a charged particle and neutral particle interact with matters.

3.2 Charge particle and their Interaction with Matters

When a charged particle with high speed is passing through a material it will experience multiple elastic and inelastic collisions with the atoms in the material, resulting in slowing down or stopping the particle. When a particle collides with an atom there are several processes that can contribute to the loss of energy. They are:

- Inelastic scattering towards atomic electrons
 - Excitation and ionization
- Elastic scattering towards atomic electrons
 - Ramsauer Effect
- Inelastic scattering towards Nuclei
 - Nuclear reaction
- Elastic scattering towards Nuclei
 - Rutherford/Nuclear scattering
- Other processes
 - Bremsstrahlung and Cherenkov radiation

Which of these that contributes to most of the loss of energy is depended on the initial energy, velocity, mass and charge of the particle as well as the properties of the material it collides with. For example, for heavy charge particles (protons or heavier ions), inelastic collisions with the atomic electrons in a material will contribute to most to the energy loss of the particle. A common expression for these processes is called "stopping power".

3.2.1 Stopping Power

If we have a particle with a given energy passing into a material, where dE is the mean energy that the particle losses by traveling through a path segment, dx of the material. Then $-\frac{dE}{dx}$ is the stopping power or also called the "rate" of energy loss for the particle. The stopping power depends on the type and energy of the radiation and on the properties of the material it passes.

The classical expression that describe the stopping power is the *Bethe Bloch formula*, and is written as you can see in equation 3.1.

$$S = -\frac{dE}{dx} = \frac{n_A Z_A Z^2 e^4}{4\pi\epsilon_0 m_e V^2} \left[\ln\left(\frac{2m_e v^2}{I}\right) - \ln\left(1 - \frac{v^2}{c^2}\right) - \frac{v^2}{c^2} \right] \quad (3.1)$$

n_A	Number of atoms per unit volume
Z_A	Average atomic number of the material
Z	Atomic number of particle
e	Electron charge
c	Speed of light
ϵ_0	Vacuum Permittivity
m_e	Electron rest mass
v	Particle velocity
I	Effective material ionization potential

3.2.2 Specific Stopping Power

Another way of looking at stopping power is by looking at energy loss as function of mass per area 3.2. Here $\xi = \rho x$ and ρ is the density of the material. The extension for specific stopping power is normally given as $[\frac{\text{MeVcm}^2}{\text{g}}]$

$$S = -\frac{dE}{d\xi} = -\frac{1}{\rho} \frac{dE}{dx} \quad (3.2)$$

From this formula we see that if we are considering two different particles with the same velocity, the only factor that changes is Z^2 . Therefore heavier particles will experience larger energy loss in a material then lighter ones. In figure 3.2.1 we can see specific energy loss for different particles in air. We can see that the value of $\frac{dE}{dx}$ for different types of particles approaches a near-constant broad minimum value at energies above several hundred MeV, where their velocity approaches the velocity of light.

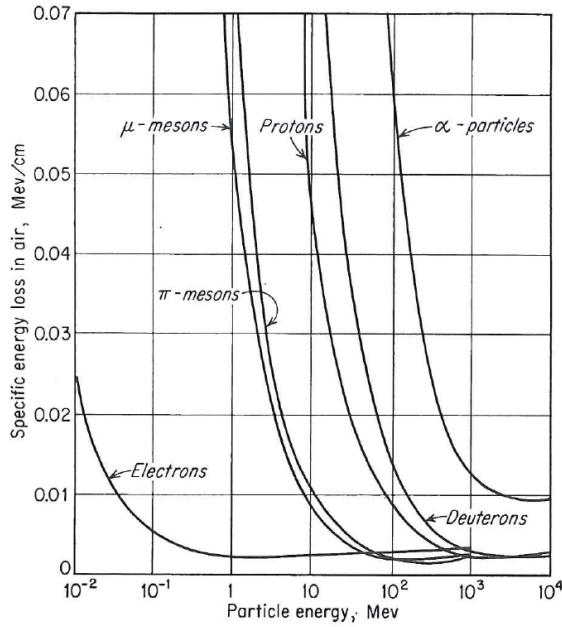


Figure 3.2.1: Variation of the specific energy loss in air versus energy of the charge particles shown

At low particles energies, where charge exchange between the particles and absorber becomes important, the Bethe Bloch formula begins to fail. That is because the positively charged particles will then tend to pick up electrons from the absorber, which effectively reduce its charge and consequently linear energy loss, and will at the end become a neutral atom.

3.2.3 Linear Energy Transfer LET

Linear Energy Transfer (LET) is closely related to stopping power of a particle, but instead of focusing on energy loss of the particle, LET focuses on the energy that is deposited in a local volume. For low energies, LET is often said to be equal to the stopping power, even though the particle energy that turn into photons may escape the local area. For higher energies, small particles like ionized electrons can escape the local volume. The local volume is defined by the user, and can be everything from part of a molecule to a whole organ. One alternate definition of LET can be seen in equation 3.3,

$$L_{\Delta} = \left(-\frac{dE}{dx} \right)_{\Delta} \quad (3.3)$$

where Δ is the upper energy limit for the secondary electrons included in the calculations. If Δ is set to ∞ , all secondary electrons are included in the calculations,

making LET the same as stopping power.

3.3 Neutral particle and their Interaction with Matter

3.3.1 Neutrons

Neutrons are subatomic structures that are present in most atomic nuclei. Neutrons carry no charge and can therefore not interact with matter by means of the Coulomb force, which dominates the energy loss mechanisms for charged particles. Neutrons can also penetrate several centimeters into matters without any type of interactions, making neutrons hard to detect. When neutrons undergo an interaction, it is with the nucleus of the absorbing material. This can result in total disappearance of the neutron resulting in one or more secondary radiations, or change of the direction of the neutron. The secondary radiations from neutrons can largely ionizing.

3.3.2 Photons

Photons may appear from gamma rays or X-rays. Photons has as neutrons no charge, and are therefore not affected by the Coulomb force, additionally photons has no rest mass and travel in constant speed of light. The energy of a photon is given in the formula $E = hf$ where f is the frequency of the particle and h is the Planck's constant. There are three main processes where a photon may react with matters, they are:

- Photo electric effects
- Compton scattering
- Pair production

3.4 Radiation Effects on Semiconductor Devices

Semiconductor devices planned to be used in a radiation environment are likely to be effected by the radiation in some way. If not taking properly into account, the radiation effects may damage or even destroy the electronics. Therefore

there is of highest importance to know about how irradiation can affect the semiconductor devices. We normally divide radiation effects in two groups that is *Singel Events effects* and *Accumulative Effects*.

3.4.1 Single Events Effects SEE

Single Event Effects are due to the energy deposited by one single particle in the electronic device. Therefore, they can happen in a moment, and their probability is expressed in terms of cross-section [12]. These effects have been an increasing problem as the manufacture process are getting smaller and smaller, making circuits more weak for radiation. In the next sections we will look into three SEE, which is Single Event Latchup (SEL), Single Event Transient (SET) and Single Event Upset (SEU).

Single Event Latchup SEL

A Single Event Latchup (SEL) is phenomena where a low resistance path between power and ground is formed, normally resulting in burned traces, which means reduced performance or destruction of the chip. Therefore it is of highest importance to know about this effect, to know how to counter or to protect from latches in design phase. In a Complementary Metal Oxide Semiconductor (CMOS) process a SEL can occur when an ionized particle penetrate the silicon in a transistor causing a charge to turn ON the parasitic bipolar transistors formed by the substrate, well, and the diffusion. This will result in a low resistance path between power and ground, and a high current will flow. If a SEL has occurred, power to the chip needs to be turned off immediately, before the high current flowing from power to ground will burn interconnections and permanently set the chip out of function.

How a latchup may occur can be understood by looking at a CMOS inverter, see figure 3.4.1. From figure 3.4.1(a) you can see a resistor formed in the well and substrate, and a parasitic bipolar npn-transistor and pnp-transistor formed inside the inverter. An equivalent circuit can be seen in figure 3.4.1(b). Originally both of the bipolar transistors are turned off, and no current flows through the transistors. A latchup can be triggered if an ionizing particle flows into the substrate creating a transient current that can set V_{sub} high, causing npn-transistor to turn ON. If the npn-transistor turns ON, then current will flow through R_{well} causing V_{well} to go low and setting pnp-transistor ON. When the pnp-transistor turns ON current will flow through R_{sub} , causing V_{sub} to rise, and we have created a positive feedback, causing high current to flow from power to ground.

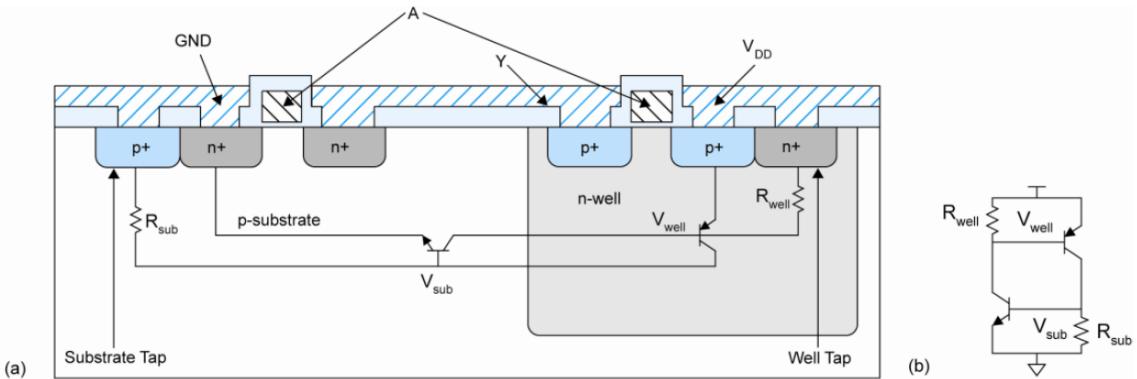


Figure 3.4.1: (a) A CMOS inverter with parasitic bipolar transistors (b) A model of the parasitic circuit

Single Event Transient SET

Single Event Transient (SET) is a transient pulse of current in a logical path of a circuit. A SET is caused by an ionizing particle leaving a transient current close or on a sensitive circuit node. This current can cause a change of value on that node for a short time, and if this value is clocked in on a register, we will have an unwanted change of value and that is called a SEU. If this value is not clocked out or saved in some way, the current peak will just flat out, and nothing will happen. A way to detect SET could be to make a shift register made up of a known number of register and a known input data. By checking the output and compare with the known value, you can detect if a SET has occurred.

Single Event Upset SEU

Single Event Upset (SEU) is change of state in a logical element, caused by radiation. This phenomenon can often be seen in memory cells or registers, where data is stored. A SEU is a "Soft error", which means that it is a non-destructive type of error. By resetting or overwriting after an SEU has occurred, the error will disappear.

For better understanding of SEU we can look at a six transistor SRAM cell, see figure 3.4.2. If we say that $Q = '0'$ and $Q_b = '1'$, so there is a value '0' written to the cell. Then a high energetic neutron strikes into the drain of transistor D_2 and hits a silicon atom. This cause shattering of the atom into charged fragments (ions) that travel through the substrate. These ions leaves a trail of electron-hole pairs, see figure 3.4.3(a). When the resultant ionization track traverses or comes close to the depletion region, carriers (electrons) are rapidly collected by the electric field creating a large current transient (SET) at that node, causing voltage drop at the node Q_b . If this voltage drop is high enough, transistor P1 will be opened up, and transistor D1 will be closed, causing Q to go towards '1' which again causing P2 to

close and D2 to open up causes Q_b to be discharged through D2, and set to '0'. Then the SRAM cell has changed value from '0' to '1', and we have a SEU.

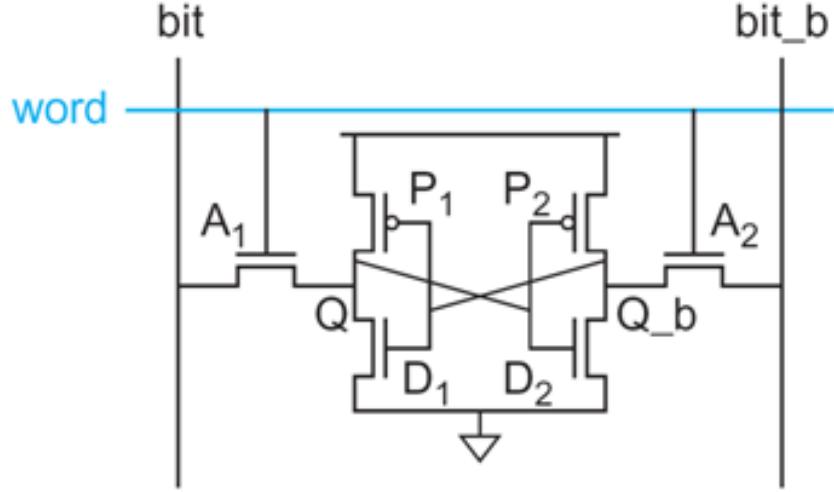


Figure 3.4.2: Six transistor SRAM Cell



Figure 3.4.3: (a) Electron hole pairs generated (b) Carrier are drawn towards the depletion region causing a current jump (c) Additional charge is collected on a more long time scale (hundreds of nanoseconds) [10]

3.4.2 Accumulative Effects

Accumulative effects are energy deposition caused by radiation for the whole lifespan of a circuit [12] and [13]. Accumulative effects are measured by the functionality of a device, and power consumption. Some circuits are weak for accumulative effects, and will stop working only after a small dose of radiation, but others device may not even have any effect after a severe dose of radiation. When a chip stops working, we say that it has reached its tolerance level. When we talk about accumulative effects we normally divide into two groups, which are displacement damage, which is a non-ionizing effect, and Total Ionizing Dose (TID) which is an ionizing effect.

Total Ionization Dose TID

Total Ionizing Dose (TID) is measurement of the dose, which is the energy deposited in a circuit by radiation in the form of ionization energy. The unit used are Gray (Gy) or rad. The relation between those two can be seen in equation 3.4.

$$1\text{Gy} = 100\text{rad} \quad (3.4)$$

The heart of TID effects is the energy deposition in the silicon dioxide. When ionizing particles penetrates into a transistor, electron-hole pairs will be created. Most of the pairs will recombine shortly after they are generated, but some do not completely recombine because of the electric field. Electrons, with high mobility, can easily leave the oxide, but holes have lower mobility and can be trapped in their point of generation in the oxide. The trapped holes cause a negative threshold voltage shift in the MOS transistor, and if enough holes are trapped, it can result in a transistor which is permanently ON. This phenomenon can be seen in figure 3.4.4.

An effect of the total ionized dose in a CMOS circuits, could be increase in current. This could be due to threshold change in the transistors. We can look at an example with an inverter. An inverter consist of only a PMOS and a NMOS, if threshold decreases, time where both transistors are on will increase, leading to increase of current. Another reason for current increase is current leakage between drain and source because of the trapped holes.

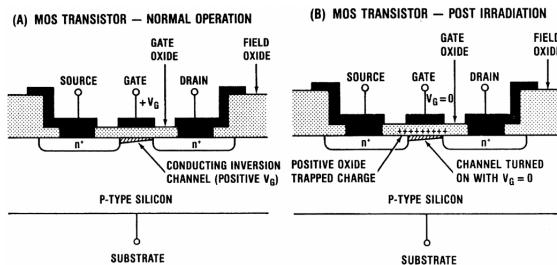


Figure 3.4.4: Layout of a MOS transistor. (A) Shows normal operation and (B) shows the transistor after irradiation.

Displacement Damage

Displacement Damage is a non-ionizing effect mostly induced by low energetic particles colliding with and breaking atoms out of the initial lattice structure of a material. This can affect the functionality of the device. CMOS circuits are normally considered immune to this effect. Displacement damage is not measured in any unit, but it is expressed in terms of the particle fluence, in particles/cm².

3.4.3 The TPC Radiation Environment

The radiation in the LHC is dominated by high energetic neutrons and protons, mostly neutrons with an estimated fluence of $(0, 6 - 1, 1) \times 10^{11}$ *neutrons/cm²*. Therefore it would be preferable to test our electronics with a neutron beam, but since there are few labs that can produce a neutron beam compared to proton beam most of the electronics is only tested at OCL with a proton beam. There has been done experiment that compares SEU induced by neutrons and protons [14], and the result shows that it is possible to use a proton beam instead of proton beam with small deviations. By comparing a Proton beam with a neutron beam of 21MeV we see that we get 10-25% less SEU cross section for a proton beam compared to a neutron beam. If we increase the energy to 88MeV then we get close to none deviations.

The dose that we could expect for a 10 year period in the ALICE detector is estimated to be approximately 0.6 kRad from Pb-Pb collisions that will be run 1 month a year and a little higher for p-p collisions that will be run 10 months a year [15] and [5]. Therefore we could expect a dose of 1-2 kRad during the time it will be used at CERN.

Chapter 4

Preparations for Radiation Testing

Testing Integrated Circuits (ICs) is a process that has been done many times before, in conjunction with design of electronics that are going to be installed in the LHC at CERN. This chapter will go through all the components that are going to be tested, and explain how to test. Much of the work presented in this thesis is based on experience from previous thesis [16] [5] [17] [18].

4.1 Test Methodology

The IC that was tested through this thesis are: TPS51200, MIC69302WU, SN74AVCB164245, SN74AVC2T245, QS3VH257, SY89831, ADN2814, MAX3748, INA210, TLV3011 and SF2 M2S050-FG896. What each of these are, and how these was tested will be discussed in the following sections.

For each of the different IC, except SF2, a simple Printed Circuit Board (PCB) was made as a platform to be able to send in input data and measure the output data. One or two connectors was placed on the different PCBs and connected to USB-DAQ (Data Acquisition) boards from National Instruments. These gave us the possibility to control the inputs of each IC and monitor the outputs. A small resistor was placed in series with the power input. By measuring voltage drop over this resistor we could calculate the current using *Ohms law* ($I = U/R$).

We wanted to have at least two PCB for each of the IC that were going to be tested, to have more test data on each IC, and as a precaution if we should have problems with one of these.

There may be some difference between two boards made for the same chip, which

is because the first board that was made may have some fix on the PCB level to make it work. When the second board was made, errors were fixed in the design before a new board was made. The second version was tested first, in case we didn't have time to test both of the versions. Later in this thesis the second boards that were made are marked with $_1$ and the first boards were marked with $_2$. Two of the ICs (ADN2814 and MAX3748) were only made one version of, since we didn't have any spare IC at that time to make a new PCB. All of the test PCBs had a mark on the back indicating the center of the IC, which was used to pinpoint the center during the tests.

To supply and measure everything on the test boards, Data Acquisition (DAQ) devices from National Instruments were used. The DAQ devices we used are called USB-6009, USB-6008 and USB-6501. USB-6009 was used as the main one, and the other were used when needed more digital or analog inputs or outputs. USB-6009 has 8 single-ended analog input (AI) channels, 2 analog output (AO) channels and 12 digital input/output (DIO) channels, and also a 2.5 V reference and 5.0 V output. The analog outputs have a limit of 5 mA, but some of the ICs that were tested required more power. In these cases the 5 V output, which are able to deliver current up to 200 mA, and a voltage regulator to 3.3 V were used, see section 4.2.2. More information on the DAQs can be seen in the reference [19].

4.2 The Tested Components

4.2.1 TPS51200

This is an adjustable power regulator from Texas Instruments. It is special designed for DDR RAM, it can be used for DDR, DDR2, DDR3 and DDR4 applications. On the RCU2 this is going to be used to supply a DDR3 RAM with 0.75 V.

In figure 4.2.1 you can see the schematic layout of the PCB for TPS51200. The PCB was designed after a recommended setup for DDR3 application from the datasheet [20]. Input voltage was set to 3.3 V. Voltage over resistor R1 (See figure 4.2.1) was measured and used to calculate current consumption. Output voltage was also monitored.

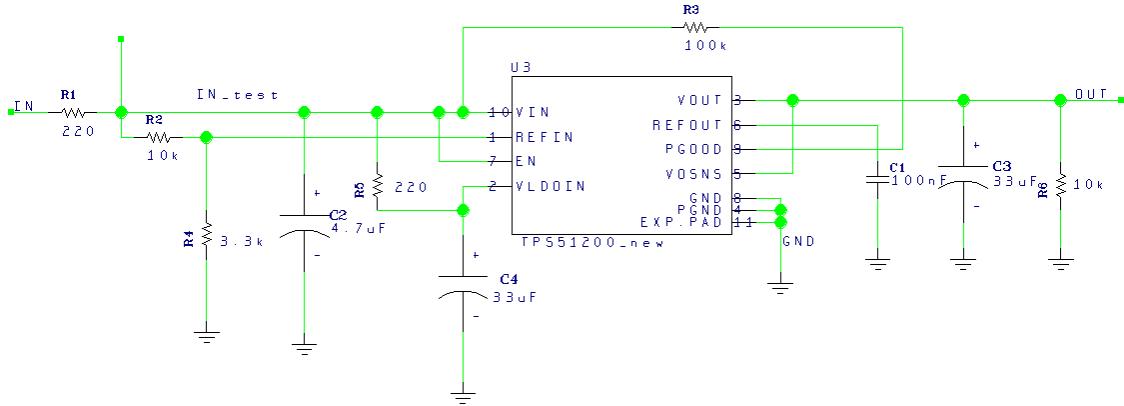


Figure 4.2.1: Schematic for the TPS51200 test board

4.2.2 MIC69302WU

This is an ultra-low dropout¹ adjustable power regulator from Micrel Incorporation. It is in a family of high current, low voltage regulators, and can deliver a current of up to 3 A. On the RCU2 this is going to be used to regulate the 3.3 V power signal down to 1.2 V power signal. The 1.2 V power signal is mainly used to power the main FPGA, the SF2, on the RCU2.

With adjustable regulator it means that by changing R1 and R2(see figure 4.2.2) you can adjust the output voltage, see equation 4.1. For the two test boards that were made we used an input voltage of 3.3 V. Voltage over resistor R3(See figure 4.2.2) was measured and used to calculate current consumption. Output voltage was also monitored. We used 10 kΩ for both R1 and R2 which gave us 1 V on the output.

A third PCB was made with this IC, which was used to supply 3.3 V to the components which requires more than 5 mA, which is the maximum the analog outputs the USB-DAQ can deliver. A version was design with resistor values of R3 = 20 Ω, R1 = 5.6k Ω and R2 = 1k Ω, which gives us 3.3 V output. This PCB was used to supply SY89831U, ADN2814 and MAX3748

$$V_{out} = 0.5 \times \left(\frac{R1}{R2} + 1 \right) \quad (4.1)$$

¹Low dropout means that voltage on the output can be close up to the input. For MIC69302WU low dropout means that $V_{IN} - V_{OUT}$ can be as low as 500 mV

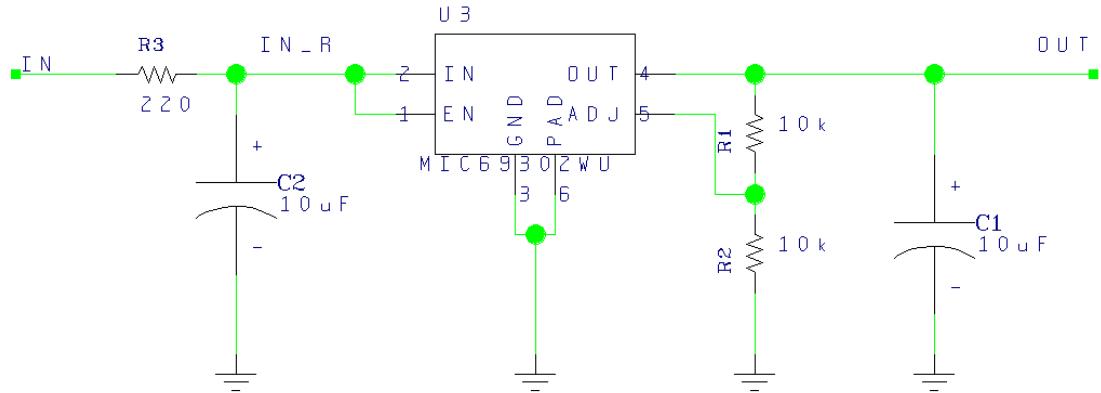


Figure 4.2.2: Schematic for the MIC69302WU test board

4.2.3 SN74AVCB164245

This is a 16-bit noninverting bus transceiver, with configurable voltage. Used for level shifting on digital signals. An application example could be to convert a 16-bit digital signal of 1.5 V to a 16-bit signal of 3.3 V. Direction of the signal is decided by DIR1 and DIR2. The input and output high value can be set to anything between 1.4 and 3.6 V, the low value is set to be 0 V.

For the two test boards that were made, the supply voltages(VCCA and VCCB, see figure 4.2.3) was both set to 3.3 V to make it more simple to test. Voltage over resistor R1 (See figure 4.2.3) was measured and used to calculate current consumption. To make sure that the circuit didn't used unmeasured current through the inputs of the chip we used a pMOS transistor that was connected as seen in figure 4.2.3. This made the current into the inputs come from the supply pin and not from the digital signal IN. The outputs were measured digitally.

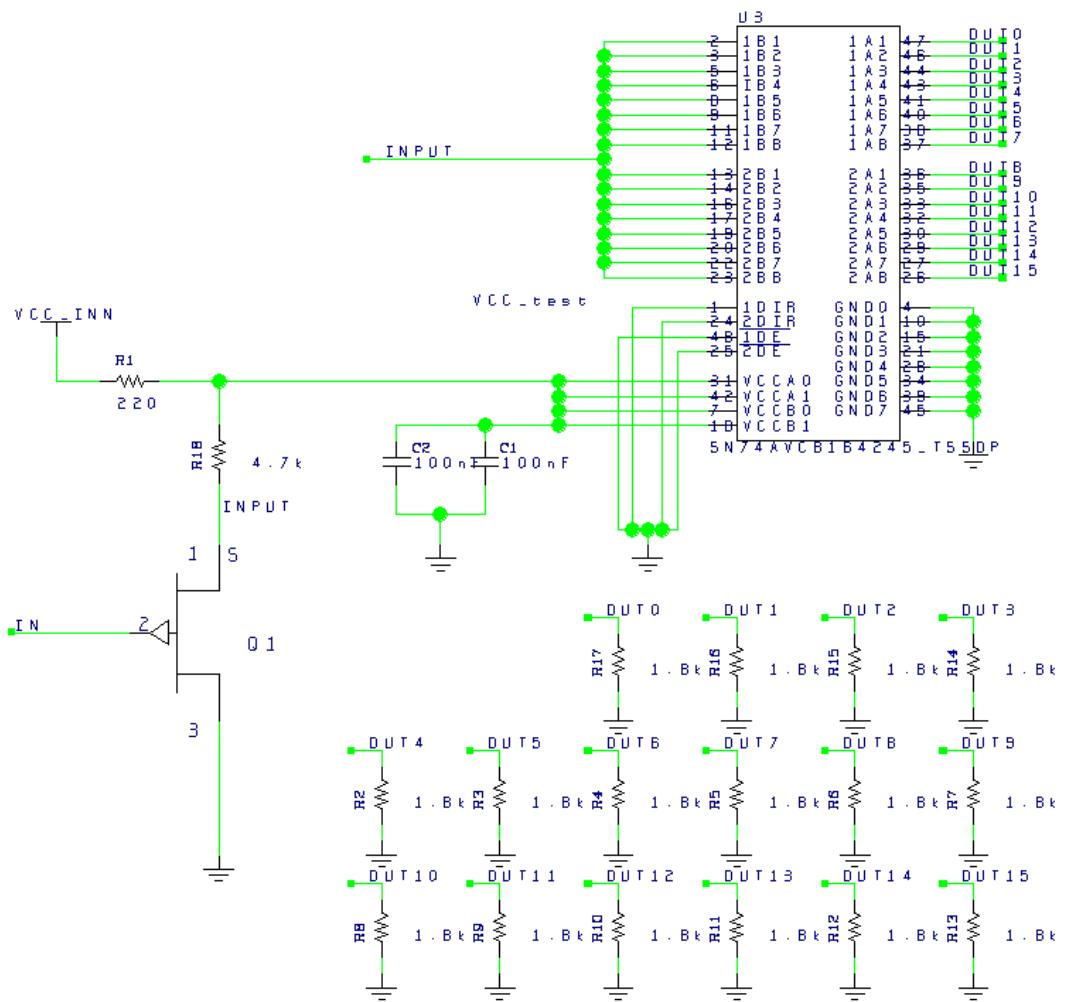


Figure 4.2.3: Schematic for the SN74AVCB164245 test board

4.2.4 SN74AVC2T245

This is a dual-bit noninverting bus transceiver, with configurable voltage. It has the same function as SN74AVCB164245, but this only has two inputs. The input and output high value can be set to anything between 1.4 and 3.6 V, the low value is set to be 0 V. Direction of the signal is decided by DIR1 and DIR2

As for SN74AVCB164245 a 3.3 V supply was used for both VCCA and VCCB, see figure 4.2.4. Voltage over resistor R1(See figure 4.2.4) was measured and used to calculate current consumption. The output signals were measured digitally.

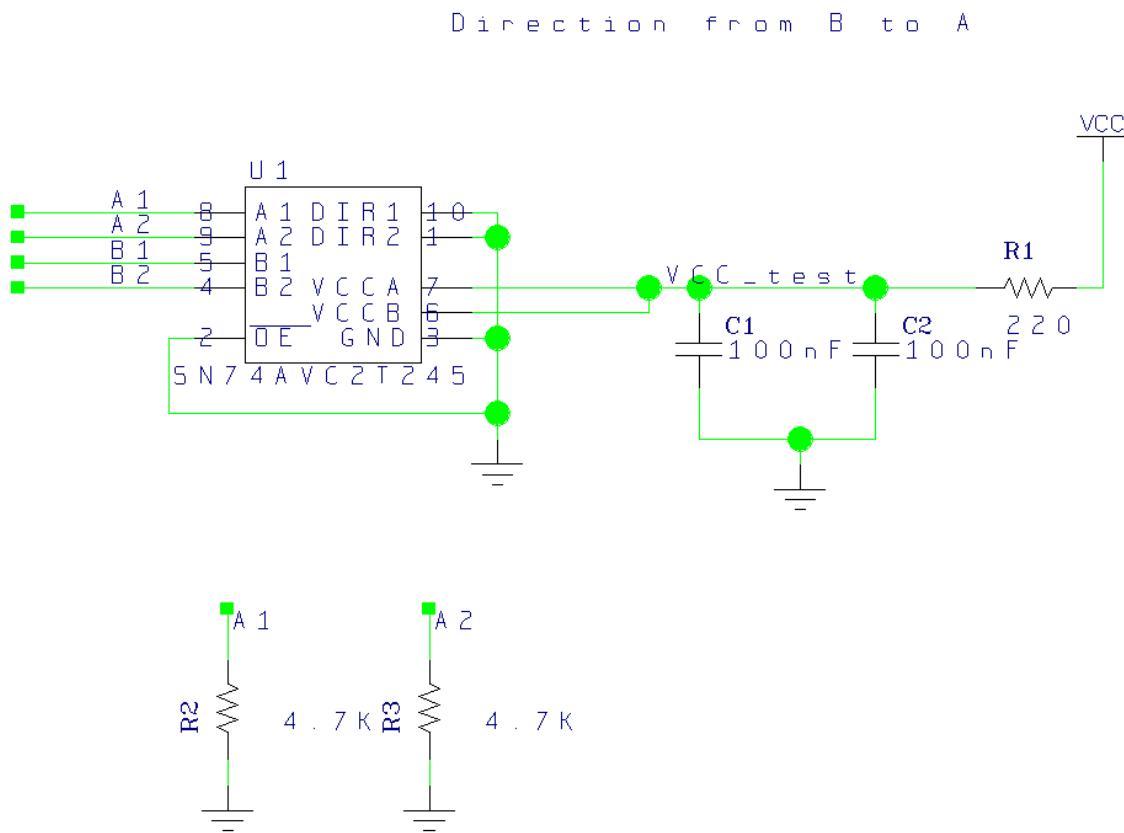


Figure 4.2.4: Schematic for the SN74AVC2T245 test board

4.2.5 QS3VH257

This IC consist of four 2 to 1 multiplexer/demultiplexer. It has high bandwidth, up to 500 MHz, low ON resistance and high OFF resistance.

For our test board, the supply voltage was set to 3.3 V. Voltage over resistor R1 (see figure 4.2.4) was measured and used to calculate current consumption. For the

Select input an analog output signal was used. The input signals were set by digital outputs from the USB-DAQ, and the outputs were measured digitally.

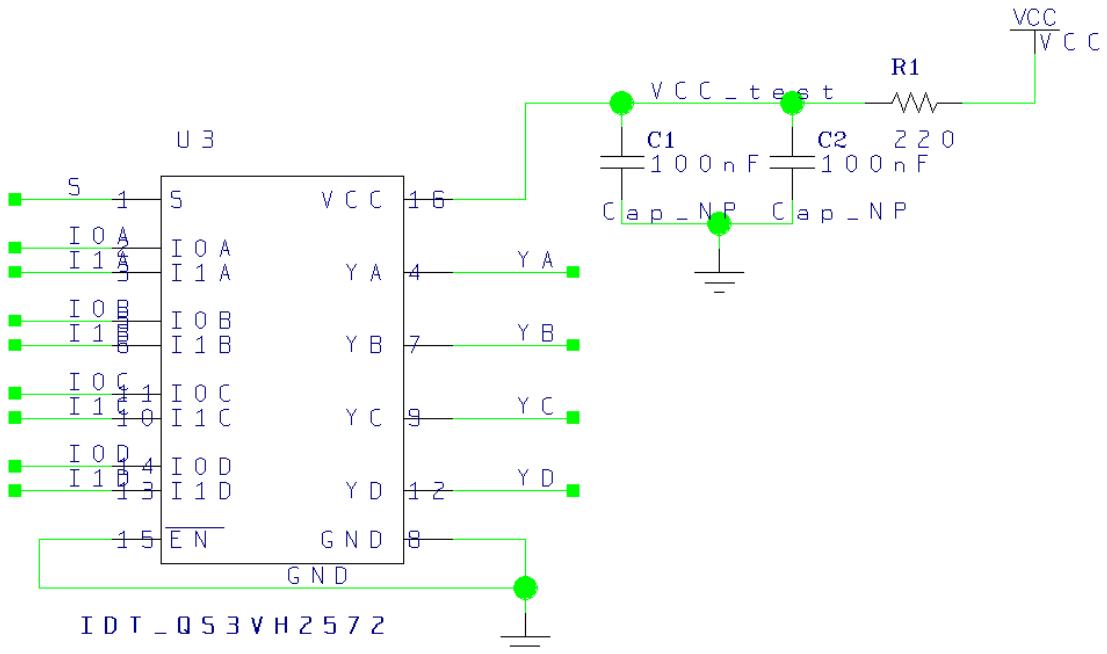


Figure 4.2.5: Schematic for the QS3VH257 test board

4.2.6 SY89831U

This is a high speed, 2GHz differential LVPECL² (Low Voltage Positive Emitter Coupled Logic) 1 to 4 fan-out buffer optimized for ultra-low skew applications.

The input signal to this IC is differential. The USB-DAQ device we were using doesn't have a differential output signal, so here we had to use a little fix to make it work. We used two single-ended output signals that were set to the opposite of the other, and every 100 ms the values switch, so that when IN+ was 3.3 V IN- was 0 V, and when IN+ was 0 V IN- was 3.3 V. The outputs were measured by the analog inputs of DAQ USB-6501.

This IC requires a large current typically around 60 mA, and we could therefore not use the analog outputs. W used the modified PCB version of the MIC69302WU, that will supply us with a 3.3 V signal up to a current of 200 mA. Current consumption was measured over the input resistor of the MIC69302WU PCB.

²LVPECL are differential signaling systems, and are mainly used in high speed and clock distribution circuits, the input/output voltages have a small swing (0.8 V), the input impedance is high and the output resistance is low; as a result, the transistors change states quickly, gate delays are low, and the fan-out capability is high.

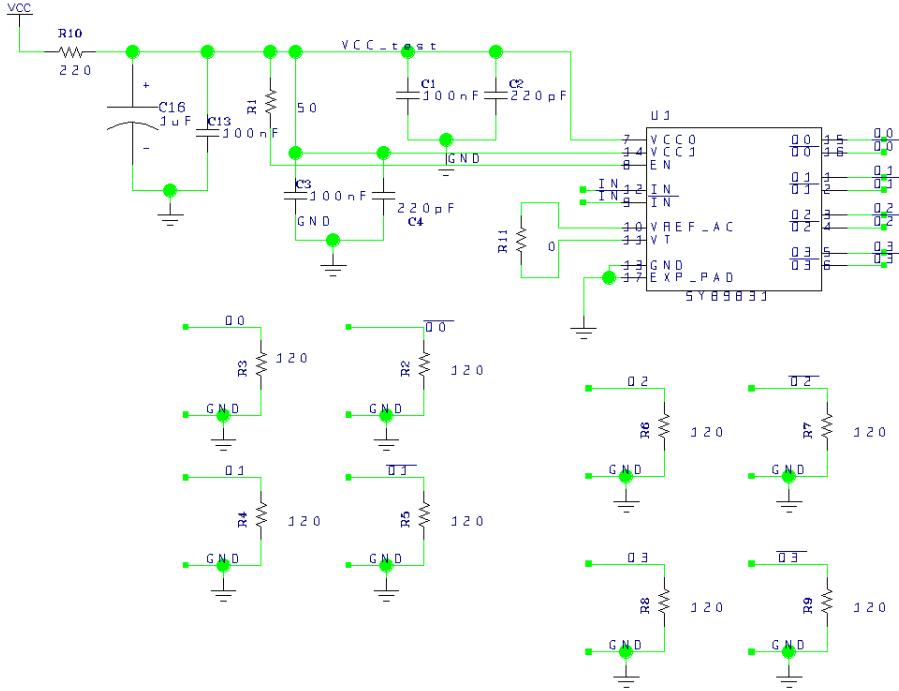


Figure 4.2.6: Schematic for the SY89831U test board

4.2.7 ADN2814 and MAX3748

These two boards are used for the same purpose, the one of these that performs best will be chosen to be used on the RCU2. ADN2814 is a clock and data recovery IC with integrated limiting amplifier. It works in rates of 10 Mb/s to 675 Mb/s, and gives output data in Low-Voltage Differential Signaling (LVDS) format. MAX3748 is a limiting amplifier. It works in rate of 155 Mb/s to 4.25 Gb/s, and gives the output data in Current-Mode Logic (CML) format.

On the RCU2, these boards are supposed to be used to make a stable signal out of a not so stable signal coming from an optical receiver. The signal which is sent into the receiver is a Manchester-decoded signal consisting of clock and data. The clock signal is going to be used as a global clock signal for all of the RCU2s, so that all of the RCU2s are synchronized. The data signal is a trigger signal which in short tells the RCU2 when it is going to do a measurement and when to send data out.

There are a few differences between the two ICs. MAX3748 comes in a smaller package and uses less power and works in higher rates, but it doesn't have a clock and data recovery function as ADN2814 has. For MAX3748, we will need to do the clock and data recovery function in the main SF2 FPGA, using some of the FPGA logic. The clock and data recovery function in ADN2814, is actually clock recovery and data re-timing, that means that the output data is actually the same as input data, except that it is limited. This means that we have to use FPGA logic to recover data, but since we have the clock signal, it is easier to decode and extract

the data signal.

To be able to make a good test for these two, we used a SF2 starter-kit. The SF2 FPGA on the starter-kit was used to decode a clock and data signal into a differential Manchester signal that was transmitted to the two circuits. The Manchester signal was used as an input for the two components. The differential Manchester signal was sent into the two test boards with wires, and a limited amplified version of the Manchester signal was sent back to the SF2, for ADN2814, we had a clock signal as well. The Manchester signal coming back had to be decoded back to clock and data, which was done in the SF2 FPGA. To be able to check if the returning data is equal the original, the original data signal had to be delayed in the FPGA, since sending data out through a IC and back contribute to some delay. The original data was delayed by sending it through a few D-latches, until the two data signals had the same phase. Then we could start comparing, this were done through a XOR-function, triggered by an 80 MHz clock. Every time the XOR function goes high, that is when the compared data is not equal, a counter will be incremented.

The recovered clock from the ADN chip is 160 MHz, which is a fairly high frequency. To be able to compare two clocks of 160 MHz, we introduced a third clock signal of 160 MHz, with a phase shift of 90 ° from the two others. This clock signal was used to trigger a XOR-function checking the two clock signals. If they are unequal a counter will be incremented.

The error counter values were accessed by the internal microcontroller on the SF2 chip. From the microcontroller the counter values were constantly transmitted out through a UART-port, which is connected to the USB-plug on the kit. The USB-plug is connected to a computer where a labVIEW program was running ready to receive data. The received data is exhibited for a viewer, and data is saved in a text file. The labVIEW program also monitors the current consumption of the IC.

Both of these components required allot of current to function correctly, so the modified MIC69302WU in combination with the 5 V on the USB-DAQ was used. This gave us a supply voltage of 3.3 V and a current limit of 200 mA.

The decoding process of the Manchester signal returned both clock and data, but since these are related, only data was checked.

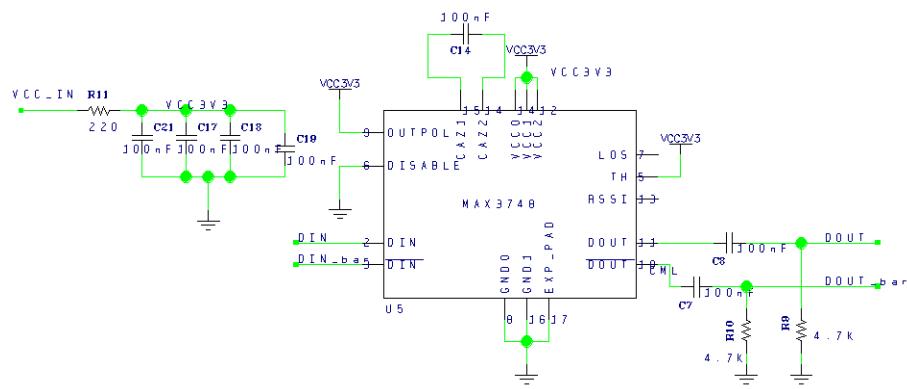


Figure 4.2.7: Schematic for the MAX3748 test board

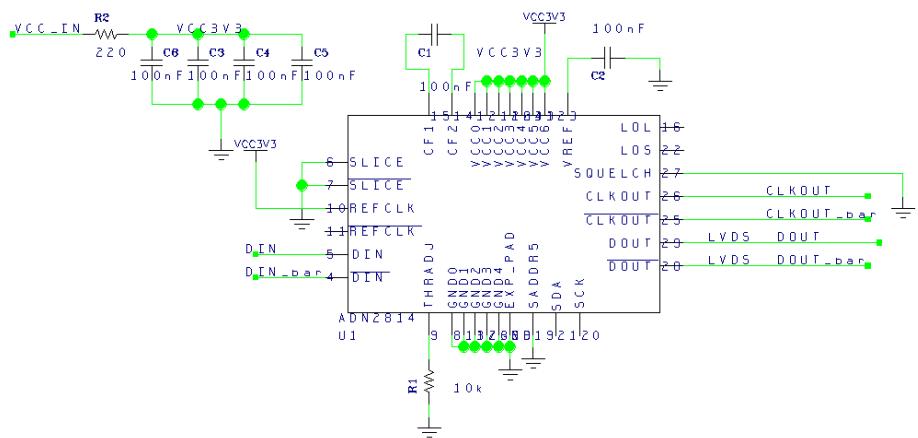


Figure 4.2.8: Schematic for the ADN2814 test board

4.2.8 INA210

INA210 is a so called Current-Shunt Monitor, which is a IC that is used to amplify small current signal into higher voltage signal. This is done by sending the signal that you want to measure current of, over a small resistor, typical smaller than 1 Ohm. Then the voltage formed over this resistor will be amplified through the IC. This IC comes in a family of 5, with different amplifications, the one we are using has an amplification of 200 V/V.

To be able to test this board, we had to have something that could use current. We added a diode and a resistor, so that we could get a small current signal over the shunt resistor R1, resulting in a small voltage, which will be amplified. If everything works as it should the output signal should stay stable at a voltage.

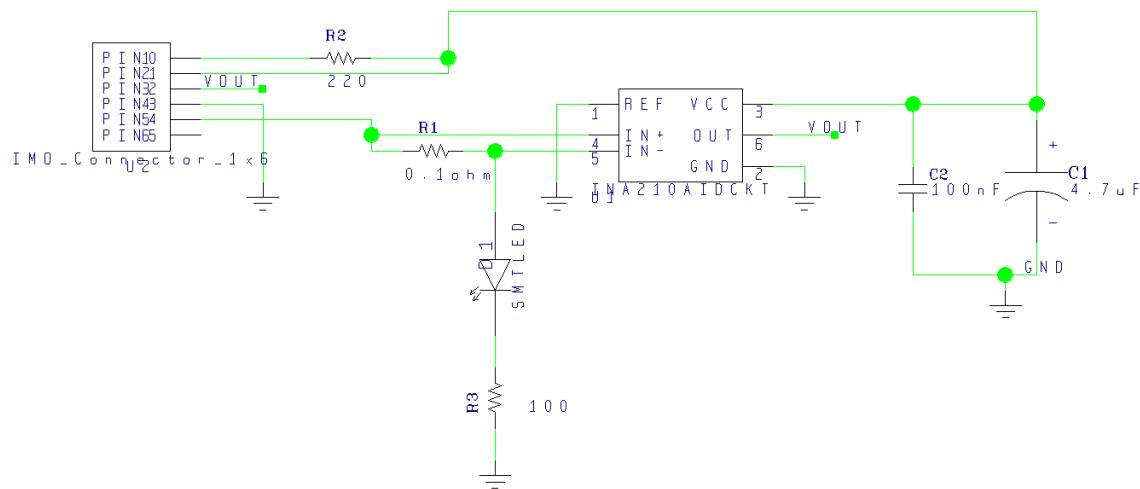


Figure 4.2.9: Schematic for the INA210 test board

4.2.9 TLV3011

This is a comparator with a built in voltage reference of 1.242 V. It supports low supply voltage from 1.8 V to 5.5 V, and has an open-drain output with fast response time. A 10 kOhm resistor is needed as a pull-up on the output.

To test this board, we used an analog input changing back and forth every other second from 2 to 3. Since there is a voltage divide on the input, see schematic in figure 4.2.10, the input to the IC will go from 1.0 V to 1.5 V, the compared value is the internal voltage reference on 1.242 V, which means that if everything works, the output should go back and forth from high to low every other seconds.

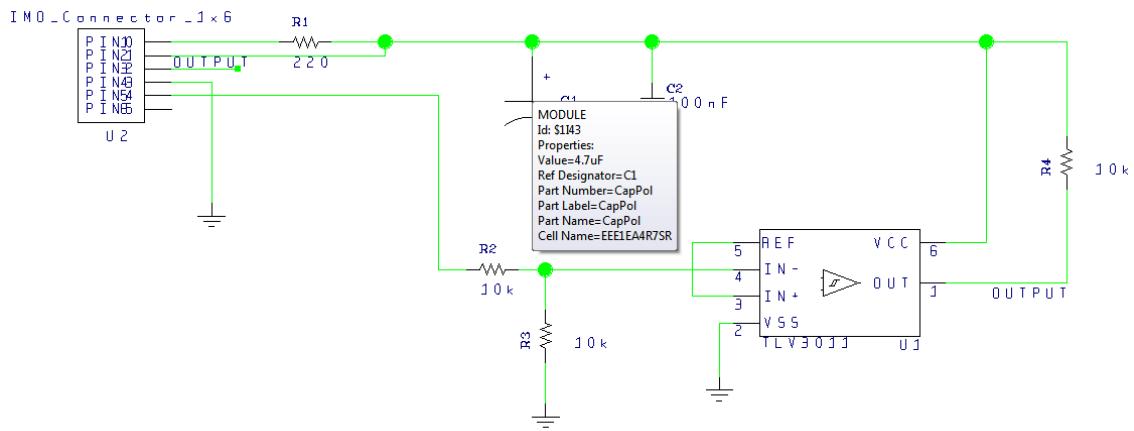


Figure 4.2.10: Schematic for the TLV3011 test board

4.2.10 All of the Test Boards

In figure 4.2.11, 4.2.12 and 4.2.13 you find pictures of all of the different PCB boards.

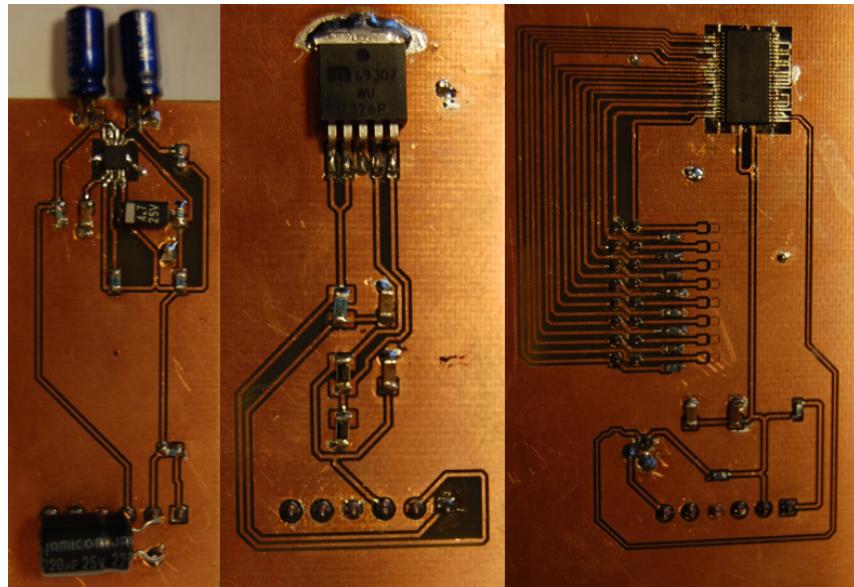


Figure 4.2.11: Picture of PCB boards, from left we have, TPS51200, MIC69302WU and SN74AVCB164245

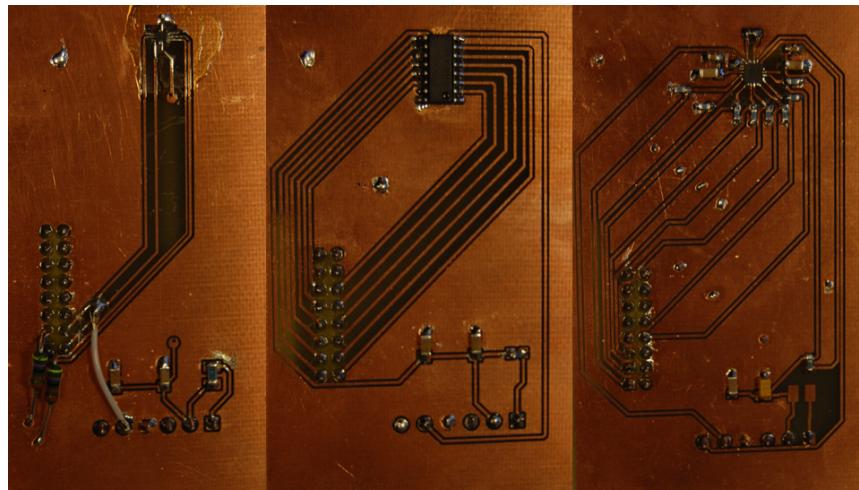


Figure 4.2.12: Picture of PCB boards, from left we have, SN74AVC2T245, QS3VH257 and SY89831U

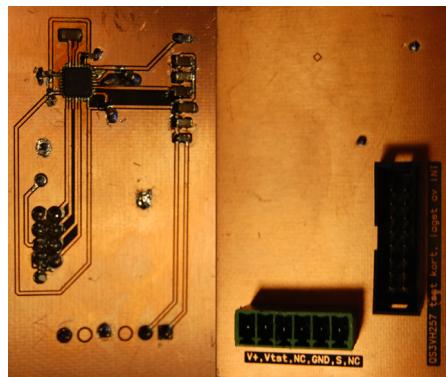


Figure 4.2.13: Picture of PCB boards, from left we have, ADN2814, MAX3748 and back-side of QS3VH257, you can see the mark at the top indicating the center of the IC

4.3 Software

For each of the different ICs that was mentioned in the subsections above, a simple labVIEW program was made specially designed to supply and monitor a specific IC under radiation. In these programs, time from start, current consumption and the status of the output signal (or the output voltage for the regulators) can be measured and monitored. Data is constantly saved in a text file on disk.

In figure 4.3.1 you can see an example of a labVIEW program used for SN74AVC2T245.



Figure 4.3.1: LabVIEW program for SN74AVC2T245

4.4 SmartFusion2

SmartFusion2 (SF2) SoC FPGA integrates a flash-based FPGA, a Microcontroller SubSystem (MSS), which consist of a microcontroller, an ARM Cortex-M3 processor, PLLs, bus communication through APB and AHB bus, communication protocols like Ethernet, UART, SPI and I^2C , and much more. It is also said to have immune configuration memory, as well as several other radiation tolerance measures implemented. We are going to use the package M2S050-FG896, with a FPGA of 56 340 logic elements, 6 PLLs, 1314 kb SRAM, 8 SERDES³ lanes, and 377 user I/O.

³Serilizer/Deserializer (SERDES) convert data between serial data and parallel interfaces in both direction

The SF2 contains allot of functionality, and there is therefore important to make a good test methodology, to be able to check the reliability under radiation. The parts of the SF2 which has been tested through this work are the internal SRAM blocks, the logical element, PLL and Single Event Latchup (SEL). How these test works will be discussed in the following subsections. Other functionality of the SF2 has also been tested, but these tests will not be discussed thoroughly through this thesis.

4.4.1 SRAM test

SRAM cells are as discussed in section 3.4.1, sensitive for radiation. It is important to know how well these work in high radiation areas, so we can know how reliable these are when used. The SRAM blocks on the SF2 are divided up into 72 micro SRAM blocks with a size of 64 x 18 bits, and 69 Large SRAM blocks with a size of 1024 x 18 bits. Both micro SRAM blocks and large SRAM blocks are so called two ports SRAM, which means that we can access two addresses at the same time.

The way the SRAM memory was tested is divided into 3 states in a state machine, which can be seen in block diagram in figure 4.4.1. The first state is a reset state, where all values are set to its nominal value. That means all counter is set to 0, write address is set to 0, read address 1, and write data is set to 1010...1010. Read address is always set be one higher then read address.

The next state is an initial state where all addresses are written to. Write data is switched opposite every address increment, so the written data is switched between 1010...1010 and 0101...0101 every other address. When the last bit is written to, the first bit is read.

The last state is a state where all of the addresses are written, read and compared through an endless loop. The data written to an address is always opposite of the previous value on that address, that is to prevent having stuck bits. The state machine will stay in this state until a reset is pushed or power is shutdown.

The SEU counter value for the micro SRAM and the Large SRAM, as well as number of cycles through all addresses is saved in registers and sent to the Microcontroller SubSystem (MSS). These register is saved with Triple Module Redundancy (TMR), which means that the values are saved in three registers, and the majority of these is used. How the data is monitored and checked is discussed in section 4.4.4.

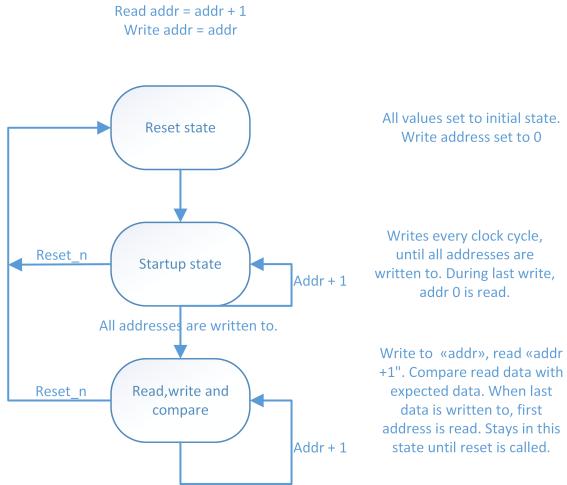


Figure 4.4.1: Flow chart for test procedure of SRAM

4.4.2 Test of the Logical Element

A logical element consist of a 4 input Look-Up Table⁴ and a separate flip-flop which can be used independently from the Look-Up Table. That means that we have 56 340 flip-flops and 56 340 Look-Up Tables available for our design. When a logical element is exposed to radiation, a Single Event Transient (SET) can occur all over the chip. If this happens in the logical element or in the interconnections between logical element, the transient current will normally just be there for a small amount of time, and then it will flat out, causing no error or bit flip in the chip. But if this transient current hits a sensitive node as the input to a flip-flop, or a node that may lead to a change of value at the input, and the input is then clocked out to the output, we would have an unwanted bit change or a so called Single Event Upset (SEU).

The way we tested the logical element is based on [21], which has done a study on how to test FPGAs in a good manner. A good overview of the design can be seen in figure 4.4.2. The idea is to make a long serial chain of flip-flops, otherwise referred to as a shift-register, where a transient can be picked up and make a SEU. By adding an even number of inverters in between each flip-flop we increase the area where a transient can occur, without changing the logic. A known pattern is added to the input of the shift-register, this can be changed depending on how advanced you want to be, but typical pattern could be even other '1' and '0'. To be able to operate at high speed, we are using something called Windowed Shift Register (WSR), which takes out the last n-bit of the shift register, and sends it out in parallel, with a frequency n times lower than the original frequency. To check the outputs for errors, the WSR bits will be sent through the I/O-pins to another SF2 starter kit, hereafter referred to as the monitoring board, where data is checked for

⁴An n-bit Look-Up Table can encode any n-bit Boolean function by modeling such functions as truth tables

errors. To be able to synchronize the two boards, a reset signal and shift enable signal will be sent from the monitoring board to the test board, and a WSR enable signal will be sent from the test board to the monitoring board.

We made generic of all the variables like number of flip-flop in the shift-register chain, number of inverters in between each flip-flop, number of bits taken out in the WSR output and how many shift-register we want to use. Typical value used is respectively 2000, 4, 4 and 4.

We wanted to be able to change the clock frequency without reprogramming the FPGA, to see how the frequency affects the number of upset detected. Clock Conditioning Circuit (CCC) which consist of a PLL, multiplexers and divider circuit, are used to configure clock signals on the SF2. The CCC can be configured through a register, so the frequency can be changed without reprogramming the FPGA.

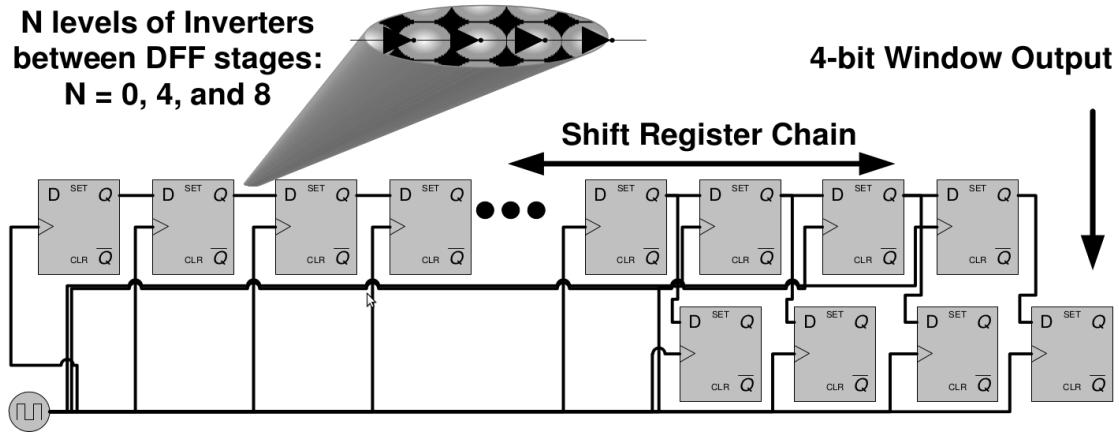


Figure 4.4.2: Flow chart for test procedure of SRAM

4.4.3 Single Event Latchup and PLL

A Single Event Latchup (SEL) is a short circuit between power and ground. If that happens on any spot on the chip, an increase in the supply current can be detected. The way to check for SET, is by constantly checking for increase in current consumption on the chip. Normally the high current will produce so much heat that tracks in the chip will be destroyed, if not countered by shutting power off immediately after the latch has occurred. That is why a separated PCB was made to measure the current, and to be able to shutdown the board if a latch is detected. See section 4.4.4 for more information on that board.

The PLLs on the SF2 has a lock signal which goes high if the PLL is in sync with the input. To check if we have a reliable clock signal, the lock signal was sent to an I/O pin and over to the monitoring board, where the lock signal was constantly checked for a falling edge.

4.4.4 Configuration and Monitoring

To make the test process as easy as possible a SF2 starter-kit was used to implement the tests discussed in the sections above. The starter-kit has serial communication to USB, which makes it possible to easily communicate with the SF2 chip from a computer, six 24-pin headers connected to the SF2 FPGA, which makes it possible to send data in and collect data out from the SF2 chip, and allot of other supporting functions.

All the tests that are mentioned above are implemented into a single project, so that everything was tested at the same time. This reduced test time, and we didn't need to use so many starter-kits.

The test setup consist of communicating with a computer through serial port, a current measurement board, connected with wires to measure current, and another starter-kit (monitoring board) was connected to the GPIO pins to be able to control and check the Logical element design. More detail of the different test programs and boards used to test the SF2 is discussed in the following sections.

Microcontroller SubSystem and labVIEW

To get the counter values and cycle counter data from registers in the FPGA to a computer, the Microcontroller SubSystem (MSS) was used. The MSS uses APB bus to collect the counter values, the microcontroller are sending the counter values through UART, which is connected to a serial to USB converter and further to a USB-plug. By connecting a computer to the USB-plug, we get serial communication to the microcontroller. A C-code was written to the microcontroller, which in short sets up the UART communication and constantly sends SEU counter and cycle counter values through UART and out to a computer, and checks for received data. The received data is used to determine the frequency, of the shift-register design, as described in section 4.4.2. A labVIEW program was written to communicate with the SF2. The labVIEW program is constantly checking for received data, and exhibits the newest received values for a user. Through this program you are also able to select some specific frequencies, by use of push-buttons in the program, by pushing a button a request to change frequency is sent to the microcontroller. When the microcontroller receives the request, it access the register controlling the *Clock Conditioning Circuit*, and changes to the frequency.

Monitoring Board

As said in section 4.4.2 a second starter-kit, called monitoring board, was used to be able to monitor and control the *Logical element test design*. On the monitoring board there is a Linux system running. A VHDL code is built on the FPGA which takes inn WSR data and WSR enable from the test board and sends out reset, shift enable and pattern. All of the output data is controlled and input data is monitored through APB bus to the Linux system. The WSR enable signal tells us when a new data is sent from the test board, when this signal goes high, the WSR data signals is clocked in a register on the monitoring board. The WSR data is then compared with the correct value, and if an error has occurred, a counter will be incremented. The counter value is read in the Linux system. The monitoring board is also used to monitor the PLL lock signal.

Current Measurement Board

To measure the current into the SmartFusion2 starter-kit, a PCB was made with a microcontroller, serial to USB converter (FTDI chip), some debugging LEDs, power switch, and all the necessary electronics to make all this work together. The microcontroller used is a Texas Instruments MSP430AFE253. That is a 16-bit microcontroller with internal 24-bit ADC. It has an internal frequency of up to 12 MHz, and support high frequency crystal up to 16 MHz. Two types of serial communication interface are available, that is USART and SPI. Since the microcontroller only has a 16-bit architecture, only 16-bit of the ADC is accessible at a time. The microcontroller has 3 differential ADC inputs, which means three different currents can be measured. A current is measured by adding a small resistor of known value in series of the signal you want to measure current of, and by measuring voltage over the resistor you can calculate the current, by using ohms law ($I = \frac{U}{R}$)

To measure current for the SF2 starter-kit a small resistor of 0.1 Ohm was placed in series with the 1.2 V supply voltage, and a 0.16 Ohm resistor for the 3.3 V supply voltage. The voltage over these resistors were measured with the ADC, and the ADC data was sent over USART port to the serial to USB converter, and further to a computer. On the computer a labVIEW program was set up to receive data through the serial port, and when data is received, the ADC value and the known resistor values are used to calculate the current. The current value is constantly saved and exposed for a viewer.

The 3.3 V regulator on the SF2 starter-kit has an enable signal, where a pull-up resistor to 5 V is placed, one of the outputs on the microcontroller is connected to this pin. If the current on one of the supply voltages goes over a certain threshold, the bit on the microcontroller is set to go low, resulting in turning the 3.3 V regulator

on the SF2-starter kit off. The 3.3 V is used to power all other regulators, so by turning this regulator off, the whole starter-kit turns off.

Schematic, PCB layout and instructions on how to use this board can be found in appendix

4.5 Equipment Used for Testing

Under a radiation test, some equipment is needed. In the following sections some of the equipment used for radiation test is presented.

4.5.1 SRAM Detector

The SRAM detector boards are made by Arild Velure, as part of his master thesis [18]. It is a SRAM-based radiation detector. Allot of tests has been done on this board, and a cross section (the probability that an incoming particle will induce an SEU) is found empirical to be $1.14 \times 10^{-6} \text{ cm}^2$. By checking SRAM chips for SEU, we can calculate the fluence⁴ of the beam.

The SRAM detector is a PCB with a flash-based FPGA, four 16 Mbit Cypress SRAM chips, connectors and supporting electronics. The board can be connected to a computer through an Opal Kelly XEM3001 board, which converts RS485 signal from the FPGA to USB. A labVIEW program has been built specially for this board. From this program we are able to reset data, do some basic settings, and monitor data. The program also constantly saves data onto the disk. The board also has an optical input for scintillator counts, so we could use this board as a scintillator counter as well.

In figure 4.5.1 you can see how the labVIEW program looked like. From here we can monitor SEU on all the 4 SRAM chips, see scintillator counts, reset counters, see time from start as well as other things. SRAM1-10 as you can see on the left side, is different SRAM-board, the board we used was SRAM6.

The approach for detecting a Single Event Upset (SEU) on the SRAM is rather straight forward, as can be seen in the flow diagram of figure 4.5.2. There is an initial startup phase where a known pattern is written to all the addresses in the SRAM. When the startup phase is done, the value from the first address is read and compared with the correct value, and if one or more of the bits are not equal

⁴Fluence is the total number of particles that intersect a unit area in a specific time interval of interest, and has units of *particle/cm²* (number of particles per meter squared)

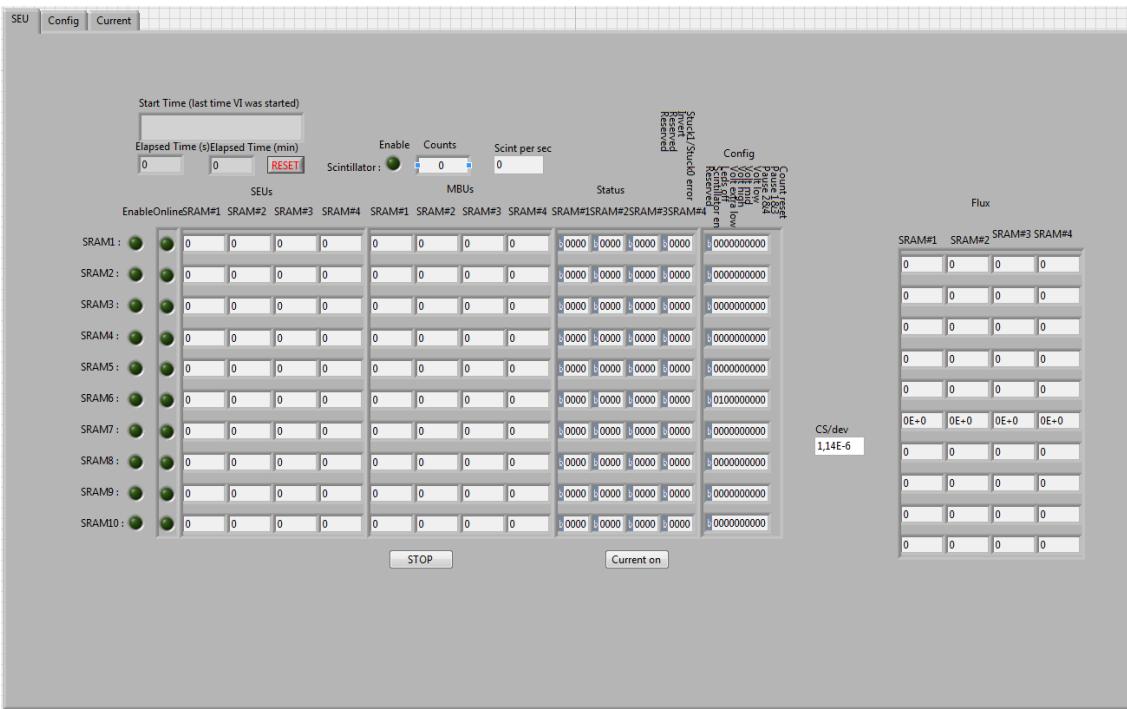


Figure 4.5.1: LabVIEW program for the SRAM

a SEU has occurred, and a counter will be incremented for each bit at the address which has suffered an upset. After the read, a new value is then written back to the address and the system moves on to the next address. A checkerboard pattern of alternating ones and zeroes, is used when writing to the SRAM. To check for stuck bits, the bit pattern is inverted for every cycle through all addresses.

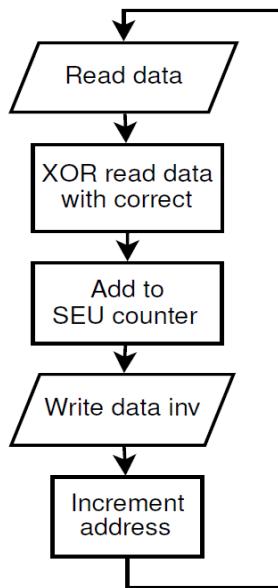


Figure 4.5.2: Flowchart for SEU detection

The SRAM detector also has an edge detector, which are able to detect rising

edges of a signal. This is used as a scintillator counter.

4.5.2 Scintillator Counter

A scintillator is a material that emits light when exposed to ionizing radiation [7]. A scintillator can be used as a standalone equipment, but then only to detect that there are radiation, by seeing that it lights up. To get a more accurate measurement, we will need a PhotoMultiplier Tube (PM-tube), which has the ability to converts light pulses to current pulses by an electron avalanche process. The current pulses can be detected by an edge counter, which count every falling or rising edge of a signal.

4.5.3 X-Y-positioning System

The X-Y-positioning system is a displacement system where things (for example a PCB) can be mounted and be moved up, down and sideways in a small area controlled by a computer. Communication is done through a serial port and a labVIEW program is used to control the system.

This was used when doing the beam profile as discussed in chapter 5.1.3. In figure 4.5.3 you can see a picture of the front and back of the X-Y-positioning system, with the SRAM detector mounted.

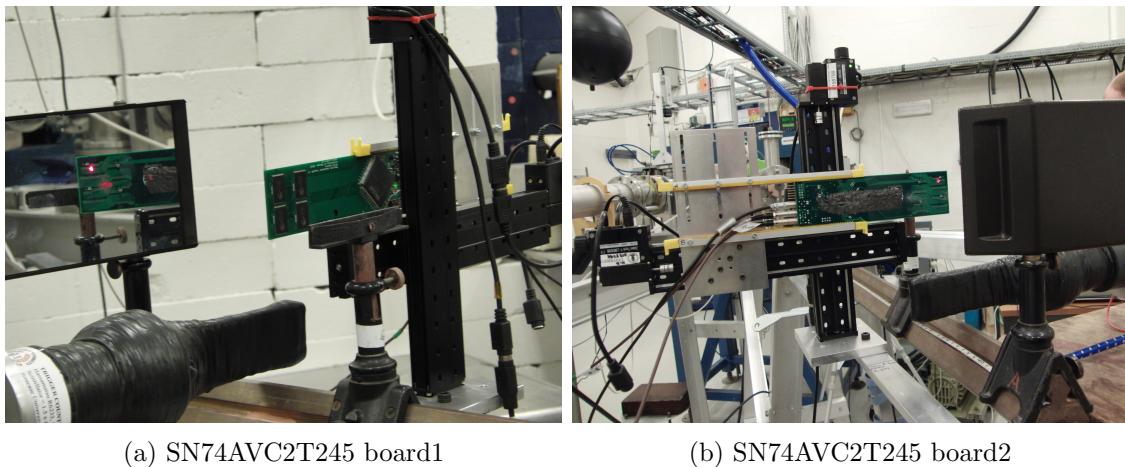


Figure 4.5.3: X-Y-positioning system upfront and behind, with SRAM-board mounted

Chapter 5

Irradiation Test Setup

Irradiation tests for the RCU2 electronics which was discussed in the previous chapter, was executed at two facilities, these are Oslo Cyclotron Laboratory (OCL) and The Svedberg Laboratory (TSL). This chapter will give a brief introduction to the two facilities, and explain how the preparation process was for each of the two facilities.

Purpose of Tests

The purpose of testing the RCU2 electronics for radiation is to see if the tested IC are able to survive in a radiation hard environment as we will find in the TPC, see section 1.1. To test the limit for each of the ICs, the ICs was irradiated until an error was detected, current consumption drastically increased or the IC received a much higher dose than was required without any error.

5.1 Irradiation on OCL

5.1.1 About OCL

Oslo Cyclotron Laboratory is located at the Department of physics at the University of Oslo, and was opened in 1978. The cyclotron is of the type MC-35 and was made by Scanditronix AB from Sweden. This is the only accelerator in Norway for ionized particles used in basic research. The cyclotron can accelerate protons, deuteron, 3He and 4He , with energies and intensities as seen in the table 5.1 below. A drawing of the lab can be seen in figure 5.1.1. The laboratory is divided in tree; the control

room, the inner experimental hall and the outer experimental hall. The cyclotron is placed in the inner hall, and a beam is sent through pipes to the outer hall. Inside the cyclotron and the pipes there is vacuum, so that the particle should not suffer energy loss from collision with air molecules. With magnet you are able to regulate the beam to your desired pipe exit. There are also several cups put on the pipeline which makes it possible to block the beam. These can be used to stop the beam during an experiment, so you are able to go into the experimental area and do changes on your setup. When the cyclotron is running and the beam is on, you are not allowed to enter the inner experimental area.

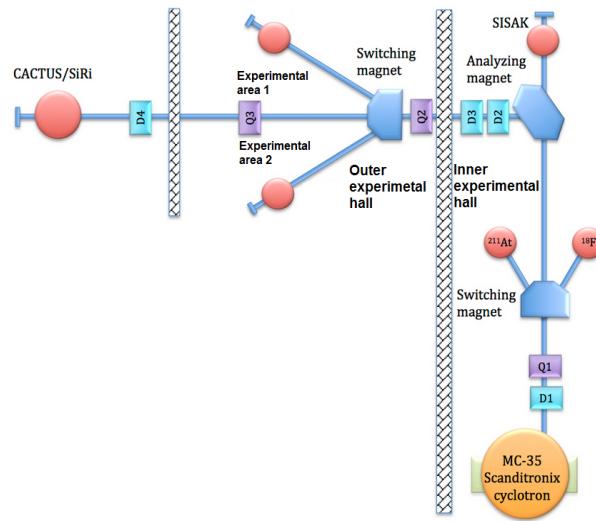


Figure 5.1.1: Out-lay of the OCL

Ionized beam particle type	Energy(MeV)	Intensity(μ A)
Proton	2-35	100
Deuteron	4-18	100
3He	6-47	50
4He	8-35	50

Table 5.1: Ionized beam particle data table

5.1.2 Experiment Setup and Equipment

The experiment setup was placed in the outer experimental hall in experimental area 2. The experimental setup as well as the equipment used can be found in the figure and table below. The equipment was kept in close to the same height around 140-150cm. Beam exit was in a height of 141.5cm.

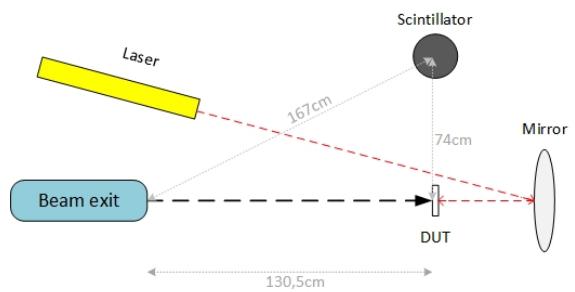


Figure 5.1.2: Experimental setup seen from above

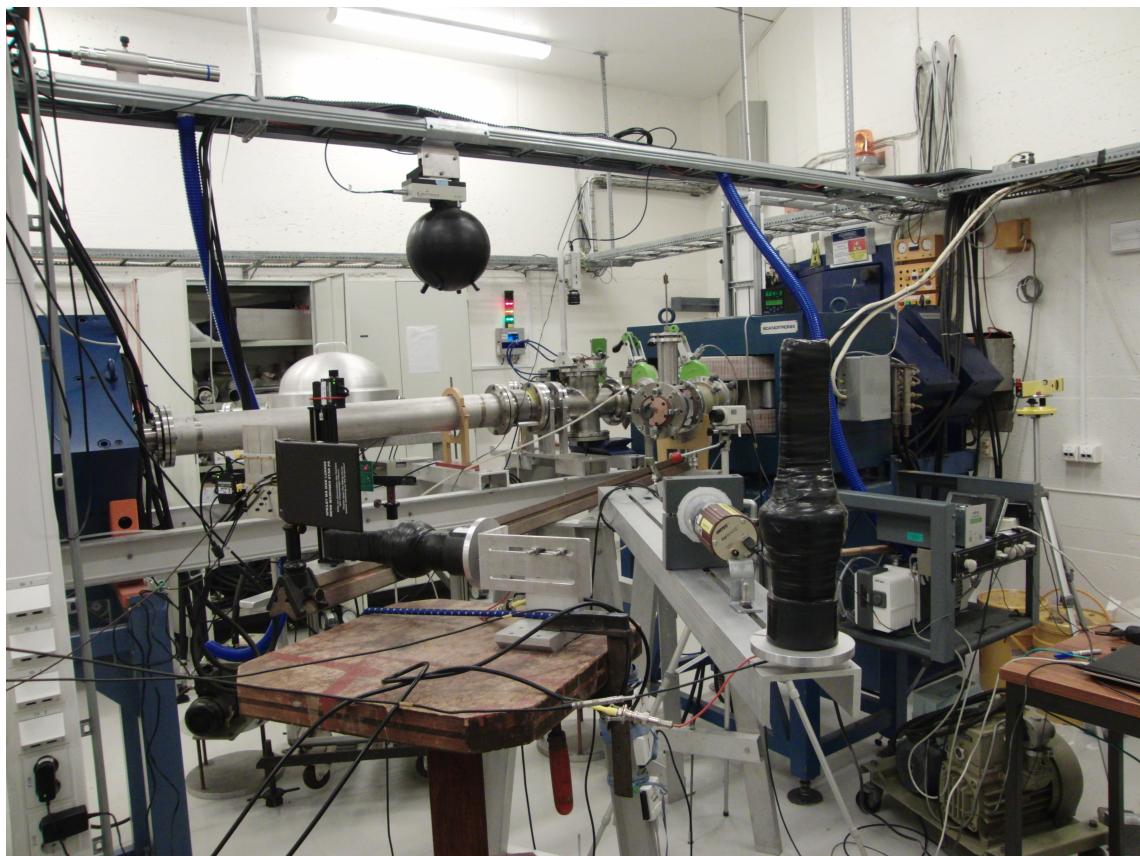


Figure 5.1.3: Picture of the experimental area

Equipment	Explanation
Scintillator	A plastic scintillator with photomultiplier. Was used to measure relative radiation. We had two of these, one that was placed right under Device Under Test (DUT) and one that was placed 75cm away from DUT.
High voltage regulator	Voltage for the photomultiplier. 800V was used.
The test boards	TPS51200, MIC69302WU, SN74AVCB164245, SN74AVC2T245, QS3VH257, SY89831U, ADN2814, MAX3748, INA210, TLV3011 and SF2 starter-kit.
SRAM detector	A PCB board with 4 SRAM cells that was used to characterize the beam and to measure scintillator counts
SF2 starter kit	A starter kit board with the SmartFusion2 (SF2) SoC FPGA.
Computer	A VNC server was set up on a computer inside the experimental hall, which made it possible to control the experiment from the control room. The computer was running all the necessary software to control and monitor the experiment.
USB DAQ	Data acquisition board form National Instruments (NI). Used to establish analog and digital connection to the test boards and send data to the computer.
Radiation film	A film that reacts when irradiated. Used to identify the beam.
leveled laser	Was used to pinpoint the center of the beam.
Mirror	Used to reflect the laser beam to the backside of the test boards.
XY-positioning system	Connected to the computer so we can change the position of the test boards from a computer

Table 5.2: Equipment used in the experiment

5.1.3 Preparation and characterization of the beam

Before we could start testing of the PCB, the cyclotron had to be made ready for a proton beam and the magnet controlling the direction had to be put in the right position to get the beam out in experiment area 2.

Beam Setup

When the beam was ready and we could start with our tests, we had to start with the characterization of the beam, to see that it hits around the area that we expect. This was done by using radiation films that turns black when exposed to radiation.

One of these was placed right in front of the beam exit and one in front of Device Under Test (DUT) area. This was done to see how the beam spread out, and to get a feeling of where the beam center was. Afterwards a more precise calibration was done by the use of the SRAM detector and the scintillator. By measuring the relation between scintillator counts on the scintillator which was in a locked position and SEU on the SRAM that was connected to the XY-position system (which made the SRAM freely to move), we were able to find a more precise position of the beam center by seeing which position gave us the highest number of SEUs compared to scintillator counts. When the beam center is found and everything works as it should, the laser was placed in a position so that the laser beam points to where we had found center of the beam to be. After that we could replace the SRAM board with the PCB that we were going to test. This had to be done every day at startup, before we could start the actual tests.

We were able to control the intensity (Current) of the beam freely from the control room inside the limitation of the beam (for protons that is up to $100 \mu\text{A}$), but we kept us in the area between 100 pA to a few nA . This way the radiation dose to the test boards can be controlled. The beam intensity could be measured by putting a Faraday Cup (FC) in front of the beam, which was connected to a high accuracy multimeter. The FC had to be removed when tests were running, since it will block the beam.

We were running up to 3 labVIEW programs through the experiment, one for controlling the XY-position system, one for the SRAM board (to measure SEU and scintillator counts when calibrating and to get scintillator counts during the tests) and one program for each of the test boards. The SRAM and test board programs were constantly saving data on the disk.

5.1.4 What was Tested at OCL

We had beam time in three periods at OCL, which is $13.11.13 - 15.11.13$, $28.11.13 - 29.11.13$ and $08.04.14 - 11.04.14$. The boards that where tested the first period are: $TPS51200_1$, $MIC69302WU_1$, $SN74AVCB164245_1$, $SN74AVC2T245_1$, $QS3VH257_1$ and $SY89831U_1$, tested in that order. The second period we tested: $ADN2814$, $MAX3748$, $SY89831U_2$, $TPS51200_2$, $MIC69302WU_2$, $SN74AVCB164245_2$, $SN74AVC2T245_2$ and $QS3VH257_2$, in that order. And the third period, the focus was mainly the SF2 starter-kit, but $INA210_1$, $INA210_2$, $TLV3011_1$ and $TLV3011_2$ was also tested.

5.2 Irradiation at The Svedberg Laboratory (TSL)

The main difference between OCL and TSL is that TSL are able to produce beam of much higher energies. TSL is a much more professional facility, in the way that there are more people working there ready to help, and we don't need any calibration before we can start radiation test. We can simply show up and expose what we want to expose, and data like fluence and exposed time, are given to use, making it easy for us to calculate the dose and flux.

5.2.1 About TSL

TSL is an accelerator facility belonging to University of Uppsala in Sweden, [22]. It is mainly used for proton therapy on cancer patient by Uppsala University Hospital, but it is also used for medical research and radiation testing of electronics. The heart of the installation is a Gustav Werner cyclotron that delivers a beam of charged particles in energies up to 192 MeV. The particles that can be produced are everything from protons to highly charged xenon ions. There are several extraction points from the cyclotron, which is controlled from the *control room*. The beam can be lead out into the *blue hall*, which is the experiment area used for electronics testing. Here there are two user areas, one for protons, and one for neutrons and heavier ions, see figure 5.2.1.

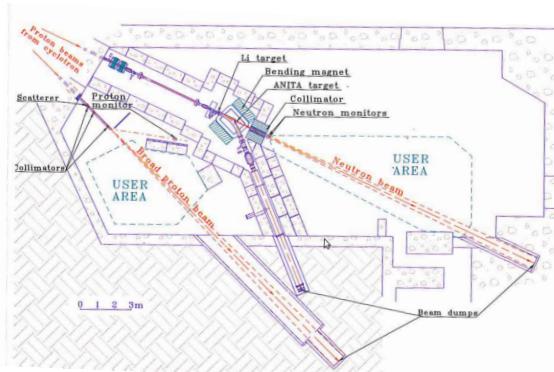


Figure 5.2.1: Layout of the Blue hall

5.2.2 Beam Setup Procedure

At TSL we didn't have to get a beam characterization as we did at OCL. In the Blue hall there is a permanently setup with detectors and a well-defined beam line. We only needed to set up our test equipment, put the test board at a given extraction

point, and start the test. The center of the beam was found by lasers places in looked positions around the hall, one for horizontal direction and one for vertical direction. The head of the laser was movable, so we could point the laser beams towards our test board. A computer which was remotely controlled through network connection was placed in the hall. This computer was used as a connection point to our test boards. We sat in a room called *counting room*, where we could turn the beam on and off as we desired. There were also a machine in the counting room, which was connected to detectors in the blue hall telling us the fluence (number of protons per cm^2 in total) and exposed time. The fluence can be used to calculate the flux and dose. The energy of the proton beam we got was 170 MeV.



Figure 5.2.2: Setup in the blue hall. Here the RCU2 is mounted, ready for test

5.2.3 What were Tested at TSL

A week before we arrived at TSL, we got the first two prototypes of the RCU2. That means that we had a limited time to make test code for all of the different parts of the board.

The focus of the visit to TSL was the SF2 SoC FPGA, but we also tested an optical receiver and an optical data link, which respectively are being used for TTC (timing, trigger and control) and to send data out from the RCU2. We brought with us two RCU2s and a total of 7 starter-kits, where 3 of these were with a smaller package, M2S050-FG484, and the rest was engineering samples versions of M2S050-FG896, which is the one used on RCU2. For the test discussed in section 4.4, we only used the SF2 starter-kits to test, since the test only involves internal parts of the SF2 SoC FPGA. Two of the starter-kits with the smaller package (M2S050-FG484) were tested, and one with engineering sample (M2S050ES-T-FG896). When the RCU2 cards was irradiation, things like SERDES (data link), trigger, clock and data recovery (CDR) and PLL was tested, which will not be discussed thoroughly in this work, but a short summary will be given. Current was measured on both the SF2 starter-kits and RCU2 boards when they were irradiated to check for latchup.

Chapter 6

Calculations and Results from Radiation Tests

This chapter will explain how the collected data after irradiation test at OCL were used to calculate flux and dose, and results from irradiation tests at OCL and TSL will be presented.

After an irradiation test at OCL, the collected data consist of the exposed time, scintillator counts, current consumption and output data of the DUT. From the calibration before radiation test, we got the relation between scintillator counts and SEU on the SRAM detector. From earlier tests with the SRAM detector the cross section for an incoming proton to induce a SEU is known. These data is used to calculate our way to the received dose for each of the different IC. The next section will explain the calculation process.

6.1 Calculation of Dose

Two ways to calculate dose will be discussed in this section, which are manually using energy loss and LET, see section 3.2, and using simulation data from a program named FLUKA. Which of these gives us the most reliable result will be discussed at the end of this section.

6.1.1 Definitions

Absorbed radiation dose has the unit of energy/mass and the SI-unit is gray (Gy), which is 1 Joule of energy absorbed in a kilogram of matter [J/Kg], see equation 6.1. Another unit which is often used when it comes to radiation of electronics is Rad, which is short for "Radiation absorbed dose". The relation between Rad and Gy can be seen in equation 6.2.

$$1\text{Gy} = 1 \frac{\text{J}}{\text{kg}} \quad (6.1)$$

$$1\text{Rad} = 0.01\text{Gy} = 0.01 \frac{\text{J}}{\text{kg}} = 10^{-5} \frac{\text{J}}{\text{g}} \quad (6.2)$$

The particle energy is normally expressed in electronvolt (eV) or Megaelectronvolt (MeV). One electronvolt is defined as the amount of kinetic energy gained by a single unbound electron when it accelerates through an electric potential of one Volt, thereof eV. Its value is $e = 1.602 \times 10^{-19}\text{C}$ which is the electric charge, multiplied with one Volt, which equals $1.602 \times 10^{-19}\text{eV}$ or $1.602 \times 10^{-19}\text{J}$.

$$1\text{MeV} = 10^6\text{eV} = 10^6 \cdot 1.602 \times 10^{-19}\text{J} = 1.602 \times 10^{-13}\text{J} \quad (6.3)$$

6.1.2 Calculating Dose Using LET

As explained in section 3.2.3, LET is energy deposited in a material through ionization when a particle crosses the material. LET is equal the energy loss a particle suffer by crossing a material, which means that we can use the Bethe Bloch formula that is expressed in equation 3.1. By looking at total LET for an IC, we are able to calculate our way to the dose. The energy loss of a particle is highly energy dependent, but for short distances it can be assumed to be constant without getting too much error.

Two energies was used when exposing components at OCL, The first time we had a proton beam with an energy of 28 MeV, the two other times we had a beam of 25 MeV. DUT was placed 130 cm from beam exit, which means that the protons will suffer some energy loss in the air between beam-exit and DUT. To make the work easier for us, an energy loss calculator program [23] was used to calculate the *energy loss* for a 28 MeV and a 25 MeV proton beam in air, we get respectively $17.52 \frac{\text{MeVcm}^2}{\text{g}}$ and $19.2 \frac{\text{MeVcm}^2}{\text{g}}$. By multiplying with the density of air which is $\rho_{air} = 0.001275 \frac{\text{g}}{\text{cm}^3}$,

we get $22.3 \frac{\text{keV}}{\text{cm}}$ and $24.5 \frac{\text{keV}}{\text{cm}}$. This means that the energy of the protons when they collide into DUT is:

$$E_{proton1} = 28 - (130\text{cm} \times 22.3 \frac{\text{keV}}{\text{cm}}) \approx 25\text{MeV} \quad (6.4)$$

$$E_{proton2} = 25 - (130\text{cm} \times 24.5 \frac{\text{keV}}{\text{cm}}) \approx 22\text{MeV} \quad (6.5)$$

By using the same energy loss calculator we get that the energy loss in silicon (which an IC mostly consist of), are:

$$-\frac{dE}{dx}(25\text{MeV}) = 17.1 \frac{\text{MeV}\text{cm}^2}{\text{g}} \quad (6.6)$$

$$-\frac{dE}{dx}(22\text{MeV}) = 18.9 \frac{\text{MeV}\text{cm}^2}{\text{g}} \quad (6.7)$$

If we look at a single proton entering a silicon material, the energy deposited by that single proton can be expressed as,

$$\Delta E_{proton} = -\frac{dE}{dx} \cdot \Delta x \cdot \rho_{Si} \quad (6.8)$$

where Δx is the length segment a proton particle penetrates into the material, and ρ_{Si} is the density of silicon.

$$\rho_{Si} = 2.33 \frac{\text{g}}{\text{cm}^3} \quad (6.9)$$

To get the total energy deposited in the IC, we have to multiply the energy of a single proton with the fluence and the area of the IC. Fluence is the total flux over a given time, expressed in $[\frac{n}{\text{cm}^2}]$. The total energy is then:

$$\Delta E_{total} = \Delta E_{proton} \cdot fluence \cdot A_{Si} = -\frac{dE}{dx} \cdot \Delta x \cdot \rho_{Si} \cdot fluence \cdot A_{Si} \quad (6.10)$$

Now we know the total energy depleted by a proton beam in an IC, and can start calculating the dose. Dose is energy per mass, as said in section 6.1.1. That means that the absorbed dose in silicon can be expressed as,

$$Dose(Si) = \frac{-\frac{dE}{dx} \cdot \Delta x \cdot \rho_{Si} \cdot \Phi \cdot A}{m_{Si}} \quad (6.11)$$

where m_{Si} is the mass of silicon.

m_{Si} can be expressed in terms of silicon density, see equation 6.9, multiplied with the volume (V_{Si}), which is Area (A_{Si}) times thickness (d_{Si}). Assuming that the protons enters the silicon in a straight line, the path segment Δx is equal the thickness, which then gives us,

$$Dose(Si) = \frac{-\frac{dE}{dx} \cdot \Delta x \cdot \rho_{Si} \cdot \Phi \cdot A}{\rho_{Si} \cdot A_{Si} \cdot d_{Si}} = -\frac{dE}{dx} \cdot fluence = \left[\frac{MeV}{g} \right] \quad (6.12)$$

To get the dose in Rad instead of $\frac{MeV}{g}$, we have to multiply with the converting factor given in equation 6.3 and divide on the factor given in equation 6.2, this gives us:

$$Dose(Si) = 1.602 \cdot 10^{-8} \cdot -\frac{dE}{dx} \cdot fluence \quad (6.13)$$

6.1.3 Calculating Dose Using FLUKA Simulations

The program FLUKA can be used to simulate particles with a user given energy in whatever material you want. We simulated a proton beam with energy of 28 MeV and 25 MeV in air, and set our DUT-position 130 cm away from beam exit. The results can be seen in table 6.1.

Energy at beam exit	28 MeV	25 MeV
Dose/primary particle at DUT[Gy]	4.08E-10	2.94E-10
Primary particles at Beam exit	1	1
Primary particles at DUT	0.1331	8.57E-2
Beam intensity reduction at DUT	7.51	11.67

Table 6.1: FLUKA simulation with 28MeV proton beam

As said in the introduction to this chapter, the known values after a radiation test are, exposed time, scintillator counts, current consumption, output data of the DUT and cross section from the SRAM detector.

The procedure to calculate the dose is first to find the proton fluence. This is found by first converting from scintillator counts to SEU, by multiplying with the converting factor, as found in the beam setup, and then divide on the cross section, which is known for the SRAM detector. Fluence can then be found as seen in equation 6.14 and the flux as in equation 6.15.

$$Fluence_{DUT} = \frac{SEU}{CS} \quad (6.14)$$

$$Flux = \frac{Fluence}{time} \quad (6.15)$$

Now we can take use of the FLUKA simulation results. The simulation results tells us how many protons will hit DUT when one proton will be sent out from beam exit, and what dose this will give the DUT. By using the calculated Fluence for DUT, found by equation 6.14, we can find the fluence at beam exit by dividing on *primary particles at DUT* from the simulation results, see equation 6.16. Then we can use *dose per primary particle at DUT* from the result and multiply with the Fluence at beam exit, which gives us the dose in gray for the DUT, see equation 6.17. By multiplying with 100 we get the dose in Rad.

$$Fluence_{BE} = \frac{fluence_{DUT}}{primaryparticles_{DUT}} \quad (6.16)$$

$$Dose_{DUT} = Fluence_{BE} \cdot \frac{Dose}{primaryparticle_{DUT}} = [Gy] \quad (6.17)$$

6.1.4 Comparison of LET and FLUKA

To compare LET calculations with FLUKA simulation we need an example. If we look at the test result for radiation of MAX3748:

Both of the methods to calculate dose requires the fluence. The fluence is given by scintillator counts, conversion value from scintillator counts to SEU on SRAM, and cross section, see equation 6.14. For MAX3748 the fluence is

time	2472
proton energy Beam exit	25 MeV
scintillator counts	2698510
scintillator counts to SEU SRAM	0.473
Cross section	1.14E-6

Table 6.2: Results after radiation of MAX3748

$$Fluence_{MAX3748} = \frac{2698510 \cdot 0.473}{1.14 \cdot 10^{-6}} = 1.12 \cdot 10^{12} \quad (6.18)$$

Calculations Using LET

To calculate the dose using LET, just follow the steps as given in section 6.1.2. We start by calculating the energy when entering the integrated circuit 130 cm away from beam exit. This is found in equation 6.4 to be 22 MeV. LET or energy loss for a 22 MeV proton particle in silicon, is calculated in equation 6.5 to be 17.1 MeV.

Fluence is found in equation 6.18. By using equation 6.13 we get the total dose in Rad to be:

$$Dose(Si) = 1.602 \cdot 10^{-8} \cdot 17.1 \cdot 1.12 \cdot 10^{12} = 306.8kRad \quad (6.19)$$

Calculations Using FLUKA Simulations

Calculating using FLUKA simulation is an easy process. First calculate fluence at Beam exit, from equation 6.16. And use that value to calculate the dose as seen in equation 6.17.

$$Fluence_{BE} = \frac{1.29 \cdot 10^{12}}{0.0857} = 1.51 \cdot 10^{13} \quad (6.20)$$

$$Dose_{DUT} = 1.51 \cdot 10^{13} \cdot 2.94 \cdot 10^{-10} = 4425.4Gy = 383.8kRad \quad (6.21)$$

Discussion

We can see that the FLUKA results give approximately 20 % higher dose than by using LET. On smaller dose this deviation will be much smaller. For example for ADN2814, the calculated does using LET is 85.6 kRad and simulation results gives us 107.1 kRad.

When calculating LET for a given IC we calculated with constant energy drop through the air before colliding with the IC and through the IC. In reality energy loss will increase as the energy decreases, this means that the calculated dose is a little smaller than the actual dose.

When it comes to FLUKA simulation, we don't really have control of what is calculated and which values are used. But the program is used for advance simulations for people at CERN and all over the world, and is an acknowledged program.

Which of these calculations gives us the most reliable calculation, can be discussed. There are small errors from approximation using LET. But then again, since we know about these approximations, we know that the energy should be a little higher than the calculated value. And can be sure that the calculated dose is at least not higher than the actual dose. From the FLUKA simulations we don't really know how the program calculates, it may be very accurate or it could do approximations as well.

There may also be other sources of errors, like that the proton beam given at the lab (it may differ from 25 MeV which it is said to be), and the conversion factor found in the beam setup. Nevertheless, the dose calculations doesn't need to be totally accurate, we only need to know the dose level, and then both of the methods are good enough. The dose values used further in this work are from FLUKA simulation, which is because this method was easiest to use, and the it gives us probably the most accurate calculations.

6.2 Results from OCL

6.2.1 Calibration process

As explained in chapter 5.1.3, we had to start by finding the center of the beam. The laser was first placed in a position pointing on what thought to be center. Then we placed a film in front of the beam exit and DUT area. By seeing how the film

looked like after irradiated, we got a feeling of where the center was. An example of two films from the beam exit and DUT area can be seen in figure 6.2.1.

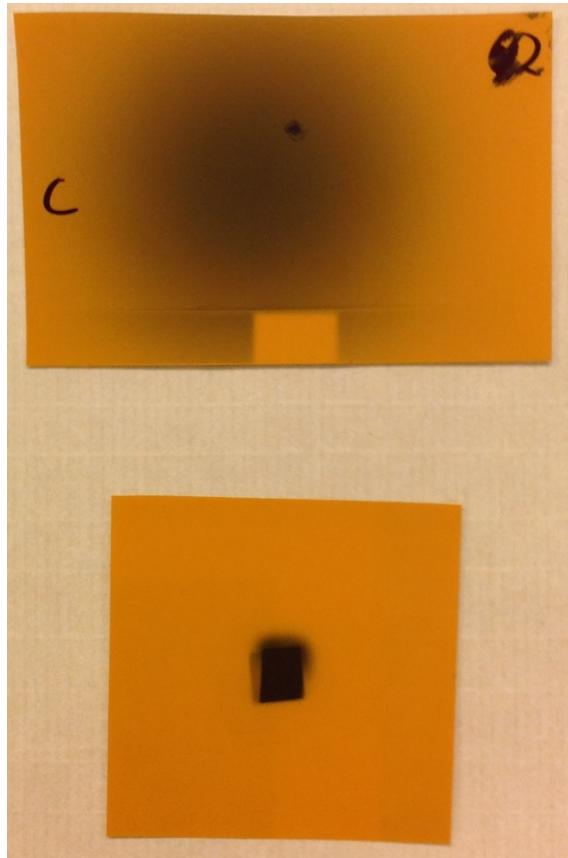


Figure 6.2.1: Example of radiation films after radiation, DUT area (top) and bream exit (button). The laser beam position is marked with a dot.

Now we had a feeling of where center is, compared to where the laser was pointing. The SRAM detector was placed with one of the SRAM chips at where the laser was pointing. This position was called position zero (x,y) = (0,0). From irradiated films, we knew approximately how much we had to move to be in center of the beam. In table 6.3 you can see the results from our calibration 15.11.2013. You can see that position $x = -2.5$ cm and $y = -1$ cm gives highest relation between SEU and scintillator counts. A total of 4 tests in that position were done and the average value gives us 0.0948. Beam setup data from all other days at OCL can be found in appendix A.1. When we irradiated the different PCBs, we didn't have SEU data, but we had scintillator counts, the relation value was used to convert from scintillator counts to SEU. We wanted to have the SEU value, because the cross section for a SEU on the SRAM detector is known. The cross section is the probability that an incoming particle will induce an SEU, and the value can be found in equation 6.22. Knowing number of SEUs and cross section, we can find the total fluence of an irradiation test.

$$CS = 1, 14e - 6 \quad (6.22)$$

Calibration test nr.:	x	y	Scint rel	SEU(SRAM)	SEU(SRAM)/sc
1	-0,8	-1	27798	1463	5,26E-02
2	-1,3	-1	17721	1239	6,99E-02
3	-1,8	-1	12904	1203	9,32E-02
4	-2,3	-1	13361	1276	9,55E-02
5	-2,8	-1	12786	1238	9,68E-02
6	-3,3	-1	12342	1156	9,37E-02
7	-2,5	-1	11696	1223	1,05E-01
8	-2,5	-1,5	11027	1075	9,75E-02
9	-2,5	-2	11835	1063	8,98E-02
10	-2,5	-0,5	15593	1540	9,88E-02
11	-2,5	0	12620	1034	8,19E-02
12	-2,5	-1	65280	5999	9,19E-02
13	-2,5	-1	52752	4803	9,10E-02
14	-2,5	-1	57229	5250	9,17E-02

Table 6.3: Calibration tests 15.11.2013

6.2.2 Test Results of the PCBs

In this section the result from irradiation test at OCL will be presented and discussed. Test of all the PCBs will be presented first, followed by a presentation of the SF2 test. The result is presented after type, meaning that two PCBs containing the same IC will be presented together. The purpose of these tests has been to check for radiation tolerance. The focus has therefore been to check the output data/voltage and current compared with the received dose.

An overview of the test can be found at the end of this section, with the total exposed time, the total irradiated dose and error status.

TPS51200

This was the first component that was tested for radiation, we started therefore out with a very low intensity to be sure that everything worked as it should. The intensity was increased for the later tests. Two PCBs of this type was supposed to be tested, but only one of these worked when we were at OCL.

In figure 6.2.2 you can see the input current and output voltage versus the received dose in kRad. The total exposed dose for this board is 42.8 kRad, and it still worked as it should, with only small increase in current. Normally we would irradiate until we would see some more irradiation effects, but since no errors occurred until 40 kRad, it was no point in exposing anymore.

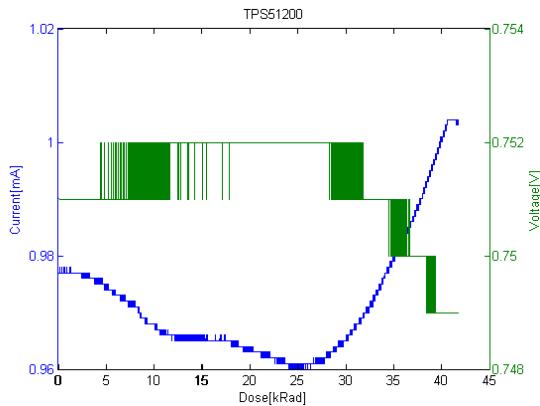


Figure 6.2.2: TPS51200 - Current/Voltage vs Dose

MIC69302WU

During the test of the first board we increased the intensity of the beam quite drastically at the end of the irradiation, which can be seen from the flux graph, in figure A.2.3.

This IC had an unexpected reaction to irradiation. You can see from both of the graphs that the current is decreasing and voltage is increasing, normally we would expect the opposite, or at least that the current would increase, see section 3.4.2. As seen from the graph in figure 6.2.3 it starts quite early to decrease in current, but it also stabilizes after a while. The output voltage is mostly stable, there were an increase of 2% on both of the tests, and that with a dose of 150 and 350 kRad.

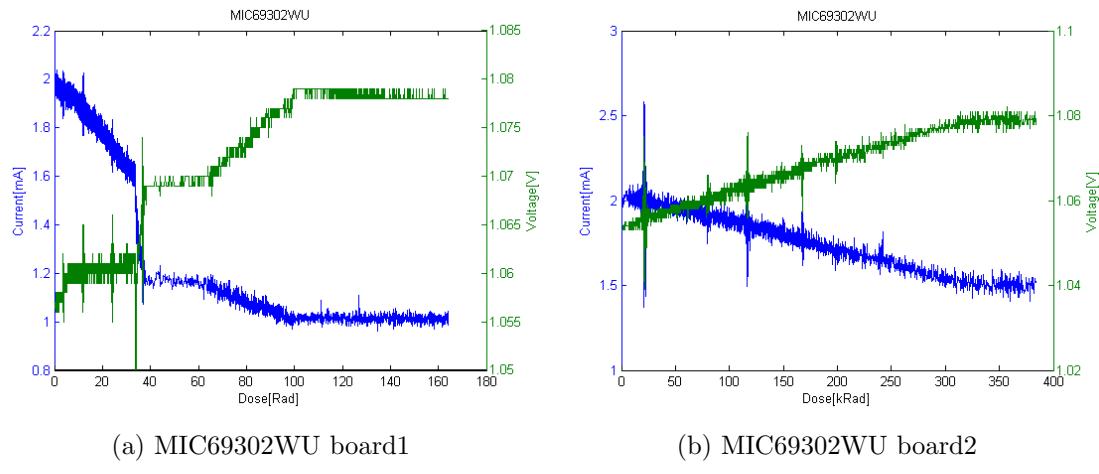


Figure 6.2.3: MIC69302WU - Current/Voltage vs Dose

SN74AVCB164245

For both of the test no errors were detected on the output data. Current versus dose can be seen in the graphs in figure 6.2.4a and 6.2.4b. The second board was exposed to a much higher dose, therefore we can see much more increase on the current for this board. The reason for the “jumps” in current is because the output is constantly changing from on to off, with a gap of 4 seconds. Not any effects are detected before a radiation dose of approximately 40 kRad.

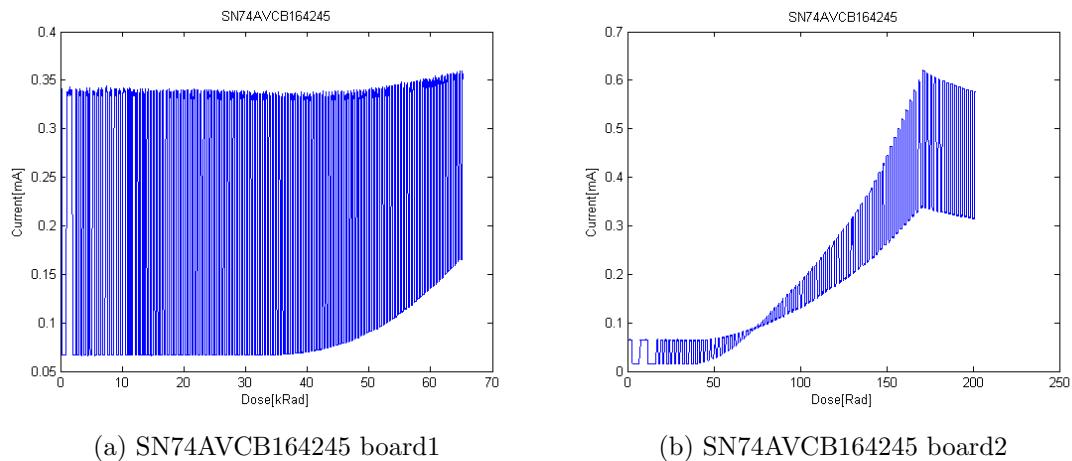


Figure 6.2.4: SN74AVC2T245 - Current vs Dose

SN74AVC2T245

On the first radiation test of this board something didn't work as it should. After 740 s and a dose of 98 Rad the chips output was stuck at '1'. The reason for this is unknown. I fear that the IC was defected before we started the radiation test, since it gives a totally different current characteristic than test board nr. 2. The input was switching from high to low every 4 second explaining the constantly change in current. If we look at the test results from board 2, the current goes unchanged up to 40 kRad, and no errors were detected at all.

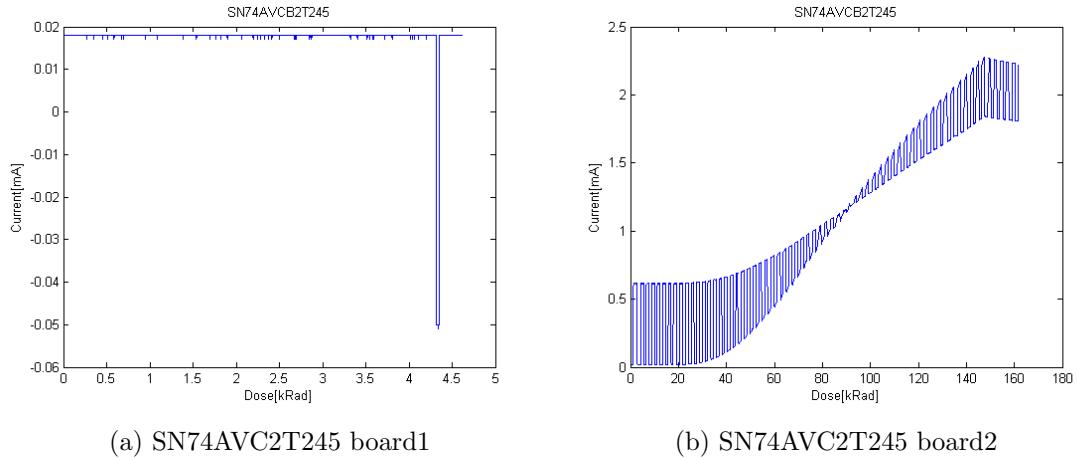


Figure 6.2.5: SN74AVC2T245 - Current vs Dose

QS3VH257

For both of the boards no errors on the output data were detected through the whole irradiation test. The current graphs can be seen in figure 6.2.6a and 6.2.6b. We see a small increase in current before 30 kRad, after that it starting increasing in a more rapid speed.

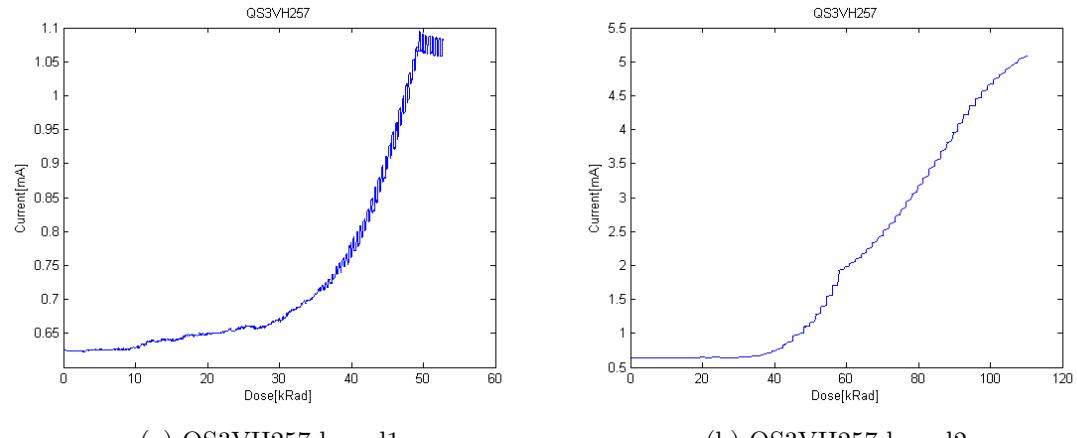


Figure 6.2.6: OS3VH257 Current vs Dose

SY89831

For test of these boards we required to use the modified MIC69302WU as described in section 4.2.2, because of the high current consumption. No errors were detected on the output data through both of the tests, the current characterization can be seen in 6.2.7a and 6.2.7b. This board is quite temperature dependent, a small increase in temperature, can increase or decrease current by hundreds of μ A. The

small increase in current we can see on both of the boards may also be temperature difference. It is nevertheless very small.

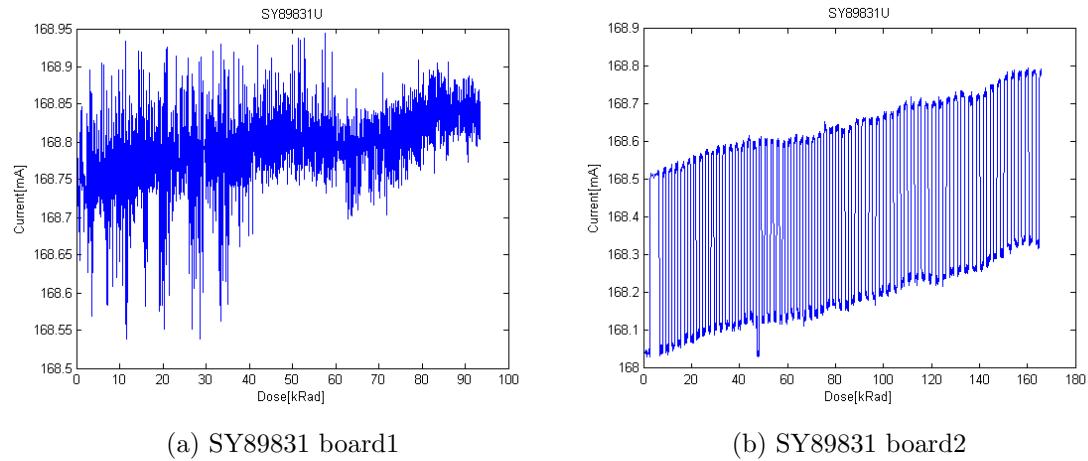


Figure 6.2.7: SY89831 - Current vs Dose

ADN2814

As mentioned in 4.2.7, we needed a SF2 starter-kit and the modified MIC69302WU board with a 3.3 V output voltage to test and supply this IC.

The current didn't change before a dose of 200 kRad had been received, but we got a clock error at a dose of ~ 11 kRad, and a data error after a dose of ~ 8 kRad, see figure 6.2.8 and 6.2.9.

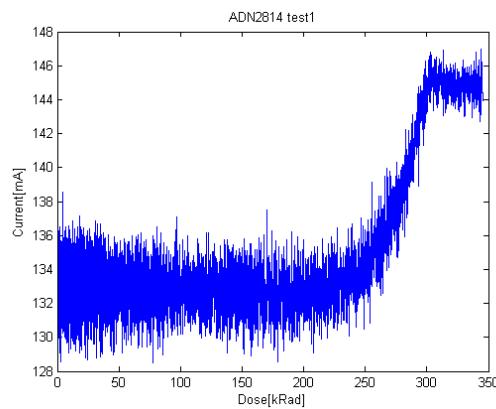


Figure 6.2.8: ADN2814 - Current vs Dose

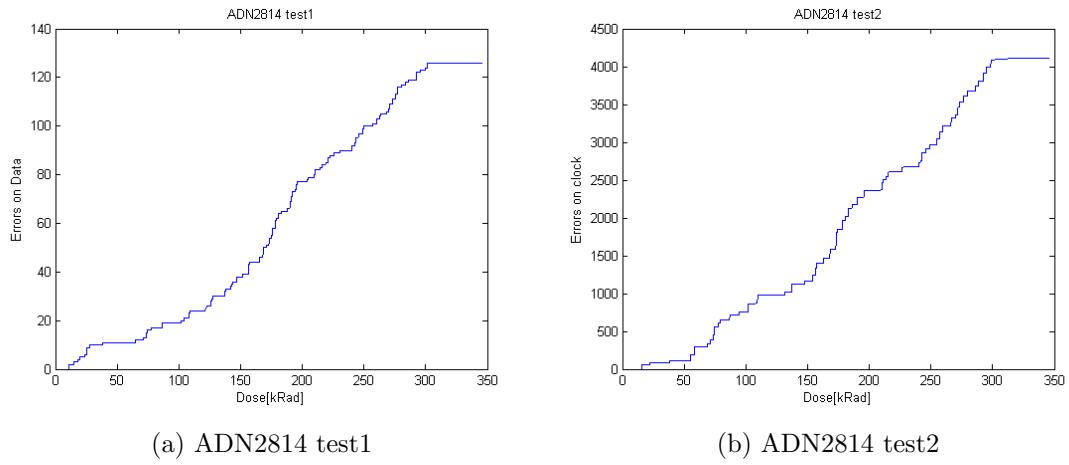


Figure 6.2.9: ADN2814 - Relative errors vs Dose

MAX3748

Also here the solution using SF2 and the modified MIC69302WU board was used to test and supply this IC.

After a dose of over 400 kRad no error were detected on the data signal, and current consumption was stable through the whole irradiation process.

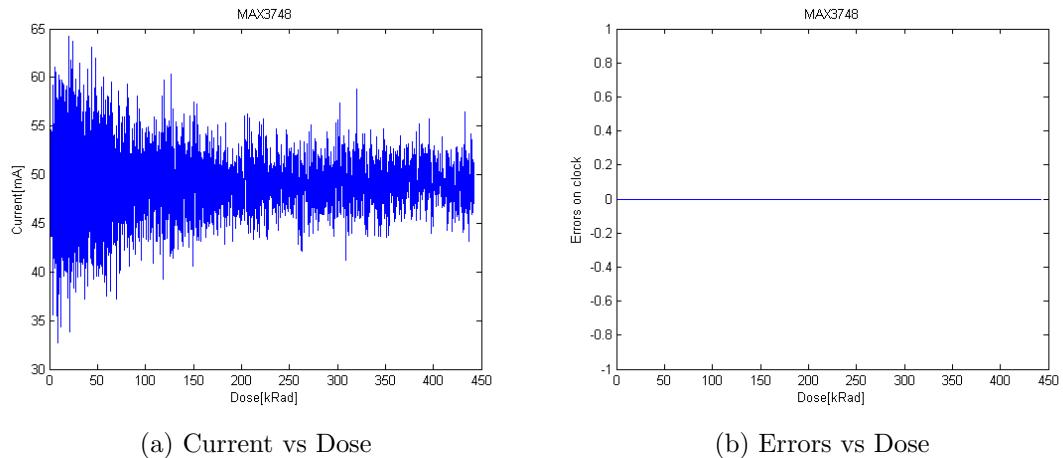


Figure 6.2.10: MAX3748

Summary of the Results

In table 6.4 and 6.5 you can see how long each ICs has been exposed to radiation, the dose they have been received and if an error occurred during the irradiation. A returning effect from radiation was that current consumption started increasing with the received dose, the exception was MIC69302WU which actually decreased

and to then stabilize after a while, which I have really no good explanation for. Some of the test didn't go as expected, like $TPS51200_2$ and $SN74AVC2T245_1$, and that is why we tried to at least have two boards which was tested, so that if one of them didn't work, we would at least have one working test.

Device	Exposed time[s]	Dose[Rad]	Error
$TPS51200_1$	2065	41800	No
$MIC69302WU_1$	2240	164000	No
$SN74AVCB164245_1$	967	65200	No
$SN74AVC2T245_1$	860	4600	Yes
$QS3VH257_1$	795	52800	No
$SY89831_1$	1251	93500	No

Table 6.4: Tests at OCL 15.nov 2013

Device	Exposed time[s]	Dose[Rad]	Error
$ADN2814_run1$	1273	20200	Yes
$ADN2814_run2$	2286	324900	Yes
$MAX3748$	2384	442200	No
$TPS51200_2$	-*	-*	-*
$MIC69302WU_2$	1385	383800	No
$SN74AVCB164245_2$	526	201400	No
$SN74AVC2T245_2$	478	161600	No
$QS3VH257_2$	264	110300	No
$SY89831U_2$	921	165800	No

*The board wouldn't work at test time

Table 6.5: Tests at OCL 27-28.nov 2013

Device	Exposed time[s]	Dose[Rad]	Error
$INA210_1$	1084	220,9	No
$INA210_2$	1661	174,9	No
$TLV3011_1$	742	120,1	No
$TLV3011_2$	1074	149.1	No

Table 6.6: Tests at OCL 08-11.April 2014

Discussion of the Result

We had access to OCL in three periods; 13.11.13-15.11.13, 28.11.13-29.11.13 and 08.04.14-11.04.14, but most of the testing was done 15.11.13, 28.11.13 and 11.04.14. The other days was used to get familiar with the instruments and equipment that was being used, to prepare the setup and setting up the beam.

There are almost impossible to get the same beam two days at a row. Each day of testing is therefore different from each other. And that is also why we had to do calibration each day at start-up.

The interesting thing when determining if an IC is tolerant towards radiation is the absorbed dose. For run2 in the LHC, which will last in three years, it has been estimated that the total dose in the TPC is 1-2 kRad. This is the absolute limit an IC has to survive, and a safe margin of at least 3 times should be used. We also have to take into account that when radiating at OCL, we have been using proton beam of less than 30 MeV, in the TPC detector in ALICE, we can receive protons and neutrons in the energy level of higher than 1 GeV, which may cause other effects that we have seen in our test at OCL. It is therefore important to have a good margin on the dose.

For the test of SN74AVCB164245, SN74AVC2T245 and QS3VH257 the output signals were only measured digitally by a USB-DAQ, which means that we really don't know if the voltage level shifted because of the received dose. The USB-DAQ used has an input low level from -0.3 V to 0.8 V and the input high level from 2.0 to 5.8, which means that we could actually have a large swing on the output without being detected. But then again, changes on the output can normally be referred back to current consumption, as we see on both TPS51200 and MIC69302WU, We didn't see any increase in current before a dose of 30-40 kRad, and therefore we can assume that the output signal were good at least until then.

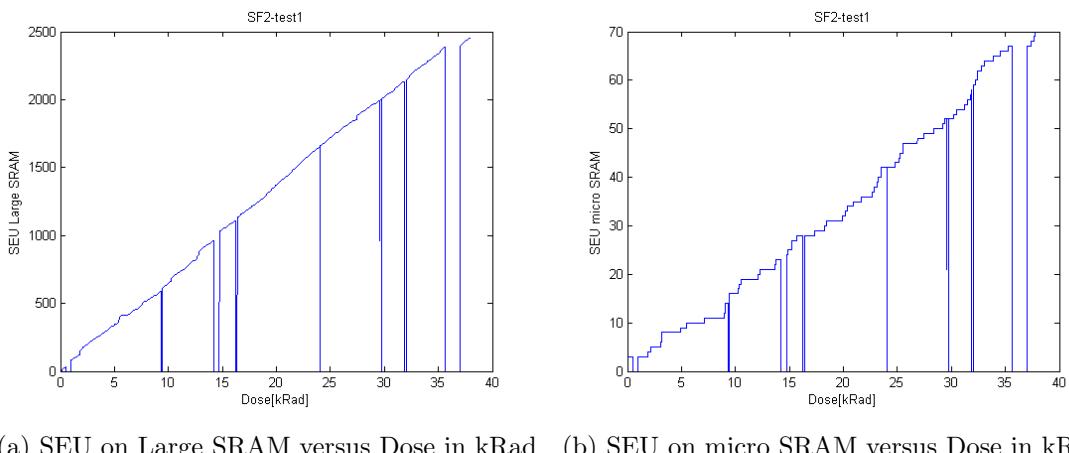
Every ICs which was tested worked after a dose of 6 kRad, which is three times more than the expected dose we could expect in the ALICE TPC. That means that every component that has been tested is cleared to be used in the RCU2 design. The IC which performed worst is ADN2814, which gave us an error after a dose of 8kRad, but then the test method wasn't necessarily the best. But since MAX3748, performed so much better, and could be used for the same purpose, this would preferable be used.

6.2.3 Test Results on SF2

In this subsection the results from radiation test on the SF2 M2S050ES chip will be presented. The different parts of SF2 which were tested will be presented for them self, and we will have a discussion on the total result at the end. Only one starter kit was tested, but the beam was turned off and on some times during the test. After a dose of approximately 37 kRad we got a very high increase in current, probably caused by a latchup. We did a power cycle of the board, and the current went back to a normal level. The test result presented are divided into before and after the power cycle, hereafter called run1 and run2. The shift-register design made for testing of the logical element, see section 4.4.2, was only used in run2. After a dose of ~ 8 kRad on run2, the current increased again. We tried another power cycle, but this time it was permanently. The total dose after radiation was ~ 45 kRad.

SRAM

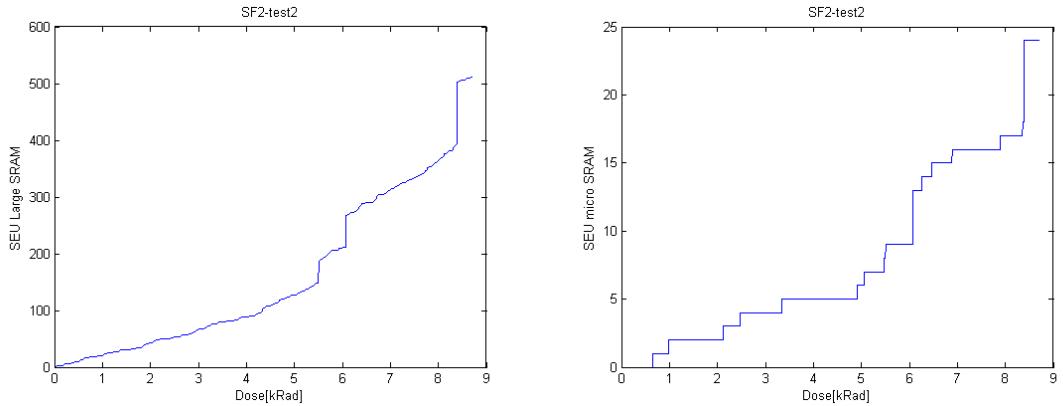
The purpose of the SRAM test is to see how reliable the SRAM memory is, and to find a cross section for upset in the memory. In figure 6.2.11 and 6.2.12 you can SEUs on large SRAM and micro SRAM versus dose. During the test, we had some problems with the Microcontroller SubSystem (MSS), which stopped working in periods. The Microcontroller SubSystem (MSS) was running in debug mode, which made it possible to restart the MSS as we wanted. If the MSS stopped working, a restart brought the communication up and running again, but then we had a short period of lost data. This can be seen as drops in the SEUs and cycles counter, and small fall in current, see appendix A.



(a) SEU on Large SRAM versus Dose in kRad (b) SEU on micro SRAM versus Dose in kRad

Figure 6.2.11: LSRAM and micro SRAM test results before shutdown

Slightly after a dose of 35 kRad, we can see a gap where we have no increase in upset on neither the large SRAM nor the micro SRAM. The flux is stable and the



(a) SEU on Large SRAM versus Dose in kRad (b) SEU on micro SRAM versus Dose in kRad

Figure 6.2.12: Large SRAM and micro SRAM test results after shutdown

cycle counter is not changing as well (see appendix A). This suggests that something is not working in the FPGA. I would think that there is a problem with the clock signal, maybe because of PLL lock loss. We got two PLLs errors in that period supporting that theory, see 6.9

We can see that for run1, the SEUs on the large SRAM is increasing quite linear, this means that a cross section can be found. The SEUs on the micro SRAM got a stepwise increase in SEUs, which doesn't look so linear. There are much fewer memory bits in the micro SRAM compared to the large SRAM, in total there are 9.5 times more large SRAM bits than micro SRAM bits (622592 and 65536). To get a more precise calculation on cross section for the micro SRAM, we should have run with a much higher intensity, or over a longer period to get more statistics.

To get as much precise calculation as possible for the cross section, we should check over the period which is most linear and without errors or as few errors as possible. Therefore the cross section for the large SRAM is being calculated from the period in between 17 and 24 kRad on run1. The corresponding fluence for the start and endpoint is respectively $5.0026E - 10$ and $6.994E - 10$, and the total SEUs for that period are 513. To calculate the cross section from the micro SRAM, we preferable would have more SEUs before calculating, but that isn't available. So to calculate the cross section for micro SRAM, we will look of the whole period, even though this might include some errors. This means that the total fluence and SEUs are respectively, $1.11 \cdot 10^{11}$ and 70. The equation to calculate the cross section can be taken from equation 6.14, giving us,

$$CS = \frac{SEUs}{Fluence_{DUT}} \quad (6.23)$$

device	CS [cm^2]	CS per bit [cm^2/bit]	$\sigma_{CS}[cm^2/bit]$
Large SRAM	$2.6 \cdot 10^{-8}$	$4.18 \cdot 10^{-14}$	$7.29 \cdot 10^{-15}$
micro SRAM	$6.31 \cdot 10^{-10}$	$9.62 \cdot 10^{-15}$	$1.32 \cdot 10^{-15}$

Table 6.7: Calculation of Cross section with uncertainty

Uncertainties

A number of uncertainties are present in the measurement, and we need therefore to take these into the calculations.

- The uncertainty resulting from finding the ratio between the number of scintillator counts and the number of SEUs (σ_{ratio}) in the calibration process of the SRAM detector was commonly about 10 %.
- The uncertainty introduced due to the nonlinear response (σ_{lin}) of the scintillator to the intensity of the beam was estimated to 10 %
- Since the number of SEUs detected are random in time and linearly dependent on the amount of incoming particles, the uncertainty can be given by Poisson distribution and is $\frac{1}{\sqrt{N_{SEU}}}$
- Uncertainties from errors (σ_{err}) occurred during the run, is estimated to be about 10 %.
- From the uncertainty of the position of the device at the extraction point we estimate 2 % (σ_{pos}).

This gives us an uncertainty on the cross section of:

$$\sigma_{CS} = \sqrt{\sigma_{ratio}^2 + \sigma_{lin}^2 + \left(\frac{1}{N_{SEU}}\right)^2 + \sigma_{err}^2 + \sigma_{pos}^2} \quad (6.24)$$

The calculated values for cross section per bit with uncertainty can be found in the table 6.7.

Logic Element

For run1 we didn't manage to turn on the shift register design, because of some errors in the test code. This was solved before run2.

SEU in the shift registers	Exposed time[s]	Dose[kRad]
1	320	2.95
2	357	3.53
3	358	3.54
4	417	4.46
5	620	7.81
*	620	7.28

* Lots of shift register errors followed after this

Table 6.8: Shift register errors in run2

On run2 we ran 4 shift register chains with shift register length of 2000, with 4 inverters in between each register and 4 windowed shift register. The frequency used was 40 MHz. In table 6.8, you find the results from run2.

We detected 5 shift register errors in total over a dose of 8 kRad and the first shift register error occurred after a dose of 2.95 kRad. That was something like we would expected, but one of the point with this test, were to see if we could distinguish between upset and transient on the tracks by changing on the frequency. Now we only run on a 40MHz, meaning we can't say anything if the error we see is an upset in the registers, or transient on the track. We got at least a feeling on how often we would see an error on the shift register with the settings used.

PLL and Latchup

Graphs of current versus dose can be found in appendix A. We got two SEL, which more than doubled the current for the 1.2 V source, from around 270 mA to around 730 mA on run1, and in run2 we went from 400 mA to around 850 mA. The nominal current for run2 was a little higher since the shift register design was also running.

In table 6.9 and 6.10 you can see the result from the PLL test. The PLL that was monitored was driven by another PLL. Thus, assuming that if the first PLL loses its lock signal and thus clock, the second PLL will also lose its lock signal. We got a total of 23 PLL lock loss, giving us 11.5 losses per PLL over a dose of 45 kRad. A noticeable thing is that the first lock loss already occurred after a dose of 0.7 kRad. We also have a period between 5.0 and 18.7 where we didn't detect any PLL lock loss at all, which is rather strange.

We can find a cross section for PLL lock loss, even though we have little data to make a good statistics. The total fluence for the whole test $1.36 \cdot 10^{11}$, which gives us a cross section per PLL to be,

PLL lock loss	Exposed time[s]	Dose[kRad]
1	88	0.7
2	166	1.3
3	304	2.3
4	473	3.6
5	523	4.0
6	663	5.0
7	2363	18.7
8	2440	19.3
9	2720	21.5
10	2938	23.1
11	2938	23.1
12	3306	26.0
13	3600	28.4
14	3633	28.6
15	4125	32.6
16	4575	36.1
17	4546	36.1
18	4624	36.5

Table 6.9: Time and dose for the PLL errors run1

PLL errors	Exposed time[s]	Dose[kRad]
1	301	2.68
2	372	3.76
3	541	5.50
4	576	7.08
5	589	7.28

Table 6.10: Time and dose for the PLL errors run2

$$CS = \frac{\frac{PLLloss}{2}}{Fluence} = \frac{11.5}{1.36 \cdot 10^{11}} = 8.46 * 10^{-11} \quad (6.25)$$

We will also have some uncertainty in the measurement. These are:

- Since the number of errors detected are random in time and linearly dependent on the amount of incoming particles, the uncertainty can be given by Poisson distribution and is $\frac{1}{\sqrt{N_{err}}}$
- The uncertainty resulting from finding the ratio between the number of scintillator counts and the number of SEUs (σ_{ratio}) in the calibration process of the SRAM detector was commonly about 10 %.
- The uncertainty introduced due to the nonlinear response (σ_{lin}) of the scintillator to the intensity of the beam was estimated to 10 %
- From the uncertainty of the position of the device at the extraction point we estimate 2 % (σ_{pos}).

$$\sigma_{CS} = \sqrt{\left(\frac{1}{N_{err}}\right)^2 + \sigma_{ratio}^2 + \sigma_{lin}^2 + \sigma_{pos}^2} \quad (6.26)$$

this gives the cross section for a PLL lock loss with uncertainty to be:

$$CS = 8.46 * 10^{-11} \pm 1.26 \cdot 10^{-11} \quad (6.27)$$

Discussion on the Results

The SRAM test gave us around the expected numbers of SEUs, but we had some problems with the MSS during the test. The calculated cross section for large SRAM and micro SRAM are respectively $4.18 \pm 0.73 \cdot 10^{-14}$ and $(9.62 \pm 1.32) \cdot 10^{-15}$, which is around the same magnitude as other SRAMs which has been tested [18] and [5], which supports the results.

But since we got some problems with the MSS, we have some potential improvements for our test. We discovered that the MSS wasn't so reliable, and the data extracted should have been done without going through the MSS. This could be done by making a serial communication code in VHDL, and using GPIO

pins as transmitting and receiving lines. If another test shall be done on the SF2 SRAM memory, this could been an option.

We had also quite many PLL errors which could be a rather big problem when the RCU2 will be mounted in the TPC. If the clock is not working, we would have a period where we don't have any data collection, and it is when there is most radiation we are most interested in the data.

We didn't detect any current increase before a dose of 37 kRad, which is a really good result.

The shift register design didn't give us the result we wanted. We wanted to see if we would have higher cross section with higher frequencies, indicating that we are able to pick up more SET with higher frequency. But since we only got to test on one frequency, we couldn't distinguish between SET and SEU in the registers.

All in all the first radiation test of the SF2 did go quite well. We had some PLL errors, but we had a feeling that this would be a problem, so it wasn't any surprise.

6.3 Results from TSL

In this section the results from the irradiation test at TSL will be presented. The focus has been on the SF2 test, but other test will briefly be presented and discussed.

A total of two RCU2s and three SF2 starter-kits were exposed to radiation. When we radiated the RCU2, we tested SERDES communication, Clock and data recovery, latchup and trigger interface. When testing the SF2 starter-kits, the focus were mainly the test mention in section 4.4.

6.3.1 SF2 Radiation Test

Two starter kit with SF2 M2S050-FG484 were tested, and one starter-kit with SF2 M2S050ES-FG896 (engineering sample). The SF2 M2S050-FG484 is the same SoC FPGA which we are going to use on the RCU2, only with smaller package. Therefore we preferred testing on these instead of the engineering sample versions, which may have some early design errors. The things that were tested on the starter-kits with the smaller package are SRAM, PLL, Logic element and latchup. When testing the M2S050ES-FG896, the focus was only to see for how long we could program the device with increasing dose.

Device	Starter-kit1	Starter-kit2
Nr. of power cycles	62	95
PLL1 loss	22	3
PLL2 loss	116	136
PLL3 loss	60	69

Table 6.11: Overview of power cycles and PLL lock loss

Some improvements have been done to the test since the radiation at OCL. We have added two more PLL lock signals to monitor, and we have found a more effective way to measure current. Instead of using the current measurement board as described in section 4.4.4, we used a small PCB with several INA226, which is an ADC with I^2C communication protocol. The SF2 also has I^2C communication protocol, which means that we could use the monitoring board to control and receive data from the ADC-chip. By using this method we also got the voltage on each of the different power source that was measured. The monitoring board was also connected to the enable pin of the 3.3 V *voltage regulator* on the test board, making it possible to turn on and off the starter-kit under test at will. Every tenth of a second the status of data was written to a console and to a file, which made it possible to monitor as the tests were running, and look at the data afterwards.

Also instead of running the Microcontroller subsystem in debug mode, as we did in OCL, we were running in release mode. This means that the MSS was running whenever we got power on the kit.

PLL and Latchup

We monitored three PLL lock signal though the test. We got a total of 176 PLL lock loss through the first test and 205 PLL loss from the second test, whenever we lost lock on PLL1 we also got a loss on PLL2, since this PLL is using the clock from PLL1 as source, therefore these hasn't been taken into account in the total lock loss. The distribution over the three PLLs lock signals can be seen in table 6.11.

The first PLL loss occurred after a dose of 0,043 kRad for the first test and after 1.332 kRad on the second, which is a fairly low dose. This means that PLLs could be a problem for the RCU2 design. If possible, we should try and not use PLLs, or have some kind of redundancy, when using these.

We can find a cross section for PLL lock loss. The total fluence for the two tests is $2.39 \cdot 10^{11}$ and $2.93 \cdot 10^{11}$, which gives us a cross section per PLL to be

$$CS = \frac{\frac{PLLloss}{3}}{Fluence} = \frac{58,67}{2.39 \cdot 10^{11}} = 2.45 * 10^{-10} \quad (6.28)$$

$$CS = \frac{\frac{PLLloss}{3}}{Fluence} = \frac{205}{68,33 \cdot 10^{11}} = 2.33 * 10^{-10} \quad (6.29)$$

We will also have some uncertainty in the measurement. These are:

- Since the number of errors detected are random in time and linearly dependent on the amount of incoming particles, the uncertainty can be given by Poisson distribution and is $\frac{1}{\sqrt{N_{err}}}$
- Downtime due to power cycle of the board during a run, we estimate 5 % (σ_{pow}) uncertainty.
- From the uncertainty of the position of the device at the extraction point we estimate 2 % (σ_{pos}).
- For the fluence measurement will also have a little uncertainty, this is estimated to be about 2 % (σ_{flu}).

$$\sigma_{CS} = \sqrt{\left(\frac{1}{N_{err}}\right)^2 + \sigma_{pow}^2 + \sigma_{pos}^2 + \sigma_{flu}^2} \quad (6.30)$$

this gives the cross section with uncertainty to be:

$$CS = 2.45 * 10^{-10} \pm 1.41 \cdot 10^{-11} \quad (6.31)$$

$$CS = 2.33 * 10^{-10} \pm 1.34 \cdot 10^{-11} \quad (6.32)$$

We discovered on the first test, that the 0.1Ω and 0.16Ω resistors which were used, respectively on the 1.2 V and 3.3 V power source, were too high, since the maximum voltage the ADC could measure are 81.92 mV. When a latchup occurred the ADC was maxed, meaning we only knew that the voltage is above 81.9 V (current above 819 mA, but not how much above). Therefore both of these resistors where replaced with a resistor of 0.025Ω on the second starter-kit test.

As for the test in OCL, we also got some drops in current. Always when the current drops the measured voltage for the 1.2 V power source would also drop, typically down to around 850 mV (the 3.3 V power source is stable though). When this happens the communication through the serial port also fails, which is understandable since the power source has dropped 300 mV below the specification for the IC. Normally when we see a decrease in voltage, we see an increase in current or opposite, but in this case both drops. The only explanation for this is that the voltage drops first, causing processes in the SF2 to shutdown, which results in decrease in current. The regulator controlling the 1.2 V power signal is placed right next to the SF2 chip, and it is therefore very exposed to radiation, and it is likely that that this regulator is the problem for this effect. (The regulator has not been tested for radiation before because we are not using it in the RCU2 design). By turning off and on the 3.3 V regulator, resulting in turning the 1.2 V off and on, since this is powered by the 3.3 V signal, the voltage and current goes back to what they were on startup. This was done through the monitoring board, where we had made a function which turns the regulators off and on again after 3 seconds. This function was used whenever we detected a latchup or a decrease in current/voltage. In total we had to restart the board because of latchup or decrease in current, 61 times on first test and 95 times on test2.

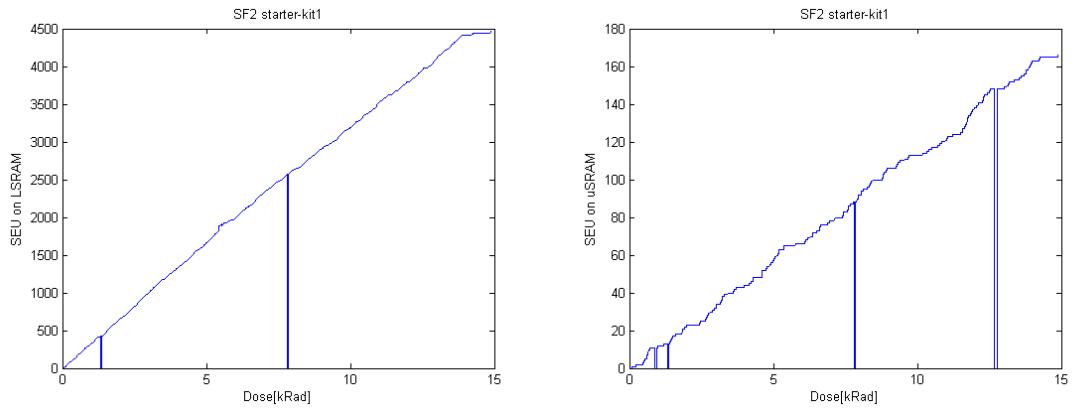
SRAM

In figure 6.3.1 and 6.3.2 you can see the results from the SRAM test after radiation of the two SF2 M2S050-FG484. In 6.3.2 we can see regularly drops down to 0 in the counter values, that are loss of communication with the SF2, probably caused by voltage drop or latchup as discussed in the previous subsection, we have the same phenomena for the first test as well, only the values didn't drop to 0, this can be seen as short flatness on the counter curve. A re-power of the board made the counters start again. This means that we have periods where we didn't get to measure the counter values, when the FPGA gets power again, the counter values are overwritten through the startup sequence, as described in section 4.4.1. The length of these non-measuring periods are varying from only a few seconds up to tens of seconds, this gives us allot of uncertainties when calculating cross section.

Cross Section Calculation

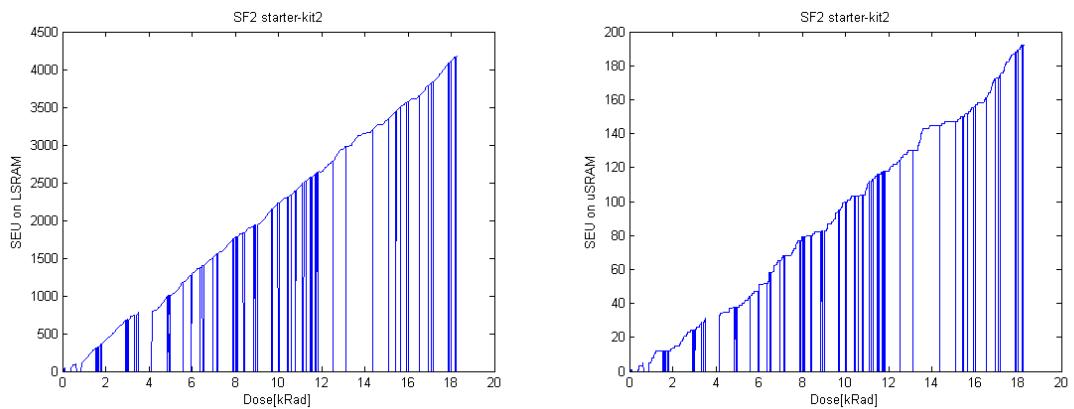
As we did when calculating cross section after the result from OCL, we want to find a period which are as linear and error free as possible. Therefore we will calculate the cross section in between 7.8 kRad to 14.3 kRad for test1 and in between 4.2 kRad to 18.5 kRad on test2.

To get as genuine value of the cross section as possible, we have to find the total fluence of when the test was working. That means that the fluence which was received when the test was stopped due to latchup, current drops and power cycles,



(a) SEU on Large SRAM versus Dose in kRad (b) SEU on micro SRAM versus Dose in kRad

Figure 6.3.1: Large SRAM and micro SRAM test results after shutdown



(a) SEU on Large SRAM versus Dose in kRad (b) SEU on micro SRAM versus Dose in kRad

Figure 6.3.2: Large SRAM and micro SRAM test results after shutdown

device	fluence start	fluence stop	fluence loss	total fluence	nr. of SEUs
Large SRAM1	$1.26 \cdot 10^{11}$	$2.29 \cdot 10^{11}$	$1.05 \cdot 10^{10}$	$9.30 \cdot 10^{10}$	1874
micro SRAM1	$1.26 \cdot 10^{11}$	$2.29 \cdot 10^{11}$	$1.05 \cdot 10^{10}$	$9.30 \cdot 10^{10}$	77
Large SRAM2	$6.70 \cdot 10^{11}$	$2.92 \cdot 10^{11}$	$3.26 \cdot 10^{10}$	$1.92 \cdot 10^{11}$	3379
micro SRAM2	$6.70 \cdot 10^{11}$	$2.92 \cdot 10^{11}$	$3.26 \cdot 10^{10}$	$1.92 \cdot 10^{11}$	159

Table 6.12: Fluence and SEUs overview for test 1 and 2

has to be subtracted. By checking the log-files we have estimated time with no data to be 108 second in between 7.8 kRad and 14.3 kRad for test1 and the 342 in between 4.2 kRad and 18.5 kRad for test2. The flux in that period is known (see flux graph in appendix A), which means that we can calculate the total fluence for the time without data collection. See table 6.12 for the calculated values.

Uncertainties

A number of uncertainties are present in the measurement

- Since the number of SEUs detected are random in time and linearly dependent on the amount of incoming particles, the uncertainty can be given by Poisson distribution and is $\frac{1}{\sqrt{N_{SEU}}}$
- Uncertainties from data collection and estimates and assumption when doing calculation, like constant flux in periods. We estimate an uncertainty of 10 % (σ_{data}).
- From the uncertainty of the position of the device at the extraction point we estimate 2 % (σ_{pos}).
- For the fluence data given to us we will also have a little uncertainty, this is estimated to be about 2 % (σ_{flu}).

This gives us an uncertainty on the cross section of:

$$\sigma_{CS} = \sqrt{\left(\frac{1}{N_{SEU}}\right)^2 + \sigma_{data}^2 + \sigma_{pos}^2 + \sigma_{flu}^2} \quad (6.33)$$

Then we can calculate the cross section per bit with uncertainty from the values in table 6.12, knowing that we have 622592 bits in the large SRAM and 65536 bits in the micro SRAM.

This gives us a average a cross section of the large SRAM and micro SRAM to be:

device	CS [cm^2]	CS per bit [cm^2/bit]	$\sigma_{CS}[cm^2/bit]$
Large SRAM1	$2.01 \cdot 10^{-8}$	$3.22 * 10^{-14}$	$3.35 \cdot 10^{-15}$
Large SRAM2	$1.76 \cdot 10^{-8}$	$2.83 * 10^{-14}$	$2.94 \cdot 10^{-15}$
micro SRAM1	$8.28 \cdot 10^{-10}$	$1.26 * 10^{-14}$	$1.32 \cdot 10^{-15}$
micro SRAM2	$8.28 \cdot 10^{-10}$	$1.26 * 10^{-14}$	$1.31 \cdot 10^{-15}$

Table 6.13: Calculation of Cross section with uncertainty

$$CS_{LSRAM} == (3.03 \pm 0.45) * 10^{-14} \quad (6.34)$$

$$CS_{LSRAM} == (1.26 \pm 0.18) * 10^{-14} \quad (6.35)$$

Logic Element

Through the test on the two starter-kits we run at 40, 80 and 160 MHz. This means that we should see some difference in upset detected by the shift register design. We used 4 shift-register chains with a length of 2500, and with 4 windowed shift registers (WSR). On run1 we used 4 inverters in between each register on run2 we had none. In table 6.14 you can see an overview of all SEU on the shift register design with a given frequency over a given fluence.

The results presented in table 6.14 are quite unexpected. We would think that by increasing the frequency, we would see more upset in the registers, but this isn't the case. Maybe the reason for this is that we had low statistics. If we had run in the respective frequencies for a longer time or with a higher flux, we would maybe see some other results.

Frequency	inverters	Fluence	shift-register upset	SEU/fluence (CS)
40 MHz	4	$1.40 \cdot 10^{11}$	51	$3.65 \cdot 10^{-10}$
80 MHz	4	$9.90 \cdot 10^{10}$	26	$2.63 \cdot 10^{-10}$
40 MHz	0	$6.16 \cdot 10^{10}$	19	$5.19 \cdot 10^{-10}$
80 MHz	0	$7.20 \cdot 10^{10}$	30	$4.17 \cdot 10^{-10}$
160 MHz	0	$1.60 \cdot 10^{11}$	32	$1.19 \cdot 10^{-10}$

Table 6.14: Cross section for the shift-register design with different frequencies

Programming Limit Test

The idea behind the programming limit test was to see how far up in dose we could go before we couldn't program anymore. We were supposed to use the same test setup as used when testing the two other starter-kits so that we would have approximately the same current, and the ability to shut it down when needed. But we didn't manage to get the current small PCB with INA226 to work. Therefore we decided that we would just power cycle regularly during our test and increase the dose of approximately 1 kRad for each time trying to program.

We tried to program after a dose of 1.20 kRad, 2.54 kRad and 3.80 kRad. The two first times worked fine, but the last time it failed.

6.3.2 Other Test at TSL

The other test at TSL includes SERDES and clock and data recovery and latchup detection under radiation of RCU2.

A brief introduction in how this were tested, and the setup will be explained:

The SERDES test involves sending data through a optical transceiver with a speed of 2.215 Gbps back and forth from the RCU2 and a *Xilinx Virtex-7 FPGA VC709 Connectivity Kit*. The test works in the way that a known pattern is sent from the Xilinx connectivity kit to the RCU2, and the RCU2 are set to echo back the received pattern to the Xilinx kit. The Xilinx FPGA checks if the returned data pattern is equal the transmitted. If the pattern is not equal a counter will be incremented.

The Clock and data recovery and trigger test were tested at the same time. To explain how the Clock and data recovery test worked, a little explanation on how the hardware setup is done is required. A optical Manchester decoded signal containing clock and data, is sent to the RCU2. On the RCU2 there is a optical receiver which receives the Manchester signal, but the received signal may vary, and is not so stable, therefore a limiting amplifier is used to make a more stable version of the signal. MAX3748 is used for that purpose (which is one of the components tested through this work). Then the stable signal coming from the limiting amplifier is sent in to the SF2 FPGA, where clock and trigger information is encoded, giving us a 40 MHz clock, and data signal. The clock signal is then sent into two different PLLs, and the PLL lock signal for both PLLs is checked for a falling edge. The idea behind using two PLLs, is to distinguish between PLL error and error in the incoming signal. If both of the PLLs loses lock at the same time we can assume that we have an error with the incoming signal and if only one of the PLLs losses lock, then we have a PLL

error. The received data signal contains a known trigger sequence, and a vhdl code is made to check for the trigger signal. Every time the trigger pattern is detected a counter is incremented. PLL lock data and trigger counter are sent to the MSS, where data is sent serial to a computer. On the computer a program was running taking in data from the serial port, and logging data every seconds.

For the SERDES test we exposed both the SF2 and the optical transceiver, which receives and sends data. For both of the test we detected few errors, less than 10 errors with a fluence of $3.18 \cdot 10^{11}$ when exposing the SF2 chip, and less than 5 errors when exposing the optical transceiver with a fluence of $3.6 \cdot 10^{11}$. This means that the SERDES will most likely not be a problem for our design.

For the Clock and data recovery test, we exposed both the SF2 and the optical receiver. When we exposed the SF2 we received PLL lock loss with around the same frequency as for the test with the Starter-kits, we got a cross section of $2.3 \cdot 10^{-10} \text{cm}^2$. Almost all the PLL errors was defined as PLL lock loss due to bad PLLs. But when we started to expose the optical receiver, we detected PLL lock losses all the time, which is quite bad, we got a cross section of $6.9 \cdot 10^{-9} \text{cm}^2$. This means that we have to find out what's the reason for this problem. Is it the optical receiver or the limiting amplifier which fails. More tests have to be done on this area, and a new solution to fix this problem or at least reduce the problem has to be found.

For the latchup test on the RCU2, we got a cross section for latchup to be $8.5 \cdot 10^{-10} \text{cm}^2$. But we did a discovery a thing while running the beam. After we received a few latchups, the 1.2 Voltage started to reduce a little, when this happened, we saw a tendency to have less latchups. We did a separated test on the RCU2, where we reduced the 1.2 Voltage to 1.1 V by changing a resistor on the board. The test showed us that we got a reduction on cross section to $1.7 \cdot 10^{-10} \text{cm}^2$, which is a reduction of ~ 5 from before. More test on this area should be performed, to see how far down in voltage we could go before things stopped working, and if the latchup problem could be reduced even more.

6.3.3 Discussion of the Results

A issues that we uncounted in the tests at TSL, and not so much in OCL, is latchup. We got regularly latchup during our runs, which means that a shutdown is required to set the board back in normal operation again. The latchups weren't destructive, a power cycle of the board put everything to normal and current level back to what it was before latchup. But it is still a problem, a latchup can cause a stop in process, and a repower of the RCU2 is required to go back to normal operation. A solution for this problem has already been set in motion. By using *INA210* to amplify a voltage over a shunt resistor for each of the power signals, and use *TLV3011* to compare against a voltage limit. If the voltage limit is exceeded, all regulators are turned off,

setting the board off. The problem here is that when we have allot of radiation and the probability of a latchup is high, that is when we are most interested in data.

We also discovered a way to reduce latchups. By changing the 1.2 source voltage to 1.1 V, we effectively reduced number of latchup by ~ 5 , and this can maybe be brought even lower by reducing the voltage even further. More test on this aspect should be performed.

The SRAM test on the two starter-kits did go fine, we had allot of downtime due to errors, but the cross section calculations for both of our test were quite close to each other, supporting our results. We got a cross section of $(3.03 \pm 0.45) \cdot 10^{-14} \text{cm}^2$ on the large SRAM, and $(1.26 \pm 0.19) \cdot 10^{-14} \text{cm}^2$ for the micro SRAM. Compared to the results from OCL, which gave us cross sections of $(4.18 \pm 0.73) \cdot 10^{-14} \text{cm}^2$ for the large SRAM, and $(9.62 \pm 1.32) \cdot 10^{-15} \text{cm}^2$ for the micro SRAM, the results doesn't seems so bad.

We would think that we would have higher cross section at OCL than in TSL, because energy deposited per proton is higher for a 25 MeV proton beam than with a 170 MeV proton beam, this can be seen from figure 3.2.1 (It shows different particles in air, but the principle is the same for silicon). The cross section for large SRAM supports this, but the micro SRAM doesn't. But then again, we had really low statistics on the micro SRAM, making the calculations not so trustworthy. Another test should be performed on the micro SRAM with higher intensity or over a longer period to check if the cross section is correct.

The Logic element design didn't go the way we thought it would go. The purpose of the test was to see if SET could be a problem on the RCU2. SET was supposed to be detected by changing frequency on the shift-register design, and if we would detected more upset when we had higher frequency, we could say that the increase of upsets was caused by SET. But we got too little statistics to be able to distinguish between upset in the registers and SET. But this is actually a good thing, because this means that we would need a rather high dose before we would have any SET. Meaning that SET most likely would not be a problem on the SF2 design.

For all of the test with PLL, we got a cross section for PLL lock loss in the area of $2 - 3 \cdot 10^{-10} \text{cm}^2$ when the SF2-chip was exposed. This is a fairly high cross section, and we don't know for how long a typical PLL lock signal stays low, if its only one clock cycle or if its up to seconds. If it is only a clock cycle we are talking about, we could probably accept this, but if it stays down for up too seconds, then we should do some measures to either reduce or counter this problem. When a PLL lock loss happened, we didn't detect any other problems in the process running on the SF2, this probably means that the clock signal only stays low for a short time period, which means that this probably could be acceptable.

A more disturbing issue happened when we moved the beam towards the

optical receiver. Then we got allot more PLL lock loss, we got a cross section of $6.09 \cdot 10^{-9} cm^2$, which is around 25 times more then when exposing the SF2. This means that either the optical receiver is not able to do its job under such radiation level, and introduces allot of noise, or the limiting amplifier MAX3748 is not able to remove noise from the incoming signal. Nevertheless this is a major problem, and a new solution or a major change is required to fix this.

Chapter 7

Conclusion and Outlook

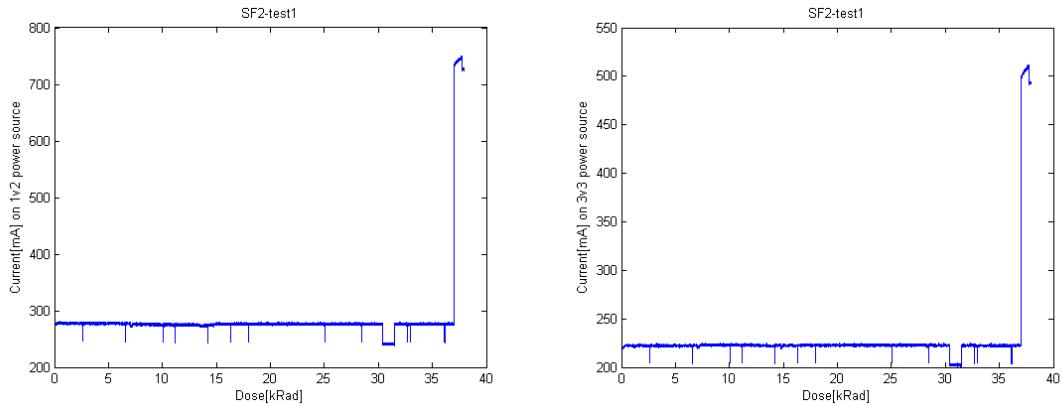
The work presented in this thesis was done to

Appendix A

Radiation Results

A.1 Beam setup data

A.2 Radiation Results from OCL



(a) Current on the 1.2 V source over time for SF2 test1 (b) Current on the 3.3 V source over time for SF2 test1

Figure A.2.1

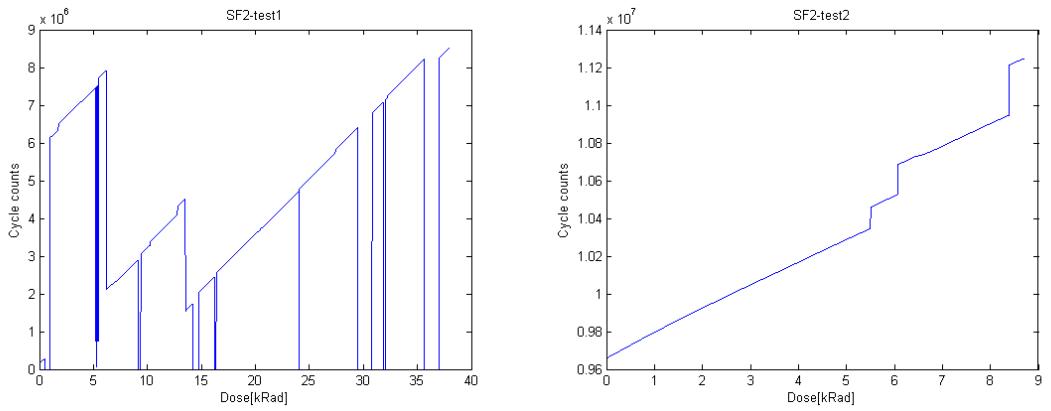
In figure A.2.3, A.2.4 and A.2.5 you can see graphs of flux vs time for the different test boards. The reason the graphs don't go as linear as one would expect, is that the beam sometimes stopped and had to restarted, and that we increased and decreased the intensities as we wanted.

Calibration test nr.:	x	y	Scint rel	SEU(SRAM)	SEU(SRAM)/sc
1	0	0	23813	1971	8.28E-02
2	0	-0.5	37930	3867	1.02E-01
3	0	-1	27527	2817	1.02E-01
4	0	-1.5	34413	3360	9.76E-02
5	0	-2	32713	2763	8.45E-02
6	0.5	0	38753	2709	6.99E-02
7	-0.5	0	23420	2483	1.06E-01
8	-1	0	20611	2232	1.08E-01
9	-1.5	0	21014	2410	1.15E-01
10	-1.5	0	20676	2260	1.09E-01
11	-2	0	35787	3776	1.06E-01
12	-2.5	0	27847	2512	9.02E-02

Table A.1: Calibration tests 14.11.2013

Calibration test nr.:	x	y	Scint rel	SEU(SRAM)	SEU(SRAM)/ sc
1	-0.8	-1	27798	1463	5.26E-02
2	-1.3	-1	17721	1239	6.99E-02
3	-1.8	-1	12904	1203	9.32E-02
4	-2.3	-1	13361	1276	9.55E-02
5	-2.8	-1	12786	1238	9.68E-02
6	-3.3	-1	12342	1156	9.37E-02
7	-2.5	-1	11696	1223	1.05E-01
8	-2.5	-1.5	11027	1075	9.75E-02
9	-2.5	-2	11835	1063	8.98E-02
10	-2.5	-0.5	15593	1540	9.88E-02
11	-2.5	0	12620	1034	8.19E-02
12	-2.5	-1	65280	5999	9.19E-02
13	-2.5	-1	52752	4803	9.10E-02
14	-2.5	-1	57229	5250	9.17E-02

Table A.2: Calibration tests 15.11.2013



(a) Cycle counter versus dose for SF2 test1 (b) Cycle counter versus dose for SF2 test2

Figure A.2.2

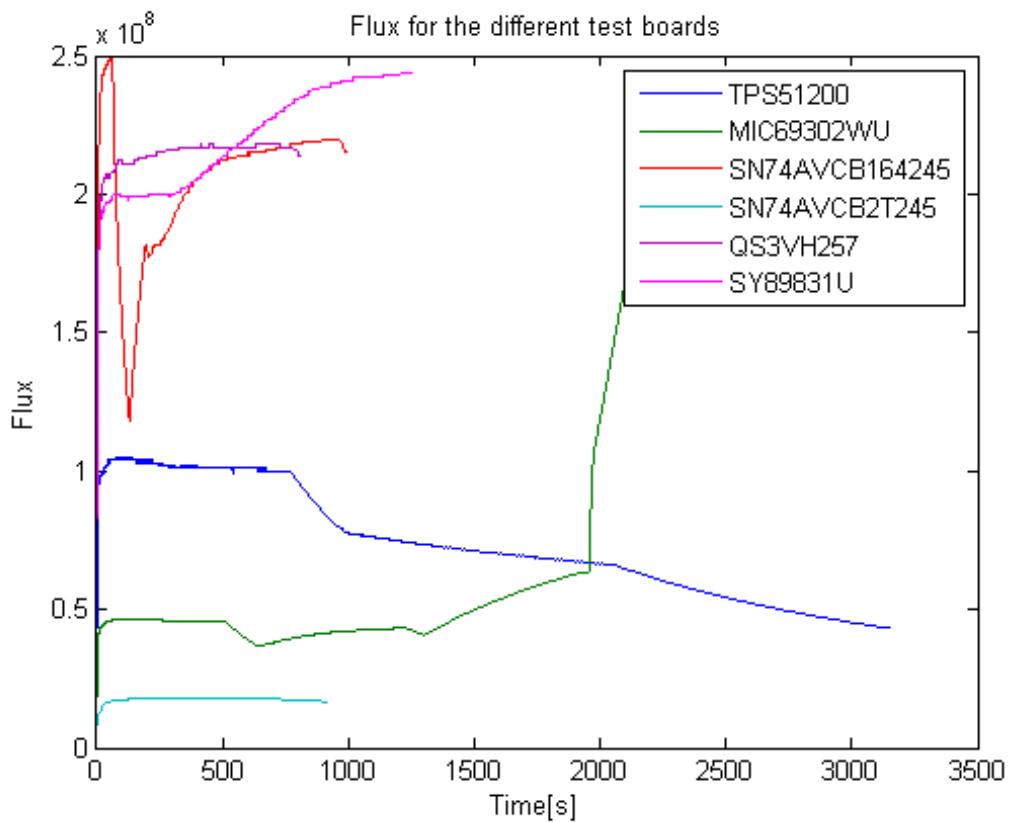


Figure A.2.3: flux for each component radiated 15.11.2013

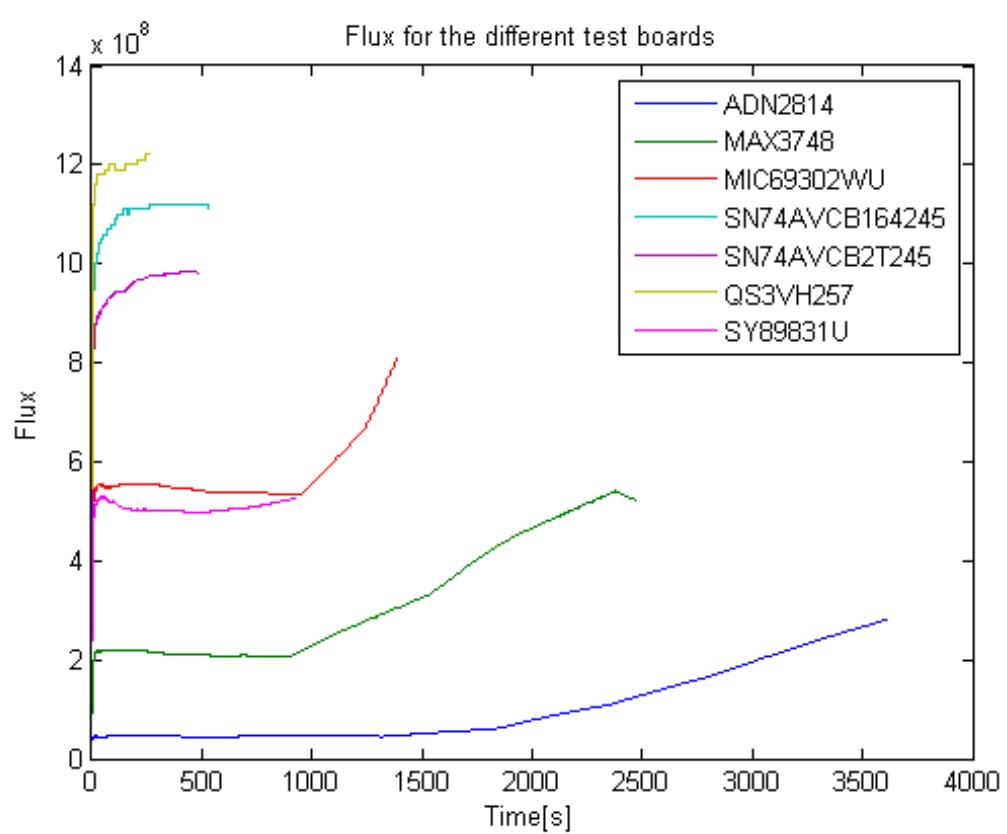


Figure A.2.4: flux for each component radiated 28.11.2013

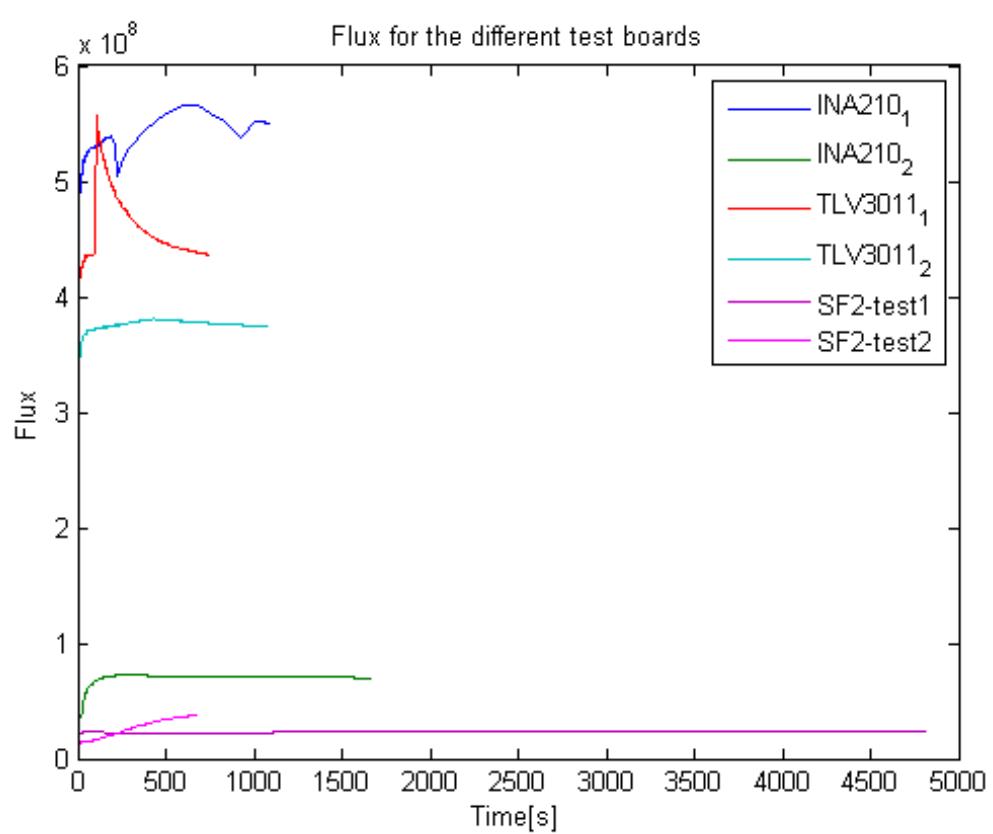


Figure A.2.5: flux for each component radiated 09.04.2014

A.3 Radiation Results from TSL

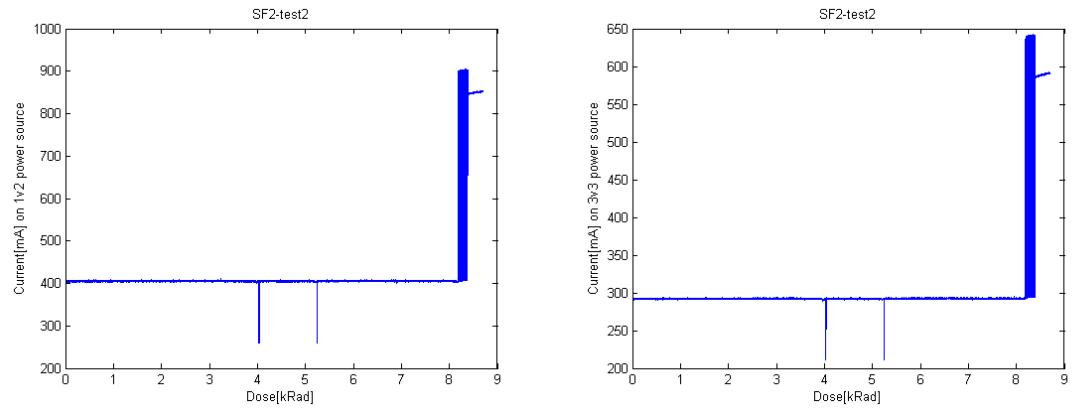


Figure A.3.1

Appendix B

Current measurement board tutorial

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