

**Department of Physics and Technology**



***Irradiation tests  
of ALTERA SRAM-based FPGAs***

**Candidatus Scientarium Thesis**

**by**

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**May 2004**

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# Abstract

The Large Hadron Collider (LHC) is the new particle accelerator which currently is under construction at CERN in Geneva. It will be capable of accelerating particles to higher collision energies than ever before, opening for a deeper look into matter. A Large Ion Collider Experiment, ALICE, is one of four experiments in the LHC. It is optimized for Pb-Pb (lead-lead) collisions where the main tracking detector is the Time Projection Chamber (TPC). Major parts of the front-end electronics in the TPC detector rely on the use of Commercial Off The Shelf (COTS) components, such as Field Programmable Gate Arrays (FPGAs). Due to the FPGAs increased complexity, they are in many cases becoming more attractive than the alternative ASICs. FPGAs based on SRAM technology make it possible to reprogram the device and may shorten the production time of the design. However, compared to the radiation tolerant ASICs, the FPGAs have proved to be sensitive to Single Event Upsets (SEUs).

A single event upset corresponds to a soft error appearing in a device due to the energy deposited in silicon by an ionising particle. It can be induced as a bit flip in the configuration memory, or as a bit flip in a register in sequential logic. An upset is random in time and all the memory bits have the same probability of being affected.

The front-end electronics of the TPC detector will be located on the detector approximately 3-5 meters from the interaction point. Consequently it will be exposed to the shower of particles produced in the collisions. Experiencing upsets during an ALICE experiment run may have fatal consequences for the integrity of the data. An upset in the configuration RAM can lead to a corrupt design and therefore a loss or stop in the data collection due to a reprogramming of the device.

The main objective of this thesis has therefore been to investigate the ALTERA APEX 20KE400 tolerance toward the TPC radiation environment, where the main particles of concern are high-energetic hadrons (protons,neutrons,pions,kaons above 10-20 MeV). It is expected that the protons will not be capable of producing enough direct ionization energy to cause a single event upset. Instead protons will interact with the nuclei of the silicon atom and produce heavy recoil ions with enough stopping power to induce a single event upset.

In order to investigate the SEU cross-section of the APEX 20KE400 device, upset detection firmware and readout software have been design for irradiation test purpose. A permanent test setup has been put together at the Oslo Cyclotron Laboratory providing a 29 MeV beam proton beam. The energy dependence of the SEU has been measured using a 38 MeV and 180 MeV proton beam at The Svedberg Laboratory in Uppsala. A cross-section of  $\sigma = 6.0 \cdot 10^{-9} \text{ cm}^2$  has been measured for the APEX 20KE400 SRAM-based FPGA. Based on simulations of the radiation levels in the TPC detector the expected error rate for the whole TPC detector will be of the order 3-4 per 4 hour run.



# Preface

This thesis has been carried out within the Microelectronics Research Group at the Department of Physics, University of Bergen, during the period of January 2003 to May 2004.

I would like to thank my supervisor Kjetil Ullaland for guidance and support throughout the period of work, and Dieter Röhrich for the many discussions and helpful hints related to the radiation physics of the thesis.

Further I would like to thank Jon Wikne and Eivind Olsen at the Oslo Cyclotron Laboratory for always providing their competence and preserving the best possible conditions throughout the test periods.

Special thanks must go to Alexander Prokofiev at TSL for his long shifts and helpful work contributing to making the irradiation periods at TSL both a pleasant and rewarding time. And also together with A.N. Smirnov from V.G.Khlopin Radium Institute for lending us some samples of their Thin Film Breakdown Counters for use in Oslo.

And last but not least my parents for their support the last few years.

Bergen, May 2004

Ketil Røed



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# Chapter 1

## Introduction

The Large Hadron Collider (LHC) is the new particle accelerator which currently is under construction at CERN in Geneva. Capable of accelerating particles to higher energies than ever before the LHC will open for a deeper look into matter. It is expected to commence operating in 2007, and will ultimately collide beams of protons at an energy of 14 TeV, and beams of lead nuclei with a collision energy of 1150 TeV. The heavy ion collisions are expected to produce a new state of matter called Quark-Gluon-Plasma (QGP). A Large Ion Collider Experiment (ALICE) is one of four main experiments in the LHC. It is optimized for heavy-ion collisions, and will through head-on collisions of Pb-Pb look for the creation of a QGP. The number of particles produced in these collisions is enormous, and ALICE has several detectors designed to track and identify these particles. The Time Projection Chamber (TPC) [8] is a cylindrical shaped detector filled with a gas mixture and serves as the main tracking detector. Particles created in the collisions will ionise the gas as they traverse the detector. The charged produced in the ionisation will be drifted by an electric field to both end plates of the TPC detector where it will be detected and converted into digital signals. The front-end electronics responsible for the readout of these signals will be placed 10 cm from the end plates and approximately 3-5 meters from the collision interaction point. Consequently it will be exposed to the shower of particles produced in the collisions. Major parts of the front-end electronics in the TPC detector rely on the use of Commercial Off The Shelf (COTS) components, components that are not custom designed for operation in radiation hazardous environments. Chapter 2 will give a more detailed description of the ALICE experiment and the front-end electronics.

Ensuring the reliability of semiconductor devices in radiation exposed areas has been an issue scientists involved in space physics have been concerned about for several years. Projects connected to space physics have therefore been leading the development of radiation hard electronics and equipment. The use of radiation hardened devices, as for instance ASICs<sup>1</sup>, has been the usual solution to the problem. However these devices, manufactured for use in military and space application, are generally very expensive. The todays development in semiconductor technology with decreasing feature sizes and higher density chips, has made programmable logic devices compatible with the custom made ASICs. Low prices and the possibility of in-system

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<sup>1</sup>Application Specific Integrated Circuits [1]

firmware updates favour the use of COTS FPGAs. Particularly the latter is a huge advantage for the TPC front-end electronics. Eventhough the LHC is not expected to start operating before 2007, all the equipment such as infrastructure, detectors, and readout electronics will be installed already in 2005. The accessibility of the ALICE experiment after installation will be extremely limited, but the use of FPGAs gives the opportunity to continue the development of firmware until the LHC will start operating. After the LHC has started taking data in 2007 there is only limited access to the experiment area to repair or change devices damaged due to radiation. Thus the use of COTS make stringent quality tests of the readout electronics mandatory before installation. Qualifying the devices involves irradiation testing to determine their radiation tolerance level. This investigation will be based on simulations of the expected radiation environment specific for the TPC detector [2].

## FPGA and radiation concerns

The system designers for the front-end electronics of the TPC have decided to use an SRAM-based Field Programmable Gate Array from ALTERA as the main controlling device of the readout electronics. This is the ALTERA APEX20K400EFC672 FPGA. There are concerns that this device might not work in the LHC radiation environment. The SRAM based FPGA is particularly sensitive to radiation effects related to the flux and dose rate, such as Single Event Effects (SEEs). Single event effects are radiation induced errors due to a single charged particle depositing energy through ionisation of the material. They are of great concern to the ALICE readout electronics since they can cause the electronics to fail at any time during operation, leading to potential loss of important data.

The main objective of this thesis has therefore been to investigate the ALTERA FPGAs tolerance for the TPC radiation environment. A major part has been to build a reliable irradiation test setup and develop firmware capable of detecting radiation effects in the FPGA. A shiftregister design has been implemented in sequential logic in order to detect Single Event Upsets, both single bit flips and configuration upsets, and for the application memory a FIFO design has been used. The energy dependence of the SEUs in the ALTERA FPGA has been measured by irradiating the device with proton energies of 25 and 28 MeV at the Oslo Cyclotron Laboratory, and with energies of 38 and 180 MeV at The Svedberg Laboratory.

## About the thesis

In order to investigate semiconductor devices for their radiation tolerance it is necessary to acquire good knowledge of the possible radiation effects that can be inflicted on such devices. Chapter 3 starts by introducing the most common types of radiation effects in semiconductor devices. It will futher address how radiation interacts with matter and silicon in particular. When doing irradiation test of electronic devices it is important to use the type of radiation that will represent the realistic scenario in the best possible manner. Thus the expected radiation levels for the TPC environment will be mapped as well. Keeping the main focus on single event upsets, some standard memory technologies will be introduces along with a special look at the Field Programmable Gate Array.

The second part of the thesis addresses the development of test methods for doing irradiation tests of an FPGA. Chapter 4 approaches the methodology from a general point of view, while chapter 5 treats the readout software and firmware upset detection designs in more detail. the irradiation test setup will be presented in chapter 6, with special focus on the beam line configuration and monitoring. Finally in chapter 7 the results from the irradiation test will be presented and the thesis will be summarised and concluded in chapter 8.

# Chapter 2

## The ALICE experiment

*This chapter gives a brief introduction to the ALICE experiment and the radiation exposed front-end electronics of the TPC detector. The information is gathered from the CERN official website[3] and the ALICE Technical Design Report [4].*

### 2.1 LHC and ALICE

CERN, the European Organisation for Nuclear Research, is a research center which provides access to particle accelerators to scientists around the world. By accelerating particles and smashing them together, different detectors near to the interaction point are used to identify the outcome of such collisions. The main objective is to explore the innermost basic constituents of matter and their mutual interaction. The extreme energy available in such collisions can contribute to discover new particles and new state of matter, and to recreate the conditions prevailing in the early universe, just after the Big Bang. Higher energy is the key word to allow these new discoveries. The Large Hadron Collider (LHC) [5] is a particle accelerator capable of accelerating particles to such energies.

The LHC is at present scheduled to start operating in 2007. Energies in the TeV range will be reached from head-on collisions of protons and heavy-ions. The new LHC accelerator will be built in the same 27 km tunnel as the LEP. Existing particle accelerators such as the Proton Synchrotron (PS) and Super Proton Synchrotron (SPS) will be used as pre-stage particle boosters for the LHC. Figure 2.1 shows a schematic overview of the complex structure of accelerators at CERN.

ALICE (A Large Ion Collider Experiment) [6], one of four main experiments in the LHC, is a general purpose experiment whose detectors measure position, time-of-flight, energy, and momentum in order to identify the particles. This is done through proton-proton, proton-nucleus, and nucleus-nucleus interactions. It is optimized for heavy-ion (Pb-Pb) reactions and is a very different design than the other three LHC experiments. Figure 2.2 shows an overview of the ALICE system.

Scientists believe that the Universe like we know it today once emerged from the Big Bang approximately fifteen billion years ago. In the first few millionths of a second the Universe was

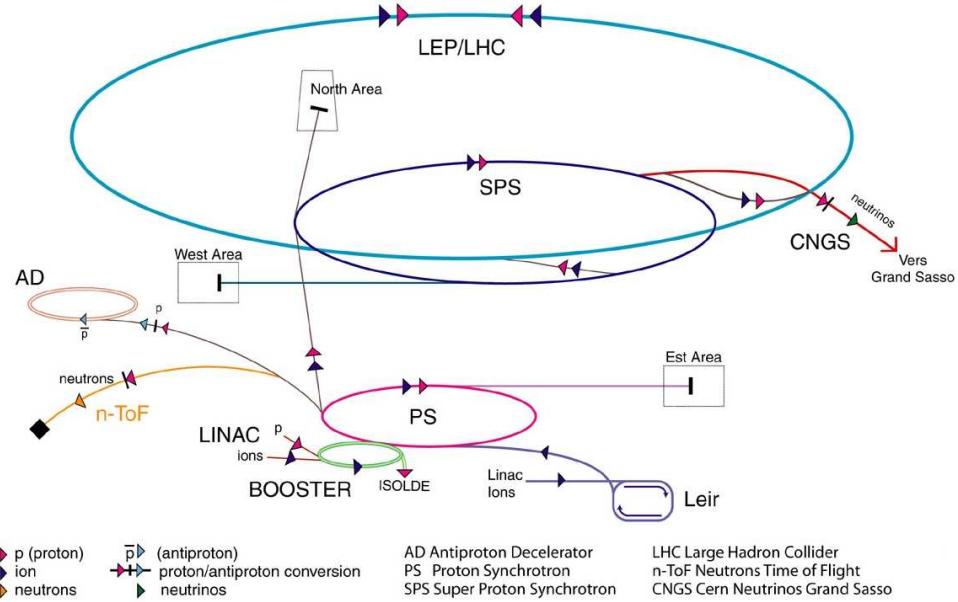


Figure 2.1: Schematic diagram giving an overview of all the accelerators at CERN [7]

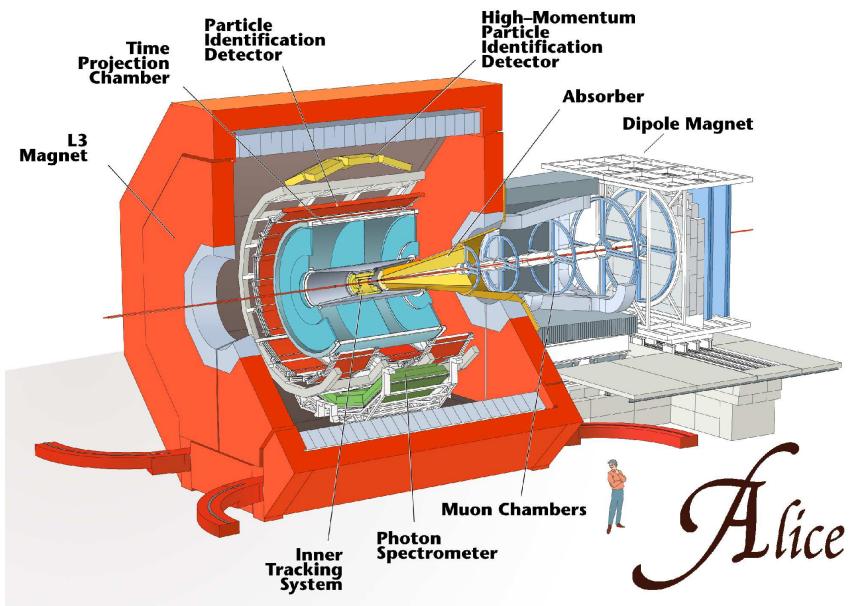


Figure 2.2: THE ALICE system [7][6]

compressed into a tiny volume. At this density the temperature would have been to high for the subatomic particles that make up an atom to stick together. The matter existing in this brief moment would be a plasma of free quarks and gluons<sup>1</sup>, Quark-Gluon Plasma. In the ALICE detector, a head-on collision of Pb+Pb particles will compress and heat the nuclei so that for a very short moment a large number of free quarks and gluons will exist. Creating this Quark-gluon plasma is therefore like looking back in time to the origin of the Universe. The lifetime of the QGP is very short and it will quickly cool down and transform into hadrons<sup>2</sup>. Thus observing if the QGP really is produced, is done by observing the particles sent out from the collision. A collision producing QGP will send out a different fingerprint of particles than a collision not producing QGP. The number of particles emitted from the collision is enormous. The ALICE detectors have to be able to track and identify particles from very low ( $\sim 100\text{MeV}/c$ ) up to fairly high ( $\sim 100\text{GeV}/c$ ) transverse momentum, to reconstruct short-lived particles such as hyperons, D and B mesons, and to perform these tasks in an environment of extreme particle density (up to 8000 charged particles per unit rapidity) [4]. The main challenge is therefore to separate the particle tracks and identify as many of the particles needed to confirm the creation of QGP.

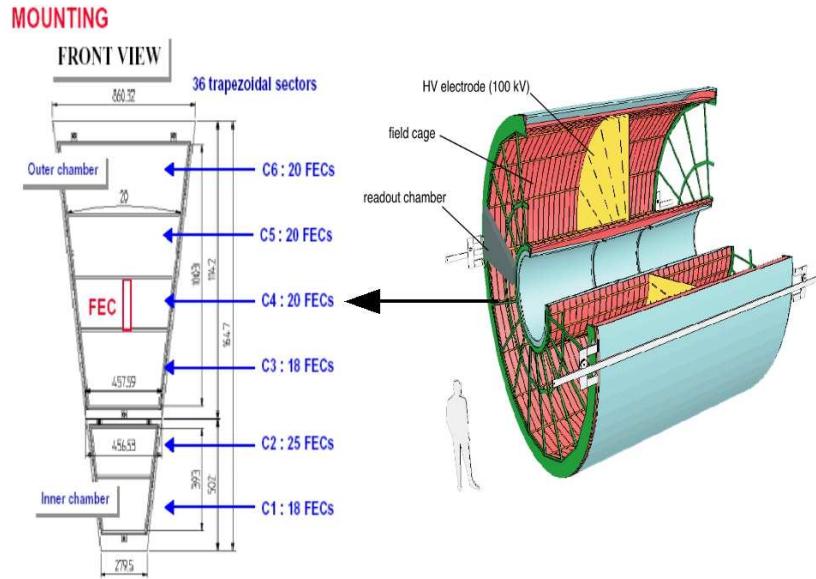


Figure 2.3: The Time Projection Chamber. Each end cap is divided into 18 regions and further subdivided into 6 sectors. Each sector has a number of front-end cards and is connected to the Readout Control Unit. Which in total makes 216 readout partitions.

<sup>1</sup>Quarks and gluons are the building blocks for protons and neutrons and other hadrons, which in turn make up the nucleus of an atom.

<sup>2</sup>Hadrons are particles made from quarks and gluons

### 2.1.1 TPC and the Front-End Electronics

The ALICE experiment consists of several different layers of sub-detectors where the Time Projection Chamber (TPC) [8] in figure 2.3 is the main tracking detector. It is a cylindrical design with an inner opening radius of about 80 cm, an outer radius of about 250 cm and an overall length in the beam direction of 500 cm. The volume TPC is filled with a gas mixture of 90% Ne and 10%  $CO_2$ . A high voltage central electrode sets up an electric field in each half of the TPC, and divides the TPC in to two drift regions. Charged particles traversing the TPC volume ionise the gas along their path, liberating electrons that drift in a straight line toward the detector end plates. The end plates consists of multiwire proportional chambers and have a grid of 570132 reception pads connected to the front-end electronics. Each end plate is divided into 18 regions and further sub-divided into 6 sectors. By detecting the arrival of electrons at the pads, it is possible to reconstruct the path of the original charged particles produced in the collisions.

The charged collected at the pads are passed on to 4356 front-end cards (FECs) for further processing before a complete readout takes place. The basic components of the front-end cards are charge sensitive amplifiers, filters and 10-bit ADCs. The readout takes place, at a speed of 200MB/s, through a 40-bit-wide backplane bus linking the front-end cards to the Readout Control Unit (RCU). Figure 2.4 shows the global architecture of the front-end electronics. The

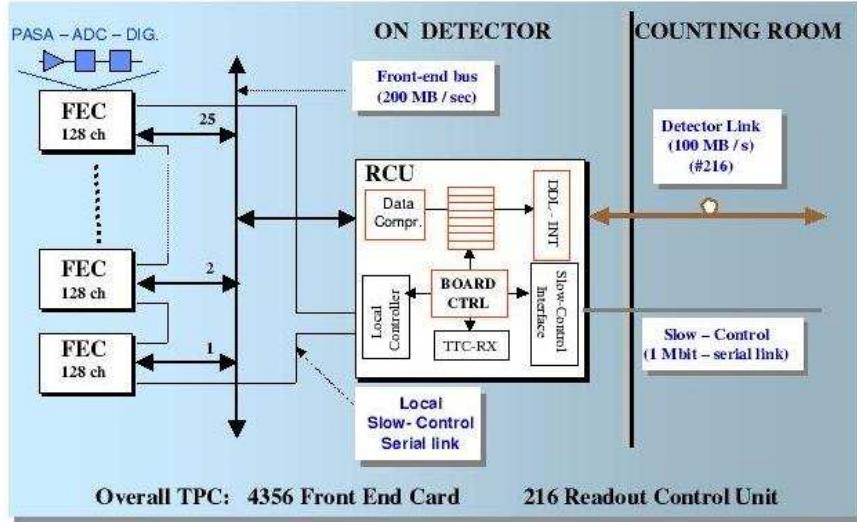


Figure 2.4: Global architecture of the front-end Electronics. Each TPC sector is served by 6 readout subsystems

readout is grouped in 216 readout partitions, one for each end cap sector, and controlled by the Readout Control Unit shown in figure 2.5(a) and 2.5(b).

#### Readout Control Unit

The Readout Control Unit [9] interfaces the front-end electronics of the TPC with the ALICE Data Acquisition, ALICE Central Trigger Processor, and the ALICE Detector Control System

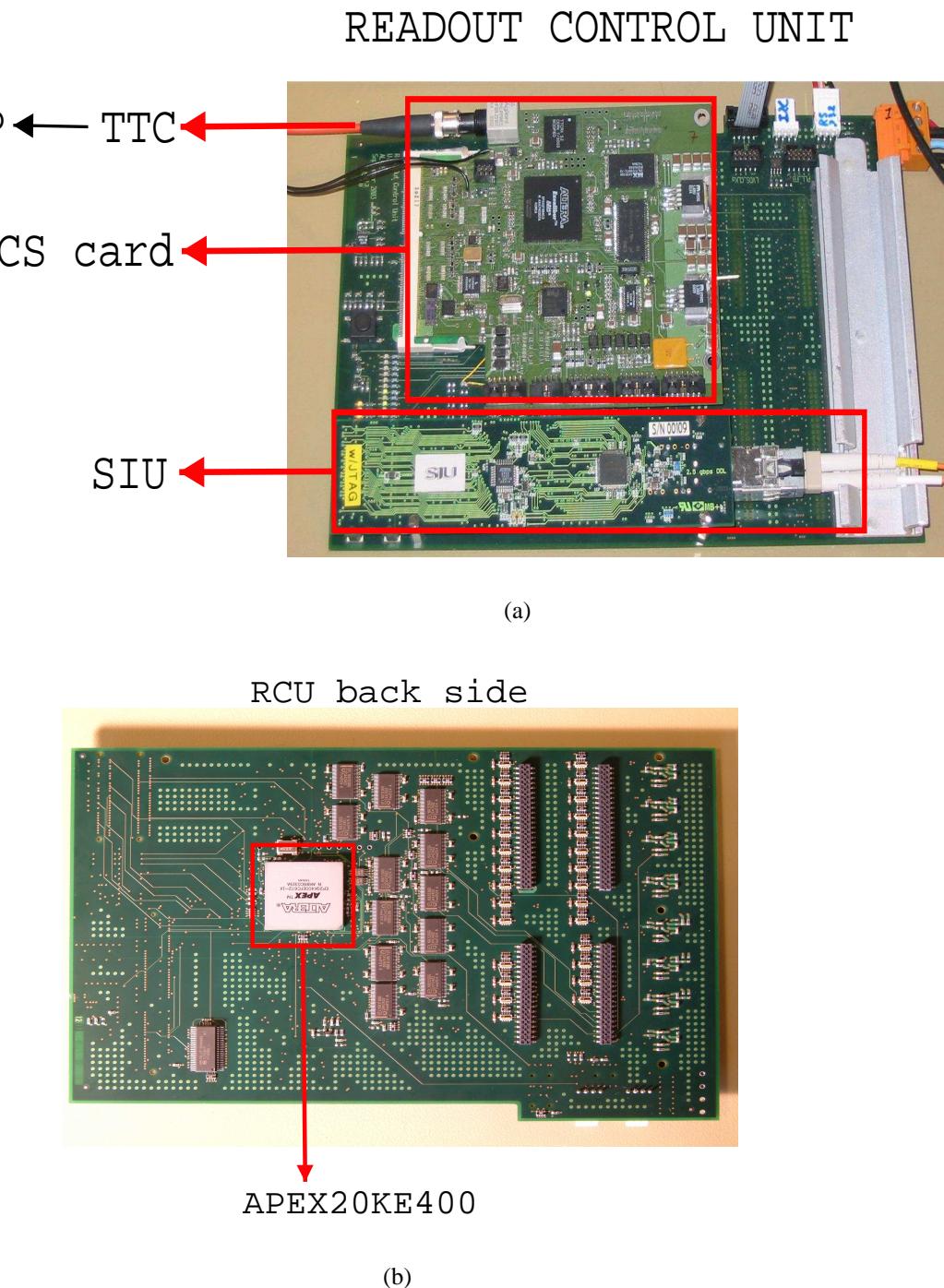


Figure 2.5: a) Readout Control Unit card, front side, with the DCS card, TTC card and SIU interface, b) Readout Control Unit card, back side, with the APEX20KE400

(DCS). It consists of three main modules, the RCU card, the DCS card, and the SIU interface module. When a complete readout is done, the RCU will send the data via the Data Detector Link (DDL) to the ALICE DAQ and High Level Trigger(farm of computers) in the counting room for further processing and track reconstructions. Figure 2.5(a) shows both the SIU Interface Module, which is the interface between the RCU and the DDL link, and the DCS mounted on the RCU card. The DCS supervises the operation of the detectors and the front-end readout electronics. It also provides the interface to the ALICE trigger system (TTC). On both the DCS and the RCU card an FPGA from ALTERA is the main controlling unit, in addition to several other circuits like SRAMs, DRAMs, FLASH RAMs, voltage regulators and buffers. All this electronics will be placed at the end plates of the TPC detector approximately 3-5 meters from the interaction point of the collisions. It will therefore be heavily exposed to the radiation produced in these collisions. Radiation shielding of the front-end electronics will not be possible, since it will create undesirable secondaries which will degrade the physics measurements of the experiment. It is therefore of concern that the electronic devices used in the front-end electronics are as radiation hard as possible, and this can only be determined by irradiation tests. Three prototypes

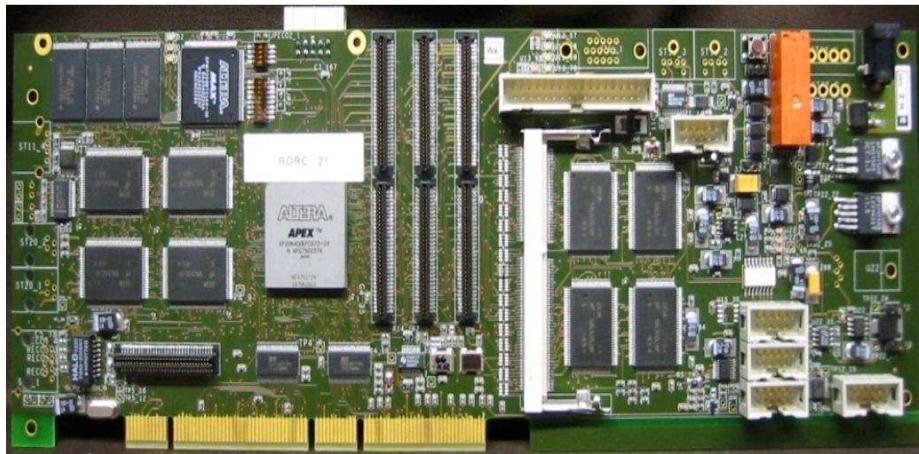


Figure 2.6: Readout Control Unit prototype II used in the irradiation tests with the ALTERA APEX FPGA

of the RCU card have been developed. Figure 2.5(a) shows the latest prototype III which will be used in the readout test of a full TPC sector in May 2004 at CERN. The test of all the major parts of the front-end electronics have been carried out using the prototype II card shown in figure 2.6.

# Chapter 3

## Radiation and semiconductor devices

*In the previous chapter the concerns about the radiation effects on the front-end electronics were introduced. High-energetic particles like for instance protons and neutrons pose a radiation risk to all electronic components. With the today smaller feature size and high density devices, this makes the electronics more vulnerable to this radiation. This chapter will present the radiation effects related to semiconductor devices, and an overview of the radiation levels expected in the proximity of the front-end electronics in the TPC [10]-[25]*

### 3.1 Radiation effects in semiconductor devices

Radiation effects in semiconductor devices can be divided in two main categories, cumulative effects and Single Event Effects (SEE). These are again divided into sub categories:

#### Cumulative effects

- Total Ionizing Dose (TID), ionisation
- Displacement damage, non-ionisation

#### Single Event Effects (SEE)

- Single Event Latchup (SEL)
- Single Event Upset (SEU)

#### 3.1.1 Cumulative effects

Cumulative effects are due to radiation effects accumulating over time due to the energy deposited by the radiation in the device. Ultimately it can lead to possible device failure.

##### Total Ionising Dose (TID)

Electronics can suffer long-term radiation effects, mostly due to electrons and protons. TID is the measurement of the energy dose deposited in the material in the form of ionisation. The ionisation of the material leads to a generation of electron-hole pairs. In presence of an electric field the pair can be separated and due to the very low mobility of the holes compared to the electrons, they can be trapped in the oxide. The electron will easily drift away, resulting in a net

positive charge in the oxide. If no electric field is present the electrons and holes will eventually recombine. Degrading the device due to high dose rates can cause the threshold for failure to decrease, leading to a higher SEU rate. TID is measured in Gray (Gy), but the old unit rad is also used, where 1 Gy = 100 rad.

### **Displacement damage**

Displacement damage is a non-ionising effect where the energy loss causes atoms to be displaced from their normal position in the lattice structure. It is not measured in any unit like for TID.

### **3.1.2 Single Event Effects**

Single event effects are radiation induced errors due to a single charged particle depositing energy through ionisation of the material. They are statistical in nature and are therefore treated in terms of their probability to occur. This is device specific and dependent of the nature of the incident particles. They can take the form of "hard" or "soft" errors depending of the consequence of the deposited energy. Single Event Effects are of great concern to the ALICE readout electronics since they can cause the electronics to fail at any time during operation.

#### **Single Event Latchup**

Single event latchups are "hard" errors, and are potentially destructive. Latchup occurs due to parasitic effects in the device triggered by the ionised energy deposited. This results in a short across the device and a current well above normal operation. Power needs to be removed at once to avoid destruction of the device due to thermal effects.

#### **Single Event Upset**

When a single charged particle strikes an integrated circuit device it deposits energy through ionisation of the silicon, and leaves behind a dense track of electron-hole pairs like in figure 3.1. Due their high mobility the newly created carriers (electrons) will easily drift if an electrical field is present and be collected at a nearby sensitive node, for instance at the drain of a CMOS transistor. If the deposited charge exceeds the critical charge for a transistor to change its logic state, this will cause a Single Event Upset or SEU. A SEU is a "soft" error, non-destructive, and a rewriting or reprogramming of the device will return the device to normal behaviour thereafter. In most cases protons do not deposit enough charge in order to cause a SEU. But, like neutrons, they can interact with the nuclei and create a heavy recoil ion through complex nuclear interactions. The short range heavy recoil ion produced in the interaction is capable of ionising the material and cause a SEU. This type of interaction will be described in further detail in section 3.2. Figure 3.2 shows how a proton hits a silicon nuclei in the transistor and "kicks" out the heavy recoil ion which in turn ionizes the material.

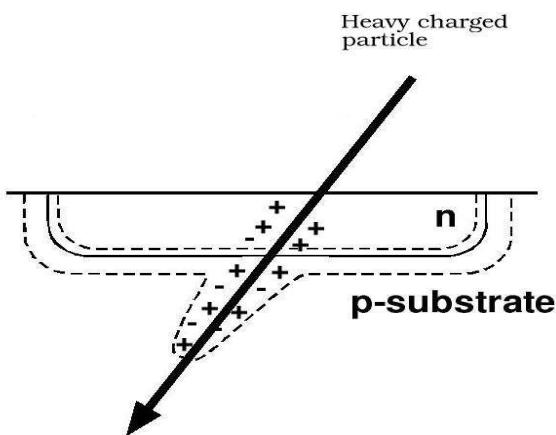


Figure 3.1: Ionising of a sensitive n-type node

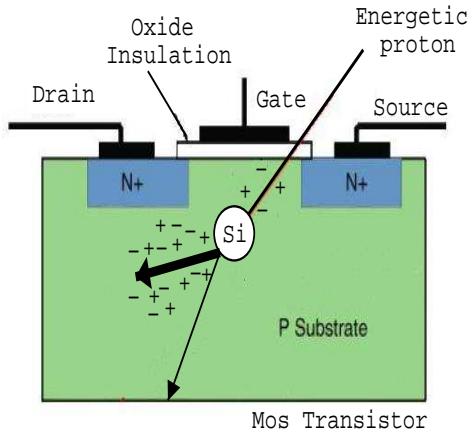


Figure 3.2: High energetic proton interacts with a Silicon nucleus and creates secondary particles and a short range heavy recoil ion capable of ionising the material and cause an SEU

## 3.2 Interaction of radiation with matter

Radiation is the transmission of energy through space or matter in the form of high speed particles and electromagnetic waves. Electromagnetic waves is radiation we encounter every day in visible light, radio waves, ultra-violet (UV) waves, and microwaves. How radiation interacts with matter can be divided in two main groups:

### Charged radiation

- Heavy charged particles (*Alpha ( $\alpha$ ) particles, protons, heavy ions*)
- Light charged particles (*Beta ( $\beta$ ) particles*)

### Neutral radiation

- Neutrons
- Photons (*x-rays, Gamma ( $\gamma$ ) rays*)

It is also normal to distinguish between *ionising radiation* and *non-ionising radiation*. When an electrically neutral atom loses an electron it becomes a positively charged ion. For this to occur the radiation striking the atom must deposit sufficient energy to remove the tightly bound electrons from their orbits, an energy greater than the binding energy of the electron. Ionisation creates an ion pair, which is the free electron and the positively charged atom from which the electron was removed. Non-ionising radiation is radiation with energies not sufficient to remove the same orbital electrons.

When a particle passes through matter, some or all of its energy is passed on to the material. How the particle interacts with the material is dependent of its energy, mass, charge, and the type

of material it passes through. The behaviour of charged particles ( $\alpha, \beta p$ ) passing through matter is fundamentally different from that of the neutral radiation ( $n, \gamma$ ).

*Neutrons* are neutral particles that are normally contained in the nucleus of all atoms. Since neutrons do not carry electric charge they do not directly ionise the material they hit. Neutrons can travel through many centimeters of matter without any type of interaction. However, a neutron can interact with the nucleus of the absorbing material and create a heavy recoil ion through complex nuclear interactions. The heavy recoil ion is in turn capable of ionising the device material.

*Gamma rays* and *X-rays* are examples of electromagnetic radiation, and differ only from radio waves and visible light in having much shorter wavelengths. They have zero rest mass, no charge, and travel with the speed of light. Gamma rays interact with matter by three basic processes:

1. photo electric effect
2. Compton scattering
3. pair production

### 3.2.1 Charged particles and specific energy loss

A heavy charged particle strongly interacts with the orbital electrons of the material which through it travels. It is affected by the coulomb interaction forces between its positive charge and the negative charge of the orbital electrons within the absorber atoms. At low energies the repulsive electric force, coulomb barrier, will prevent the the particles from entering into reach of the nuclear forces. Unless the particle is highly relativistic, ionisation is the main contribution to the energy loss for a charged particle. For particles of higher energies, the nuclear forces will become of increasing importance.

The products of a single ionizing event are called an electron-ion pair. The amount of energy required to create an ion pair,  $w_{ehp}$ , is material dependent. For silicon it is  $w_{ehp} = 3.6\text{eV}$ , and the density is  $\rho = 2.33\text{g/cm}^3$ . A conversion factor between charge and energy is then

$$\frac{w_{ehp}}{q}(Si) = \frac{3.6 \cdot 10^{-6} \text{ MeV/ionpair}}{1.6 \cdot 10^{-7} \text{ pC/ionpair}} = 22.5 \frac{\text{MeV}}{\text{pC}} \quad (3.1)$$

Table 3.1 lists a few material properties for some semiconductors and insulators.

*Specific energy loss*, also called stopping power, of a charged particle is defined as the differential energy loss for that particle within the material divided by the corresponding differential path length:

$$S = \left( \frac{dE}{dx} \right)_{tot} = \left( \frac{dE}{dx} \right)_{col} + \left( \frac{dE}{dx} \right)_{nuc} \quad (3.2)$$

where  $(dE/dx)_{col}$  is the energy loss due to coulomb interaction (ionisation and excitation), and  $(dE/dx)_{nuc}$  is the energy loss due to the nuclear interactions. The amount of energy lost through

Table 3.1: Properties of air, intrinsic germanium, silicon, gallium arsenide, and silicon dioxide at 27C [10]

Material	Air	Ge	Si	GaAs	$SiO_2$
Type	insulator	semiconductor	semiconductor	semiconductor	insulator
Atomic weight	-	72.6	28.09	144.63	60.08
Density [ $g/cm^3$ ]	$1.20 \cdot 10^{-3}$	5.33	2.33	5.32	2.27
$w_{ehp}$ [eV]	34	2.8	3.6	4.8	17

coulomb interaction by the particle per unit path length is called the *linear energy transfer* (LET), and is equivalent to the term  $(dE/dx)_{col}$ . LET is often defined with respect to the material density ( $\rho$ ) so that

$$LET = \frac{dE}{dx} \left[ \frac{\text{MeV}}{\text{mg}/\text{cm}^2} \right] \quad (3.3)$$

According to the *Bethe-Bloch formula*[14],

$$-\frac{dE}{dx} = \frac{4\pi e^4 z^2}{m_0 v^2} N B \quad (3.4)$$

where

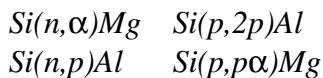
$$B \equiv Z \left[ \ln \frac{2m_0 v^2}{I} - \ln \left( 1 - \frac{v^2}{c^2} \right) - \frac{v^2}{c^2} \right]$$

specific energy loss is:

$$\frac{dE}{dx} \propto \frac{ez^2}{v^2} \quad (3.5)$$

where  $v$  and  $z$  is the velocity and atomic number of the primary particle,  $N$  and  $Z$  are the number density and atomic number of the absorber atoms,  $m_0$  is the electron rest mass, and  $e$  is the electronic charge. When comparing different charged particles of the same velocity the only factor that may change is the  $z^2$ . Therefore, heavy charged particles will have the largest specific energy loss. Figure 3.3 shows the variation of the specific energy loss for a number of different charged particles over a wide range of energy. When the energy increases, to where the particles velocities approaches the velocity of light, the  $dE/dx$  approaches a near-constant minimum value. Because of the particles similar energy loss at these values, they are often referred to as "minimum ionising particles". At low energies the *Bethe-Bloch formula* indicates an increase in specific energy loss, before the  $dE/dx$  curve at sufficiently low energies reaches a maximum and starts decreasing. Theoretical energy loss in silicon are shown in figure 3.4(a) for some typical ion species, and in figure 3.4(b) for protons, and figure 3.5 shows the specific energy loss for protons in silicon.

At the LHC the heavy ions will be produced by hadronic interactions, mainly induced by high energetic protons, pions and neutrons:



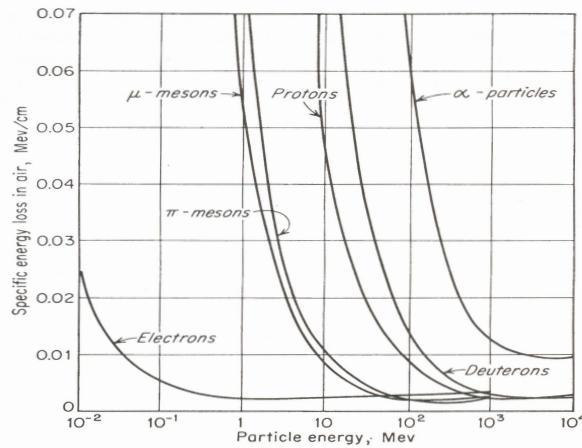


Figure 3.3: Variation of the specific energy loss in air versus energy of the charged particles shown [14]

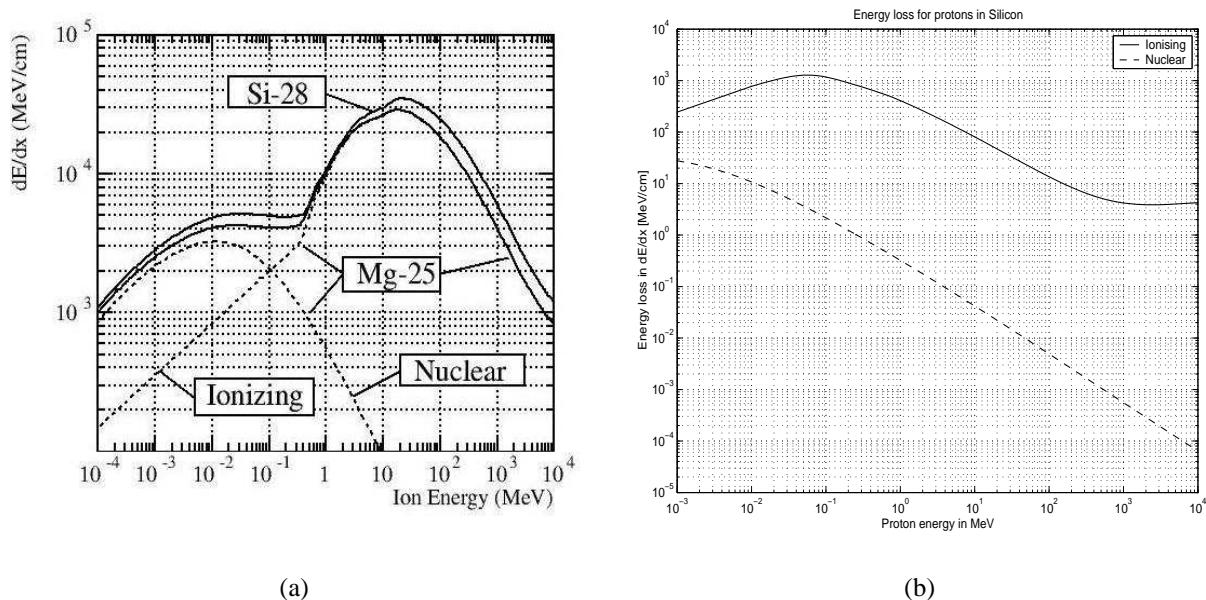


Figure 3.4: Energy loss in silicon ( $\rho = 2.33 \text{ g/cm}^3$ ) as a function of kinetic energy for some ion species 3.4(a) [16] and protons 3.4(b) [13]

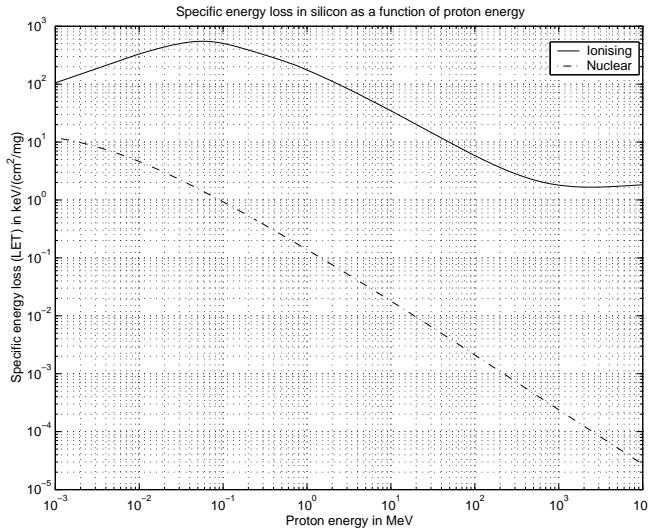


Figure 3.5: Specific energy loss, LET, for protons in silicon [13]

Table 3.2: This table gives some theoretical values for peak LET, the range for peak LET, the energy for peak LET, and range and LET at 10 MeV for protons and some typical recoil ions

Particle		Al-27	Mg-24	Si-28	Proton
Peak LET	[MeV/mg/cm²]	13.37	12.18	14.57	0.55
Range	[μm]	8.29	7.52	8.45	62.8
Energy	[MeV]	20.26	16.74	22.46	0.055
LET at 10 MeV	[MeV/mg/cm²]	12.66	11.82	13.54	0.035
Range at 10 MeV	[μm]	4.95	5.13	4.7	711(7 mm)

The recoil ions have rather low energies, rarely exceeding 10 MeV. Thus their range is very limited (below 10 μm), which means that they have to be produced locally and near to the sensitive area in order to induce a SEU [16]. Using reference [18] and [13], the peak LET and corresponding range have been calculated for protons and some typical ions. Table 3.2 shows that the heavy ions have a higher energy deposition and shorter range in silicon than a proton. Protons have a maximum ionisation energy of about 5% of the recoil ions. This maximum value corresponds to a proton energy of 55 keV, and a further increase in proton energy gives a decrease in LET. As the kinetic energy of protons increases the absorption of the particles energy through strong interaction processes the nucleus will become more dominant.

### Simple approach for sensitive volume and LET

The device immunity is determined by its linear energy transfer threshold ( $LET_{th}$ ). It is defined as the minimum LET that can cause a single event effect. Consider a simple capacitor upon which the incoming ion deposits sufficient charge  $Q$  to result in a voltage change. The  $LET_{th}$  is equivalent to the LET required to produce such a voltage change,  $\Delta V$ , and cause an SEU.

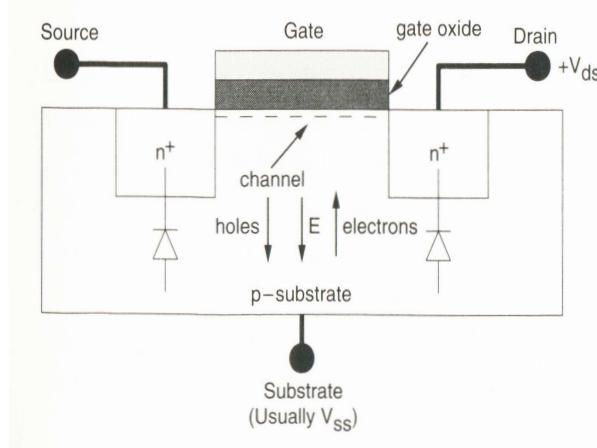


Figure 3.6: Physical structure of an NMOS transistor[25]

$$LET_{th} \propto \Delta V = Q_{crit}/C \quad (3.6)$$

In other words, there is a minimum charge that must be deposited in the node in order to cause an upset. This minimum charge is called the critical charge ( $Q_{crit}$ ). Figure 3.6 shows the structure of a standard NMOS transistor. In operation, a positive voltage is applied between the drain and the source. A voltage applied to the gate, which is positive with respect to source and the substrate, produces an electric field  $E$  across the substrate, which attracts electrons toward the gate oxide. If the gate voltage is sufficiently large, larger than the threshold voltage needed to turn the transistor "on", the region just below the gate oxide changes from p-type to n-type due to the accumulation of attracted electrons. The surface of the underlying p-type silicon is said to be inverted. This provides a conduction path(channel) between the source and drain, and a current starts to flow in the channel due to the voltage applied between drain and source. A gate-source voltage just below the threshold voltage, will not attract enough electrons to form a channel and turn the transistor "on". However the electric field sets up a depletion region where the holes are repelled and the electrons are swept over. This depletion region extends out below the channel and around the drain and source.

Consider a charge particle travelling through the transistor leaving behind a dense track of electron-hole pairs. Some of the pairs will recombine, but a considerable amount of the electrons will be swept over the depletion region and accumulate below the gate oxide. If the ionising particle has deposited enough charge so that a channel will form, the drain-source voltage will attract the accumulated electrons toward the drain. Hence a current is induced in the channel and the transistor turns "on" for a brief moment. A Single Event upset has occurred.

According to [16], the SEU occurrence depends on two parameters:

1. The Sensitive Volume (SV) within which the ionisation has to take place for the charge to be collected on the node.

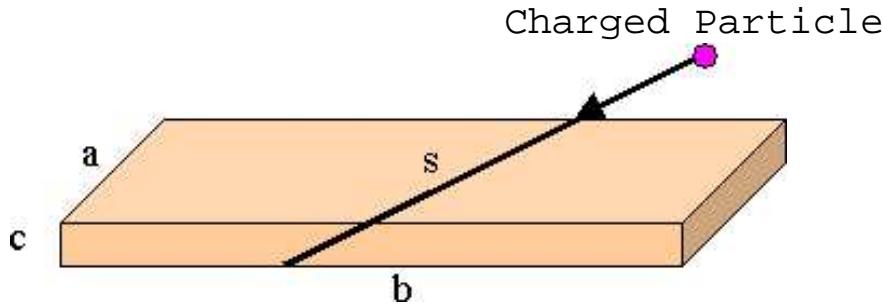


Figure 3.7: A parallelepiped of dimensions  $a, b, c$  where  $c$  is the device depth.  $s$  is the path length of the particle

2. The Critical Energy ( $E_{crit}$ ) which has to be exceeded by the deposited ionising energy within the SV in order to trigger an upset .

Where  $E_{crit} \propto Q_{crit}$ . A simple approach to the sensitive volume is to use the parallelepiped shown in figure 3.7 as the medium of which the charged particle travels through. The LET threshold will correspond to the maximum travel length possible.

$$s_{max}^2 = a^2 + b^2 + c^2 \quad (3.7)$$

Total energy deposited by a particle traversing the material is

$$E_{dep} = LET \cdot s \cdot \rho \quad (3.8)$$

where  $s$  is the length travelled and  $\rho$  is the density of the material. Similar the deposited charge is

$$Q_{dep} = \frac{E_{dep} \cdot q}{w_{ehp}} = \frac{LET \cdot \rho \cdot s \cdot q}{w_{ehp}} \quad (3.9)$$

As mentioned the sensitive volume is crucial for the critical energy and and threshold LET. The critical charge  $Q_{crit}$  has been measured for a number of IC technologies to be:[10]

$$Q_{crit} = (0.0023 pC/\mu m^2) L^2 \quad (3.10)$$

where  $L \times L$  is the sensitive area. In other words  $Q_{crit} \propto L^2$ . This is because the deposited charge will drift in a vertical electric field toward the inversion region of a transistor, having a cross-section of  $L \times L$ , or  $W \times L$  if the width is different from the length. The sensitive area will probably extend over the whole depletion region of the transistor. For a transistor, the critical charge will be dependent on the capacitance over the gate oxide and other parameters related to the threshold voltage. For an ionising particle the deposited charge is dependent on the length of the path which the particle travels. Thus if enough energy can be deposited to exceed the critical energy, depends not only on the sensitive area but also of the thickness of it. In other words the sensitive volume. Re-arranging equation 3.9 and exchanging  $Q_{dep}$  by  $Q_{crit}$  and  $s$  by  $s_{max}$ , we get an expression for the  $LET_{th}$

$$LET_{th} = \frac{Q_{crit} \cdot w_{ehp}}{\rho \cdot s_{max} \cdot q} \quad (3.11)$$

where  $s_{max}$  is the maximum possible path where the particle can deposit energy within the sensitive volume. Figure 3.8 shows the threshold LET as a function of the feature length  $L=a=b$ , and depths  $c$  of the sensitive area.

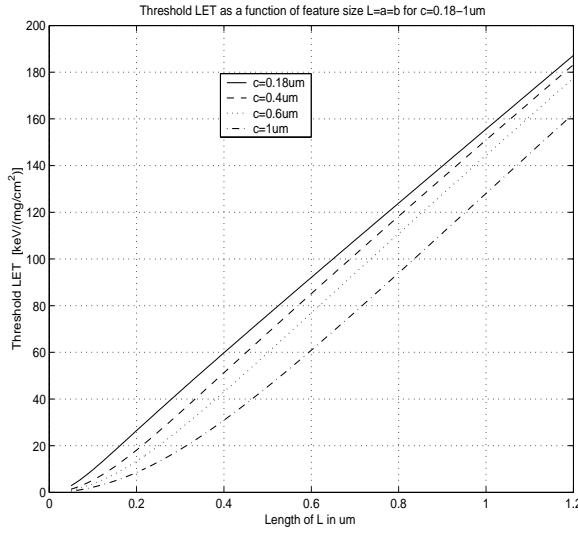


Figure 3.8: Threshold LET plotted as a function of  $L=a=b$  for different depths,  $c$ , of the sensitive area. Calculated using equation 3.8 and 3.7 and reference [18]

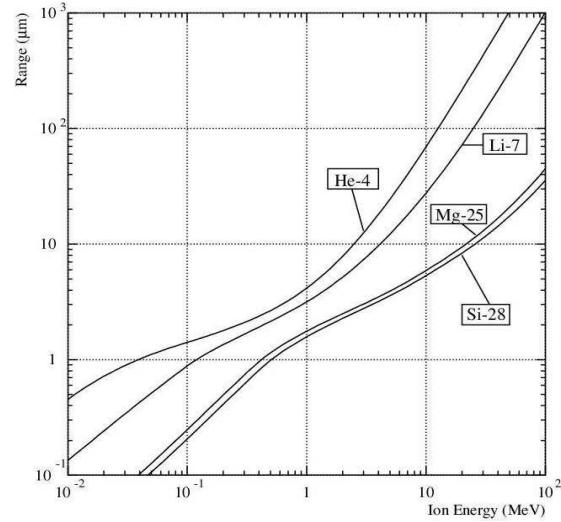


Figure 3.9: Range of a few ion types in silicon [16]

### 3.2.2 Practical SEU calculation, Cross-Section

The influence of a particle in the material is measured by its energy  $E$  [eV] and its flux [ $1/\text{s} \cdot \text{cm}^2$ ]. The flux is the number of particles passing through a unit area ( $1\text{cm}^2$ ) during one second. Integrating the flux over the time gives the fluence, [ $1/\text{cm}^2$ ]. The device SEU sensitivity is characterized by its cross-section. The cross-section is normally measured by irradiating the DUT by a known particle flux, most often with protons or heavy ions. In the case of proton irradiation, the cross-section is calculated as the ratio of the number of SEU over the proton fluence, and is plotted as a function of the proton energy.

$$\sigma = \frac{\text{No. of SEU}}{\text{Flux} \cdot \text{Time}} = \frac{\text{No. of SEU}}{\text{Fluence}} \quad (3.12)$$

Figure 3.11 shows an example of a simulated cross-section curve, where the SEU cross-section varies as a function of the critical energy and sensitive area. The simulations are based on a lattice of sensitive areas, where the sensitive volume sizes used are  $1 \times 1 \times 0.5$ ,  $1 \times 1 \times 1$ ,  $1 \times 1 \times 2$  and  $2 \times 2 \times 2 \mu\text{m}^3$  [16]. For the APEX 20K used in this thesis the minimum technology is  $0.18\mu\text{m}$  [33]. However the deposited charge from a heavy ion travelling through the transistor is collected from

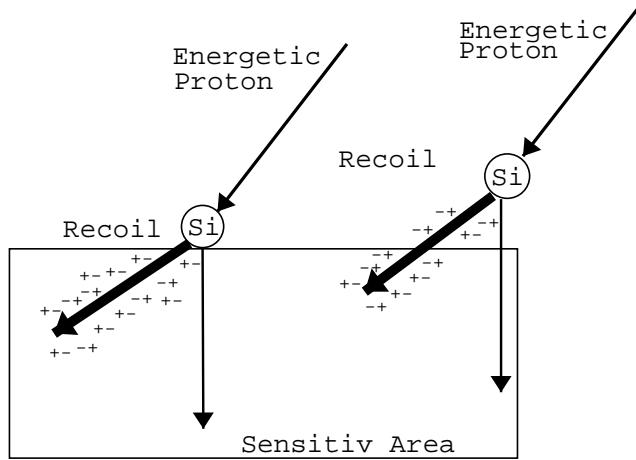


Figure 3.10: Figure showing one silicon nuclei hit by a high-energetic outside the sensitive area and one at the boarder of the sensitive area, and thus the recoils will deposit a different amount of charge..

outside the inversion and depletion region as well. How far this sensitive area extends is very hard to estimate for a given technology.

Looking at the cross-section plot in figure 3.11, it seems like the SEU cross-section may be showing a small increase with decreasing proton energy at low values of critical energy. Increasing the critical energy, the cross-section starts to show a larger dependency on the proton energy for all different sizes of SV. When the critical energy increases the ion must deposit more energy in order to cause an SEU. In the case of two recoil ions of the same energy, one produced outside the SV and one produced inside, as sketched in figure 3.10, they will deposit different amounts of energy within the SV. The recoil ion produced inside the SV will therefore be able to cause an SEU for a higher critical energy. Thus as the critical energy increases, less recoils will be able to cause an SEU, resulting in a decrease in the overall cross-section as seen in figure 3.11. The increase at low proton energies for very small  $E_{crit}$  and large SV might be due to direct ionisation of the incident proton. Figure 3.14 shows a simulated energy spectra of recoils for various incident neutron energies above 20 MeV. The maximum energy of the recoils increases with the energy of the incident neutron. For proton and neutron energies around 20 MeV , the recoils have typical energies of 0.5 to 3 MeV, at 200 MeV the range extends to about 6 MeV. Figure 3.12 shows that there is a small difference in the proton induced cross-section and the neutron induced cross-section for low energies, and as the energy of the incident proton or neutron increases this difference decreases. Thus when incident energies exceeds a few tens of MeV protons and neutrons can be considered to give similar radiation effects. The energy loss curve for  $^{28}Si$  in figure 3.4(a) shows that the LET will be at its highest around 20 MeV. The production probability of fragments (nuclear cross-section) has to be folded with the energy loss of the corresponding recoils which results in an almost constant rate of SEUs as a function of the incident proton or neutron energy.

As the proton energy decreases the inelastic cross-section decreases due to the coulomb barrier, and below 10-20 MeV the protons do no longer contribute to the SEU cross-section through

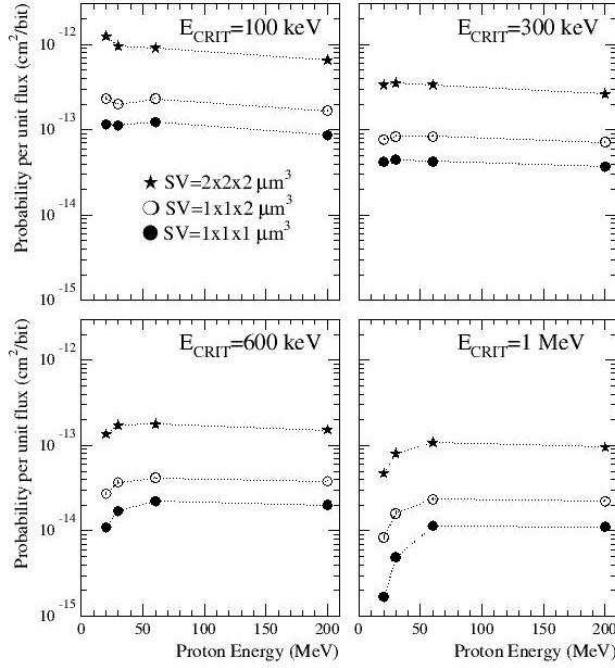


Figure 3.11: Variation of the SEU cross-section as a function of  $E_{crit}$  and sensitive area sizes[16]

nuclear interactions. Thus a threshold level will be reached for which below no SEUs will occur.

Figure 3.13 shows a cross-section results for heavy ion beam testing of the ALTERA 20K device. The LET threshold fit parameter is given as 0.1 MeV/mg/cm<sup>2</sup>. It shows that there is a threshold level for decreasing LET values and thus that the device has a critical energy. Saturation levels are reached at LET values of 5-10 MeV/mg/cm<sup>2</sup> [19].

The objective of irradiation tests are in fact to confirm this cross-section behaviour for the device of interest, and to estimate the SEU sensitivity of that device from the measured cross-section. By multiplying the cross-section value by the number of particles, flux, expected in the radiation environment of concern, this gives the probability of having a SEU per second. Also, by comparing the shape of the cross-section curve and saturation value with the plots in figure 3.11, a rough estimation of the critical energy and sensitive area for the device can be made.

For the front end electronics and the RCU in particular, the SEU upset rate is estimated as upsets per run, where a run period in ALICE is 4 hours.

$$\text{No. of SEU per run} = CS \cdot \text{flux} \cdot \text{time} \cdot \text{no. of FPGAs} \quad (3.13)$$

where  $CS$  is the cross-section saturation value,  $\text{time}$  is the time of a run, and  $\text{no. of FPGAs}$  is the number of FPGAs in the front-end electronics. However in order to do this calculation it is necessary to map the radiation environment which the electronics will be exposed to. Only then it is possible to estimate a realistic flux value for use in equation 3.13

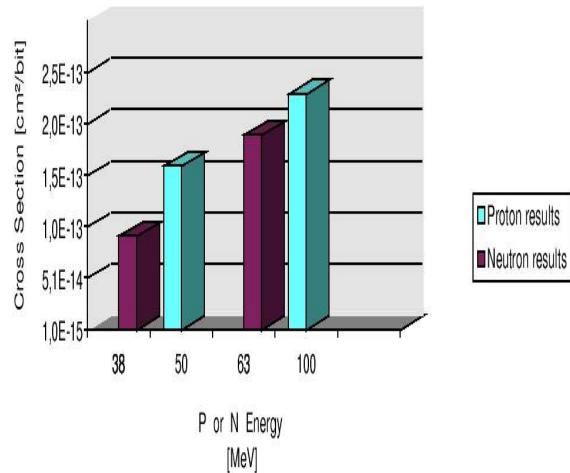


Figure 3.12: Proton and neutron irradiation results for Hitachi 512Kx8 SRAM [17]

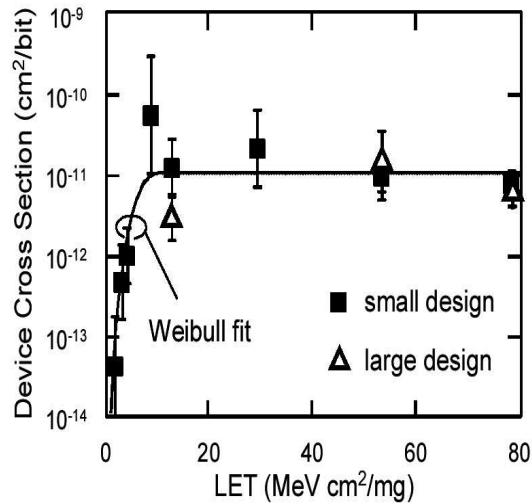


Figure 3.13: Device cross-section for heavy ion beam testing of the APEX 20K400E[19].

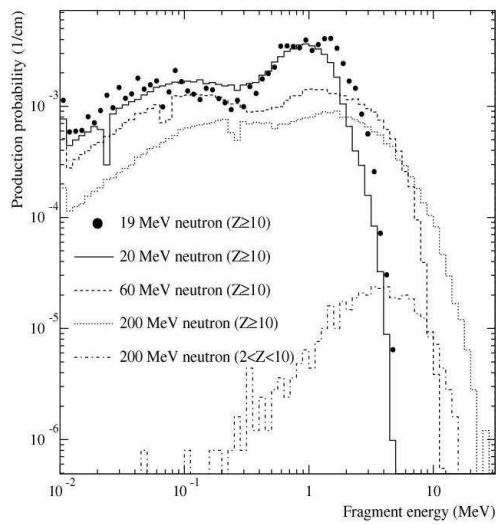


Figure 3.14: Fragment energy spectra from  $n-^{28}\text{Si}$  scattering at energies above 20 MeV [16]

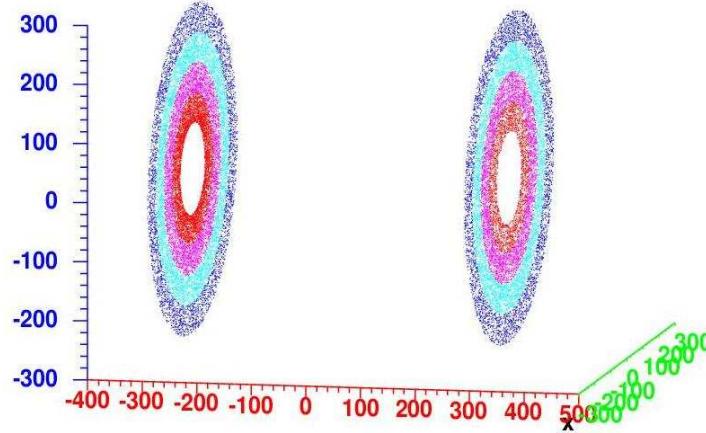


Figure 3.15: Scoring regions of the end plates[2]

### 3.3 Radiation level in the ALICE TPC electronics

The main focus of the ALICE experiment is to study Pb-Pb collisions at nucleus-nucleus center-of-mass energy of 5.5 TeV. This high beam energy combined with high luminosities ( $10^{27} \text{ cm}^{-2} \text{s}^{-1}$ ) result in high primary particle multiplicities.

Due to the high energies, the radiation inflicted on the electronics will be more critical than ever before. It is therefore necessary to have a good understanding of the radiation environment within which the electronics will be placed. Detailed particle transport simulations are needed to help the system designer to evaluate the risk of radiation damage to the electronics, and to implement the necessary precautions to prevent system failure due to radiation effects.

The TPC surrounds the Inner Tracking System (ITS) and is the main tracking detector of the central barrel. It is a cylindrical design with an inner radius of about 80 cm, an outer radius of about 250 cm, and an overall length in the beam direction of about 250 cm. A gas mixture of 90% Ne and 10% CO<sub>2</sub> has been chosen for operating the detector. The front-end electronics will be situated at the readout chambers approximately 10 cm from the end caps of the TPC. Simulation of the ALICE radiation levels is preformed using the FLUKA transport code. It has a full treatment of low and high energy nuclear, hadronic and electromagnetic physics processes and provides similar accuracy for the radiation due to hadrons, muons, electrons, photons and low energy neutrons [2]. The FLUKA transport code contains all the geometrical data of the TPC, and each end cap is divided into 4 concentric cylindrical layers of silicon as shown in figure 3.15, called scoring regions. The scoring region extends from 77 cm to 278 cm in radial distance from the center. Outer radial distance for regions 1 to 4 is respectively 127 cm, 177 cm, 227 cm and 278 cm. Figure 3.16 shows the geometry of the central detector as implemented in FLUKA. Two studies are preformed, one for each end cap referred to as the  $\mu$ -absorber and non-absorber side. The geometry of the TPC is not symmetrical due to the muon absorber on one side. The effect of this muon absorber can be seen in the neutron plot in figure 3.17(b). While absorbing hadrons, it will produce extra neutrons. In figure 3.17 the plots of the kinetic

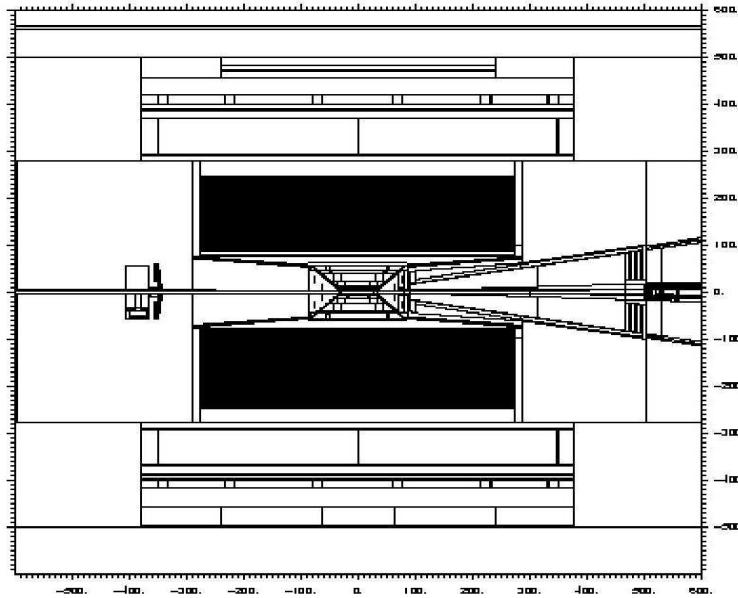


Figure 3.16: Geometry of the TPC, vertical cross-section[2]

energy spectrum of neutrons, protons, pions, and kaons are shown. They are plotted for one central event. Considering particularly flux, causing single event upsets, the main radiation components of concern are the high-energetic hadrons that can induce nuclear reactions in the silicon (with  $E > 20$  MeV - protons, neutrons, pions, kaons). Heavy recoil ions produced in these reactions are able, through ionisation of the material, to cause single event effects in the electronic devices. Figure 3.17 shows the kinetic energy spectrum of neutrons, protons, pions, and kaons simulated for one central event. The simulation is based on minimum bias events with average multiplicity of 80000 primary particles. Figure 3.17(a) shows that the proton distribution peaks at 100-200 MeV, and thus will contribute to the nuclear interactions in the silicon. For neutrons, figure 3.17(b), the peak is around 1 MeV, but a considerable amount of neutrons have energies above 20 MeV and have to be considered. Intermediate energy neutrons ( $2 \text{ MeV} < E < 20 \text{ MeV}$ ) are considered to contribute with less than 10% to the potential damaging radiation [16]. And it is further expected that thermal neutrons will have almost no effect on the electronics. Table 3.3 and 3.4 lists the particle fluxes for the particles of interest for the different cylindrical layers on the  $\mu$ -absorber side and the non-absorber side. Flux values for the particles with  $E_{\text{kin}} > 10 \text{ MeV}$  are added up to get the total estimated flux within each respective layer.

The cross-section plotted for  $E_{\text{crit}} = 1 \text{ MeV}$  in figure 3.11 shows that the curve starts to drop for protons below 60 MeV. However the energy threshold and saturation value of the cross-section depend on details of the device structure and sensitive area in particular. It is expected that a threshold level will be located somewhere around 10-20 MeV. 30 MeV protons, which are available at the OCL, will probably be located close up to the knee of the cross-section curve, a factor 2-3 off the saturation level. Irradiation at an energy above 60-100 MeV can confirm this. Also the proton distribution peak around 100 - 200 MeV in the TPC favour the use of the 180

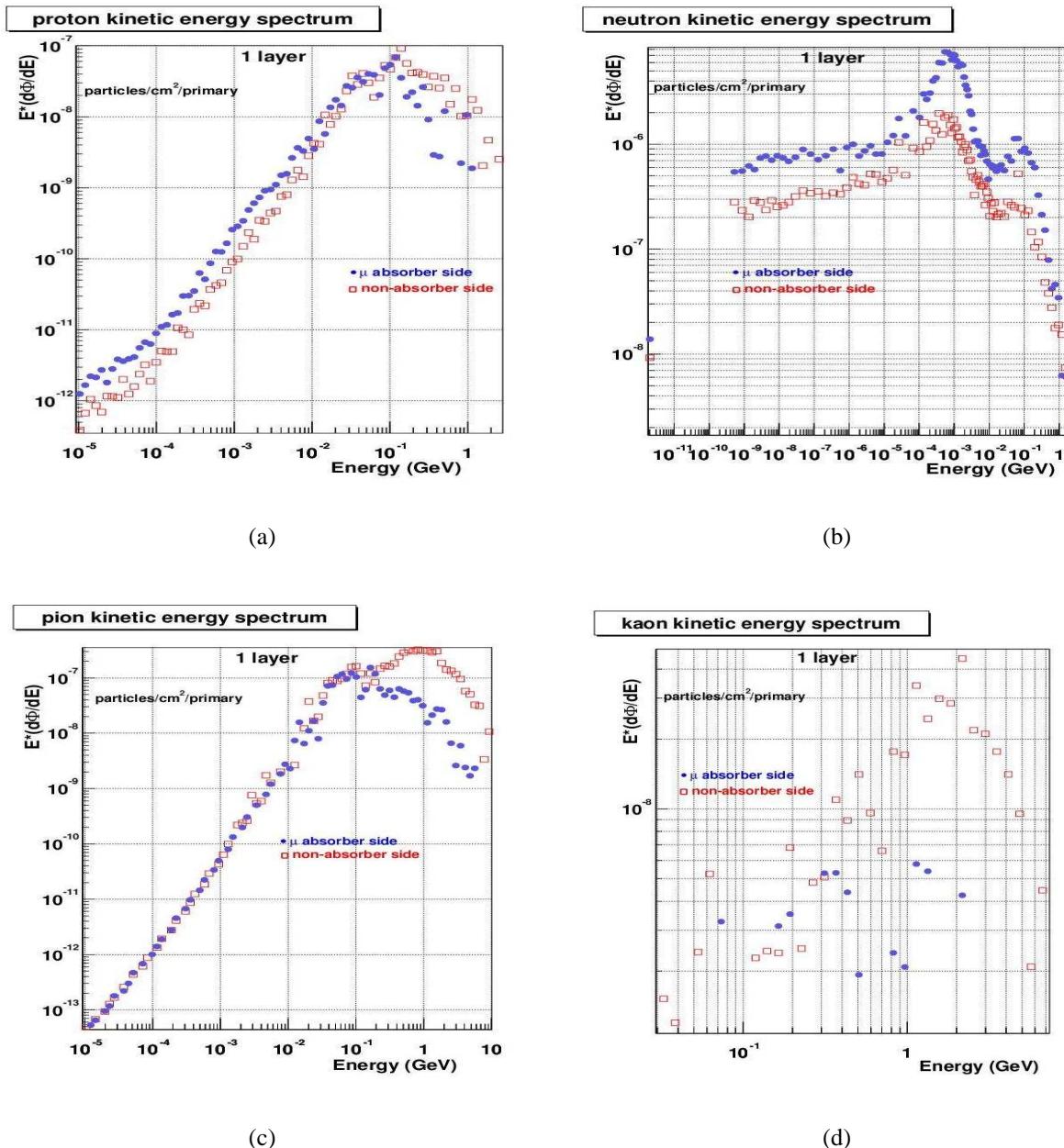


Figure 3.17: Energy spectra of produced particles for one central event.[2]

Table 3.3: Particle fluxes (particles/cm<sup>2</sup>/s) for minimum bias Pb-Pb running (**absorber side**)[2]

Layers	<b>1</b>	<b>2</b>	<b>3</b>	<b>4</b>
Neutron Flux [cm <sup>-2</sup> s <sup>-1</sup> ]	4377.6±1.6%	3289.6±0.3%	2726.4±0.9%	2368±0.5%
Neutron Flux [cm <sup>-2</sup> s <sup>-1</sup> ] with E <sub>kin</sub> > 10 MeV	334.1	204.8	134.4	959
Proton Flux [cm <sup>-2</sup> s <sup>-1</sup> ]	13.2±26.7%	7.7±6.9%	5.0±10.6%	5.1±10.6%
Proton Flux [cm <sup>-2</sup> s <sup>-1</sup> ] with E <sub>kin</sub> > 10 MeV	12.7	7.5	4.9	5.0
Pion <sup>±</sup> Flux [cm <sup>-2</sup> s <sup>-1</sup> ]	37.46±5.7%	55.9±3.1%	47.5±2.4%	28.5±2.8%
Pion <sup>±</sup> Flux [cm <sup>-2</sup> s <sup>-1</sup> ] with E <sub>kin</sub> > 10 MeV	37.2	55.8	47.5	1.3
Sum Flux with E <sub>kin</sub> > 10 MeV	384	268	187	129

Table 3.4: Particle fluxes (particles/cm<sup>2</sup>/s) for minimum bias Pb-Pb running (**non-absorber side**)[2]

Layers	<b>1</b>	<b>2</b>	<b>3</b>	<b>4</b>
Neutron Flux [cm <sup>-2</sup> s <sup>-1</sup> ]	1625.6±1.3%	1638.4±2.1%	1625.6±1.2%	1626±1.3%
Neutron Flux [cm <sup>-2</sup> s <sup>-1</sup> ] with E <sub>kin</sub> > 10 MeV	111.4	74.2	57.2	45.6
Proton Flux [cm <sup>-2</sup> s <sup>-1</sup> ]	19.5±9.6%	9.2±11.5%	8.1±19.3%	4.6±8.5%
Proton Flux [cm <sup>-2</sup> s <sup>-1</sup> ] with E <sub>kin</sub> > 10 MeV	19.2	9.1	7.9	4.5
Pion <sup>±</sup> Flux [cm <sup>-2</sup> s <sup>-1</sup> ]	114.4±1.0%	65.7±2.5%	46.7±4.0%	31.0±3.0%
Pion <sup>±</sup> Flux [cm <sup>-2</sup> s <sup>-1</sup> ] with E <sub>kin</sub> > 10 MeV	114.3	65.4	46.6	31.0
Sum Flux with E <sub>kin</sub> > 10 MeV	245	149	112	81

MeV proton beam at The Svedberg Laboratory.

### 3.4 Semiconductor devices exposed to radiation

Memory elements, and particularly SRAM cells, are known to be sensitive to single event upsets[11]. In the following sections a general introduction to the most important memory technologies and their susceptibility to SEU is given, before focusing in detail on the ALTERA APEX20KE400 FPGA.

Before continuing it can be mentioned that there is an area where the semiconductor devices sensitivity toward ionising radiation is used as an advantage. This is in the radiation detector industry. Modern radiation detectors employ discrete semiconductor devices as their sensor elements. The basic structure of a semiconductor radiation detector is a large silicon or germanium diode of p-n or p-i-n type operated in the reverse bias mode. It is based on the principle that a single charged particle can ionise the material which it travels through. The carriers (electrons) created through this ionisation are drifted by the strong electric field in the reverse biased diode and creates a current pulse which is detected and amplified [14].

#### 3.4.1 CMOS Memory elements

CMOS technology memory elements such as RAMs are divided into static structures and dynamic structures. Static cells use some form of latched storage or feedback, while dynamic cells are based on storage of charge on a capacitor.

## SRAM cells

The 6-transistor, cross-coupled inverter circuit in figure 3.18 and 3.19 is the most basic SRAM cell architecture. The cross-coupled inverters stores one bit of information, while two bitlines takes care of the reading and writing through n-type pass transistors on each side. The wordline must be high for both read and write cycles. Typically the inverters will have a strong n-type pull-down transistor and a weak p-type pull-up transistor[15]. Hence the key operation of the cell is to pull the bit line from high to low.

**Read cycle:** Both bitlines must start *high*. A *high* value on both bitlines will not change the value in the cell, and the cell will pull one of the lines *low* when the wordline is enabled.

**Write cycle:** One of the bitlines is forced *low*, while the other is *high*. When the wordline is enabled the *low* value on the bitline will overpower the inverter having the P-type transistor in the *on* state, and the new value will be latched in to the cell

SRAM cells are sensitive to SEU. If the particle strikes a sensitive area of a SRAM cell, it

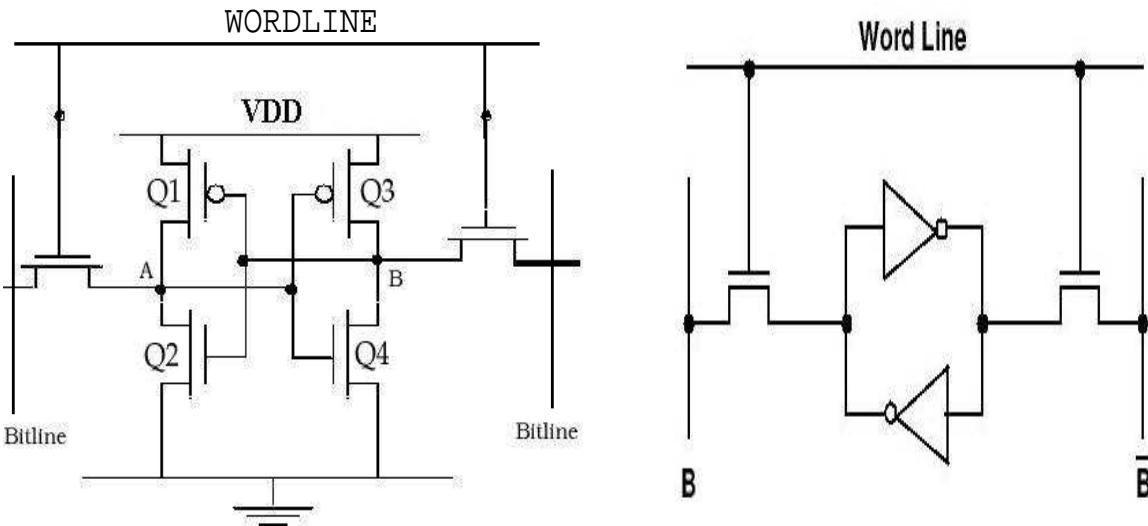


Figure 3.18: Typical 6 transistor SRAM cell

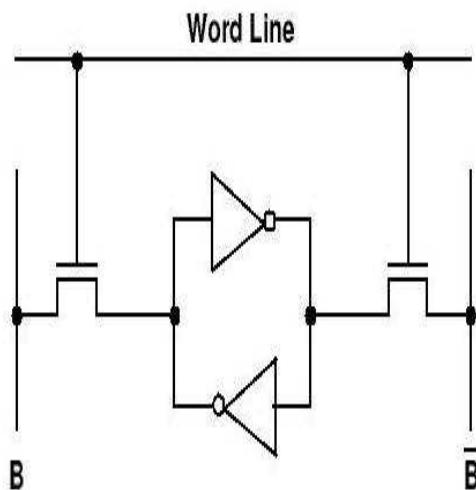


Figure 3.19: SRAM cell showing the cross coupled inverters

could result in a flip of memory data from logical 1 to a logical 0 or vice-versa. The SRAM cell has two stable states representing a stored 1 or 0 respectively. In the case of a stored 1 transistors Q4 and Q1 in figure 3.18 are *off*, while Q2 and Q3 are *on*. Suppose a charge particle causes ionisation nearby the sensitive volume of transistor Q4, an n-type transistor in *off* state. If the collected charge is sufficient, Q4 will be turned *on* for a short moment forcing the output value of the inverter *low*. In turn the input of the other inverter will respond to this *low* value and change its output value to *high*. This output is again connected to the input of the first inverter

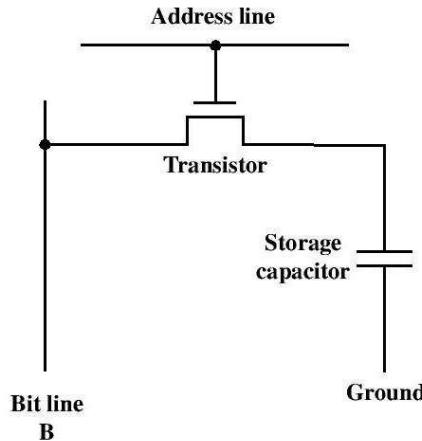


Figure 3.20: Typical one transistor DRAM cell

and thereby causing the new value to be latched into the SRAM cell. The resemblance to a write cycle is striking, and is in fact what this SEU causes. However the difference is that an incoming ionising particle can cause a flip of memory data even though the wordline is *low* keeping the pass transistor closed. From this one can conclude that the sensitive node of the SRAM cell is the drain of the n-channel transistor in *off* state.

Due to the strong n-type pull-down transistor a similar effect on the p-type pull-up transistor will not be able to overwin a conducting n-channel transistor. Also, in a p-channel transistors the majority carriers are holes which have lower mobility than electrons. If the two inverters are identical in size, the probability of an SEU causing a flip from a logical 1 to a logical 0 is just as great as for a logical 0 to logical 1. Independent of which value is stored in the SRAM cell, it will have one n-channel transistor in *off* state and therefore sensitive to an SEU.

## DRAM cells

In order to design memory blocks with higher density (more bits per chip) one had to design a memory cell using less transistors than the SRAM cell. Such a memory cell is the one transistor DRAM cell. It is not possible to build a bistable element with just one transistor. Instead the memory cells in a *dynamic* RAM (DRAM) store the bit information on a tiny capacitor accessed through a MOS transistor. The simplest possible DRAM cell is the single transistor cell shown in figure 3.20.

**Write Cycle:** The wordline is set *high* in order to access the capacitor. A *high* or *low* value is then put on the bitline in order to store either a *high* or a *low* value.

**Read cycle:** The bitline is first pre-charged to a voltage halfway between *high* and *low*, and then the wordline is set *high*. Depending on whether the capacitor voltage is *high* or *low*, the pre-charged bit line is pulled slightly higher or lower. The small change in voltage is detected by

a sense amplifier as either a *high* or a *low* value accordingly. Reading a DRAM cell destroys the original voltage stored on the capacitor. So the data must be rewritten after a reading in order to keep storing the value.

The capacitor is discharging also when no read operation is preformed. However the high input impedance of the pass transistor gives a relative long discharge time. Nevertheless, the DRAM cells needs to have periodic refresh cycle in order to keep their stored value. The small capacitor, and the fact that it does not have an active signal regeneration like the SRAM cell, makes the DRAM cell sensitive to radiation.

## Flash RAM and EEPROM

Flash RAM and EEPROM are in principle similar types of memories. The only difference is that in a array of Flash RAM cells all cells can be erased at the same time, while the EEPROM cells have to be erased on bit at a time. A Flash RAM cell is build up by two transistors which are separated from each other by a thin oxide layer. One of the transistors has a floating gate, and the other one has a control gate. The wordline or bitline can only access the floating gate through the control gate. Programming a flash cell means that charge, or electrons, are added to the floating gate. This is done by applying a high programming voltage (10-13V) to the drain and gate with respect to the source. A high electric field causes electrons flowing toward the drain to move so fast they "jump" across the insulating gate oxide where they are trapped on the bottom, floating gate. This is known as *hot-electron injection*. Electrons trapped on the floating gate raise the threshold voltage of the n-channel transistor. Erasing the cell is preformed with gate grounded and the source at a high voltage. Figures 3.21 and 3.21 show the principle schematic of a Flash

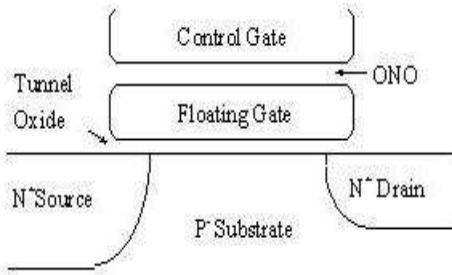


Figure 3.21: Flash RAM with floating gate

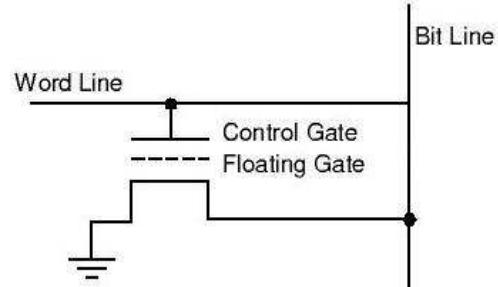


Figure 3.22: Flash RAM cell

RAM cell. In difference from the SRAM and DRAM cell the Flash RAM cell does not need any feedback or refresh cycle in order to keep the stored value. It will also keep its content after a power cycle. Due to the high operating voltages needed during programming and erasing, the sensitivity to radiation is very low compared to the SRAM and DRAM cell.

## Antifuse

This is a two terminal device that is a highly resistive element in its unprogrammed state, and is programmed to a low impedance. When programmed it is not reversible. It has a high tolerance toward ionising radiation [22].

### 3.4.2 FPGA

FPGA stands for Field Programmable Gate Array. An FPGA is fabricated as a large array of programmable logic blocks distributed across the entire chip, and is programmed by the end user in the field. The logic blocks are connected through a sea of programmable interconnections, and the entire array is surrounded by programmable I/O cells. Figure 3.23 shows a conceptual diagram of a two dimensional array of logic blocks that are connected through programmable interconnection resources. The logic blocks are the key elements and the basic architecture of an FPGA. They typically contain some logic gates, a look-up table and a some type of flip-flop for implementation of sequential logic. The FPGA uses memory cells to control the behaviour of the logic blocks or the routing of the interconnections. Most FPGAs today are based on either SRAM, Flash RAM, or Antifuse memory technology. The SRAM memory cells are volatile, this means they do not retain their state when power is removed. Therefore, when power is first applied to an SRAM based FPGA, all of its memory cells must be initialised for the FPGA to hold any functional circuits. The process of loading the SRAM bit pattern into the FPGA is called configuration. Configuring the FPGA can be done from a computer using a communication interface called the IEEE Std. 1149.1[24] (JTAG<sup>1</sup>), or by a separate, external nonvolatile memory, like for instance Flash RAM containing the bit pattern. Figure 3.25 shows how the state of an SRAM cell can control if a transmission gate is open or closed, or how two SRAM cells are needed in order to decide which of the two inputs of a multiplexor are put through to the output. Programming a design into an FPGA is done by loading a bit pattern, which is synthesized and compiled from a special programming language called VHDL<sup>2</sup> or Verilog, into the SRAM cells. An FPGA can contain several million of these memory cells depending on the size and complexity of the device.

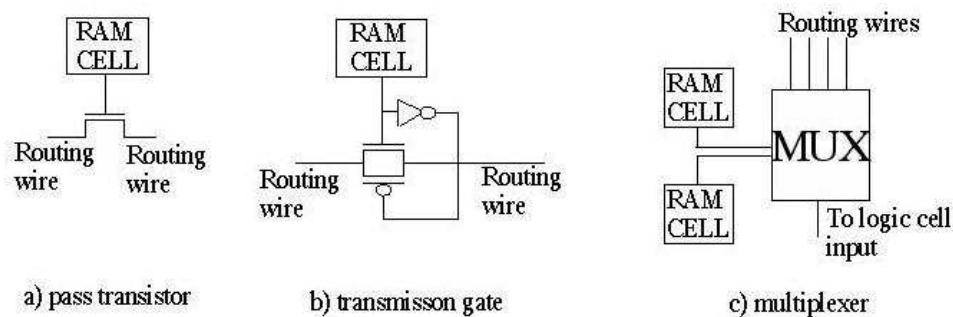
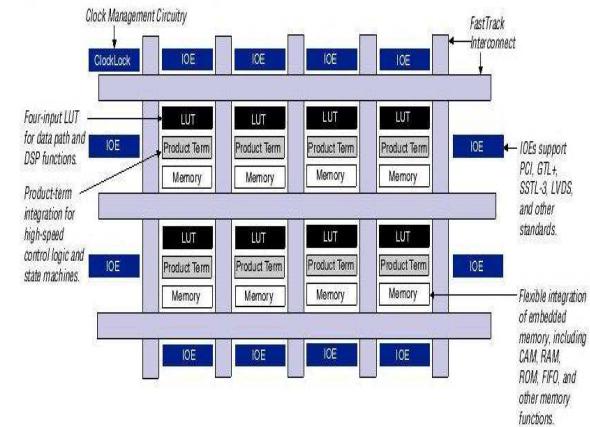
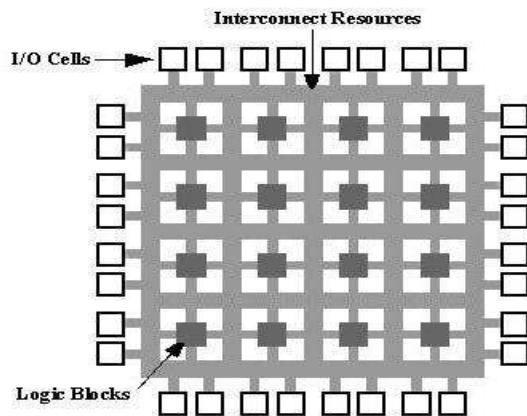
## ALTERA APEX20KE400 FPGA

The APEX 20K devices are designed with ALTERAs MultiCore architecture [24], figure 3.24, and are constructed from a series of MegaLAB structures, figure 3.27. Each MegaLAB structure contains a group of logic array blocks (LABs), one ESB, and a MegaLab interconnect, which routes signals within the MegaLAB structure. A LAB is further made up of 10 Logic Elements (LEs), which is the smallest unit of logic in the APEX20KE400. Figure 3.28 shows the architecture of the APEX 20K Logic Element. It contains a four-input Look-Up-Table (LUT), a programmable register, and carry and cascade chains. The LUT can implement any function of four variables, while the programmable register can be configured for D, T, JK, or SR operation.

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<sup>1</sup>Joint Test Action Group[23]

<sup>2</sup>see section 4.3



**Figure 3.25: SRAM cell controls the behaviour of different logic**

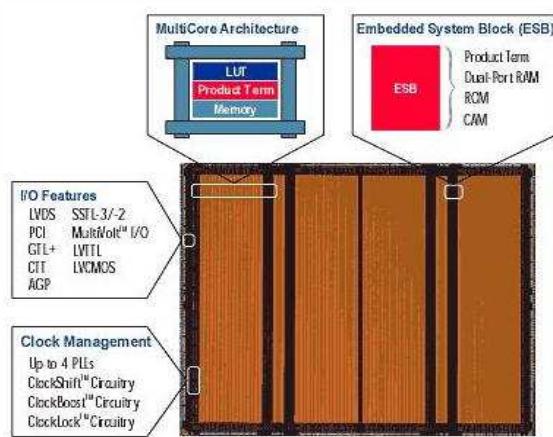


Figure 3.26: A picture of the architecture of the APEX 20K FPGA. [33]

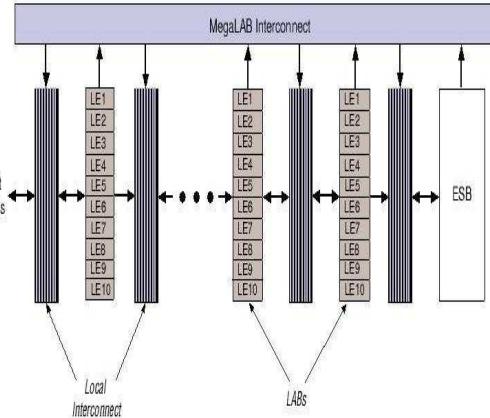


Figure 3.27: MegaLAB structure

ESB stands for Embedded System Block and can implement various types of memory blocks, like dual-port RAM, ROM, and FIFO. It includes input registers to synchronise writing of the memory. The ESB blocks will further be referred to as the internal RAM or application memory of the APEX FPGA. Figure 3.26 shows a picture of the physical layout of the APEX 20K FPGA, where we can see that the application memory blocks (ESB) are grouped in columns in each half of the device.

### FPGA and SEU concerns

There are three main types of SEUs that have to be considered in an FPGA. That is SEUs in sequential or combinational logic, in application memory, or in configuration memory, where the latter is of most concern.

An FPGA can contain several millions of SRAM cells used for both configuration memory and application memory. The difference is that the configuration cells can only be written to during programming of the device and not during normal operation. Thus an SEU in an SRAM cell used for application memory or configuration memory will in principle be identical, but will cause different effects. A bit flip in a memory position in the application memory will only be present until the same position is overwritten with a new value. For instance when a FIFO is implemented in the application memory for storing temporary data. Such a bitflip is therefore not of major concern. However, this of course depends on the upset rate of the device in mind. A low upset rate can in many cases be tolerated, and the loss of data due to a single event upset can be dealt with through different error detecting and correcting techniques.

If a bit flip occurs in the configuration part of the memory, this is a totally different matter. When a FPGA is programmed, the bit pattern describing the functionality of the device is stored in configuration SRAM cells. These SRAM cells are only initialised during programming of the device. Thus if a single event upset causes a configuration memory bit to flip from a logical

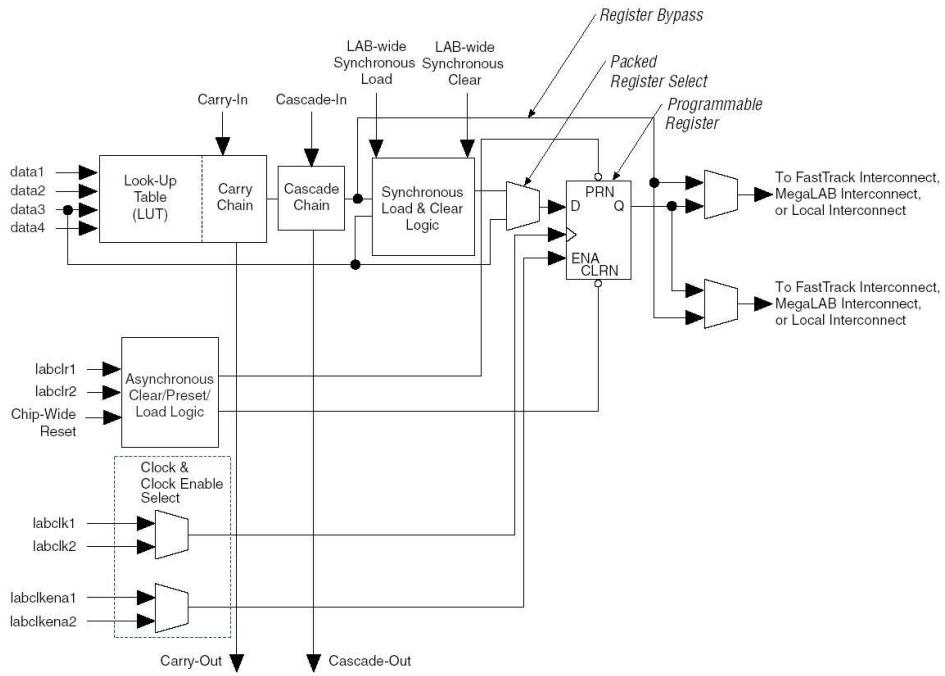


Figure 3.28: Logic Element of the APEX 20K [33]

1 to a 0, there is no way of changing it back without reprogramming the device. A bit flip in the configuration memory can alter the behaviour of the design and cause device failure. For example a 2 input LUT (Look-up table) that is set to be an AND gate would have a configuration of "0001", where the last bit represents the case where both inputs are 1. If an upset occurs and changes the configuration to "0101", the LUT will change and operate as a buffer. It will always pass the value of the second input to the output. An SEU causing a LUT or register to change its behaviour may only be located to a small part of the design and do necessarily not have to be crucial for the operation of the full design. However experiencing a SEU related to the interconnection of a global clock line this will most likely cause total failure in the operation.

An upset in the configuration memory can also be potentially destructive if the upset alters an input pin to be configured as an output pin, and thereby causing a short circuit. This is sometimes referred to as a SEFI (Single Event Functional Interrupt), and relates to errors changing the behaviour of areas in the device used for special function such as the JTAG and I/O buffers. Most likely the number of configuration memory cells used for I/O functions is low relative to the total number of configuration memory cells, thus giving a relatively low probability for an upset to alter the I/O functions. Good practice is anyway to implement a watchdog device to supervise the current consumption of the device and start a power cycle and reconfiguration if it increases above normal operating current.

Another form of SEU is an incoming energetic particle hitting a sensitive element in combinational logic. This can induce a current pulse that can propagate on a wire and potentially be latched into a register. Such a register bit flip will be restored in the next clock cycle and can

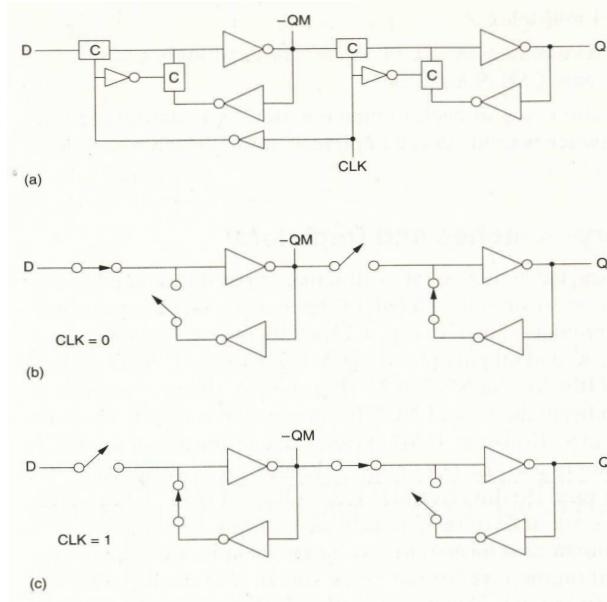


Figure 3.29: Basic D-flip-flop architecture, positive edge triggered [25]

possibly be detected and correct using different coding techniques. This type of SEU will depend on if the pulse will arrive at the data input of the register on the rising or falling edge of the clock, depending on which edge triggering is used.

When designing sequential logic like for instance a state machine, the design will be implemented using the programmable registers in the Logic Elements. For the shiftregister design described later, the programmable registers will be implemented as D-flip-flops. The basic architecture of such a D-flip-flop is shown in figure 3.29. From the figure we can see the close resemblance to the basic 6 transistor SRAM cell. The D-flip-flop is made up of two basic D-latches, each using a 2 input multiplexer. In principle the cross-coupled inverters can experience SEU like for the SRAM cell, but this bitflip will only be present until the value is updated in the next clock cycle.

# Chapter 4

## Irradiation test Methodology

*This chapter will discuss some of the different aspects related to irradiation tests of electronic devices such as FPGAs. It will give an overview of the basic equipment needed, such as readout hardware and software, and a general introduction of upset detection firmware that can be used for irradiation testing of FPGAs. Eventhough this chapter focuses on the FPGA, most of the methods are general enough to apply for other electronic devices as well.*

### 4.1 Introduction

One of the most important jobs that has to be done in the early phase of a system development, is to acquire a detailed overview of the radiation environment of where the system is to be placed. It is also advisable to identify which components needs to be tested and their importance to the system. Some components will be of crucial importance to the system operation and will require a low tolerance level, while other components conduct operations of less importance such that the system, in case of SEU failure, can bare without them for shorter moments. Thus these components can accept a higher tolerance level. Failing to do an appropriate classifying of the different components in the system can lead to unwanted delays or in worst case total redesign of the system. Both increasing costs rapidly. Some background research in order to see if other similar irradiation test have been carried out, can also be worth while. Such information can be helpful and give an initial indication of which tolerance levels to expect. However, one can not relay only one this information, thus irradiation tests of all the components to be used in the design are mandatory<sup>1</sup>.

Single event effects have a statistical nature and can be different from device to device. Even just small adjustments in the technology between generations of devices, like decreasing the minimum channel length, can change the behaviour related to single event effects.

Once the components to be irradiated are identified, the next step will be to make a detailed plan for the irradiation tests. This also involves identifying the type of radiation to be used. Different types of radiation will induce different kinds of damage. Therefore irradiation tests must

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<sup>1</sup>The SEU cross-section is strongly dependent on  $E_{crit}$  and the sensitive volume SV, and specific for each single component

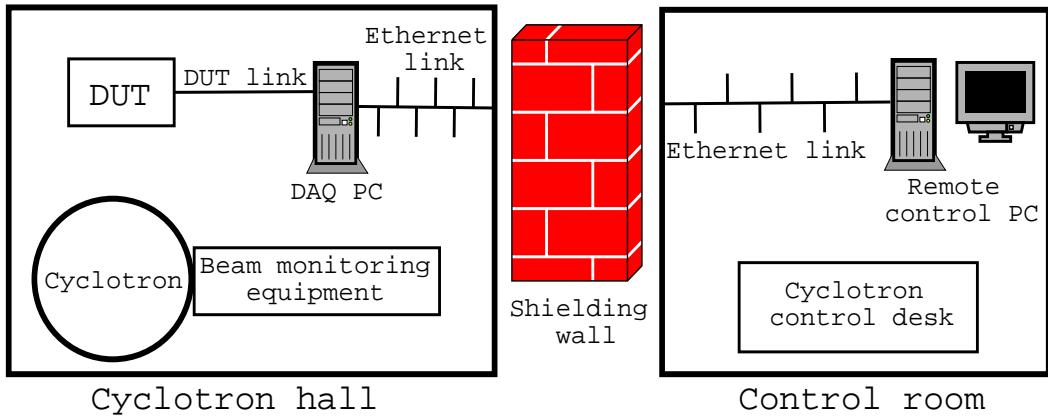


Figure 4.1: Typical irradiation test setup

be conducted with radiation types, energies, and fluxes similar to the actual radiation environment in mind. Some components, like the FPGA, will also need custom designed firmware in order to detect single event upsets.

## 4.2 Accelerated proton irradiation

Irradiation tests can be conducted at facilities having access to particle accelerators such as cyclotrons and linear accelerators. These are capable of producing mono-energetic beams of protons with different fluxes appropriate for testing electronic devices for radiation tolerance. This allows for measuring cross-section at a precise value of particle energy. And by doing tests at different energies it is possible to plot the energy dependence of the observed radiation effects.

### 4.2.1 Standard test setup

There are a few standard requirements one should consider when doing irradiation tests. Due to limited access to irradiation facilities, careful planning and preparation is necessary. The irradiation facilities might just not provide the test equipment necessary for doing custom made irradiation tests of electronic devices. Giving only access to beam time and a setup area, equipment like power supplies, cabling, computers and infrastructure, special purpose beam monitoring equipment, and other measuring instrumentation must be installed on request. The possibility of having a permanent setup is also slim, it is therefore advisable that parts of the test setup is portable so that it easily can be transported to and from the facility. Thus, a detailed overview of accessibility, available equipment, and infrastructure must be made prior to making the trip.

A typical irradiation test setup is shown in figure 4.1. The Device Under Test (DUT) is placed in the beam and connected to a nearby computer containing appropriate Data Acquisition (DAQ) hardware and software. Another computer is placed in the control room and can remotely

supervise the DAQ computer over an Ethernet link. The shielded control room also contains the control desk for operating and monitoring the cyclotron and beam parameters.

### Irradiation procedure

A typical irradiation procedure can be as follows:

1. Install the test setup
2. Calibrate the flux, energy and beam profile to the wanted settings
3. Place the DUT in the beam, and irradiate for a pre-selected time or fluence.
4. Monitor flux, current assumption, voltage levels and frequencies during exposure
5. Analyse data and calculate the cross-section.
6. Repeat 2-4 to collect sufficient statistics

## 4.3 VHDL test methodology

This section will focus on some of the methods available for irradiation testing of an FPGA. As explained in section 3.4.2, an FPGA is a programmable device where the main programming language used is VHDL or Verilog HDL. Both VHDL and Verilog HDL are languages for describing digital electronic systems, and the main difference between them is related to the syntax. The firmware designs in this thesis are based on the VHDL language.

### VHDL

VHDL stands for *VHSIC Hardware Description Language* [26], where VHSIC is short for *Very High Speed Integrated Circuit*. It is a language optimized for describing the behaviour of digital systems, from simple components like logic gates and multiplexors to complex microprocessors and custom made chips. VHDL is design to be used in all aspects of developing digital systems from specification, design, simulation and analysis, to documentation. VHDL allows both a structural and a functional description of the system. Structural means how the system is decomposed into different modules or subsystem and how these are interconnected. The systems functional behaviour can be described by using a familiar programming language form. What differs VHDL from a high level programming language is the concept of describing concurrent events. In programming languages such as C the code is in comparison executed in a sequential way, line by line.

### 4.3.1 Upset detection in FPGAs

As already mentioned there are three main areas to consider when designing firmware for detection of single event upsets in an FPGA, these are configuration memory, application memory, and sequential logic. The best alternative for testing configuration memory is to load the FPGA with a design, and to irradiate the device while continuously reading back the configuration bit stream. Comparing the read back bit stream to the initial loaded bit stream gives an accurate prediction of the FPGAs SEU rate. However, some devices, like the ALTERA APEX20KE400, do not offer the feature of reading back the configuration bit stream. Unfortunately other solutions have to be considered for these devices.

Other hardware parameters such as available I/O ports, also restricts the flexibility of the test design. The possibility of designing a custom made test card for irradiation purpose can be a great advantage. This allows for specifying which I/O ports to use, and route them to appropriate connectors for easy connection to external DAQ hardware and software. Thus, also giving a broader choice of communication protocols.

Designing firmware for single event upset detection in an FPGA can be based on *static* testing and *dynamic* testing [27]:

**Static testing:** For static tests, a fixed pattern is loaded into the memory before the device is irradiated. Data collection is thereafter done during or after exposure is ended. No further data stimuli are put on the I/O ports during exposure.

**Dynamic testing:** For dynamic tests, the DUT is irradiated during normal operation to see the effect of SEUs on the functional behaviour. Alternating data is continuously inflicted on the input ports and collected at the output ports during exposure. This method is suited for testing sequential logic.

### Configuration memory

If available, configuration memory is tested using only the option to read back the configuration bit stream. Should this option not be available, configuration upsets have to be detected indirectly using a design implemented in VHDL code. This means that a bit flip or an error observed in the data, will reflect the change in logic due to an upset in a configuration bit, and thus be an indirect detection of a configuration upset. A 100% use of configuration memory bits is very unlikely, thus redundant configuration upsets can occur. A redundant upset is an upset that makes no difference to the circuit operation, that is, it will not influence the behaviour and therefore not be detectable [1]. Hence, the irradiation tests will not give an exact configuration upset rate, but only an estimate.

Implementing a VHDL design for indirectly detecting single event upsets in the configuration memory has several solutions. To create a large cross-section, the design should use as much of the available resources as possible. An example is to design a small unit component, for instance a d-flip-flop, for then to replicate it until all programmable register resources are used.

For a large design there will always be a trade off between the number of elements to probe,

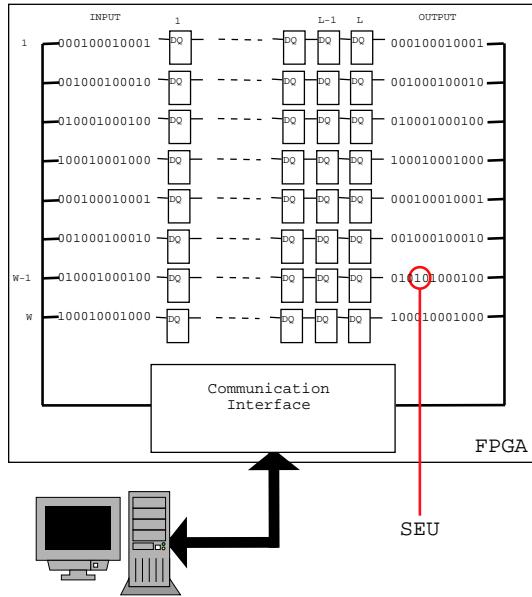


Figure 4.2: The shiftregister is implemented in the logic elements using the programmable registers. A fixed pattern is shifted through the shiftregister and compared at the output to detect an SEU. This is controlled from software. The marked ring indicates an example of a single bit flip.

and the I/O resources for reading out the data. Using an internal test design to verify the content of the elements can be one solution. Only when an upset is detected, an error signal will be sent to an output port for software detection. A drawback of this solution is that the internal test design can, like the design tested, just as well experience an upset such that it will no longer carry out its task as expected. However, keeping the internal test design small compared to the total number of available resources, will increase the reliability of this method.

### Shiftregister design

A design for detecting single event upsets can be a shiftregister using the programmable registers available in the Logic Elements of the FPGA. Its basic structure is an  $W \times L$  matrix of d-flip-flops, where  $W$  is the data width and  $L$  is the length of the shiftregister. During dynamic testing, an alternating pattern is shifted through the shiftregister and compared with expected data when read out at the outputs. A certain number of bits in the configuration memory will be related to the behaviour of the programmable register. An upset in one or more of these memory bits can change the behaviour of the programmable register, so that it no longer will operate as a d-flip-flop. For instance, the data input may be disconnected, the clock input may change from rising edge to falling edge triggering, or even be disconnected. The actual change in logic due to an upset is impossible to decide, but the effect will be seen at the output of the shiftregister. A d-flip-flop with a stuck output port will result in a pattern different from what is expected at the output.

Figure 4.2 shows a principle schematic of such a shiftregister design. The shiftregister design can also be used to detect single bit flips such as transient pulses latched into a register, see section 3.4.2. A change in logic caused by a configuration upset or a single bit flip induced directly in the logic, will at first glance have the same appearance. It will only be distinguishable by looking at it over time. While a configuration upset will give a permanent change in the logic, and therefore be reflected as a continuous error at the output, a single bit flip will only be present until the next clock cycle loads a new value into the register. A configuration upset can only be fixed by reconfiguring the FPGA. Using the shiftregister design therefore covers the detection of both configuration upsets and single bit flips in sequential logic.

### Application memory

The basic test methodology for memory arrays is to store a fixed pattern in the array while the DUT is exposed. After irradiation the stored value is read back and compared with the initial loaded pattern, *static* testing. However internal memory can also be evaluated during exposure by continuously reading back the stored pattern, or by shifting a pattern through for instance a FIFO. A FIFO, First In First Out, has in principle an identical functionality to a shiftregister design. Implementing internal RAM using a FIFO design will therefore only introduce a small additional control logic to make both designs compatible with the same readout software.

## 4.4 Readout/DAQ software

Testing electronics will involve some type of DAQ hardware and software. The main task will be to generate a test pattern, write the pattern to the inputs of the FPGA, read data back from the output, and compare for upset detection. The FPGA must therefore be connected to external hardware like a computer. How the FPGA interfaces the computer is dependent on available communication protocols, such as the serial port (RS232), parallel port, game port, and PCI-bus. Software like LabView and Matlab offer built in modules for some of these communication ports. However using a Linux platform, custom made programs based on c-programming can relatively easily gain access to the communication ports.

In addition the software should contribute to the analysis of the irradiation tests and presentation of the results. Analysing the data can for instance be done real time during irradiation testing. However, a full analysis in real time is generally not a requirement while doing irradiation tests. Post analysis should be sufficient, given that some results can be interpreted during runs so that adjustments can be done based on unexpected behaviour or problems.

# Chapter 5

## Firmware and software for irradiation tests

### 5.1 Introduction

*The main focus in this chapter is the development of firmware and software for detecting single event upsets in the ALTERA APEX20KE400 FPGA. The chapter is divided in two main sections, one covering the firmware design and one describing the readout software.*

### 5.2 Firmware development

When developing firmware for irradiation tests of the FPGA there are two main parts to implement. The firmware design capable of detecting single event upsets, and the firmware able to communicate with external devices. The latter implies that additional communication hardware will be used.

#### 5.2.1 DUT related hardware

Housed in a 672-Pin FineLine Ball Grid Array (BGA) package, the ALTERA FPGA is a relatively complex device. Designing a custom made test card for the APEX demands expensive equipment and complex routing of the layout. Thus for practical reasons an existing RCU prototype II (fig. 2.6, section 2.1.1) card, containing an APEX 20K FPGA , was used for the irradiation tests. Additionally a serial protocol (SCSN, Slow Control Serial Network, see section 5.2.2) for communication between the FPGA and the readout software was available for implementation. Thus, using already available hardware and software it was possible to start doing preliminary irradiation tests within a relatively short time.

## 5.2.2 Communication interface

The RCU prototype card II offers several options of communication, such as USB<sup>1</sup>, Ethernet<sup>2</sup>, UART<sup>3</sup>, SCSN<sup>4</sup>, and parallel connection to I/O pins of the DUT. A solution implementing a USB or Ethernet interface would demand a complex onchip firmware design, and was therefore not considered. There are three main iterations in the communication firmware design:

1. Slow Control Serial Network (SCSN) design
2. External communication design
3. UART communication interface

### The Slow Control Serial Network

The Slow Control Serial Network (SCSN)[29] is a high<sup>5</sup> speed interface, that provides a serial communication between one master and multiple clients over a single signal wire. It is made redundant, and with full duplex communication, by using 4 signal wires, two for transmitting data and two for receiving data. The protocol offers a 16 bit address bus and a 32 bit data bus multiplexed over one single line. It is written in VHDL, synthesized in hardware and already tested out. Therefore, this protocol was used as a first approach to the communication link. It has a ring topology (see fig. 5.1), however in this case only the master and one client are used. The RCU prototype II can be powered by an external power source and run in stand alone mode, or mounted in the PCI-interface of a computer. Figure 5.2 show a principle schematic of how the SCSN protocol is used. The master design is placed in the card which is connected to the PCI bus of the experiment PC. It is further connected by the 4 wires to the other RCU card, which is in stand alone mode and running the client design on the DUT.

By running a SCSN client onboard the DUT, there is always the possibility of experiencing single event upsets in the SCSN design as well. To a first approximation this problem is minimized by periodic loop back of the data present at the SCSN client output. This means that the

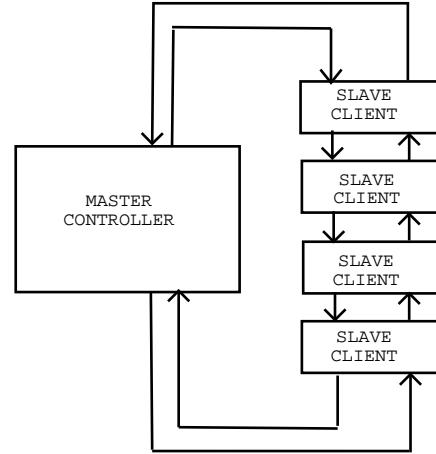


Figure 5.1: Shows the ring topology of the SCSN network. The ring is redundant by using to lines with duplex communication

<sup>1</sup>Universal Serial Bus [28]

<sup>2</sup>Local area network[28]

<sup>3</sup>Universal Asynchronous Receiver/Transmitter[28]

<sup>4</sup>Slow Control Serial Network, see section [29]

<sup>5</sup>Network speed: max. 1/3 of clock speed.(tested up to 24 MBits/s at 72 MHz)[29]

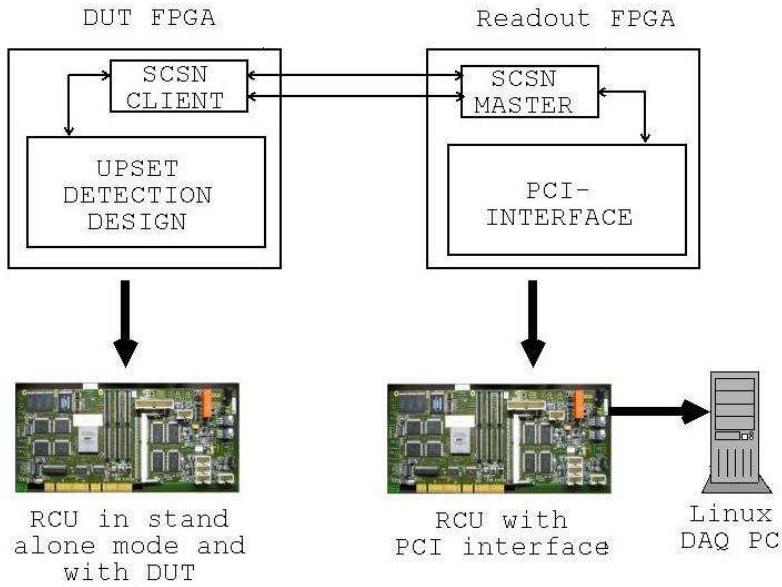


Figure 5.2: The schematic displays the principle architecture of the communication protocol using the SCSN. An FPGA with the master on board communicates over four wires to the DUT, which contains a SCSN client and the upset detecting VHDL. The experiment PC is connected over Ethernet to a remote PC in the control room

data sent to the FPGA is not shifted through the upset detection design, but returned directly back through the SCSN network to the computer. This checks for configuration upsets related to the communication interface. The SCSN client is a complex interface, uses approximately 10% of the internal logic, and has far more functionality than needed for this purpose. It was therefore decided to design a less complex communication interface.

### External communication design

The communication interface was moved off the DUT and on to an external device so that only the upset detection design was left on the DUT. For practical reasons, a Stratix Nios development Kit[31][33] was used for this purpose. The Stratix Nios Development kit is a general purpose card containing a Stratix FPGA for developing and testing out different kinds of VHDL designs, including the NIOS softcore processor[32]. The Stratix FPGA ( $0.13\mu\text{m}$  technology) is the next generation FPGA after the APEX family ( $0.18\mu\text{m}$  technology)[33]. As most similar development cards it offers a standard UART interface to the Stratix chip. A UART VHDL design was therefore designed and synthesized on the Stratix chip in order to communicate with the serial port on the DAQ PC. This solution also made the RCU prototype II card in the PCI-interface superfluous. On the DUT the upset detection design was directly connected to I/O pins of the APEX. The Stratix development kit and the RCU card with the DUT was connected using a flat cable containing 16 wires for data, 8 for each direction, one enable line for latching the

shiftregisters, and a few wires for ground connection. This parallel connection was limited by the available connector width on both the RCU card and the Stratix development card. A data bus width of only 8 bit means that a very long shiftregister design (approx. 2000 bit long) has to be implemented in order to make use of all the available programmable register resources in the device.

### **UART communication interface, current version**

The UART VHDL design was implemented directly on the APEX 20K FPGA (DUT), and thereby removed the additional hardware( Stratix Nios development Kit) introduce in the previous iteration. Eventhough this solution created additional control logic on the DUT, the UART design uses approximately 1% of the total logic resources available, which is an acceptable size compared to the 10% of the SCSN protocol. As for the SCSN design, a loop back of the data is done to cover possible configuration upsets related to the communication. A multiplexer is added to increase the width of the shiftregister from 8 bit to 32 bit. This shortens the needed length of the shiftregister to fill the device, and thereby also increases the upset detection level for SEUs, see section 5.3.2. A principle schematic of the top level design in the FPGA using the UART interface is shown in figure 5.4, while figure 6.1 shows an overview of the setup.

For the three iterations described above, version 1 was used for the preliminary and two first test periods at the Oslo Cyclotron Laboratory, and version 3 was used for the two irradiation periods at the The Svedberg Laboratory and the the last period at OCL. When using version two, the CMC Mezzanine connectors used on the RCU prototype II gave rise to unwanted errors in the data transmission due to poor contact points. Thus it is was not used for any further irradiation tests.

### **5.2.3 VHDL upset detection design**

Based on the test methods introduced in chapter 4, this section will describe the upset detection design for both sequential logic and application memory.

#### **Shiftregister design, sequential logic**

The design can be divided into three levels where the basic level is the D-flip-flop in figure 5.3(a). VHDL has some powerful programming features, and the *generate* statement is one of them. By minimal amount of code the *generate* statement replicates the component or statement of interest. It is particularly useful if the number of times we want to replicate the component or statement is not fixed, but is determined by a generic constant. See reference [26] for more information on VHDL and the *generate* statement. By employing the *generate* statement in two stages, a 2 dimensional ( $W \times L$ ) array of D-flip-flops is created, where  $W$  is the number of rows or the width, and  $L$  is the number of columns or length of the array. By only varying the values of  $W$  and  $L$ , the shiftregister can be changed to any size, only limited by the available programmable registers in the FPGA.

The intermediate level generates a row of  $L$  D-flip-flops, and on the top level this row is replicated  $W$  times in order to create the full shiftregister. In figure 5.4 a principle sketch is shown for the top level design. The control logic synchronises the data between the UART interface and the shiftregister over an internal data bus, having the same width as the shiftregister. This figure also applies when using the SCSN interface or FIFO upset detection design. One only exchanges the UART interface with the SCSN interface and the shiftregister design with the FIFO design.

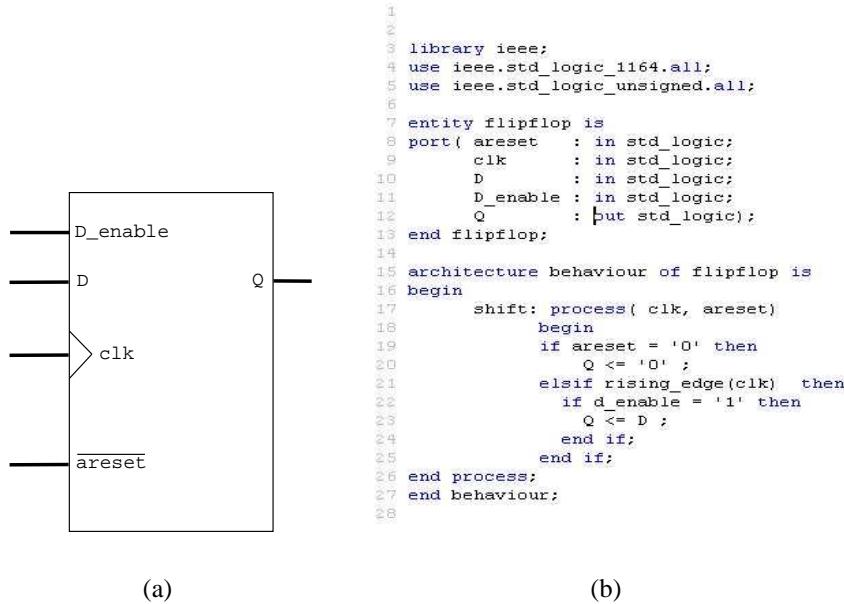


Figure 5.3: a) Basic symbol for D-flipfbp with data enable and asynchronous reset, b) VHDL code representation of the flip-flops behaviour

A 33 MHz clock, generated from the onboard 66 MHz crystal, is used as the system clock. Data is latched into the shiftregister on rising edge of the clock when the data enable input is high. This is represented in the VHDL code for a single d-flip-flop in figure 5.3(b). The data enable input is forced high whenever new data has arrived from the communication interface. When the data enable input is low, a loop back of the output to the input is done internally in the register. How often data is latched into the registers is limited by the frequency of the communication interface. For the UART interface the baud rate is 115.2k bit/s. Calculating with a transfer of  $W$  bits plus additional start and stop bits, and delays in software and UART buffers in the computer, the data update frequency is obviously lower than the baud rate. In other words, a system clock of 33MHz is more than sufficient for this purpose. However the higher the frequency the higher the probability of detecting single event upsets due to transient currents propagating in the logic for then to be latched into the register. See section 5.4 for more information on the data transfer rate.

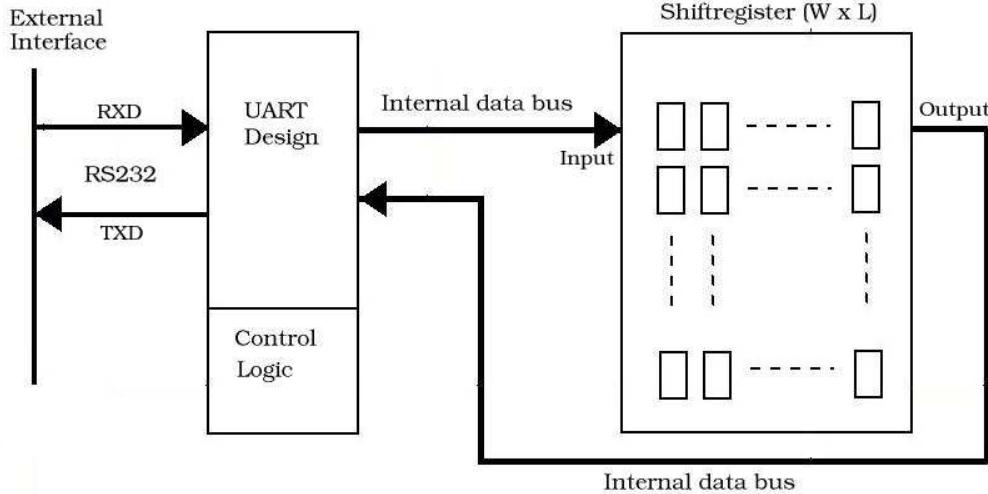


Figure 5.4: Principal overview of the top level design

### FIFO design, internal RAM

Internal RAM and the programmable registers are tested separately by dividing them in two different design files. The FIFO design uses approximately 130000 memory bits while the number of programmable registers in comparison is 16000 (typically  $W \times L = 32 \times 500$ ). Thus doing a test integrating both designs would create more complex software to synchronize reading and writing of data to and from the device.

Quartus[34] Megawizard Plug-in Manager is used to create a standard FIFO which is implemented in the internal RAM of the APEX FPGA. The FIFO has in principle a similar behaviour to the shiftregister design, and just minor changes in the control logic is needed. It uses the same internal clock as the shiftregister design and the data enable line is now connected to the write enable pin of the FIFO. In order to use the complete size of the FIFO, the read enable pin needs to be inactive until the FIFO is filled with data. For a FIFO size of  $8 \times 8192$  ( $W \times L$ ), the read enable must therefore be inactive for the first 8192 data write cycles. When creating the FIFO one can decide to add an output which will flag the event of a full FIFO, and thereby activate the read enable on this event.

Using the SCSN protocol, with a data bus width of 32, one FIFO was implemented with a 32 bit data input and a depth of 4096. Quartus limits the depth of the FIFOs to 8192. In order to reduce the control logic (multiplexers) the FIFO for the UART design was implemented using an 8 bit data input and a depth of 8192. Thus using the same amount of memory bits as for the SCSN version. In total 131072 internal memory bits were used, which is approximately 60% of the available memory bits. Table 5.1 summerises the use of resources for the different designs.

Table 5.1: A summary of the use resources in the different designs, the data bus width is given for the communication interface

	UART		SCSN	
	Shiftregister	FIFO	Shiftregister	FIFO
Width	32	16	32	32
Length	500	8192	400	4096
No. Registers	16000	0	12800	0
RAM bits	0	131072	0	131072
Data bus width (Ext)	8	8	32	32
Used at	OCL/TSL	OCL/TSL	OCL	OCL

### Preliminary design

One of the most important considerations when designing firmware for single event upset detection is not only its susceptibility to SEUs, but also how an SEU will appear in the data read out of the device. If the design is too complicated it might be difficult to analyse what type of SEU has occurred and the number of them. An example is the design used for the first design approximation and implemented for the preliminary tests in Oslo. Figure 5.5 shows the principle behaviour of the design. It was based on the idea of comparing two identical 8 bit counters. Implemented with 8 programmable registers each, they were compared after every clock cycle to see if they differed. The 8 bit counters were running on the system clock of 33MHz, and the communication interface was the SCSN protocol. If a SEU occurred in one of the counters, a

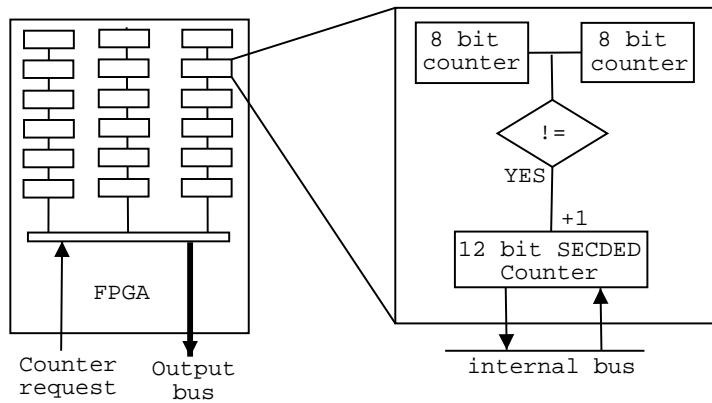


Figure 5.5: Preliminary upset detection design based on comparing the values of two identical 8 bit counters, and a hamming coded counter incrementing when the two counters are unlike.

hamming SECDED<sup>6</sup> coded 12 bit counter would be incremented by one. Keeping track of the number of SEUs occurring in the 8 bit counters, it was reset after a readout was requested by software. If a single bit flip occurred in this counter, it would be corrected by the SECDED

<sup>6</sup>Single Error Correction Double Error Detection

scheme implemented. A double error would be detected when decoded in software and thus disregarding the counting value. Several of these upset detection elements were distributed in the FPGA filling up the available resources. This design involved having some of the detecting analysis on-chip. It was design with the intention that the SEUs would be largely dominated by single bit flips in the register and not configuration upsets. However a frequent readout of the SECDED counter showed counting values far above what was expected. It was also difficult to determine if these counting values were the result of many single bit flips or configuration upsets. Later measurements using the new shiftregister design showed that the SEUs were dominated by configuration upsets and not single bit flips as the counter design described above was intended for.

Thus it became clear that the idea of doing some of the detection analysis on-chip not necessarily was the best solution, since the direct effect of the SEU could not be seen in the data read out. Keeping the upset detection design simple by using a shiftregister gave less complexity in the data read out, making it possible to distinguish between a single bit flip and a configuration upset.

## 5.3 Software and analysis

The basic function of the software is to communicate with the hardware, that is, synchronise writing and reading of data to the hardware, and to store and analyse the data read out. It was difficult to foresee how SEUs would affect the data shifted through the device. Preliminary results from the irradiation tests were therefore analysed manually. Clearly, changes like flips of bits from 1 to 0 or 0 to 1 would be expected. But the typical patterns created by such flips needed to be investigate closer before an effective and automatic analysis program could be written. This section will try to give an overview of the basic behaviour and tasks of the software used for the irradiation tests.

### 5.3.1 Readout software

As a direct result of the communication interface iterations, the software used for the irradiation tests are divided in two versions,

1. Readout software using the SCSN interface
2. Readout software using the UART interface

The *SCSN interface* is both a firmware and software design. The software is written in ANSI-C and the main function is to write and read data over the PCI-bus of the PC. This program is based on the PCI and Shared memory Interface (PSI)[30], which is a library and corresponding kernel module for accessing PCI devices and shared memory (physical, logical, bigphysarea) from user space programs. Current version of this module is only available for Linux. A program customised for the purpose of irradiation tests was written based on the functions needed to access the PCI interface.

After implementing the *UART interface*, parts of the c-program had to be rewritten. It involved removing all code related to the SCSN interface and replace it with a less complex c-code for accessing the serialport of the computer.

The principle of the readout program is similar for both the SCSN interface and the UART interface version. In figure 5.6 a flow chart of the main routines in the readout program is shown, and the different blocks are described below.

**Start:** The program is started from a Linux shell environment.

**INIT:** During initialisation, the logfile for storing data is opened for writing. Altera's Jamplayer software is used to program the APEX 20K FPGA over the JTAG, and is called from within the c-program.

After initialisation and programming of the APEX device, the program enters the main routines which handles the writing and reading of data to the FPGA. It is divided into a initialisation loop and a main loop.

**INIT LOOP:** On start up the shiftregister and FIFO contains no bit pattern thus this initialisation loop fills them with a pattern of ones and zeros. At this point the behaviour of the shiftregister and FIFO is different. While the shiftregister will shift out all zeros when being filled up, the FIFO will have the read enable inactive during the same period, and will therefore only be written to. However for the shiftregister version a compare for SEUs will be done on the zero bit pattern.

**TEST I:** If a SEU is detected it will be logged with a time stamp and the corresponding expected value of the upset bit pattern. When the whole shiftregister or FIFO is filled, the program will jump out of the *INIT LOOP* and continue into the *MAIN LOOP*.

**MAIN LOOP:** This loop will continuously shift a fixed pattern through the device.

**TEST II:** Same as for *TEST I*, except it will continue until a termination of the program is forced by the user.

An automatic termination of a running program due to time out, or that a predefined number of errors is reached, has not been implemented. During irradiation runs it is recommended to

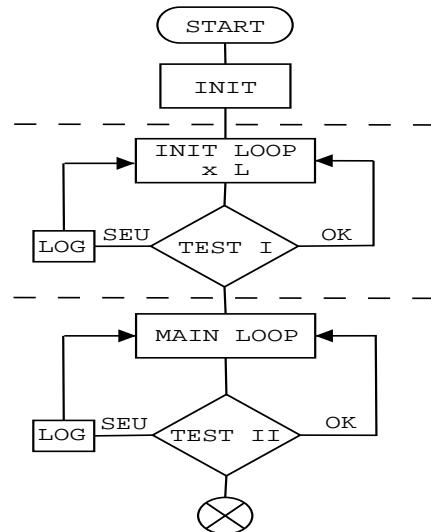


Figure 5.6: Basic fbw chart for the readout software.

supervise the program so that it can be terminated manually in case of unwanted behaviour. Such behaviour can be that a SEU has caused the readout design to fail and thereby generating worthless data on the output.

### Test pattern

The readout software generates a pattern of ones and zeros which is shifted through the FPGA. An example of a full test pattern is given in table 5.2. Only the 4 least significant bits in the hexadecimal representation are used as data bits (highlighted in the table). The 4 most significant bits are used as control bits for the firmware. A bit combination of "0000xxxx" will clear the shiftregister or FIFO, "1111xxxx" will loop back the written data directly from the UART interface on the FPGA, and for all other combinations, the 4 last bits will be written as data to the shiftregister or FIFO. The column *Pattern table* contains the data pattern. It is sub divided into

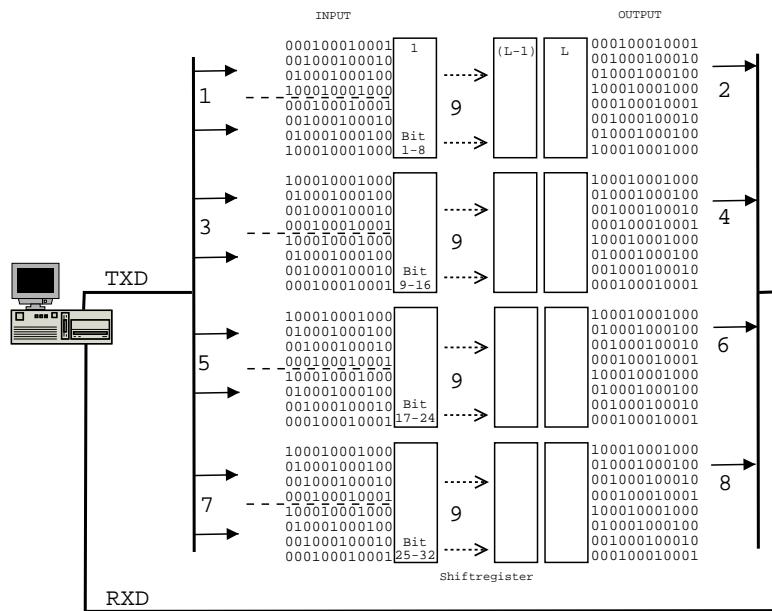


Figure 5.7: Principle schematic showing the bit pattern loaded into the shiftregister on the left side and read back out on the right side  $L$  clock cycles later, where  $L$  is the length of the shiftregister. Numbers 1-8 represents the write and read transmissions in chronological order, followed by a data enable and data latch operation for number 9. The schematic also applies for the FIFO design, except that the number of inputs are reduced from 32 to 16

4 columns, where each column represents the 32 data bits that will be latch into the shiftregister or FIFO<sup>7</sup>.

In order to write data to all 32 inputs of the shiftregister, the four last bits in each hexadecimal number are written to 8 inputs at a time. Which means that 4 and 4 inputs have a similar

<sup>7</sup>For the 16 bit wide FIFO only the first two rows in the table are used

Table 5.2: Example of test pattern used for the irradiation tests. Left column contains the data shifted through the device, while the right column contains the test pattern that will be compared with the read back data to check for SEUs

Row	Pattern table	Test table
1	0x41 0x42 0x44 0x48	0x11 0x22 0x44 0x88
2	0x48 0x44 0x42 0x41	0x88 0x44 0x22 0x11
3	0x48 0x44 0x42 0x41	0x88 0x44 0x22 0x11
4	0x48 0x44 0x42 0x41	0x88 0x44 0x22 0x11

pattern, see figure 5.7. After 8 UART transmissions, 4 write and 4 read, all the 32 inputs of the shiftregister have received new data, and the value on all the 32 outputs have been read. The data enable (*d\_enable*) is put to high for one clock cycle and the data is latched into the shifregister, thus also latching new data to the output. The 32 bit data read from the output is compared to the expected value listed in the column *Test table*.

A *walking one* pattern is used in the example given, but other patterns can be used as well. A thorough investigation into which pattern gives the best detectability of SEUs has not be carried out. For the internal and configuration memory, the probability of flipping a logic 1 to logic 0 should statistically be the same as flipping a logic 0 to a logic 1. This is due to the configuration SRAM cell always having an n-type transistor in the *off* state. The probability of having an upset should therefore be independent of the stored bit value. See section 3.4.1 for a description of the SRAM configuration cell. Thus frequently alternating pattern of ones and zeros should be able to give a sufficient detectability level.

### 5.3.2 Analysis software

During irradiation testing the readout software shifts a bit pattern through the DUT, reads it back and checks for changes in the pattern. If a change is detected the XOR result of the expected data and the corrupted data is stored in a logfile. Table 5.3 gives an example of how such a logfile can look like. The right most column is the data pattern read back form the DUT. The data is compared to the expected data and the XOR pattern of this comparison is shown in the column marked *XOR*. Line 2036 shows how a single bit flip can look like. Compared to the two other SEUs shown in the example, this bit flip only appears once and is not repeated in time. The two other SEUs have a repeating pattern which is a clear sign that a configuration upset has occurred, forcing a stuck-at value at one of the registers in the respective shiftregister row. However as the table show, the configuration upset are not detected in every line or pattern shifted through. Lets look at the most right SEU in the *XOR* column. Comparing with the data column we can see that a bit flip from a logic 1 to a logic 0 has occurred. This bit flip will only be detectable when ever the output of the shiftregister is suppose to have a value of 1, but instead forces a 0. A reverse test pattern ,of a walking zero, would give a repeated *XOR* pattern with three 1's , one 0 , three 1's , one 0 and so on. In other words, different test patterns will give different *XOR* patterns. But the consistent idea is that a configuration upset pattern will repeat itself in time while a single bit flip SEU will be present for a limited time only.

Table 5.3: Example of a parts of a log file containing read out data and a XOR of the read back data with the expected data. The horizontal line indicates that a part has been cut out between the second error and the third error. This example is modified for the purpose of describing how SEU can be analysed.

In order to count the number of SEUs in a logfile the XOR pattern is plotted as a function of the time column. An example is shown in figure 5.8. Each of the sub-plot represents one of the bit columns in the XOR pattern, hence one of the 32 outputs bits. The values in the sub-plots

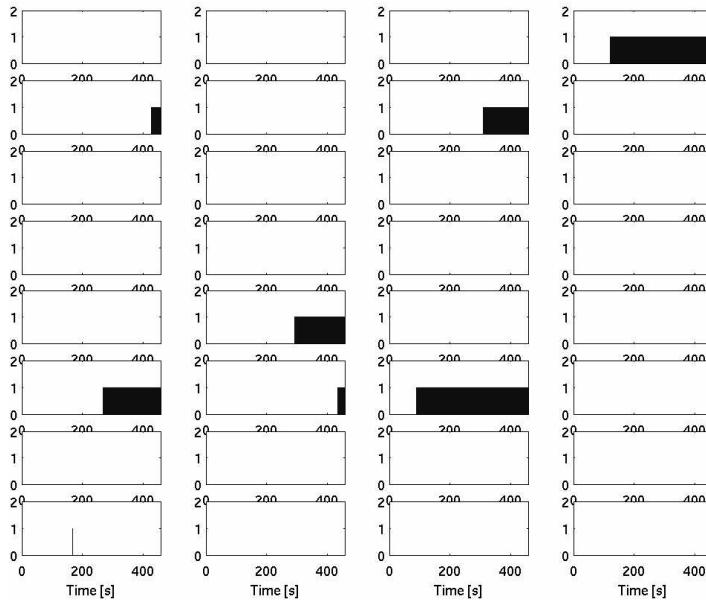


Figure 5.8: Example of plotting the XOR bit pattern (SEUs) as a function of time. Each subplot represents the output data from the shiftregister as a function of time. All the 32 outputs are plotted, with the four plots in row one representing bit output 1-4, the next row bit 5-8, and the last row bit 29-32. This plot is not connected to the logfile in table 5.3.

are either 0, if no SEU has occurred, or 1 if a SEU is detected. A single bit flip will be plotted as a single bar, as shown in the most left subplot on the bottom row. A continuous value of 1 indicates a configuration upset. In reality it is not a continuous plot, but a bar plot of spaced 1's. It only looks continuous because of the large amount of bars plotted in a small area. Thus, figure 5.8 represents a logfile with 7 configuration upsets and 1 single bit flip for a shiftregister design.

One can argue that a single bit flip in between a configuration upset plot will not be discovered due to the continuous look of the plot. Lets take an example of a row of 500 registers. If a configuration upset is inflicted on register number 400, it will be detected on the output 100 latched clock cycles later. From now on this output will no longer produce the expected data. If a new SEU is inflicted in one of the registers 1-399 it will not reach the output due to the upset in register 400. However a single bit flip or new configuration upset in registers 401-500 will reach the output, but due to the already change pattern from register 400 it will be hard to detect without intelligent pattern recognition software.

In order to avoid this extra pattern recognition software the output which experiences a configuration upset will be disregarded as an observable source for new SEUs for the rest of the test. Thus as increasing numbers of configuration upsets are detected, more and more of the flip-flops

in the shiftregister will become redundant to the SEU tests. In other words, the SEU detectability level of the design will decrease. This can be noticed if the number of upsets is plotted as a function of time as in the first plot in figure 5.9. Below 300 seconds, 16 SEUs, the number of

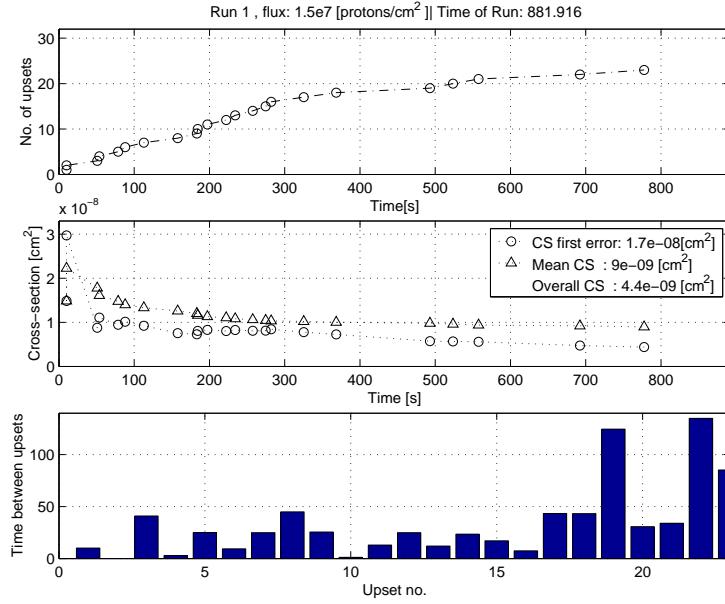


Figure 5.9: Example plots of a logfile.

SEUs seems to have a linear increase. After this point the slope decreases slightly and the time between upsets increases. For 16 SEUs, half of the outputs and thus half of the shiftregister can not be used as a detector for new SEUs. Statistically this half will experience the same amount of new upsets as the other half, but they will not be detected and thus the upset rate will decrease. A critical point in the irradiation tests is therefore to decide how many SEUs can be detected before one can regard the test design as a poor SEU detector. For the irradiation tests of the shiftregister and FIFO design described in this thesis, the runs have been carried out until about 25-30% of the outputs have been inflicted with an SEU. For a data width of 32, this means 8-10 outputs.

Figure 5.9 is the result of an analysis done in Matlab. The Matlab function `find(X)` searches through the XOR matrix and finds the first occurrence of a 1 in every column and its corresponding time tag. This will give the number of configuration SEUs. In order to use this method, a visual check of the plot is needed to see that it has an expected appearance, for instance like figure 5.8. Also, all single bit flips have to be counted for and removed from the logfile when calculating the configuration upset cross-section. It is therefore recommended to make a backup of the logfile. The cross-section is calculated as the total number of upsets divided by the fluence (flux integrated over time). The irradiation tests are in average run over 400-600 seconds producing all from 5 to 10 SEUs. Thus in order to produce statistical valid results several runs must be carried out.

## 5.4 Limitations and future improvements

The ideal test method for configuration memory is the option to read back the configuration bit stream. Being able to distinguish application memory bits from the configuration memory bits in this read back, will give an accurate cross-section result for both. That this feature is not available for the ALTERA APEX 20K FPGA limits this accuracy. Because not all configuration upsets will lead to a detectable error in the design, an additional dynamic test should also be carried out. A dynamic test will be design specific, and thus measurements from the irradiation test of the upset detection design can not give an accurate cross-section for the final design. This makes an irradiation test of the final design running on the final hardware mandatory.

Eventhough the shiftregister design uses approximately all of the available logic elements in the FPGA, it does not imply that it uses all of the available and potential sensitive configuration memory bits. The LEs of the APEX 20K also have available logic that will not be used in a shiftregister design, for instance the 4-input LUT. It is therefore questionable if the cross-section measured is the cross-section of the configuration bits, the Logic Elements, or maybe only the of the programmable registers in the FPGA.

### Readout software

A bottleneck in the test setup is the speed of the interface link between the DAQ computer and FPGA. Running the UART on 115 kbits/s limits shifting of the test pattern through the FPGA. Reading and writing to the serialport is done by using the functions *write(portHandle, &data, 1)* and *read(portHandle, &data, bytes)*, where *portHandle* gives the reference to the port of interest, *&data* is a pointer to the data which will be written to or read from the port, and *bytes* is the number of bytes which shall be written or read in one operation[36]. The typical operation in the shiftregister design is to write one byte over the serial port and then read back one byte, repeated 4 times in order to write and read 32 data bits. The syntax used is as follows:

```
...
write(portHandle, &c, 1);
delay(milliseconds(12);
read(portHandle, &c2, 1);
...
```

A rough calculation of the time to shift a 32 bit pattern through a 500 bit long shiftregister is:

$$\begin{aligned} t &= (1/\text{baudrate} \cdot \text{bits} \cdot 2 + 12 \text{ ms}) \cdot 4 \cdot \text{length} \\ t &= ((1/115200 \cdot 10 \cdot 2) + 12 \cdot 10^{-3}) \cdot 4 \cdot 500 \text{ s} \simeq 24 \text{ s} \end{aligned} \quad (5.1)$$

where *bits* is the number of bits in one UART transmission, 8 data bits plus a start and stop bit, and *length* is the length of the shiftregister. The brackets represents the time for one *write* and one *read* operation plus the necessary delay. 4 such operation are needed to write a full 32 bit pattern of data to the shiftregister, and is repeated as often as necessary to shift the pattern through the

whole shiftregister. Similar for a 16 bit pattern through a 8192 deep FIFO:

$$\begin{aligned} t &= ((1/\text{baudrate} \cdot \text{bits} \cdot 2) + 12 \text{ ms}) \cdot 2 \cdot \text{length} \\ t &= ((1/115200 \cdot 10 \cdot 2) + 12 \cdot 10^{-3}) \cdot 2 \cdot 8192 \text{ s} \simeq 200 \text{ s} \end{aligned} \quad (5.2)$$

These numbers are confirmed by the logfiles. A shift through time of 24 and 200 seconds is very poor considering the 66 MHz clock in the FPGA. But with a low beam flux causing only 1-2 upsets every 30 s, this gives an acceptable estimation of the configuration upset cross-section. For the FIFO the main type of upsets are single bit flips and not configuration upsets. This gives a longer "lifetime" of the test run due to a low occurrence of outputs experiencing configuration upsets. A long run of several times the shift through time, should secure an acceptable measurement for the FIFO design.

Equations 5.1 and 5.2 show that the main limitations are the delay of 12 ms and the length of the test array. Decreasing the delay below 10 ms gave incorrect data when reading the UART read buffer, and the delay therefore seemed to be a fixed constraint. One possible way of increasing the speed is to make use of the UART buffer in the PC. Increasing the number of bytes for each write and read operation will suppress the importance of the delay time. The 4 write and read operations in order to send 32 data bits to the FPGA, can be decreased to 1 by setting the *bytes* variable in the *write* and *read* functions to 4, reducing the delay time from 4 x 12 ms to only 1 x 12 ms for the shiftregister:

$$\begin{aligned} t &= (1/\text{baudrate} \cdot \text{bits} \cdot 2 \cdot 4 + 12 \text{ ms}) \cdot \text{length} \\ t &= (1/115200 \cdot 10 \cdot 2 \cdot 4 + 12 \cdot 10^{-3}) \cdot 500 \text{ s} \simeq 6 \text{ s} \end{aligned} \quad (5.3)$$

and from 2 x 12ms to 1 x 12 ms for the FIFO design:

$$\begin{aligned} t &= (1/\text{baudrate} \cdot \text{bits} \cdot 2 \cdot 2 + 12 \text{ ms}) \cdot \text{length} \\ t &= (1/115200 \cdot 10 \cdot 2 \cdot 2 + 12 \cdot 10^{-3}) \cdot 8192 \text{ s} \simeq 101 \text{ s} \end{aligned} \quad (5.4)$$

Table 5.4 gives a few more results varying the width and length of the FIFO and shiftregister designs. The numbers are calculated using the equations:

Table 5.4: The numbers are calculated using equation 5.5

FIFO				Shiftregister			
Width	Length	No. of bytes	Time [s]	Width	Length	No. of bytes	Time [s]
16	8192	2	101.1	32	512	4	6.5
32	4096	4	52.0	64	256	8	3.4
64	2048	8	27.4	128	128	16	1.9
128	1024	16	15.1	256	64	32	1.1
256	512	32	9.0	512	32	64	0.7
512	256	64	5.9	1024	16	128	0.5
1024	128	128	4.4	2048	8	256	0.5
2048	64	256	3.6	4096	4	512	0.4

$$\begin{aligned} t_{\text{fi fo}} &= (1/\text{baudrate} \cdot \text{bits} \cdot 2 \cdot \text{width}_{\text{fi fo}} + 12\text{ms}) \cdot \text{length}_{\text{fi fo}} \\ t_{\text{shift}} &= (1/\text{baudrate} \cdot \text{bits} \cdot 2 \cdot \text{width}_{\text{shift}} + 12\text{ms}) \cdot \text{length}_{\text{shift}} \end{aligned} \quad (5.5)$$

where *width* and *length* are respectively the width and length of the shiftregister or FIFO design, and the total number of resource used are 16384 registers and 131072 RAM bits. The column *No. of bytes* corresponds to the *bytes* in the *write* and *read* function. It also gives the size of the multiplexer that has to be implemented in the FPGA firmware design. From the table we can see that there is a limited effect when increasing the width by more than 512 bits. Decreasing the length and increasing the width will require a larger multiplexer design. Limiting the width to 128 bits, and using this as a starting point for the next iteration, the time to shift through a 128 bit pattern will be 15 s for a 1024 deep FIFO, and 3 s for a 128 long shiftregister. This change will increase the SEU detectability level considerably. It should be mentioned that these numbers are so far only calculations and have not yet been implemented.

# Chapter 6

## Irradiation test setup

### 6.1 Introduction

*Two facilities, the Oslo Cyclotron (OCL) and The(odor) Svedberg Laboratory (TSL), have been used for irradiation tests of the ALTERA APEX 20K FPGA. This chapter will give an overview of the test setup used at both facilities, where special attention will be given to the beam line configuration and monitoring*

### 6.2 Facilities and setup

Eventhough the OCL and TSL are different facilities, the principle of the irradiation test setup is similar and consists of the following parts:

**Cyclotron:** Beam energies of 29 MeV (OCL), 38 and 180 MeV (TSL)

**Beam line and target alignment:** Laser and optical survey system used for aligning the beam and DUT.

**Beam monitoring:** Absolute flux measurement, beam profile, and relative beam intensity or flux monitor.

**DUT:** Device Under Test, ALTERA APEX 20KE400EFC672.

**Readout software and hardware:** the DUT is mounted on the RCU prototype II card and is connected to the DAQ computer over a communication link. The readout software configures the FPGA and controls the communication between the DAQ computer and FPGA during an irradiation run.

**DAQ computer:** computer placed a few meters form the experiment setup, and runs the readout software. Connected to the remote computer over the local network. Linux OS.

**Remote computer:** used to remotely control the readout software from a shielded control room. Linux/Windows OS.

Figure 6.1 shows a conceptual overview of the common setup. Only the cyclotron and beam line

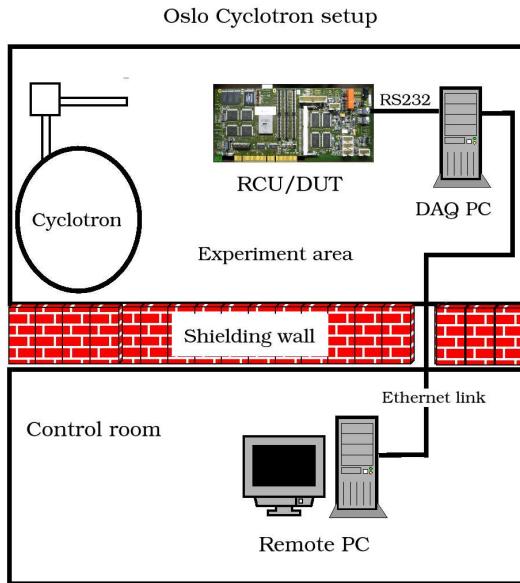


Figure 6.1: A conceptual overview of the irradiation test setup common for both OCL and TSL equipment are fixed at the facilities, while the other parts are reinstalled prior to every run.

### 6.2.1 The Oslo Cyclotron

The Oslo Cyclotron [37], is situated at the University of Oslo, Department of Physics. It is a Scanditronix MC-35 (fig. 6.2), and can accelerate protons,  $^3He$  and  $^4He$  to respectively 29, 48 and 35 MeV. Highest available intensity for protons is  $100\mu A$ . However, the intensities used for testing the APEX 20K is in the order of tens of pA.

#### Instrumentation setup

Figure 6.3 shows the schematic floorplan of the Cyclotron experiment hall. The laboratory is divided into two experiments halls and a shielded control room. The Cyclotron is situated in the innermost experiment hall, and the proton beam is deflected into different beam lines by bending magnets. A fixed setup area for irradiation tests of electronics is allocated at one of the beam lines in the outermost experiment hall, and highlighted in figure 6.3. The DUT is fixed in the beam path using a movable tripod in a distance 20-160 cm from the beam exit point. The DUT is mounted with its top surface perpendicular to the beam axis, see fig. 6.4(d). A laser, reflected in parallel with the beam path using a mirror, is used to align the DUT. The alignment procedure is carried out in three steps:

1. A high intensity proton beam, in the order of several times the test intensities, is used to illuminate a ceramic viewer fixed in the beam path, figure 6.4(a).



Figure 6.2: The Oslo Cyclotron inner experiment hall

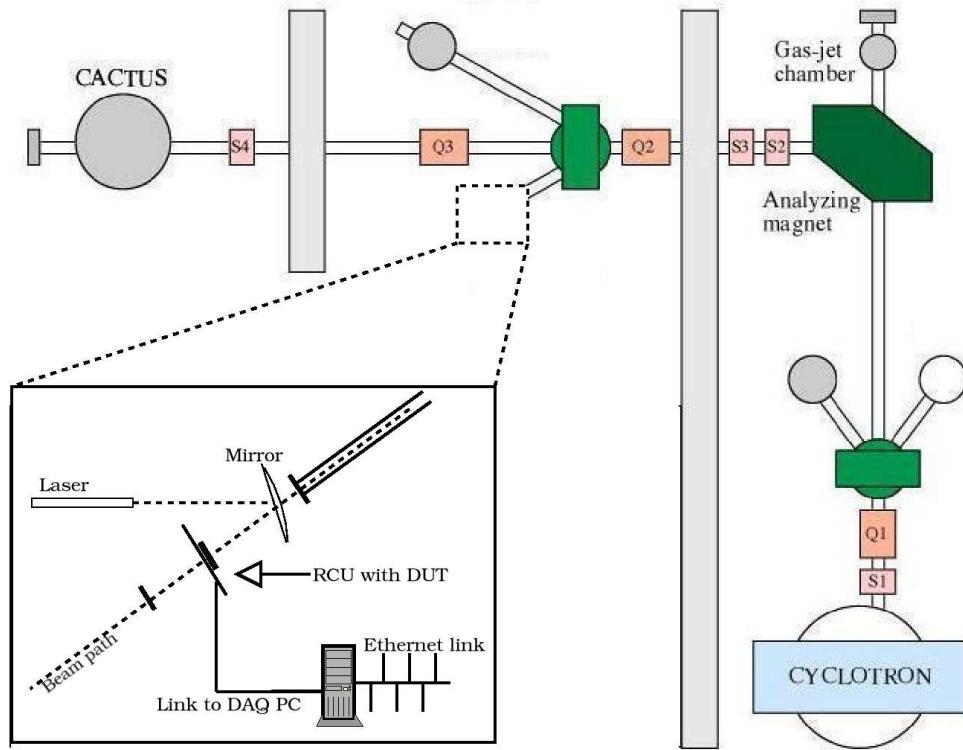


Figure 6.3: Schematic view of the Cyclotron beam line and fborplan

2. The beam is aligned as symmetrically as possible around a marking spot on the viewer, and monitored by a camera placed next to the setup and adjusted from the control room.
3. Switching the beam off, the laser is aligned with the marking spot before the viewer is removed and replaced by the DUT, figures 6.4(b) through 6.4(d).

A Linux computer, connected to an Ethernet link, is placed a few meters from the setup area and runs the DAQ software and hardware needed to run the tests and readout of the DUT. The experiment is supervised from a computer in the shielded control room.

### 6.2.2 The Svedberg Laboratory

The Svedberg Laboratory (TSL) [38] is a national research facility located in Uppsala, Sweden and hosted by Uppsala University. The experimental program at the laboratory covers a wide range of activities from basic research in subatomic physics, materials physics, accelerator physics, biomedicine and proton therapy to industrial applications. TSL provides neutron and proton beams, in the range 20-180 MeV, for irradiation testing of electronics.

#### Instrumentation setup

The physical setup for irradiation tests at TSL is in principle similar to the setup at OCL. Aligning the DUT a fixed distance upstream in the beam path is done with the aid of a laser. Different from the setup at OCL is that the laser is placed in parallel to, and at the end of the beam path. Figure 6.5 gives a full overview of the setup area at TSL. A graphite collimator (point 4 in fig. 6.5) is placed in the beam path, between the DUT and exit point of the beam, to limit the beam spot on the DUT. Thus also protecting other components on the RCU card. Section 6.4.1 treats the collimator and beam monitoring in further detail. The laser is raised to a level where it propagates through the opening of the collimator and hits the center of the beam exit point. Aligning the DUT in the beam path is done by mounting it so that the laser hits the center rear part of the device. During exposure, the laser is lowered out of the beam to avoid damage. During the 38 MeV irradiation period an optical alignment system was used to align the DUT in the beam path. The experiment computer is placed close to the setup and is shielded with a number of lead blocks, and the remote computer is situated in the counting room outside the experiment hall.

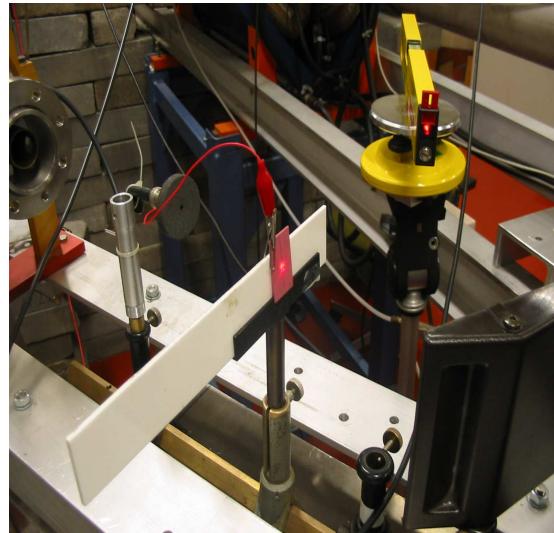
## 6.3 Device Under Test

The device tested is the ALTERA APEX20K400EFC672 [24] FPGA, and the basic architecture of the device has already been presented in section 3.4.2. Table 6.1 summarises the DUT properties.

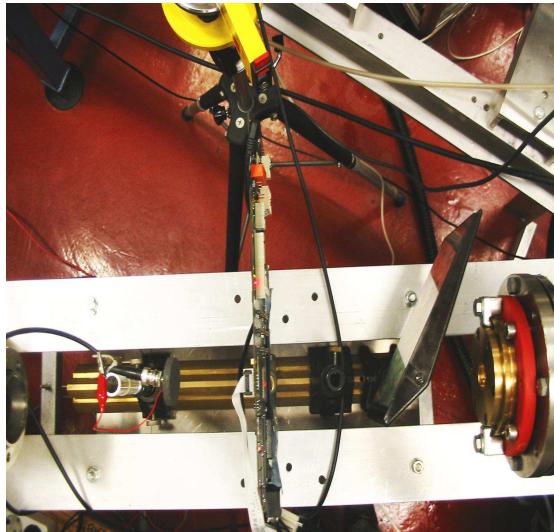
Irradiating the FPGA it is important to know whether the beam hits all of the sensitive area of the device. Thus knowledge about the physical size of the sensitive die area and its position in the FPGA package is crucial. The package size, 27 mm x 27 mm for the APEX FPGA, is



(a)



(b)



(c)



(d)

Figure 6.4: a) A high intensity proton beam, above 1nA, illuminates the ceramic viewer. The beam is aligned with the cross falling in the center of the beam spot. b) The laser is mirrored in parallel with the beam path and aligned with the cross on the ceramic viewer. The ceramic viewer is connected to the gray circular Faraday cup using a normal wire. c) The RCU and DUT is mounted int the beam path. d) Laser spot is aligned to the center of the DUT.

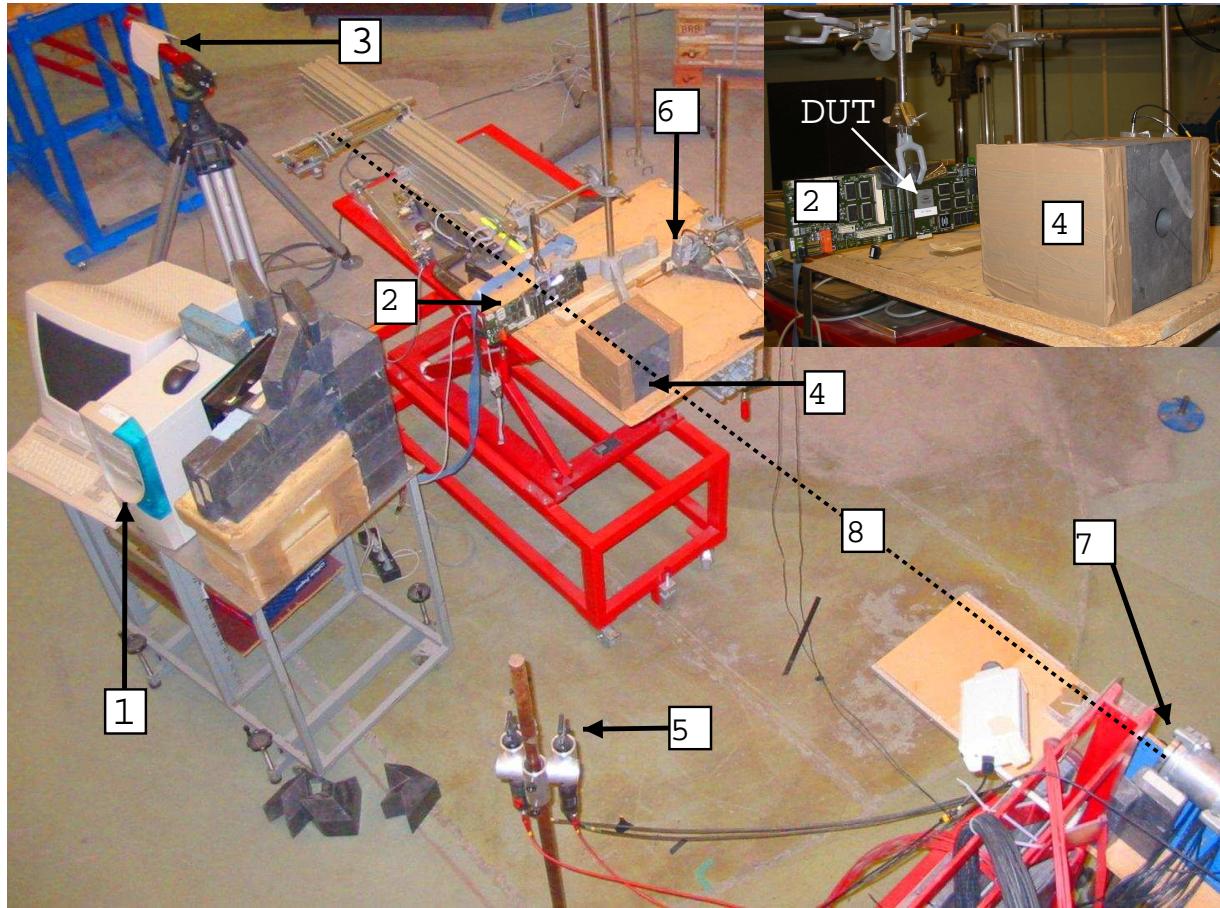


Figure 6.5: Irradiation setup at The Svedberg Laboratory Blue Hall

1. Experiment DAQ PC, 2. RCU prototype II card and DUT, 3. Alignment laser, 4. Graphite collimator, 5. Scintillation telescope(relative flux monitoring), 6. TFBC for flux and beam profile measurement, 7. Beam exit point, 8. Beam line/path

Table 6.1: Device under test information,[24]

Device	<b>APEX20KE400EFC672</b>
Typical Gates	400000
Maximum System Gates	1051648
Logic elements	16640
Maximum RAM bits	212992
Phase-Locked Loops (PLLs)	4
Speed Grades	-2/-1
Maximum User I/O Pins	488
Internal voltage	1.8V
MultiVolt I/O operation	3.3V, 2.5V, 1.8V
Package [mm]	672-Pin FineLine BGA Package (27x27)
Die size	approximately 11 mm x 11 mm
Manufacturing process	0.18 um CMOS, 8-Layer aluminum process

larger than the chip die which is placed in the center of the package. Large parts of the package it therefore only wiring from the die to the pins of the device. Having an evenly distributed beam spot covering the whole FPGA package should be sufficient. Information about the total number of configuration bits, number of configuration bits connected to I/O pins, and the physical distribution of these bits is also considered to be of high importance. Some of this information is confidential and not accessible for the general users outside ALTERA. The physical die size of the chip was however obtained by opening a defect device and measuring it to be approximately 11 mm x 11 mm.

## 6.4 Beam line intensity and monitoring

The difference in the beam line configuration and monitoring between the two facilities showed to be of great importance to the results of the irradiation measurements. An unexpected difference between the first 180 MeV proton beam irradiation test at TSL and the already conducted test at 28 MeV in Oslo, lead to a major change in the beam monitoring method in Oslo. New irradiation tests were first carried out at TSL with a proton energy of 38 MeV. This was the energy that was offered closest to the 28 MeV beam in Oslo. The 38 MeV irradiation gave a result consistent with the 180 MeV measurements, The following section will show how the change of beam monitoring methods can explained the discovered difference.

### 6.4.1 The Svedberg Laboratory beam line setup

TSL serves as a commercial site with experience in irradiation testing of electronic components. Thus it is expected that their beam line configuration and monitoring methods are reliable. This section is based on the beam line configuration and monitoring notes in appendix A. Figure 6.5 shows an overview of the setup area at TSL. When the proton beam exits the vacuum pipe and enters the experiment hall it exits through a circular opening with a diameter of 8 cm. A graphite collimator, approximately a cube of 16x16x16 cm, with a circular opening of 30 mm in diameter is placed 3-4 meters upstream the beam path. It will narrow down the beam so that it will only hit the FPGA, hence also protect the other circuits on the card.

During irradiation, the beam flux is monitored by a scintillation telescope measuring the scattered beam at an angle relative to the beam path, see point 5 in figure 6.5. The proton flux is proportional to the count rate of the scintillation telescope, see table 6.5. The flux is measured using a Thin Film Breakdown Counter (TFBC) [39] [40]. The TFBC is made up of a double-sided  $1 \text{ cm}^2$  uranium target and two Thin Film Breakdown Counters placed on both sides of the target surface. When the proton hit the Uranium target a fission reaction takes place and the fission fragments created in the reaction ionise the silicon material in the TFBC. Protons do not create enough charge to induce a signal in the silicon material. It can only be used at low intensities and allows measurements of the absolute proton flux. A sample of such a counter is shown in figure. 6.8(a) and 6.8(b). The counting rate is proportional to the proton flux, and this calibration is known for the target isotope, target thickness and the energy of the proton beam.

At the end of each irradiation run the counter value from the scintillation telescope is collected together with the duration of the test period.

### Beam profile

The beam profile is measured by positioning the TFBC in different positions along the vertical ( $y$ ) and horizontal ( $x$ ) axis, and it is normalised against the scintillation telescope. Two irradiation periods have been carried out at the TSL, both having the same beam line configuration and monitoring. Figures 6.7 and 6.6 shows the beam profile for the 38 MeV and 180 MeV run respectively. While the profile in both  $x$ - and  $y$ -axis were measured for the 28 MeV, only the  $x$ -axis was done for the 180 MeV. The dotted lines in the plots shows the expected geometric

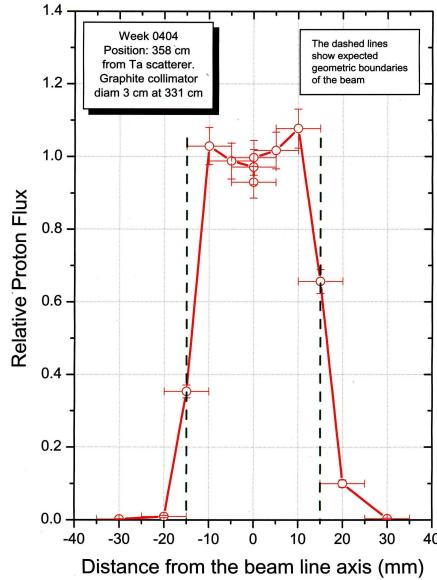


Figure 6.6: Beam profile, 180 MeV, measured by positioning the TFBC in different positions along the  $x$ -axis

boundaries of the graphite collimator (diameter of 30 mm). The beam profile is defined as the Full Width Half Maximum (FWHM) of the plots. With a chip size of 27 mm  $\times$  27 mm and a die size of approximately 11mm  $\times$  11mm, a beam profile of a diameter of 30mm should be sufficient to make sure that the whole sensitive area of the FPGA will be irradiated. Table 6.5 lists the estimated beam profiles for the TSL irradiation periods.

#### 6.4.2 Oslo cyclotron beam line setup

The beam is defocused and made divergent by the last quadrupole. A quadratic collimator, 1 cm  $\times$  1 cm, is placed at the beam exit point, inside the the vacuum pipe, along with a gold foil at the

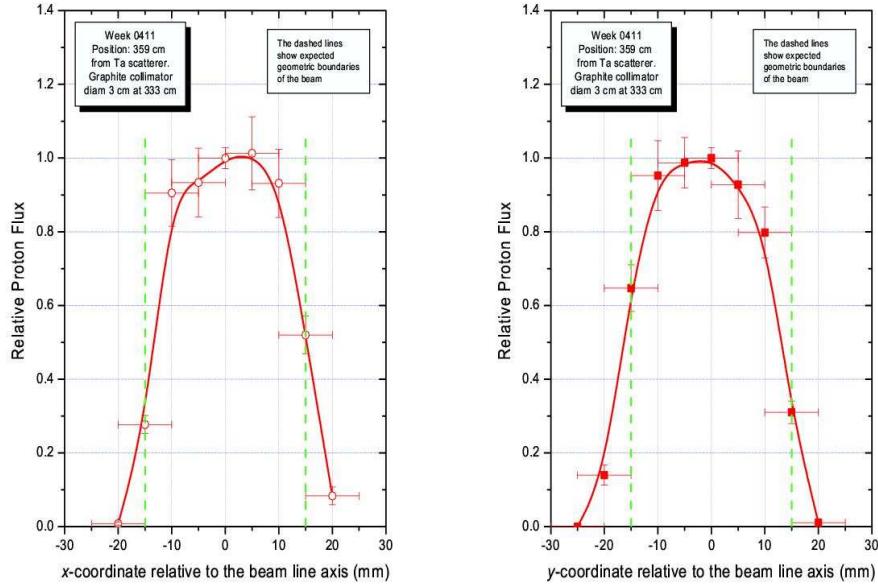


Figure 6.7: Beam profile, 38 MeV, measured by positioning the TFBC in different positions along the x- and y-axis

exit window to make the distribution as uniform as possible. Two different methods of measuring the beam flux have been used at OCL:

1. Flux measurement using a Faraday cup
2. Flux Measurement, using a Thin Film Breakdown Counter (TFBC)

The beam and DUT is aligned using the illuminated ceramic viewer and a laser. Before irradiation the beam intensity is adjusted to the pre-selected value using an amperemeter on the control desk. During irradiation there is no equipment for relative flux measurement. Due to the interactions in the target and the air the absolute current measurement using the Faraday cup is unstable. After irradiation the DUT is removed and the ceramic viewer is replaced in the beam path. A new intensity measurement is done to look for any drift in current and alignment since the first measurement.

At low intensities current measurements using the Faraday cup are not accurate. A second method of measuring the flux at OCL involved using as similar measurement equipment as at TSL, except for the relative monitor (scintillation telescope). Two new Thin Film Breakdown Counters were therefore put together for use at OCL, in addition to a custom made beam profile measuring target. Figure 6.8(a) and 6.9 shows the TFBC and the beam profile measuring target.

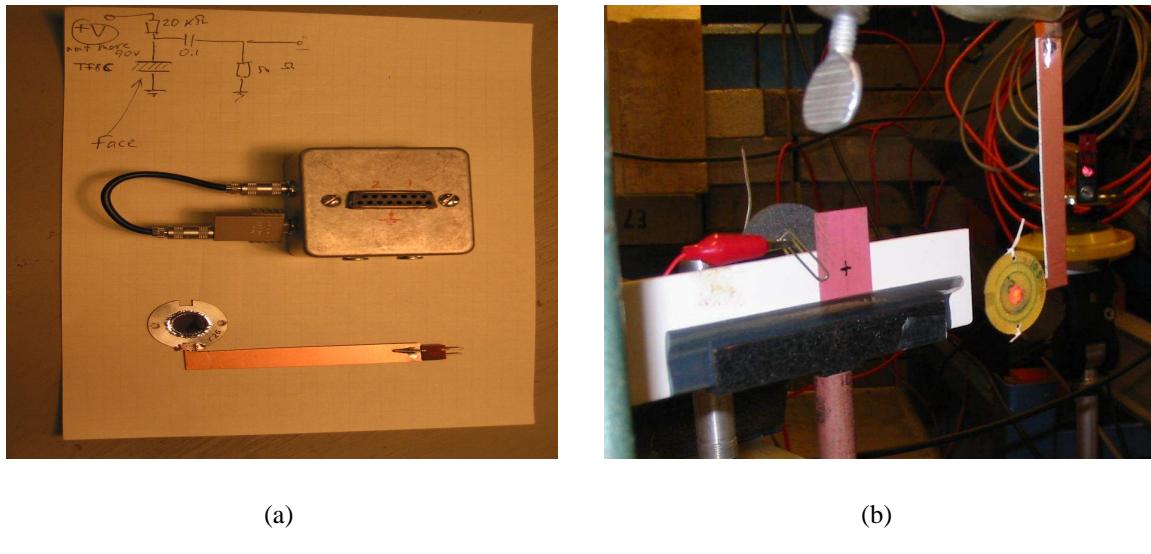


Figure 6.8: Thin Film Breakdown Counters

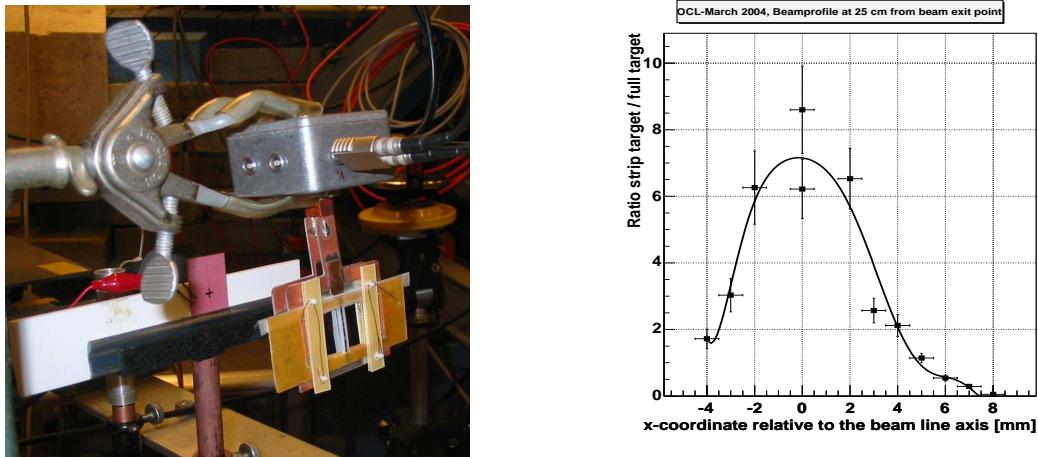


Figure 6.9: Beam profile measuring target

Figure 6.10: x-coordinate of the beam profile at setup position 25 cm from beam exit point

### Beam profile

During the first irradiation runs in Oslo no accurate beam profile was measured. To a first approximation the illuminated beam spot on the ceramic viewer was used as a reference, knowing the geometry of the viewer.

The profile measuring device used for the last period consists of two uranium targets and counters. One quadratic uranium target of 22 mm x 22 mm, and a thicker uranium strip target of 1 mm x 22 mm. The beam profile is measured by moving the strip target along the horizontal and vertical axis Plotting the ratio of counts between the strip target and the quadratic target gives the measurement of the beam profile. In order to improve the profile measurement done at the first setup location 25 cm from the beam exit point, a new measurement was done at the same position. Figure 6.10 shows that the profile is about 6 mm for the horizontal direction, less than the expected 10 mm. The profile was only done for the x-direction.

In order to increase the beam spot, the setup was moved further away to a position 161 cm away from the beam exit point. New measurements were done, both in x- and y-direction, and the plots are shown in figure 6.11 and 6.12.

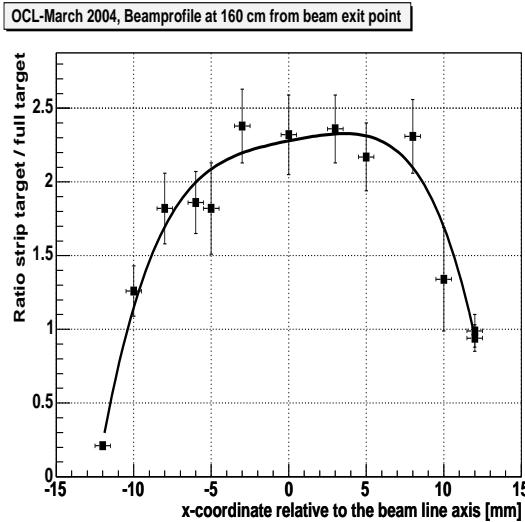


Figure 6.11: The beam profile in horizontal direction

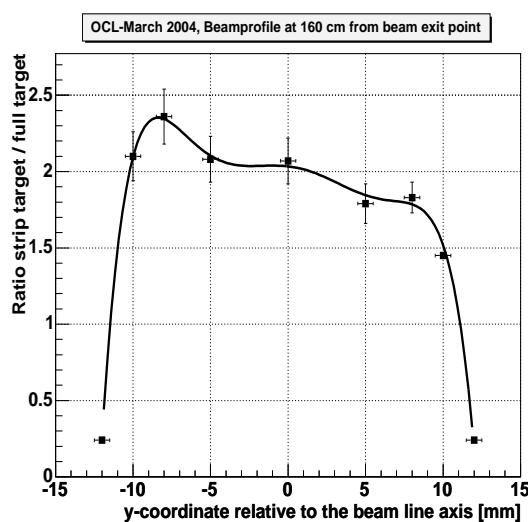


Figure 6.12: The beam profile in vertical direction

### 6.4.3 Remarks on the beam line monitoring methods

There are several remarks to be made for the intensity measurements. First of all it is the discovery of the narrow beam profile. With such a narrow beam spot, the accuracy of the aligning methods becomes crucial. But even with perfect aligning the beam spot will not cover the whole sensitive area of the FPGA. Further the flux is calculated as the current divided by the elementary charge, and defined to be per  $\text{cm}^2$ . This is the current measured on the Faraday. Eventhough the

intensity is rather small outside the beam profile boundaries, it is hard to say if it is negligible. Also the fact that the area of the intensity plateau is smaller than  $1 \text{ cm}^2$ , makes the flux calculation incorrect. Thus a correction has to be done in order compensate for this. Infact that these calculation were incorrect was discovered after the first irradiation run in the 180 MeV proton beam at TSL. TSL results of a factor 20-30 higher than the 28 MeV results were not expected. Thus leading to the new flux measurements methods described, and confirmation that the old flux measurements were incorrect.

Ionisation of the air will also contribute to the total current measured. Positioning the Faraday cup at different positions gives a higher measured current when it is moved further away from the exit point<sup>1</sup>. Another source of uncertainty is the internal sensitivity of the amperemeter for the low intensities used in the irradiation tests. A simple test connecting a small fixed current source to the amperemeter show the same instability as experienced during irradiation measurements. At an intensity of 15 pA there is as much as a  $\pm 5\text{pA}$  fluctuation in the measurements. When most of the irradiation measurements for the FPGA are carried out at intensities below 30-40pA, one can argue if the the results gathered from these measurements can be regarded as valid or not.

#### 6.4.4 Scaling measurements

In order to present the results from the measurement carried out using the old beam monitoring method, an approach to the scaling of these results will be introduced.

Measuring the beam profile at the old setup position approximately 25 cm from the beam exit point, revealed a smaller beam spot than assumed. Figure 6.10 shows a plot measured with the beam profile measured with the custom made beam profile measuring target. Assuming this measurement to be somewhat symmetrical in the y-direction, the HWFM gives an approximate beam profile of  $6 \text{ mm} \times 6 \text{ mm}$ . Thus the old measurements first have to be scaled for this reduced beam spot. Flux correction:

$$\text{Flux}(old)_{corrected} = \frac{\text{Flux}(old)}{0.36} [\text{protons}/\text{cm}^2\text{s}] \quad (6.1)$$

When we know that the cross-section is calculated as

$$CS(old) = \frac{\#SEU}{\text{Flux} \cdot \text{time}} [\text{cm}^2] \quad (6.2)$$

the correction for the beam spot will decrease the old cross-section results so that

$$CS(old)_{corrected,I} = \frac{\#SEU}{\text{Flux}(old)_{corrected} \cdot \text{time}} [\text{cm}^2] \quad (6.3)$$

This account for a die size of  $1 \text{ cm}^2$ , but infact it is larger<sup>2</sup>. In order to make sure that we cover the whole die size an additional safety factor is added. Thus the correction of the old cross-section

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<sup>1</sup>The current was measured at 35 cm, 73 cm, 161 cm and gave respectively 250 pA, 300 pA, 700 pA

<sup>2</sup>approximately measured to  $11 \text{ mm} \times 11 \text{ mm}$  by opening a chip

measurements is

$$CS(old)_{corrected,II} = \frac{\#SEU}{Flux(old)_{corrected} \cdot time} \cdot A \text{ [cm}^2\text{]} \quad (6.4)$$

where  $A$  is

$$A = \frac{A_{die}}{0.36} \text{ [cm}^2\text{]} \quad (6.5)$$

and  $A_{die}$  is the area of the die included the safety margin. Thus the final correction of the old cross-section measurement is

$$CS(old)_{corrected,II} = \frac{\#SEU}{Flux(old) \cdot time} \cdot A_{die} \text{ [cm}^2\text{]} \quad (6.6)$$

So far the flux and cross-section measurements are only corrected for the small beam spot and larger die size. In addition the flux measurements using the TFBC showed a difference compared to the intensity measurements using the Faraday cup. This scaling factor for the proton beam at the old setup positng had to be measured using both the Faraday cup and the TFBC, for thereafter to compare the results. The result of this calibration measurement is shown in figure 6.13, where the ratio between the flux measurement using the Faraday cup and the flux measurement using the TFBC is plotted. Table 6.2 gives the calibration factor for the various intensity values

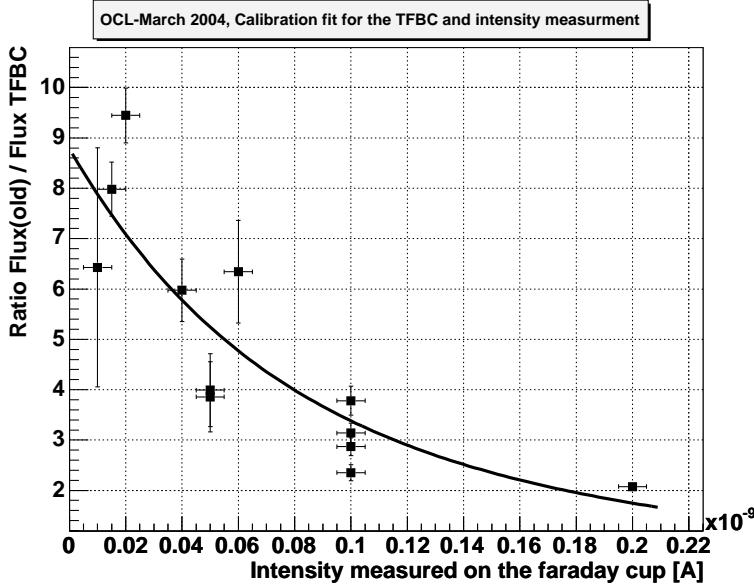


Figure 6.13: A fit of the ratio between the flux measurement using the Faraday cup and the flux measurement using the TFBC

used in the irradiation tests.

Table 6.2: Fit ratio between intensity and flux measurements

Current [pA]	Fit ratio
10	7.8
20	7.0
25	6.8
30	6.4
40	5.8

### Scaling of old results

Table 6.4.4 presents the unscaled and scaled cross-section and flux measurements from 28 MeV proton irradiation for the shiftregister design (32 x 400) using the SCSN communication interface.

Table 6.3: Cross-section for configuration upsets, 28 MeV proton irradiation using the shifregister design(32 x 400).

Current [pA]	Unscaled		Scaled	
	Flux [p/cm <sup>2</sup> s]	CS [cm <sup>2</sup> ]	Flux [p/cm <sup>2</sup> s]	CS [cm <sup>2</sup> ]
10	$6.3 \cdot 10^7$	$5.8 \cdot 10^{-11} \pm 2.8 \cdot 10^{-11}$	$1.7 \cdot 10^8$	$9.3 \cdot 10^{-10} \pm 4.6 \cdot 10^{-10}$
20	$1.3 \cdot 10^8$	$1.7 \cdot 10^{-10} \pm 6.0 \cdot 10^{-11}$	$3.5 \cdot 10^8$	$2.5 \cdot 10^{-9} \pm 8.7 \cdot 10^{-10}$
25	$1.6 \cdot 10^8$	$3.7 \cdot 10^{-10} \pm 5.6 \cdot 10^{-11}$	$4.3 \cdot 10^8$	$5.2 \cdot 10^{-9} \pm 8.0 \cdot 10^{-10}$
30	$1.9 \cdot 10^8$	$3.0 \cdot 10^{-10} \pm 1.3 \cdot 10^{-10}$	$5.2 \cdot 10^8$	$3.9 \cdot 10^{-9} \pm 1.7 \cdot 10^{-9}$
40	$2.5 \cdot 10^8$	$3.4 \cdot 10^{-10} \pm 4.4 \cdot 10^{-11}$	$6.9 \cdot 10^8$	$4.1 \cdot 10^{-9} \pm 5.4 \cdot 10^{-10}$
Mean CS		$2.5 \cdot 10^{-10} \pm 4.1 \cdot 10^{-11}$		$3.3 \cdot 10^{-9} \pm 4.4 \cdot 10^{-10}$

Similar scaling of the results from the irradiation test for the FIFO design 32 x 4096 using the SCSN communication interface is presented in table 6.4. Tables 6.5 and 6.6 summarises the beam line configuration and monitoring at TSL and OCL.

Table 6.4: Cross-section single bit flips, 28 MeV proton irradiation using the FIFO design(32 x 4096).

Current [pA]	Unscaled		Scaled	
	Flux [p/cm <sup>2</sup> s]	CS [cm <sup>2</sup> ]	Flux [p/cm <sup>2</sup> s]	CS [cm <sup>2</sup> ]
10	$6.3 \cdot 10^7$	$1.9 \cdot 10^{-10} \pm 9.4 \cdot 10^{-11}$	$1.7 \cdot 10^8$	$3.1 \cdot 10^{-9} \pm 1.5 \cdot 10^{-9}$
20	$1.3 \cdot 10^8$	$3.6 \cdot 10^{-10} \pm 1.6 \cdot 10^{-10}$	$3.5 \cdot 10^8$	$5.2 \cdot 10^{-9} \pm 2.4 \cdot 10^{-9}$
25	$1.6 \cdot 10^8$	$5.4 \cdot 10^{-10} \pm 2.9 \cdot 10^{-10}$	$4.3 \cdot 10^8$	$7.6 \cdot 10^{-9} \pm 4.2 \cdot 10^{-9}$
30	$1.9 \cdot 10^8$	$6.9 \cdot 10^{-10} \pm 4.5 \cdot 10^{-10}$	$5.2 \cdot 10^8$	$9.2 \cdot 10^{-9} \pm 6.0 \cdot 10^{-9}$
40	$2.5 \cdot 10^8$	$3.5 \cdot 10^{-10} \pm 2.3 \cdot 10^{-11}$	$6.9 \cdot 10^8$	$4.3 \cdot 10^{-9} \pm 2.8 \cdot 10^{-9}$
Mean CS		$4.3 \cdot 10^{-10} \pm 1.0 \cdot 10^{-10}$		$5.9 \cdot 10^{-9} \pm 1.7 \cdot 10^{-9}$

Table 6.5: Summary of the beam line configuration at OCL for the two different monitoring methods

Test period	OCL 29 MeV (I)	OCL 29 MeV (II)
Particle energy nominal	29 MeV	29 MeV
Particle energy delivered by cyclotron	29 MeV	29 MeV
Particle energy deduced at exit of beam line	28 MeV	28 MeV
Particle energy deduced at TFBC target	27.5 MeV	24.6 MeV
Irradiation setup and absolute monitoring position	25cm	161cm
Beam profile	~ 6 mm x 6 mm	21 mm x 22 mm (x-y direction)
Beam profile equipment	Digital camera -Ceramic viewer: 2.2 cm x 3.5 cm	TFBC
Beam flux measurement	Faraday cup	TFBC
Beam monitors	-Faraday cup 3.8 cm diameter -Amperemeter:610CR Solid State Electrometer; Keithley Instruments	-Faraday cup: 3.8cm diameter -Amperemeter:610CR Solid State Electrometer; Keithley Instruments

Table 6.6: Summary of the beam line configuration at TSL

Test period	January, 180 MeV	March, 38 MeV
Particle energy nominal	180 MeV	38 MeV
Particle energy delivered by cyclotron	177 MeV	38 MeV
Particle energy deduced at exit of beam line	171 MeV	37 MeV
Particle energy deduced at TFBC target	171	34.2 MeV
Beam-shaping equipment	Tantalum scattering foil, 1.5mm	Tantalum scattering foil, 0.08mm
Collimator	Graphite cube (16 cm x16 cm x 16 cm) circular opening of 33mm	Graphite cube (16x16x16 cm) circular opening of 33mm
Position of Collimator from scattering foil	419 cm	333 cm
Irradiation setup and absolute monitoring position	445 cm	359 cm
Relation between the beam flux and the monitor count rate $r$	$j=3.5 \cdot 10^4 \cdot r$	$j=3.9 \cdot 10^4 \cdot r$
Beam profile	20 mm in x-direction	20 mm x 20 mm (x-y direction)
Beam profile equipment	TFBC	TFBC
Beam flux measurement	TFBC	TFBC
Beam monitors	Scintillation telescope	Scintillation telescope

# Chapter 7

## Results of SEU cross-section measurements

The results presented in this chapter are based on one period of irradiation runs for each of the proton energies used. That is, the period giving the best statistical results from the 28 MeV proton irradiation in Oslo, and the 38 MeV and 180 MeV runs at TSL. The OCL results also includes the results from the last irradiation test using the new beam monitoring equipment.

### 7.1 Results at 180 MeV

Table 7.1 lists the result from the irradiation test using the shiftregister design (32 x 500) with the UART communication interface. Table 7.2 lists the results from the irradiation test using the FIFO design (16 x 8192) with the UART communication interface. The results can be summarised as follows:

**180 MeV, shiftregister design:** during 18 runs of in total 4 hours exposure only 9 single bit flips were detected compared to 213 configuration upsets.

*Mean cross-section configuration SEU:*  $5.4 \cdot 10^{-9} \pm 1.0 \cdot 10^{-9} \text{ cm}^2$

**180 MeV, FIFO design:** during 8 runs of in total 1 hour exposure 77 single bit flips were detected while 6 configuration related upsets were experienced

*Mean cross-section:*  $7.7 \cdot 10^{-9} \pm 1.9 \cdot 10^{-9} \text{ cm}^2$

Table 7.1: Configuration upset rate and cross-section for the **shiftregister design**

Energy	Flux [protons/cm <sup>2</sup> s]	Upset/s	cross-section [cm <sup>2</sup> ]
180 MeV	$2.0 \cdot 10^6$	$1.3 \cdot 10^{-2}$	$6.2 \cdot 10^{-9} \pm 2.6 \cdot 10^{-9}$
180 MeV	$3.8 \cdot 10^6$	$2.1 \cdot 10^{-2}$	$5.6 \cdot 10^{-9} \pm 1.2 \cdot 10^{-9}$
180 MeV	$7.8 \cdot 10^6$	$4.1 \cdot 10^{-2}$	$5.3 \cdot 10^{-9} \pm 1.2 \cdot 10^{-9}$
180 MeV	$1.6 \cdot 10^7$	$6.7 \cdot 10^{-2}$	$4.4 \cdot 10^{-9} \pm 5.6 \cdot 10^{-10}$
Mean CS 180 MeV			$5.4 \cdot 10^{-9} \pm 1.0 \cdot 10^{-9}$

The tables are plotted in figures 7.1 through 7.4. The cross-section curve is expected to be independent of the flux. Looking at the figures the cross-section measurements are consistent for

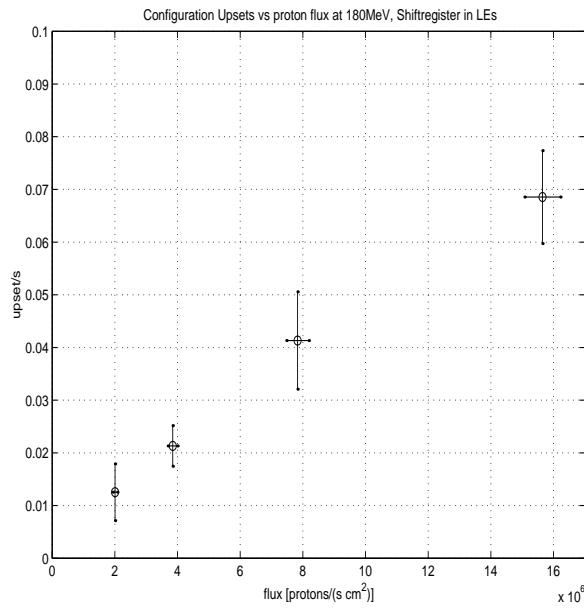


Figure 7.1: Configuration upset rate in registers versus proton flux at 180MeV

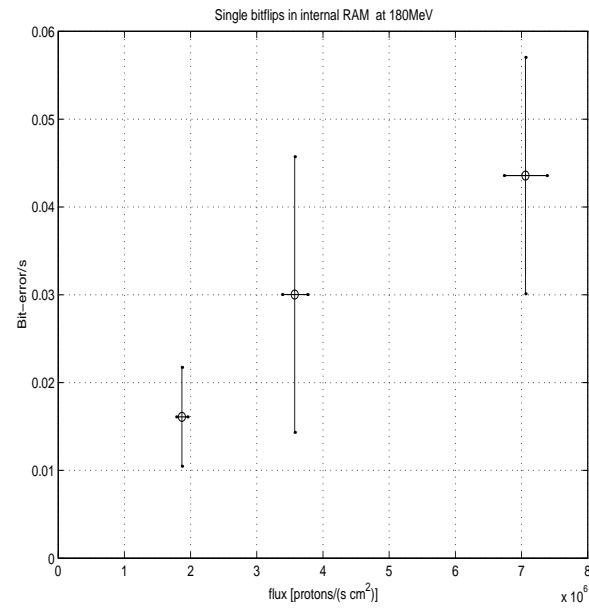


Figure 7.2: Single bitflip upset rate in internal RAM versus proton flux at 180MeV

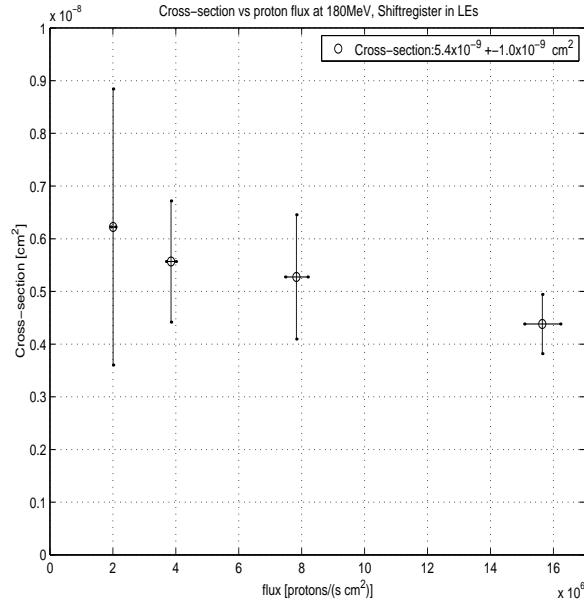


Figure 7.3: Cross-section for configuration upsets in registers versus proton flux at 180MeV

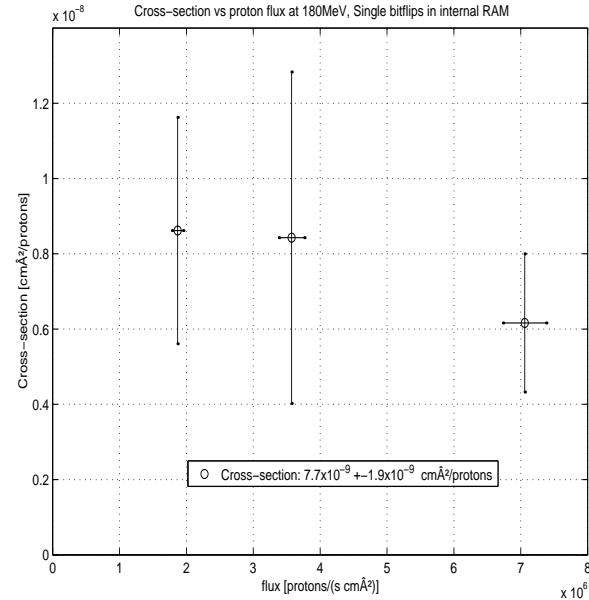


Figure 7.4: Cross-section for single bitflip upsets in internal RAM versus proton flux at 180MeV

Table 7.2: Single bit flip upset rate and cross-section for the **FIFO design**

Energy	Flux [protons/cm <sup>2</sup> s]	Upset/s	cross-section [cm <sup>2</sup> ]
180 MeV	$1.9 \cdot 10^6$	$1.6 \cdot 10^{-2}$	$8.6 \cdot 10^{-9} \pm 3.0 \cdot 10^{-9}$
180 MeV	$3.6 \cdot 10^6$	$3.0 \cdot 10^{-2}$	$8.4 \cdot 10^{-9} \pm 4.4 \cdot 10^{-9}$
180 MeV	$7.1 \cdot 10^6$	$4.4 \cdot 10^{-2}$	$6.2 \cdot 10^{-9} \pm 1.8 \cdot 10^{-9}$
Mean CS 180 MeV			$7.7 \cdot 10^{-9} \pm 1.9 \cdot 10^{-9}$

different flux values, and the upset rate shows a linear dependence on the flux as expected. It seems like there is a small decrease in the cross-section for increasing flux. This can be related to the limitations in the test methods. As the flux increases the upset rate increases. Due to the limitations in the readout speed and the number of outputs of the shiftregister, increasing upset rates will decrease the designs ability to detect the upsets.

## 7.2 Results at 38 MeV

During the 38 MeV irradiation only the shiftregister design (32 x 500) using the UART interface was tested.

**38 MeV, shiftregister:** during 11 runs of in total 1.5 hours exposure only 2 single bit flips were detected compared to 70 configuration upsets.

*Mean cross-section configuration SEU:*  $6.9 \cdot 10^{-9} \pm 2.1 \cdot 10^{-9} \text{ cm}^2$

Table 7.3: Single bit flip upset rate and cross-section for the **shiftregister design**

Energy	Flux [protons/cm <sup>2</sup> s]	Upset/s	cross-section [cm <sup>2</sup> ]
38 MeV	$2.0 \cdot 10^6$	$1.4 \cdot 10^{-2}$	$6.9 \cdot 10^{-9} \pm 2.1 \cdot 10^{-9}$
Mean CS 38 MeV			$6.9 \cdot 10^{-9} \pm 2.1 \cdot 10^{-9}$

The 38 MeV run in table 7.3 gives the average result of the measurements done at 38MeV with a flux of  $2.0 \times 10^6$  [protons/cm<sup>2</sup>s]. A cross-section of  $6.9 \times 10^{-9} \text{ cm}^2$  is consistent with the 180MeV measurements, thus indicating that the 38MeV and 180MeV point is both on the saturation part of the cross-section curve.

## 7.3 Results 28 MeV

The results for the 28 MeV irradiation period are scaled in reference to section 6.4.4, and are listed in table 7.4 for the shiftregister design (32 x 400) and in table 7.5 for the FIFO design (32 x 4096) Both designs are using the SCSN interface.

**28 MeV, shiftregister design:** during 21 runs of in total 3.5 hours exposure no single bit flips were detected compared to 201 configuration upsets.

*Mean cross-section configuration SEU:*  $3.3 \cdot 10^{-9} \pm 4.4 \cdot 10^{-10} \text{ cm}^2$

**28 MeV, FIFO design:** during 19 runs of in total 3.5 hours exposure 327 single bit flips were detected while 68 configuration related upsets were experienced

$$\text{Mean cross-section: } 5.9 \cdot 10^{-9} \pm 1.7 \cdot 10^{-9} \text{ cm}^2$$

Table 7.4: Cross-section for configuration upsets, 28 MeV proton irradiation using the shifregister design.

Current [pA]	Flux [p/cm <sup>2</sup> s]	Upsets/s	CS [cm <sup>2</sup> ]
10	$1.7 \cdot 10^8$	$3.6 \cdot 10^{-3}$	$9.3 \cdot 10^{-10} \pm 4.6 \cdot 10^{-10}$
20	$3.5 \cdot 10^8$	$2.1 \cdot 10^{-2}$	$2.5 \cdot 10^{-9} \pm 8.7 \cdot 10^{-10}$
25	$4.3 \cdot 10^8$	$5.8 \cdot 10^{-2}$	$5.2 \cdot 10^{-9} \pm 8.0 \cdot 10^{-10}$
30	$5.2 \cdot 10^8$	$5.6 \cdot 10^{-2}$	$3.9 \cdot 10^{-9} \pm 1.7 \cdot 10^{-9}$
40	$6.9 \cdot 10^8$	$8.4 \cdot 10^{-2}$	$4.1 \cdot 10^{-9} \pm 5.4 \cdot 10^{-10}$
Mean CS 28 MeV			$3.3 \cdot 10^{-9} \pm 4.4 \cdot 10^{-10}$

Table 7.5: Cross-section single bit flips, 28 MeV proton irradiation using the FIFO design.

Current [pA]	Flux [p/cm <sup>2</sup> s]	Upsets/s	CS [cm <sup>2</sup> ]
10	$1.7 \cdot 10^8$	$1.2 \cdot 10^{-2}$	$3.1 \cdot 10^{-9} \pm 1.5 \cdot 10^{-9}$
20	$3.5 \cdot 10^8$	$4.5 \cdot 10^{-2}$	$5.2 \cdot 10^{-9} \pm 2.4 \cdot 10^{-9}$
25	$4.3 \cdot 10^8$	$8.3 \cdot 10^{-2}$	$7.6 \cdot 10^{-9} \pm 4.2 \cdot 10^{-9}$
30	$5.2 \cdot 10^8$	$1.3 \cdot 10^{-1}$	$9.2 \cdot 10^{-9} \pm 6.0 \cdot 10^{-9}$
40	$6.9 \cdot 10^8$	$8.9 \cdot 10^{-2}$	$4.3 \cdot 10^{-9} \pm 2.8 \cdot 10^{-9}$
Mean CS 28 MeV			$5.9 \cdot 10^{-9} \pm 1.7 \cdot 10^{-9}$

In figure 7.7 and 7.8 the plots for the cross-section do not show a clear independency of the flux as for the 180 MeV results. This can be related to uncertainties due to the old flux measurement methods.

## 7.4 Results at 25 MeV

After the new beam monitoring equipment was installed at OCL in march, a new irradiation run was carried out. The FPGA was placed 161 cm upstream from the exit point of the proton beam

Table 7.6: Cross-Section for configuration upsets in sequential logic

Energy	Flux [protons/cm <sup>2</sup> s]	Upsets/s	CS config [cm <sup>2</sup> ]
25MeV	$3.6 \cdot 10^6$	$1.3 \cdot 10^{-2}$	$3.2 \cdot 10^{-9} \pm 1.1 \cdot 10^{-9}$
25MeV	$7.2 \cdot 10^6$	$2.3 \cdot 10^{-2}$	$3.8 \cdot 10^{-9} \pm 9.5 \cdot 10^{-10}$
Mean CS			$3.4 \cdot 10^{-9} \pm 9.6 \cdot 10^{-10}$

where the beam profile was measured to be approximately 21 mm x 22 mm. Estimated loss of energy for a 28 MeV proton in air is 21 keV/cm [13], which gives an approximately decrease in energy of 3.4 MeV before the beam hits the FPGA. Thus the beam has an energy of around 25 MeV at the interaction point. Four runs were made at a flux of  $7.2 \cdot 10^6$  [p/cm<sup>2</sup>s] and three at

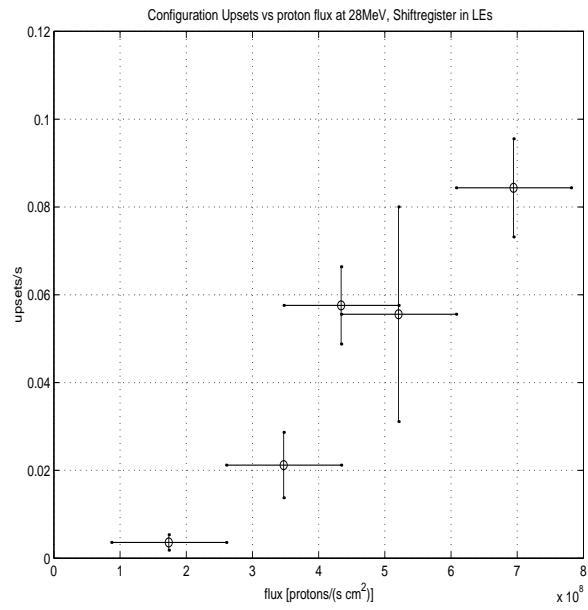


Figure 7.5: Configuration upset rate in registers versus proton flux at 28 MeV

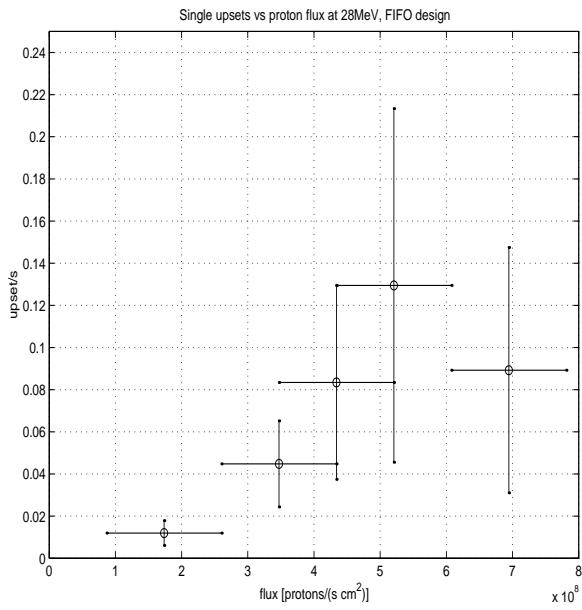


Figure 7.6: Single bitflip upset rate in internal RAM versus proton flux at 28 MeV

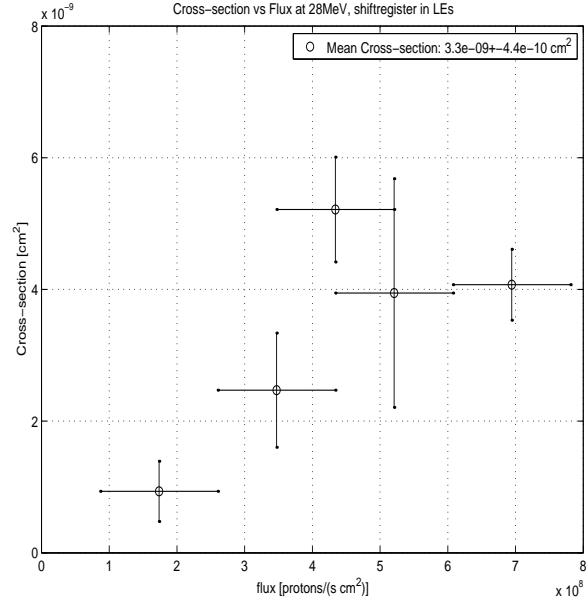


Figure 7.7: Cross-section for configuration upsets in registers versus proton flux at 28 MeV

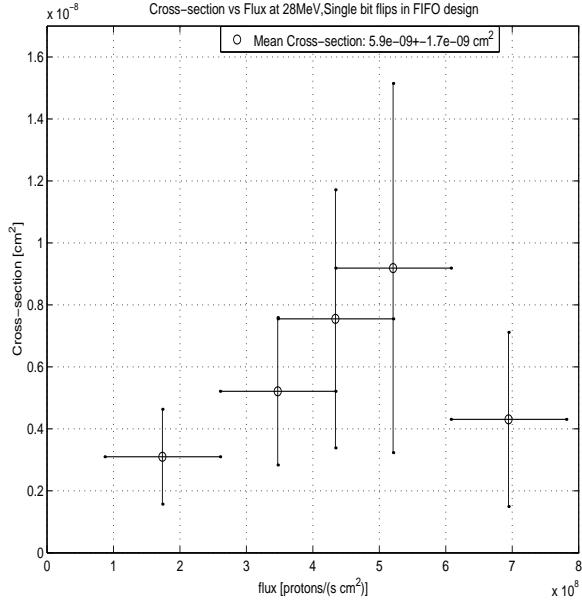


Figure 7.8: Cross-section for single bitflip upsets in internal RAM versus proton flux at 28MeV

a flux of  $3.6 \cdot 10^0 6 [p/cm^2 s]$ . Table 7.6 show the average results of the measurements. Only the shiftregister design (32 x 500) using the UART interface were tested.

**25 MeV, shiftregister:** during 7 runs of in total 50 minutes exposure only no single bit flips were detected compared to 54 configuration upsets.

*Mean cross-section configuration SEU:*  $6.9 \cdot 10^{-9} \pm 2.1 \cdot 10^{-9} \text{ cm}^2$

A mean cross-section result of  $3.4 \cdot 10^{-9} \pm 9.6 \cdot 10^{-10} \text{ cm}^2$  is approximately a factor 2 lower than for the 38 MeV and 180 MeV results at TSL, and is consistent with the discussion concerning the cross-section curve in chapter 3.

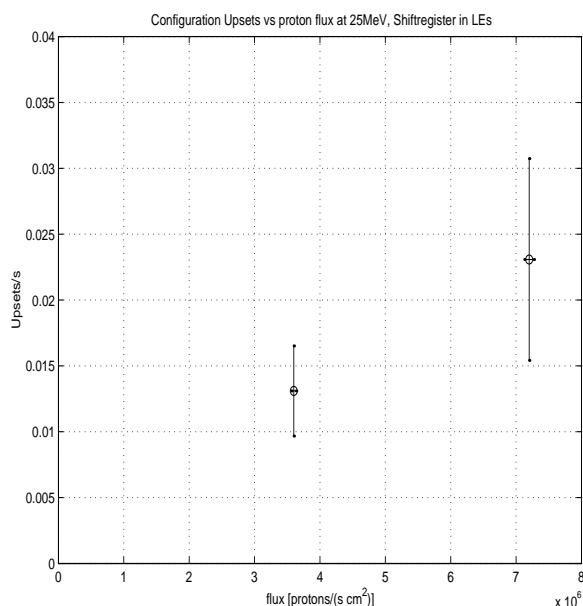


Figure 7.9: Configuration upset rate in the shiftregister design versus proton flux at 25MeV

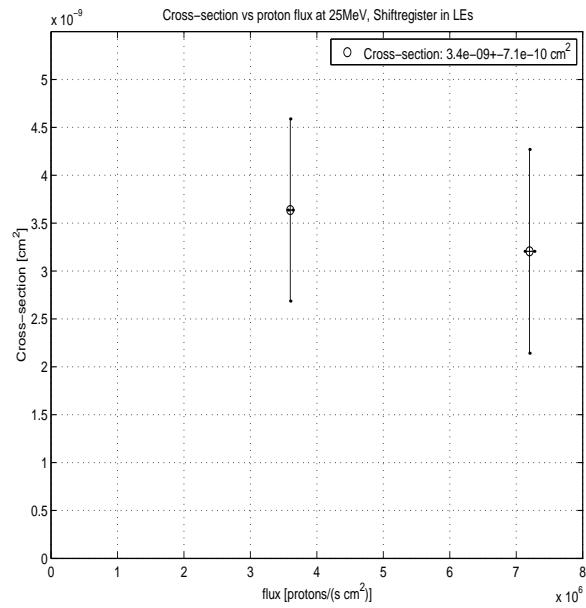


Figure 7.10: Cross-section for configuration upsets in the shiftregister design versus proton flux at 25MeV

## 7.5 Results at 7 MeV

An additional measurement was done where as 2 mm iron plate was put in between the beam exit point and the DUT, in order to decrease the energy to approximately 10 MeV. No SEUs were detected.

$$E_{2 \text{ mm iron}} = 28 \text{ MeV} - (13.1 \text{ MeV/g/cm}^3 \cdot 7.9 \text{ g/cm}^3) * 0.2 \text{ cm} = 7.3 \text{ MeV} \quad (7.1)$$

Table 7.7: Irradiation run using 2 mm iron plate with an energy of approximately 7 MeV.

Energy	Flux [p/cm <sup>2</sup> s]	CS [cm <sup>2</sup> ]
7 MeV	$1.7 \cdot 10^7$	-

## 7.6 Summary

The scaling method introduced is used as a first approximation to explain the difference from the 28 and 180 MeV irradiation tests results at TSL. Presenting the scaled results, it has to be pointed out that there are some considerable uncertainties related to the scaling measurements. The two main sources are the unstable amperemeter readings below 50 pA, and the beam profile estimation. Thus a systematic error of  $1.5 \cdot 10^{-9}$  cm<sup>2</sup> is added to the final cross-section result for the 28 MeV measurements.

Table 7.8: Cross-section for configuration upsets in the shiftregister design, where the 28 MeV cross-section is scaled.

Energy [MeV]	Configuration SEU [cm <sup>2</sup> ]
7	0
25	$3.4 \cdot 10^{-9} \pm 9.6 \cdot 10^{-10}$
28	$3.3 \cdot 10^{-9} \pm 1.9 \cdot 10^{-9}$
38	$6.9 \cdot 10^{-9} \pm 2.1 \cdot 10^{-9}$
180	$6.0 \cdot 10^{-9} \pm 1.1 \cdot 10^{-9}$

Table 7.9: Cross-section vs Energy for single bit flips in the FIFO design, where the 28 MeV cross-section is scaled

Energy [MeV]	Configuration SEU [cm <sup>2</sup> ]
28	$5.9 \cdot 10^{-9} \pm 1.7 \cdot 10^{-9}$
180	$7.7 \cdot 10^{-9} \pm 1.9 \cdot 10^{-9}$

Another interesting result of the irradiation tests is that most of the SEUs in the shiftregister design are related to configuration upsets, and only very few single bit flips were detected. A discovery also made by [19] for heavy ion beam testing of the APEX 20KE.

Several irradiation tests have been carried out on the ALTERA APEX20KE400 FPGA over some period of time. Table 7.8 and 7.9 summarises the cross-section for the configuration SEUs in the shiftregister design and the single bit flips in the FIFO design. New beam monitoring methods at OCL gave consistent results with the irradiation tests at TSL. A method for scaling the old measurements was also introduced.

Figure 7.11 shows the cross-section plotted as a function of the proton energy. A review of the discussion in chapter 3 section 3.2.2 about the sensitive area and critical energy, show that the measured cross-section has a threshold and saturation level.

The APEX 20K FPGA has approximately 3900000 configuration RAM bits [19]. The cross-section [cm<sup>2</sup>/bit] is then  $1.6 \cdot 10^{-15}$  cm<sup>2</sup>, see figure 7.12. It is however probably slightly higher

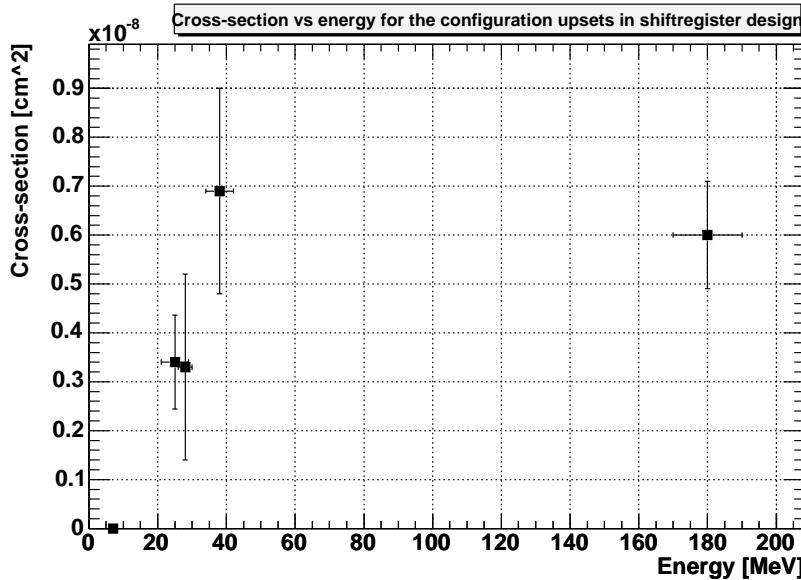
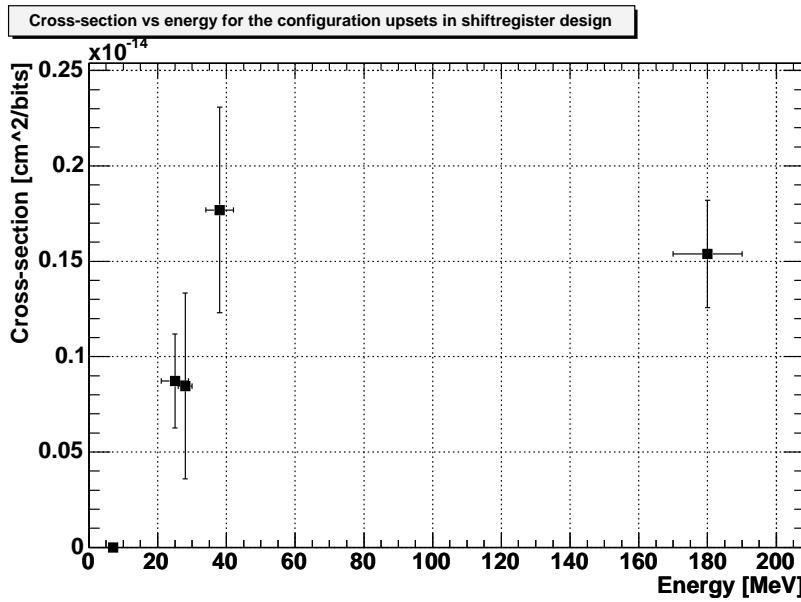
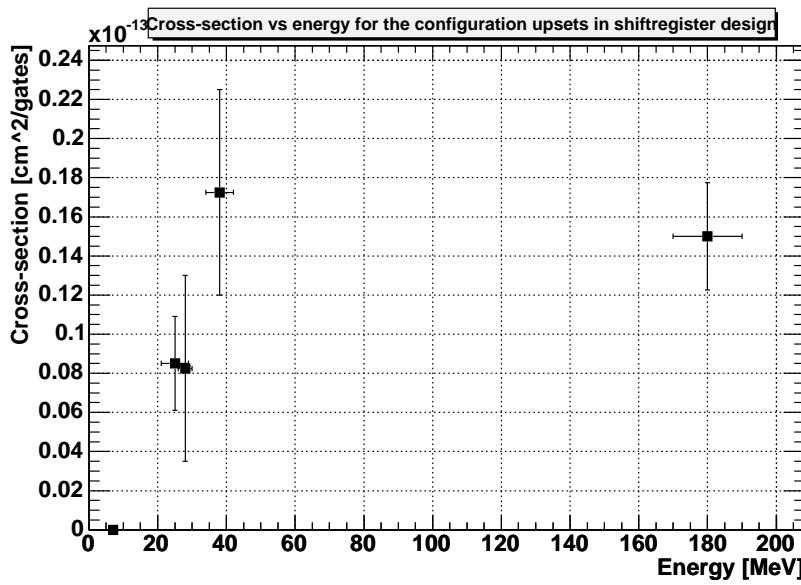


Figure 7.11: Cross-Section plotted versus energy for the ALTERA APEX20KE400 FPGA

since some of the configuration bits are redundant for the shiftregister design, that is, it does not use a 100% of the configuration bits. However, even assuming that only half of the available configuration bits can cause an SEU in the shiftregister design, it is still lower than for the plots in figure 3.11. This might imply that the sensitive area is smaller than what is used for the simulations. A similar plot is shown for the cross-section [cm<sup>2</sup>/gates], when the typical number of gates is 400000. At 25 MeV the cross-section is roughly half of the saturation value. Comparing with the cross-section plots in figure 3.11 this same behaviour is shown for the plot having critical energy of 600 keV. Thus an approximation to the critical energy can be that it lies in the area between 300 keV and 600 keV. Comparing the measured energy dependence of SEU to the simulated one, one could estimate the sensitive volume. Assuming a structure size of .18 μm, a SV of .18 x .18 x 2 μm<sup>3</sup> could explain the observed error rate. However, in chapter 3 the heavy-ion cross-section result for the APEX 20K is plotted in figure 3.13 where the threshold LET is 0.1 MeV/mg/cm<sup>2</sup>. Using equation 3.8 one would expect a SV much larger than the above. The reason for this discrepancy is at the moment not understood.

$$E_{crit} = 0.1 \frac{MeV}{mg/cm^2} \cdot \sqrt{0.18^2 + 0.18^2 + 2^2} \mu m \cdot 2.33 \frac{g}{cm^2} = 46.8 \text{ keV}$$

Figure 7.12: Cross-section [ $\text{cm}^2/\text{bit}$ ]Figure 7.13: Cross-section [ $\text{cm}^2/\text{gate}$ ]

# Chapter 8

## Summary and conclusion

### 8.1 Summary

In the ALICE experiment the front-end electronics of the Time Projection Chamber, the main tracking detector, is placed only a few meters from the interaction point of the particle collisions. The collisions will produce a shower of particles that will drift in the TPC and hit the end plates where the readout electronics is mounted. Since the front end electronics for the TPC is quite complex (large data rates, interface to DAQ, Trigger and DCS), the control unit designs are based on FPGAs.

Responsible for the data collections from these collisions, it is crucial that the readout electronics will survive the radiation environment present in the TPC detector. Experiencing upsets during an ALICE experiment run may have fatal consequences for the integrity of the data. An upset in the configuration RAM can lead to a corrupt design and therefore a loss or stop in the data collection due to a reprogramming of the device.

Based on SRAM configuration cells, the APEX 20KE400 used on the RCU card, has shown to be sensitive to deposited energy from heavy ionising particles. The different types of radiation induced effects in semiconductor devices and FPGAs in particular, have been treated in chapter 3. Treating the radiation levels in the TPC detector it was pointed out that the distribution peak for the kinetic energy of protons lies between 100-200 MeV, and that intermediate range neutrons ( $2 \text{ MeV} < E < 20 \text{ MeV}$ ) are considered to contribute with less than 10% of the SEUs. Thus the main particles of concern for the APEX 20K are the high energetic hadrons (mainly above 20 MeV) capable of inducing SEUs through nuclear interactions.

Irradiation tests using a 29 MeV proton beam at the Oslo Cyclotron Laboratory, and a 38 and 180 MeV proton beam at The Svedberg Laboratory in Uppsala were carried out to measure the proton induced SEU cross-section of the APEX 20K.

In order to detect single event upsets in an FPGA, special firmware and software were produced for this purpose. Unfortunately the APEX 20K FPGA did not offer the feature of direct read back of the configuration memory. This would give an accurate detection of SEUs in the configuration cells. Thus an alternative method had to be used. A shiftregister and FIFO design was therefore written in VHDL and synthesized for the APEX 20K FPGA. There are three main

SEU types that can occur in an FPGA. The shiftregister design was chosen since it was capable of detecting both upsets in the configuration SRAM cells and single bit flips in sequential logic such as registers. The application memory or internal RAM was covered by the FIFO design. Most of the iterations leading to improved firmware and software were based on the irradiation tests carried out at the Oslo Cyclotron. Thus the early results from these test where only used as a preliminary indication and for improving the test setup.

The possibility of short notice access, due to the informal nature of requesting beam time at the OCL, was the key factor for the frequent use of this facility. TSL proposols demanded more effort put into the request for beam time. Both a letter of intent and a presentation of the project were needed for the committee to decided whether or not to give access to the facility. TSL is also a larger facility with more users than the Cyclotron in Oslo, included several commercial users. These factors contributed to the late start of irradiation tests at TSL, and therefore the late discovery of incorrect beam monitoring methods at OCL.

After installing the new beam measuring equipment (TFBC), new irradiation runs were carried out at OCL. A custom made beam profile monitor revealed that the beam spot used for the early tests at LOCL was smaller than expected. Thus by moving the setup area further away from the beam exit point the beam spot was increased. Results from new irradiation tests showed to be consistent with the TSL measurements. Comparing the flux measurements done with the TFBC and the intensity measurements done with the Faraday cup, a scaling method was suggested for the old 28 MeV results.

## 8.2 Conclusion

The APEX 20K FPGA has been characterised for its radiation tolerance using the facilities at the Oslo Cyclotron Laboratory and The Svedberg Laboratory. It has proved to be sensitive single event upsets induced by heavy recoil ions produced through nuclear interaction with protons. Proton energies of 25,28,38 and 180 MeV have been used to irradiate the FPGA. Energies representative for the radiation levels that are expected to be present near the front-end electronics of the TPC in the ALICE experiment.

The measured configuration SEU cross-section for the APEX 20K is  $6.0 \cdot 10^{-9} \pm 1.1 \cdot 10^{-9} \text{ cm}^2$ . Figure 8.1(a) and 8.1(b) plots the expected flux in the TPC detector as function of the radius. The numbers are collected from tables 3.3 and 3.4 and assumed to be in the middle of each scoring region.

The TPC readout electronics is divided into 216 readout partitions, that is, 18 regions on each end cap and 6 sectors in each region. The inner and outer radius of the scoring regions are 80 and 280 cm. The SEU rate is estimated by dividing this area into six sections, placing an RCU in the middle of each section and using the flux value given for that position from figures 8.1(a) and 8.1(b). Table 8.1 lists the expected SEU rate for the APEX 20K devices for each section. Each section contains 18 RCUs, thus multiplying by 18 and over a 4 hour run table 8.2 presents the total expected SEU rate number for the whole TPC detector.

Table 8.1: Expected numbers of SEUs for the different scoring regions in the TPC detector

Sector	$\mu$ -absorber side					
	1	2	3	4	5	6
SEU/(FPGA s) [ $x 10^{-6}$ ]	$2.4 \pm 0.4$	$2.0 \pm 0.4$	$1.6 \pm 0.3$	$1.1 \pm 0.2$	$0.9 \pm 0.2$	$0.8 \pm 0.1$
non-absorber side						
SEU/(FPGA s) [ $x 10^{-6}$ ]	$1.6 \pm 0.3$	$1.3 \pm 0.2$	$0.9 \pm 0.2$	$0.7 \pm 0.1$	$0.6 \pm 0.1$	$0.5 \pm 0.1$

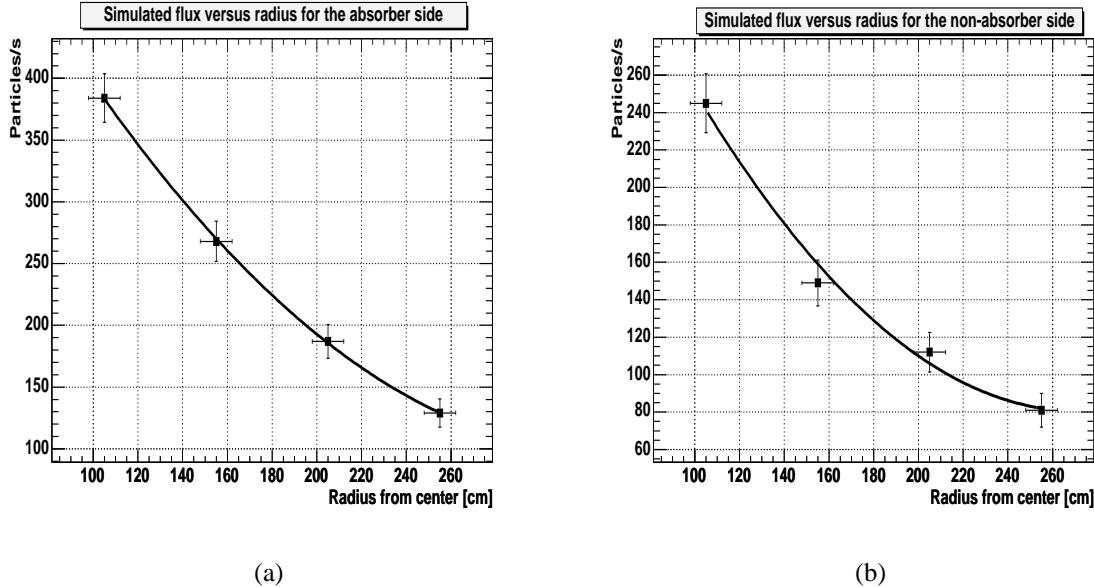


Figure 8.1: a) Expected SEU rate for the APEX 20K for the absorber side, b) Expected SEU rate for the APEX 20K for the non-absorber side

Table 8.2: Total expected numbers of SEUs for the whole TPC detector per 4 hour run, 216 devices

SEU/(216 FPGAs 4hr)	$3.7 \pm 0.2$
---------------------	---------------

## 8.3 Outlook

The result obtained from the irradiation tests so far shows that the expected SEU rate in the SRAM-based FPGAs are at the limit of what can be tolerated. This makes radiation tolerant designs necessary, which is possible, but complicates the firmware development. Alternatively, FLASH-based FPGAs (Actel) which are supposed to be radiation tolerant could replace the ALTERA devices, but that would mean a re-design of parts of the front-end electronics. Another alternative to the APEX FPGA is the Xilinx Virtex FPGA which offer the feature of direct reading back the configuration memory. It also supports partial reconfiguration, that is, if a an upset is detected in a part of the configuration memory, this part can be reconfigured seperately while other parts continue normal operation. A desirable feature for the FPGA on the Readout Control Unit.

A few irradiation tests with a 28 MeV proton beam have already been carried out for the Actel APA075 device. It is interesting to note that the errors experienced for the ACTEL device were potentially "hard" errors, that is, an error inflicted a permanent error on the device. Reconfiguration did not refresh the device. Such a behaviour may imply a sensitivity to cummulative effects. The preliminary critical fluence measured for the Actel APA075 is approximately  $6.5 \cdot 10^{12} \text{ protons/cm}^2$ . The expected particle fluences per 10 year of ALICE running are about  $10^{10}$  (above 10 MeV) or  $10^{11}$  (all energies). Therefore, the FLASH-based ACTEL device is an alternative solution.

For the ALTERA APEX 20K FPGA the proton irradiation results have to be argumented by neutron irradiation. Eventhough it is expected that protons and neutrons above a few tens of MeV will cause similar radiation effects, the measurements in table 3.12 shows some difference. Thus further investigation has to be carried out to see if the difference can be negligible for the APEX 20K FPGA.

Finally, the complete readout-chain (the readout controller unit connected to a front-end board, detector control and trigger board and the optical fibre to DAQ) will have to be irradiation tested under normal data taking conditions. The Svedberg Laboratory with a range of proton and neutron energies and various sizes of beam spots is perfectly suited for these experiments.

## **Appendix A**

### **Note for users at TSL**

Note for users, A. Prokofiev 040319  
 Alexander.Prokofiev@tsl.uu.se

## Beam line configuration and monitoring

**Date:** 040312

**Week:** 0411

**Beam line:** B

**User:** FA163 Dieter Roerich and Ketil Roed

**Particles delivered:** protons

**Particle energy:**

- Nominal: 38 MeV
- Measured, delivered by the cyclotron: 38.0 MeV
- Deduced, at the exit of the beam line: 37.0 MeV. Protons of this energy were incident on the user's irradiated object.
- Deduced, at the target of the TFBC-monitor: 34.2 MeV.

**Beam-shaping equipment at the end of the line:**

- Tantalum scattering foil, 0.08 mm thick
- Graphite collimator: approximately a cube, 16x16x16 cm, with an opening, 30 mm in diameter, at the beam axis. The front end of the collimator is positioned at the distance of 333 cm from the scattering foil.

**Beam monitors:**

1. Scintillation telescope, viewing the exit window of the beam line. Can be used at any beam intensity, without disturbing or interrupting the beam. Requires calibration.
2. Thin film breakdown counter #r-12 with a  $^{238}\text{U}$  sample #103. Operational voltage: 75V. Can be used only at low beam intensity. Allows measurement of the absolute proton flux. The  $^{238}\text{U}(\text{p},\text{f})$  cross section is taken from the review [1]. The detection efficiency is obtained in a calibration with a  $^{252}\text{Cf}$  sample #245. A correction is applied that takes into account the difference in target thickness and fission fragment properties for calibration and working samples [2].
3. Faraday cup. A crude monitor. Can be used only at high beam intensity. Interrupts the beam. During the run, monitor #1 is permanently used. It was calibrated before the run using monitor #2.

**Position for user's irradiation, absolute monitoring, and profile measurements:** at about 359 cm from the scattering foil.

**Relation between the beam flux and the monitor count rate**

The beam flux ( $\text{cm}^{-2}\text{s}^{-1}$ ) is proportional to the count rate of the monitor #1,  $r$ :

$$j = 3.5\text{E}4 r$$

The proportionality is confirmed within 10% in the flux range  $4\text{E}6 \dots 7\text{E}7 \text{ cm}^{-2}\text{s}^{-1}$  (see Fig. 1).

**Beam profile:**

measured with monitors #2 (movable) and #1 (for normalization). See Fig. 2a and b for horizontal and vertical profiles, respectively.

## References

1. A.V. Prokofiev, Compilation and Systematics of Proton-Induced Fission Cross Section Data, Nuclear Instruments and Methods in Physics Research v. A463, pp. 557-575 (2001).
2. A.N. Smirnov, private communication.

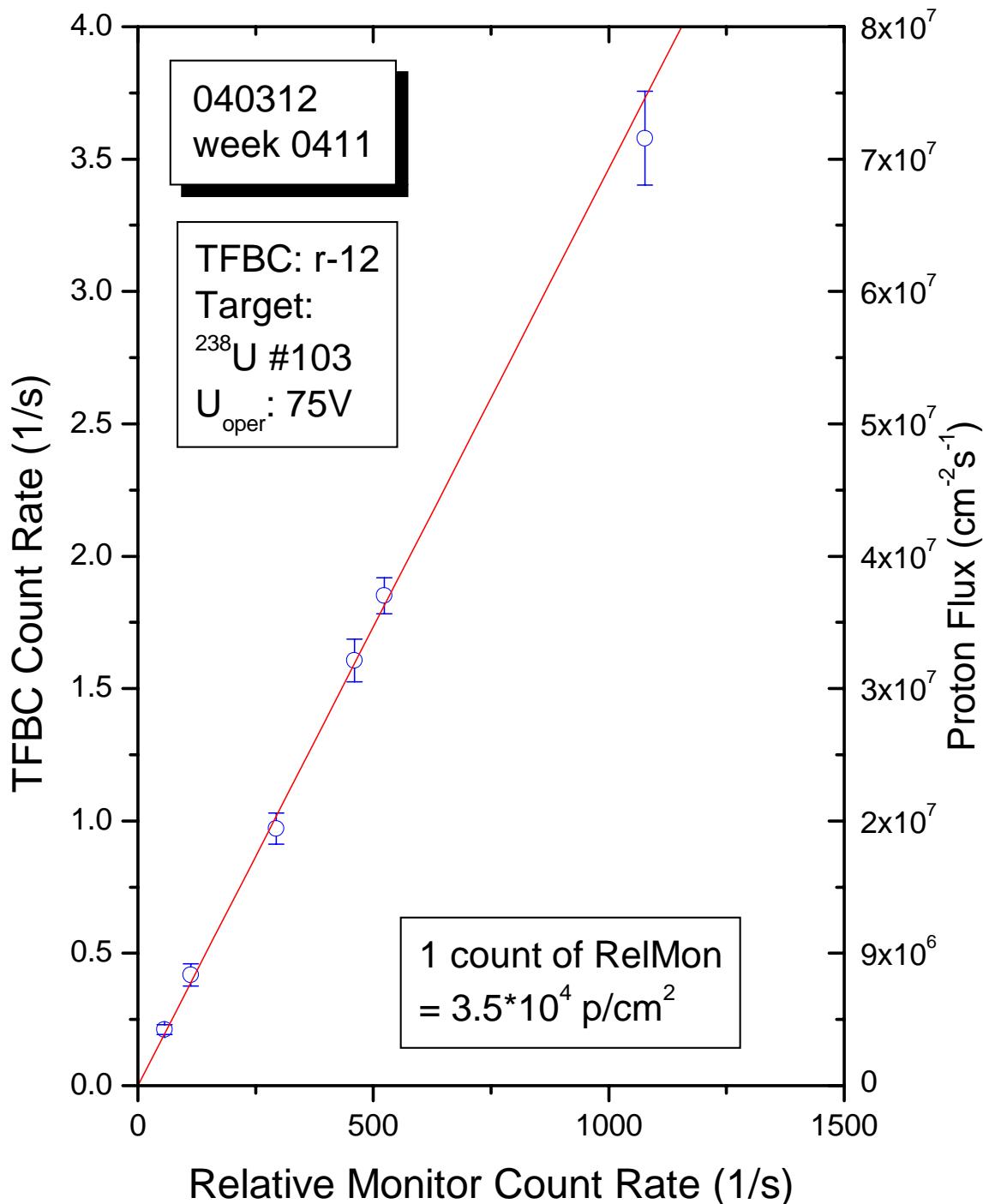


Fig. 1.  
The TFBC count rate and the beam flux versus the count rate of the relative monitor.

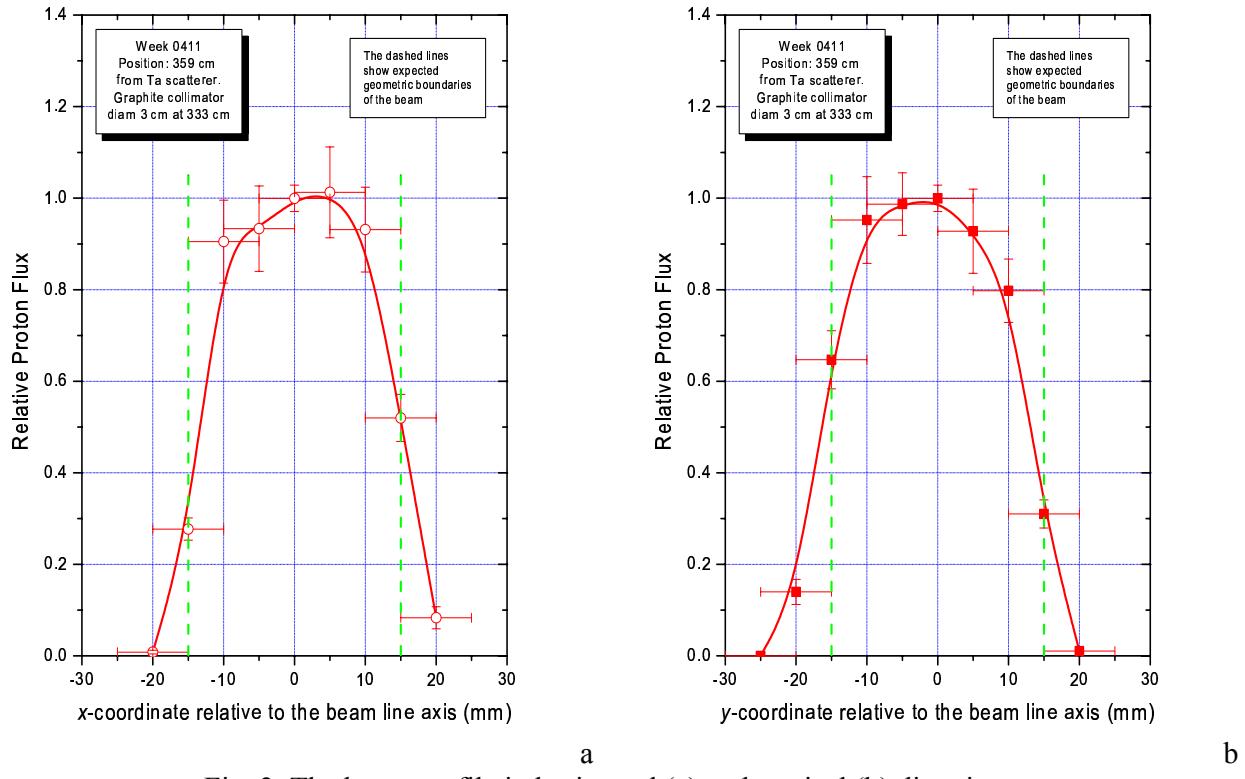


Fig. 2. The beam profile in horizontal (a) and vertical (b) direction.

## Note for users

A. Prokofiev 040123

## Beam line configuration and monitoring

Date: 040123

Week: 0404

Beam line: B

User: FA163 Ketil Roed

Particles delivered: protons

Particle energy:

\* Nominal: 180 MeV

\* Measured, delivered by the cyclotron: 177 MeV

\* Deduced, at the exit of the beam line: 171 MeV

## Beam-shaping equipment at the end of the line:

\* Tantalum scattering foil, 1.5 mm thick

\* Graphite collimator: approximately a cube, 16x16x16 cm, with an opening, 30 mm in diameter, at the beam axis. The front end of the collimator is positioned at the distance of 415 cm from the scattering foil.

## Beam monitors:

1. Scintillation telescope, viewing the exit window of the beam line. Can be used at any beam intensity, without disturbing or interrupting the beam. Requires calibration.
2. Thin film breakdown counter. Can be used only at low beam intensity. Allows measurement of the absolute proton flux.
3. Faraday cup. Can be used only at high beam intensity. Interrupts the beam.

During the run, monitor #1 is permanently used. It was calibrated before the run using monitors #2 and 3.

Irradiation position: at about 445 cm from the scattering foil.

Beam profile: measured with monitors #2 (movable) and #1 (for normalization). See figure.

Relation between the beam current and the monitor count rate

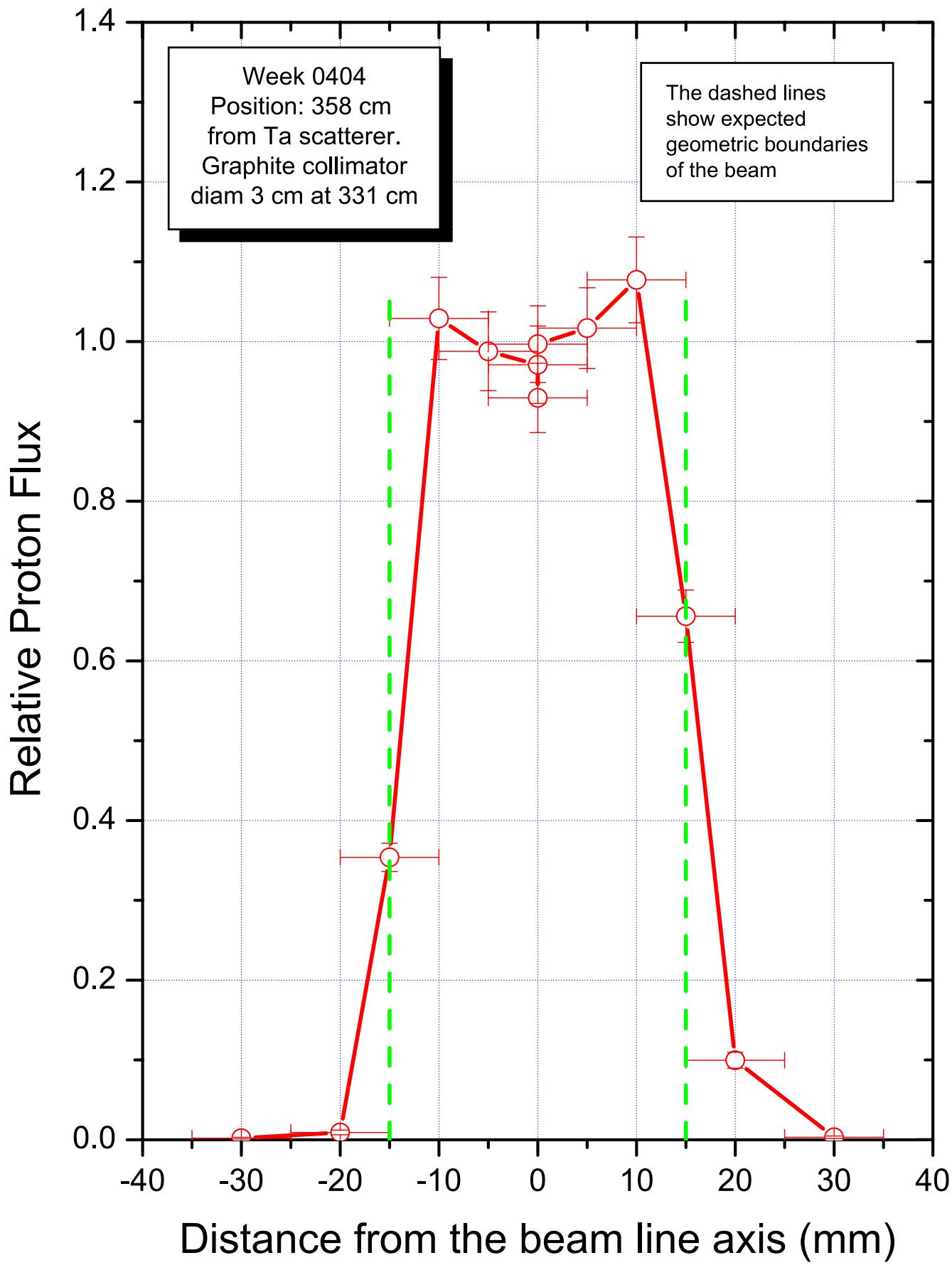
For low count rates (<1000 s<sup>-1</sup>, corresponding to <25 pA on chip), the beam current on chip, I<sub>chip</sub> (pA) is proportional to the count rate of the monitor #1, r:

$$I_{\text{chip}} = 0.025 r.$$

The proportionality is valid within 5%.

For higher count rates (= higher beam currents), the monitor count rate increases higher than the beam current, possibly due to the increasing background caused by scattering of protons by the massive graphite collimator. The following relation is valid for any beam current up to 150 pA on chip:

$$I_{\text{chip}} = 120(\sqrt{1+r/2400}) - 1$$



# Appendix B

## TFBC sensitivity tables

Tables B.1 through B.3 lists the sensitivity of the Thin Film Breakdown counters available for the OCL runs. The *Sens63/75* is the number of protons need for generating a signal in the TFBC. *dsens63/75* is the uncertainty in prosent. 63 and 75 is the voltage supply level for the TFBC. For the OCL 25 MeV test, we used target r26 U(101) for 75V:  $1.35 \cdot 10^{-8}$ . The tables are made by A.N.Smirnov, V.G. Khlopin Radium Institute, 2<sup>nd</sup> Murinskiy Prospect 28, St.Petersburg 194021, Russia.

Table B.1: Sensitivity for table for target r25 U(101)

Energy	Sens63	dsens63	Sens75	dsens75
20	5,50E-9	13,3	1,07E-8	12,9
21	5,91E-9	13,3	1,15E-8	12,9
22	6,29E-9	13,3	1,22E-8	12,9
23	6,63E-9	13,3	1,28E-8	12,9
24	6,96E-9	13,3	1,34E-8	12,9
25	7,27E-9	13,3	1,40E-8	12,9
26	7,55E-9	13,3	1,45E-8	12,9
27	7,82E-9	13,3	1,49E-8	12,9
28	8,05E-9	13,3	1,53E-8	12,9
29	8,27E-9	13,3	1,57E-8	12,9
30	8,45E-9	13,3	1,60E-8	12,9
31	8,60E-9	13,3	1,62E-8	12,9
32	8,72E-9	13,3	1,65E-8	12,9
33	8,79E-9	13,3	1,66E-8	12,9
34	8,82E-9	13,3	1,67E-8	12,9
35	8,81E-9	13,3	1,68E-8	12,9

Table B.2: Sensitivity table for target r26 U(101)

Energy	Sens63	dsens63	Sens75	dsens75
20	5,41E-9	13,2	1,03E-8	13,1
21	5,81E-9	13,2	1,11E-8	13,1
22	6,18E-9	13,2	1,18E-8	13,1
23	6,52E-9	13,2	1,24E-8	13,1
24	6,84E-9	13,2	1,30E-8	13,1
25	7,14E-9	13,2	1,35E-8	13,1
26	7,42E-9	13,2	1,40E-8	13,1
27	7,68E-9	13,2	1,44E-8	13,1
28	7,92E-9	13,2	1,48E-8	13,1
29	8,12E-9	13,2	1,52E-8	13,1
30	8,30E-9	13,2	1,55E-8	13,1
31	8,45E-9	13,2	1,57E-8	13,1
32	8,57E-9	13,2	1,59E-8	13,1
33	8,64E-9	13,2	1,61E-8	13,1
34	8,67E-9	13,2	1,62E-8	13,1
35	8,66E-9	13,2	1,62E-8	13,1

Table B.3: Sensitivity table for target r27 U(101)

Energy	Sens63	dsens63	Sens75	dsens75
20	5,96E-9	13,3	1,10E-8	13,0
21	6,40E-9	13,3	1,18E-8	13,0
22	6,81E-9	13,3	1,25E-8	13,0
23	7,18E-9	13,3	1,32E-8	13,0
24	7,54E-9	13,3	1,38E-8	13,0
25	7,87E-9	13,3	1,44E-8	13,0
26	8,18E-9	13,3	1,49E-8	13,0
27	8,46E-9	13,3	1,53E-8	13,0
28	8,72E-9	13,3	1,57E-8	13,0
29	8,95E-9	13,3	1,61E-8	13,0
30	9,15E-9	13,3	1,64E-8	13,0
31	9,31E-9	13,3	1,67E-8	13,0
32	9,44E-9	13,3	1,69E-8	13,0
33	9,52E-9	13,3	1,71E-8	13,0
34	9,56E-9	13,3	1,72E-8	13,0
35	9,54E-9	13,3	1,73E-8	13,0

# Appendix C

## VHDL code

Table C.1 lists the different VHDL files used for the irradiation tests of the APEX 20K FPGA.

Table C.1: Description of VHDL files

File	Description
apex_shift.vhd	Top level design. Initiates all components used from the other VHDL files. Generates the final size of the shiftregister by using $W$ (width of shiftregister) rows of <i>register_row.vhd</i> . Controls the connection between the UART interface and the shiftregister using a control state machine and a multiplexer. Uses <i>altclock.vhd</i> to create a 33MHz clock from the external 66MHz onboard crystal.
rx_uart.vhd	UART Receiver interface. Simple state machine
tx_uart.vhd	UART transceiver interface. Simple state machine
register_row.vhd	Generates a row of $L$ (length of shiftregister) simple D-flip-flops from <i>shift_register.vhd</i> .
shift_register.vhd	Contains the VHDL code describing the basic D-flip-flop used in the shiftregister design.
clk_div.vhd	A VHDL component that scales the external 66MHz clock down to different values
altclock.vhd	Scales the external 66MHz clock down to 33MHz.
apex_fifo.vhd	Same as for <i>apex_shift.vhd</i> except it implements a FIFO ( <i>lpm_fifo_clear.vhd</i> ) instead of the shiftregister.
lpm_fifo_clear.vhd	Mega Wizard Plug-in Manager generated FIFO.
chiptest_top_shift.vhd	Top level design when using the SCSN protocol. Shiftregister design.
chiptest_top_fifo.vhd	Top level design when using the SCSN protocol. FIFO design
mcm_network_interface.edf	SCSN client. The master client was already implemented on the RCU card connected to the PCI-bus.

# Appendix D

## Software

Table D.1 lists the different software files used for the irradiation tests of the APEX 20K FPGA.

Table D.1: Description of software files

File	Description
seu_com.c	Readout software. Writes data to the FPGA, reads the data back and compares to check for SEUs. Uses UART communication
shiftreg.c	Readout software. Writes data to the FPGA, reads the data back and compares to check for SEUs. Uses the SCSN interface.
scsn.h [30]	headerfile for the SCSN functions
scsn.c [30]	Contains the functions for reading and writing over the PCI-bus
analyse.m	Software for analysis of the logfiles produced by seu_com.c and shiftreg.c.

# Appendix E

## Result tables

### E.1 Result 180MeV, January

Table E.1: 180MeV, TSL January 2004, Shiftregister design, different sizes of the shiftregister design are used. Uart interface

Run	Flux [protons/cm <sup>2</sup> s]	Usage [%]	LE	Time [s]	SEU register	SEU config	CS register [cm <sup>2</sup> ]	CS config [cm <sup>2</sup> ]
1	$1.5 \times 10^7$	change		883	0	23	$< 7.6 \times 10^{-11}$	$1.8 \times 10^{-9}$
2	$7.4 \times 10^6$	98		484	0	20	$< 2.9 \times 10^{-10}$	$5.6 \times 10^{-9}$
3	$3.9 \times 10^6$	98		978	1	18	$< 2.7 \times 10^{-10}$	$4.8 \times 10^{-9}$
4	$3.8 \times 10^6$	98		1270	3	21	$6.2 \times 10^{-10}$	$4.4 \times 10^{-9}$
5	$3.8 \times 10^6$	98		975	0	19	$< 2.7 \times 10^{-10}$	$5.2 \times 10^{-9}$
14	$3.6 \times 10^6$	58		618	0	8	$< 7.8 \times 10^{-10}$	$6.3 \times 10^{-9}$
15	$3.6 \times 10^6$	58		474	0	5	$< 1.0 \times 10^{-9}$	$5.0 \times 10^{-9}$
16	$3.6 \times 10^6$	43		523	0	6	$< 1.3 \times 10^{-9}$	$7.5 \times 10^{-9}$
17	$3.6 \times 10^6$	43		210	0	2	$< 3.2 \times 10^{-9}$	$6.3 \times 10^{-9}$
18	$3.6 \times 10^6$	43		1219	1	14	$< 5.4 \times 10^{-10}$	$7.5 \times 10^{-9}$
6	$1.9 \times 10^6$	98		987	2	10	$1.1 \times 10^{-9}$	$5.3 \times 10^{-9}$
7	$1.9 \times 10^6$	98		767	0	18	$< 6.7 \times 10^{-10}$	$1.2 \times 10^{-8}$
8	$1.9 \times 10^6$	98		870	1	9	$< 6.0 \times 10^{-10}$	$5.4 \times 10^{-9}$
9	$1.9 \times 10^6$	98		784	0	12	$< 6.8 \times 10^{-10}$	$8.2 \times 10^{-9}$
10	$1.9 \times 10^6$	98		553	0	6	$< 9.5 \times 10^{-10}$	$5.7 \times 10^{-9}$
11	$1.9 \times 10^6$	98		880	0	7	$< 6.1 \times 10^{-10}$	$4.2 \times 10^{-9}$
12	$1.9 \times 10^6$	98		780	1	12	$< 6.7 \times 10^{-10}$	$8.0 \times 10^{-9}$
13	$1.9 \times 10^6$	58		766	0	3	$< 1.2 \times 10^{-9}$	$3.6 \times 10^{-9}$

Table E.2: Cross-section summerized from table E.1, 180 MeV, TSL January 2004 Shiftregister design (different sizes)

Energy	Flux [protons/cm <sup>2</sup> s]	Upset/s	cross-section [cm <sup>2</sup> ]
180 MeV	$2.0 \cdot 10^6$	$1.3 \cdot 10^{-2}$	$6.2 \cdot 10^{-9} \pm 2.6 \cdot 10^{-9}$
180 MeV	$3.8 \cdot 10^6$	$2.1 \cdot 10^{-2}$	$5.6 \cdot 10^{-9} \pm 1.2 \cdot 10^{-9}$
180 MeV	$7.8 \cdot 10^6$	$4.1 \cdot 10^{-2}$	$5.3 \cdot 10^{-9} \pm 1.2 \cdot 10^{-9}$
180 MeV	$1.6 \cdot 10^7$	$6.7 \cdot 10^{-2}$	$4.4 \cdot 10^{-9} \pm 5.6 \cdot 10^{-10}$
38 MeV	$2.0 \cdot 10^6$	$1.4 \cdot 10^{-2}$	$6.9 \cdot 10^{-9} \pm 2.1 \cdot 10^{-9}$
Mean CS 180 MeV			$5.4 \cdot 10^{-9} \pm 1.0 \cdot 10^{-9}$

Table E.3: 180 MeV, TSL January 2004, FIFO design (16 x 8192), UART interface. Uses approximately 61% of available application memory bits

Run	Flux [protons/cm <sup>2</sup> s]	Int RAM usage [%]	Time [s]	Config upsets	Bitflips RAM	CS config [cm <sup>2</sup> ]	CS int RAM [cm <sup>2</sup> ]
23	$7.1 \cdot 10^6$	61	337	1	7	$< 1.2 \cdot 10^{-9}$	$5.9 \cdot 10^{-9}$
22	$7.0 \cdot 10^6$	61	741	3	24	$1.6 \cdot 10^{-9}$	$7.5 \cdot 10^{-8}$
27	$3.6 \cdot 10^6$	61	299	0	8	$< 2.6 \cdot 10^{-9}$	$1.2 \cdot 10^{-8}$
26	$3.6 \cdot 10^6$	61	318	0	8	$< 2.6 \cdot 10^{-9}$	$1.2 \cdot 10^{-8}$
25	$3.5 \cdot 10^6$	61	200	0	4	$< 4.1 \cdot 10^{-9}$	$9.3 \cdot 10^{-9}$
24	$3.5 \cdot 10^6$	61	1179	1	20	$< 6.8 \cdot 10^{-10}$	$7.8 \cdot 10^{-9}$
21	$3.7 \cdot 10^6$	61	369	1	1	$< 2.2 \cdot 10^{-9}$	$< 1.2 \cdot 10^{-9}$
1	$1.9 \cdot 10^6$	61	509	0	5	$< 2.9 \cdot 10^{-9}$	$8.6 \cdot 10^{-9}$

Table E.4: Cross-section summerized from table E.3, 180 MeV, TSL January 2004 FIFO design (16 x 8192)

Energy	Flux [protons/cm <sup>2</sup> s]	Upset/s	cross-section [cm <sup>2</sup> ]
180 MeV	$1.9 \cdot 10^6$	$1.6 \cdot 10^{-2}$	$8.6 \cdot 10^{-9} \pm 3.0 \cdot 10^{-9}$
180 MeV	$3.6 \cdot 10^6$	$3.0 \cdot 10^{-2}$	$8.4 \cdot 10^{-9} \pm 4.4 \cdot 10^{-9}$
180 MeV	$7.1 \cdot 10^6$	$4.4 \cdot 10^{-2}$	$6.2 \cdot 10^{-9} \pm 1.8 \cdot 10^{-9}$
Mean CS 180 MeV			$7.7 \cdot 10^{-9} \pm 1.9 \cdot 10^{-9}$

## E.2 Result 38MeV, March

Table E.5: 38 MeV, TSL March 2004, Shiftregister design (32 x 500), uses approximately 98% of available programmable registers

CS first: Cross-section calculated at the time of the first detected SEU

CS last: Cross-section calculated at the time of the last detected SEU

CS overall: Cross-section calculated at the end of the run

Run	Flux [ $p/cm^2 s$ ]	Fluence [ $p/cm^2$ ]	Time [s]	Config SEU	Single SEU	CS first	CS last [ $cm^2$ ]	CS overall [ $cm^2$ ]
1	2.0e+06	8.1e+08	389	6	0	1.3e-08	1.0e-08	7.4e-09
4	1.9e+06	7.7e+08	403	8	0	1.0e-08	1.2e-08	1.0e-08
5	2.2e+06	9.7e+08	488	7	0	8.2e-09	8.3e-09	7.2e-09
6	2.1e+06	1.1e+09	520	4	0	1.1e-08	9.6e-09	3.7e-09
7	2.1e+06	9.3e+08	447	6	0	1.3e-08	7.3e-09	6.4e-09
8	2.0e+06	1.1e+09	514	6	0	4.8e-09	6.4e-09	5.7e-09
9	1.9e+06	1.0e+09	550	7	1	4.3e-09	6.8e-09	6.7e-09
10	1.6e+06	8.7e+08	561	4	0	1.1e-08	4.8e-09	4.6e-09
11	2.0e+06	8.3e+08	407	5	0	2.0e-08	7.7e-09	6.0e-09
12	2.1e+06	9.4e+08	459	7	1	5.5e-09	8.0e-09	7.4e-09
14	2.1e+06	9.3e+08	447	10	0	4.1e-09	1.1e-08	1.1e-08

Table E.6: Cross-section summarized from table E.5, 38 MeV, TSL March 2004 Shiftregister design(32 x 500)

Energy	Flux [protons/ $cm^2 s$ ]	Upset/s	cross-section [ $cm^2$ ]
38 MeV	$2.0 \cdot 10^6$	$1.4 \cdot 10^{-2}$	$6.9 \cdot 10^{-9} \pm 2.1 \cdot 10^{-9}$
Mean CS 180 MeV			$7.7 \cdot 10^{-9} \pm 1.9 \cdot 10^{-9}$

### E.3 Results 28MeV september

Table E.7: 28 MeV, September 2003, shiftregister design (32 x 400). Uses approximately 77% of available programmable registers

Run	Intensity [pA]	Flux [protons/cm <sup>2</sup> s]	Usage LE [%]	Time [s]	SEU reg- ister	SEU con- fig	CS config [cm <sup>2</sup> ]
1	10	$6.3 \cdot 10^7$	77	3312	0	6	$3.7 \cdot 10^{-11}$
2	10	$6.3 \cdot 10^7$	77	3220	0	12	$7.7 \cdot 10^{-11}$
3	20	$1.3 \cdot 10^8$	77	871	0	11	$1.3 \cdot 10^{-10}$
4	20	$1.3 \cdot 10^8$	77	1273	0	17	$1.4 \cdot 10^{-10}$
5	20	$1.3 \cdot 10^8$	77	276	0	4	$1.5 \cdot 10^{-10}$
6	20	$1.3 \cdot 10^8$	77	523	0	13	$2.6 \cdot 10^{-10}$
7	25	$1.6 \cdot 10^8$	77	57	0	3	$4.4 \cdot 10^{-10}$
8	25	$1.6 \cdot 10^8$	77	106	0	4	$3.1 \cdot 10^{-10}$
9	25	$1.6 \cdot 10^8$	77	166	0	7	$3.5 \cdot 10^{-10}$
10	25	$1.6 \cdot 10^8$	77	139	0	7	$4.2 \cdot 10^{-10}$
11	25	$1.6 \cdot 10^8$	77	412	0	16	$3.2 \cdot 10^{-10}$
12	30	$1.9 \cdot 10^8$	77	214	0	15	$4.9 \cdot 10^{-10}$
13	30	$1.9 \cdot 10^8$	77	406	0	11	$1.9 \cdot 10^{-10}$
14	30	$1.9 \cdot 10^8$	77	338	0	12	$2.6 \cdot 10^{-10}$
15	30	$1.9 \cdot 10^8$	77	312	0	12	$2.7 \cdot 10^{-10}$
16	40	$2.5 \cdot 10^8$	77	74	0	4	$2.8 \cdot 10^{-10}$
17	40	$2.5 \cdot 10^8$	77	88	0	6	$3.5 \cdot 10^{-10}$
18	40	$2.5 \cdot 10^8$	77	108	0	6	$2.9 \cdot 10^{-10}$
19	40	$2.5 \cdot 10^8$	77	112	0	8	$3.7 \cdot 10^{-10}$
20	40	$2.5 \cdot 10^8$	77	106	0	8	$3.9 \cdot 10^{-10}$
21	40	$2.5 \cdot 10^8$	77	292	0	19	$3.4 \cdot 10^{-10}$

Table E.8: Cross-section summarized from table E.7, 28 MeV September 2003 shifregister design(32 x 400)

Current [pA]	Flux [p/cm <sup>2</sup> s]	CS [cm <sup>2</sup> ]
10	$6.3 \cdot 10^7$	$5.8 \cdot 10^{-11} \pm 2.4 \cdot 10^{-11}$
20	$1.3 \cdot 10^8$	$1.7 \cdot 10^{-10} \pm 5.1 \cdot 10^{-11}$
25	$1.6 \cdot 10^8$	$3.7 \cdot 10^{-10} \pm 4.8 \cdot 10^{-11}$
30	$1.9 \cdot 10^8$	$3.0 \cdot 10^{-10} \pm 1.1 \cdot 10^{-10}$
40	$2.5 \cdot 10^8$	$3.4 \cdot 10^{-10} \pm 3.8 \cdot 10^{-11}$
Mean CS		$2.5 \cdot 10^{-10} \pm 3.3 \cdot 10^{-11}$

Table E.9: 28 MeV, September 2003, FIFO design (32 x 4096). Uses approximately 61% of available application memory bits

Run	Intensity [pA]	Flux [protons/cm <sup>2</sup> s]	Int RAM usage [%]	Time [s]	Config upsets	Bitflips RAM	CS config [cm <sup>2</sup> ]	CS int RAM [cm <sup>2</sup> ]
1	10	$6.3 \cdot 10^7$	61	3308	4	32	$3.2 \cdot 10^{-11}$	$2.6 \cdot 10^{-10}$
2	10	$6.3 \cdot 10^7$	61	3215	4	15	$3.3 \cdot 10^{-11}$	$1.2 \cdot 10^{-11}$
3	20	$1.3 \cdot 10^8$	61	866	2	27	$3.1 \cdot 10^{-11}$	$4.1 \cdot 10^{-10}$
4	20	$1.3 \cdot 10^8$	61	1269	3	51	$3.2 \cdot 10^{-11}$	$5.4 \cdot 10^{-10}$
5	20	$1.3 \cdot 10^8$	61	272	1	3	$< 4.9 \cdot 10^{-11}$	$1.5 \cdot 10^{-10}$
6	20	$1.3 \cdot 10^8$	61	520	0	13	$< 2.4 \cdot 10^{-11}$	$3.3 \cdot 10^{-10}$
7	25	$1.6 \cdot 10^8$	61	102	1	7	$< 1.1 \cdot 10^{-10}$	$7.3 \cdot 10^{-10}$
8	25	$1.6 \cdot 10^8$	61	162	3	12	$2.0 \cdot 10^{-10}$	$7.9 \cdot 10^{-10}$
9	25	$1.6 \cdot 10^8$	61	84	2	1	$2.5 \cdot 10^{-10}$	$< 1.3 \cdot 10^{-10}$
10	25	$1.6 \cdot 10^8$	61	135	3	4	$2.4 \cdot 10^{-10}$	$3.2 \cdot 10^{-10}$
11	25	$1.6 \cdot 10^8$	61	409	3	27	$7.8 \cdot 10^{-11}$	$7.0 \cdot 10^{-10}$
12	30	$1.9 \cdot 10^8$	61	210	5	7	$2.1 \cdot 10^{-10}$	$3.0 \cdot 10^{-10}$
13	30	$1.9 \cdot 10^8$	61	402	4	14	$8.8 \cdot 10^{-11}$	$3.1 \cdot 10^{-10}$
14	30	$1.9 \cdot 10^8$	61	309	1	37	$2.9 \cdot 10^{-11}$	$1.1 \cdot 10^{-9}$
15	30	$1.9 \cdot 10^8$	61	334	0	41	$< 2.6 \cdot 10^{-11}$	$1.1 \cdot 10^{-9}$
16	40	$2.5 \cdot 10^8$	61	102	10	3	$6.5 \cdot 10^{-10}$	$2.0 \cdot 10^{-10}$
17	40	$2.5 \cdot 10^8$	61	104	17	2	$1.1 \cdot 10^{-9}$	$1.3 \cdot 10^{-10}$
18	40	$2.5 \cdot 10^8$	61	108	2	10	$1.2 \cdot 10^{-10}$	$6.2 \cdot 10^{-10}$
19	40	$2.5 \cdot 10^8$	61	288	3	21	$6.9 \cdot 10^{-11}$	$4.5 \cdot 10^{-10}$

Table E.10: Cross-section summarized from table E.9, 28 MeV September 2003 FIFO design(32 x 4096), Single bit flips

Current [pA]	Flux [p/cm <sup>2</sup> s]	CS [cm <sup>2</sup> ]
10	$6.3 \cdot 10^7$	$1.9 \cdot 10^{-10} \pm 9.4 \cdot 10^{-11}$
20	$1.3 \cdot 10^8$	$3.6 \cdot 10^{-10} \pm 1.6 \cdot 10^{-10}$
25	$1.6 \cdot 10^8$	$5.4 \cdot 10^{-10} \pm 2.9 \cdot 10^{-10}$
30	$1.9 \cdot 10^8$	$6.9 \cdot 10^{-10} \pm 4.5 \cdot 10^{-10}$
40	$2.5 \cdot 10^8$	$3.5 \cdot 10^{-10} \pm 2.3 \cdot 10^{-11}$
Mean CS		$4.3 \cdot 10^{-10} \pm 1.0 \cdot 10^{-10}$

## E.4 Results 25MeV March

Table E.11: 25MeV, March 2004, Shiftregister design (32 x 500), UART interface. Uses approximately 98% of available application memory bits

CS first: Cross-section calculated at the time of the first detected SEU

CS last: Cross-section calculated at the time of the last detected SEU

CS overall: Cross-section calculated at the end of the run

Run	Flux [p/cm <sup>2</sup> s]	Fluence [p/cm <sup>2</sup> ]	Time [s]	Config SEU	Single SEU	CS first	CS last [cm <sup>2</sup> ]	CS overall [cm <sup>2</sup> ]
1	7.2e+06	3.6e+09	498	6	0	4.0e-09	1.9e-09	1.7e-09
2	7.2e+06	2.7e+09	377	9	0	4.7e-09	3.7e-09	3.3e-09
3	7.2e+06	2.7e+09	381	11	0	5.7e-09	4.4e-09	4.0e-09
4	7.2e+06	2.1e+09	291	8	0	3.8e-09	5.3e-09	3.8e-09
5	3.6e+06	1.9e+09	536	9	0	1.1e-09	4.8e-09	4.7e-09
6	3.6e+06	1.7e+09	481	6	0	6.2e-09	3.6e-09	3.5e-09
7	3.6e+06	1.8e+09	499	5	0	2.5e-09	2.9e-09	2.8e-09
Mean	5.7e+06	2.4e+09	438	7.7	0	4.0e-09	3.8e-09	3.4e-09

Table E.12: Cross-section summarized from table E.11, 25 MeV March 2004 Shiftregister design(32 x 500)

Energy	Flux [protons/cm <sup>2</sup> s]	Upsets/s	CS config [cm <sup>2</sup> ]
25MeV	$3.6 \cdot 10^6$	$1.3 \cdot 10^{-2}$	$3.2 \cdot 10^{-9} \pm 1.1 \cdot 10^{-9}$
25MeV	$7.2 \cdot 10^6$	$2.3 \cdot 10^{-2}$	$3.8 \cdot 10^{-9} \pm 9.5 \cdot 10^{-10}$
Mean CS			$3.4 \cdot 10^{-9} \pm 9.6 \cdot 10^{-10}$

## **Appendix F**

### **Paper for LECC 2003**

The preliminary irradiation tests were presented at the 9th Workshop on Electronics for LHC Experiments held September 29 to October 3 in Amsterdam, The Netherlands.

# Irradiation tests of the ALTERA SRAM based FPGA and fault tolerant design concepts

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## Abstract

In the ALICE Time Projection Chamber [1] TPC at CERN the front end electronics will be located about 3 meters from the interaction point and will therefore be exposed to radiation generated by the particle collisions. Consequently this can lead to single event upsets in sequential logic or in the configuration RAM of the FPGA. Irradiation tests have therefore been developed and carried out using the cyclotron in the physics department at the University of Oslo in Norway. The objective of the test experiment was to measure the radiation tolerance of a SRAM-based field programmable gate array (FPGA). This paper presents an overview of the irradiation tests, the latest test results and will address further investigation into hardening techniques.

## I. INTRODUCTION

The ALICE TPC is a large gas cylinder ( $88 \text{ m}^3$ ) divided in two drift regions by a central electrode located at its axial centre. A field cage creates a uniform electric field along each half of the chamber. Charged particles traversing the TPC volume ionise the gas along their path, liberating electrons that drift towards the detector end plates. The end plates consist of readout chambers divided into 18 regions on each side of the TPC, each region divided into 6 sections.

The readout electronics for the ALICE TPC detector consists of 4356 front-end cards (FECs) that contain the complete chain to readout the signals coming from 570132 pads. The front-end cards are grouped in 216 readout partitions, each controlled by a Readout Control Unit [2] fig. 1(RCU) that interfaces the FECs to the DAQ, the Trigger, and the Detector Control System. Each RCU contains the Altera APEX EP20K400E FPGA we have tested.

Due to the Field Programmable Gate Arrays (FPGA) increased complexity they are in many cases becoming more at-

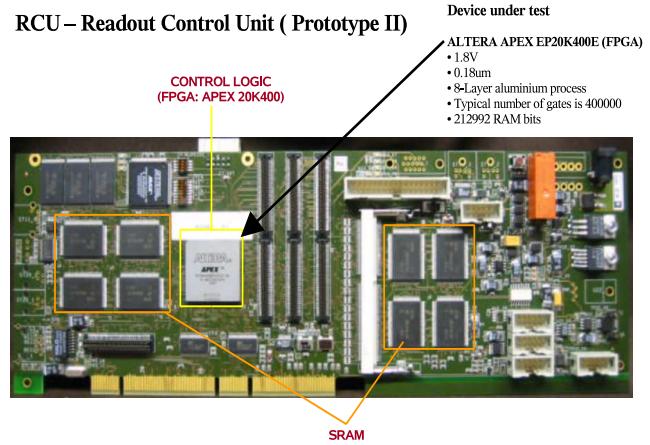


Figure 1: RCU prototype II layout. SRAM is organized in 2 banks with separate data and address lines. The control logic is contained in the on board FPGA (DUT)

tractive in use than the alternative ASICs. FPGA based on SRAM technology makes it possible to reprogram the device and may shorten the production time of the design. However compared to the radiation tolerant ASICs, the FPGAs are sensitive to Single Event Upsets SEU. Experiencing SEUs during an ALICE experiment run may have fatal consequences. An upset in the configuration RAM can lead to a corrupt design and therefore a loss or stop in the data collection due to a reprogramming of the device. It is therefore necessary to investigate the radiation tolerance of the front end electronics. While configuration RAM upsets will have to be repaired by reconfiguration of the device, register bit-flip may on the other hand be corrected with different kinds of detecting/correcting coding techniques. For a low rate of upsets during an ALICE lifetime

this may show to be a sufficient solution.

## II. SINGLE EVENT UPSET, SEU

A single event upset [3] corresponds to a soft error appearing in a device due to the energy deposited in silicon by an ionizing particle. The main concern are high-energetic ( $E > 20$  MeV) particles (protons, neutrons, pions) which induce nuclear reactions in the silicon. An incoming proton will not deposit enough charge to cause a SEU through direct ionization. Most protons pass through the device with little effect, however a few incoming energetic protons can collide with a nucleus in the device material. This results in complex nuclear interactions which creates a heavy recoil ion. The heavy ion in turn ionizes the device material which through it travels, and leaves behind a track of electron-hole pairs. If this happens near to for instance a CMOS transistor, the newly created carriers will drift in the electric field in the material and will be collected at a nearby node. If the charge is sufficient to flip the state of the transistor from a binary "1" to a "0" or vice-versa, this will be a Single Event Upset. A SEU is non-destructive and a rewriting or reprogramming of the device will return the device to normal behavior thereafter. A SEU can be induced as a bit flip in a configuration memory cell or in sequential logic as a bit flip in a register. An upset is random in time and all the memory bits have the same probability of being affected.

## III. EXPERIMENTAL ARRANGEMENT

The Oslo Cyclotron [4] is situated at the University of Oslo, Department of physics. It is a Scanditronix MC-35 and can deliver an external proton beam of 29MeV, with beam intensities  $\geq 10\text{pA}$ . For our test we have used a beam spot of  $1\text{cm}^2$ . For our test we have used a beam spot of  $1\text{cm}^2$ . The beam distribution is made as uniform as possible by defocusing and using a gold foil placed upstream in the beamline.

### A. Setup and alignment

The DUT, which is mounted on the RCU prototype, is placed in the proton beam with its top surface perpendicular to the beam axis, see fig. 2. It is in turn connected to another RCU card in the PCI bus of a Linux PC (experiment PC) running software for communication and data collection from the DUT. The communication protocol between the two RCU cards is the Slow Control Serial Network [5](SCSN). The SCSN consists of a VHDL block design on the FPGA placed on both RCU cards. This means that there is a possibility of experiencing single event upsets in the SCSN design as well. In future version the communication handling will be moved out of the DUT. For now, a periodic loop back of the output of the SCSN is done to check for upsets related to the communication. Another Linux PC is placed in the control room and is used for

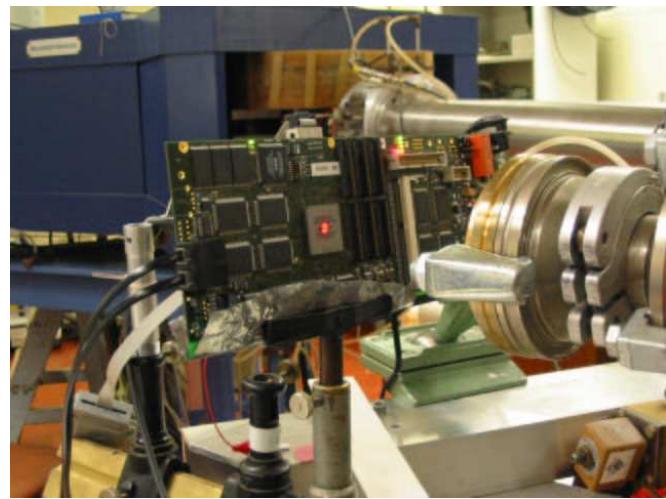


Figure 2: RCU prototype card mounted in the beam path. A laser is used to align the FPGA correctly

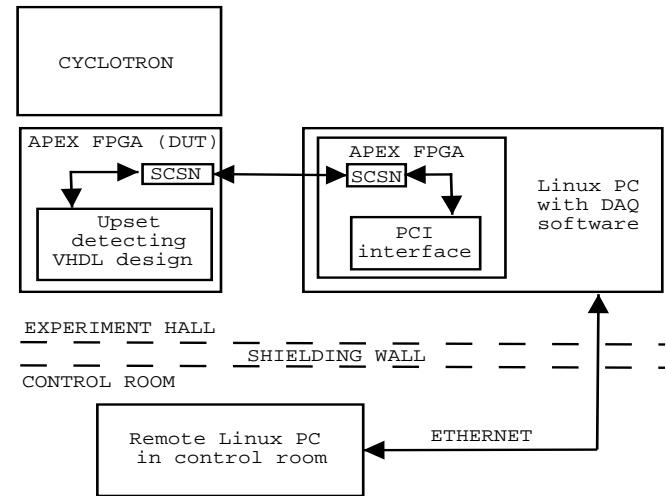


Figure 3: schematic showing an overview of the basic architecture of the test setup

remote control of the irradiation test. Both PCs are connected to Internet and the test can in principle be run from anywhere. In fig. 3 a schematic overview of the setup is shown.

The alignment of the DUT is done by using a laser mirrored in parallel to the beam path.

A camera is placed in the experiment hall and with the help of a monitor in the control room a ceramic viewer with a marking spot is aligned in the beam. A proton beam in the order 10 times the test intensities illuminates the viewer. The marking spot on the viewer is used as a reference for the laser so that the DUT can be securely mounted in the beam path when the beam is off.

## IV. SEU MEASUREMENT

### A. DUT

The device tested was the ALTERA APEX EP20K400E FPGA [6] [7]. This device is fabricated in a 1.8V, 0.18um, 8-Layer aluminum process. The APEX 20KE device is constructed from a series of MegaLAB structures. Each MegaLAB structure contains 16 logic array blocks (LABs), one Embedded System Block (ESB), and a MegaLab interconnect, which routes signals within the MegaLAB structure. Each LAB consists of 10 logic elements (LEs). The ALTERA APEX EP20K400E FPGA contains 16640 logic elements and 212992 internal RAM bits, and the typical number of gates is 400000. Each logic element has a programmable register, a four-input Look Up Table (LUT) and carry and cascade chains. The RAM bits are divide throughout the device in Embedded System Blocks (ESB). The ESB can implement various types of memory blocks including dual-port RAM, ROM and FIFO. It is housed in a 672-Pin FineLine BGA Package.

### B. Upset detection

The ALTERA FPGA tested does not offer the option to read out the content of the configuration RAM. Therefore the configuration upsets have to be detected indirectly using a design implemented in VHDL code. This means that a bit flip or an error observed will reflect the change in logic due to an upset in a configuration bit, and not the configuration bit flip itself. A 100% use of configuration memory bits is very unlikely, thus configuration upsets that will not influence the behavior and therefore not be detectable, can occur. Thus the result will not give an exact number of configuration bit flips, but only an estimate. It is also hard to say if a detectable change in logic is due to a single or a double bit flip in the configuration RAM. A change in the logic caused by a configuration upset or a single bit flip induced directly in the logic will at first glance have the same appearance. It will only be distinguishable by looking at it over time. While a configuration upset will give a permanent change in the logic, until reprogramming of the device, and therefore be reflected as a stuck at error in the read out, a single bit flip will only be present until the next clock cycle loads a new value into the register. Taken in account the above discussed behavior of upsets, a VHDL design to detect both single bit flips in sequential logic and configuration upsets was designed. Since the ALTERA APEX FPGA contains both logic elements and internal RAM, the design should concern both. The design implemented is a 32 bit wide and 400 bit long shift register in the logic elements, see principle schematic in fig. 4, and a 32 bit wide and 4096 bit deep FIFO in the internal RAM blocks. The shift register uses approximately 90% of the logic elements while the number for the internal RAM bits is 60%

A walking one and zero pattern was shifted through both the shift register and the FIFO. The read out pattern from the design is compared with the expected value and if it differs a

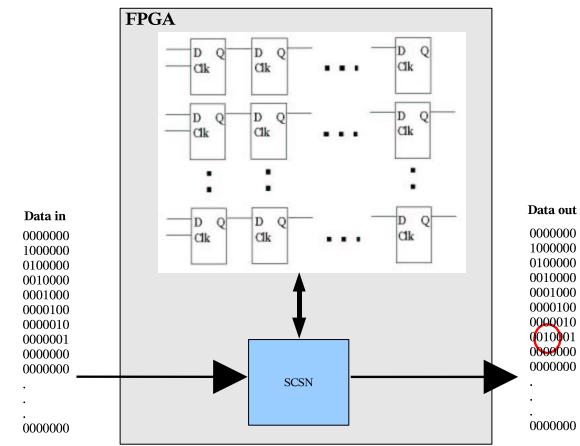


Figure 4: The shift register is implemented in the logic elements of the FPGA. A fixed pattern is shifted through the register and is compared for expected value at the output. The shift register is 32 bit wide and 400 bit long

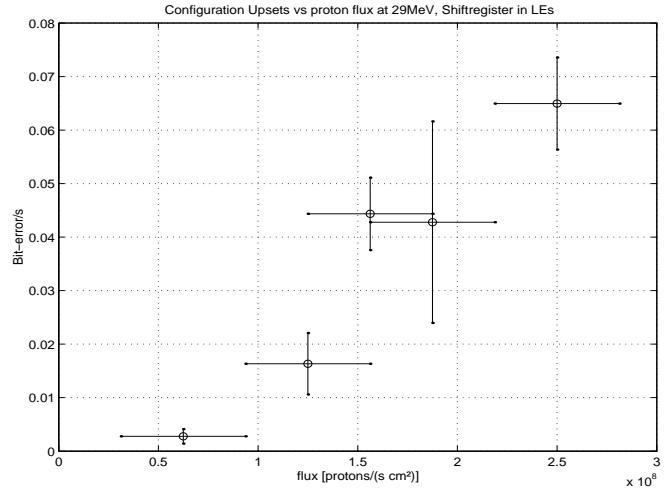


Figure 5: The rate of configuration upsets in logic elements plotted versus the flux

single event upset has occurred.

## V. RESULTS

Irradiation of the FPGA was done with a 29MeV proton beam with fluxes ranging from  $0.63 \cdot 10^8 - 2.5 \cdot 10^8 p/cm^2 \cdot s$ . Several runs were done and the results are plotted in figures fig. 5, fig. 6, fig. 7. The cross-section for the configuration upsets in the logic elements is plotted in fig. 8. The plots for the upsets in the internal RAM is corrected by a factor of 1.7 due to the use of RAM bits is 60%.

Assuming the upsets are random in time and uncorrelated we would expect a linear dependency in the upsets plots and

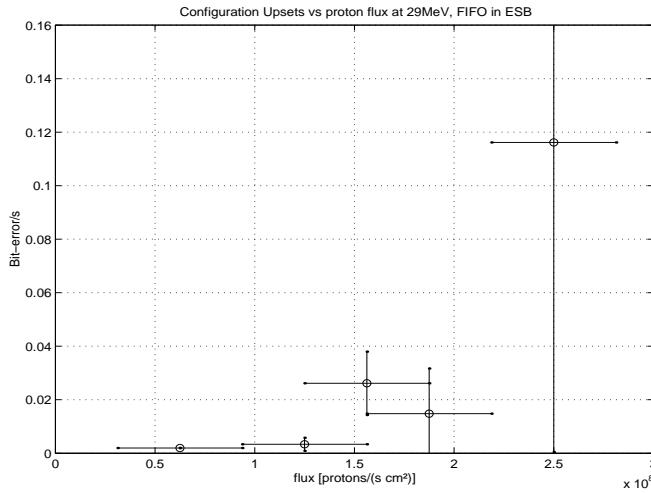


Figure 6: The rate of configuration upsets in internal RAM plotted versus the flux

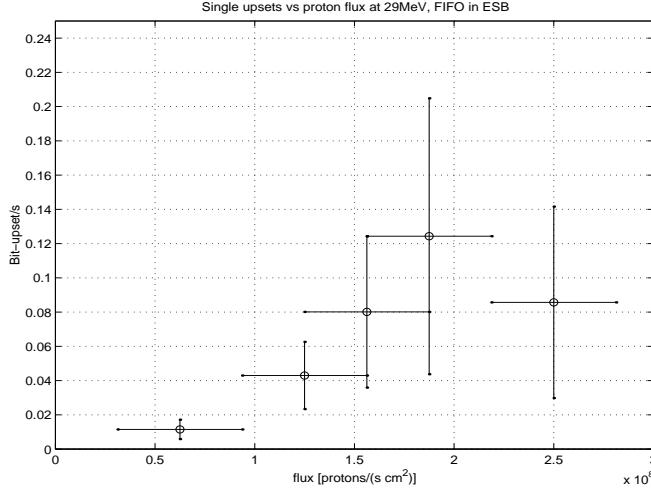


Figure 7: The rate of single upsets in internal RAM plotted versus the flux

a constant value in the cross-section plots. For the configuration upsets in the logic elements we can see the resemblance of a linear plot. However the error bars are considerable due to uncertainties in the measurements.

For these test single bit flips are discovered in the internal RAM only, and the corresponding cross-section is higher than for the configuration upsets in the logic elements. The reason for this might be that the density of SRAM cells in the ESB blocks are much higher than in the logic elements. And therefore the probability of hitting a SRAM cell in the internal RAM is considerably higher.

In the logic elements the SRAM cells will configure the behavior and interconnection of the logic, and this is only done once. For the internal RAM the SRAM cells will be updated every time they are written to. Since the Embedded System

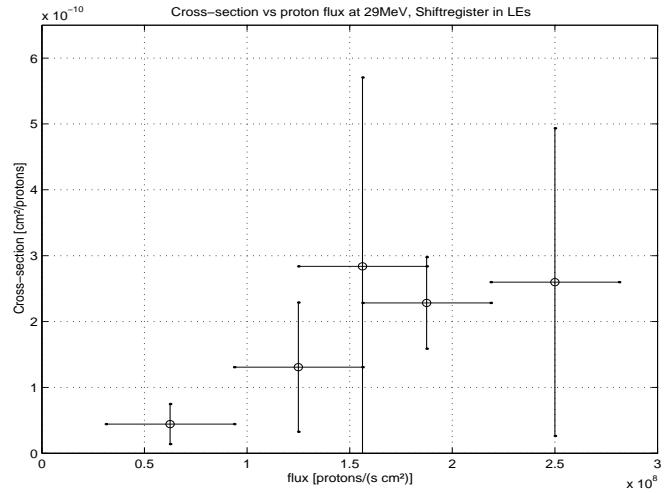


Figure 8: A plot of the cross-section versus the flux for configuration upsets in the logic elements Cross-section  $1.9 \times 10^{-10} \pm 0.8 \times 10^{-10} \text{ cm}^2$

Table 1: Cross-section for configuration upsets

Type	Cross-section [ $\text{cm}^2$ ]
Logic	$1.9 \times 10^{-10} \pm 0.8 \times 10^{-10}$
Internal RAM	$1.5 \times 10^{-10} \pm 0.8 \times 10^{-10}$

Table 2: Cross-section for single upsets

Type	Cross-section [ $\text{cm}^2$ ]
Logic	$< 5.3 \times 10^{-12}$
Internal RAM	$4.1 \times 10^{-10} \pm 2.2 \times 10^{-10}$

Blocks also contain some logic like input registers this might be the reason that we also see configuration upsets in the internal RAM.

## VI. HARDENING INVESTIGATION

As the device sizes decrease the circuits become more sensitive to soft errors as for instance single event upsets. Fault-tolerant techniques have therefore emerged as an important design consideration for FPGA-based systems. The FPGA has become more complex over the last few years and can today implement a whole system on one chip. While a SEU in a RAM or FIFO will only give a loss in some data points, a configuration upset in the logic of the device may cause the functional behavior of the design to change. So different fault-tolerant techniques have to be considered for the control functions and the data storage circuits. A single flip in a storage device can be detected and corrected by using for instance hamming coding. In logic elements different error detecting techniques can also be used to detect and if possible correct an error. However if the configuration of the logic is affected a solution will be to use redundancy in the circuit. If a part of the design fails an identical part placed elsewhere in the circuit continues the task until this

fails as well. Implementing two or three identical versions of a critical part of the logic may lengthen the lifetime of the device before reprogramming is needed. Introducing this kind of redundancy will of course influence the space requirements. So a priority has to be made with regards to which part of the circuit to protect. If it turns out that fault-tolerant concepts in the VHDL design will not be able to cope with the radiation experienced, one might have to face the reality of changing to radiation tolerant devices such as Flash based ones. Radiation tests of such a device, a ProASIC<sup>P</sup>LUS from ACTEL, is underway.

## VII. CONCLUSIONS

It is hard to draw any final conclusions from the tests so far. For sure single event upsets will have to be considered for the FPGA designs, but there are still a few open questions with regards to the expected radiation levels. At the moment we are planning the next test where the methods and designs will be improved to cope with some of the uncertainties experienced, and to support the preliminary results and to collect more statistics. One important change will be to replace the SCSSN communication and have the inputs and outputs of the shift register and FIFO connected directly to input and output pins. Tests will also include Flash based FPGAs. Some more detailed simulations and calculations of the expected radiation levels in the ALICE TPC detector will have to be carried out before one can decide if the rate of upsets during an ALICE run is below a acceptable level.

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