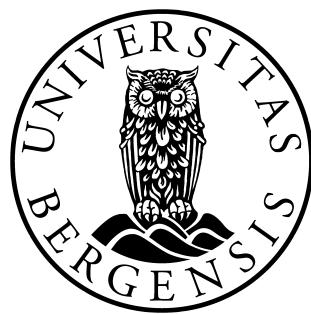


# Radiation Testing of RCU2 Components

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# Acknowledgements

# Abstract

At CERN in Switzerland the largest particle accelerator ever built called Large Hadron Collider (LHC) is located. The LHC is placed 100 meter below ground level in a 27 km long tunnel where four experiment areas are located, one of these experiment is A Large Ion Collider Experiment (ALICE). ALICE is built to study a matter known as Quark-gluons plasma, which will be generated under collisions of heavy ions. LHC is currently shutdown for maintenance and preparation for even higher energies. This period called Long Shutdown 1 (LS1), started January 2013 and will last until the end of 2014.

ALICE comprises of several sub-detectors, one of these are Time Projection Chamber (TPC), which is the main tracking device of ALICE. For LS1 it has been decided that a upgrade should be performed on the Readout Control Unit (RCU), which controls the readout in the TPC. The new RCU, named RCU2, will increase the present readout rate by a factor of up to 2.6, and will be more immune to radiation induced errors.

For the RCU2 design new components are introduced, where some of these hasn't been tested for radiation tolerance. The work presented through this thesis comprises of irradiation tests of these components. The tested components consist of power regulators, bus transceivers, limiting amplifier, multiplexer/demultiplexer, buffer, comparator, Current Shunt Monitor and the RCU2's main FPGA, the Microsemi SmartFusion2 (SF2). The tests performed consist mostly of test for accumulative effects, but test for Single Event Effects (SEE) will also be performed for some of the components.

The main focus has been on the SF2 SoC FPGA, where test of Single Event Effects like Single Event Upset (SEU), Single Event Transient (SET) and Single Event Latchup (SEL) has been executed on SRAM, logic element and PLL.

The irradiation tests has been executed at Oslo Cyclotron Laboratory (OCL) in Oslo Norway, with a proton beam of 25 and 28 MeV and at The Svedberg Laboratory (TSL) in Uppsala Sweden, with a proton beam of 170 MeV.

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# Chapter 1

## Introduction

At CERN in Switzerland there are being conducted experiments on fundamental structure of the universe. This is done by accelerating particles up to an energy level of 4 TeV per proton, and then colliding them with other particles on the same energy level. The largest accelerator is called Large Hadron Collider (LHC), and is the largest particle accelerator ever built, installed in a 27 km long tunnel. Particles are accelerated in both directions in the LHC. When the particles have reached high enough energy, particles from the opposite directions are made to collide at 4 experiment areas, one of these is called ALICE. ALICE is built to study a matter known as Quark-gluons plasma , which will be generated under collisions of heavy ions [1]. ALICE consists of several sub-detectors with different functionalities. TPC is one of these, and is the main tracking detector placed closest to the beam-line, see chapter 2. Under a collision, high energy particles will be generated, which will also pose a risk to the electronics used. It is therefore of highest importance to test everything that is planned to be used in the ALICE for radiation.

LHC is currently shutdown for maintenance and preparation for even higher energies. This period called Long Shutdown 1 (LS1), started January 2013 and will last until the end of 2014. In this period

One of the main boards used in the TPC detector is the Readout Control Unit (RCU). It has been decided that a new RCU shall be made, named RCU2. Because of the radiation level in the LHC, every component used in the design of the RCU2 has to be tested for radiation to be sure that it won't fail when it is installed in the TPC detector.

## 1.1 How to Test

The radiation tests performed through this work are mainly tests for accumulative effects. Accumulative effects are effects caused by the total radiation of a component, and are measured by the functionality and power consumption of the component, see subsection 3.4.2 for more information.

Test for Single Event Effects (SEE) like Single Event Upset (SEU), Single Event Transient (SET) and Single Event Latchup (SEL) on a Microsemi SF2 System On a Chip (SoC) Field Programmable Gate Array (FPGA) have also been performed.

Research has previous been performed on the radiation level in the ALICE TPC [2] and [3], and is used to decide if the tested components can be used or not.

## 1.2 About This Work

I started working on the RCU2-project in the autumn of 2013, and before that, the design and the schematic layout for the RCU2 was basically finished. In the design process components that already were tested or are proven to be radiation tolerant were used when possible, but such components weren't always available. Therefore my work in this project has been to do irradiation tests on components for the RCU2 design which didn't have any record of being tested for radiation.

The components which I have tested are: TPS51200, MIC69302WU, SN74AVCB164245, SN74AVC2T245, QS3VH257, SY89831, ADN2814, TLV3011 and SF2-M2S050-FG896. These components consist of: power regulators, bus transceivers, limiting amplifier, multiplexer/demultiplexer, buffer, comparator, Current Shunt Monitor and SoC FPGA. In order to investigate the radiation tolerance of these circuits I had to first acquire good knowledge of radiation induced effect that may occur in such devices. I also needed to study the components to be able to find a reasonable test methodology. Further, I had to familiarize myself with CAD tools such as *expedition PCB* and *DXdesigner* and programming and developing environments like Libero and LabVIEW in order to develop a sufficient hardware and software based test setup for the components.

The RCU2's main FPGA the Microsemi SF2, has been the main focus through this work. This is because the component will be hard to replace, and a functional failure on this one may set the whole RCU2 out of function. The radiation effects that were tested on the SF2 are SRAM blocks for SEU, logic elements for SEU and SET, and in general SEL. These effects can be read about in subsection 3.4.1.

The irradiation tests were executed in four periods; three times at OCL with a proton

beam of 28 MeV and 25 MeV, and one time at TSL with a proton beam of 170 MeV.

To summarize, this work has been consisting of practical work like making Printed Circuit Boards (PCBs), writing test code in VHDL, making LabVIEW programs and making test codes in C. It has also included getting the necessary knowledge of the components tested, learning to program in VHDL and C, as well as learning to use the tools and programs for the different tasks. And of course setting up test setup, and irradiate the components.

# Chapter 2

## ALICE Experiment

Since 1954 physicists at European Council for Nuclear Research (CERN) have studied the nucleus and its structure to find the fundamental structure of the universe. CERN is the world largest research center for nuclear and particle physics, and has a total of 21 member states. One of the biggest attractions at CERN is the Large Hadron Collider (LHC), which is a circular particle accelerator placed in a 27 km long tunnel around 100 meters beneath ground level. This is the last accelerator in a chain of up to 7 (depending on which particle to accelerate), see Figure 2.1, where the particles gradually accelerate to higher and higher energies, up to their maximum energy of 4 TeV and speed close to the speed of light. When particles have reached this energy level accelerated particles from opposite directions are made to collide inside 4 different experiment areas, where one of these is called A Large Ion Collider Experiment (ALICE), see Figure 2.2.

The main purpose of ALICE is to study a state of matter called quark-gluon plasma which will be generated when heavy ions collides. Under these collisions a temperature 100 000 times higher than the temperature of the sun is generated. There is then high enough energy to split the protons and neutrons, and achieve a plasma of unbound quarks and gluons, and that is what's called quark-gluon plasma.

All ordinary matter in today's universe is made up of atoms. Each atom contains a nucleus composed of protons and neutrons (except hydrogen, which has no neutrons), surrounded by a cloud of electrons. Protons and neutrons are in turn made of quarks bound together by other particles called gluons. No quark has ever been observed in isolation: the quarks, as well as the gluons, seem to be bound permanently together and confined inside composite particles, such as protons and neutrons.

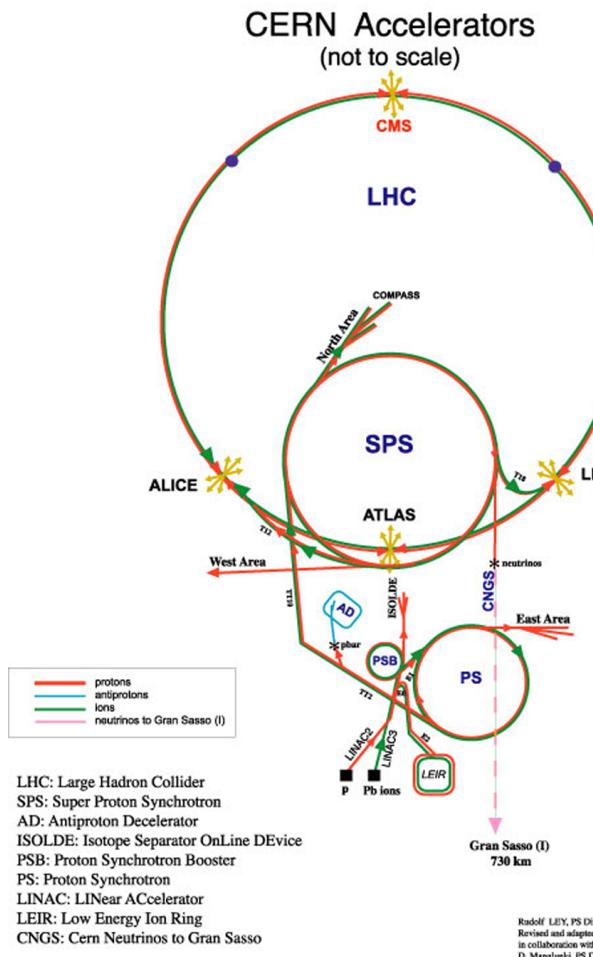


Figure 2.1: CERN accelerators [4]

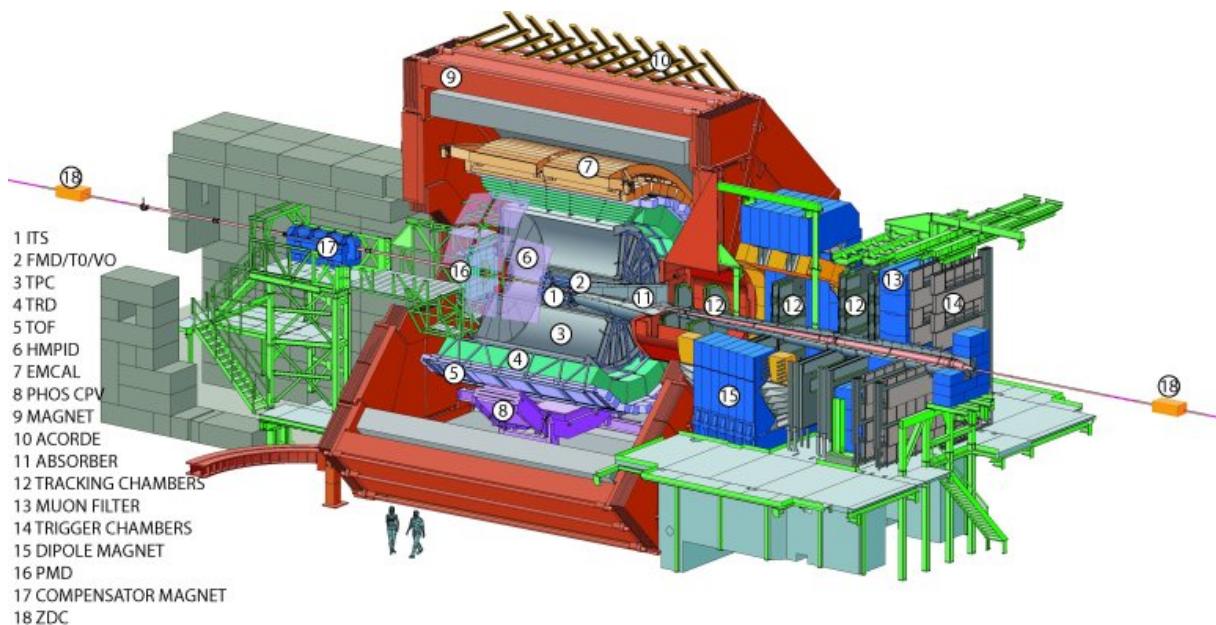


Figure 2.2: Layout of the ALICE experiment [5]

## 2.1 The Time Projection Chamber TPC

The ALICE detector comprises of several sub-detectors, where one of these is the Time Projection Chamber (TPC). The TPC is the main tracking detector of ALICE. The functions of TPC are tracking particles, measure the charged particles momentum and identification of particles. A drawing of the TPC can be seen in Figure 2.3. The TPC detector has a cylindrical shape, with an inner radius of 85 cm and outer radius of 250 cm, and has an overall length of 510 cm. The detector is made up of a large cylindrical field cage, filled with  $88 \text{ m}^3$  of 90% Ne gas and 10%  $\text{CO}_2$  gas. A high voltage electrode is placed in the center of the detector, dividing the TPC into two drift regions, and making an electric field between the electrode and the two end plates. When a charged particle is generated inside the detector, the gas inside the cage will be ionized. The free electrons and the ions will then drift in the electric field between the high voltage electrode and the two end plates. At the end-plates the Readout Chamber is located, which is divided into 18 trapezoidal sectors, where each sector is again divided into the inner and outer chamber. In the readout chamber, there are a total of 560 000 readout pads.

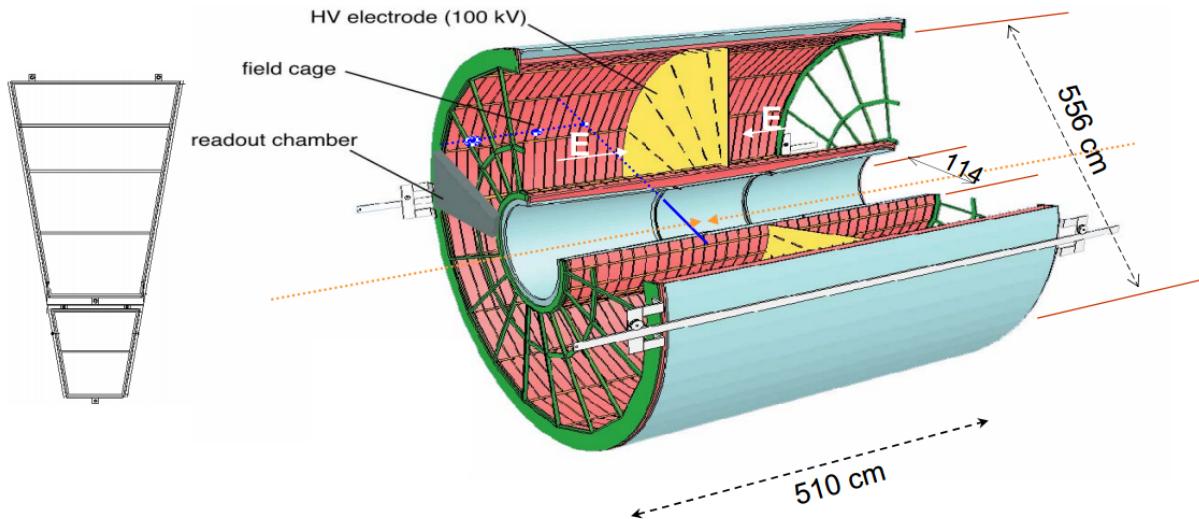


Figure 2.3: Layout of the TPC [5]

## 2.2 The TPC Front End electronics FEE

Each of the 36 sections ( $2 \times 18$ ) are also divided into 6 readout partitions; 2 in the inner chamber and 4 in the outer chamber. There are a total of 216 RCU connected to a total of 4356 Front End Card (FEC) which are connected to all of the 560 000 readout pads, and all together this sums up the Front End Electronics (FEE), see Figure 2.4. In short, the task of the FEE is to read out the charge received at the readout pads, process it and sends the acquired data to a computer.

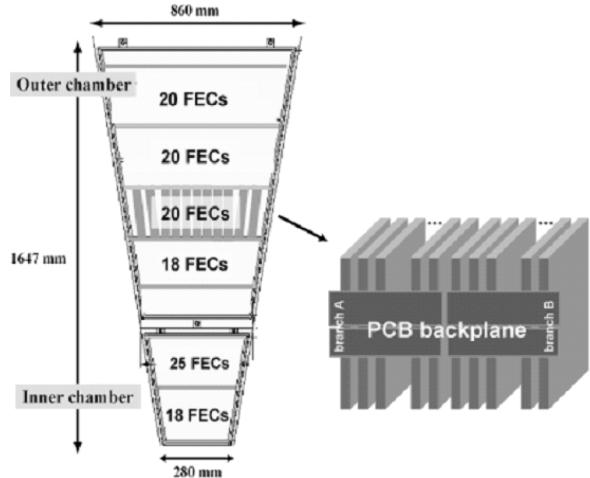


Figure 2.4: A TPC sector, showing distribution of FECs [6]

### 2.2.1 Front End Card FEC

A current signal given by one of the pads, is sent into a Front End Card (FEC) which consist of three basic functional units, see block diagram in Figure 2.5. The first unit is a charge sensitive amplifier/shaper called PASA, the second unit is a 10-bit 10 MHz low-power Analog to Digital Converter (ADC), and the last unit is a digital circuit that performs the baseline subtraction, tail cancellation, zero-suppression<sup>1</sup>, formatting, and buffering. The ADC and the digital unit together constitute the so called ALTRO chip. There are 16 PASA chips and 16 ALTRO chips on the FEC. The PASA chip is connected to 16 readout pads each, which gives a total of 128 readout pads for each FEC.

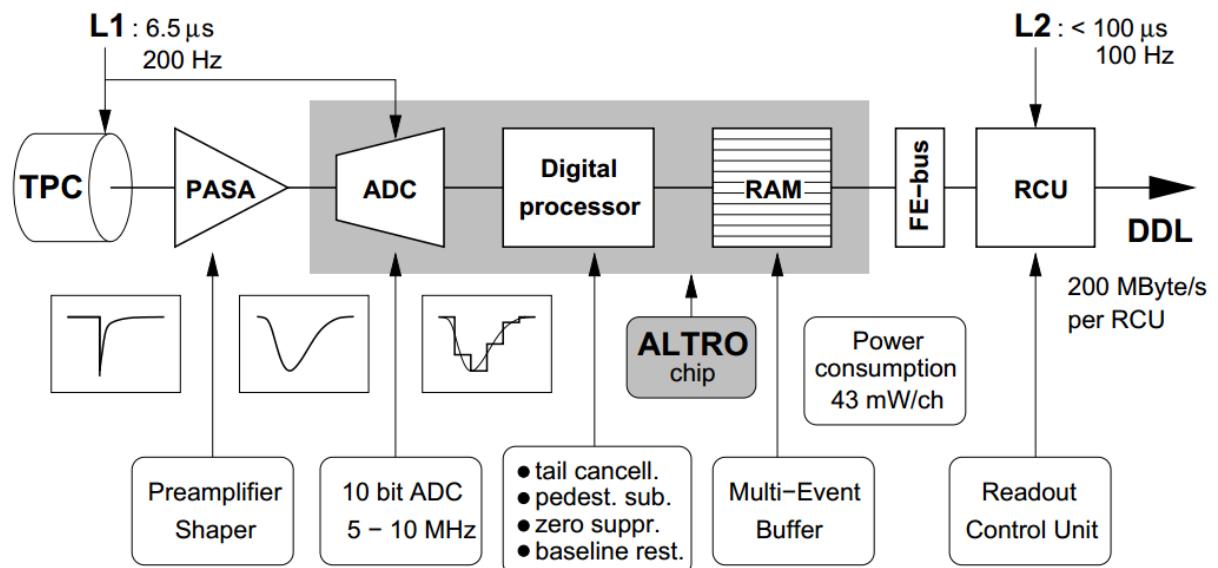


Figure 2.5: Block diagram of the Front End Card [5]

## 2.2.2 Readout Control Unit RCU

One Readout Control Unit (RCU) is connected to one row of FECs (up to 25 pieces), through a backplane<sup>2</sup>, see Figure 2.4. The RCU task is to control the entire Front End Electronics (FEE) all the way from the readout pads through the FECs, and out to a Data Acquisition (DAQ) System. The RCU consist of three separated boards which are the Motherboard board, the Control System board (DCS), and the Source Interface Unit (SIU). Most of the RCU functions are controlled by the Xilinx Virtex-II Pro FPGA. This FPGA are controlling the readout process of the TPC detector. It is also responsible for moving data from the FECs to the Source Interface Unit (SIU) board, where data is transmitted via an optical link to the Data Acquisition system. In the Data Acquisition system data is stored and is accessible for analysis.

The Xilinx Virtex-II Pro is a Static Random Access Memory (SRAM) based FPGA. SRAM cells are vulnerable for Single Event Upsets (SEUs), see subsection 3.4.1.3. Therefore a flash based FPGA, Actel ProASIC is used to monitor the SRAM memory and reprogram/reconfigure if an error occurs.

The DCS board is basically an embedded computer running Linux. This board is connected through an Ethernet link to a computer on the outside of the ALICE detector. Through this link it is possible to upgrade and reprogram the FPGAs on the RCUs. So even though the hardware is inaccessible after it has been mounted in the TPC, the SIU boards gives some kind of flexibility. In addition, it has an optical interface, receiving the clock and trigger information from the Timing, Trigger and Control system, also called TTC.

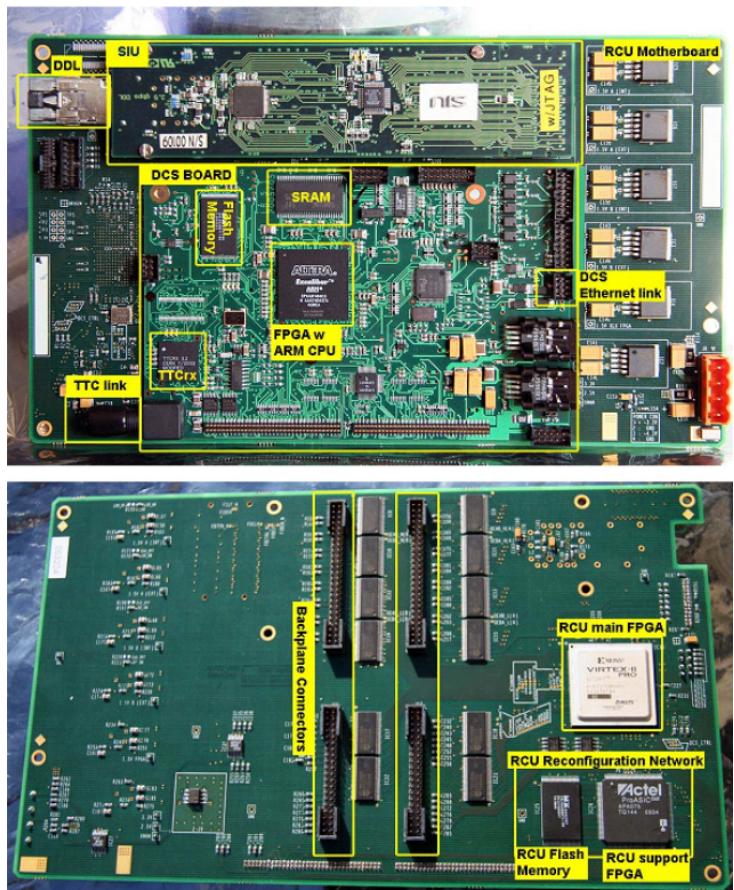


Figure 2.6: The Readout Control Unit top side and bottom side [6]

<sup>1</sup>Zero Compressions means that signal below a given threshold will be filtered away.

<sup>2</sup>A backplane is a PCB board, that connects Front End Cards to a Readout Control Unit. This is used instead of cables to get a more stability, and to keep things in place.

In Figure 2.7 you can see a full overview of the RCU and its connections.

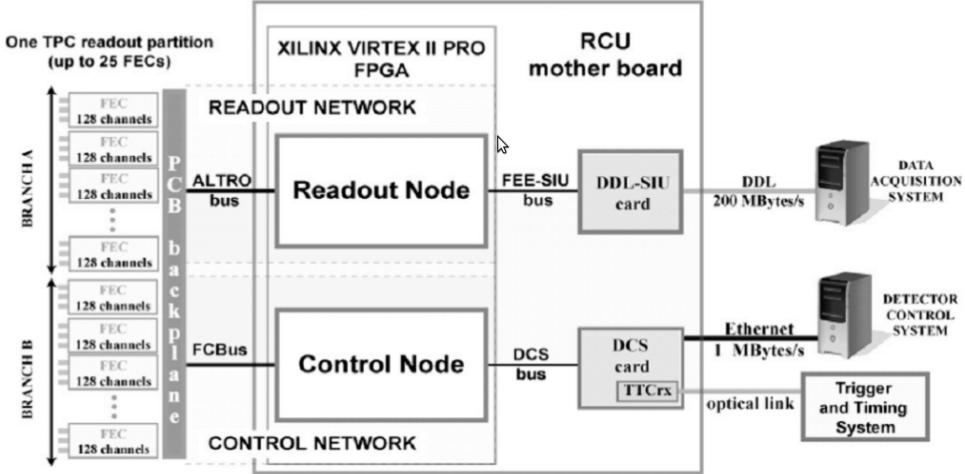


Figure 2.7: The architecture and readout path of the TPC electronics for one readout partition [6].

### 2.2.3 RCU2

#### 2.2.3.1 Why Upgrade RCU

LHC is currently shut down for maintenance and preparation for even higher energies. This period, called Long Shutdown 1 (LS1), lasts until end of 2014. The present TPC readout electronics will be a limiting factor with the foreseen readout rate for the next run period (run2) [7]. The bus between RCU and FECs is not able to read all data for high occupancy events, like Pb-Pb collisions. In addition stability issues related to SEU on the SRAM based FPGA have been observed with the present setup. 9 % of the run time had to be stopped because of errors in the TPC readout electronics [7].

#### 2.2.3.2 The New Readout Control Unit, the RCU2

The main challenge making the RCU2 was to develop a solution that gives the needed performance improvement, and at the same time was feasible within the limited time-frame. Therefore some of the old infrastructure has to be reused, like cables for Ethernet, trigger and power and the cooling envelops. RCU2 will increase the present readout rate by a factor of up to 2.6, and will be more immune to radiation induced errors.

The main difference between the RCU2 and RCU1 is that the main FPGA, the Xilinx Virtex-II Pro, has been replaced by a Microsemi SmartFusion2 (SF2) System

On a Chip (SoC) FPGA M2S050-FG896. This is a flash-based<sup>1</sup> FPGA which has SEU immune configuration memory, as well as several other radiation tolerance measures implemented [8]. It also comes with a Microcontroller Subsystem which is based on a hardcore ARM Cortex-M3 microcontroller. On the Microcontroller Subsystem a Linux system can be built, which replaces the functionality of the DCS board. The ProASIC was also not needed as a reconfiguration FPGA anymore, but will still be used as a radiation monitor. This part of the RCU2 is called RadMon, and consists of a ProASIC and SRAM chips. The TTCrx chip that was used for handling the clock and trigger signal on RCU1 was out of stock and obsolete, and will be replaced by an optical receiver and a limiting amplifier. The limiting amplifier has been tested in the work presented in this thesis, see subsection 4.2.7.

One of the limits with the old setup was that the bus between RCU and FECs was too slow, especially after the upgrade in the LHC for run2. This was fixed by dividing the readout into 4 sections instead of 2, which effectively doubled the readout speed. Therefore all of the backplanes had to be redesigned and replaced.

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<sup>1</sup>Flash-based FPGA means that configuration registers are saved in flash memory cells. Compared to SRAM-based FPGA where configuration is saved in SRAM cells, flash-based FPGA is much more tolerant against radiation.

# Chapter 3

## Radiation and Radiation effect on Semiconductor Devices

Radiation and radiation induced effects are known challenges when designing electronics which is going to be used in the LHC. It is therefore of highest importance to know about these effects, how they affect the electronics, how much damage they can cause and how to protect and prevent the radiation effects to do damage.

This chapter is based on references [9], [10], [11], [12] and [13] if not otherwise stated.

### 3.1 Interaction of Radiation with Matter

Radiation is defined as a process in which energy in the form of energetic particles or electromagnetic waves are transmitted through a medium or space. Radiation is normally divided into two categories, namely *Charged radiation* and *Neutral radiation*.

Charged radiation consist of charged particles like protons ( $p$ ), alpha ( $\alpha$ ), beta ( $\beta$ ) and heavier ions. Neutral radiation consist of neutral particles like neutrons ( $n$ ) and photons from gamma ( $\gamma$ ) and X-rays. Particles which interacts with a material will deposit some or all of its energy in the interaction, and can either interact with atoms, electrons, nucleus or the particles inside a nuclei. How much energy is deposited, and which of these a particle will interact with, depends on the energy, mass, the charge of the particle and what material it interacts with. One of the main differences between charged particle and neutral particle is that charged particles will be affected by the Coulomb force, which is the attraction or repulsion of particles or objects due to their electric charge. In the following sections we will look more closely into how a charged particle and neutral particle interacts with matters.

## 3.2 Charge particle and their Interaction with Matters

When a charged particle with high speed is passing through a material it will experience multiple elastic and inelastic collisions with the atoms in that material, resulting in slowing down or stopping the particle. When a particle collides with an atom there are several processes that can contribute to the loss of energy. They are:

- Inelastic scattering towards atomic electrons
  - Excitation and ionization
- Elastic scattering towards atomic electrons
  - Ramsauer Effect
- Inelastic scattering towards Nuclei
  - Nuclear reaction
- Elastic scattering towards Nuclei
  - Rutherford/Nuclear scattering
- Other processes
  - Bremsstrahlung and Cherenkov radiation

Which of these processes that contributes most to the loss of energy depends on the initial energy, velocity, mass and charge of the incoming particle as well as the properties of the material it collides with. For example, for heavy charge particles (protons or heavier ions), inelastic collisions with the atomic electrons in a material will contribute to most to the energy loss of the particle, fro energies below a few MeV [9]. A common expression for these processes is called "stopping power".

### 3.2.1 Stopping Power

If a particle with a given energy passing into a material, where  $dE$  is the mean energy that the particle loses by traveling through a path segment,  $dx$  of the material. Then  $-\frac{dE}{dx}$  is the stopping power or also called the "rate" of energy loss for the particle. The stopping power depends on the type and energy of the radiation and on the properties of the material it passes.

The classical expression that describe the stopping power is the *Bethe Bloch formula*, and is written as seen in Equation 3.1.

$$S = -\frac{dE}{dx} = \frac{n_A Z_A Z^2 e^4}{4\pi\epsilon_0 m_e V^2} \left[ \ln\left(\frac{2m_e v^2}{\bar{I}}\right) - \ln\left(1 - \frac{v^2}{c^2}\right) - \frac{v^2}{c^2} \right] \quad (3.1)$$

$n_A$	Number of atoms per unit volume
$Z_A$	Average atomic number of the material
$Z$	Atomic number of particle
$e$	Electron charge
$c$	Speed of light
$\epsilon_0$	Vacuum Permittivity
$m_e$	Electron rest mass
$v$	Particle velocity
$\bar{I}$	Effective material ionization potential

From this formula, if considering two different particles with the same velocity, the only factor that changes is  $Z^2$ . Therefore heavier particles will experience larger energy loss in a material compared to lighter ones. Figure 3.1 shows energy loss for different particles in air. The value of  $-\frac{dE}{dx}$  for different types of particles approaches a near-constant broad minimum value at energies above several hundred MeV, where their velocity approaches the velocity of light.

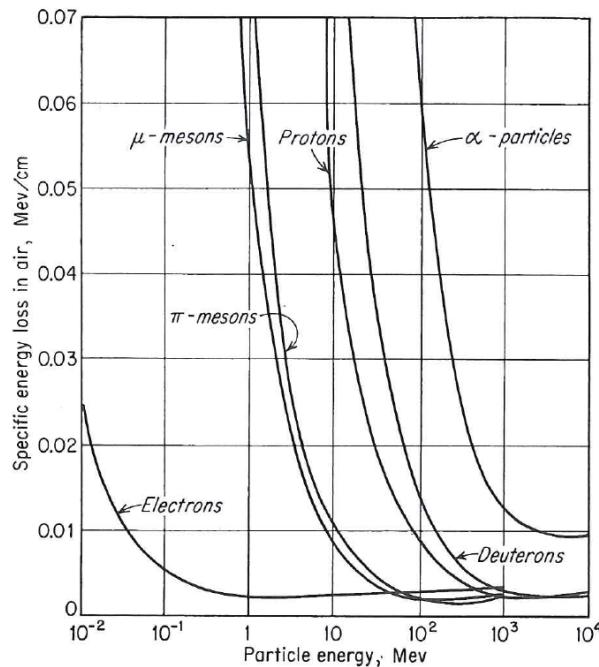


Figure 3.1: Variation of the specific energy loss in air versus energy for different particles [9]

### 3.2.2 Linear Energy Transfer LET

Linear Energy Transfer (LET) is closely related to stopping power of a particle, but instead of focusing on energy loss of a particle, LET focuses on the energy that is deposited to a material in a local volume. For low energies, LET is often said to be equal to the stopping power, even though the particle energy that turns into photons may escape the local area. For higher energies, small particles like ionized electrons can escape the local volume. The local volume is defined by the user, and can be everything from part of a molecule to a whole organ. One alternate definition of LET can be seen in equation 3.2,

$$L_{\Delta} = \left( -\frac{dE}{dx} \right)_{\Delta} \quad (3.2)$$

where  $\Delta$  is the upper energy limit for the secondary electrons included in the calculations. If  $\Delta$  is set to  $\infty$ , all secondary electrons are included in the calculations, making LET the same as stopping power.

## 3.3 Neutral particle and their Interaction with Matters

### 3.3.1 Neutrons

Neutrons are subatomic structures that are present in most atomic nuclei. Neutrons carry no charge and can therefore not interact with matter by means of the Coulomb force, which dominates the energy loss mechanisms for charged particles on energy level below a few MeV. Neutrons can also penetrate several centimeters into matters without any type of interactions, making neutrons hard to detect. When neutrons undergo an interaction it is with the nucleus of the absorbing material. This can result in total disappearance of the neutron creating one or more secondary radiations, or change of the direction of the neutron. The secondary radiations from neutrons are largely ionizing.

### 3.3.2 Photons

Photons may appear from gamma rays or X-rays. Photons have as neutrons no charge, and are therefore not affected by the Coulomb force, additionally photons have no rest mass and travel in constant speed of light. The energy of a photon is given in the formula  $E = hf$ , where  $f$  is the frequency of the particle and  $h$  is the Planck's constant. There are

three main processes where a photon may react with matter, they are: Photo electric effects, Compton scattering and Pair production.

## 3.4 Radiation Effects on Semiconductor Devices

Semiconductor devices planned to be used in a radiation environment are likely to be effected by the radiation in some way. If not taken properly into account, the radiation effects may damage or even destroy the electronics. Therefore it is of highest importance to know how irradiation can affect semiconductor devices. Normally radiation effects are divided into two groups; *Singel Events effects* and *Accumulative Effects*.

### 3.4.1 Single Events Effects SEE

Single Event Effects (SEE) happens due to the energy deposited by one single particle in a electronic device.

These effects can happen in any moment under radiation, and their probability is expressed in terms of cross section<sup>1</sup> [14]. These effects have been an increasing problem as the manufacture processes are getting smaller and smaller. In the following sections the three most known SEE will be looked more into. These are; Single Event Latchup (SEL), Single Event Transient (SET) and Single Event Upset (SEU).

#### 3.4.1.1 Single Event Latchup SEL

A Single Event Latchup (SEL) is a phenomenon where a low resistance path between power and ground is formed, causing large current to flow. Normally latches will cause burned interconnections, which means reduced performance or destruction of a chip. SEL can be discovered by measuring current of a component, and can be seen as large jumps in current. The only way to counter a latchup is by turning power off, and that is before the high current will burn interconnections and permanently set the component out of function.

How a latchup may occur can be understood by looking at a CMOS inverter, see Figure 3.2. Figure 3.2(a) shows a parasitic bipolar npn-transistor, pnp-transistor and resistors formed inside the inverter. An equivalent circuit can be seen in Figure 3.2(b). Originally both of the bipolar transistors are turned off, and no current flows through

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<sup>1</sup>Cross section is the probability that an incoming particle will induce a single event effect, and is expressed in cm<sup>2</sup>

the transistors. A latchup can be triggered if an ionizing particle flows into the substrate creating a transient current that can set  $V_{sub}$  high, causing npn-transistor to turn ON. If the npn-transistor turns ON, then current will flow through  $R_{well}$  causing  $V_{well}$  to go low and setting the pnp-transistor ON. When the pnp-transistor turns ON current will flow through  $R_{sub}$ , causing  $V_{sub}$  to rise, and a positive feedback is created, causing high current to flow from power to ground.

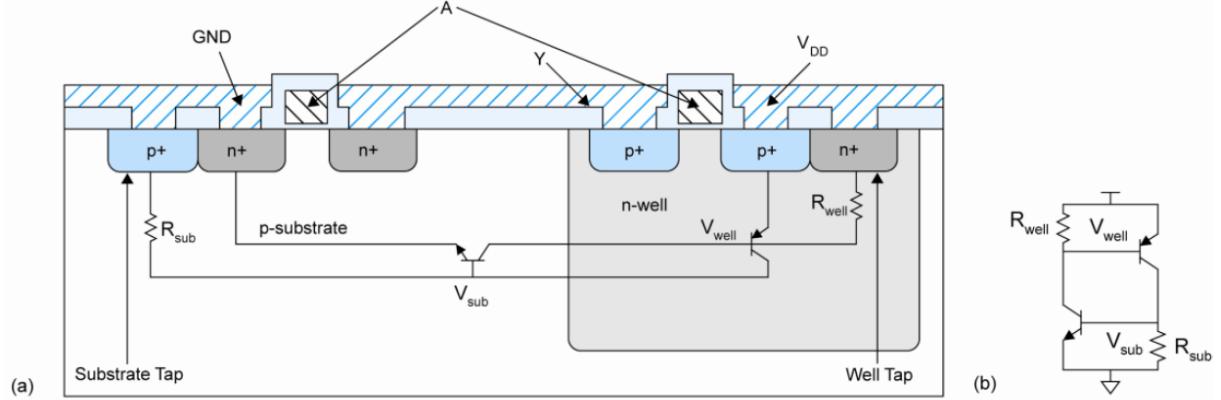


Figure 3.2: (a) A CMOS inverter with parasitic bipolar transistors (b) A model of the parasitic circuit [10]

### 3.4.1.2 Single Event Transient SET

Single Event Transient (SET) is a transient pulse of current in a logical path of a circuit. A SET is caused by an ionizing particle which travels through a material, leaving a transient current pulse on a node in a circuit. If a transient occurs close or on a sensitive circuit node like the input signal to a register, the transient can cause a short period of changed value on input node. If the clock signal to that register goes high exactly when the SET occurs, it can cause an unwanted change on the output signal of the register, which is called a SEU. If the transient is not clocked out or saved in some way, the current peak will just flat out, and will probably not be detected or cause any damage. Since SETs are close to impossible to detect, SET is often measured in terms of SEU.

### 3.4.1.3 Single Event Upset SEU

Single Event Upset (SEU) is change of state in a logical element, caused by radiation. This phenomenon can often be seen in memory cells or registers, where data is stored. A SEU is a "Soft error", which means that it is a non-destructive type of error. By resetting or overwriting after an SEU has occurred, the error will disappear.

For better understanding of SEU a six transistor SRAM cell will be explored, see Figure 3.3. We start with  $Q = '0'$  and  $Q\_b = '1'$ , which means that there is a value

'0' written to the cell. Then a high energetic neutron strikes into the drain of transistor  $D_2$  and hits a silicon atom, which causes shattering of the atom into charged fragments (ions) that travel through the substrate. These ions leave a trail of electron-hole pairs, see Figure 3.4(a). When the resultant ionization track traverses or comes close to the depletion region, carriers (electrons) are rapidly collected by the electric field creating a large current transient at that node, causing a voltage drop at node  $Q.b$ . If this voltage drop is high enough, transistor  $P_1$  will be opened, and transistor  $D_1$  will be closed, causing  $Q$  to be charged towards '1'. When  $Q$  goes towards '1' transistor  $P_2$  will be closed and transistor  $D_2$  will be open, causing  $Q.b$  to be discharged through  $D_2$ , and fall towards '0'. The SRAM cell has then got an unwanted change of value from '0' to '1', and that is called a SEU.

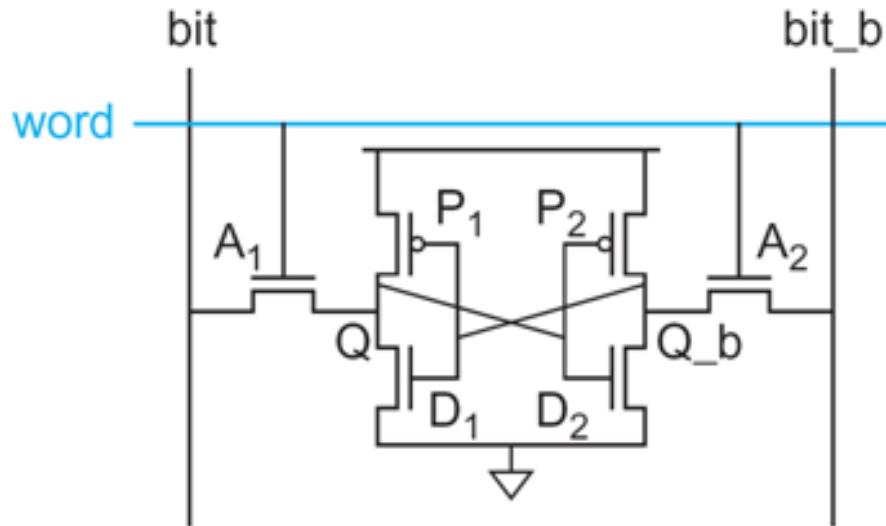


Figure 3.3: Six transistor SRAM Cell [10]

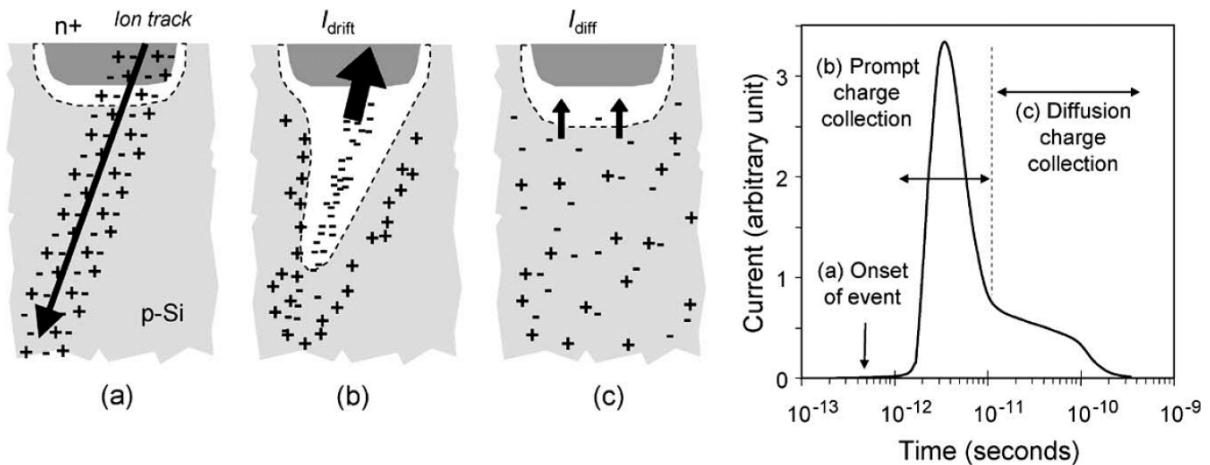


Figure 3.4: (a) Electron hole pairs generated (b) Carrier are drawn towards the depletion region causing a current jump (c) Additional charge is collected on a more long time scale (hundreds of nanoseconds) [12]

### 3.4.2 Accumulative Effects

Accumulative effects are energy deposition caused by radiation for the entire lifespan of a circuit [14], [15]. Accumulative effects are measured by the functionality of a device, and power consumption. Some circuits are weak for accumulative effects, and will stop working only after a small dose of radiation, but other devices may not even have any effect after a severe dose of radiation. When a chip stops working, it has reached its tolerance level. Talking about accumulative effects it is normal to divide into two groups; displacement damage, which is a non-ionizing effect and Total Ionizing Dose (TID), which is an ionizing effect.

#### 3.4.2.1 Total Ionization Dose TID

Total Ionizing Dose (TID) is a measurement of the energy deposited in a circuit by radiation in the form of ionization energy. The units used are Gray (Gy) or rad. The relation between those two can be seen in equation 3.3.

$$1\text{Gy} = 100\text{rad} \quad (3.3)$$

The heart of TID effects is the energy deposition in the silicon dioxide. When ionizing particles penetrate into a transistor, electron-hole pairs will be created. Most of the pairs will recombine shortly after they are generated, but some do not completely recombine because of the electric field. Electrons, with high mobility, can easily leave the oxide, but holes have lower mobility and can be trapped in their point of generation in the oxide. The trapped holes cause a negative threshold voltage shift in the MOS transistor, and if enough holes are trapped, it can result in a transistor which is permanently ON. This phenomenon can be seen in Figure 3.5.

One effect of the total ionized dose in CMOS circuits is increase in current, which could be caused by threshold change in transistors. An example with an inverter can be explored. An inverter consist of only a PMOS and NMOS transistor, if threshold decreases, time where both transistors are on will increase, leading to increase of current. Another reason for current increase is current leakage between drain and source because of trapped holes.

#### 3.4.2.2 Displacement Damage

Displacement Damage is a non-ionizing effect mostly induced by low energetic particles colliding with and breaking atoms out of the initial lattice structure of a material. This

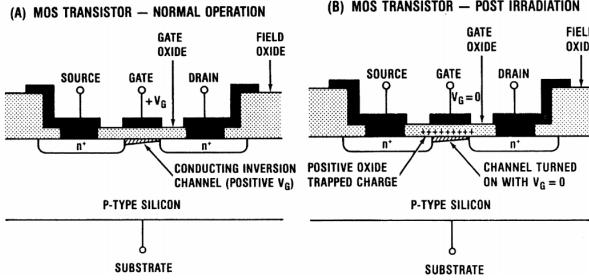


Figure 3.5: Layout of a MOS transistor. (A) Shows normal operation and (B) shows the transistor after irradiation. [6]

can affect the functionality of the device. CMOS circuits are normally considered immune to this effect. Displacement damage is not measured in any unit, but it is expressed in terms of the particle fluence, in particles/cm<sup>2</sup>.

### 3.4.3 The TPC Radiation Environment

Radiation in the LHC is dominated by high energetic neutrons and protons, mostly neutrons [3]. It would therefore be preferable to test our electronics with a neutron beam, but since there are few labs that can produce a neutron beam compared to proton beam most of the electronics are only tested at OCL with a proton beam. There has been conducted experiments that compares SEU induced by neutrons and protons [16], and the results shows that it is possible to use a proton beam instead of neutron beam with small deviations. By comparing a proton beam with a neutron beam of 21 MeV there are 10-25% less SEU cross section for a proton beam compared to a neutron beam. If the energy is increased to 88 MeV there is close to no deviation.

Several calculations has been done on the present radiation level in ALICE [3] and [17]. From these calculations it is expected a high energy hadron fluence rate ( $> 20\text{MeV}$ ) of  $0.8\text{kHz}/\text{cm}^2$ , and that is for the worst case location of the TPC electronics, and for an interaction rate of 8 kHz. Scaling this fluence rate to an interaction rate of 30 kHz, which is the expected interaction rate of Run2, the expected fluence rate becomes  $3\text{kHz}/\text{cm}^2$ . For run1 a total dose and 1 MeV neutron-equivalent fluence was estimated to be 1.6 kRad and  $4.5 \cdot 10^{10}\text{cm}^{-2}$  respectively, and this for a total operation of 10 ALICE years. If assuming a similar run program of p-p, p-Pb and Pb-Pb interactions, and then scaling for a 3 year running period of Run2 including an increased interaction rate of 30 kHz for Pb-Pb, a similar dose of around 1-2 kRad and a fluence in the order of  $10^{10}$  could be expected for run2.

# Chapter 4

## Preparations for Radiation Testing

*Testing components is a process that has been done many times before in conjunction with design of electronics that are going to be installed in the LHC. This chapter will go through all the components that are tested, and give a short description of the software and equipment used. Much of the work presented in this thesis is based on experience from previous thesis [18] [6] [19] [20].*

### 4.1 Test Methodology

The components that were tested through this thesis are: TPS51200, MIC69302WU, SN74AVCB164245, SN74AVC2T245, QS3VH257, SY89831, ADN2814, MAX3748, INA210, TLV3011 and SF2 M2S050-FG896. What each of these are, and how these were tested will be discussed in the following sections.

For each of the different components, except the SF2, a simple Printed Circuit Board (PCB) was used as a platform to be able to send inputs and measure output data. One to two USB-DAQ (Data Acquisition) devices from National Instruments, were used to connect to the PCBs. These gave us the possibility to control the inputs of each component and measure the outputs. A small resistor was placed in series with the power input. By measuring voltage drop over this resistor the current could be calculate using *Ohms law* ( $I = U/R$ ).

Two PCBs were made for each of the components that were going to be tested. This was to have more test data on each component, and as a precaution if a problem should occur with one of these. But we had two exceptions; ADN2814 and MAX3748, where only one PCB was made. All of the PCBs had a mark on the bottom of the PCB indicating the center of the component, which was used to pinpoint the center during a test.

To supply and measure everything on the test boards, Data Acquisition (DAQ) devices from National Instruments were used. The DAQ devices used are called USB-6009, USB-6008 and USB-6501. USB-6009 was used as the main one, and the others were used when more digital or analog inputs or outputs where needed. USB-6009 has 8 single-ended analog input (AI) channels, 2 analog output (AO) channels and 12 digital input/output (DIO) channels, and also a 2.5 V reference and 5.0 V output. The analog outputs have a limit of 5 mA, but some of the components that were tested required more power. In these cases the 5 V output, which is able to deliver current up to 200 mA, and a voltage regulator to 3.3 V were used, see section 4.2.2. More information on the DAQs can be seen in the reference [21].

## 4.2 The Tested Components

### 4.2.1 TPS51200 - Power Regulator

TPS51200 is an adjustable power regulator from Texas Instruments. It is specially designed for DDR RAM, it can be used for DDR, DDR2, DDR3 and DDR4 applications. On the RCU2, this is going to be used to supply a DDR3 RAM with 0.75 V.

Figure 4.1 shows the schematic layout of the PCB for TPS51200. The PCB was designed after a recommended setup for DDR3 application from the datasheet [22].

Under radiation test, an input voltage of 3.3 V was used to supply the component, and voltage over resistor R1, see Figure 4.1 was measured and used to calculate current consumption. Output voltage was also monitored.

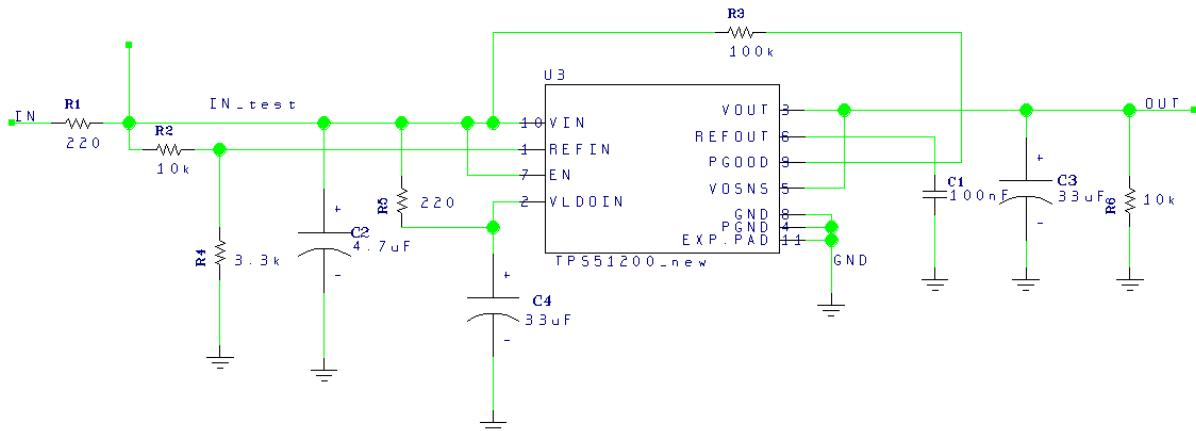


Figure 4.1: Schematic for the TPS51200 test board

#### 4.2.2 MIC69302WU - Power Regulator

MIC69302WU is an ultra-low dropout<sup>1</sup> adjustable power regulator from Micrel Incorporation. It is a high current, low voltage regulator, and can deliver a current of up to 3 A. On the RCU2 this is going to be used to regulate a 3.3 V power signal down to 1.2 V, which is used to power the SF2 SoC FPGA.

The regulator is adjustable in the way that by replacing R1 and R2, see Figure 4.2, the output voltage can be adjusted, see Equation 4.1.

$$V_{out} = 0.5 \times \left( \frac{R1}{R2} + 1 \right) \quad (4.1)$$

Under radiation test, an input voltage of 3.3 V was used to supply the component, and voltage over resistor R3, see Figure 4.2, was measured and used to calculate current consumption.  $10\text{ k}\Omega$  was used for both R1 and R2, which gave an output voltage of 1 V, which was measured under test.

A third PCB was made with this component. This version was designed with resistor values of  $R_3 = 20 \Omega$ ,  $R_1 = 5.6 \text{ k}\Omega$  and  $R_2 = 1 \text{ k}\Omega$ , which gave us a 3.3 V output. The analog 5 V signal from the USB-DAQ with current limit of 200 mA was used to supply this PCB, which gives an output voltage of 3.3 V with current limits of approximately 200 mA. This version was used to supply SY89831U, ADN2814 and MAX3748, since they required more power than what the analog outputs from the USB-DAQ can deliver.

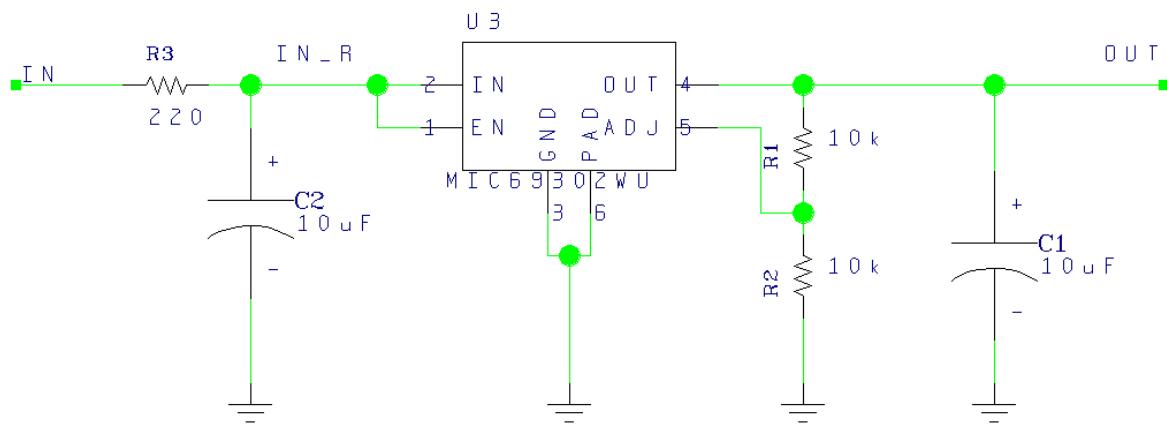


Figure 4.2: Schematic for the MIC69302WU test board

<sup>1</sup>Low dropout means that voltage on the output can be close up to the input. For MIC69302WU low dropout means that  $V_{IN} - V_{OUT}$  can be as low as 500 mV

### 4.2.3 SN74AVCB164245 - Bus Transceiver

SN74AVCB164245 is a 16-bit noninverting bus transceiver, with configurable input and output voltage. It is used for level shifting of digital signals. The input and output high values can be set to anything between 1.4 and 3.6 V, and the low value is set to GND (0 V). The direction of the signals are decided by 1DIR and 2DIR, see Figure 4.3 and [23]. On the RCU2 this is going to be used for level shifting of a 16-bit digital signal of 1.5 V to 3.3 V.

Since this component have so many input signals a small amount of current may go in to the input signals. Therefore to make sure that the component didn't use unmeasured current through the inputs of the chip, a pMOS transistor and a pull up resistor was added to the design, see Figure 4.4. When the IN signal, see Figure 4.4, is brought low the PMOS transistor will be open, pulling the input signals to ground. When IN is brought high, the PMOS transistor is closed, which means that the the input signals will be pulled up to 3.3 V from the supply signal.

Under radiation test of SN74AVCB164245, the same 3.3 V signal was used to supply both VCCA and VCCB, see Figure 4.3, which means that there is no level shifting from the inputs to the outputs, but that isn't necessary for test purposes. The voltage over resistor R1, see figure Figure 4.3, was measured and used to calculate current consumption, and the outputs were measured digitally by USB-6501. The input signal IN was switching back and forth from on to off every 4 seconds.

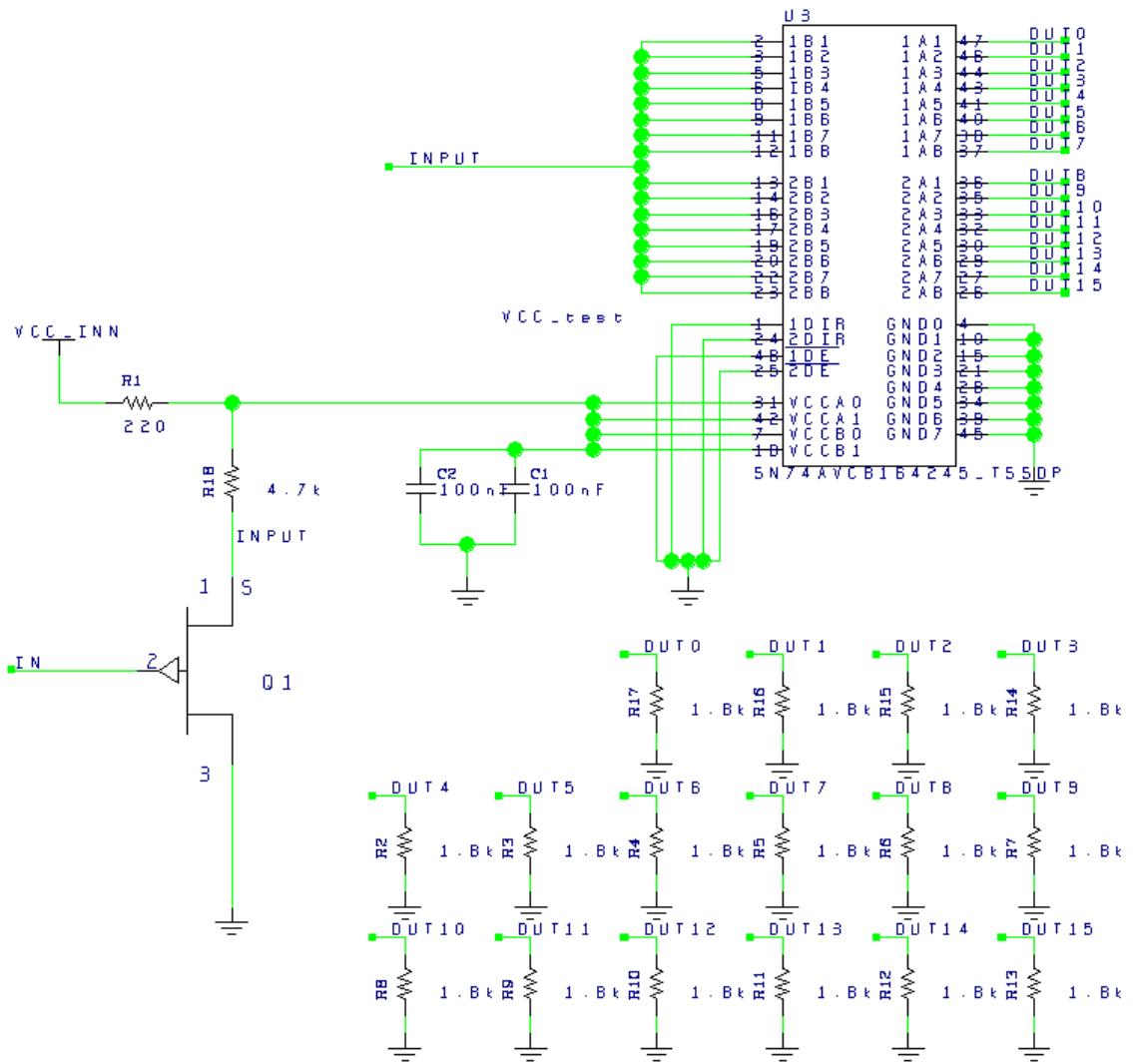


Figure 4.3: Schematic for the SN74AVCB164245 test board

#### 4.2.4 SN74AVC2T245 - Bus Transceiver

SN74AVC2T245 is a dual-bit noninverting bus transceiver, with configurable voltage. It has the same function as SN74AVCB164245, but it only have two inputs and outputs. The input and output high values can be set to anything between 1.4 and 3.6 V, and the low value is set to GND (0 V). The direction of the signals are decided by DIR1 and DIR2, see Figure 4.4 and [24]. On the RCU2 board, this is planned to be used for level shifting of a 2.5 V Serial Peripheral Interface (SPI) signal to 3.3 V.

Under radiation test of SN74AVCB164245 a 3.3 V supply voltage was used for both VCCA and VCCB, see Figure 4.4. The voltage over resistor R1, was measured and used to calculate current consumption, and the output signals were measured digitally by USB-6501. The input signals B1 and B2 were switching back and forth from on to off every 4 seconds.

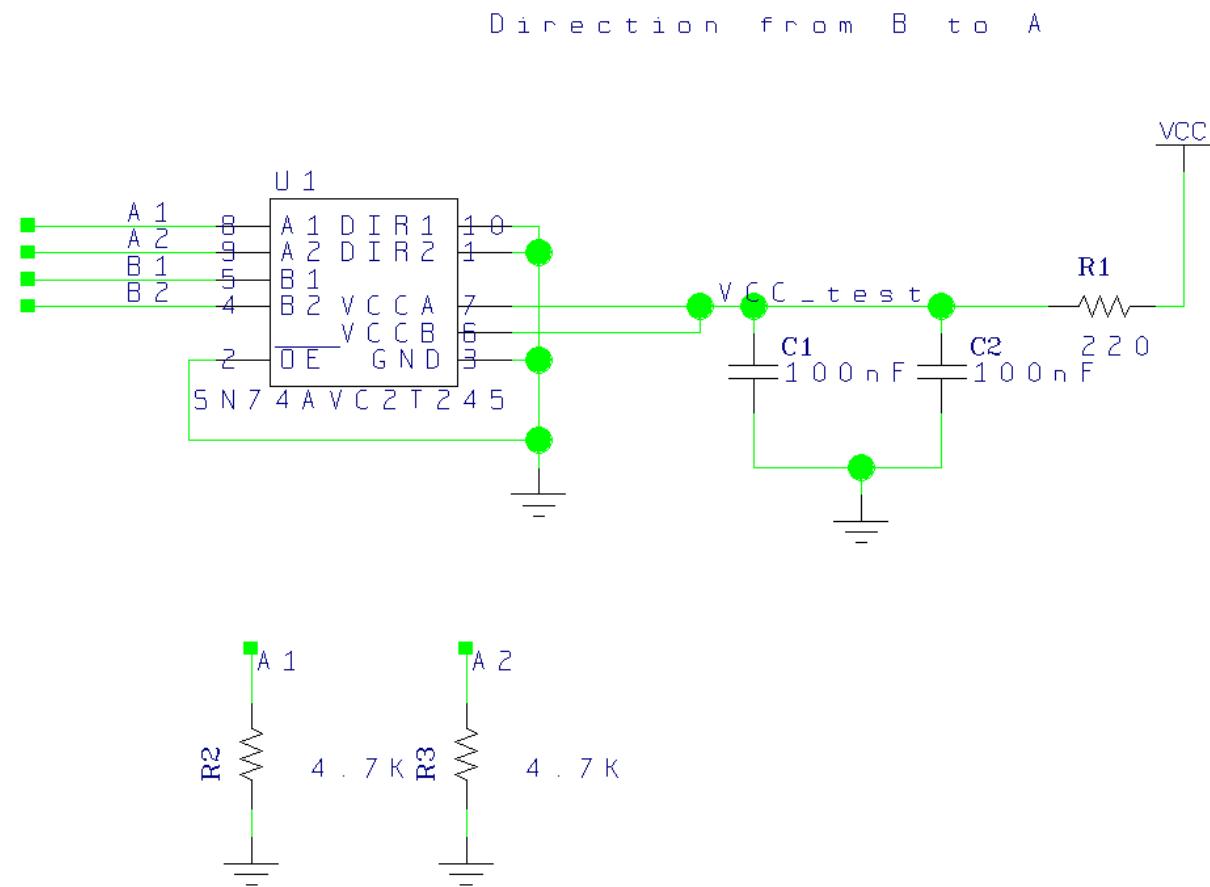


Figure 4.4: Schematic for the SN74AVC2T245 test board

#### 4.2.5 QS3VH257 - Multiplexer/Demultiplexer

This component consist of four 2 to 1 multiplexers/demultiplexers. It has high bandwidth, up to 500 MHz, low ON resistance and high OFF resistance.

Under radiation test, the supply voltage was set to 3.3 V. Voltage over resistor R1, see Figure 4.4, was measured and used to calculate current consumption. For the Select input an analog output signal was used, switching back and forth ever 4 seconds from 0 V to 3.3 V. The input and output signals were set and measured by USB-6501.

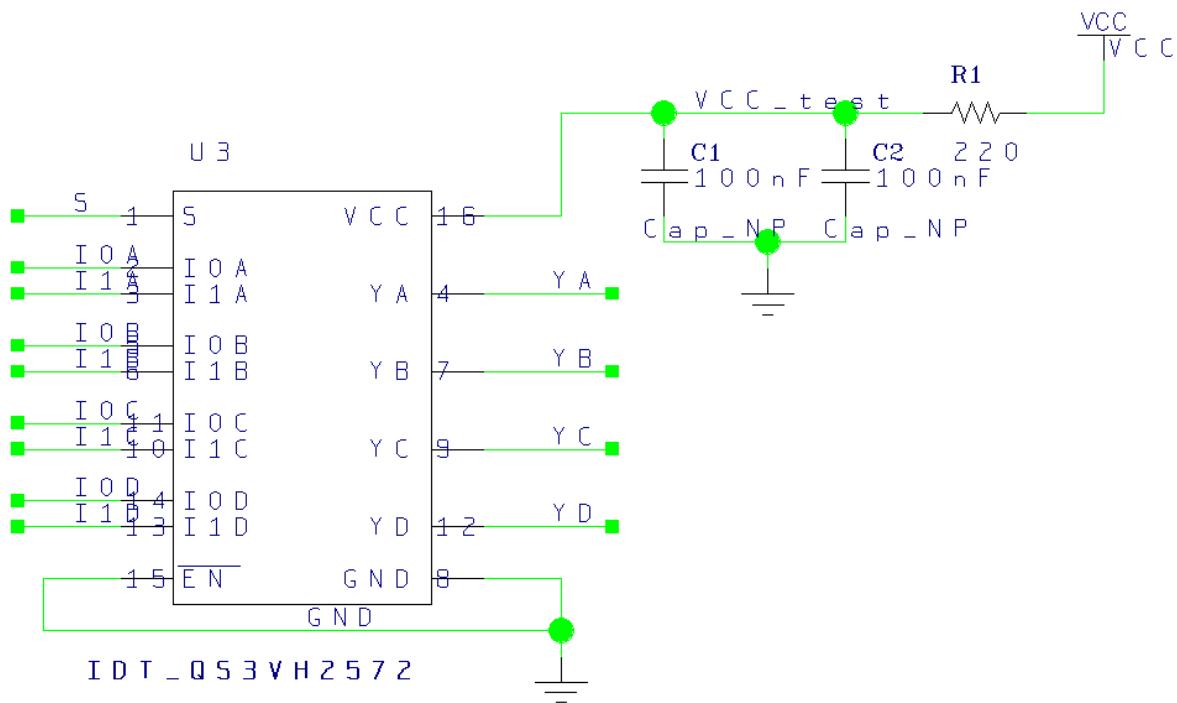


Figure 4.5: Schematic for the QS3VH257 test board

#### 4.2.6 SY89831U - 1 to 4 fan-out Buffer

SY89831U is a high speed, 2GHz differential LVPECL<sup>2</sup> 1 to 4 fan-out buffer optimized for ultra-low skew applications.

The input signal to this component is differential. The USB-DAQ devices which are being used doesn't have a differential output signal. Therefore two single-ended outputs were used to make a differential signal. The two single-ended output were set to be

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<sup>2</sup>LVPECL (Low Voltage Positive Emitter Coupled Logic) is a differential signaling system, and are mainly used in high speed and clock distribution circuits. The input/output voltages have a small swing (0.8 V), the input impedance is high and the output resistance is low. As a result, the transistors change states quickly, gate delays are low, and the fan-out capability is high.

opposite of the other, switching back and forth from 0 V to 3.3 V every 4 seconds, which results in a differential signal.

For the radiation test the modified PCB version of the MIC69302WU, see subsection 4.2.2, was used to supply this component, since it requires a current higher than the analog output from the USB-DAQ can deliver, typically around 60 mA. Current consumption was measured over the input resistor of the MIC69302WU PCB and the outputs were measured by the analog inputs of USB-6008.

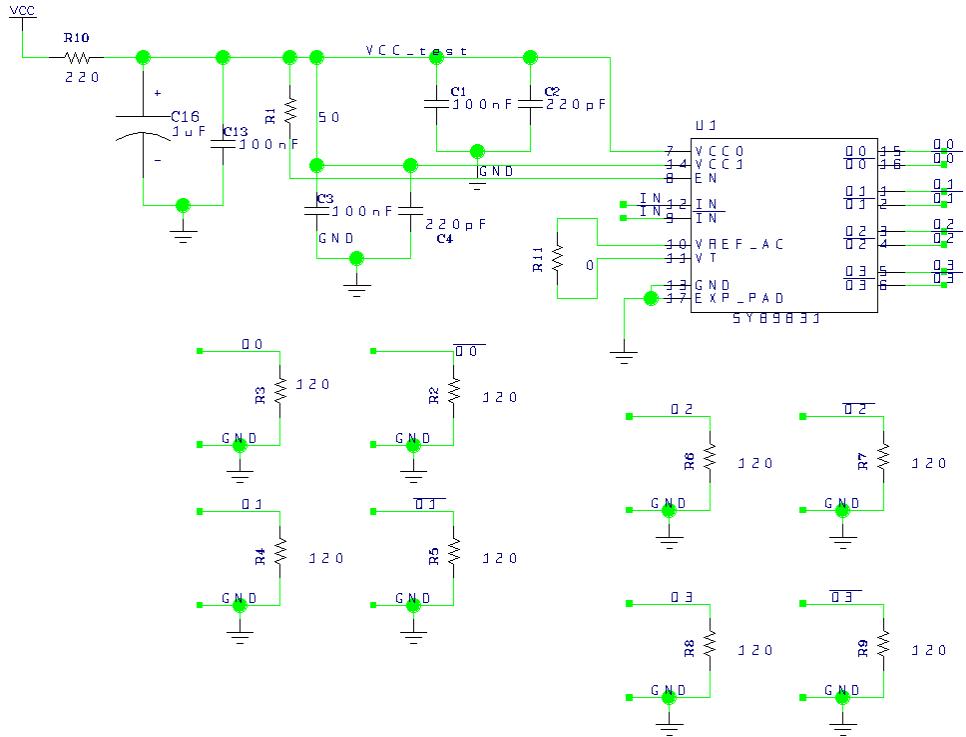


Figure 4.6: Schematic for the SY89831U test board

#### 4.2.7 ADN2814 and MAX3748 - Limiting Amplifiers

These two components are used for the same purpose, and the one of these that performs best will be chosen to be used on the RCU2. ADN2814 is a clock and data recovery component with integrated limiting amplifier. It works in rates of 10 Mb/s to 675 Mb/s, and gives output data in Low-Voltage Differential Signaling (LVDS)<sup>3</sup> format. MAX3748 is a limiting amplifier. It works in rate of 155 Mb/s to 4.25 Gb/s, and gives the output data in Current-Mode Logic (CML)<sup>3</sup> format.

On the RCU2, these boards are supposed to be used to make a stable signal out of

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<sup>3</sup>LVDS and CML are both differential signaling systems used mainly in high speed and clock distribution circuits. The output swing on such signals are typical 0.5-0.8 V, which results in high operation speed.

a not so stable signal coming from an optical receiver. The signal which is sent into the receiver is a Manchester-coded signal consisting of clock and data. The clock signal is going to be used as readout clock for all of the RCU2s, so that the readout of all of the RCU2s are synchronized. The data signal is a trigger signal which in short tells the RCU2 when it is going to do a measurement and when to send data.

There are a few differences between these two components. MAX3748 comes in a smaller package and uses less power and works in higher rates, but it doesn't have a clock and data recovery function as ADN2814 has. For MAX3748, clock and data recovery has to be done the SF2 FPGA, using FPGA logic. The clock and data recovery function in ADN2814 is actually clock recovery and data re-timing, that means that the output data is actually the same as input data, except that it is in LVDS format. This means that FPGA logic has to be used to recover data, but since the clock signal is available, it is easier to decode and extract the data signal.

To be able to make a good test for these two components, a SF2 starter-kit was used. The SF2 FPGA on the starter-kit was used to encode a clock and data signal into a differential Manchester signal that was transmitted to the component under test. The differential Manchester signal was sent to the test boards with wires, and a limited amplified version of the Manchester signal was sent back to the SF2. For ADN2814 a clock signal was also sent back. The Manchester signal coming back had to be decoded back to clock and data, which was done in the SF2 FPGA. To be able to check if the returning data was equal the original, the original data signal had to be delayed in the FPGA, since sending data through a component and back contribute to some delay. The original data was delayed by sending it through a few D-latches until the two data signals were equal. Then the two signals could be compared, this were done through a XOR-function, triggered by an 80 MHz clock signal. Every time the XOR function goes high, that is when the compared data is not equal, a counter will be incremented.

The recovered clock from the ADN chip is 160 MHz, which is a fairly high frequency. To be able to compare two clock signals of 160 MHz, a third clock signal of 160 MHz, with a phase shift of  $90^\circ$  from the two others had to be introduced. This clock signal was used to trigger a XOR-function checking the two clock signals, and if they are unequal a counter will be incremented.

The error counter values were accessed by the internal microcontroller on the SF2 chip. From the microcontroller the counter values were constantly transmitted serial to a computer where a LabVIEW program was running ready to receive data. The received data is exhibited for a viewer, and data is saved in a text file. The LabVIEW program also measures the current consumption of the component.

Both of these components required a lot of current to function correctly, so the modified MIC69302WU was also used here, see subsection 4.2.2

The decoding process of the Manchester signal returned both clock and data, but since

these are related, only data was checked.

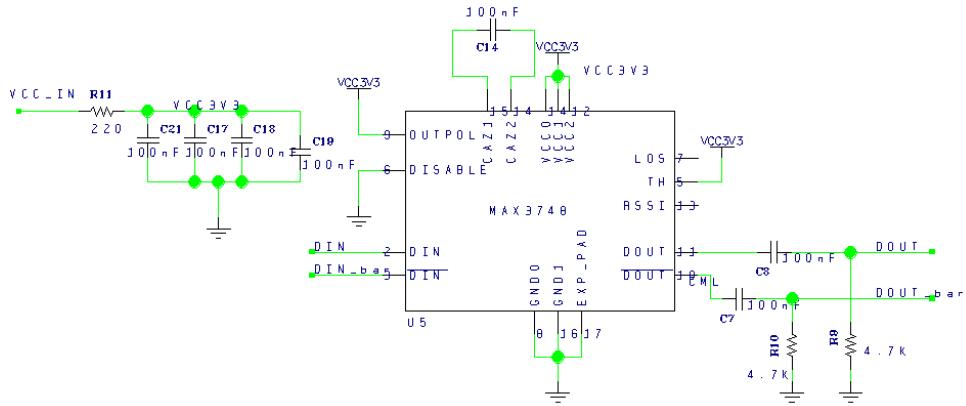


Figure 4.7: Schematic for the MAX3748 test board

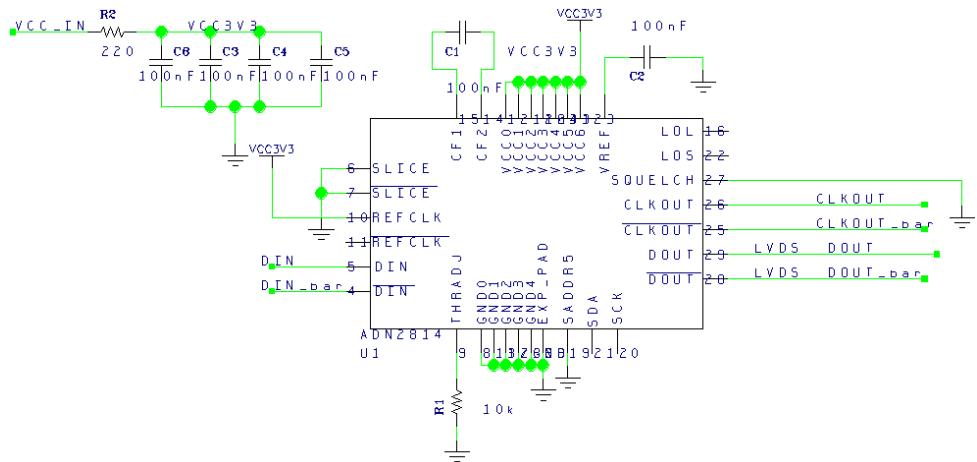


Figure 4.8: Schematic for the ADN2814 test board

#### 4.2.8 INA210 - Current Shunt Monitor

INA210 is a so called Current-Shunt Monitor, which is designed to monitor a current signal by measuring the voltage drop across a resistor (typical smaller than  $1\ \Omega$ , but could be as low as  $0.01\ \Omega$ ) placed in the current path. The measured voltage drop is amplified by 200 through the circuit, and the amplified voltage is sent to the output.

To be able to test this component a signal to measure current over is needed. This was generated by using one of the analog outputs from the USB-DAQ to produce a voltage of 3.3 V to the PCB, where a diode and a resistor was added only to use current. A shunt resistor, R1, was added in the current path before the diode and the resistor and connected to the differential input signal of the component, see Figure 4.9. When the analog output signal was on, a small current will be generated over R1, producing a small voltage drop, which was amplified through the circuit.

For the radiation test we used a supply voltage of 3.3 V, and voltage over resistor R2, see Figure 4.9 was measured and used to calculate current consumption. Output voltage was also measured.

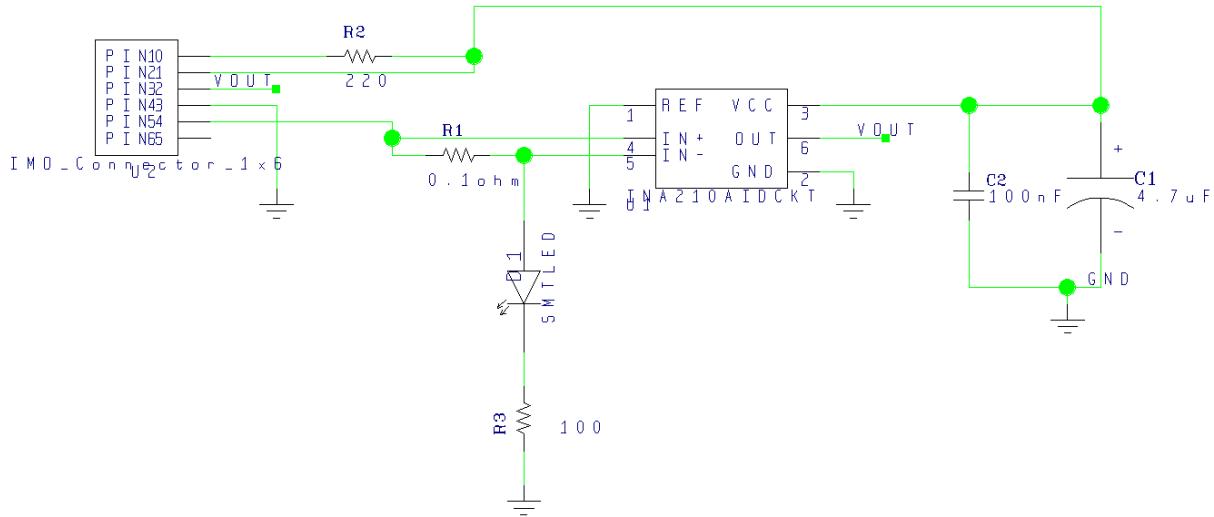


Figure 4.9: Schematic for the INA210 test board

#### 4.2.9 TLV3011 - Comparator

TLV3011 is a comparator with a built-in voltage reference of 1.242 V. It supports low supply voltage from 1.8 V to 5.5 V, and has an open-drain output with fast response time. A 10 k $\Omega$  pull-up resistor is needed on the output.

For the radiation test, we used a supply voltage of 3.3 V and voltage over resistor R1, see Figure 4.10, was measured and used to calculate current consumption. For the input signal to IN-, an analog input changing back and forth from 2 V to 3 V every two second was used. On the input of the PCB there is a voltage divider, see schematic in Figure 4.10, which means that the input to the component will go from 1.0 V to 1.5 V. The value used to compare with, is the internal voltage reference of 1.242 V, which means that if everything works, the output should go back and forth from high to low every two seconds.

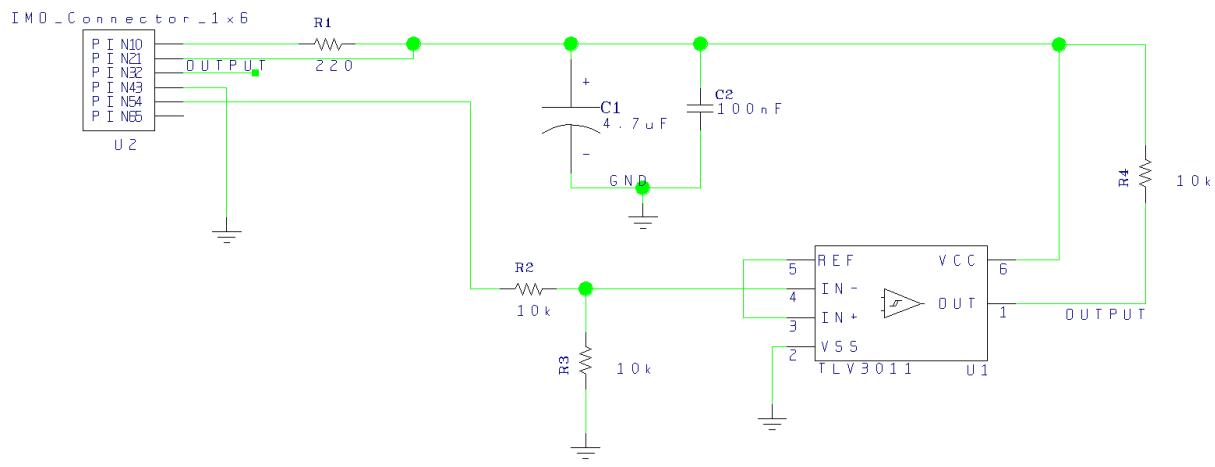


Figure 4.10: Schematic for the TLV3011 test board

#### 4.2.10 The Test Boards

In figure 4.11, 4.12 and 4.13 you find pictures of all of the different PCB boards, which have been made through this work.

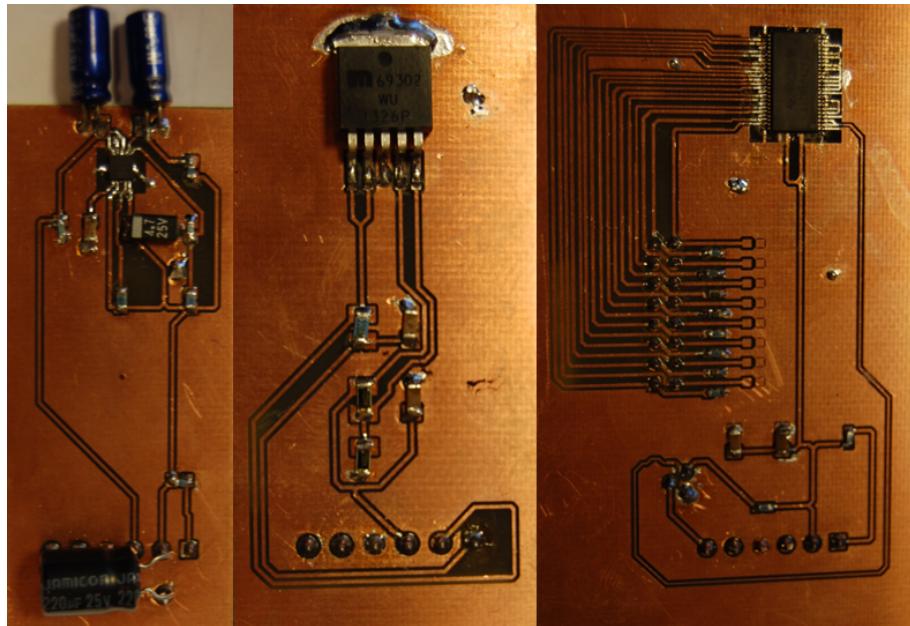


Figure 4.11: Picture of PCB boards, from left we have, TPS51200, MIC69302WU and SN74AVCB164245

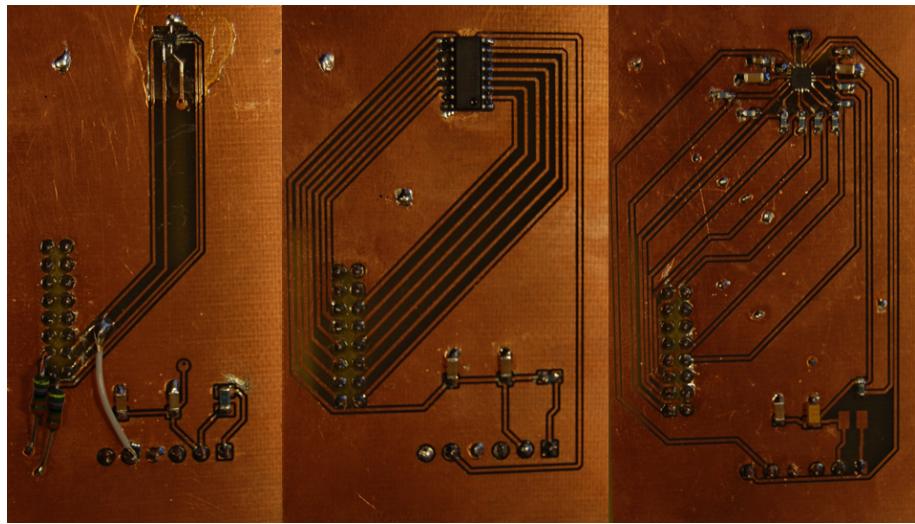


Figure 4.12: Picture of PCB boards, from left we have, SN74AVC2T245, QS3VH257 and SY89831U

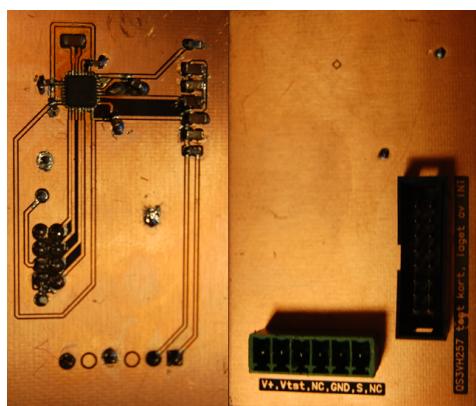


Figure 4.13: Picture of PCB boards, from left we have, ADN2814, MAX3748 and back-side of QS3VH257. The mark at the top of QS3VH257 indicates the center of the component

## 4.3 Software

For each of the different components mentioned in the section above, simple LabVIEW programs were made, specially designed to supply and monitor a specific component under radiation. In these programs, time from start, current consumption and the status of the output signal (or the output voltage for the regulators) can be measured and monitored. Data is continuously saved in a text file on the hard drive.

In figure 4.14 you can see an example of a LabVIEW program used for SN74AVC2T245.

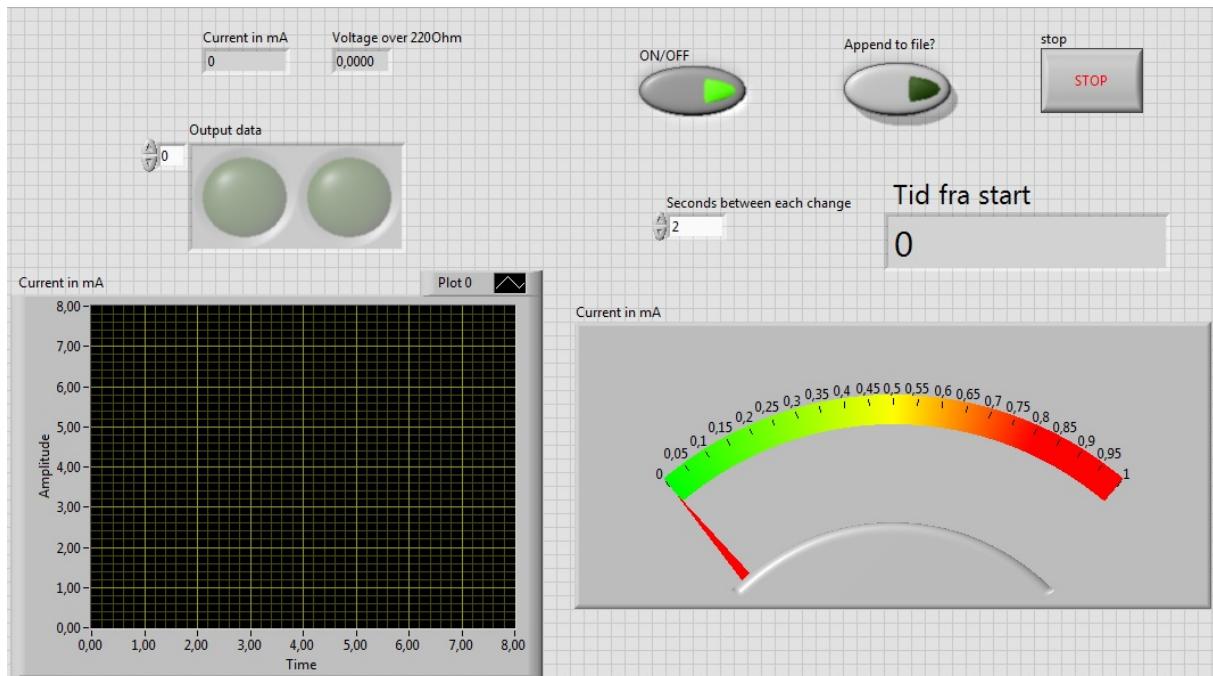


Figure 4.14: LabVIEW program for SN74AVC2T245

## 4.4 SmartFusion2

SmartFusion2 (SF2) SoC FPGA integrates a flash-based FPGA and a microcontroller subsystem consisting of a microcontroller, an ARM Cortex-M3 processor, PLLs, bus communication through APB and AHB bus, communication protocols like Ethernet, UART, SPI and  $I^2C$ , and much more. It is also said to have immune configuration memory, as well as several other radiation tolerance measures implemented. The package used for the RCU2 design is M2S050-FG896. This package consist of 56 340 logic elements, 6 PLLs, 1314 kb SRAM memory, 8 SERDES<sup>3</sup> lanes, and 377 user I/O.

<sup>3</sup>Serializer/Deserializer (SERDES) convert data between serial data and parallel interfaces in both direction

The SF2 contains a lot of functionalities, and it is therefore important to make a good test methodology to be able to check the reliability under radiation. The parts of the SF2 that have been tested through this work are the internal SRAM blocks, the logical element, PLL and Single Event Latchup (SEL). How these test were performed will be discussed in the following subsections. Other functionalities of the SF2 have also been tested, but these tests will not be discussed thoroughly through this thesis.

#### 4.4.1 SRAM test

SRAM cells are as discussed in section 3.4.1.3, sensitive to radiation. It is important to know how well the SRAM function in high radiation areas, so we would know how reliable these are when used. The SRAM blocks on the SF2 are divided up into 72 micro SRAM blocks with a size of 64 x 18 bits, and 69 Large SRAM blocks with a size of 1024 x 18 bits. Both micro SRAM blocks and large SRAM blocks are so called two ports SRAM, which means that we can access two addresses at the same time.

To test the SF2 SRAM memory a test code is written in the SF2 FPGA. In short the code writes a known pattern to all addresses and constantly checks if the values changes. If they do a counter will be incremented for every SEU detected. The test process is performed in a state machine with 3 states, see block diagram in Figure 4.15. The first state is a reset state, where all values are set to its nominal value. That means all counters are set to '0', write address is set to '0', read address set to '1', and write data is set to "1010...1010". Read address is always set to be one higher then the write address.

The second state is an initial state where all addresses are written to. Write data is inverted every address increment, so the written data is switched between 1010...1010 and 0101...0101 every other address. When the last bit is written to, the first bit is read.

The last state is a state where all of the addresses are written to, read and compared through an endless loop. The data written to an address is always inverted of the previous value on that address. This is to prevent stuck bits. The state machine will stay in this state until a reset is asserted.

The SEU counter values for the micro SRAM and the Large SRAM, as well as the number of cycles through all addresses are saved in registers and sent to the microcontroller subsystem. These registers are saved with Triple Module Redundancy (TMR), which means that the values are saved in three registers, and the majority of these is used. How the data is monitored and checked is discussed in section 4.4.4.1.

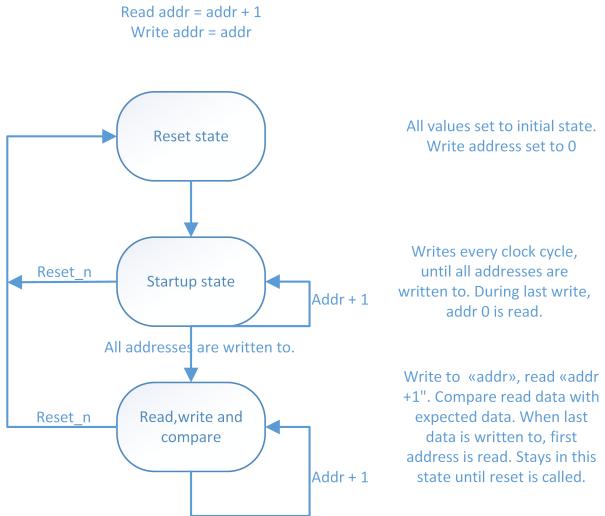


Figure 4.15: Flow chart for test procedure of SRAM

#### 4.4.2 Test of the Logical Element

A logical element consists of a 4 input Look-Up Table<sup>4</sup> and a separated flip-flop which can be used independently from the Look-Up Table. That means that we have 56 340 flip-flops and 56 340 Look-Up Tables available for our design. Flip-flops stores data and Single Event Upset (SEU) can therefore occur if exposed to radiation. Look-Up Tables doesn't save data and will therefore not suffer any SEU, but a Single Event Transient (SET) can occur. If a SET occurs in the logical element or in interconnections in the chip, the transient current will normally only appear for a small amount of time before it falls back to normal, causing no error or bit flip in the chip. But if this transient current hits a sensitive node as the input to a flip-flop, or a node that may lead to a change of value on a flip-flop input, and the changed input is then clocked out to the output, we would have an unwanted bit change or a SEU caused by SET.

The way the logical elements are tested is based on [25], which has studied how to test FPGAs in a good manner. A good overview of the design can be seen in figure 4.16. The idea is to make a long serial chain of flip-flops, also known as a shift-register, where a transient can be picked up and make a SEU. By adding an even number of inverters in between each flip-flop we increase the area where a transient can occur, without changing the logic. A known pattern is added to the input of the shift-register. This can be changed depending on how advanced you want to be, but a typical pattern could be every other '1' and '0'. To be able to operate at high speed, we are using something called Windowed Shift Register (WSR), which takes out the last n-bit of the shift register, and sends it out in parallel, with a frequency n times lower than the original frequency. To check the outputs for errors, the WSR bits will be sent through the I/O-pins to another SF2 starter kit, hereafter referred to as the monitoring board, where data is checked for errors. To

<sup>4</sup>An n-bit Look-Up Table can encode any n-bit Boolean function by modeling such functions as truth tables

be able to synchronize the two boards, a reset signal and shift enable signal will be sent from the monitoring board to the test board, and a WSR enable signal will be sent from the test board to the monitoring board.

We made generics of all the variables like number of flip-flop in the shift-register chain, number of inverters in between each flip-flop, number of bits taken out in the WSR output and how many shift-registers chains we wanted to use. Typical value used is respectively 2000, 4, 4 and 4.

In this kind of design we can have SEUs in the registers and we can have SETs that are causing SEUs. Number of detected SET is dependent on the frequency, but SEU in the register are not. To be able to distinguish between these two types of errors, we will run the test with different clock frequency, so that we will hopefully detect more SEU with higher frequency. By seeing how much increase we have with increasing frequency, we should be able to say something about how many of a number of detected SEUs are caused by SET.

Clock Conditioning Circuit which consist of a PLL, multiplexers and divider circuit, is used to configure clock signals on the SF2. The Clock Conditioning Circuit can be accessed and configured through a register, so that the frequency can be changed without needing to reprogram the SF2. For the test of the logic element the Clock Conditioning Circuit register was accessed from the microcontroller subsystem through APB bus, so that we were able to configure the clock frequency for the shift-register design without reprogramming the chip.

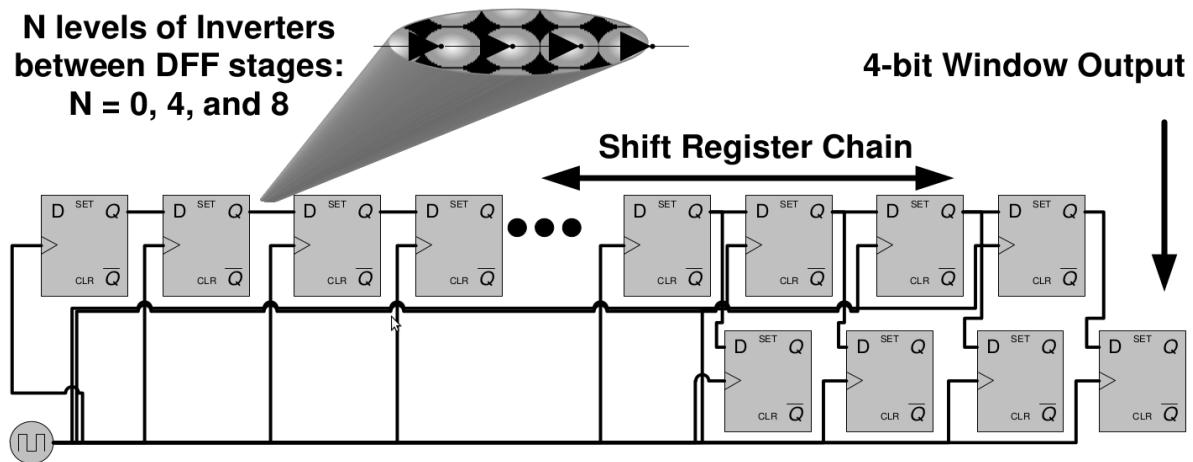


Figure 4.16: Overview of the shift-register design for test of the logic element [25]

#### 4.4.3 Single Event Latchup and PLL

A Single Event Latchup (SEL) is a short circuit between power and ground. If this occurs on any spot on the chip, an increase in the supply current can be detected. The way to

check for SEL is by constantly checking for increase in current consumption on the chip. Normally the high current will produce so much heat that interconnections in the chip will be destroyed, if not countered by shutting the power off immediately after the latch has occurred. That is why a separated PCB was made to measure the current, and to be able to shut down the board if a latch is detected. See section 4.4.4.3 for more information on that board.

To test a PLL on the SF2 the PLL's lock signal was monitored. The lock signal goes high if the output clock signal is in sync with the input, and since the input signal is assumed to be stable since it comes from a crystal, we will therefore have an indication if the PLL is working by checking the lock signal. A lock signal was checked by sending the lock signal to an I/O pin and over to the monitoring board, where the lock signal was constantly checked for a falling edge.

#### 4.4.4 Configuration and Monitoring

The SF2 M2S050-FG896 is a chip with 896 BGA pads distributed over a chip of 2.5 cm x 2.5 cm. This means that making a simple PCB is close to impossible. Therefore, to test this component, SF2 starter-kits were used. The starter-kit has serial communication to USB, which makes it possible to easily communicate with the SF2 chip from a computer. A number of GPIO pins are also available on the kit, which makes it possible to send data in and out from the SF2.

All the tests that are mentioned above are implemented into a single project, so that everything was tested at the same time. This reduced the test time, and we didn't need to use more starter-kits than necessary.

The test setup for the SF2, consists of USB to serial communicating from a computer to the SF2, a current measurement board, connected with wires to measure current, and another starter-kit (monitoring board) was connected to GPIO pins to be able to control and check the Logical element design. More details on the different test programs and boards used to test the SF2, are discussed in the following sections.

##### 4.4.4.1 Microcontroller SubSystem and LabVIEW

To get the SEU and cycle counter values from the registers in the FPGA to a computer, the microcontroller subsystem was used. The microcontroller subsystem uses APB bus to collect the counter values, and the microcontroller is sending the counter values through serial communication to a computer. A C-code was written on the microcontroller, which in short sets up the serial communication and constantly sends SEU counter and cycle counter values serial to a computer, and constantly checks for received data. The received

data is used to determine the frequency of the shift-register design, as described in section 4.4.2. A LabVIEW program was written to communicate with the SF2. The LabVIEW program is constantly checking for received data, and exhibits the newest received values for the user. Through this program it is also possible to select some specific frequencies by use of push-buttons. By pushing one of the buttons a request to change frequency is sent to the microcontroller, and when the microcontroller receives the request, it accesses the registers controlling the *Clock Conditioning Circuit*, and changes to the frequency.

#### 4.4.4.2 Monitoring Board

As mentioned in subsection 4.4.2, a second starter-kit, called monitoring board, was used to monitor and control the *Logical element test design*. On the monitoring board we were running a Linux system, where the whole test is controlled from. The monitoring boards main tasks is to monitor the lock signal(s) and the output of the shift-register test, as described in subsection 4.4.2. It is also able to select which pattern to be used in the shift-register test, and start and stop the test with a reset and an enable signal going into the starter-kit under test. The measured values from the starter-kit is checked for errors, and if any errors detected a counter will be incremented for every bit which is not correct. There is also a loss of lock counter, counting every falling edge of the lock signal. Both of these counters is exhibited to the user under a test, and counter data with time stamp is saved in a text file.

#### 4.4.4.3 Current Measurement Board

To measure the current into the SmartFusion2 starter-kit, a PCB was made with a microcontroller, serial to USB converter (FTDI chip), some debugging LEDs, power switch, and all the necessary electronics to make all this work together. The microcontroller used is a Texas Instruments MSP430AFE253. That is a 16-bit microcontroller with internal 24-bit ADC. It has an internal frequency of up to 12 MHz, and support high frequency crystal up to 16 MHz. Two types of serial communication interface are available; USART and SPI. Since the microcontroller only has a 16-bit architecture, only 16-bit of the ADC is accessible at a time. The microcontroller has 3 differential ADC inputs, which means three different currents can be measured. A current is measured by adding a small resistor of known value in series of the signal you want to measure current of, and by measuring voltage over the resistor you can calculate the current, by using ohms law ( $I = \frac{U}{R}$ )

To measure current for the SF2 starter-kit a small resistor of 0.1 Ohm was placed in series with the 1.2 V supply voltage, and a 0.16 Ohm resistor for the 3.3 V supply voltage. The voltage over these resistors were measured with the ADC, and the ADC data was sent over serial port to the “serial to USB converter”, and further to a computer. On the computer a LabVIEW program was set up to receive data through the USB port. When

data was received, the ADC value and the known resistor values were used to calculate the current. The current value was constantly saved and exhibited in the labVIEW program during a test.

The 3.3 V regulator on the SF2 starter-kit has an enable signal, where a pull-up resistor to 5 V is placed. One of the outputs on the microcontroller is connected to this pin. If the current on one of the supply voltages goes over a certain threshold, the bit on the microcontroller is set to go low, resulting in turning the 3.3 V regulator on the SF2-starter kit off. The 3.3 V is used to power all other regulators on the kit, therefore by turning this regulator off, the entire starter-kit turns off.

Schematic, PCB layout and instructions on how to use this board can be found in appendix

## 4.5 Equipment Used for Testing

Under a radiation test, some equipment is needed. In the following sections some of the equipment used for radiation test is presented.

### 4.5.1 SRAM Radiation Detector

The SRAM radiation detector boards are made by Arild Velure, as part of his master thesis [20]. It is a SRAM-based radiation detector. A lot of tests have been performed on this board, and a cross section (the probability that an incoming particle will induce an SEU) is found empirical to be  $1.14 \cdot 10^{-6} \frac{\text{cm}^2}{\text{device}}$  [20]. By checking SRAM chips for SEU, we can calculate the fluence<sup>4</sup> of the beam.

The SRAM radiation detector is a PCB with a flash-based FPGA, four 16 Mbit Cypress SRAM chips, connectors and supporting electronics. The board can be connected to a computer through an Opal Kelly XEM3001 board, which converts RS485 signal from the FPGA to USB. A LabVIEW program has been built specially for this board. From this program we are able to reset data, do some basic settings, and monitor data. The program also constantly saves data onto the disk. The board also has an optical input for scintillator counts, so we could use this board as a scintillator counter as well.

In Figure 4.17 you can see a snapshot of the LabVIEW program. From here we can monitor SEU on all the 4 SRAM chips, see scintillator counts, reset counters, see time

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<sup>4</sup>Fluence is the total number of particles that intersect a unit area in a specific time interval of interest, and has units of *particle/cm<sup>2</sup>* (number of particles per meter squared)

from start, as well as other things. SRAM1-10, as you can see on the left side, is different SRAM-boards, the SRAM-board we used was SRAM6.

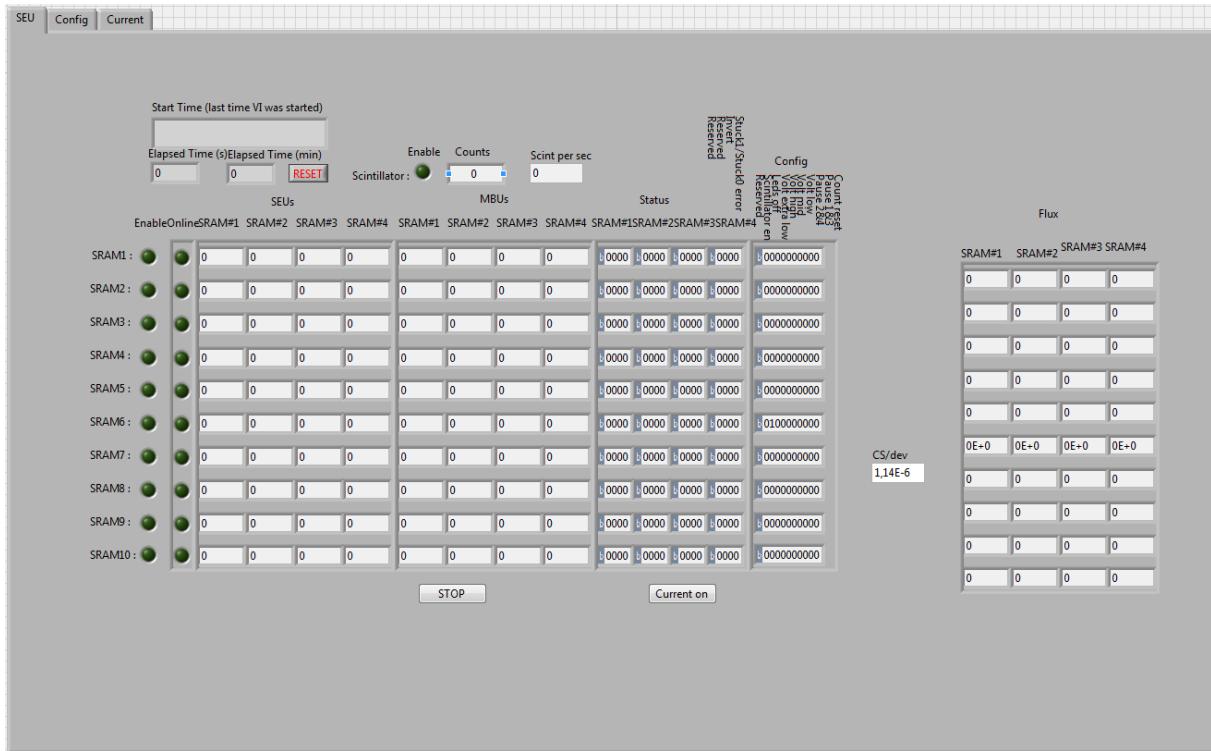


Figure 4.17: LabVIEW program for the SRAM

The approach for detecting a Single Event Upset (SEU) on the SRAM is rather straight forward, as can be seen in the flow diagram of Figure 4.18. There is an initial startup phase where a known pattern is written to all the addresses in the SRAM. When the startup phase is completed , the value from the first address is read and compared with the correct value, and if one or more of the bits are not equal a SEU has occurred, and a counter will be incremented for each bit at the address which has suffered an upset. After the read, a new value is written back to the address and the system moves on to the next address. A checkerboard pattern of alternating ones and zeroes, is used when writing to the SRAM. To check for stuck bits, the bit pattern is inverted for every cycle through all addresses.

The SRAM radiation detector also has an edge detector, which is able to detect rising edges of a signal. This is used as a scintillator counter.

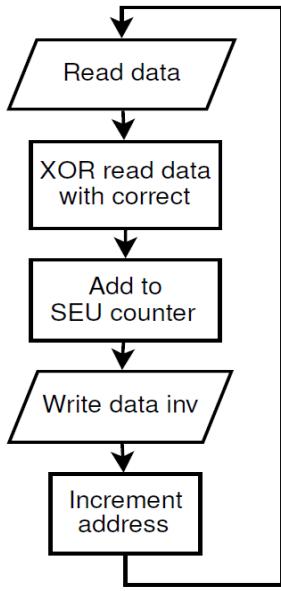


Figure 4.18: Flowchart for SEU detection

#### 4.5.2 Scintillator

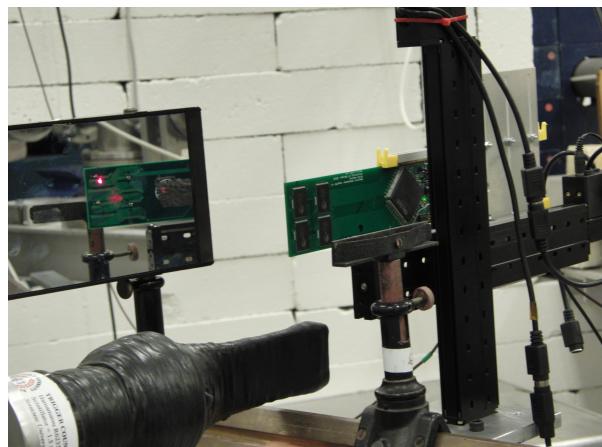
A scintillator is a material that emits light when exposed to ionizing radiation [9]. A scintillator can be used as a standalone equipment, but then only to detect that there is radiation, by seeing that it lights up. To get a more accurate measurement, we will need a PhotoMultiplier Tube (PM-tube), which has the ability to convert light pulses to current pulses by an electron avalanche process. The current pulses can be detected by an edge counter, which count every falling or rising edge of a signal.

The Scintillator with its PM-tube will be used to measure relative radiation. There are a close to linear relation between scintillator counts and SEUs on the SRAM radiation detector. Under beam setup before radiation, as discussed in subsection 5.1.2, we will find this relation, and when exposing the test boards, we use this relation to calculate or way back to SEUs, so that we can calculate the fluence for a given test.

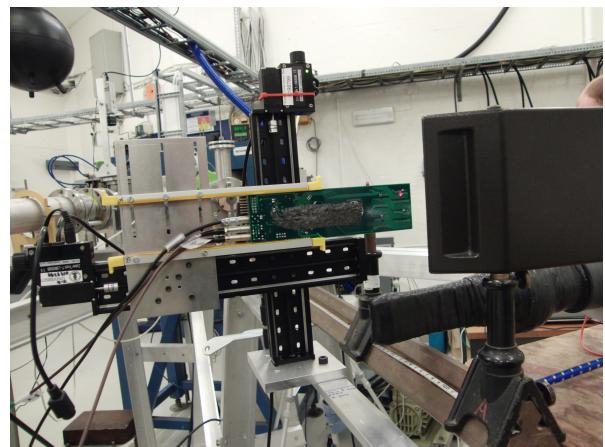
#### 4.5.3 X-Y-positioning System

The X-Y-positioning system is a displacement system where PCBs can be mounted and be moved up, down and sideways in a small area controlled by a computer. Communication is made through a serial port, and a LabVIEW program is used to control the system.

This was used when doing the beam profile as discussed in chapter 5.1.2. In figure 4.19 you can see a picture of the front and back of the X-Y-positioning system with the SRAM radiation detector mounted.



(a) X-Y-positioning system from behind



(b) X-Y-positioning system upfront

Figure 4.19: X-Y-positioning system upfront and behind stationed in OCL. The SRAM radiation detector is mounted

# Chapter 5

## Irradiation Test Setup

Irradiation tests for the RCU2 electronics were performed at two facilities: Oslo Cyclotron Laboratory (OCL) and The Svedberg Laboratory (TSL). This chapter will give a brief introduction to the two facilities, and explain the preparation process for each of the two.

The purpose of testing the RCU2 electronics for radiation is to see if the tested components are able to survive in a radiation hard environment as we will find in the TPC, see section 1.1. To test the limit for each of the components, the components was irradiated until an error was detected, current consumption drastically increased or the components received a much higher dose than were required without any error.

### 5.1 Irradiation on OCL

Oslo Cyclotron Laboratory is located at the Department of physics at the University of Oslo, and was opened in 1978. The cyclotron is of the type MC-35 and was made by Scanditronix AB from Sweden. This is the only accelerator in Norway for ionized particles used in basic research. The cyclotron can accelerate protons, deuteron,  $^3He$  and  $^4He$ , with energies and intensities as seen in the table 5.1 below. A drawing of the lab can be seen in figure 5.1. The laboratory is divided in three; the control room, the inner experimental hall and the outer experimental hall. The cyclotron is placed in the inner hall, and a beam is sent through pipes to the outer hall. There is vacuum inside the pipes and the cyclotron, so that the particle should not suffer energy loss from collision with air molecules. With magnets it is possible to regulate the beam to your desired pipe exit. There are also several cups put on the pipeline which makes it possible to block the beam. These can be used to stop the beam during an experiment, so that it is possible to go into the experimental area and do changes on the setup. When the cyclotron is running and the beam is on, you are not allowed to enter the inner experimental area.

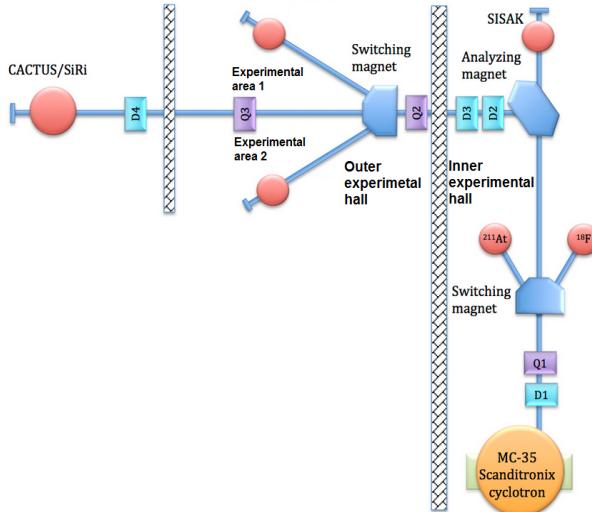


Figure 5.1: Layout of the beam area at OCL

Ionized beam particle type	Energy(MeV)	Intensity( $\mu\text{A}$ )
Proton	2-35	100
Deuteron	4-18	100
$^3\text{He}$	6-47	50
$^4\text{He}$	8-35	50

Table 5.1: Ionized beam particle data table

### 5.1.1 Experiment Setup and Equipment

The experiment setup was placed in the outer experimental hall in experimental area 2. The experimental setup as well as the equipment used can be found in the figure and table below. The equipment was kept in a height of 140-150cm. Beam exit was in a height of 141.5cm.

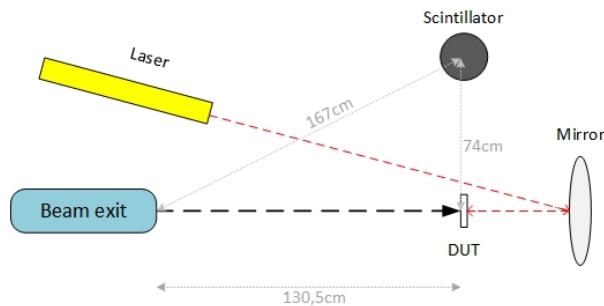


Figure 5.2: Experimental setup seen from above

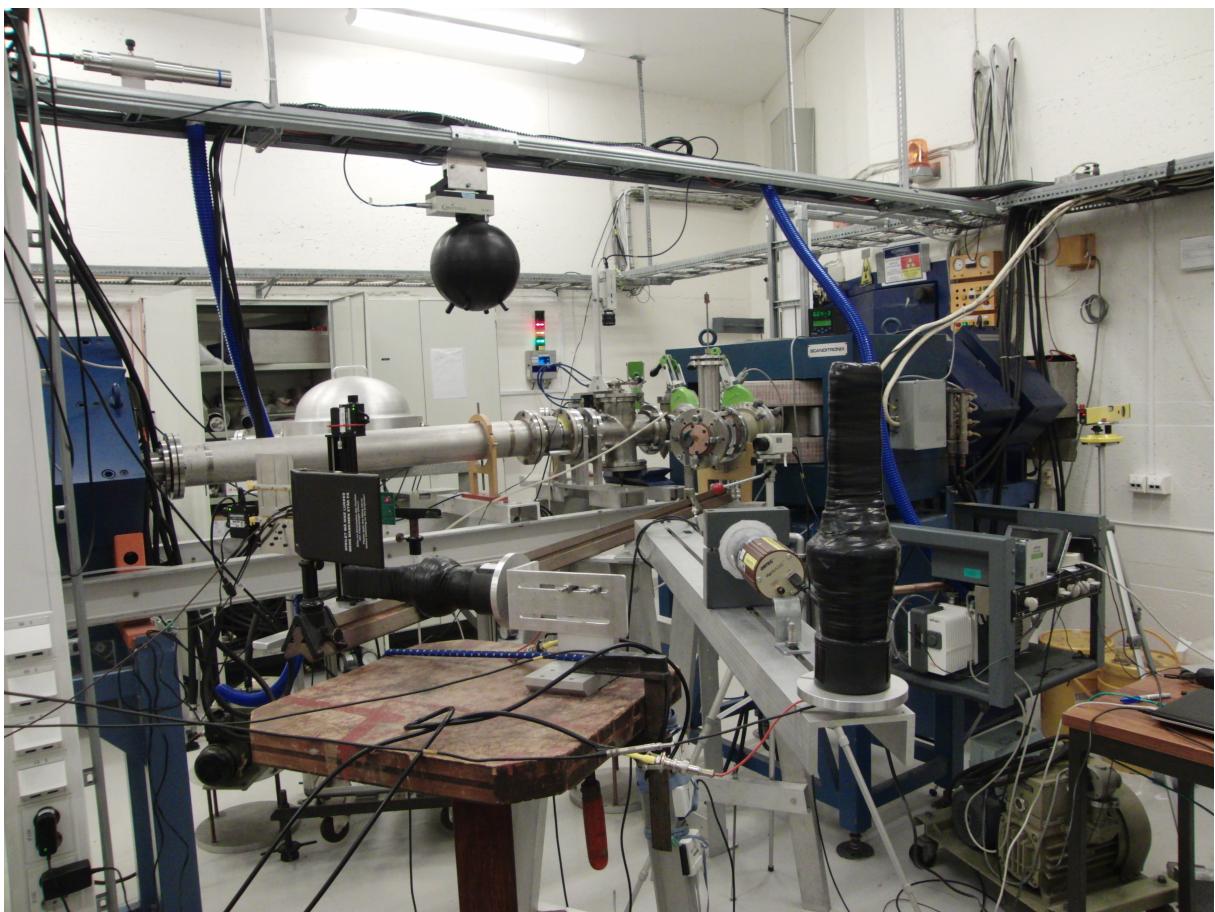


Figure 5.3: Picture of the experimental area

Equipment	Explanation
Scintillator	A plastic scintillator with photomultiplier. Was used to measure relative radiation. We had two of these, one that was placed directly under Device Under Test (DUT) and one that was placed 75cm away from DUT.
High voltage regulator	Voltage for the photomultiplier. 800V was used.
The test boards	TPS51200, MIC69302WU, SN74AVCB164245, SN74AVC2T245, QS3VH257, SY89831U, ADN2814, MAX3748, INA210, TLV3011 and SF2 starter-kit.
SRAM radiation detector	A PCB board with 4 SRAM cells that was used to characterize the beam and to measure scintillator counts
Computer	A VNC server was set up on a computer inside the experimental hall, which made it possible to control the experiment from the control room. The computer was running all the necessary software to control and monitor the experiment.
USB DAQ	Data acquisition board form National Instruments (NI). Used to establish analog and digital connection to the test boards and send data to the computer.
Radiation film	A film of the type <i>grafchromic</i> that reacts when irradiated. Used to identify the beam.
leveled laser	Was used to pinpoint the center of the beam.
XY-positioning system	Connected to the computer so that we could change the position of the test boards from a computer

Table 5.2: Equipment used in the experiment

### 5.1.2 Preparation and characterization of the beam

Before we could start with the radiation the radiation test, we had to start with characterization of the beam, and check that it hits around the area that we expected. This was done by using radiation films that turns black when exposed to radiation. One of these was placed directly in front of the beam exit and one in front of Device Under Test (DUT) area. This was done to see how the beam spread out, and to get a indication of where the beam center was. Afterwards a more precise calibration was performed by the use of the SRAM radiation detector and the scintillator. By measuring the relation between scintillator counts on the scintillator which was in a locked position and SEU on the SRAM that was connected to the XY-position system (which made the SRAM freely to move), we were able to find a more precise position of the beam center by observing which position gave us the highest number of SEUs compared to scintillator counts. When the beam center was found and everything worked as it should, the laser was placed in a position so that the laser beam pointed to where we had found center of the beam to be. Thereafter we could replace the SRAM board with the PCB that we were going to test. This had to be done every day at startup, before we could start the actual tests.

Test period	Tested boards
13.11.13 – 15.11.13	<i>TPS51200</i> <sub>1</sub> , <i>MIC69302WU</i> <sub>1</sub> , <i>SN74AVCB164245</i> <sub>1</sub> , <i>SN74AVC2T245</i> <sub>1</sub> , <i>QS3VH257</i> <sub>1</sub> and <i>SY89831U</i> <sub>1</sub>
28.11.13 – 29.11.13	<i>ADN2814</i> , <i>MAX3748</i> , <i>SY89831U</i> <sub>2</sub> , <i>TPS51200</i> <sub>2</sub> , <i>MIC69302WU</i> <sub>2</sub> , <i>SN74AVCB164245</i> <sub>2</sub> , <i>SN74AVC2T245</i> <sub>2</sub> and <i>QS3VH257</i> <sub>2</sub>
08.04.14 – 11.04.14	<i>INA210</i> <sub>1</sub> , <i>INA210</i> <sub>2</sub> , <i>TLV3011</i> <sub>1</sub> , <i>TLV3011</i> <sub>2</sub> and SF2 M2S050ES-T-FG896

Table 5.3: Overview of the tested components at OCL

We were able to control the intensity (Current) of the beam freely from the control room inside the limitation of the beam (for protons that is up to 100  $\mu\text{A}$ ), but we kept us in the area between 100 pA to a few nA. This way the radiation dose to the test boards could be controlled. If desirable the beam intensity could be measured by putting a Faraday Cup (FC) in front of the beam, which was connected to a high accuracy multimeter. But the FC had to be removed when tests were running, since it would block the beam.

We were running up to 3 LabVIEW programs through the experiment, one for controlling the XY-position system, one for the SRAM board (to measure SEU and scintillator counts when calibrating and to get scintillator counts during the tests) and one program for each of the test boards. The SRAM and test board programs were constantly saving data on the disk.

### 5.1.3 What was Tested at OCL

We had beam time in three periods at OCL; 13.11.13 – 15.11.13, 28.11.13 – 29.11.13 and 08.04.14 – 11.04.14. What were tested in the respectively periods, can be seen in Table 5.3.

## 5.2 Irradiation at The Svedberg Laboratory (TSL)

The main difference between OCL and TSL is that TSL is able to produce a beam of much higher energies. TSL is a much more professional facility, meaning that there are more people working there available for assistance, and there is no need for any calibration before starting a radiation test. We can simply show up and expose what we want to expose, and data, like fluence and exposed time, are given to use, making it easy for us to calculate the dose and flux.

TSL is an accelerator facility belonging to University of Uppsala in Sweden, [26]. It is mainly used for proton therapy on cancer patients by Uppsala University Hospital, but it is also used for medical research and radiation testing of electronics. The heart of the installation is a Gustav Werner cyclotron that delivers a beam of charged particles in energies up to 192 MeV. The particles that can be produced are everything from protons to highly charged xenon ions. There are several extraction points from the cyclotron, which are controlled from the *control room*. The beam can be lead out into the *blue hall*, which is the experiment area used for electronics testing. The Blue hall has two user areas; one for protons, and one for neutrons and heavier ions, see Figure 5.4.

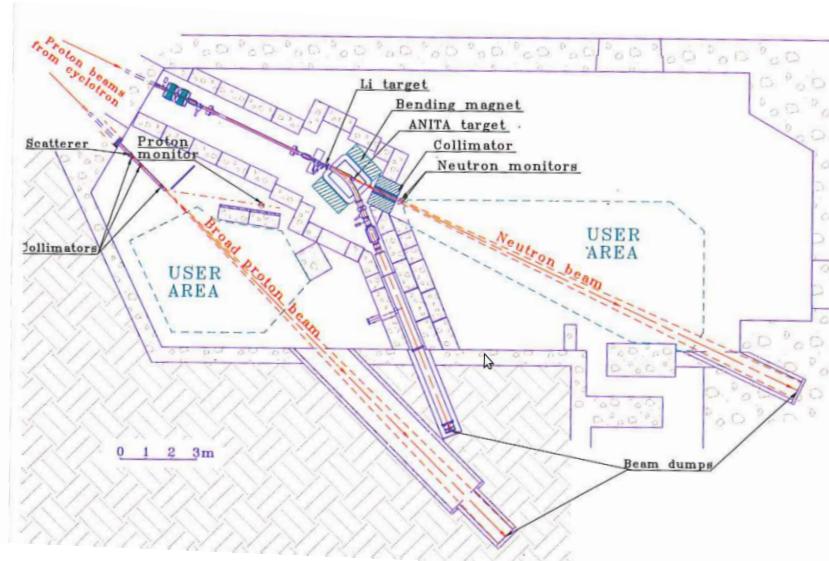


Figure 5.4: Layout of the Blue hall

### 5.2.1 Beam Setup Procedure

At TSL we didn't have to get a beam characterization as we did at OCL. In the Blue hall there is a permanently setup with detectors and a well-defined beam line. We only needed to set up the test equipment, put the test board at a given extraction point, and start the test. The center of the beam was found by lasers placed in locked positions around

the hall, one for horizontal direction and one for vertical direction. The head of the laser was movable, so we could point the laser beams towards our test board. A computer which was remotely controlled through network connection was placed in the hall. This computer was used as a connection point to our test boards. We sat in a room called *counting room*, where we could turn the beam on and off as we desired. There was also a machine in the counting room that was connected to detectors in the blue hall, telling us the fluence (number of protons per  $\text{cm}^2$  in total) and exposed time. The fluence can be used to calculate the flux and dose. The energy of the proton beam we got was 170 MeV.



Figure 5.5: Setup in the blue hall. The RCU2 is mounted, ready to be exposed for radiation

### 5.2.2 What were Tested at TSL

A week before we arrived at TSL, we got the first two prototypes of the RCU2. That means that we had limited time to make tests for all of the different parts of the board.

The focus of the visit to TSL was the SF2 SoC FPGA, but we also tested an optical receiver and an optical transceiver, which respectively are being used for TTC (timing, trigger and control) and for Detctor Data Link2 (DDL2). We brought with us two RCU2s and a total of 7 starter-kits, where 3 of these were with a smaller package of SF2 (M2S050-FG484), and the rest were engineering samples versions of M2S050-FG896, which is the one used on RCU2. For the tests as discussed in section 4.4, we only used the SF2 starter-kits, since the test only involves internal parts of the SF2 SoC FPGA. Two of the starter-kits with the smaller package (M2S050-FG484) were tested, and one with engineering sample (M2S050ES-T-FG896). When the RCU2 cards were exposed to radiation, things like detector data link2 (DDL2), TTC and PLL were tested, which will not be discussed

thoroughly in this work, but a short summary will be given. Current was measured on the SF2 starter-kits and the RCU2 boards when they were irradiated to check for latchup.

# Chapter 6

## Calculations and Results from Radiation Tests

*This chapter will explain how the collected data from radiation tests were used to calculate flux and dose, and results from radiation tests at OCL and TSL will be presented and discussed.*

After an irradiation test at OCL, the collected data consists of the exposed time, scintillator counts, current consumption and output data of the DUT. From beam setup before the radiation test, we found the relation between scintillator counts and SEU on the SRAM radiation detector. From earlier tests with the SRAM radiation detector the cross section for an incoming proton to induce a SEU is known. These data are used to calculate the received dose for each components. The next section will explain the calculation process.

### 6.1 Calculation of Dose

Two ways to calculate the dose will be discussed in this section; manually using LET, see section 3.2, and using simulations from a program named FLUKA. Which of these gives us the most reliable result will be discussed at the end of this section.

#### 6.1.1 Definitions

Absorbed radiation dose has the unit of energy/mass and the SI-unit is gray (Gy), which is 1 Joule of energy absorbed in a kilogram of matter [J/Kg], see equation 6.1. Another

unit often used when it comes to radiation of electronics is Rad, short for "Radiation absorbed dose". The relation between Rad and Gy can be seen in equation 6.2.

$$1\text{Gy} = 1 \frac{\text{J}}{\text{kg}} \quad (6.1)$$

$$1\text{Rad} = 0.01\text{Gy} = 0.01 \frac{\text{J}}{\text{kg}} = 10^{-5} \frac{\text{J}}{\text{g}} \quad (6.2)$$

The particle energy is normally expressed in electronvolt (eV) or Megaelectronvolt (MeV). One electronvolt is defined as the amount of kinetic energy gained by a single unbound electron when it accelerates through an electric potential of one Volt, thereof eV. Its value is  $e = 1.602 \times 10^{-19}\text{C}$  which is the electric charge, multiplied with one Volt, which equals  $1.602 \times 10^{-19}\text{J}$ .

$$1\text{MeV} = 10^6\text{eV} = 10^6 \cdot 1.602 \times 10^{-19}\text{J} = 1.602 \times 10^{-13}\text{J} \quad (6.3)$$

### 6.1.2 Calculating Dose Using LET

As explained in subsection 3.2.2, LET is energy deposited in a material through ionization when a particle crosses the material. LET is equal to the energy loss a particle suffer by crossing a material, which means that we can use the Bethe Bloch formula that is expressed in equation 3.1. By looking at total LET for an component while knowing the fluence, the dose can be calculated, see Equation 6.13. The energy loss of a particle is highly energy dependent, but for short distances it can be assumed to be constant without getting any noticeable error.

Two energies were used when exposing components at OCL. The first time a proton beam with an energy of 28 MeV, and the two other times a beam of 25 MeV. DUT was placed 130 cm away from beam exit, which means that the protons would suffer some energy loss in the air between beam-exit and DUT. To make the work easier for us, an energy loss calculator program [27] was used to calculate the *energy loss* for a 28 MeV and a 25 MeV proton beam in air, we got respectively  $17.52 \frac{\text{MeVcm}^2}{\text{g}}$  and  $19.2 \frac{\text{MeVcm}^2}{\text{g}}$ . By multiplying with the density of air which is  $\rho_{air} = 1.275 \frac{\text{mg}}{\text{cm}^3}$ , we got  $22.3 \frac{\text{keV}}{\text{cm}}$  and  $24.5 \frac{\text{keV}}{\text{cm}}$ . This means that the energy of the protons when they collide into DUT is:

$$E_{proton1} = 28 - (130\text{cm} \times 22.3 \frac{\text{keV}}{\text{cm}}) \approx 25\text{MeV} \quad (6.4)$$

$$E_{proton2} = 25 - (130\text{cm} \times 24.5 \frac{\text{keV}}{\text{cm}}) \approx 22\text{MeV} \quad (6.5)$$

By using the same energy loss calculator we find find that the energy loss in silicon (which is the main component in integrated circuit), to be:

$$-\frac{dE}{dx}(25\text{MeV}) = 17.1 \frac{\text{MeV}\text{cm}^2}{\text{g}} \quad (6.6)$$

$$-\frac{dE}{dx}(22\text{MeV}) = 18.9 \frac{\text{MeV}\text{cm}^2}{\text{g}} \quad (6.7)$$

Looking into a single proton entering a silicon material, the energy deposited by that single proton can be expressed as;

$$\Delta E_{proton} = -\frac{dE}{dx} \cdot \Delta x \cdot \rho_{Si} = [\text{MeV}] \quad (6.8)$$

where  $\Delta x$  is the length segment a proton particle penetrates into the material, and  $\rho_{Si}$  is the density of silicon.

$$\rho_{Si} = 2.33 \frac{\text{g}}{\text{cm}^3} \quad (6.9)$$

To determine the total energy deposited in the component, we have to multiply the energy of a single proton with the fluence and the area of the component. Fluence is the total flux over a given time, expressed in  $[\frac{n}{\text{cm}^2}]$ , where n is number of protons. The total energy is then:

$$\Delta E_{total} = \Delta E_{proton} \cdot fluence \cdot A_{Si} = -\frac{dE}{dx} \cdot \Delta x \cdot \rho_{Si} \cdot fluence \cdot A_{Si} = [\text{MeV}] \quad (6.10)$$

Now we know the total energy depleted in an component by a proton beam , and can start calculating the dose. Dose is energy per mass, as explained in section 6.1.1. Meaning that the absorbed dose in silicon can be expressed as,

$$Dose(Si) = \frac{-\frac{dE}{dx} \cdot \Delta x \cdot \rho_{Si} \cdot \Phi \cdot A_{Si}}{m_{Si}} = \left[ \frac{\text{MeV}}{\text{g}} \right] \quad (6.11)$$

where  $m_{Si}$  is the mass of silicon.

$m_{Si}$  can be expressed in terms of silicon density, see equation 6.9, multiplied with the volume ( $V_{Si}$ ), which is Area ( $A_{Si}$ ) times thickness ( $d_{Si}$ ). Assuming that the protons enter the silicon in a straight line, the path segment  $\Delta x$  is equal the thickness, which then gives us:

$$Dose(Si) = \frac{-\frac{dE}{dx} \cdot \Delta x \cdot \rho_{Si} \cdot \Phi \cdot A_{Si}}{\rho_{Si} \cdot A_{Si} \cdot d_{Si}} = -\frac{dE}{dx} \cdot fluence = \left[ \frac{\text{MeV}}{g} \right] \quad (6.12)$$

To determine the dose in Rad instead of  $\frac{\text{MeV}}{g}$ , we multiply with the converting factor given in equation 6.3 and divide by the factor given in equation 6.2. This gives us:

$$Dose(Si) = 1.602 \cdot 10^{-8} \cdot -\frac{dE}{dx} \cdot fluence = [\text{Rad}] \quad (6.13)$$

### 6.1.3 Calculating Dose Using FLUKA Simulations

The FLUKA Monte Carlo code is a well benchmarked general purpose tool for calculations of particle transport and interactions with matter, covering an extended range of applications like for example proton and electron accelerator shielding, target design, calorimetry, activation and dosimetry, cosmic ray studies, and radiotherapy. It can simulate with high accuracy the interaction and propagation in matter of about 60 different particles, including photons and electrons from 1 keV to thousands of TeV, neutrinos, muons of any energy, and hadrons of energies up to 20 TeV [28].

We simulated a proton beam with energy of 28 MeV and 25 MeV in air, and set our DUT-position 130 cm away from beam exit. The results can be seen in table 6.1.

Energy at beam exit	28 MeV	25 MeV
Dose/primary particle at DUT[Gy]	4.08E-10	2.94E-10
Primary particles at Beam exit	1	1
Primary particles at DUT	0.1331	0.0857
Beam intensity reduction at DUT	7.51	11.67

Table 6.1: FLUKA simulation with 28MeV proton beam

As mentioned in the introduction to this chapter, the known values after a radiation test are exposed time, scintillator counts, current consumption, output data of the DUT and cross section from the SRAM radiation detector.

The procedure to calculate the dose starts with finding the total fluence. This is found by first converting from scintillator counts to SEU, by multiplying with the converting factor as found in beam setup. And then divide on the cross section, which is known for the SRAM radiation detector, see subsection 4.4.1. Fluence can then be found as seen in equation 6.14 and the flux as in equation 6.15.

$$Fluence_{DUT} = \frac{SEU}{CS} = \left[ \frac{n}{cm^2} \right] \quad (6.14)$$

$$Flux = \frac{Fluence}{time} = \left[ \frac{n}{cm^2} \right] \quad (6.15)$$

The FLUKA simulation results tells us how many protons will collide into DUT for each proton coming out from beam exit, and what dose this will contribute to at DUT. By using the calculated Fluence for DUT, found by equation 6.14, we can find the fluence at beam exit by dividing on *primary particles at DUT* from the simulation results, see equation 6.16. Then we can use *dose per primary particle at DUT* from the result and multiply with the Fluence at beam exit, which gives us the dose in gray for the DUT, see equation 6.17. By multiplying by 100 we get the dose in Rad.

$$Fluence_{BE} = \frac{fluence_{DUT}}{primaryparticles_{DUT}} = \left[ \frac{n}{cm^2} \right] \quad (6.16)$$

$$Dose_{DUT} = Fluence_{BE} \cdot \frac{Dose}{primaryparticle_{DUT}} = [Gy] \quad (6.17)$$

#### 6.1.4 Comparison of LET and FLUKA Calculations

The results from radiation of MAX3748 can be used to compare LET calculation with FLUKA, the test results can be found in Table 6.2. Both methods to calculate dose require the fluence. The fluence is given by SEU on SRAM, and cross section, see Equation 6.14, and SEU on SRAM are given by the conversion factor found in beam setup and scintillator counts. For MAX3748 the fluence is:

$$Fluence_{MAX3748} = \frac{2698510 \cdot 0.473}{1.14 \cdot 10^{-6}} = 1.12 \cdot 10^{12} \frac{n}{cm^2} \quad (6.18)$$

To calculate the dose using LET, we follow the steps given in subsection 6.1.2. Starting by calculating the energy when entering the component 130 cm away from beam exit. This

time	2472 s
proton energy Beam exit	25 MeV
scintillator counts	2698510
scintillator counts to SEU SRAM	0.473
Cross section	$1.14E - 6 \frac{cm^2}{device}$

Table 6.2: Results after radiation of MAX3748

is found in equation 6.4 to be 22 MeV. LET, or energy loss, for a 22 MeV proton particle in silicon, is calculated in equation 6.5 to be 17.1 MeV.

Fluence is found in equation 6.18. By using Equation 6.13 we find the total dose in Rad to be:

$$Dose(Si) = 1.602 \cdot 10^{-8} \cdot 17.1 \cdot 1.12 \cdot 10^{12} = 306.8 kRad \quad (6.19)$$

Calculation using FLUKA simulation is an easy process, starting by calculating the fluence at Beam exit, from equation 6.16, and then using that value to calculate the dose as seen in Equation 6.17.

$$FluenceBE = \frac{1.29 \cdot 10^{12}}{0.0857} = 1.51 \cdot 10^{13} \frac{n}{cm^2} \quad (6.20)$$

$$DoseDUT = 1.51 \cdot 10^{13} \cdot 2.94 \cdot 10^{-10} = 4425.4 Gy = 383.8 kRad \quad (6.21)$$

It can be seen that finding the dose using FLUKA simulation gives approximately 20 % higher dose than by using LET. Why we have this difference will be discussed.

When calculating LET for a given component we calculated with constant energy drop through the air before colliding with the component and through the component. In reality energy loss will increase as the energy decreases. This means that the calculated dose is lower than the actual dose.

When using LET to calculate the dose, we get a small error from approximations and assumptions. But since we know about these, we also know that the energy should be a little higher than the calculated value, and can be sure that the calculated dose is at least not higher than the actual dose. The FLUKA simulations are using advance models for the calculations, which makes the results very accurate.

Other than the calculation method, there may also be other sources of errors, like that the energy level of the proton beam (it may differ from 28/25 MeV which it is said to

be), the conversion factor found in the beam setup and unlinearity between scintillator counts and SEU on SRAM. Which means that if the calculation method is precise, we will still get errors due to other error sources. We are nevertheless mainly interested in getting a total dose which is more than the total dose it will receive in the ALICE TPC. That means that the accuracy isn't that important as long as it is over this level with a safety margin. That means that both of the methods are good enough.

At OCL, FLUKA simulation was used to calculate the dose, and at TSL, LET was used to calculate the dose.

## 6.2 Results from OCL

### 6.2.1 Calibration process

As explained in chapter 5.1.2, we had to start by finding the center of the beam. The laser was first placed in a position pointing at what was thought to be center. Then we placed a radiation film in front of the beam exit and at DUT area. By observing how the radiation films reacted to radiation, we got a indication of where the center of the beam was. An example of two films from the beam exit and DUT area can be seen in figure 6.1.

Now we had an indication of where center was compared to where the laser was pointing. The SRAM radiation detector was mounted in the XY-positioning system and placed so that the laser was pointing at one of the SRAM chips. This position was defined as position zero  $(x,y) = (0,0)$ , and from the radiation films we knew approximately how much the SRAM radiation detector had to be moved in order to be in the center of the beam. In Table 6.3 you find the results from calibration 14.11.2013. Position  $x = -1.5$  cm and  $y = 0$  cm gives highest relation between SEU and scintillator counts, and the laser was moved so that it points to this position. Two tests were performed in that position and the average value gives us 1.0948. A graph showing us relation between SEU on SRAM and scintillator counts for the different x and y position can be seen in Figure 6.2. The graph tells us also something about the thickness of the beam at DUT position. Beam setup data from all other days at OCL can be found in appendix A.1.

When we irradiated the different PCBs, we only measured scintillator counts, as a indication of the beam intensity. When we were finished exposing a component, the relation value was used to convert from scintillator counts to SEUs. Then fluence could then be calculated since the cross section for a proton inducing a SEU on the SRAM is known. Cross section for the SRAM radiation detector can be found from [20] and is given in Equation 6.22.

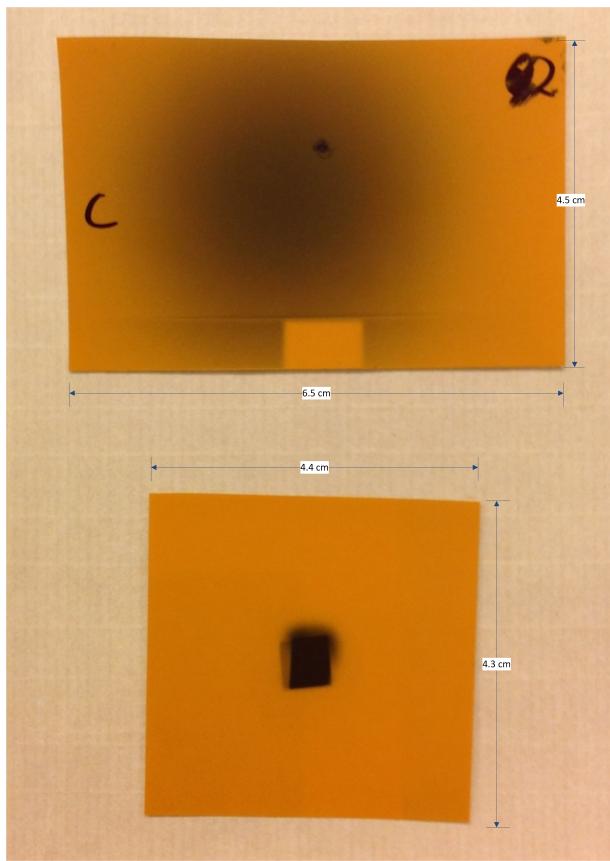


Figure 6.1: Example of radiation films after radiation, DUT area (top) and bream exit (bottom). The laser beam position is marked with a black dot.

Calibration test nr.:	x[cm]	y[cm]	Scint count	SEU(SRAM)	SEU/scint count
1	0	0	23813	1971	8.28E-02
2	0	-0.5	37930	3867	1.02E-01
3	0	-1	27527	2817	1.02E-01
4	0	-1.5	34413	3360	9.76E-02
5	0	-2	32713	2763	8.45E-02
6	0.5	0	38753	2709	6.99E-02
7	-0.5	0	23420	2483	1.06E-01
8	-1	0	20611	2232	1.08E-01
9	-1.5	0	21014	2410	1.15E-01
10	-1.5	0	20676	2260	1.09E-01
11	-2	0	35787	3776	1.06E-01
12	-2.5	0	27847	2512	9.02E-02

Table 6.3: Calibration tests 14.11.2013

$$CS = 1.14 \cdot 10^{-6} \frac{cm^2}{device} \quad (6.22)$$

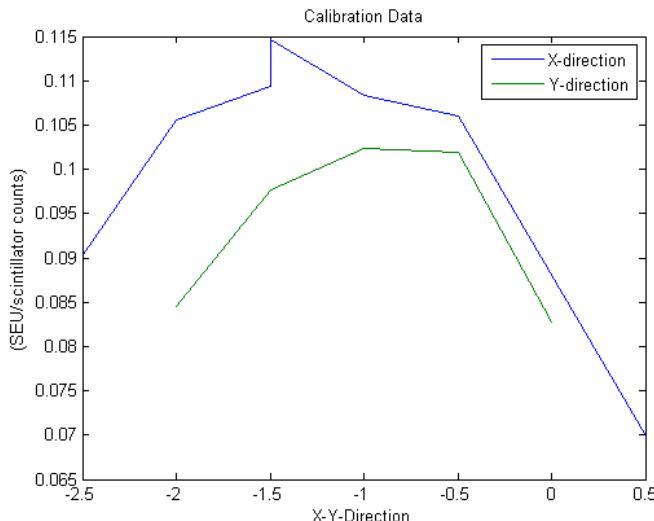


Figure 6.2: Calibration data from 14.11.2013

### 6.2.2 Test Results of the PCBs

In this section the the radiation test results from OCL will be presented and discussed. Tests of all the PCBs will be presented, followed by a discussion at the end. The results are presented after type, meaning that two PCBs containing the same component will be presented together. The purpose of these tests have been to check for radiation tolerance, and the focus has therefore been to check for long therm effects like current consumption

and output voltage as function of the accumulated dose. For the components where the output errors were counted (single event effects), we have plotted output errors as function of fluence, this counts for test of ADN2814 and MAX3748.

An overview of the tests can be found at the end of this section, with the total exposed time, the total accumulated dose and error status. For information regarding flux for the different tests, see Appendix A.2 Figure A.4, A.5 and A.6

### 6.2.2.1 TPS51200 - Voltage Regulator

TPS51200 was the first component that was tested for radiation. We started therefore with a very low intensity on the beam to be sure that everything worked as it should. The intensity was increased in the following tests. Two PCBs of this type were supposed to be tested, but only one of these worked when we were at OCL.

Figure 6.3 shows the input current and output voltage versus the received dose in kRad. The total exposed time and dose for this board were respectively 34 min and 42.8 kRad, and it still worked with only small increase in current and decrease in voltage.

A small increase in voltage and decrease in current can be seen already after 5 kRad, the reason for this effect could be increased resistance in the component caused by radiation. The reduction/increase is nevertheless quite small, and would not harm if it should happen in a real design.

After 25 kRad, the current started to increase and voltage decreased, this is a more expected effect to radiation, which was discussed in subsubsection 3.4.2.1. The cause may be threshold decrease or current leakage in the internal transistors.

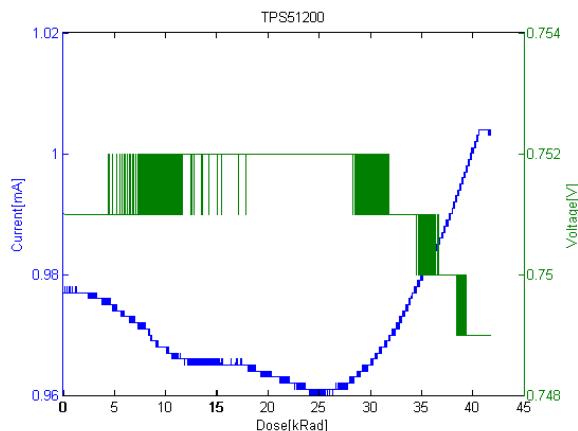


Figure 6.3: TPS51200 - Current/Voltage vs Dose

### 6.2.2.2 MIC69302WU - Voltage Regulator

For this component we also had the effect with a increase in voltage and decrease in current (see Figure 6.4). The reason for this is presumed to be the same as for the test with TPS51200 that the resistance in the component is increasing.

For both of our test we also detect some glitching on both the current and voltage. Maybe this is caused by change of threshold in internal transistors resulting in current leakage, and a feedback loop is trying to compensate, resulting in a small period of unstable current and voltage.

The current decreased to about the half for the first test and to about three quarters on the second test, but that were with a dose of 160 kRad and 380 kRad respectively, which is way more than the radiation level in the TPC. The output voltage is stable, there were an increase of approximately 2% on both of the tests, which is tolerable.

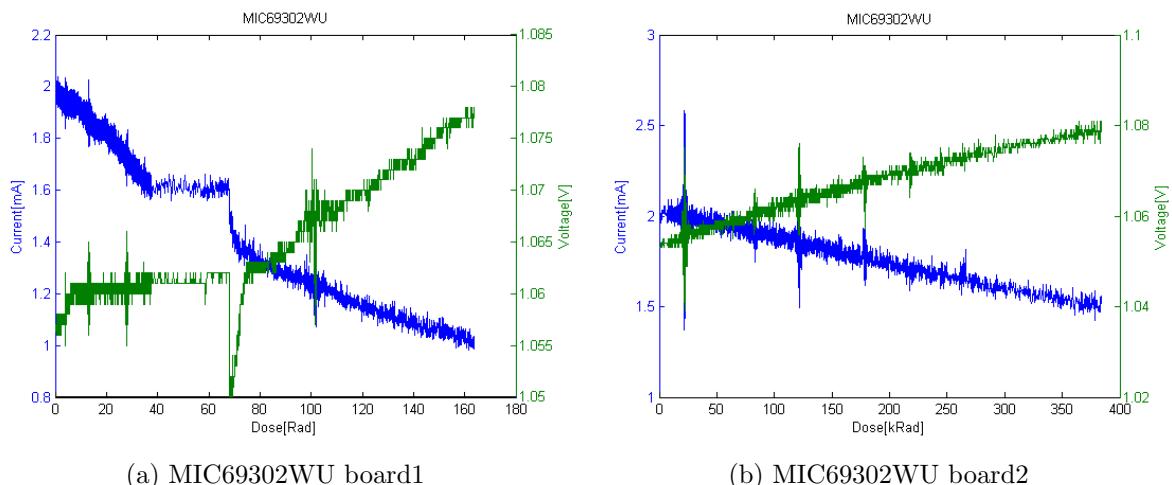


Figure 6.4: MIC69302WU - Current/Voltage vs Dose

### 6.2.2.3 SN74AVCB164245 - Bus Transceiver

For the radiation test of the two test boards for SN74AVCB164245 we detected no errors on the output data. Current as a function of dose for the two test boards can be seen in Figure 6.5. The current characteristic for the two test boards seems alike. The only difference is that the second board was exposed to a much higher dose, therefore we can see a much more increase in current. The reason for the regularly increase and decrease in current is that the output is constantly changing back and forth from on to off, with a gap of 4 seconds. No radiation effects are detected until a dose of approximately 40 kRad, where the current started slowly to increase.

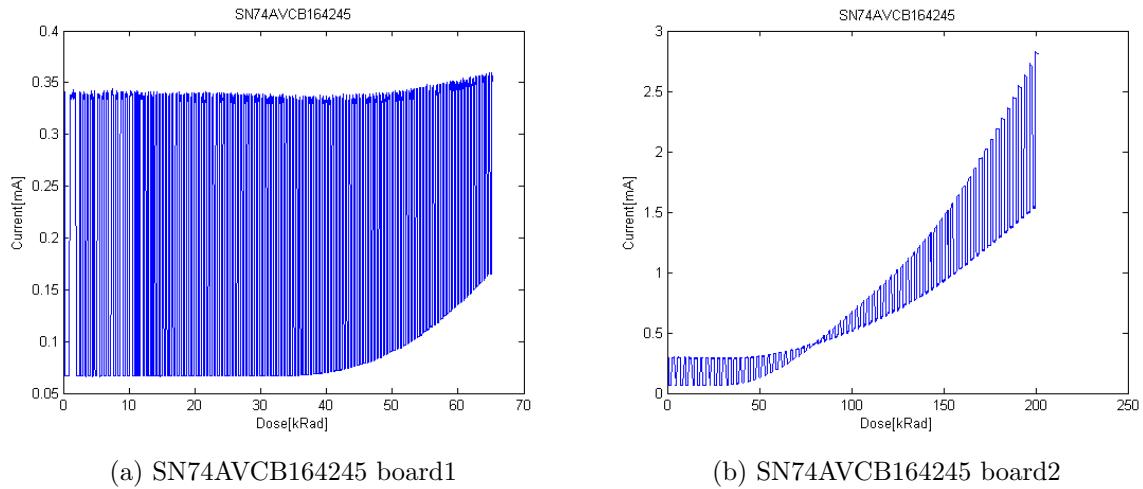


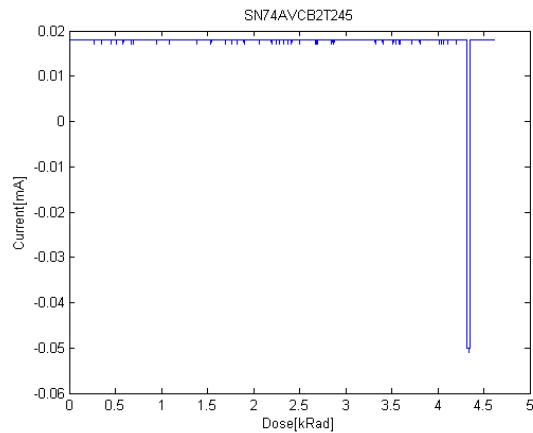
Figure 6.5: SN74AVC2T245 - Current vs Dose

#### 6.2.2.4 SN74AVC2T245 - Bus Transceiver

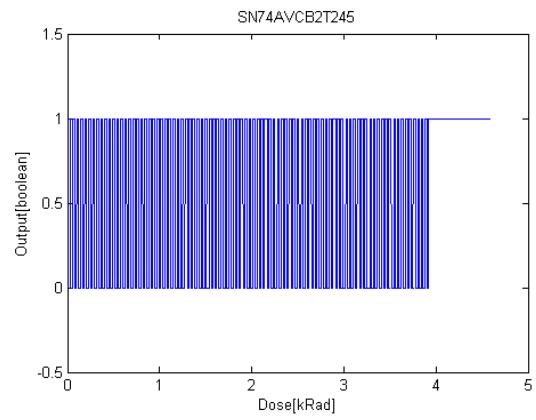
On the radiation of the first of the two test boards of SN74AVC2T245, we got an error on the output data. After about 740 s and a dose of approximately 4 kRad the outputs got stuck at '1', this can be seen in Figure 6.6b. We also see a different characteristic on the current as function of dose graphs for test board 1 and 2, see Figure 6.6a and 6.7. The input data is changing every 4 seconds, which means that we should have a constantly change in current consumption, as we see in Figure 6.7. This suggest that the test on the first board didn't go as it should from the start. This could be due to damage during the soldering process to the PCB.

The test result from board 2, shows that the current goes unchanged up to a dose of 40 kRad, and no errors were detected.

If the radiation results for board 2 is compared to the tests results of SN74AVCB164245, which is basically the same chip only with more input and output signals. We find more or less equal current characteristic, which supports the test results.



(a) SN74AVC2T245 Current vs dose



(b) SN74AVC2T245 Digital output data vs Dose

Figure 6.6: SN74AVC2T245 test board1

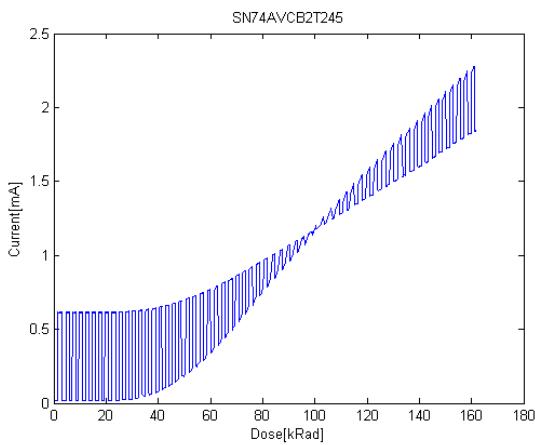


Figure 6.7: Current vs dose for SN74AVC2T245 test board2

### 6.2.2.5 QS3VH257 - Multiplexer/Demultiplexer

For both of the test boards for QS3VH257, no errors were detected on the output data through the entire irradiation test. Current as a function of dose for the two test boards can be seen in Figure 6.8. The behavior to radiation seems quite alike, the only difference is that the second test board was exposed to a much higher dose and therefore we can see a higher increase in current.

For both of the test boards, the current starts increasing after a dose of approximately 40 kRad. For board 2 the current increased to almost 9 times the starting current after it had received a dose of 110 kRad, but until a dose of 40 kRad we didn't detect any effects to radiation on the two test boards.

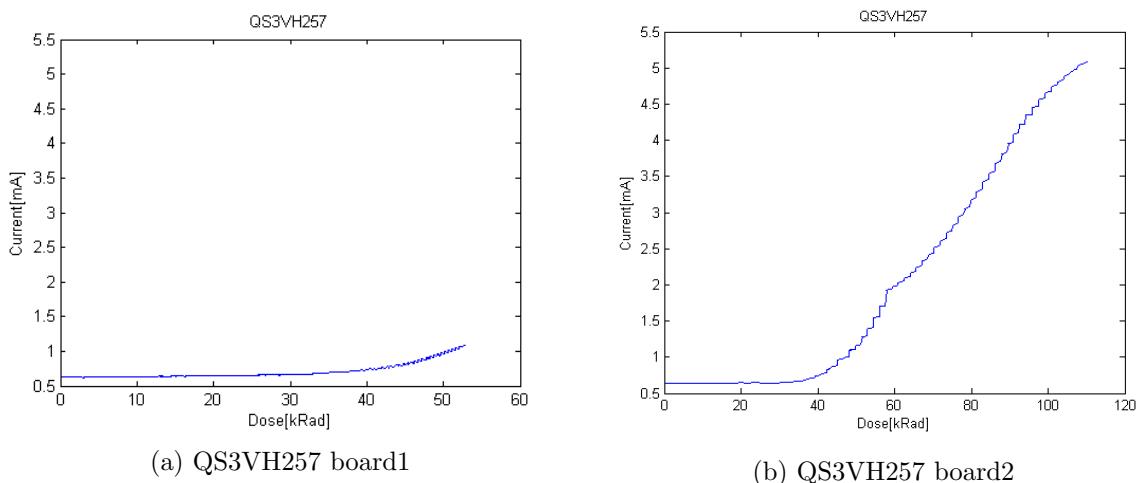


Figure 6.8: QS3VH257 - Current vs Dose

### 6.2.2.6 SY89831 - 1 to 4 fan-out Buffer

No errors were detected on the output data through both of the radiation tests for SY89831. Graphs of current as function of dose for the two test boards can be seen in Figure 6.9. Also here a difference in current characteristic can be seen. The two test boards should be equal, so the difference is probably caused by internal differences in the component, maybe caused by rough treatment during soldering. The current level is in the same magnitude, and we got no errors on the output data for both of the tests.

A total of 90 and 160 kRad was exposed to the two test boards without detecting any error and with only small increase in current for test board 2.

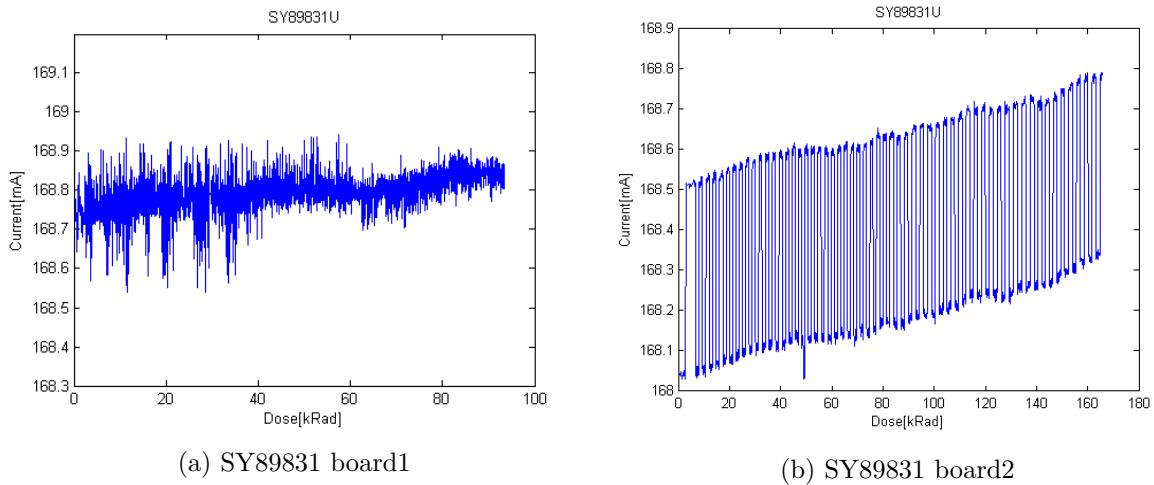


Figure 6.9: SY89831 - Current vs Dose

#### 6.2.2.7 ADN2814 - Limiting Amplifier

For the test of ADN2814, we didn't detect any current change until a dose of 270 kRad, see Figure 6.10, but unfortunately we got allot of output errors, see Figure 6.11. The first errors occurred after a dose of 11 kRad for the clock signal, and after a dose of 8 kRad for the data signal. After these errors the errors starting coming more regularly.

If we look at the clock and data output as function of time, which can be found in appendix A.2 figure A.1, we see that after the beam stops after 3600 seconds, the errors stopped increasing, this means that the errors on clock and data are directly effected by the radiation.

The errors tells us that either the signal is incorrect or the timing is incorrect. For the RCU2 design it is critically that that the timing is correct for both the clock and data. The clock signal is the clock signal controlling the readout from the readout pads, which should be synchronized with all of the RCU2s. The data signal is used to decide when to do measurement and when to send the acquired data out from the RCU2. It is therefore quite important that the timing is correct. If the clock or data is incorrect, then we may lose useful data in that period.

It can be discussed if the effect we see is a single event effect or accumulative effects. What we know is that we have a short period without errors before we start getting errors with an increasing rate. The short period without errors in the beginning indicates that the error we see is more accumulative effect, where the output data are getting worse and worse, maybe cause by increasing noise or skew or decrease in the voltage of the output signals. The fact that we in periods can see a almost linear increase with the increasing dose, points towards that the error we see is a more like a single event effects. We have also a stop in counter values after the beam was turned off, this also suggest that what we see is single event effects.

If this chip is going to be used, more test should preferable be done, which have more focus on what is happening with the output signal. Maybe small samples of the clock and data signal should be taken as the radiated dose increases, so the output signal can be properly be examined.

We could also calculate cross section for these errors, but it wouldn't tell us anything useful. Since we don't have any linear increase with the radiated dose, the cross section would only give us a imprecise calculation, which is only applicable for the same fluence.

The current graph, as seen in Figure 6.10 is varying quite a lot in current, typically variation in the beginning is 130 to 136 mA. This may be caused by large variation in the input signal, and production of two differential output signals with very high frequency (160 Mhz for the clock, and a little less for the data). More capacitors on the supply voltage could probably help to reduce this variations.

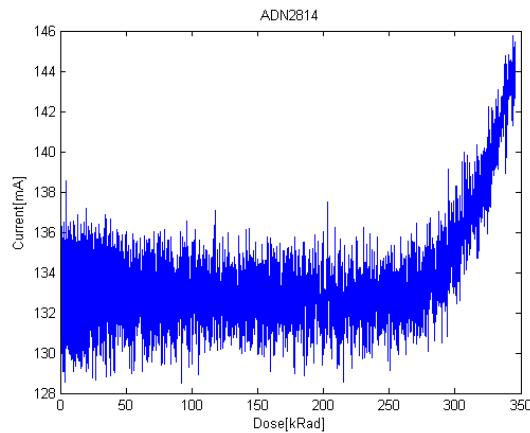


Figure 6.10: ADN2814 - Current vs Dose

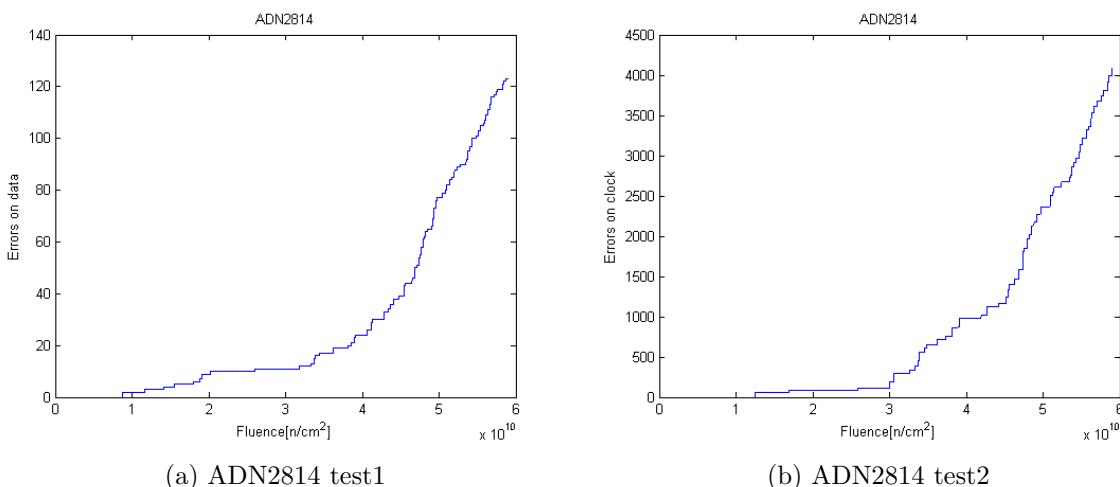


Figure 6.11: ADN2814 - Relative errors vs Dose

### 6.2.2.8 MAX3748 - Limiting Amplifier

The test board for MAX3748 was exposed to a dose of over 400 kRad. We can also detect a large variation in current consumption, see Figure 6.12. I presume that the reason is in the same manner as for the ADN2814 test board. That the large variations on the input signal, causing current consumption to vary depending on the state of the input signal. More capacitors on the supply voltage could also be a solution here to help reduce this variations.

Through this test we detected no errors on the output data, and the current consumption seems rather stable through the entire irradiation process, if not taken the large variation into account.

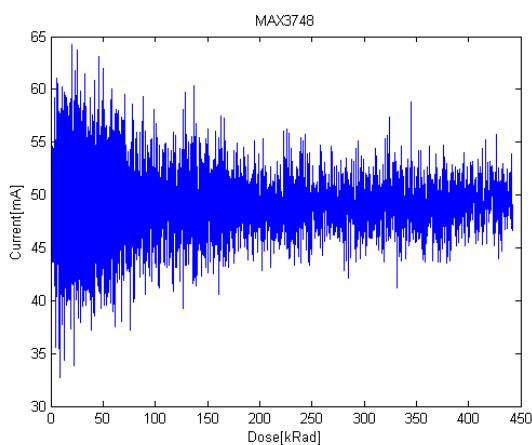


Figure 6.12: MAX3748 - Current vs Dose

### 6.2.2.9 INA210 - Current Shunt Monitor

In Figure 6.13 we find graphs of current and voltage as function of dose for the two test boards for INA210. A different reaction to radiation can be seen for the two boards. On the first board the output voltage increase and on the second board the output voltage decreased. This is quite strange, since the two boards should be exactly alike. Maybe the diode located on the input to the component got effected by the radiation on one of the two test boards, increasing or decreasing the measured current. It may also just be process variation. The current characteristic as function of dose are quite alike, the only difference is that on the second test board the current starts to increase a little earlier.

For test board 1 the current and voltage starts to rise after a dose of approximately 80 kRad. For the second test board we see a small increase in current already after 20 kRad, but the voltage stays stable until a dose of 100 kRad.

The increase we see on the output voltage from start to the peak on test board 1

contribute to a input current increase of  $2.85 \text{ mA}$  ( $\frac{0.352 - 0.295}{200} / 0.1 = 2.85\text{mA}$ ). Compared to the starting input current of  $14.75 \text{ mA}$  this contributes to a increase of  $19 \%$ . The cause of this effect could be offset variation on the output voltage, change in the internal amplification or a increase in current on the measured input signal. If its only a offset on the output, the small increase will probably not matter when we have a larger current to measure, but if its the internal amplification which are changing, this could be a problem when the current on the input is larger. The effect happens anyway after a very high dose, and wouldn't be a problem in the TPC.

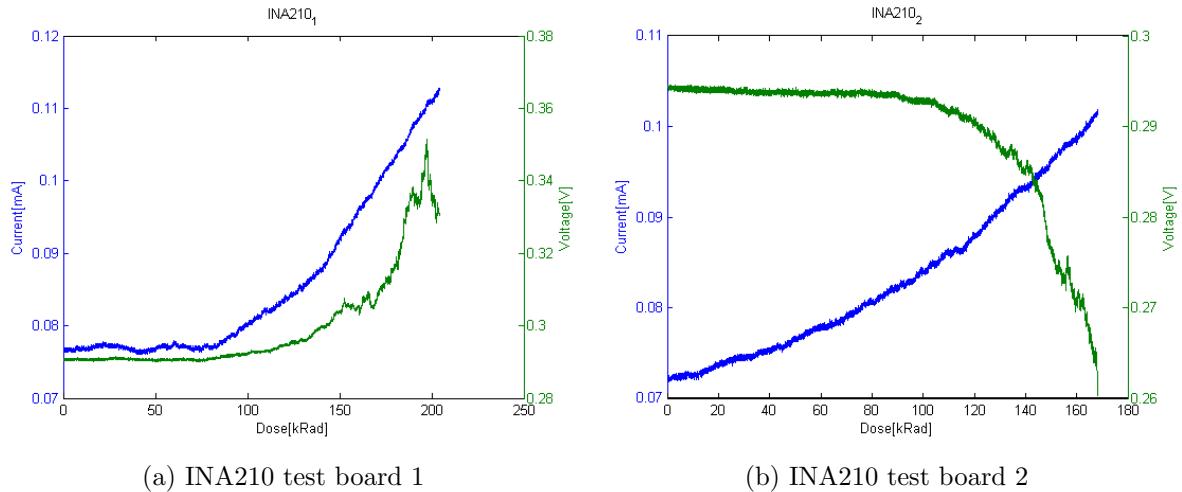


Figure 6.13: INA210 - Current and output voltage vs Dose

### 6.2.2.10 TLV3011 - Comparator

The result after radiation of the two test board for TLV3011 can be seen in the graphs in Figure 6.14 and 6.15. The graphs goes up and down because the input signal is changing every 4 seconds.

The first test board was exposed to a total dose of  $110 \text{ kRad}$ , after a dose of approximately  $85 \text{ kRad}$  the output voltage high value changed from  $3.2 \text{ V}$  to  $2.3 \text{ V}$ , and we saw a major increase in current. The period until  $85 \text{ kRad}$  we detected only a small increase in current and small decrease in output voltage, but the changes was so small that it wouldn't matter if it should happen in a PCB design.

In the area right before  $20 \text{ kRad}$ , the output voltage seems to stay high for a longer time. That is not the case, the reason for this effect is a sudden increase in intensity of the beam, see Figure A.6. Graphs of current and voltage as function of time can be seen in appendix A.2 Figure A.7, showing that the current and voltage stays stable.

The second test board was exposed to a dose of  $138 \text{ kRad}$ , The output voltage was stable until a dose of  $95 \text{ kRad}$ , but then the output voltage got stuck at high value. This could be caused by a change of the internal reference voltage, a offset on the input signal

or a stuck at error at the output. Through the entire radiation test, we detect only a small increase in current of about 0.15 mA.

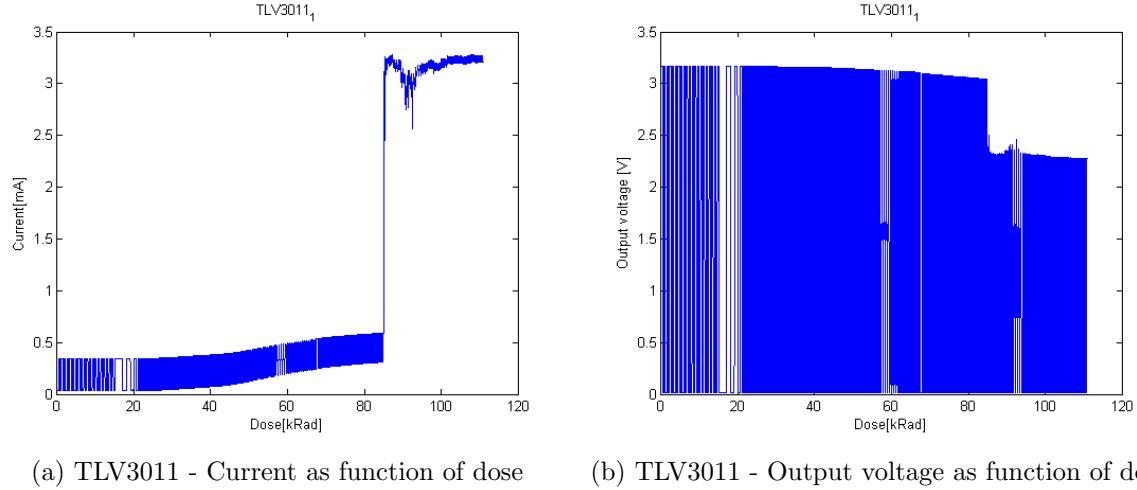


Figure 6.14: TLV3011 - Test board 1

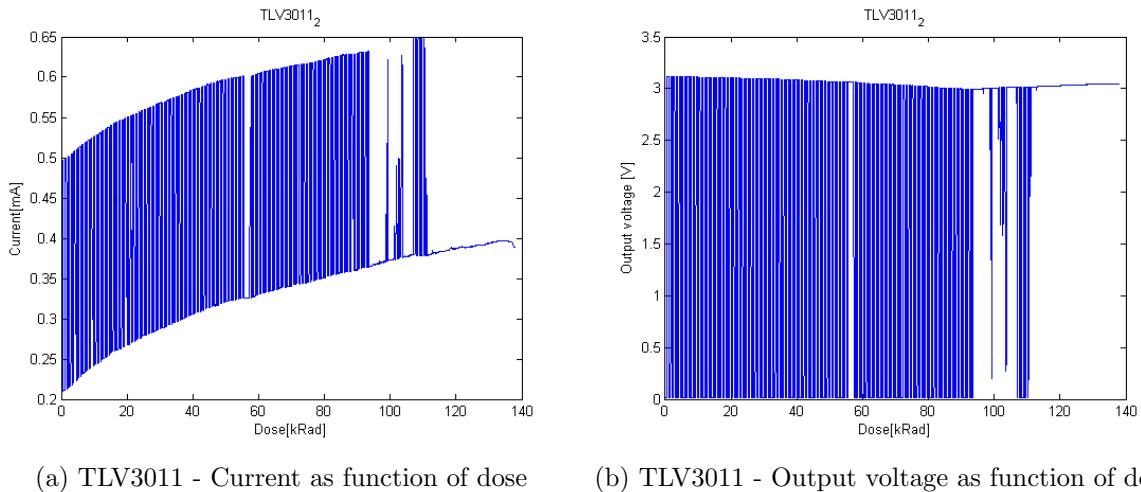


Figure 6.15: TLV3011 - Test board 2

### 6.2.2.11 Summary of the Results

In Table 6.4, 6.5 and 6.6 shows how long each components has been exposed to radiation, the dose and fluence they have received and if error(s) occurred during the irradiation. A returning effect from irradiation was that the current consumption started to increase in line with the increasing received dose. The exception was TPS51200 and MIC69302WU which both had a small decrease in current as the output voltage increased. This was probably caused by increase of the internal resistance for the components caused by the radiation.

We has some problems with some of the components tested, this could be due to rough treatment when soldering. Some of the components didn't have any leads, which means

that the entire component had to be heated to be able to solder the pads beneath them, since the heat can go up to several hundred degrees, it may cause some damage on the chip. That is part of the reason why we tried to at least have two boards which was tested, to ensure at least one successful test.

A challenge when we exposed the test boards, is that the proton beam didn't seem to be as stable, this can be seen from the flux graphs in Figure A.4, A.5 and A.6.

Device	Exposed time[s]	Dose[kRad]	Error
<i>TPS51200</i> <sub>1</sub>	2065	42	No
<i>MIC69302WU</i> <sub>1</sub>	2240	164	No
<i>SN74AVCB164245</i> <sub>1</sub>	967	65	No
<i>SN74AVC2T245</i> <sub>1</sub>	860	4.6	Yes
<i>QS3VH257</i> <sub>1</sub>	795	53	No
<i>SY89831</i> <sub>1</sub>	1251	94	No

Table 6.4: Tests at OCL 15.nov 2013

Device	Exposed time[s]	Dose[kRad]	Error
<i>ADN2814</i>	3600	345	Yes
<i>MAX3748</i>	2384	442	No
<i>TPS51200</i> <sub>2</sub>	-*	-*	-*
<i>MIC69302WU</i> <sub>2</sub>	1385	384	No
<i>SN74AVCB164245</i> <sub>2</sub>	526	201	No
<i>SN74AVC2T245</i> <sub>2</sub>	478	162	No
<i>QS3VH257</i> <sub>2</sub>	264	110	No
<i>SY89831U</i> <sub>2</sub>	921	166	No

\*The board didn't work at test time

Table 6.5: Tests at OCL 27-28.nov 2013

Device	Exposed time[s]	Dose[kRad]	Error
<i>INA210</i> <sub>1</sub>	1084	204	No
<i>INA210</i> <sub>2</sub>	1661	175	No
<i>TLV3011</i> <sub>1</sub>	742	111	Yes
<i>TLV3011</i> <sub>2</sub>	1074	138	Yes

Table 6.6: Tests at OCL 08-11.April 2014

### 6.2.2.12 Discussion of the Result

We had access to OCL in three periods; 13.11.13-15.11.13, 28.11.13-29.11.13 and 08.04.14-11.04.14, but most of the testing was performed 15.11.13, 28.11.13 and 11.04.14. The remaining days were used to become familiar with the instruments and equipment that was being used, to prepare the setup and setting up the beam.

Due to variations in the cyclotron setup and beam tuning from day to day, beam calibration had to be done each day at start-up.

The interesting aspect when determining if a component is tolerant against radiation is the absorbed dose of radiation. For run2 in the LHC, which will last for three years, it has been estimated that the total dose in the TPC is 1-2 kRad, see subsection 3.4.3. When it comes to radiation of components in this manner, there is a lot of uncertainties, like: the relation between scintillator counts and SEU on the SRAM, nonlinear relation between Scintillator counts and beam intensity, variation in the beam, measure of the output data, calculation, and more. We also have to take into account that when radiating at OCL, we have been using proton beam of less than 30 MeV. In the TPC detector in ALICE, we can receive protons and neutrons in the energy level of above 1 GeV, which may cause other effects than what we have seen in our test at OCL. It is therefore important that we have a good margin from the estimated radiation level in the TPC of 1-2 kRad, so that we won't risk see errors when all of the RCU2s are installed in the TPC. A safe margin of at least 3 times should be used, before clearing the components to be used in the TPC.

When it comes to radiation of components in this manner, there is a lot of uncertainties, like: the relation between scintillator counts and SEU, nonlinear relation between Scintillator counts and beam intensity, variation in the beam, measure of the output data, calculation, and more. There is therefore important that we have a good margin for the estimated radiation level in the TPC of 1-2 kRad, so that we won't risk see errors when all of the RCU2s are installed in the TPC.

For the test of SN74AVCB164245, SN74AVC2T245 and QS3VH257 the output signals were only measured digitally by using a USB-DAQ, which means that we don't know if we had a shift in voltage level caused by the received dose. The USB-DAQ used has an input low level from -0.3 V to 0.8 V and the input high level from 2.0 to 5.8, which means that we could actually have a large swing on the output without it being detected. Anyhow, changes on the output can normally be referred back to current consumption, as we can see on TPS51200, MIC69302WU and INA210. For all of the tests where we used digital measured output, we didn't see any increase in current until a dose of approximately 40 kRad, and therefore we can assume that the output signals were reliable at least until then.

Every components that was tested worked after receiving a dose of 6 kRad, which is three times more than the expected dose in ALICE TPC. That means that every

component that has been tested is cleared to be used in the RCU2 design. The component which performed worst is ADN2814, which gave us an error after a dose of 8 kRad, but since MAX3748, performed much better, and could be used for the same purpose, this would preferably be used.

### 6.2.3 Test Results on SF2

In this section the results from the radiation test of the SF2 M2S050ES will be presented. The different parts of the SF2 that were tested will be presented separately, and will be discussed at the end. Only one starter kit was tested, but the beam was turned off and on a few times during the test. After a dose of approximately 37 kRad we saw a very high increase in current, probably caused by a latchup. We did a power cycle of the board, and the current went back to a normal level. The test results presented are divided into before and after the power cycle, hereafter called run1 and run2. The shift-register design made for testing the logical element, see section 4.4.2, was only used in run2. After a dose of approximately 8 kRad on run2, the current increased again. We tried another power cycle, but this time it was permanently. The total dose after radiation was approximately 45 kRad.

#### 6.2.3.1 SRAM

The purpose of the SRAM test is to see how reliable the SRAM memory is, and to find a cross section for SEU in the memory. Figure 6.16 and 6.17 shows SEUs and fluence on large SRAM and micro SRAM as function of time for the radiation tests of the two starter-kits.

During the test, we had some problems with the microcontroller subsystem, which stopped working in periods, caused by the received radiation. The microcontroller subsystem was running in debug mode, which made it possible to restart the microcontroller subsystem when needed. When the microcontroller subsystem stopped working, a restart brought the communication back to normal. This can be seen as drops down to 0 in the SEU counter and small fall in current, see Figure 6.16 and A.2.

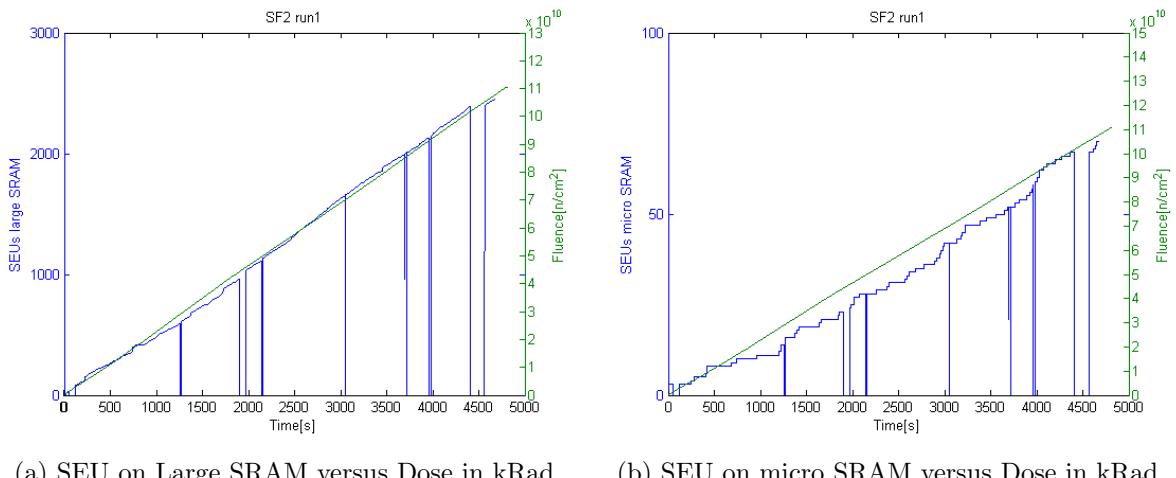


Figure 6.16: Large SRAM and micro SRAM test results before shutdown

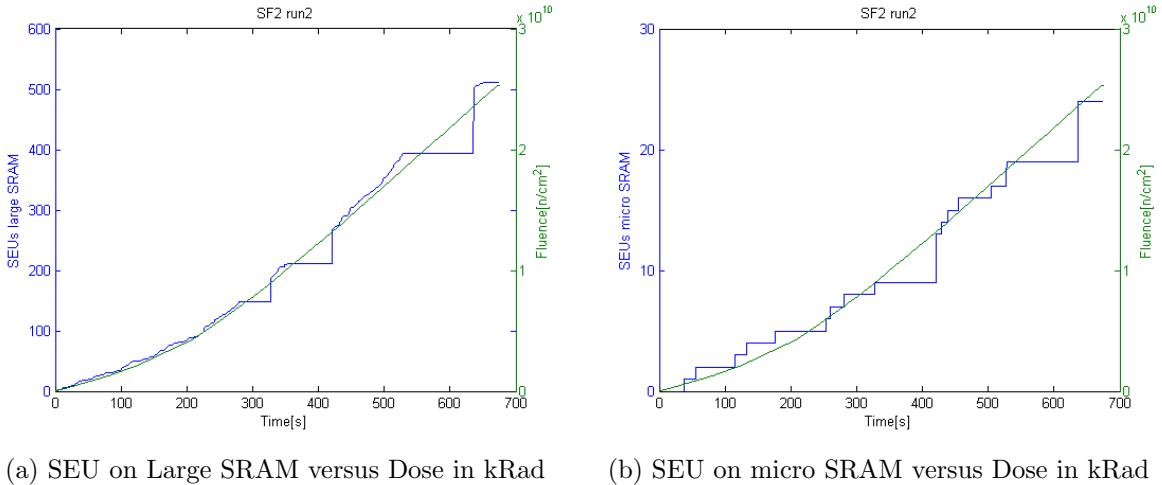


Figure 6.17: Large SRAM and micro SRAM test results after shutdown

For run 1 after around 4400 s, we see a gap where we had no increase in SEU on neither the large SRAM or the micro SRAM, see Figure 6.16. The flux is stable and the cycle counter is not changing either (see appendix A). This suggests that something is not working in the FPGA, and most likely something with the clock signal, possibly because of PLL lock loss. We got two PLL errors in that period supporting this theory, see Table 6.8

For both run1 and run2, see Figure 6.16 and 6.17, the SEU counters for the large SRAM and micro SRAM are increasing in line with the fluence. This means that we have a linear increase between the SEU counters and fluence, and cross section can be calculated.

There are much fewer memory bits in the micro SRAM compared to the large SRAM, in total there are approximately 9.5 times more bits in the large SRAM compared to the micro SRAM, respectively 622592 and 65536. That is why the SEU counter on micro SRAM isn't increasing as fast as for the large SRAM.

During run2, see Figure 6.17, the problem with the microcontroller subsystem increased. This can be seen as large periods with no increase in counter values and then high jumps in counter values when we got contact with the microcontroller subsystem again. The FPGA is working independently of the microcontroller system, and we should therefore not have any errors due to this problem.

To calculate the cross section, we should analyze over a period with as few errors as possible. The problem with the microcontroller subsystem didn't effect the SEU detection in the FPGA as we can see clearly from Figure 6.17. Therefore to calculate cross section for run1 we calculated in the period from 0 to 4400 seconds where we clearly got some kind of error. The fluence after 4400 seconds is  $1.04 \cdot 10^{11} \frac{n}{cm^2}$ , and the total SEUs for that period are 2386 and 70, respectively for the large SRAM and the micro SRAM. For

run2, we will calculate over the period from 0 seconds until we lost connection after 650 seconds. The fluence in that period is  $2.43 \cdot 10 \frac{n}{\text{cm}^2}$ , and the large SRAM SEU counter and micro SRAM SEU counter are respectively 511 and 24. The equation to calculate the cross section can be taken from equation 6.14, giving us:

$$CS = \frac{SEUs}{FluenceDUT} \frac{\text{cm}^2}{device} \quad (6.23)$$

## Uncertainties

A number of uncertainties are present in the measurement, and we therefore need to include them in the calculations.

- The uncertainty resulting from finding the ratio between the number of scintillator counts and the number of SEUs in the the SRAM radiation detector ( $\sigma_{ratio}$ ) was commonly about 10 %.
- The uncertainty introduced due to the nonlinear response ( $\sigma_{lin}$ ) of the scintillator to the intensity of the beam was estimated to be 10 %
- Since the number of SEUs detected are random in time and linearly dependent on the amount of incoming particles, the uncertainty can be given by Poisson distribution and is  $\frac{1}{\sqrt{N_{SEU}}}$
- Uncertainties from the errors ( $\sigma_{err}$ ) that occurred during the run, is estimated to be 10 %.
- The uncertainty of the position of the device at the extraction point we estimate to be 2 % ( $\sigma_{pos}$ ).

This gives us an uncertainty on the cross section of:

$$\sigma_{CS} = \sqrt{\sigma_{ratio}^2 + \sigma_{lin}^2 + \left(\frac{1}{N_{SEU}}\right)^2 + \sigma_{err}^2 + \sigma_{pos}^2} \quad (6.24)$$

The calculated values for cross section per bit with uncertainty can be found in Table 6.7.

To get a more precise calculation of cross section for the micro SRAM, we should have tested over a longer period or with a higher intensity, so we could have more statistics to base our calculations on.

Device	$N_{SEU}$	CS [ $\frac{cm^2}{device}$ ]	CS per bit [ $cm^2/bit$ ]	$\sigma_{CS}[cm^2/bit]$
$LargeSRAM_{run1}$	2386	$2.29 \cdot 10^{-8}$	$3.68 \cdot 10^{-14}$	$6.42 \cdot 10^{-15}$
$microSRAM_{run1}$	70	$6.73 \cdot 10^{-10}$	$1.03 \cdot 10^{-14}$	$1.80 \cdot 10^{-15}$
$LargeSRAM_{run2}$	511	$2.10 \cdot 10^{-8}$	$3.37 \cdot 10^{-14}$	$5.88 \cdot 10^{-15}$
$microSRAM_{run2}$	24	$9.88 \cdot 10^{-10}$	$1.51 \cdot 10^{-14}$	$2.71 \cdot 10^{-15}$

Table 6.7: Calculation of cross section with uncertainty

### 6.2.3.2 PLL and Latchup

The current was measured while irradiating the SF2, graphs of current as function of dose can be found in appendix A.2. Two SEL was detected during the radiation process. The first latchup occurred after a dose of approximately 37 kRad on run1 where the current went from around 270 mA to around 730 mA. Power needed to be turned off and on again for the current level to go back to normal. After a dose of approximately 8 kRad in run2 another latchup occurred increasing the current from 400 mA to around 850 mA. The nominal current for run2 was a little higher since the shift register design was also running.

In Table 6.8 and Figure 6.18 you can see the results from the PLL test for run1 and run2. The monitored lock signal came from a PLL that was driven by another PLL. Thus, assuming that if the first PLL loses its lock signal and thus clock, the second PLL will also lose its lock signal. This means that the counted number of PLL lock-loss have to be divided on two to get number of PLL lock-loss per PLL.

We have a large period in between a fluence of  $1.47 \cdot 10^{10} \frac{n}{cm^2}$  and  $5.45 \cdot 10^{10} \frac{n}{cm^2}$ , where we didn't detect any PLL lock-loss, which is rather strange. When calculating the cross section we will therefore calculate before and after this period, where the PLL lock-loss increases more linear with the increasing fluence, see Figure 6.18a.

Test	PLL lock loss	Exposed time[s]	Fluence [ $\frac{n}{cm^2}$ ]
Run1	18	4624	$1.06 \cdot 10^{11}$
Run2	5	589	$2.12 \cdot 10^{10}$

Table 6.8: Time and dose for the PLL errors run1

$$CS = \frac{\frac{PLLloss}{2}}{Fluence} = \frac{11.5}{1.36 \cdot 10^{11}} = 8.46 \cdot 10^{-11} \frac{cm^2}{PLL} \quad (6.25)$$

### Uncertainties

We will also here have some uncertainties in the measurement. These are:

- Since the number of errors detected is random in time and linearly dependent on the

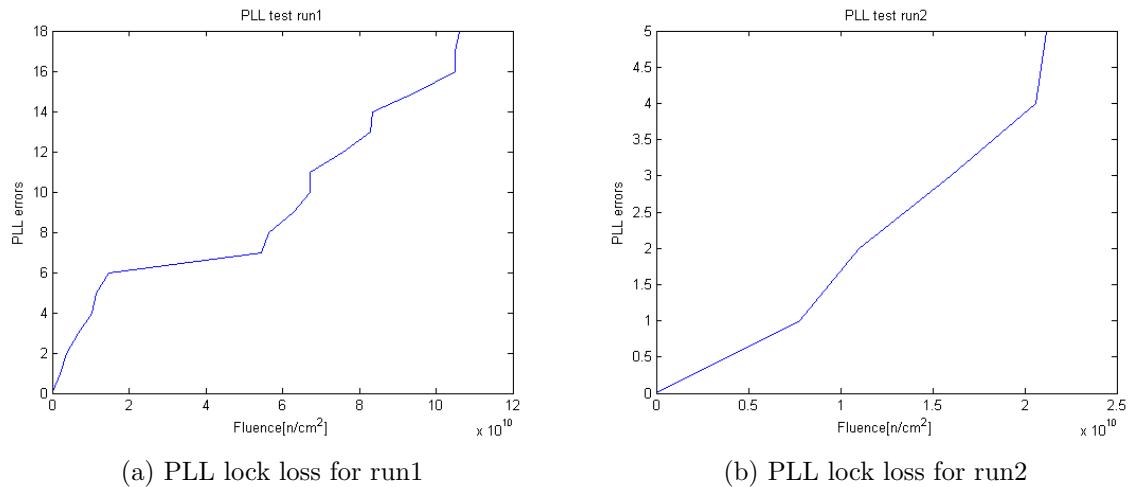


Figure 6.18: PLL lock loss as function of fluence

amount of incoming particles, the uncertainty can be given by Poisson distribution and is  $\frac{1}{\sqrt{N_{err}}}$

- The uncertainty resulting from finding the ratio between the number of scintillator counts and the number of SEUs in the SRAM radiation detector in the calibration process of the beam was commonly about 10 %.
  - The uncertainty introduced due to the nonlinear response ( $\sigma_{lin}$ ) of the scintillator to the intensity of the beam was estimated to be 10 %
  - The uncertainty of the position of the device at the extraction point we estimate to be 2 % ( $\sigma_{pos}$ ).

$$\sigma_{CS} = \sqrt{\left(\frac{1}{N_{err}}\right)^2 + \sigma_{ratio}^2 + \sigma_{lin}^2 + \sigma_{pos}^2} \quad (6.26)$$

The calculated cross section for a PLL lock-loss with uncertainties are as given in Table 6.9.

Test	PLL lock loss per PLL	Fluence[ $\frac{n}{\text{cm}^2}$ ]	CS [ $\frac{\text{cm}^2}{\text{PLL}}$ ]	$\sigma_{CS}$ [ $\frac{\text{cm}^2}{\text{PLL}}$ ]
Run1_period1	3	$1.47 \cdot 10^{10}$	$2.04 \cdot 10^{-10}$	$7.40 \cdot 10^{-11}$
Run1_period2	6	$5.19 \cdot 10^{10}$	$1.16 \cdot 10^{-10}$	$2.54 \cdot 10^{-11}$
Run2	2.5	$2.12 \cdot 10^{10}$	$1.18 \cdot 10^{-10}$	$5.01 \cdot 10^{-11}$

Table 6.9: Time and dose for the PLL errors run1

SEUs in the shift registers	Exposed time[s]	Fluence[n/cm <sup>2</sup> ]
5	620	$2.28 \cdot 10^{10}$

Table 6.10: Shift register errors in run2

### 6.2.3.3 Logic Element

For run1 we didn't manage to use the shift register design, due to some errors in the test code. This was solved before run2.

For the shift register design in run2 we had 4 shift register chains with a shift register length of 2000 registers, with 4 inverters in between each register and 4 windowed shift register for each chain. The clock frequency used was 40 MHz. Table 6.10 and Figure 6.19 shows the results from run2.

We detected 5 shift register errors in total over a total fluence of  $2.28 \cdot 10^{10}$ , see Table 6.10, this gives a cross section of  $2.19 \cdot 10^{-10} \frac{\text{cm}^2}{\text{device}}$ , and cross section per register of  $2.74 \cdot 10^{-14} \frac{\text{cm}^2}{\text{register}}$ . With the same uncertainties as for the PLL test, we get cross section with uncertainty to be,  $2.74 \pm 0.67 \cdot 10^{-14} \frac{\text{cm}^2}{\text{register}}$ . If compared to the cross section for SRAM memory, see Table 6.7, we got a little higher cross section than the micro SRAM and little lower then that large SRAM. Since the cross section for shift register error is calculated only from 5 errors, the calculated cross section may suffering from coincidence, and may not be precise.

One of the point with this test was to see if we could distinguish between SEU in the registers and SEUs caused by SET, by changing the frequency as discussed in subsection 4.4.2. This time we only run with a 40 MHz clock, meaning we can't say anything if the error we see is an upset in the registers, or a transient causing a upset. At least we got a indication of how often we would see an error in the shift register with a 40 Mhz clock and the settings we used for the test.

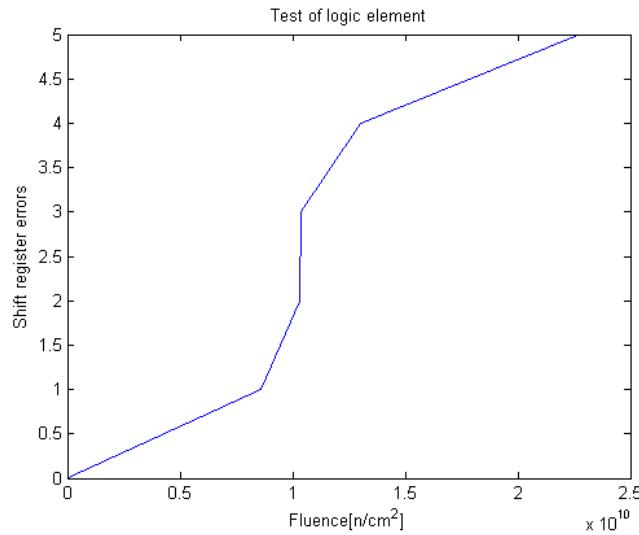


Figure 6.19: SEUs in the Shift register as function of fluence

#### 6.2.3.4 Discussion on the Results

The SRAM test gave us approximately the expected numbers of SEUs, however we had some problems with the microcontroller subsystem during the test. The calculated cross section for large SRAM for run 1 and 2 are respectively are  $3.68 \pm 0.64 \cdot 10^{-14} \frac{cm^2}{bit}$  and  $3.37 \pm 0.59 \cdot 10^{-14} \frac{cm^2}{bit}$ , and cross section for micro SRAM for run 1 and 2 are respectively  $1.03 \pm 0.18 \cdot 10^{-14} \frac{cm^2}{bit}$  and  $1.51 \pm 0.27 \cdot 10^{-14} \frac{cm^2}{bit}$ . The calculated values for both large SRAM and micro SRAM from run1 and run2 are very close to each other, which supports the result. Compared to other SRAM chips that have been tested [20] [6], the calculated cross section is in the same magnitude. The average cross section for the large SRAM is  $3.53 \pm 0.47 \cdot 10^{-14} \frac{cm^2}{bit}$  and the average for micro SRAM is  $1.27 \pm 0.16 \cdot 10^{-14} \frac{cm^2}{bit}$ .

Since we got problems with the microcontroller subsystem, we have some potential improvements for our test. We discovered that the microcontroller subsystem wasn't sufficiently reliable when exposed to radiation. That means that data extraction should preferable be performed without going through the microcontroller subsystem. This could have be done by making a serial communication code in VHDL, and using GPIO pins as transmitting and receiving lines. If another test should be done on the SF2 SRAM memory, this could been an improvement to the test.

We also had a noticeable amount of PLL lock-losses which could be problematic when the RCU2s will be mounted in the TPC. If the assumption that when the PLL loses its lock, the clock also falls low, is correct, we would have a period where we don't have any data collection every time the lock signal falls down. The average cross section for PLL lock-loss, calculated from the values found in Table 6.9, is  $1.46 \pm 0.31 \cdot 10^{-10} \frac{cm^2}{PLL}$

We didn't detect any current increase before a dose of 37 kRad, which is a really

good result compared to the dose of 1-2 kRad that we can expect in the TPC, see subsection 3.4.3.

For the shift register design we wanted to see if we would have higher cross section with higher frequencies, indicating that we are able to pick up more SET with higher frequency. Since we only tested on one frequency, we couldn't distinguish between SET and SEU in the registers, but we still got an indication of the radiation tolerance of the logic element. The calculated cross section for SEU in the shift-register design with a 40 Mhz clock signal, and 4 inverts in between each register is  $2.74 \pm 0.67 \cdot 10^{-14} \frac{\text{cm}^2}{\text{register}}$ .

To know how often we can expect to encounter errors for the parts of the SF2 which gave been tested, when the RCU2s will be mounted in the TPC, an new variable will be introduced called Mean time between Failure (MTBF). Mean time between failure tells us the expected time between two errors, or from start to the first error, and the equation is as can be seen in Equation 6.27.

$$MTBF = \frac{1}{CS * flux} [\text{s}] \quad (6.27)$$

The expected flux has been estimated in subsection 3.4.3, to be  $3 \frac{\text{KHz}}{\text{cm}^2}$  or  $3 \cdot 10^3 \frac{1}{\text{cm}^2 \text{s}}$ . And cross section has allready bee calculated. To calculate a MTBF in the TPC we have to scaled up for 216 RCU2s, 56340 registers, 622592 large SRAM bits, 65536 micro SRAM bits and 1 PLL. Table 6.11 shows the results.

Tested	Average cross section [ $\text{cm}^2$ ]	MTBF run2 216 RCU2 [hours]
large SRAM	$3.53 \pm 0.47 \cdot 10^{-14}$	0.02
micro SRAM	$1.27 \pm 0.16 \cdot 10^{-14}$	0.52
PLL	$1.46 \pm 0.31 \cdot 10^{-10}$	2.94
Registers	$2.74 \pm 0.67 \cdot 10^{-14}$	0.28

Table 6.11: Cross section and MTBF for run2, based on result from TSL

From the results presented in Table 6.11, it can be seen how often we can expect an error for the different parts of the SF2 which has been tested, assuming we uses all registers, all of the SRAMs, and only on PLL in the RCU2 design. Memory cells like SRAM and registers are known to be week for radiation, see subsubsection 3.4.1.3, so the result wasn't any surprise. All of the SRAM memory and registers, will probably not be used, which means that the calculated MTBF will in reality be that low.

A PLL lock-loss will happen every third hour according to the acquired data, and that is with am assumption that only 1 PLL is used per RCU2. The effect of a PLL lock-loss, is still partially unknown, it may only result in one lost clock period, which probably wont harm to much, or it may fall down for seconds, which means that useful data can be lost. More test should be performed on this aspect when we have a more complete firmware running on the RCU2, to see if the firmware tolerates to lose clock for a short period.

All in all the first radiation test of the SF2 did go quite well.

## 6.3 Results from TSL

In this section the results from the irradiation tests at TSL will be presented. The focus has been to test the SF2 SoC FPGA, but other tests will briefly be presented and discussed.

A total of two RCU2s and three SF2 starter-kits were exposed to radiation. When we radiated the RCU2, we tested detector data link (DDL), Clock and data recovery, latchup and trigger interface. When testing the SF2 starter-kits, the focus was mainly the test mentioned in section 4.4.

### 6.3.1 SF2 Radiation Test

Two starter-kits with SF2 M2S050-FG484, and one starter-kit with SF2 M2S050ES-FG896 (engineering sample) were tested. The SF2 M2S050-FG484 is the same SoC FPGA which are used on the RCU2, only with smaller package. Therefore we preferred testing these instead of the engineering sample versions, which may have some early design errors. The parts of the SF2 that were tested on the starter-kits with the smaller package are SRAM, PLL, Logic element and latchup. When testing the M2S050ES-FG896, the focus was only to see for how long we could program the device with increasing dose of radiation.

Some improvements have been made to the test since the radiation at OCL. We have added two more PLL lock signals to measure, and we have found a more effective way to measure current. Instead of using the current measurement board as described in section 4.4.4.3, we used a small PCB with several INA226 chips, which is an ADC with  $I^2C$  communication protocol. The SF2 also has  $I^2C$  communication protocol, meaning we could use the monitoring board to control and receive data from the ADC-chip. By using this method we also got the voltage on each of the different power source that was measured. The monitoring board was also connected to the enable pin of the 3.3 V *voltage regulator* on the test board, making it possible to turn on and off the starter-kit during a test. Every tenth of a second the status of data was written to a console and to a file, which made it possible to monitor as the tests were running, and look at the data afterwards.

Also instead of running the Microcontroller subsystem in debug mode, as we did in OCL, we were running in release mode. This means that the microcontroller subsystem was running whenever we got power on the kit.

Device	Starter-kit1	Starter-kit2
Nr. of power cycles	62	95
PLL1 loss	22	3
PLL2 loss	116	136
PLL3 loss	60	69

Table 6.12: Overview of power cycles and PLL lock loss

### 6.3.1.1 PLL and Latchup

We monitored three PLL lock signal during the tests of the two starter-kits. We got a total of 176 PLL lock loss from the first test and 205 PLL lock-loss from the second test. Whenever we lost lock on PLL1 we also got a lock-loss on PLL2 since this PLL was using the clock from PLL1 as source. Therefore the PLL1 lock-loss count hasn't been taken into the total lock loss count. The distribution over the three PLL lock signals can be seen in table 6.12.

We can find a cross section for PLL lock loss. The total fluence for the two tests is  $2.39 \cdot 10^{11} \frac{n}{cm^2}$  and  $2.93 \cdot 10^{11} \frac{n}{cm^2}$ , which gives us a cross section per PLL:

$$CS_{test1} = \frac{\frac{PLLloss}{3}}{Fluence} = \frac{58,67}{2.39 \cdot 10^{11}} = 2.45 \cdot 10^{-10} \frac{cm^2}{PLL} \quad (6.28)$$

$$CS_{test2} = \frac{\frac{PLLloss}{3}}{Fluence} = \frac{205}{68,33 \cdot 10^{11}} = 2.33 \cdot 10^{-10} \frac{cm^2}{PLL} \quad (6.29)$$

We will also have some uncertainties in the measurement. These are:

- Since the number of errors detected are random in time and linearly dependent on the amount of incoming particles, the uncertainty can be given by Poisson distribution and is  $\frac{1}{\sqrt{N_{err}}}$
- Downtime due to power cycle of the board during a run we estimate a uncertainty of 5 % ( $\sigma_{pow}$ ).
- From the uncertainty of the position of the device at the extraction point we estimate 2 % ( $\sigma_{pos}$ ).
- The fluence measurement will have a some uncertainty. This is estimated to be about 2 % ( $\sigma_{flu}$ ).

$$\sigma_{CS} = \sqrt{\left(\frac{1}{N_{err}}\right)^2 + \sigma_{pow}^2 + \sigma_{pos}^2 + \sigma_{flu}^2} \quad (6.30)$$

The cross section, with uncertainty taken into account, will be:

$$CS_{test1} = 2.45 \pm 0.14 \cdot 10^{-10} \frac{cm^2}{PLL} \quad (6.31)$$

$$CS_{test2} = 2.330.13 \cdot 10^{-10} \frac{cm^2}{PLL} \quad (6.32)$$

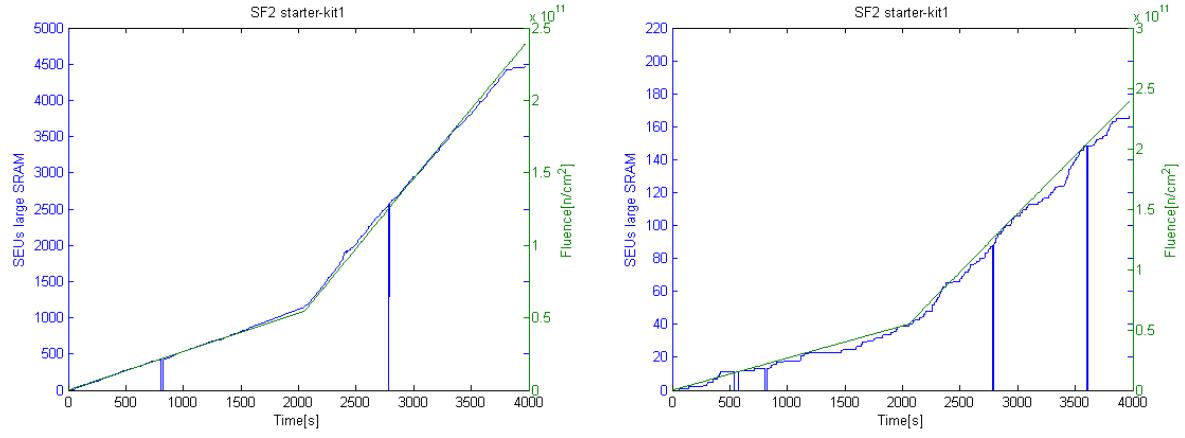
We discovered during the first test, that the  $0.1 \Omega$  and  $0.16 \Omega$  resistors which were used, respectively to measure current on the  $1.2 \text{ V}$  and  $3.3 \text{ V}$  power source, were too high, since the maximum voltage the ADC could measure is  $81.92 \text{ mV}$ . When a latchup occurred, the ADC was maxed, meaning we only knew that the voltage is above  $81.9 \text{ mV}$  (current above  $819 \text{ mA}$  and  $509 \text{ mA}$ , respectively for  $1.2 \text{ V}$  and  $3.3 \text{ V}$ ). Therefore both of these resistors were replaced with a resistor of  $0.025 \Omega$  on the second test with the starter-kits.

Sometimes during our tests we got sudden fall in current. When this happens the measured voltage for the  $1.2 \text{ V}$  power source also drops, typically down to about  $850 \text{ mV}$  (the  $3.3 \text{ V}$  power source is stable though). When this happens the communication through the serial port also fails, which is understandable since the power source has dropped  $300 \text{ mV}$  below the specification for the component. Normally when we see a decrease in voltage, we see an increase in current, or opposite, but in this case they both drop. This suggest that the voltage drops first, causing processes in the SF2 to shut down, which results in decrease in current. What's causing this effect is unknown, but a theory could be that the DC-DC regulator, which controls the  $1.2 \text{ V}$  power source had some reaction to irradiation. The regulator is located right next to the SF2 chip, and it is therefore very exposed to radiation. Normally regulators have a gradually increase or decrease in the output voltage, as can be seen on both TPS51200 and MIC69302WU, but since this is a DC-DC regulator with programmable output voltage, we may have other effects, like the one that we detected.

By turning off and on the  $3.3 \text{ V}$  regulator, resulting in turning the  $1.2 \text{ V}$  off and on (since this is powered by the  $3.3 \text{ V}$  signal), the voltage and current goes back to start value. This was done through the monitoring board, where we had made a function which turns the regulators off and on again after 3 seconds. This function was used whenever we detected a latchup or a decrease in current/voltage. In total we had to restart the board because of latchup or decrease in current 61 times on the first test and 95 times on the second test, as seen in Table 6.12.

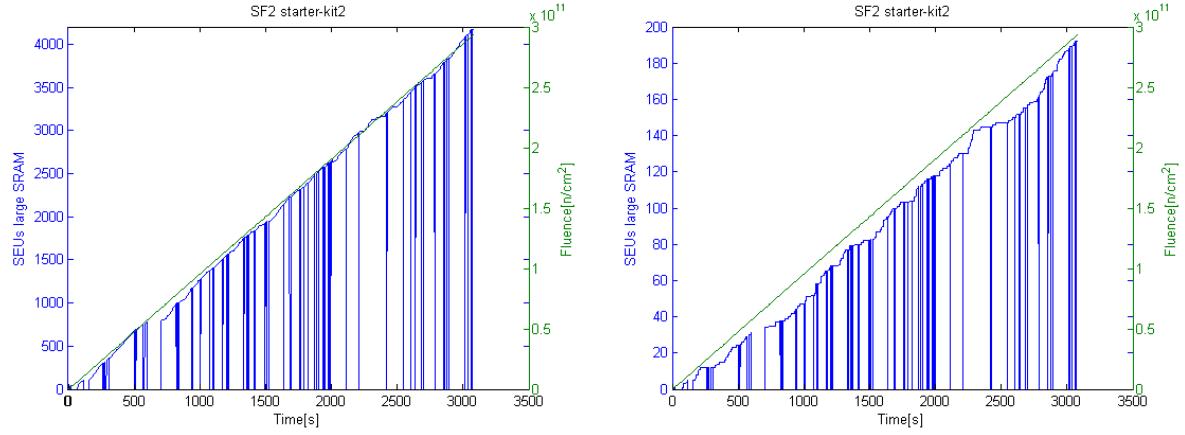
### 6.3.1.2 SRAM

Figure 6.20 and 6.21 shows the results from the SRAM test after radiation of the two starter-kits. We detect regularly drops down to 0 in the counter values. This is due to loss of communication with the microcontroller subsystem, and thereof the SF2, probably caused by voltage drop or latchup as discussed in the previous subsection. A re-power of the board made the counters start again. This means that we had short periods where we didn't get to measure counter values. When the FPGA was powered again, the counter values are overwritten through the startup sequence, as described in section 4.4.1. The length of these non-measuring periods are varying from only a few seconds up to tens of seconds, which gives us a lot of uncertainties when calculating cross section.



(a) SEU on Large SRAM and fluence versus Time (b) SEU on micro SRAM and fluence versus Time

Figure 6.20: Large SRAM and micro SRAM test results after shutdown



(a) SEU on Large SRAM and fluence versus Time (b) SEU on micro SRAM and fluence versus Time

Figure 6.21: Large SRAM and micro SRAM test results after shutdown

### Cross Section Calculation

we can see that we have almost linear increase in the SEUs counter compared to fluence

Device	Fluence start [ $\frac{n}{cm^2}$ ]	Fluence stop [ $\frac{n}{cm^2}$ ]	Fluence loss [ $\frac{n}{cm^2}$ ]	Total fluence [ $\frac{n}{cm^2}$ ]	$N_{SEU}$
Large SRAM1	$2.20 \cdot 10^{10}$	$2.23 \cdot 10^{11}$	$2.47 \cdot 10^{10}$	$1.76 \cdot 10^{11}$	3994
micro SRAM1	$2.20 \cdot 10^{10}$	$2.23 \cdot 10^{11}$	$2.47 \cdot 10^{10}$	$1.76 \cdot 10^{11}$	146
Large SRAM2	$6.70 \cdot 10^{10}$	$2.92 \cdot 10^{11}$	$6.38 \cdot 10^{10}$	$1.61 \cdot 10^{11}$	3379
micro SRAM2	$6.70 \cdot 10^{10}$	$2.92 \cdot 10^{11}$	$6.38 \cdot 10^{10}$	$1.61 \cdot 10^{11}$	159

Table 6.13: Fluence and SEUs overview for test 1 and 2

for test1 and 2 of the starter kit, see Figure 6.20 and 6.20. We have a small gap after a approximately 800 s for under test 1 and we have a small gap between 600 and 700 seconds for test 2. When calculating the cross section we will calculate from after these two gaps. That means that the fluence for test 1 is  $2.01 \cdot 10^{11}$  and number of SEU in that period is 3388 and 192 respectively for large SRAM and micro SRAM. The total fluence for test 2 is  $1.61 \cdot 10^{11}$ , and the number of SEU in that period is 3379 for large SRAM and 159 for micro SRAM.

To get as genuine value of the cross section as possible, we have to find the total fluence of when the test was working. This means that the fluence received when the test was stopped due to latchup, current drops and power cycles, have to be subtracted. By checking the log-files we have estimated time with no data to be 287 second in the period of interest for test1 and the 669 in in the period of interest for test2. The flux in that period is known (see flux graph in appendix A), which means that we can calculate the total fluence for the time without data collection. See table 6.13 for the calculated values.

## Uncertainties

A number of uncertainties are present in the measurement:

- Since the number of SEUs detected are random in time and linearly dependent on the amount of incoming particles, the uncertainty can be given by Poisson distribution and is  $\frac{1}{\sqrt{N_{SEU}}}$
- Uncertainties from data collection, estimations and assumptions when doing calculation, like constant flux in periods. We estimate an uncertainty of 10 % ( $\sigma_{data}$ ).
- The uncertainty of the position of the device at the extraction point we estimate to be 2 % ( $\sigma_{pos}$ ).
- The fluence data given to us we will also have some uncertainty. This is estimated to be 2 % ( $\sigma_{flu}$ ).

This gives us an uncertainty on the cross section of:

device	CS [ $cm^2$ ]	CS per bit [ $cm^2/bit$ ]	$\sigma_{CS}[cm^2/bit]$
Large SRAM1	$2.27 \cdot 10^{-8}$	$3.64 \cdot 10^{-14}$	$3.79 \cdot 10^{-15}$
micro SRAM1	$8.30 \cdot 10^{-10}$	$1.27 \cdot 10^{-14}$	$1.32 \cdot 10^{-15}$
Large SRAM2	$2.10 \cdot 10^{-8}$	$3.37 \cdot 10^{-14}$	$3.50 \cdot 10^{-15}$
micro SRAM2	$9.88 \cdot 10^{-10}$	$1.51 \cdot 10^{-14}$	$1.57 \cdot 10^{-15}$

Table 6.14: Calculation of Cross section with uncertainty

$$\sigma_{CS} = \sqrt{\left(\frac{1}{N_{SEU}}\right)^2 + \sigma_{data}^2 + \sigma_{pos}^2 + \sigma_{flu}^2} \quad (6.33)$$

Now we can calculate the cross section per bit with uncertainty from the values in table 6.13, knowing that we have 622592 bits in the large SRAM and 65536 bits in the micro SRAM.

This gives us the average a cross section of the large SRAM and micro SRAM to be:

$$CS_{LSRAM} = (3.65 \pm 0.26) \cdot 10^{-14} \frac{cm^2}{bit} \quad (6.34)$$

$$CS_{uSRAM} = (1.39 \pm 0.10) \cdot 10^{-14} \frac{cm^2}{bit} \quad (6.35)$$

### 6.3.1.3 Logic Element

For the two tests with the starter-kits we used a clock signal of 40, 80 and 160 MHz for the shift-register design. This means that we should see some difference in cross section for the different frequencies. We used 4 shift-register chains with a length of 2500 flip-flops, and with 4 windowed shift registers (WSR). On run1 we used 4 inverters in between each register, and on run2 we used none. Table 6.15 shows an overview of SEU on the shift register for the different frequencies and the total fluence over that period. the cross section is also calculated with the same uncertainties as for PLL, see subsubsection 6.3.1.1.

The results presented in table 6.15 are quite unexpected. We would think that by increasing the frequency, we would see more SEUs in the registers, but this isn't the case. The reason for this may be that we had too low statistics. If we had run in the respectively frequencies for a longer time period or with a higher flux, we would maybe see different results.

Frequency	inverters	Fluence [ $\frac{n}{cm^2}$ ]	SEU on shift-register	CS [ $\frac{cm^2}{register}$ ]
40 MHz	4	$1.40 \cdot 10^{11}$	51	$3.65 \pm 0.22 \cdot 10^{-14}$
80 MHz	4	$9.90 \cdot 10^{10}$	26	$2.63 \pm 0.18 \cdot 10^{-14}$
40 MHz	0	$6.16 \cdot 10^{10}$	19	$5.19 \pm 0.40 \cdot 10^{-14}$
80 MHz	0	$7.20 \cdot 10^{10}$	30	$4.17 \pm 0.28 \cdot 10^{-14}$
160 MHz	0	$1.60 \cdot 10^{11}$	32	$1.19 \pm 0.08 \cdot 10^{-14}$

Table 6.15: Cross section for the shift-register design with different frequencies

#### 6.3.1.4 Programming Limit Test

The idea behind the programming limit test was to see how high in radiation dose we could expose the SF2 and still be able to program. We were supposed to use the same test setup as used when testing the two starter-kits so that we would have approximately the same current, and the ability to shut it down when needed. But we didn't managed to get the small PCB with INA226 to work. we therefore decided to just power cycle the board regularly during our test and increase the dose of approximately 1 kRad for each time attempting to program.

We tried to program after a dose of 1.20 kRad, 2.54 kRad and 3.80 kRad. The two first times it worked fine, but the last time the programming failed.

### 6.3.2 Other Test at TSL

The other test at TSL includes Detector data link 2 (DDL2) test, Timing Trigger and Control (TTC) test and latchup detection under radiation of RCU2. A brief introduction to how this was tested, and the setup used is explained below:

#### 6.3.2.1 Detector Data Link 2 DDL2

The DDL2 test involves sending data with a speed of 2.215 Gbps back and forth from the RCU2 and a *Xilinx Virtex-7 FPGA VC709 Connectivity Kit*, through optical transceivers. To control the test a *Chip Scope IBERT core* [29] was used, which includes pattern generators and checkers for the optical transceivers on the Connectivity kit. From the IBERT core we are able to send a given data sequence with a desired line rate out from the optical transceiver on the kit. The transmitted data is sent to the DDL2 on the RCU2, and further to the SERDES lines on the SF2. The SERDES lines is set to echo back the received signal to the DDL2, which sends it further back to the Connectivity kit. The returning data to the Connectivity kit is checked for bit errors in the IBERT core, and if the incoming data is not equal the outgoing data, a counter will be incremented. A

sketch of the setup, can be seen in Figure 6.22

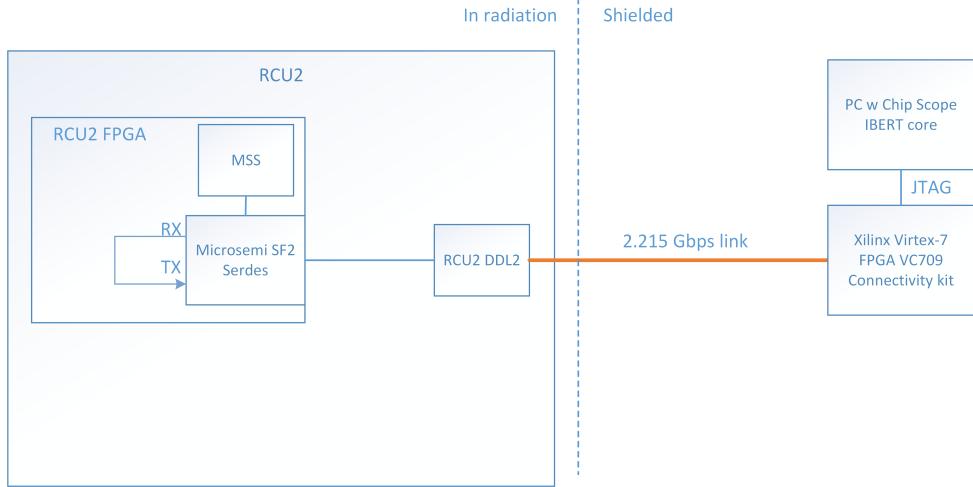


Figure 6.22: A sketch of the DDL2 test

For the test we exposed both the SF2 and the optical transceiver on the RCU2. For both of the test we detected few errors, less than 10 errors with a fluence of  $3.18 \cdot 10^{11} \frac{n}{cm^2}$  when exposing the SF2 chip, and less than 5 errors when exposing the optical transceiver with a fluence of  $3.6 \cdot 10^{11} \frac{n}{cm^2}$ . This gives cross section of  $3.14 \cdot 10^{-11} cm^2$  and  $1.39 \cdot 10^{-11} cm^2$  respectively for when exposing the SF2 and the optical transceiver.

### 6.3.2.2 Timing Trigger Control TTC test

To explain how the TTC test worked, a little explanation on how the hardware is set up is required. An optical Manchester decoded signal containing clock and data is sent to the RCU2. On the RCU2 there is an optical receiver which receives the Manchester signal, but the received signal may vary, and is not so stable. Therefore a limiting amplifier is used to make a stable digital signal of the signal coming from the optical receiver. MAX3748 [30] is used for that purpose (which is one of the components tested through this work). Then the stable signal coming from the limiting amplifier is sent in to the SF2 FPGA, where clock and data is encoded, giving us a 40 MHz clock, and data signal. The clock signal is then sent into two different PLLs, and the PLL lock signal for both PLLs is checked for a falling edge. The idea behind using two PLLs, is to distinguish between PLL error and error in the incoming signal. If both of the PLLs lose lock at the same time we can assume that we have an error with the incoming signal and if only one of the PLLs loses lock, we have a PLL error. The received data signal contains a known trigger sequence, and a VHDL code is made to check for this trigger sequence. Every time the trigger pattern is detected a counter is incremented. PLL lock data and trigger counter are sent to the microcontroller subsystem, where data is sent serial to a computer. On the computer a program is running receiving data from the serial port, and logging data every seconds. A overview of the setup can be seen in Figure 6.23

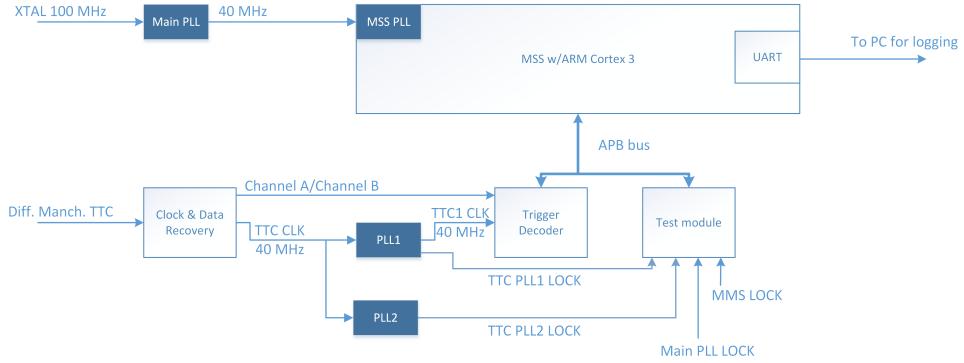


Figure 6.23: An overview of the TTC test

For the TTC test, we exposed both the SF2 and the optical receiver. When we exposed the SF2, we received PLL lock loss with about the same frequency as for the test with the Starter-kits, and the calculated cross section was  $2.3 \cdot 10^{-10} \frac{\text{cm}^2}{\text{PLL}}$ . Almost all the PLL errors were defined as PLL lock-loss due to bad PLLs. But when we started to expose the optical receiver, we detected PLL lock-loss on both of the PLLs all the time, we got a cross section of  $6.9 \cdot 10^{-9} \text{cm}^2$ .

For the latchup test on the RCU2, we determined the cross section for latchup to be  $8.5 \cdot 10^{-10} \text{cm}^2$ . We made a discovery while running the beam. After we received a few latchups, the 1.2 Voltage started to reduce a little, and when this happened, we saw a tendency of receiving less latchups. We did a separated test on the RCU2 where we reduced the 1.2 Voltage to 1.1 V by changing a resistor on the board. The test showed us that we got a reduction on cross section to  $1.7 \cdot 10^{-10} \text{cm}^2$ , which is a reduction of approximately 5. More tests on this area should be performed, to see how far down in voltage one could go before things stopped working, and if the latchup problem could be reduced even more.

### 6.3.3 Discussion of the Results

A issue that we encountered in the tests at TSL, but not so much in OCL, is latchup. We got regularly latchup during our tests, and a repower was required to set the board back in normal operation again. The latchups weren't destructive. A solution for this issue has already been set in motion. By using *INA210* to amplify a voltage over a shunt resistor for each of the power signals, and use *TLV3011* to compare the amplified voltage with a voltage limit. If the voltage limit is exceeded, all regulators are turned off, setting the board off. But we will still have a small period of lost data when repowering the RCU2.

We also discovered a way to reduce latchups. By changing the 1.2 source voltage to 1.1 V, we effectively reduced number of latchup by approximately 5, and this can possibly be brought even lower by reducing the voltage even further. More test on this aspect should be performed.

The SRAM test on the two starter-kits was successfully performed, we had a lot of downtime due to errors, but the calculated cross section for both of our test were quite close, which supports the results. The average cross section for large SRAM is  $3.65 \pm 0.26 \cdot 10^{-14} \text{cm}^2$ , and for micro SRAM is  $1.39 \pm 0.10 \cdot 10^{-14} \text{cm}^2$ . This can be compared with the results from OCL, where a cross sections of  $3.53 \pm 0.47 \cdot 10^{-14} \text{cm}^2$  for the large SRAM, and  $1.27 \pm 0.16 \cdot 10^{-14} \text{cm}^2$  for the micro SRAM were found. There is a noticeable difference in energy level from OCL to TSL, and we would therefore examine if we should expect a difference in the calculated cross sections.

SEU occur due to ionizing particles charge generation close to sensitive nodes. Proton has in itself not enough ionizing capability to directly cause a SEU, but protons can have nuclear reactions with silicon or other material in a component, producing secondary radiation with higher ionization capability, which then can cause a SEU. [19] shows that cross section for proton-silicon interaction has a peak value around 20 MeV. But a component consist of more than only silicon that have other cross sections for interaction with proton. We will also with higher energies have higher chance of having secondary radiations and the ionizing capability of the secondary radiation increases as well. There is therefore hard to say which energy to expect highest cross section, since there are effects pointing in both direction. The results shows a little higher cross section for a 170 MeV beam compared to a 25 MeV beam, but taken the uncertainties into account, we could say that they are equal.

For the test of the logic element, we wanted to see if SET could be a problem on the SF2. SET was supposed to be detected by getting a higher cross section with a higher frequency on the shift-register design. However the results as presented inn Table 6.15 doesn't show a increase with higher frequency, and we are therefore not able to distinguish between SEU and SET. It may be that we didn't have sufficient data to have a good statistic, and therefore are seeing inconsistency increase of SEU with the frequency.

For all of the test with PLL, we got a cross section for PLL lock-loss in the area of  $2 - 3 \cdot 10^{-10} \text{cm}^2$  when the SF2-chip was exposed. From the TTC test, we got a cross section of  $2.3 \cdot 10^{-10} \frac{\text{cm}^2}{\text{PLL}}$  and when exposing the starter-kits we got a cross section of  $2.39 \pm 0.10 \cdot 10^{-10} \frac{\text{cm}^2}{\text{PLL}}$ . But when we exposed the optical receiver instead of the SF2, we got a lot more PLL lock-loss. The calculated cross section was  $6.9 \cdot 10^{-9} \text{cm}^2$ , which is around 25 times more then when the SF2 was exposed. This means that either the optical receiver is not able to do its job under high radiation level, and introduces a lot of noise, or the limiting amplifier MAX3748 is not able to remove noise from the incoming signal.

To know how often we can expect to encounter the different Single event effects errors when the RCU2s will be mounted in the TPC, we will calculate MTBF, as we did after the result in OCL. See Equation 6.27 for how MTBF is calculated. We also have to scale up for 216 RCU2s, 622592 large SRAM bits, 65536 micro SRAM bits and 1 PLL. The results can be found in Table 6.16.

Test	Average cross section [cm <sup>2</sup> ]	MTBF run2 216 RCU2 [hours]
large SRAM	$3.65 \pm 0.26 \cdot 10^{-14}$	$\sim 0.02$
micro SRAM	$1.39 \pm 0.10 \cdot 10^{-14}$	$\sim 0.47$
PLL starter kit test	$2.39 \pm 0.10 \cdot 10^{-10}$	$\sim 1.79$
TTC PLL when SF2 irradiated	$2.3 \cdot 10^{-10}$	$\sim 1.86$
TTC PLL when optical receiver irradiated	$6.9 \cdot 10^{-9}$	$\sim 0.06$
Latchup SF2 irradiated 1.2 V	$8.5 \cdot 10^{-10}$	$\sim 0.5$
Latchup SF2 irradiated 1.1 V	$1.7 \cdot 10^{-10}$	$\sim 2.5$

Table 6.16: Cross section and MTBF for run2, based on result from TSL

The result from Table 6.16 tells us that every 4 minutes for run2 in the TPC we will have a PLL error due to radiation on the optical receiver. This is quite often, and it could be a major problem if not countered or fixed in some way. This means either that the optical receiver are not able to convert the optical signal correctly under high radiation level, or the optical receiver is producing some noise due to radiation, which the limiting amplifier are not able to suppress. It is nevertheless quite often and a solution to reducing or remove this effect should be found.

Whats happening to the clock signal when the lock signal falls down could also be discussed. we have previous assumed that when the lock signal falls down, so those the clock signal, but this is necessary the case. The lock signal should tell us if the input signal and output signal to the PLL is in sync, but it doesn't necessarily kills the output signal of the PLL when the lock signal falls low. If we have a lock-loss and the clock signal still goes through, it means that we would have a clock signal which are missing one or more clock pulses, are out of phase, or have a lot of noise. The effect of these cases is unknown, it may cause the entire RCU2 firmware to fall down, or it may not cause any harm at all. During the radiation tests we had had periods where we didn't got contact with the SF2 from time to time, if this was caused by PLL lock-loss or other effects like latchup is unknown. More test on this aspect should also be performed to be sure that it wont a problem when all of the RCU2's are mounted in the TPC.

We also see that we could expect a latchup every half an hour in the TPC, if the normal 1.2 V core voltage is used. We can also see that time between each latchup increases by a factor 5 by reducing the core voltage to 1.1 V instead of 1.2 V. We don't know if 1.1 V is the absolute minimum we could go before functions in the SF2 stops working, and more test on this aspect should also be performed. Maybe the latchup problem could be removed by using a 1.0 V core voltage.

The MTBF results also shows that we would have a SEU in the large SRAM ever minutes if all of the RCU2 memory is used. This is quite expected since it is SRAM, which is known to be weak towards radiation, see subsection 4.4.1.

# **Chapter 7**

## **Conclusion and Outlook**

The work presented in this thesis was carried out in order to investigate the radiation tolerance for components used in the design of RCU2. The main focus has been on the RCU2's main FPGA, the SmartFusion2 SoC FPGA. This has been tested for single event upset in the internal SRAM memory, registers and PLLs, single event transient in the logic elements and interconnections, and single event latchup for the entire chip. The other components that have been tested are TPS51200, MIC69302WU, SN74AVCB164245, SN74AVC2T245, QS3VH257, SY89831, ADN2814, MAX3748, INA210 and TLV3011, but then the focus has been on accumulative effects.

# **Appendix A**

## **Radiation Results**

### **A.1 Beam setup data**

Calibration test nr.:	x	y	Scint rel	SEU(SRAM)	SEU(SRAM)/sc
1	0	0	23813	1971	8.28E-02
2	0	-0.5	37930	3867	1.02E-01
3	0	-1	27527	2817	1.02E-01
4	0	-1.5	34413	3360	9.76E-02
5	0	-2	32713	2763	8.45E-02
6	0.5	0	38753	2709	6.99E-02
7	-0.5	0	23420	2483	1.06E-01
8	-1	0	20611	2232	1.08E-01
9	-1.5	0	21014	2410	1.15E-01
10	-1.5	0	20676	2260	1.09E-01
11	-2	0	35787	3776	1.06E-01
12	-2.5	0	27847	2512	9.02E-02

Table A.1: Calibration tests 14.11.2013

Calibration test nr.:	x	y	Scint rel	SEU(SRAM)	SEU(SRAM)/ sc
1	-0.8	-1	17798	1463	5.26E-02
2	-1.3	-1	17721	1239	6.99E-02
3	-1.8	-1	12904	1203	9.32E-02
4	-2.3	-1	13361	1276	9.55E-02
5	-2.8	-1	12786	1238	9.68E-02
6	-3.3	-1	12342	1156	9.37E-02
7	-2.5	-1	11696	1223	1.05E-01
8	-2.5	-1.5	11027	1075	9.75E-02
9	-2.5	-2	11835	1063	8.98E-02
10	-2.5	-0.5	15593	1540	9.88E-02
11	-2.5	0	12620	1034	8.19E-02
12	-2.5	-1	65280	5999	9.19E-02
13	-2.5	-1	52752	4803	9.10E-02
14	-2.5	-1	57229	5250	9.17E-02

Table A.2: Calibration tests 15.11.2013

## A.2 Radiation Results from OCL

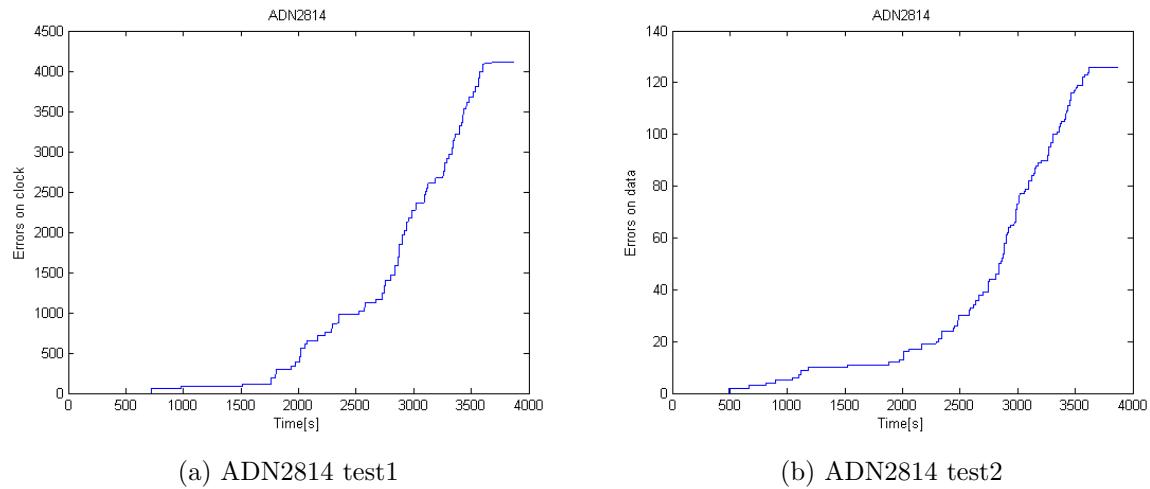


Figure A.1: ADN2814 - Errors on data and clock vs Time

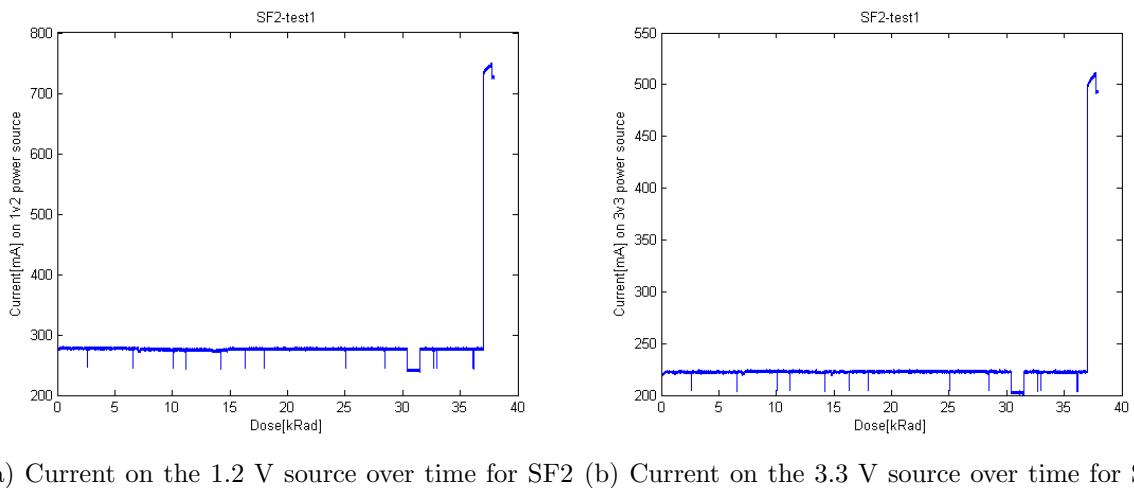
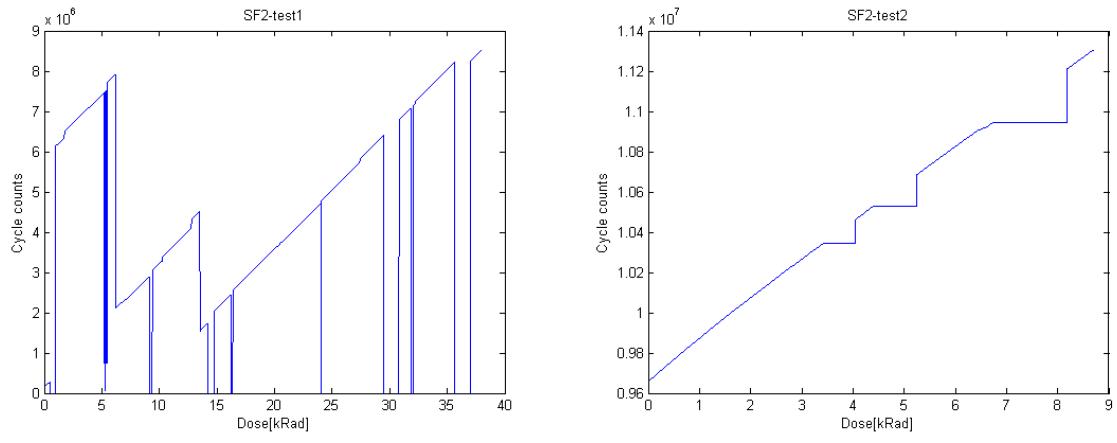


Figure A.2: SF2 - Cycles vs dose

In Figure A.4, A.5 A.6 you can see graphs of flux vs time for the different test boards tested at OCL. The reason the graphs don't go as linear as one would expect, is that the cyclotron wasn't as stable as one would expect, sometimes the beam stopped and had to restarted, and we sometimes we had sudden jumps in intensity. We also increased and decreased the intensities as we saw fitting, and that would also effect the graphs.



(a) Cycle counter versus dose for SF2 test1

(b) Cycle counter versus dose for SF2 test2

Figure A.3: SF2 - cycles vs dose

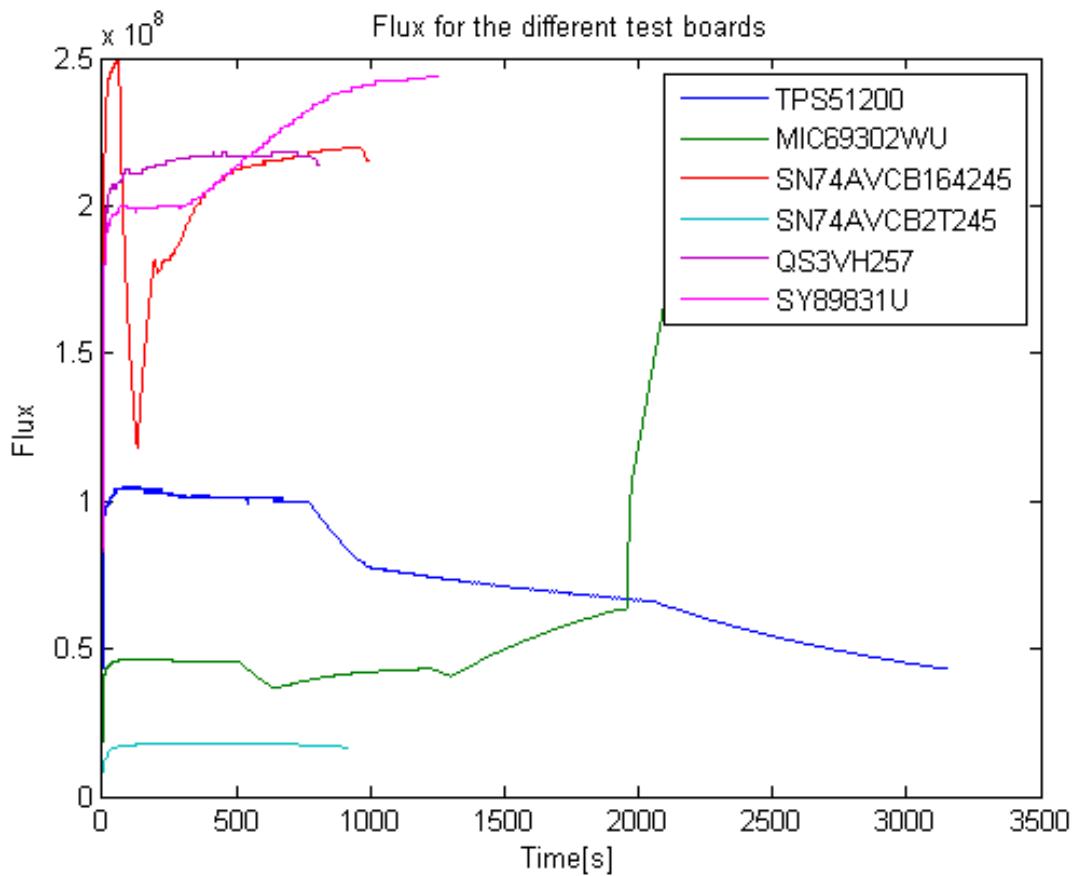


Figure A.4: flux for components radiated 15.11.2013

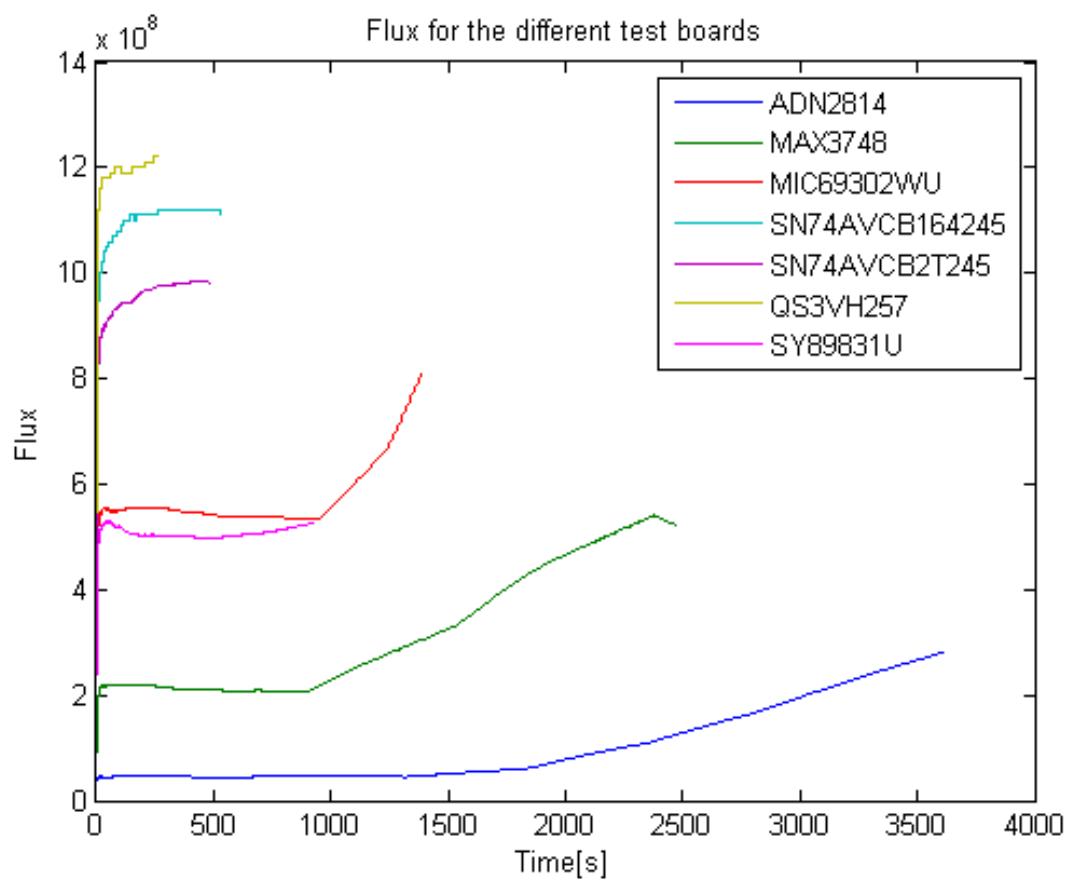


Figure A.5: flux for components radiated 28.11.2013

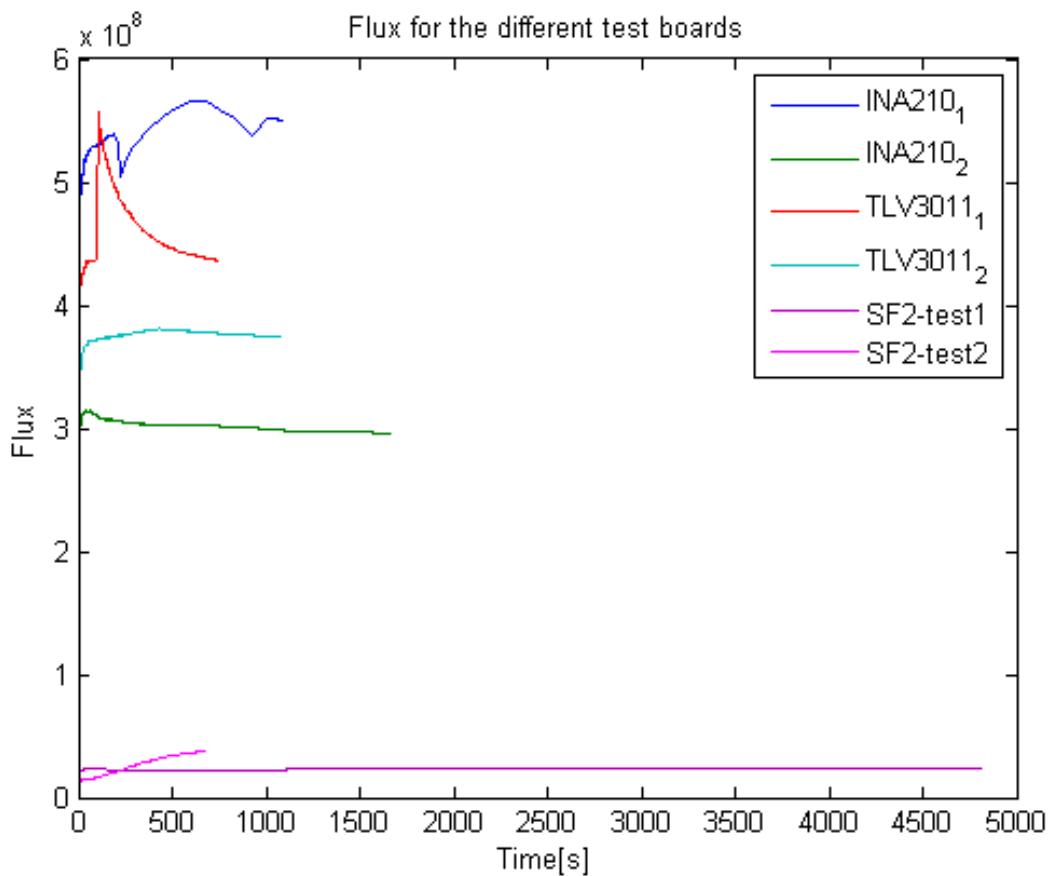


Figure A.6: flux for components radiated 09.04.2014

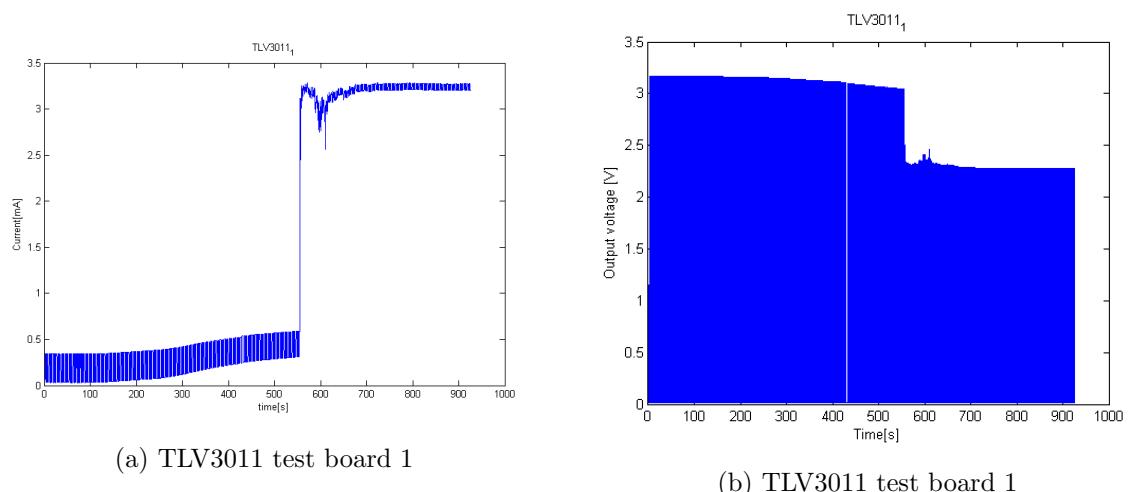


Figure A.7: TLV3011 - Current and voltage as function of dose

### A.3 Radiation Results from TSL

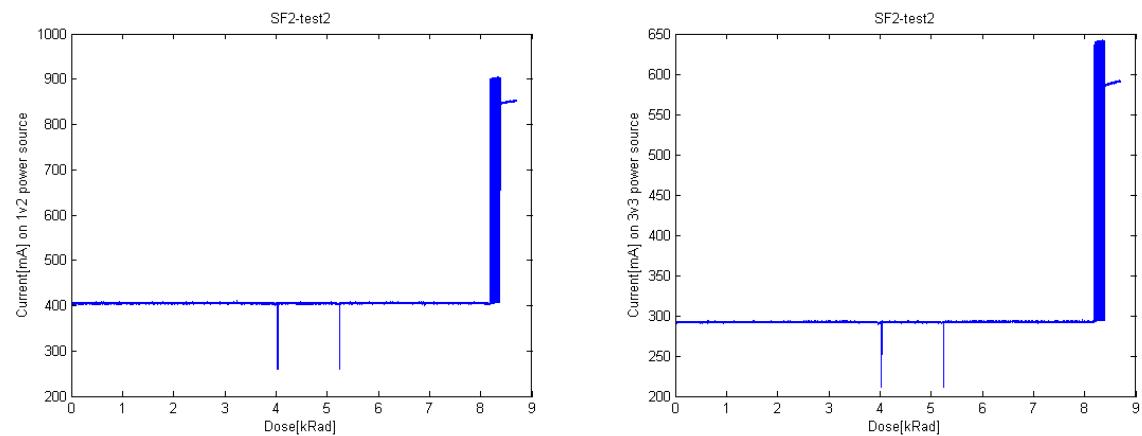


Figure A.8: SF2 - Current vs dose

## **Appendix B**

### **Current measurement board tutorial**

# Acronyms

<b>CERN</b>	European Council for Nuclear Research
<b>ALICE</b>	A Large Ion Collider Experiment
<b>OCL</b>	Oslo Cyclotron Laboratory
<b>DUT</b>	Device Under Test
<b>RCU</b>	Readout Control Unit
<b>LHC</b>	Large Hadron Collider
<b>FEE</b>	Front End Electronics
<b>FEC</b>	Front End Card
<b>FPGA</b>	Field Programmable Gate Array
<b>SEE</b>	Single Event Effects
<b>SEU</b>	Single Event Upset
<b>SET</b>	Single Event Transient
<b>SEL</b>	Single Event Latchup
<b>PCB</b>	Printed Circuit Board
<b>LVDS</b>	Low-Voltage Differential Signaling
<b>DAQ</b>	Data Acquisition
<b>SF2</b>	SmartFusion2
<b>CML</b>	Current-Mode Logic
<b>TPC</b>	Time Projection Chamber
<b>SRAM</b>	Static Random Access Memory
<b>TID</b>	Total Ionizing Dose

**ADC** Analog to Digital Converter

**LET** Linear Energy Transfer

**SoC** System On a Chip

**DCS** Control System board

**SIU** Source Interface Unit

**TSL** The Svedberg Laboratory

**WSR** Windowed Shift Register

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