

**RN0190**

**MiV\_RV32IMAF\_L1\_AHB v2.0 Release Notes**





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# 1 Revision History

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The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

## 1.1 Revision 1.0

Revision 1.0 is the first publication of this document. Created for MiV\_RV32IMAF\_L1\_AHB v2.0.

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## 2 MiV\_RV32IMAF\_L1\_AHB v2.0 Release Notes

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### 2.1 Overview

These release notes accompany the production release of MiV\_RV32IMAF\_L1\_AHB v2.0. This document provides details about the features, enhancements, system requirements, supported families, implementations, known issues, and workarounds.

### 2.2 Features

- Designed for low power ASIC microcontroller and FPGA soft-core implementations
- Integrated 8Kbytes instructions cache and 8 Kbytes data cache
- A Platform-Level Interrupt Controller (PLIC) can support up to 31 programmable interrupt with a single priority level
- Supports the RISC-V standard RV32IMAF ISA
- On-Chip debug unit with a JTAG interface
- Two external AHB interfaces for IO and memory

### 2.3 Delivery Types

MiV\_RV32IMAF\_L1\_AHB does not require license. Complete RTL source code is provided for the core.

### 2.4 Supported Families

- PolarFire®
- RTG4™
- IGLOO®2
- SmartFusion®2

### 2.5 Supported Tool Flows

MiV\_RV32IMAF\_L1\_AHB requires Libero® System-on-Chip (SoC) software v11.8 or later.

### 2.6 Installation Instructions

The MiV\_RV32IMAF\_L1\_AHB CPZ must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the **Add Core** catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project.

Refer to the [Libero SoC Online Help](#) for further instructions on core installation, licensing, and general use.

## 2.7 Documentation

This release contains a copy of the *MiV\_RV32IMAF\_L1\_AHB Handbook*. The handbook, describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also implementation suggestions. Refer to the [Libero SoC Online Help](#) for instructions on obtaining IP documentation.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

<http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores>.

## 2.8 Supported Test Environments

No testbench is provided with MiV\_RV32IMAF\_L1\_AHB.

The MiV\_RV32IMAF\_L1\_AHB RTL can be used to simulate the processor executing a program using a standard Libero generated HDL testbench.

## 2.9 Resolved History

Table 1 lists the release history for MiV\_RV32IMAF\_L1\_AHB.

**Table 1 • Release History**

Version	Date	Changes
2.0	November, 2017	First Production release.

## 2.10 Known Limitations and Workarounds

Since this is first release. There are no known limitations and workarounds for MiV\_RV32IMAF\_L1\_AHB.