HYBRID CMOS-MEMRISTOR BASED LOGIC GATES DESIGN

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The creation of the most advanced logic systems requires the use of small, low-power devices with extremely high processing speeds. The Hybrid CMOS-Memristor notably satisfies these requirements and is a key component in digital circuit design. In this work, design, implementation, and performance evaluation of Hybrid CMOS-Memristor based logic gates, such as NOT, AND, NAND, OR, NOR, XOR, and XNOR, are presented via SPECTRE in Cadence Virtuoso. Herein, an optimized design of Hybrid CMOS-Memristor based logic gates have been drawn for a comparative analysis with the conventional 180-nm complementary metal oxide semiconductor (CMOS) technology. The area, power, and delay calculated from these combinational circuits are found to be reduced by more than 75%, 50%, and 60%, respectively, as compared to the conventional CMOS technology. The impact of multiple CMOS technology nodes (90 and 180 nm) on the power consumption at the chip-level logic circuit implementation has also been investigated. The adopted Hybrid CMOS-memristor based design significantly improves the performance of various logic designs, which makes it area and power efficient and enables a major breakthrough in designing various low-power, low-cost, ultrafast, and compact circuits.