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F			ASSEMBLY NOTES BLOCK 1. This is a static sensitive assembly- use static eliminating measures during assembly and handling. 2. Manufacture to IPC 610A workmanship standards. 3. Trim component leads within .062 from solder side of PWA with exception of indicated area, which must be trimmed to .010 +/- .010 4. Apply part number and serial number labels in areas shown. 5. Install item 19 (120-1032-001 heat sink as follows: A. Clean bottom surface of heat sink and mounting B. Apply sufficient amount of Item 21 (120-1031-001), epoxy tube, to bottom of heat sink. C. Apply Item 21, activator tube to mounting surface of Pentium Module D. Mount heat sink onto Pentium Module and allow to sit for 30 seconds. 6. Discard nylon washer supplied with Item 16 (120-9958-002)			FABRICATION NOTES BLOCK 1. MAT'L: Copper clad plated sheet per MIL-P-13949/4, Type GFM, A. Copper Weight: a) Outer Layers 1.5 OZ. b) Inner Plane Layers 1 OZ. c) Inner Signal Layers 1 OZ. B. Laminate using Pre-Preg Material Per MIL-P-13949/12, Type PC-GF. Tg minimum 170 deg C. 2. Overall Board thickness to be .093 +/- .009. 3. Unless otherwise specified all hole dimensions apply after plating. All plated through holes to have a minimum of .001 copper. 4. All holes shall be located within .003 diameter of true position. Layer to layer registration shall be within .005. All holes surrounded by land shall have a minimum annular ring of .001. Tangency on holes with breakout is acceptable. 5. Conductor widths and spacing shall be within +/- 20% of artwork originals. 6. Apply solder mask (liquid photo imageable) over bare copper, solder mask to be per IPC-SM-84D, Type B, Class 3, Color: Transparent Green. All exposed conductive surfaces to be solder coated. 7. Ware or twist of board shall not exceed .0075 inch per inch.			F																																												
E									E																																												
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C	PAGE DESCRIPTION: PAGE01:COVER PAGE PAGE02: LAYER MATERIALS AND STACK-UP PAGE03: PANELS AND ELEMENTS 1 PAGE04: PANELS AND ELEMENTS 2								C																																												
B	PCB MECHANICAL DETAILS: 1. PCB SIZE: 47.5 mm X 66.5 mm 2. PCB THICKNESS: 1.62 mm 3. NUMBER OF LAYERS: 4 4. IMPEDANCE CONTROL: NO		 <table><tr><td>DRAWN</td><td>DATE</td></tr><tr><td>Molganov A.A.</td><td>24.07.2024</td></tr><tr><td>ENGINEER</td><td>DATE</td></tr><tr><td>Molganov A.A.</td><td>24.07.2024</td></tr><tr><td>CHECKED</td><td>DATE</td></tr><tr><td>Molganov A.A.</td><td>24.07.2024</td></tr><tr><td>APPROVED</td><td>DATE</td></tr><tr><td>Vafaev A.R.</td><td>25.07.2024</td></tr><tr><td>ISSUED</td><td>DATE</td></tr><tr><td>Vafaev A.R.</td><td>01.09.2024</td></tr></table>			DRAWN	DATE	Molganov A.A.	24.07.2024	ENGINEER	DATE	Molganov A.A.	24.07.2024	CHECKED	DATE	Molganov A.A.	24.07.2024	APPROVED	DATE	Vafaev A.R.	25.07.2024	ISSUED	DATE	Vafaev A.R.	01.09.2024	<table><tr><td colspan="4">COVER PAGE</td></tr><tr><td colspan="4">TITLE</td></tr><tr><td colspan="4">ST-Link V3 (Based on STM32F723)</td></tr><tr><td>SIZE</td><td>CAGE CODE</td><td>DWG NO</td><td>REV</td></tr><tr><td>A3</td><td></td><td></td><td>A</td></tr><tr><td colspan="2">SCALE 1 : 1</td><td colspan="2">SHEET 1 OF 4</td></tr></table>			COVER PAGE				TITLE				ST-Link V3 (Based on STM32F723)				SIZE	CAGE CODE	DWG NO	REV	A3			A	SCALE 1 : 1		SHEET 1 OF 4		B
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A	<table><tr><td colspan="4">REVISION TIMELINE</td></tr><tr><td>REV</td><td>DESCRIPTION</td><td>DATE</td><td>APPROVED</td></tr><tr><td>1.0</td><td>Main release to PCB</td><td>24.07.2024</td><td>Molganov A.A.</td></tr></table>		REVISION TIMELINE				REV	DESCRIPTION	DATE	APPROVED	1.0	Main release to PCB	24.07.2024	Molganov A.A.							A																																
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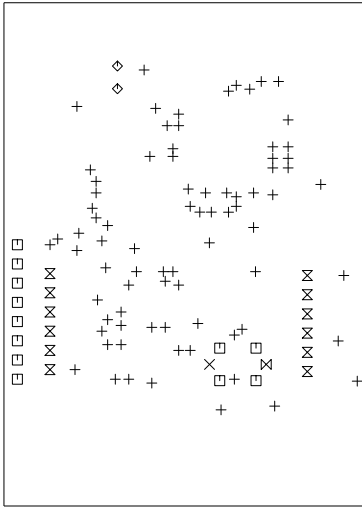
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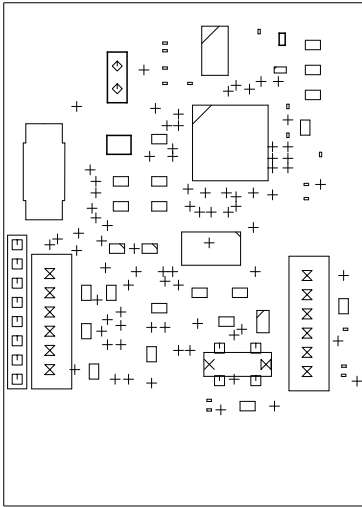
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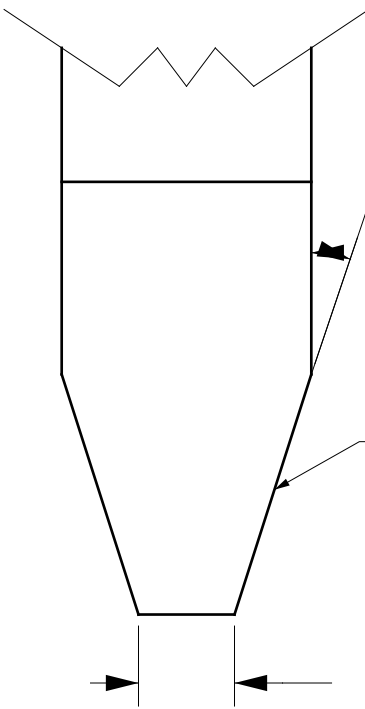
BOARD OUTLINE



DRILL PATTERN



PCB View



HOLE

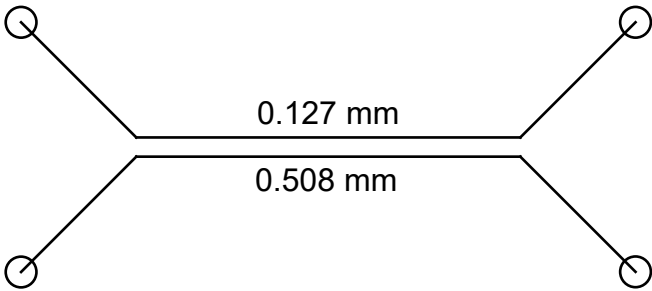
Drill Chart

Size	Sym	Qty	Plated	Tolerance
0.013	+	79	Yes	+0/-0.013
0.024	×	1	No	+/-0.002
0.028	□	12	Yes	+/-0.003
0.035	◇	2	No	+/-0.002
0.043	⊗	12	Yes	+/-0.003
0.046	⊗	1	No	+/-0.002
Total		107		

LAYER STACK-UP

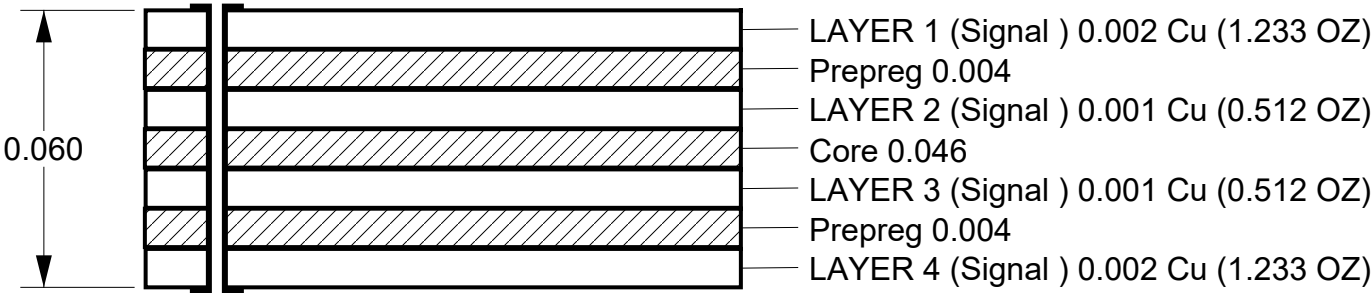
LAYER	COPPER
Signal (LAYER 1)	1.233 OZ
Signal (LAYER 2)	0.512 OZ
Signal (LAYER 3)	0.512 OZ
Signal (LAYER 4)	1.233 OZ

	LAYER 1 (Signal) 0.002 Cu (1.233 OZ)
	Prepreg 0.004
	LAYER 2 (Signal) 0.001 Cu (0.512 OZ)
	Core 0.046
	LAYER 3 (Signal) 0.001 Cu (0.512 OZ)
	Prepreg 0.004
	LAYER 4 (Signal) 0.002 Cu (1.233 OZ)




SCALE: NONE
TRACE WIDTH

VIA STACK-UP



PCB Materials Table

Material Name	Material Type	Qty
COPPER	Conductor	4
FR-4	Dielectric PrePreg	3

		LAYER MATERIALS AND STACK-UP			
DRAWN Molganov A.A.	DATE 24.07.2024	TITLE ST-Link V3 (Based on STM32F723)			
ENGINEER Molganov A.A.	DATE 24.07.2024				
CHECKED Molganov A.A.	DATE 24.07.2024				
APPROVED Vafaev A.R.	DATE 25.07.2024	SIZE A3	CAGE CODE	DWG NO	REV A
ISSUED Vafaev A.R.	DATE 01.09.2024	SCALE 1 : 1		SHEET 2 OF 4	

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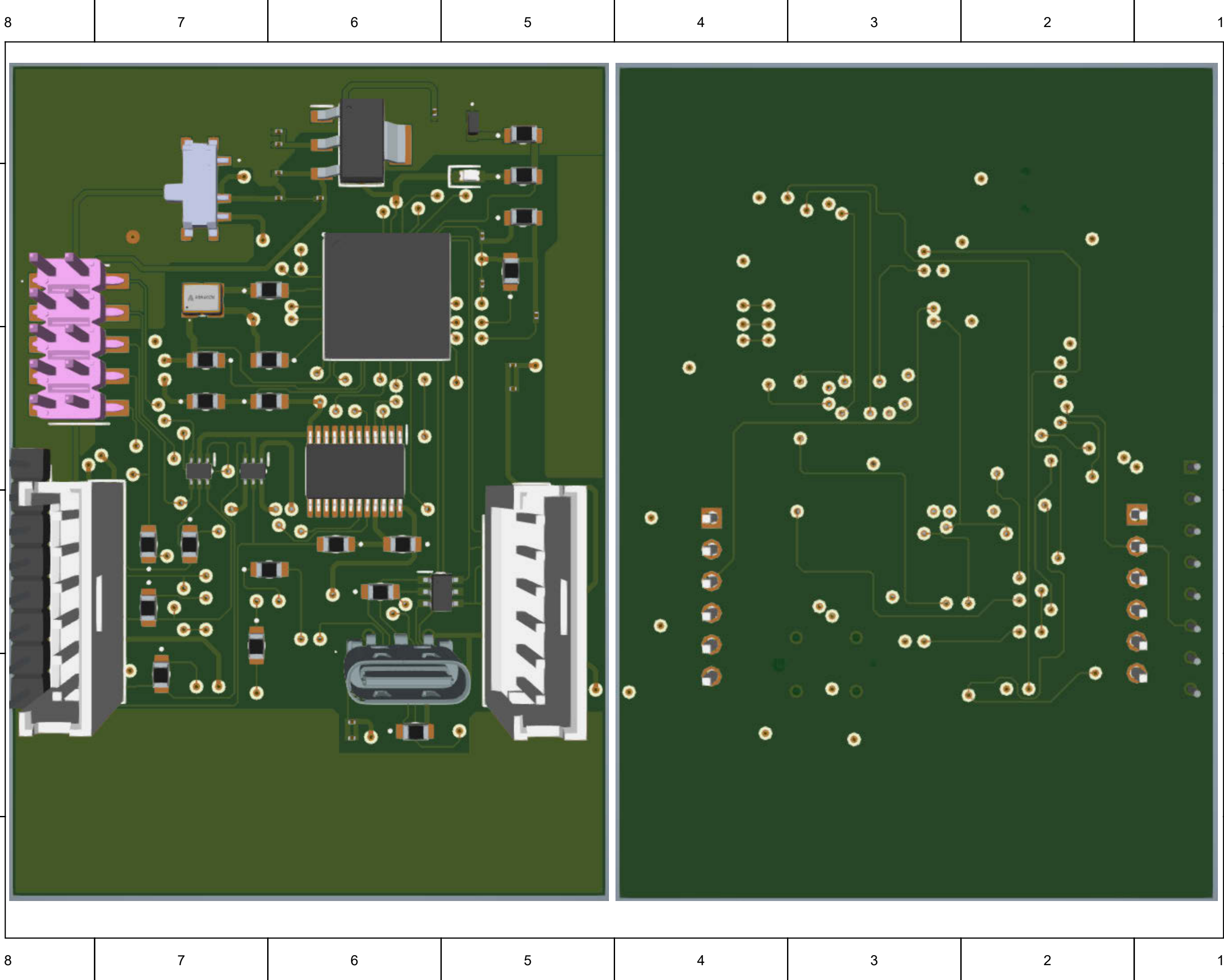
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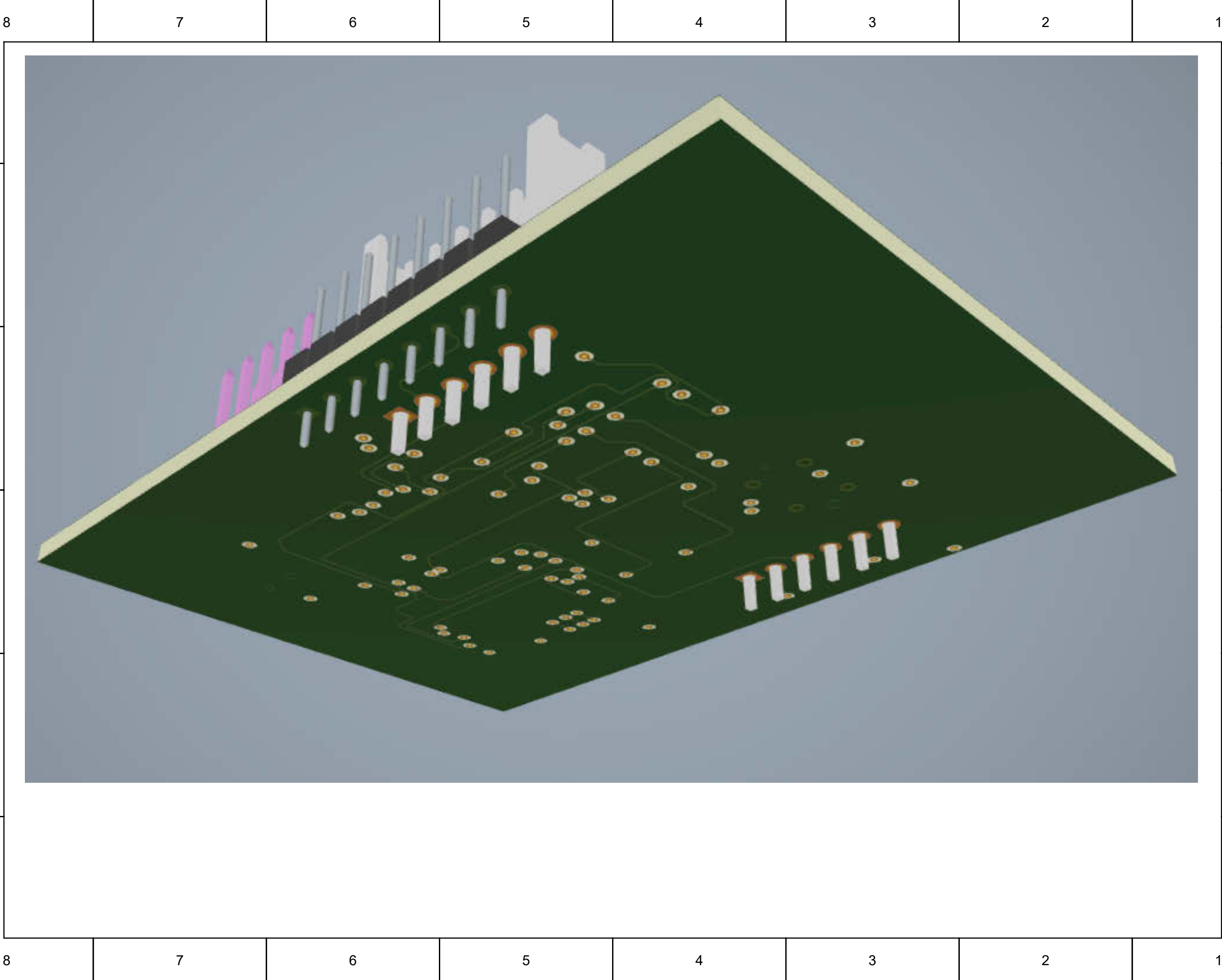
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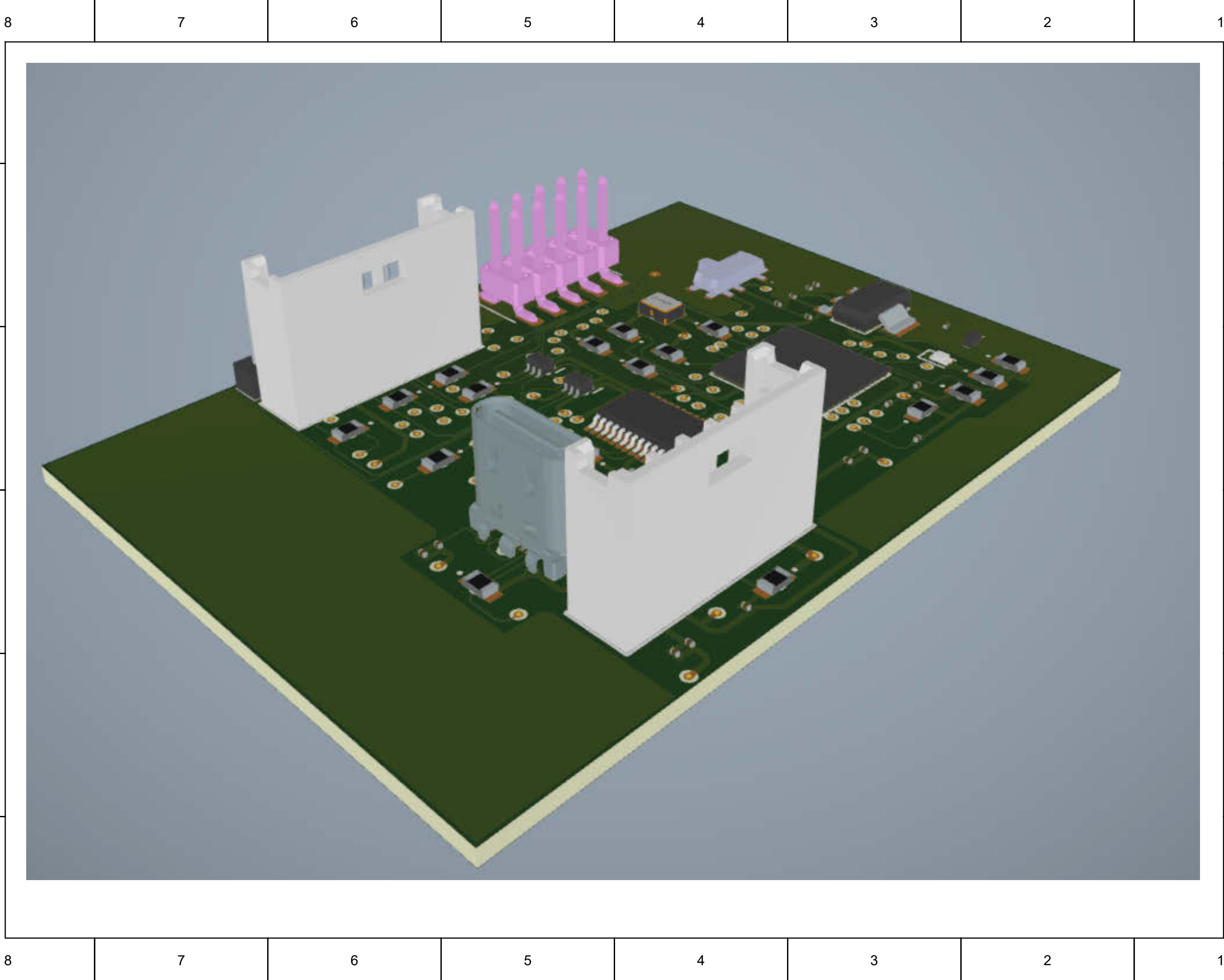
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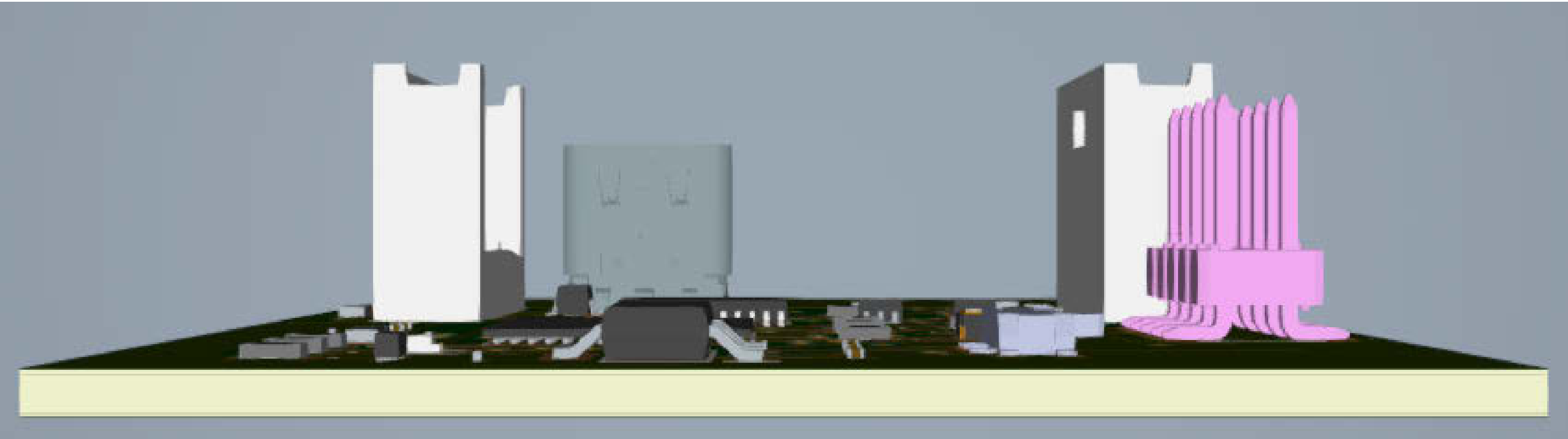
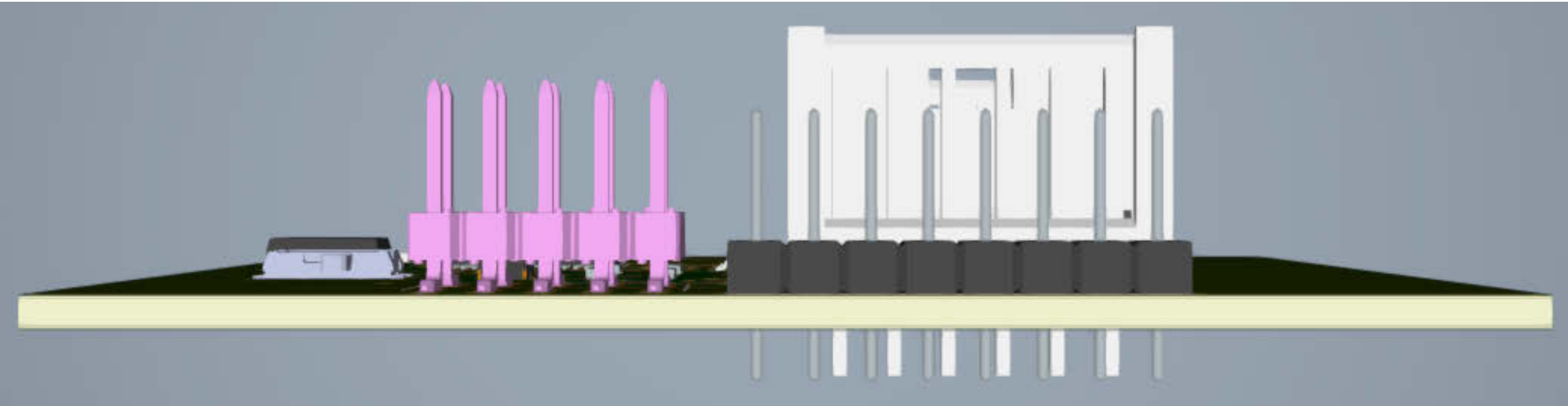
A

[illegible]







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