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F			ASSEMBLY NOTES BLOCK 1. This is a static sensitive assembly- use static eliminating measures during assembly and handling. 2. Manufacture to IPC 610A workmanship standards. 3. Trim component leads within .062 from solder side of PWA with exception of indicated area, which must be trimmed to .010 +/- .010 4. Apply part number and serial number labels in areas shown. 5. Install item 19 (120-1032-001 heat sink as follows: A. Clean bottom surface of heat sink and mounting B. Apply sufficient amount of Item 21 (120-1031-001), epoxy tube, to bottom of heat sink. C. Apply Item 21, activator tube to mounting surface of Pentium Module D. Mount heat sink onto Pentium Module and allow to sit for 30 seconds. 6. Discard nylon washer supplied with Item 16 (120-9958-002)			FABRICATION NOTES BLOCK 1. MAT'L: Copper clad plated sheet per MIL-P-13949/4, Type GFM, A. Copper Weight: a) Outer Layers 1.5 OZ. b) Inner Plane Layers 1 OZ. c) Inner Signal Layers 1 OZ. B. Laminate using Pre-Preg Material Per MIL-P-13949/12, Type PC-GF. Tg minimum 170 deg C. 2. Overall Board thickness to be .093 +/- .009. 3. Unless otherwise specified all hole dimensions apply after plating. All plated through holes to have a minimum of .001 copper. 4. All holes shall be located within .003 diameter of true position. Layer to layer registration shall be within .005. All holes surrounded by land shall have a minimum annular ring of .001. Tangency on holes with breakout is acceptable. 5. Conductor widths and spacing shall be within +/- 20% of artwork originals. 6. Apply solder mask (liquid photo imageable) over bare copper, solder mask to be per IPC-SM-84D, Type B, Class 3, Color: Transparent Green. All exposed conductive surfaces to be solder coated. 7. Ware or twist of board shall not exceed .0075 inch per inch.			F																																													
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D									D																																													
C	PAGE DESCRIPTION: PAGE01:COVER PAGE PAGE02: LAYER MATERIALS AND STACK-UP PAGE03: PANELS AND ELEMENTS 1 PAGE04: PANELS AND ELEMENTS 2					 <table><tr><td>Cadence</td><td>Capture CIS 23.10.005</td></tr><tr><td>Cadence</td><td>PCB Editor 23.10.005</td></tr><tr><td>TRADEMARK</td><td>USED ON</td></tr><tr><td colspan="2">APPLICATION</td></tr></table>			Cadence	Capture CIS 23.10.005	Cadence	PCB Editor 23.10.005	TRADEMARK	USED ON	APPLICATION		C																																					
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B	PCB MECHANICAL DETAILS: 1. PCB SIZE: 47.5 mm X 66.5 mm 2. PCB THICKNESS: 1.62 mm 3. NUMBER OF LAYERS: 4 4. IMPEDANCE CONTROL: NO		 <table><tr><td>DRAWN</td><td>DATE</td><td colspan="2">COVER PAGE</td></tr><tr><td>Molganov A.A.</td><td>24.07.2024</td><td colspan="2" rowspan="3">TITLE ST-Link V3 (Based on STM32F723)</td></tr><tr><td>ENGINEER</td><td>DATE</td></tr><tr><td>Molganov A.A.</td><td>24.07.2024</td></tr><tr><td>CHECKED</td><td>DATE</td><td>SIZE</td><td>CAGE CODE</td><td>DWG NO</td><td>REV</td></tr><tr><td>Molganov A.A.</td><td>24.07.2024</td><td>A3</td><td></td><td></td><td>A</td></tr><tr><td>APPROVED</td><td>DATE</td><td colspan="2">SCALE 1 : 1</td><td colspan="2">SHEET 1 OF 4</td></tr><tr><td>Vafaev A.R.</td><td>25.07.2024</td><td colspan="2"></td><td colspan="2"></td></tr><tr><td>ISSUED</td><td>DATE</td><td colspan="2"></td><td colspan="2"></td></tr><tr><td>Vafaev A.R.</td><td>01.09.2024</td><td colspan="2"></td><td colspan="2"></td></tr></table>			DRAWN	DATE	COVER PAGE		Molganov A.A.	24.07.2024	TITLE ST-Link V3 (Based on STM32F723)		ENGINEER	DATE	Molganov A.A.	24.07.2024	CHECKED	DATE	SIZE	CAGE CODE	DWG NO	REV	Molganov A.A.	24.07.2024	A3			A	APPROVED	DATE	SCALE 1 : 1		SHEET 1 OF 4		Vafaev A.R.	25.07.2024					ISSUED	DATE					Vafaev A.R.	01.09.2024					B
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A	<table><tr><th colspan="4">REVISION TIMELINE</th></tr><tr><th>REV</th><th>DESCRIPTION</th><th>DATE</th><th>APPROVED</th></tr><tr><td>1.0</td><td>Main release to PCB</td><td>24.07.2024</td><td>Molganov A.A.</td></tr></table>		REVISION TIMELINE				REV	DESCRIPTION	DATE	APPROVED	1.0	Main release to PCB	24.07.2024	Molganov A.A.							A																																	
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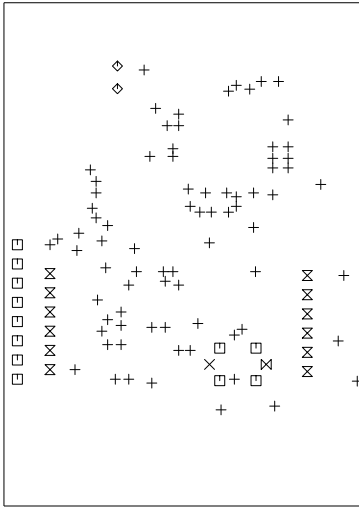
3

2

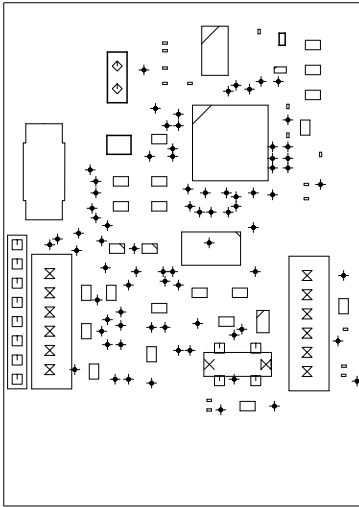
1



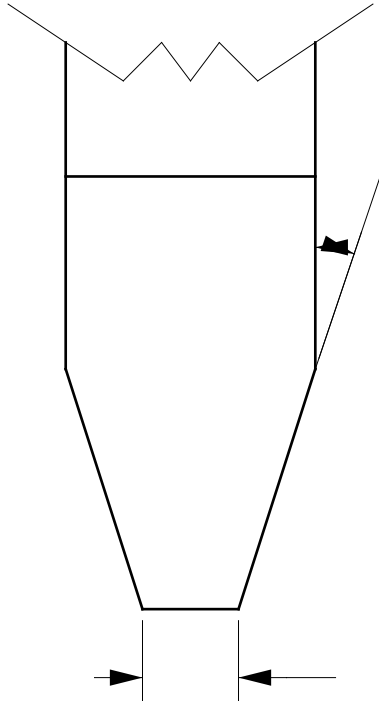
BOARD OUTLINE



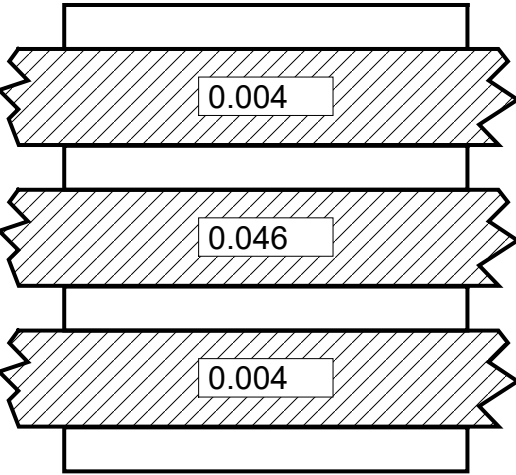
DRILL PATTERN



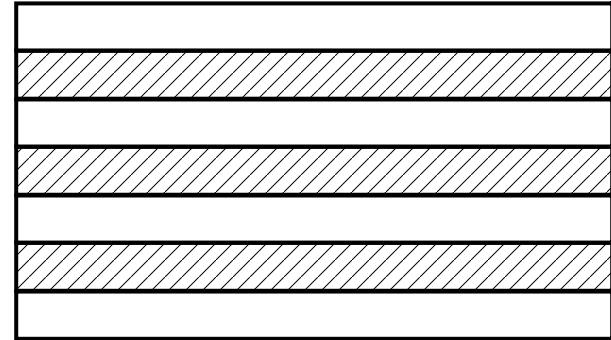
PCB View



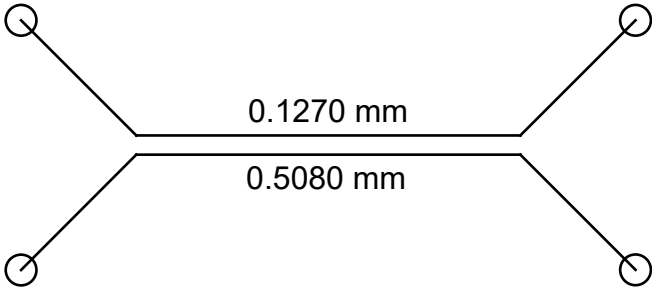
Drill Chart				
Size	Sym	Qty	Plated	Tolerance
0.013	+	78	Yes	+0/-0.013
0.024	×	1	No	+/-0.002
0.028	□	12	Yes	+/-0.003
0.035	◇	2	No	+/-0.002
0.043	⊗	12	Yes	+/-0.003
0.046	⊗	1	No	+/-0.002
Total		106		



LAYER	COPPER
Signal (LAYER 1)	1.233 OZ
Signal (LAYER 2)	0.512 OZ
Signal (LAYER 3)	0.512 OZ
Signal (LAYER 4)	1.233 OZ

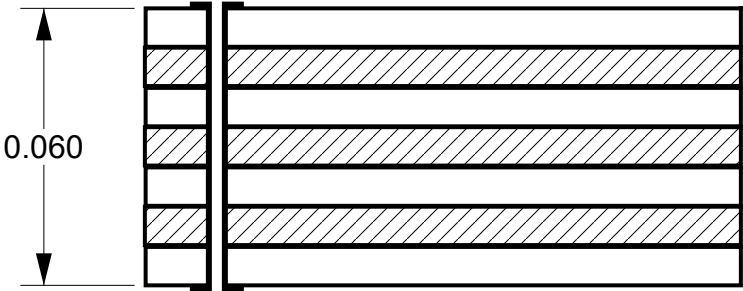


- LAYER 1 (Signal) 0.002 Cu (1.233 OZ)
- Prepreg 0.004
- LAYER 2 (Signal) 0.001 Cu (0.512 OZ)
- Core 0.046
- LAYER 3 (Signal) 0.001 Cu (0.512 OZ)
- Prepreg 0.004
- LAYER 4 (Signal) 0.002 Cu (1.233 OZ)




SCALE: NONE
TRACE WIDTH

VIA STACK-UP



- LAYER 1 (Signal) 0.002 Cu (1.233 OZ)
- Prepreg 0.004
- LAYER 2 (Signal) 0.001 Cu (0.512 OZ)
- Core 0.046
- LAYER 3 (Signal) 0.001 Cu (0.512 OZ)
- Prepreg 0.004
- LAYER 4 (Signal) 0.002 Cu (1.233 OZ)

PCB Materials Table		
Material Name	Material Type	Qty
COPPER	Conductor	4
FR-4	Dielectric PrePreg	3

		LAYER MATERIALS AND STACK-UP			
DRAWN Molganov A.A.	DATE 24.07.2024	TITLE ST-Link V3 (Based on STM32F723)			
ENGINEER Molganov A.A.	DATE 24.07.2024				
CHECKED Molganov A.A.	DATE 24.07.2024				
APPROVED Vafaev A.R.	DATE 25.07.2024	SIZE A3	CAGE CODE	DWG NO	REV A
ISSUED Vafaev A.R.	DATE 01.09.2024	SCALE 1 : 1		SHEET 2 OF 4	

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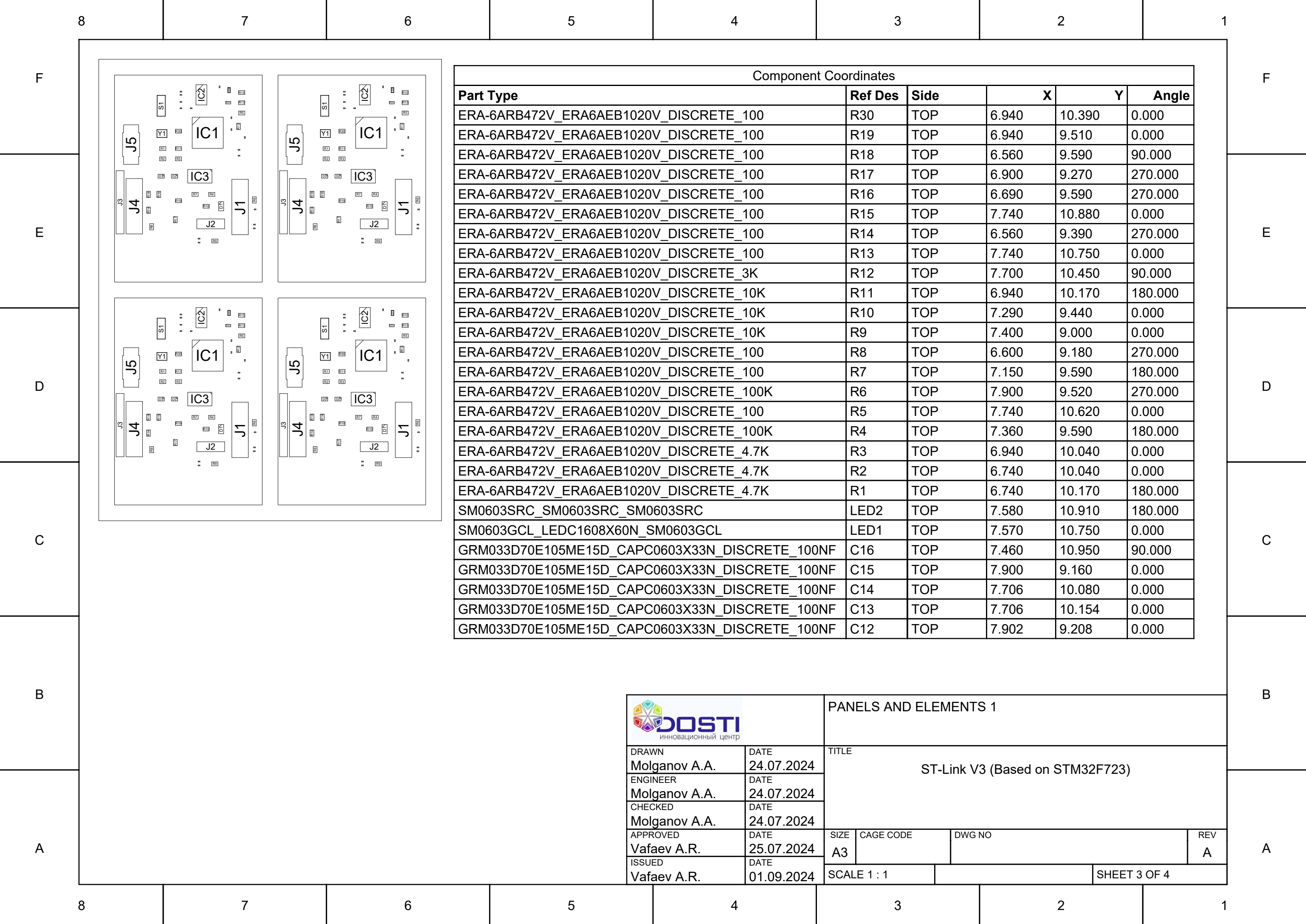
5

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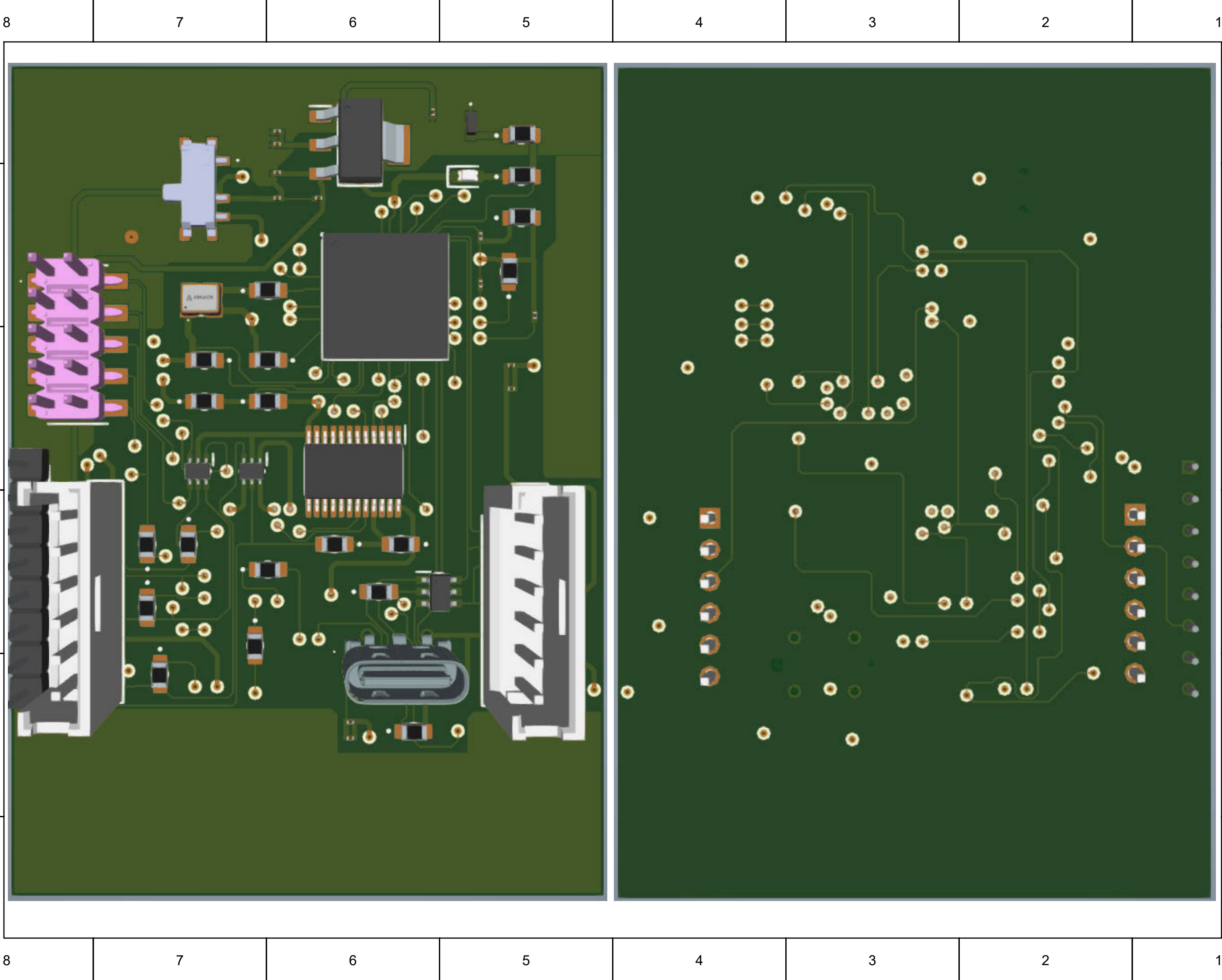
1

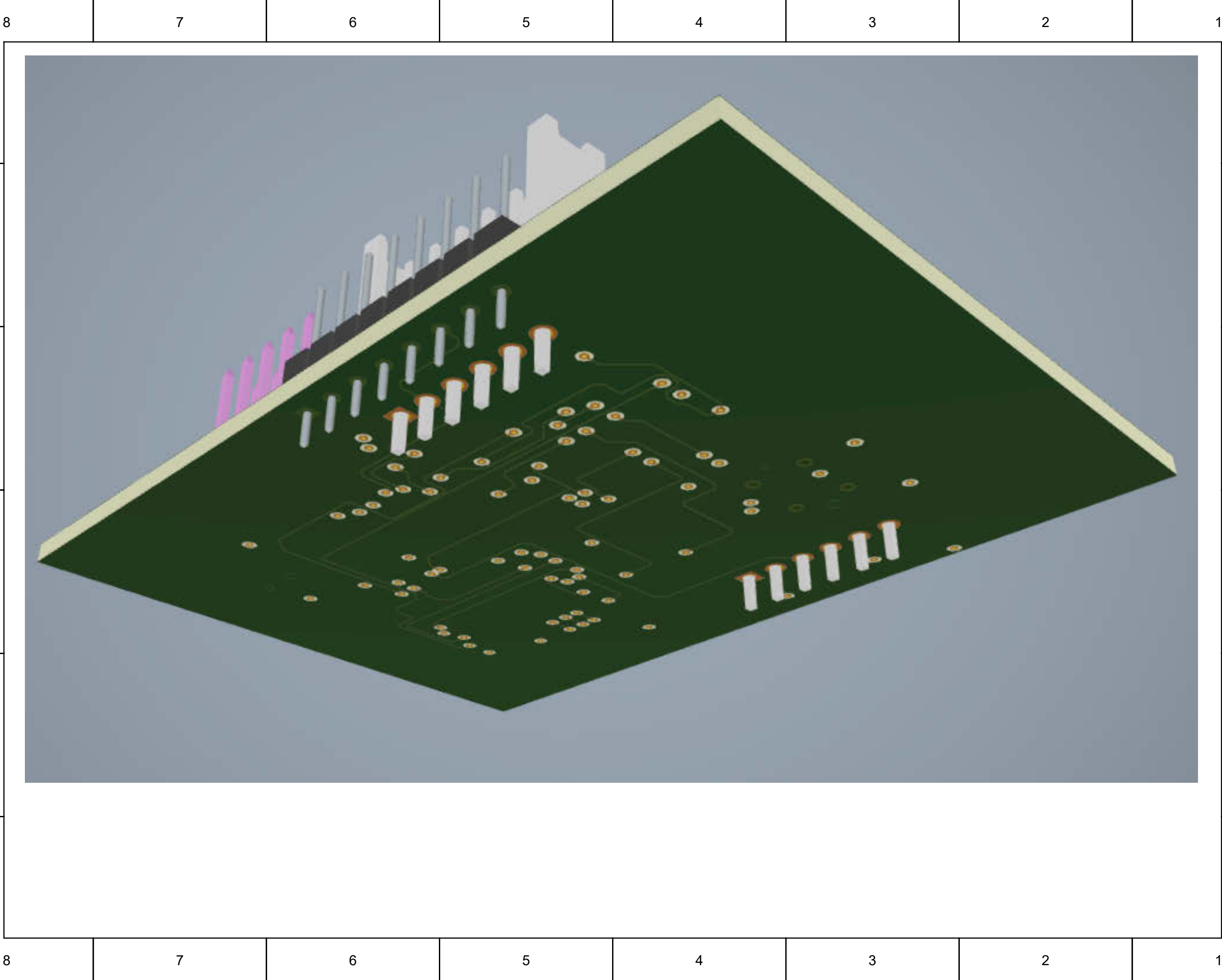


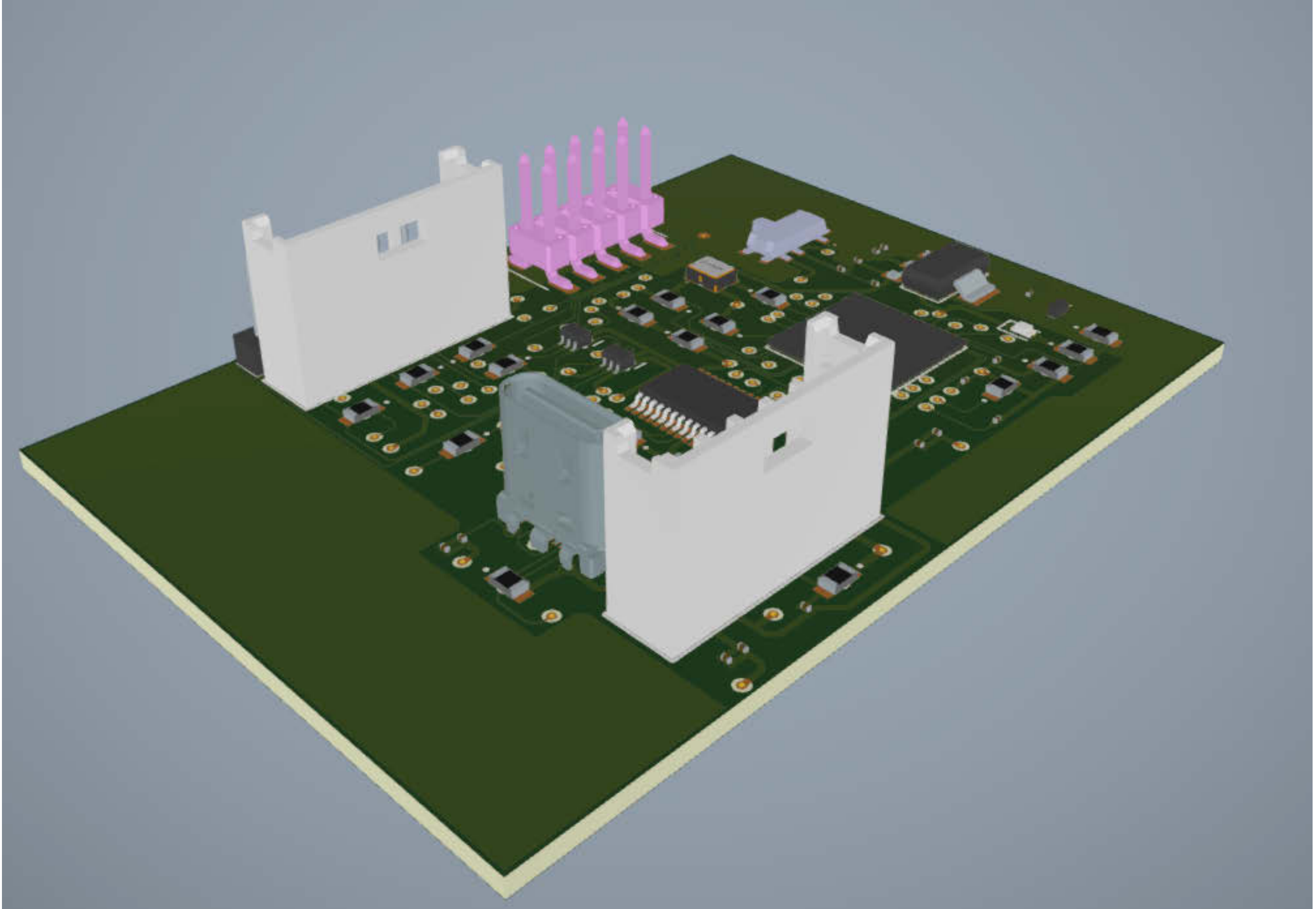
Component Coordinates					
Part Type	Ref Des	Side	X	Y	Angle
ERA-6ARB472V_ERA6AEB1020V_DISCRETE_100	R30	TOP	6.940	10.390	0.000
ERA-6ARB472V_ERA6AEB1020V_DISCRETE_100	R19	TOP	6.940	9.510	0.000
ERA-6ARB472V_ERA6AEB1020V_DISCRETE_100	R18	TOP	6.560	9.590	90.000
ERA-6ARB472V_ERA6AEB1020V_DISCRETE_100	R17	TOP	6.900	9.270	270.000
ERA-6ARB472V_ERA6AEB1020V_DISCRETE_100	R16	TOP	6.690	9.590	270.000
ERA-6ARB472V_ERA6AEB1020V_DISCRETE_100	R15	TOP	7.740	10.880	0.000
ERA-6ARB472V_ERA6AEB1020V_DISCRETE_100	R14	TOP	6.560	9.390	270.000
ERA-6ARB472V_ERA6AEB1020V_DISCRETE_100	R13	TOP	7.740	10.750	0.000
ERA-6ARB472V_ERA6AEB1020V_DISCRETE_3K	R12	TOP	7.700	10.450	90.000
ERA-6ARB472V_ERA6AEB1020V_DISCRETE_10K	R11	TOP	6.940	10.170	180.000
ERA-6ARB472V_ERA6AEB1020V_DISCRETE_10K	R10	TOP	7.290	9.440	0.000
ERA-6ARB472V_ERA6AEB1020V_DISCRETE_10K	R9	TOP	7.400	9.000	0.000
ERA-6ARB472V_ERA6AEB1020V_DISCRETE_100	R8	TOP	6.600	9.180	270.000
ERA-6ARB472V_ERA6AEB1020V_DISCRETE_100	R7	TOP	7.150	9.590	180.000
ERA-6ARB472V_ERA6AEB1020V_DISCRETE_100K	R6	TOP	7.900	9.520	270.000
ERA-6ARB472V_ERA6AEB1020V_DISCRETE_100	R5	TOP	7.740	10.620	0.000
ERA-6ARB472V_ERA6AEB1020V_DISCRETE_100K	R4	TOP	7.360	9.590	180.000
ERA-6ARB472V_ERA6AEB1020V_DISCRETE_4.7K	R3	TOP	6.940	10.040	0.000
ERA-6ARB472V_ERA6AEB1020V_DISCRETE_4.7K	R2	TOP	6.740	10.040	0.000
ERA-6ARB472V_ERA6AEB1020V_DISCRETE_4.7K	R1	TOP	6.740	10.170	180.000
SM0603SRC_SM0603SRC_SM0603SRC	LED2	TOP	7.580	10.910	180.000
SM0603GCL_LEDC1608X60N_SM0603GCL	LED1	TOP	7.570	10.750	0.000
GRM033D70E105ME15D_CAPC0603X33N_DISCRETE_100NF	C16	TOP	7.460	10.950	90.000
GRM033D70E105ME15D_CAPC0603X33N_DISCRETE_100NF	C15	TOP	7.900	9.160	0.000
GRM033D70E105ME15D_CAPC0603X33N_DISCRETE_100NF	C14	TOP	7.706	10.080	0.000
GRM033D70E105ME15D_CAPC0603X33N_DISCRETE_100NF	C13	TOP	7.706	10.154	0.000
GRM033D70E105ME15D_CAPC0603X33N_DISCRETE_100NF	C12	TOP	7.902	9.208	0.000

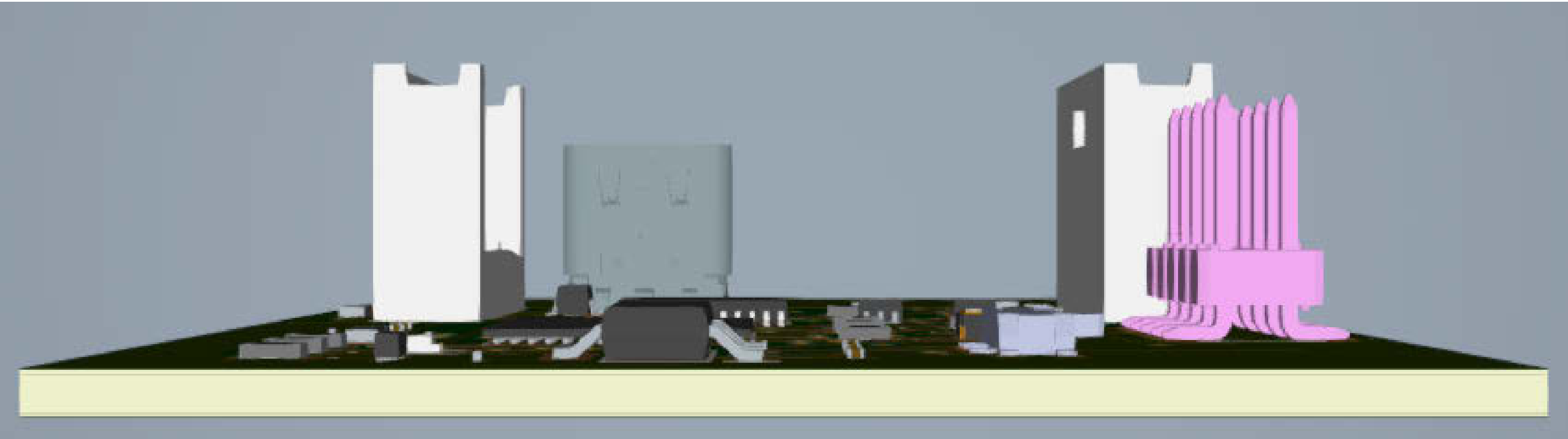
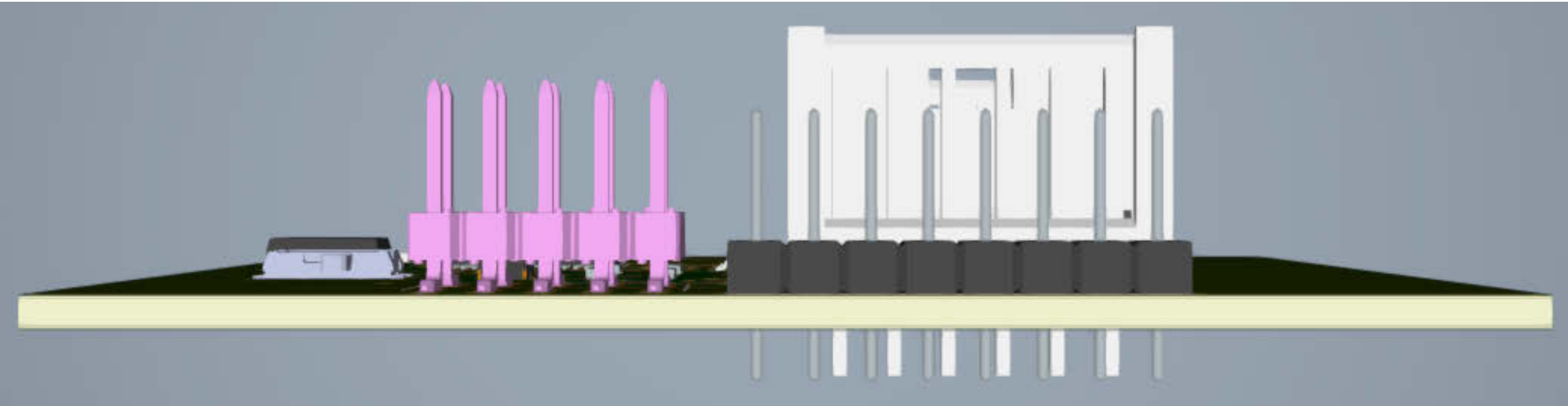
		PANELS AND ELEMENTS 1			
DRAWN Molganov A.A.	DATE 24.07.2024	TITLE ST-Link V3 (Based on STM32F723)			
ENGINEER Molganov A.A.	DATE 24.07.2024				
CHECKED Molganov A.A.	DATE 24.07.2024				
APPROVED Vafaev A.R.	DATE 25.07.2024	SIZE A3	CAGE CODE	DWG NO	REV A
ISSUED Vafaev A.R.	DATE 01.09.2024	SCALE 1 : 1		SHEET 3 OF 4	

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