RK3328

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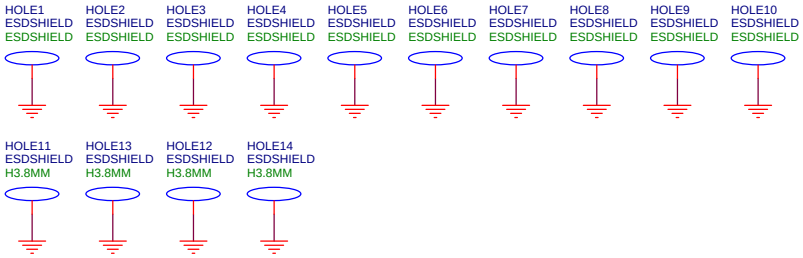


Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

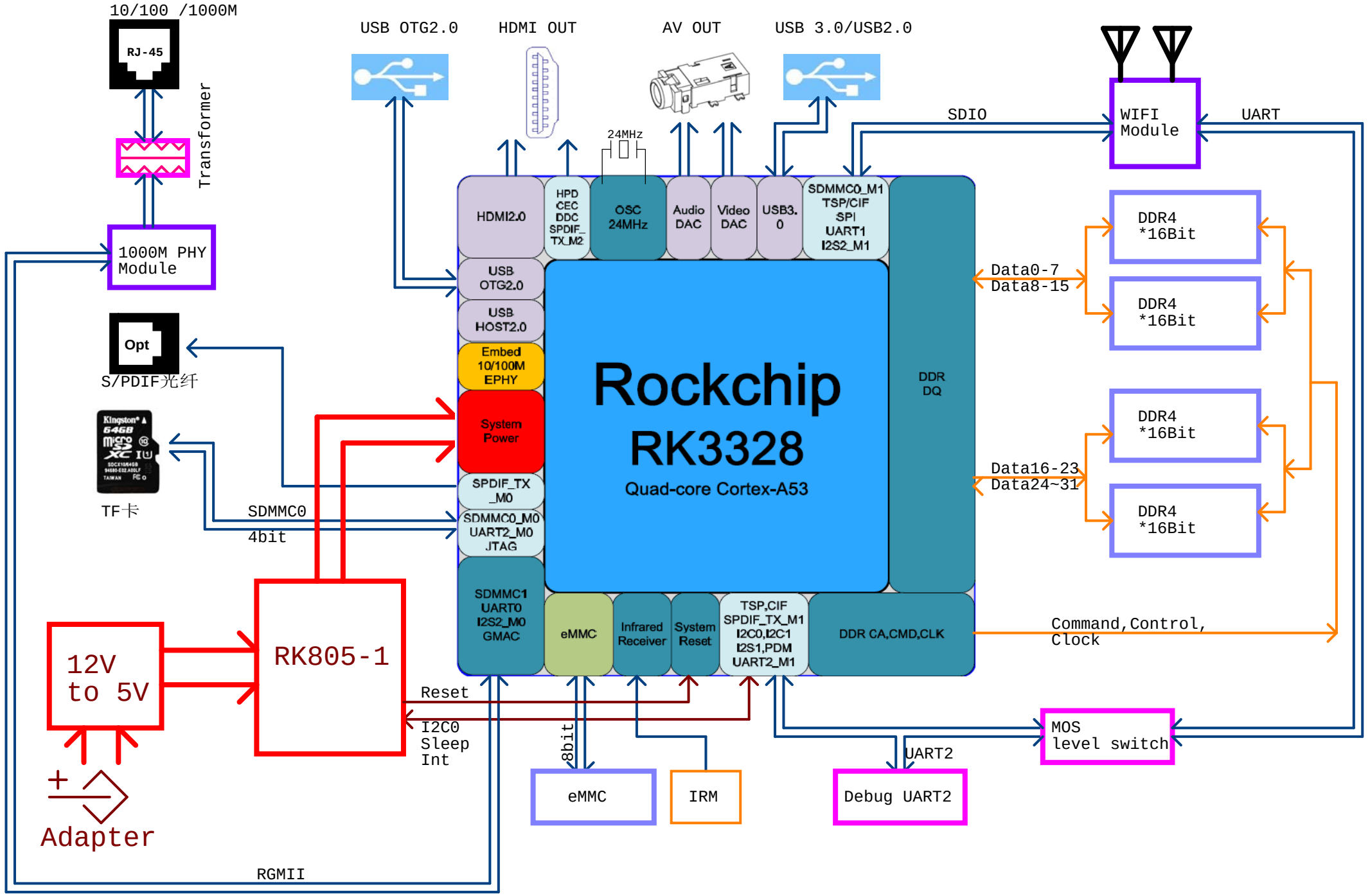
{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Note：
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Demo4		
File:	Index		
Date:	Tuesday, July 18, 2017	Rev:	V1.1
Designed by:	Zhangdz	Sheet:	1 of 24

Version	Date	Author	Change Note	Approved
V1.0	20170320	ZDZ	First edictor	
V1.1	20170718	ZDZ	1：修改记录请见：RK3328_BOX_DEMO4_RK805-1_DDR4P416DD6_V11_SCH_Modify_Notes	

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Demo4		
File:	Change List		
Date:	Tuesday, July 18, 2017	Rev:	V1.1
Designed by:	Zhangdz	Sheet:	2 of 24



Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics
Project:	RK3328_BOX_Demo4
File:	Block Diagram
Date:	Tuesday, July 18, 2017
Rev:	V1.1
Designed by:	Zhangdz
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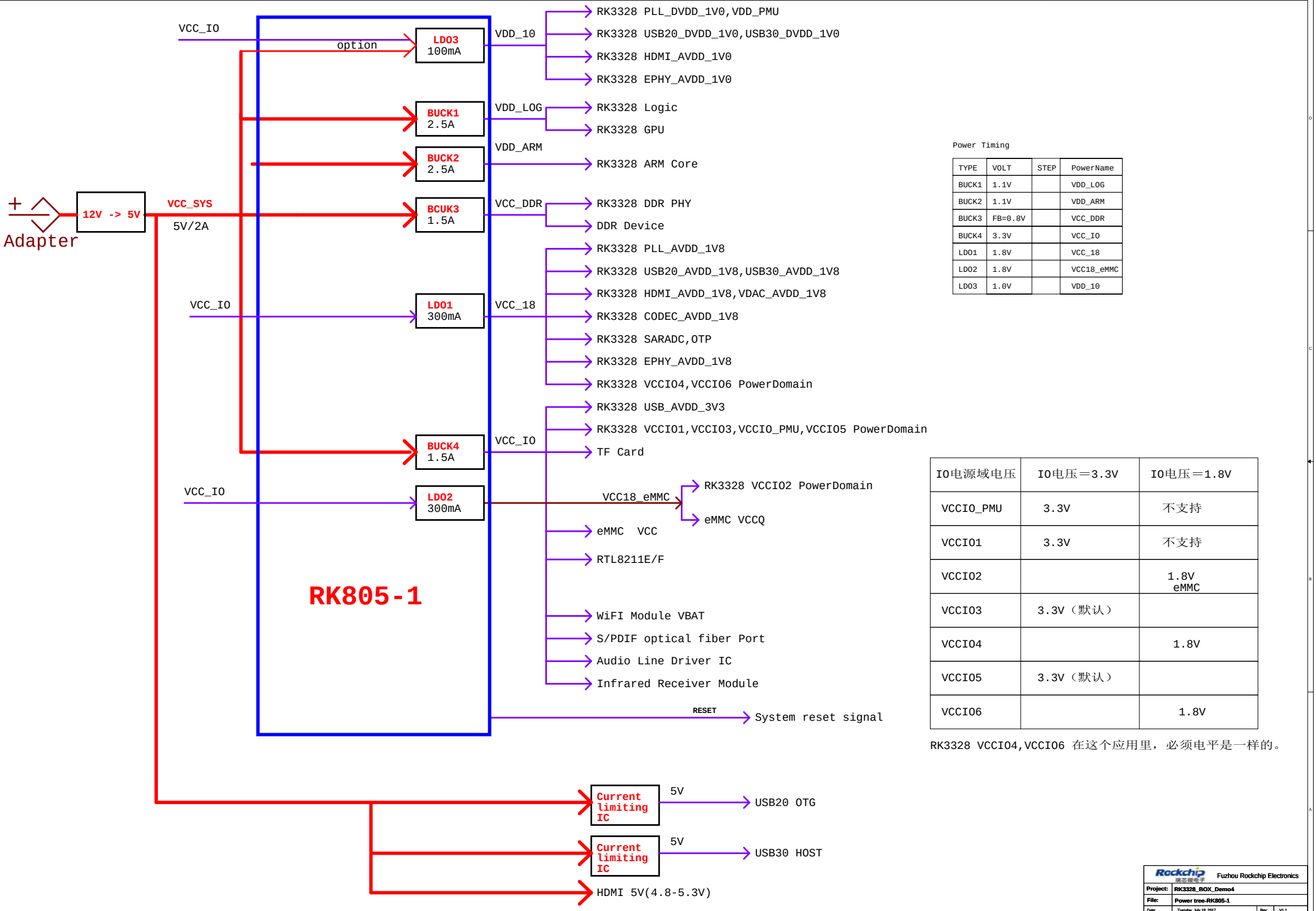

Power Timing

TYPE	VOLT	STEP	PowerName
BUCK1	1.1V		VDD_LOG
BUCK2	1.1V		VDD_ARM
BUCK3	FB=0.8V		VCC_DDR
BUCK4	3.3V		VCC_IO
LDO1	1.8V		VCC_18
LDO2	1.8V		VCC18_eMMC
LDO3	1.0V		VDD_10

IO电源域电压	IO电压＝3.3V	IO电压＝1.8V
VCCIO_PMU	3.3V	不支持
VCCIO1	3.3V	不支持
VCCIO2		1.8V eMMC
VCCIO3	3.3V（默认）	
VCCIO4		1.8V
VCCIO5	3.3V（默认）	
VCCIO6		1.8V

RK3328 VCCIO4,VCCIO6 在这个应用里，必须电平是一样的。

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics
Project:	RK3328_BOX_Demo4
File:	Power tree-RK805-1
Date:	Tuesday, July 18, 2017
Rev:	V1.1
Designed by:	Zhangzb
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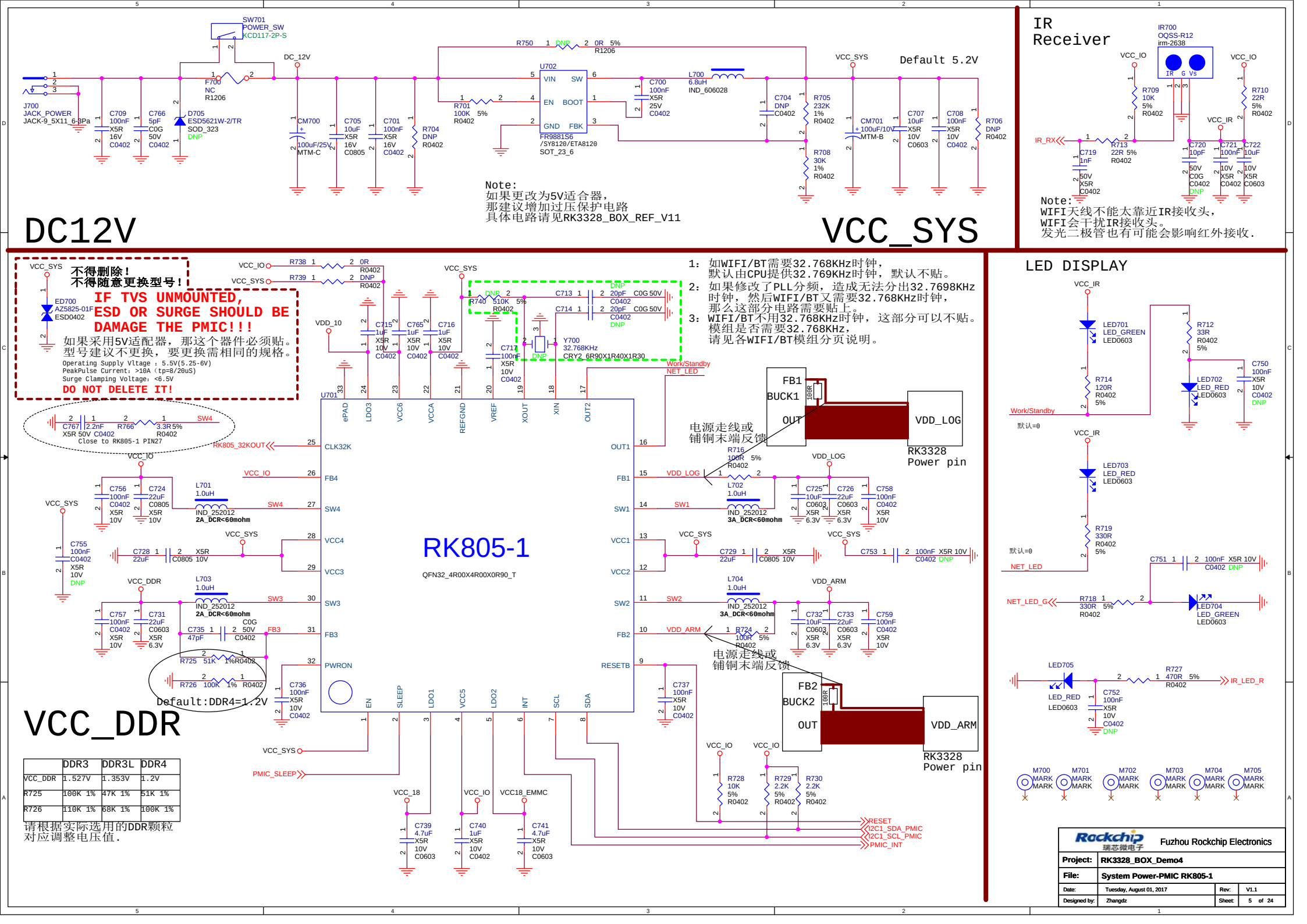
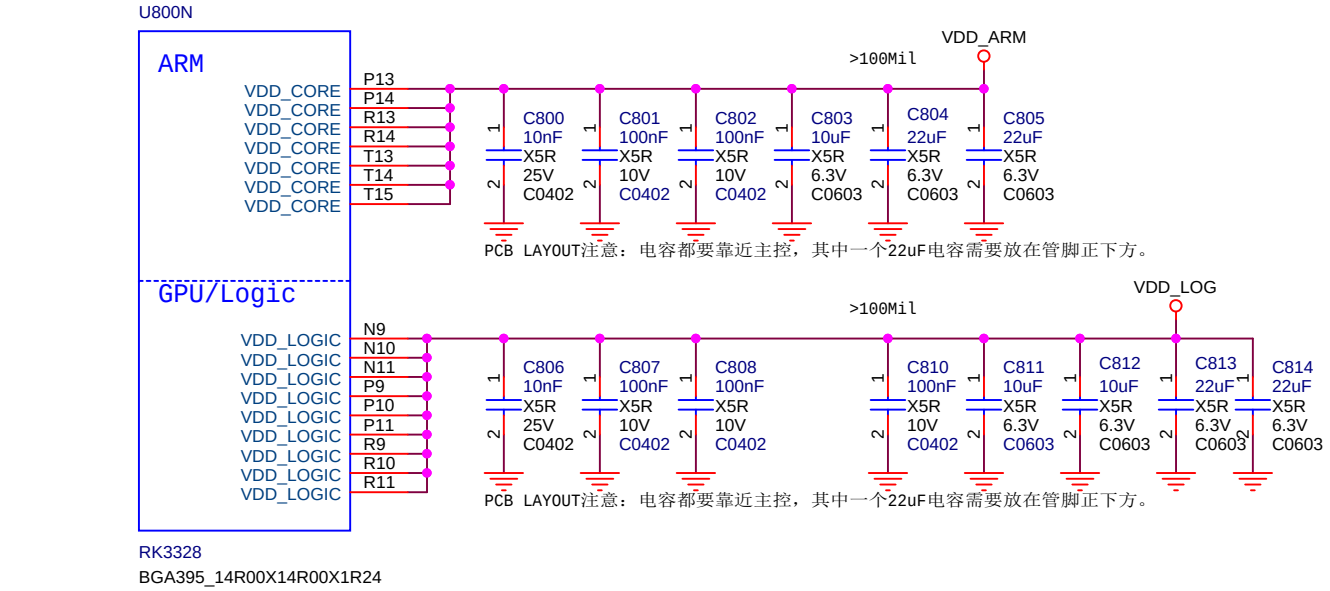
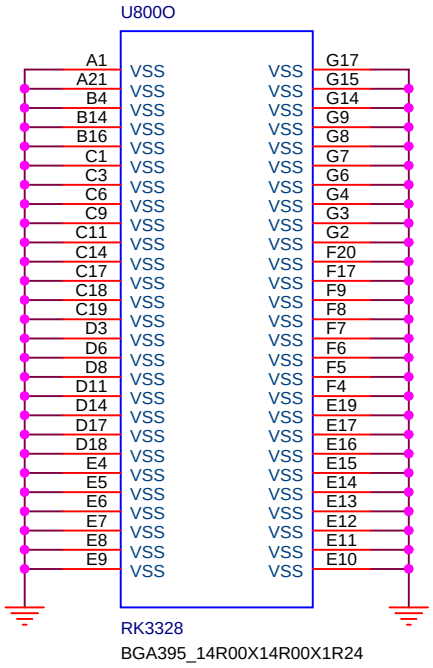
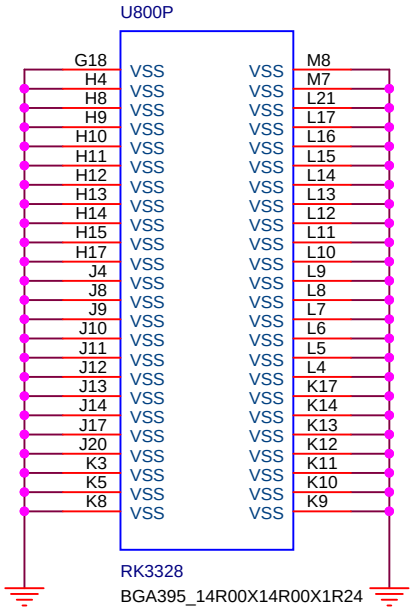
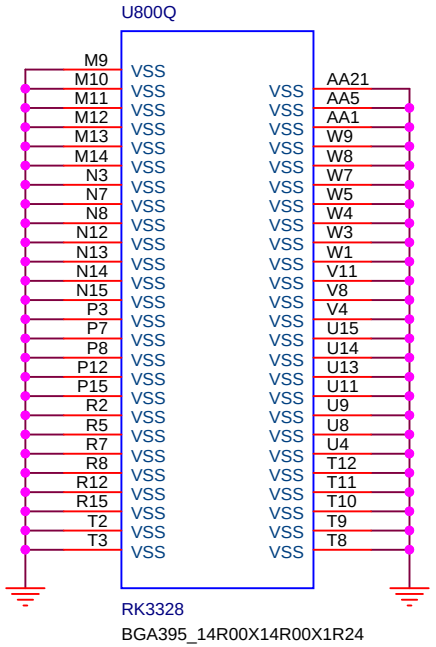


	DDR3	DDR3L	DDR4
VCC_DDR	1.527V	1.353V	1.2V
R725	100K 1%	47K 1%	51K 1%
R726	110K 1%	68K 1%	100K 1%

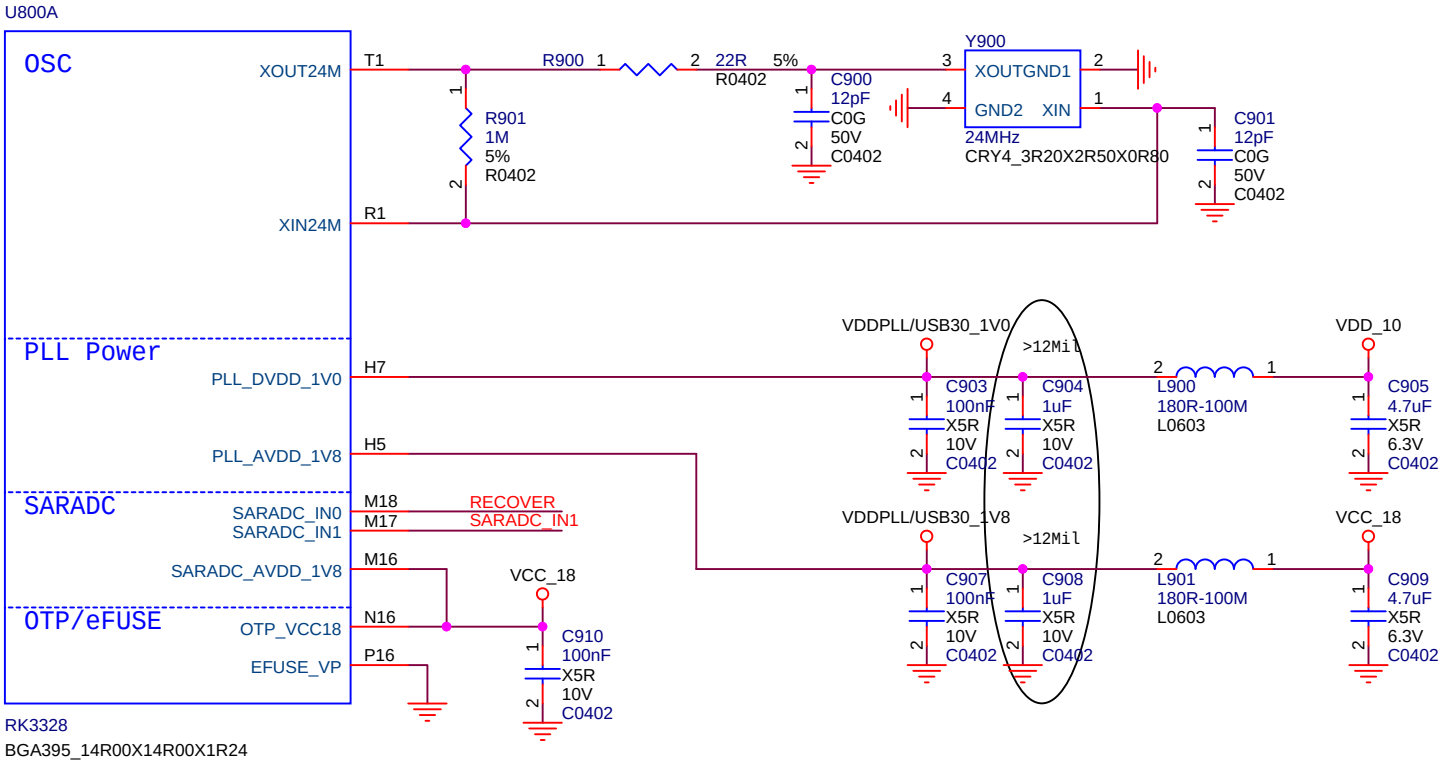


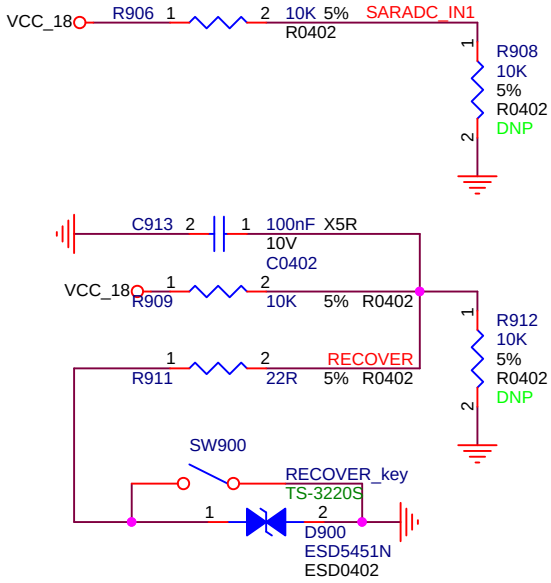






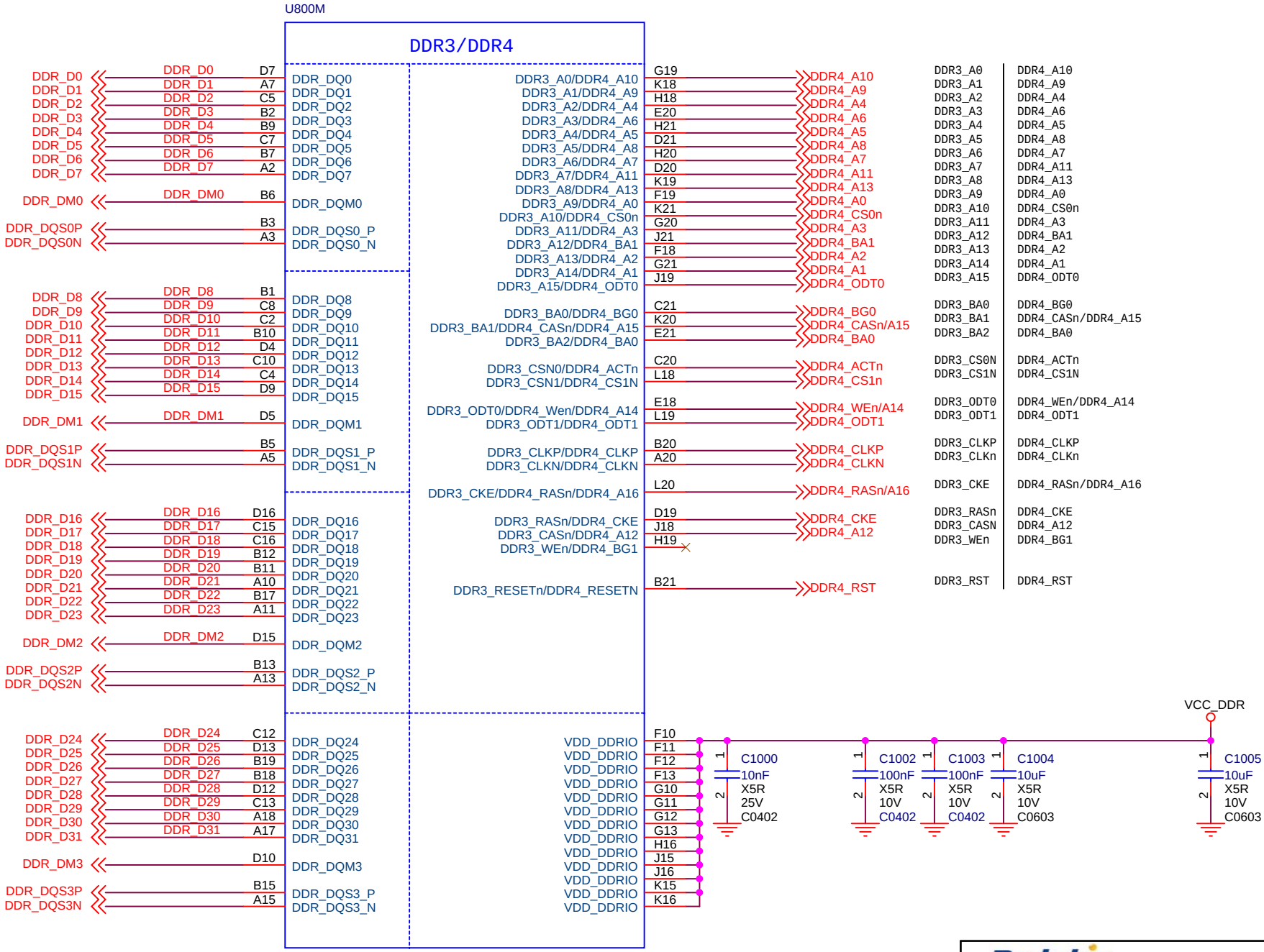
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Demo4		
File:	RK3328 Power		
Date:	Tuesday, July 18, 2017	Rev:	V1.1
Designed by:	Zhangdz	Sheet:	6 of 24





SARADC_IN0 BOM版本	SARADC_IN1 PCB版本	Up阻值	Down阻值	
Recover		DNP	10K	
BOM1		110K	10K	
BOM2		100K	20K	
BOM3		100K	33K	
BOM4		36K	18K	
BOM5		51K	36K	
BOM6		51K	51K	
BOM7		36K	51K	
BOM8		18K	36K	
BOM9		33K	100K	
BOM10		20K	100K	
BOM11		10K	110K	
BOM12		10K	DNP	

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Demo4		
File:	RK3328 OSC/PLL/OTP/SARADC		
Date:	Tuesday, July 18, 2017	Rev:	V1.1
Designed by:	Zhangdz	Sheet:	7 of 24


U800M
DDR3/DDR4
DDR_D0
DDR_D1
DDR_D2
DDR_D3
DDR_D4
DDR_D5
DDR_D6
DDR_D7
DDR_DM0
DDR_DQS0P
DDR_DQS0N
DDR_D8
DDR_D9
DDR_D10
DDR_D11
DDR_D12
DDR_D13
DDR_D14
DDR_D15
DDR_DM1
DDR_DQS1P
DDR_DQS1N
DDR_D16
DDR_D17
DDR_D18
DDR_D19
DDR_D20
DDR_D21
DDR_D22
DDR_D23
DDR_DM2
DDR_DQS2P
DDR_DQS2N
DDR_D24
DDR_D25
DDR_D26
DDR_D27
DDR_D28
DDR_D29
DDR_D30
DDR_D31
DDR_DM3
DDR_DQS3P
DDR_DQS3N
DDR_DQ0
DDR_DQ1
DDR_DQ2
DDR_DQ3
DDR_DQ4
DDR_DQ5
DDR_DQ6
DDR_DQ7
DDR_DQM0
DDR_DQS0_P
DDR_DQS0_N
DDR_DQ8
DDR_DQ9
DDR_DQ10
DDR_DQ11
DDR_DQ12
DDR_DQ13
DDR_DQ14
DDR_DQ15
DDR_DQM1
DDR_DQS1_P
DDR_DQS1_N
DDR_DQ16
DDR_DQ17
DDR_DQ18
DDR_DQ19
DDR_DQ20
DDR_DQ21
DDR_DQ22
DDR_DQ23
DDR_DQM2
DDR_DQS2_P
DDR_DQS2_N
DDR_DQ24
DDR_DQ25
DDR_DQ26
DDR_DQ27
DDR_DQ28
DDR_DQ29
DDR_DQ30
DDR_DQ31
DDR_DQM3
DDR_DQS3_P
DDR_DQS3_N
DDR3_A0/DDR4_A10
DDR3_A1/DDR4_A9
DDR3_A2/DDR4_A4
DDR3_A3/DDR4_A6
DDR3_A4/DDR4_A5
DDR3_A5/DDR4_A8
DDR3_A6/DDR4_A7
DDR3_A7/DDR4_A11
DDR3_A8/DDR4_A13
DDR3_A9/DDR4_A0
DDR3_A10/DDR4_CS0n
DDR3_A11/DDR4_A3
DDR3_A12/DDR4_BA1
DDR3_A13/DDR4_A2
DDR3_A14/DDR4_A1
DDR3_A15/DDR4_ODT0
DDR3_BA0/DDR4_BG0
DDR3_BA1/DDR4_CASn/DDR4_A15
DDR3_BA2/DDR4_BA0
DDR3_CSN0/DDR4_ACTn
DDR3_CSN1/DDR4_CS1n
DDR3_ODT0/DDR4_Wen/DDR4_A14
DDR3_ODT1/DDR4_ODT1
DDR3_CLKP/DDR4_CLKP
DDR3_CLKN/DDR4_CLKN
DDR3_CKE/DDR4_RASn/DDR4_A16
DDR3_RASn/DDR4_CKE
DDR3_CASn/DDR4_A12
DDR3_WEn/DDR4_BG1
DDR3_RESETn/DDR4_RESETN
VDD_DDRIO
DDR4_A10
DDR4_A9
DDR4_A4
DDR4_A6
DDR4_A5
DDR4_A8
DDR4_A7
DDR4_A11
DDR4_A13
DDR4_A0
DDR4_CS0n
DDR4_A3
DDR4_BA1
DDR4_A2
DDR4_A1
DDR4_ODT0
DDR4_BG0
DDR4_CASn/DDR4_A15
DDR4_BA0
DDR4_ACTn
DDR4_CS1n
DDR4_WEn/DDR4_A14
DDR4_ODT1
DDR4_CLKP
DDR4_CLKN
DDR4_RASn/DDR4_A16
DDR4_CKE
DDR4_A12
DDR4_RST
DDR3_A0 DDR4_A10
DDR3_A1 DDR4_A9
DDR3_A2 DDR4_A4
DDR3_A3 DDR4_A6
DDR3_A4 DDR4_A5
DDR3_A5 DDR4_A8
DDR3_A6 DDR4_A7
DDR3_A7 DDR4_A11
DDR3_A8 DDR4_A13
DDR3_A9 DDR4_A0
DDR3_A10 DDR4_CS0n
DDR3_A11 DDR4_A3
DDR3_A12 DDR4_BA1
DDR3_A13 DDR4_A2
DDR3_A14 DDR4_A1
DDR3_A15 DDR4_ODT0
DDR3_BA0 DDR4_BG0
DDR3_BA1 DDR4_CASn/DDR4_A15
DDR3_BA2 DDR4_BA0
DDR3_CS0N DDR4_ACTn
DDR3_CS1N DDR4_CS1N
DDR3_ODT0 DDR4_WEn/DDR4_A14
DDR3_ODT1 DDR4_ODT1
DDR3_CLKP DDR4_CLKP
DDR3_CLKn DDR4_CLKn
DDR3_CKE DDR4_RASn/DDR4_A16
DDR3_RASn DDR4_CKE
DDR3_CASN DDR4_A12
DDR3_WEn DDR4_BG1
DDR3_RST DDR4_RST
VCC_DDR
C1000 10nF X5R 25V C0402
C1002 100nF X5R 10V C0402
C1003 100nF X5R 10V C0402
C1004 10uF X5R 10V C0603
C1005 10uF X5R 10V C0603
RK3328
BGA395_14R00X14R00X1R24
Fuzhou Rockchip Electronics
Project: RK3328_BOX_Demo4
File: RK3328 DDR Controler
Date: Tuesday, July 18, 2017
Rev: V1.1
Designed by: Zhangdz
Sheet: 8 of 24

For WIFI

Note:
该项目不要求SD BOOT，
然后由于模具原因，
把SDMMC0EXT更改接SD/TF卡。
SDMMC0接WIFI

For SD/TF card

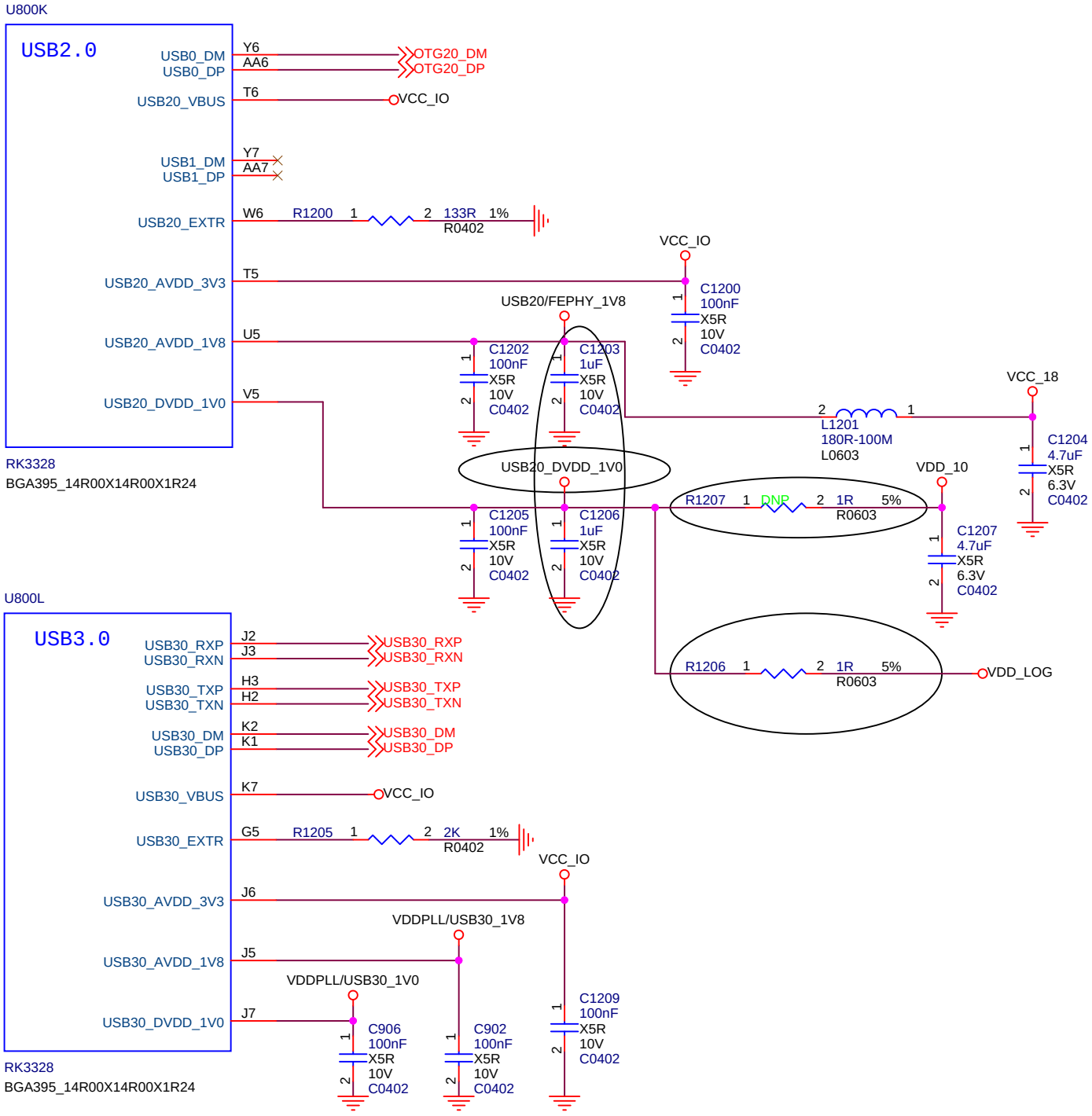
Note:
SDMMC0支持SD Boot，Max 150MHz
SDMMC0EXT不支持SD Boot，Max 100MHz

SDMMC0_D0	----------	SD_D0
SDMMC0_D1	----------	SD_D1
SDMMC0_D2/JTAG_TCK	----------	SD_D2
SDMMC0_D3/JTAG_TMS	----------	SD_D3
SDMMC0_CMD	----------	SD_CMD
SDMMC0_CLK	----------	SD_CLK
SDMMC0_DET	----------	SD_DET
VCCIO3	----------	VCC_IO
SDMMC0EXT_D0	----------	WIFI_D0_EXT
SDMMC0EXT_D1	----------	WIFI_D1_EXT
SDMMC0EXT_D2	----------	WIFI_D2_EXT
SDMMC0EXT_D3	----------	WIFI_D3_EXT
SDMMC0EXT_CMD	----------	WIFI_CMD_EXT
SDMMC0EXT_CLK	----------	WIFI_CLK_EXT
GPIO3_A1	----------	WIFI_WAKE_HOST_EXT
VCCIO6	----------	VCCIO_WL_EXT

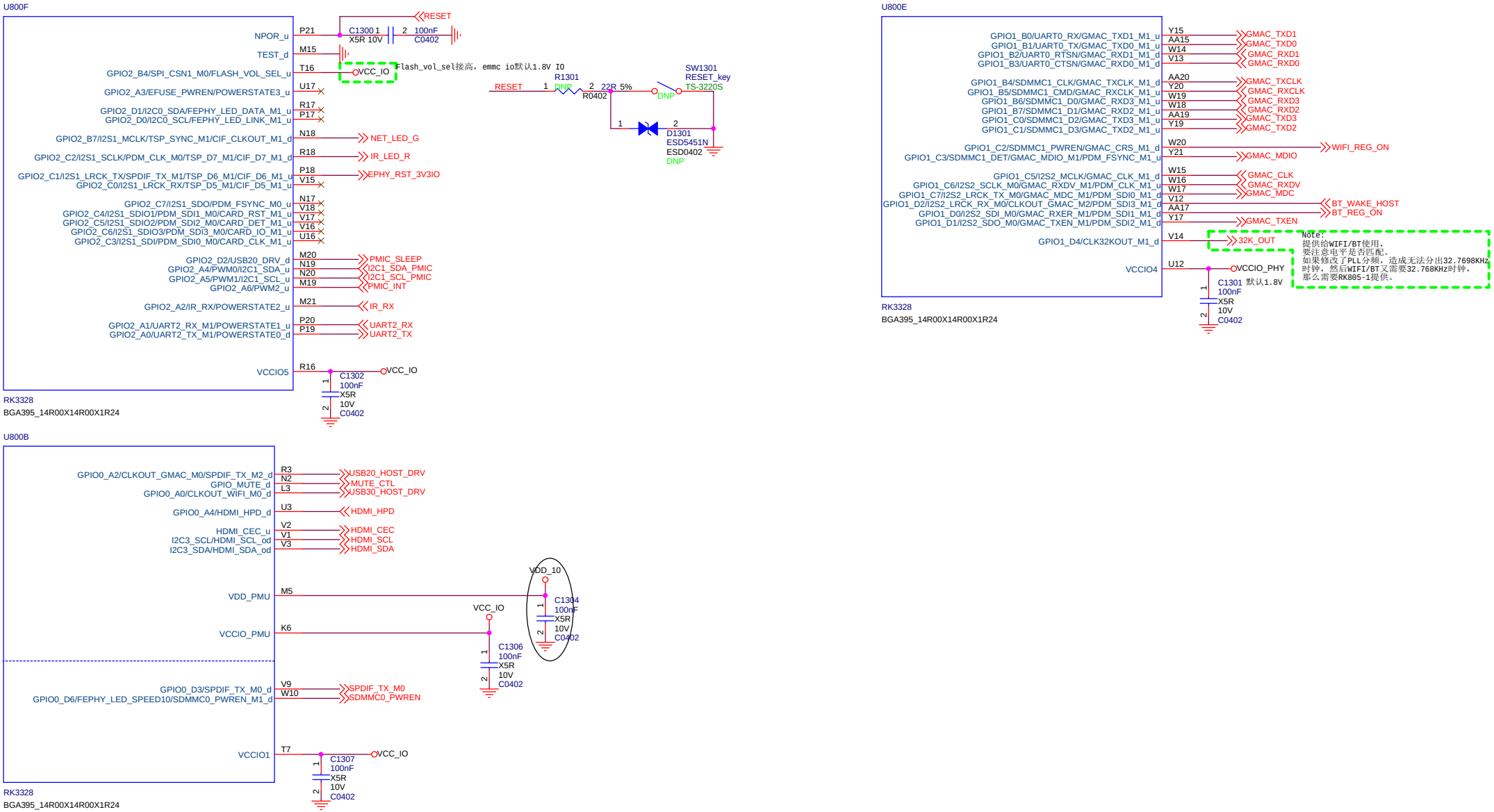
SDMMC0_D0	----------	WIFI_D0_EXT
SDMMC0_D1	----------	WIFI_D1_EXT
SDMMC0_D2/JTAG_TCK	----------	WIFI_D2_EXT
SDMMC0_D3/JTAG_TMS	----------	WIFI_D3_EXT
SDMMC0_CMD	----------	WIFI_CMD_EXT
SDMMC0_CLK	----------	WIFI_CLK_EXT
SDMMC0_DET	----------	WIFI_WAKE_HOST_EXT
VCCIO3	----------	VCCIO_WL_EXT
SDMMC0EXT_D0	----------	SD_D0
SDMMC0EXT_D1	----------	SD_D1
SDMMC0EXT_D2	----------	SD_D2
SDMMC0EXT_D3	----------	SD_D3
SDMMC0EXT_CMD	----------	SD_CMD
SDMMC0EXT_CLK	----------	SD_CLK
SDMMC0EXT_DET	----------	SD_DET
VCCIO6	----------	VCC_IO

如果WIFI需要高性能，前提是不需要支持SD Boot功能
WIFI SDIO接到SDMMC0口上。
SDMMC0EXT接SD卡

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Demo4		
File:	RK3328 eMMC Controler/TF		
Date:	Wednesday, August 16, 2017	Rev:	V1.1
Designed by:	Zhangdz	Sheet:	9 of 24

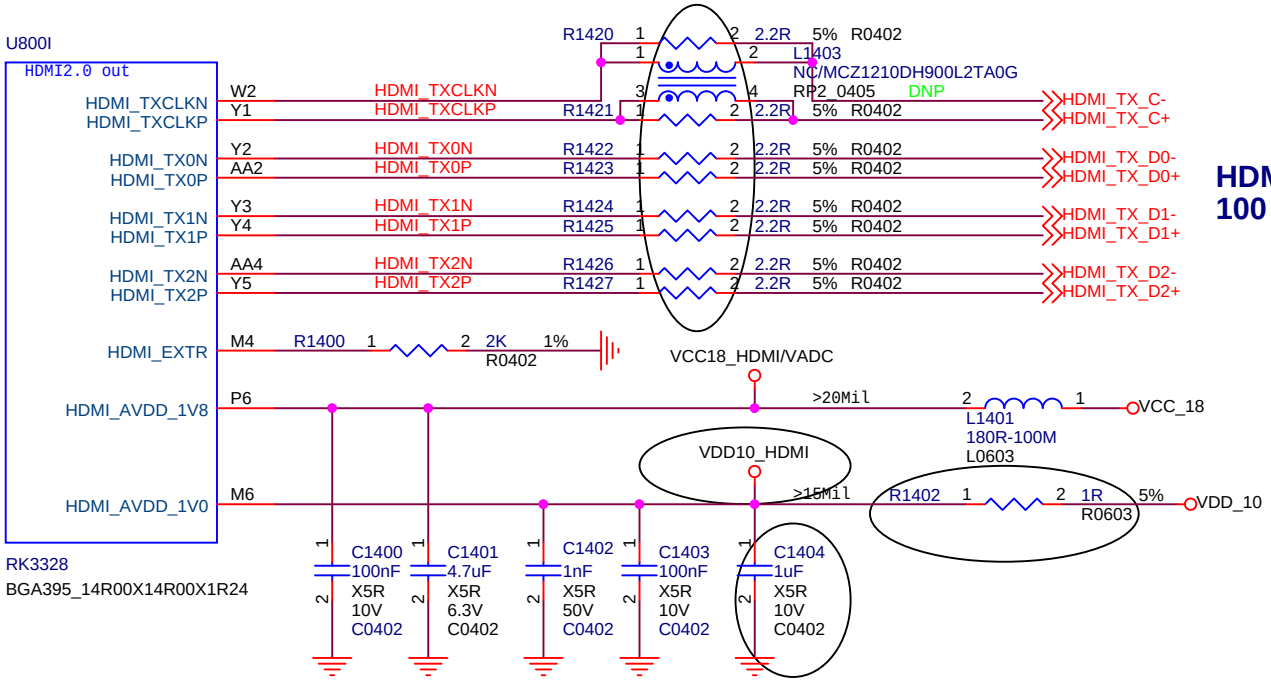


Fuzhou Rockchip Electronics			
Project:	RK3328_BOX_Demo4		
File:	RK3328 USB2 PHY/USB3 PHY		
Date:	Tuesday, July 18, 2017	Rev:	V1.1
Designed by:	Zhangdz	Sheet:	10 of 24



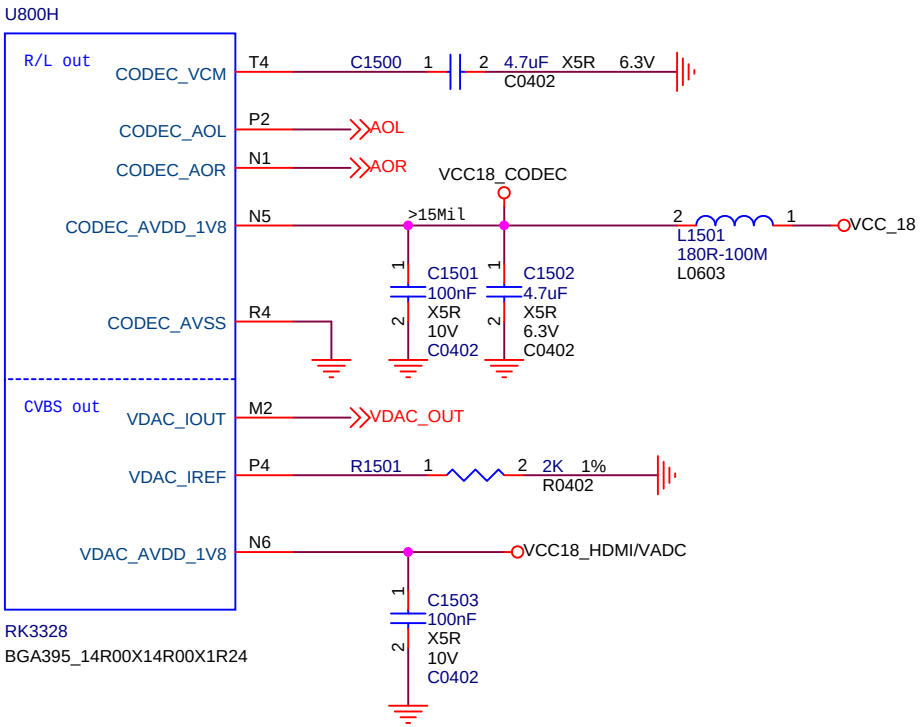
Rockchip 瑞芯微电子 Fuzhou Rockchip Electronics

Project:	RK3328_BOX_Demo4		
File:	RK3328 SDIO/UART/I2C/I2S/IR		
Date:	Tuesday, July 18, 2017	Rev:	V1.1
Designed by:	Zhangdz	Sheet:	11 of 24

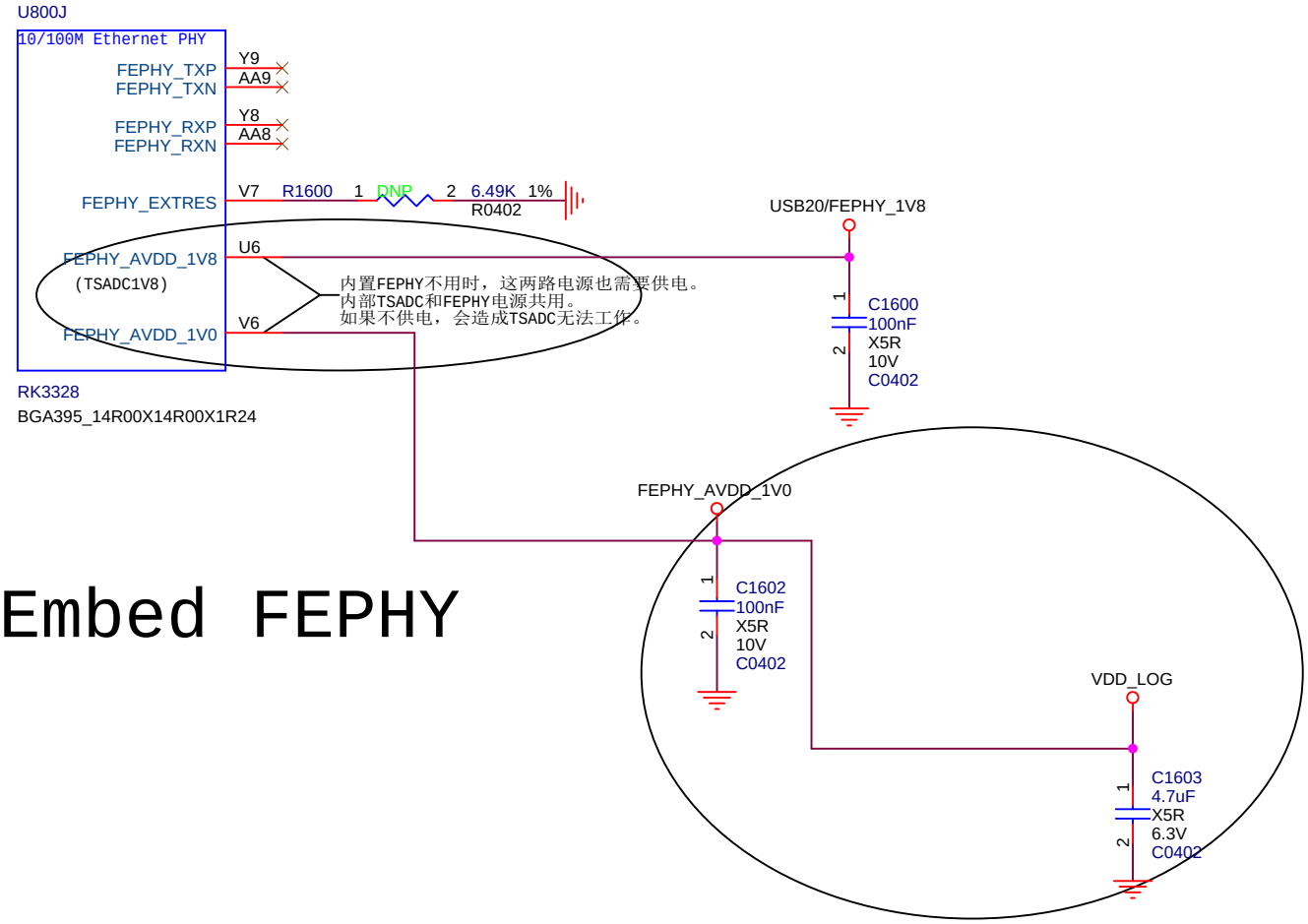


HDMI TMDS trace
100 Ohm +-10%

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Demo4		
File:	RK3328 HDMI PHY		
Date:	Tuesday, July 18, 2017	Rev:	V1.1
Designed by:	Zhangdz	Sheet:	12 of 24

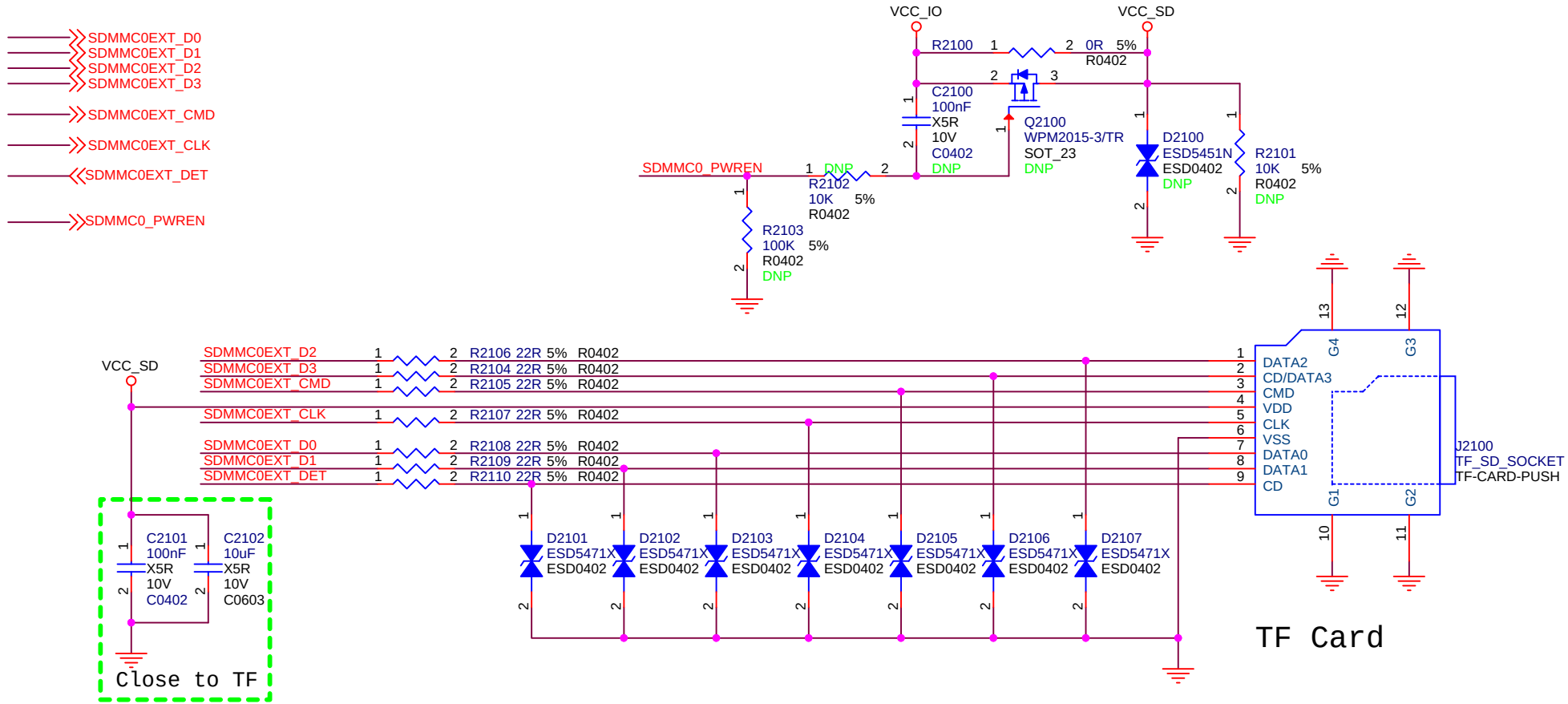


Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Demo4		
File:	RK3328 AV Interface		
Date:	Tuesday, July 18, 2017	Rev:	V1.1
Designed by:	Zhangdz	Sheet:	13 of 24

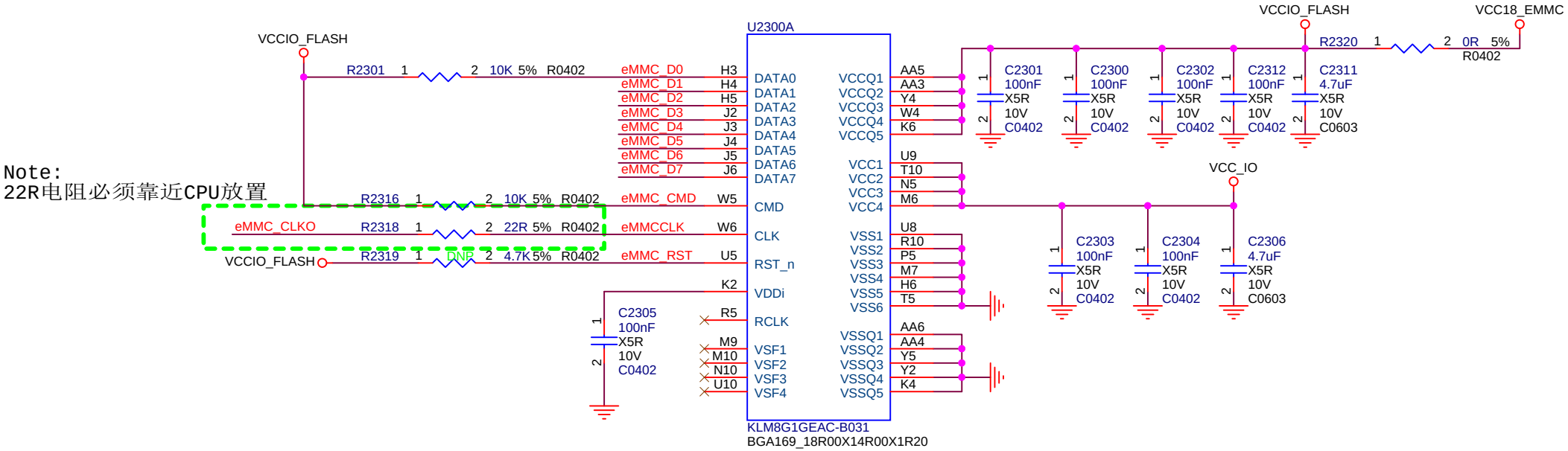


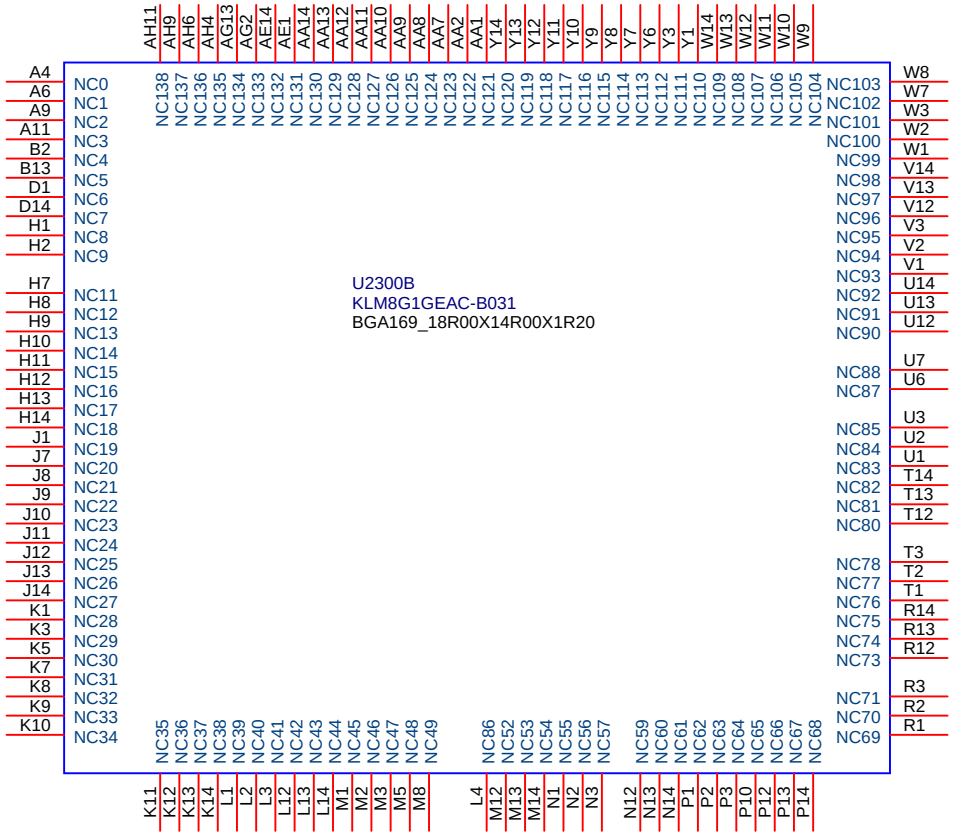
Embed FEPHY

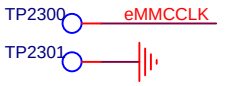
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Demo4		
File:	RK3328 FEPHY		
Date:	Tuesday, July 18, 2017	Rev:	V1.1
Designed by:	Zhangdz	Sheet:	14 of 24



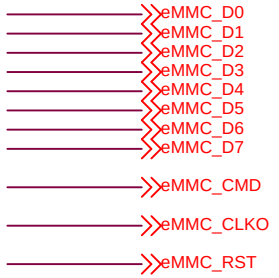
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Demo4		
File:	TF/SD Card		
Date:	Tuesday, July 18, 2017	Rev:	V1.1
Designed by:	Zhangdz	Sheet:	15 of 24



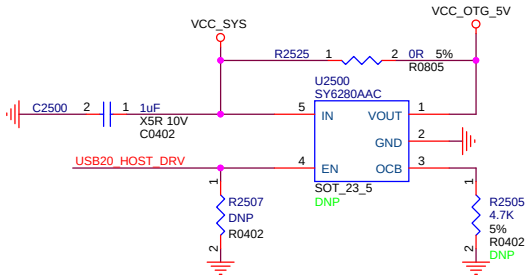


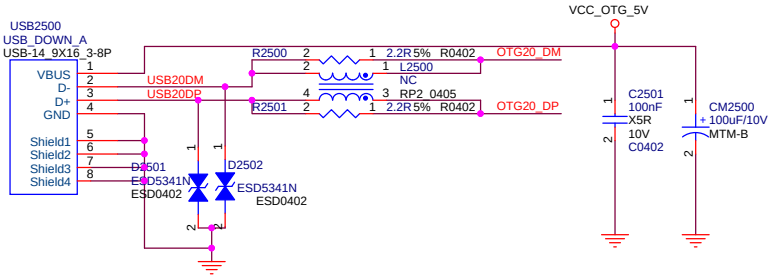


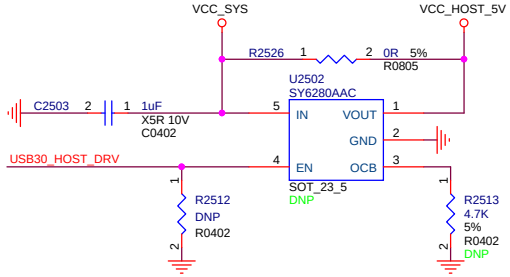
Note:
eMMC Update.

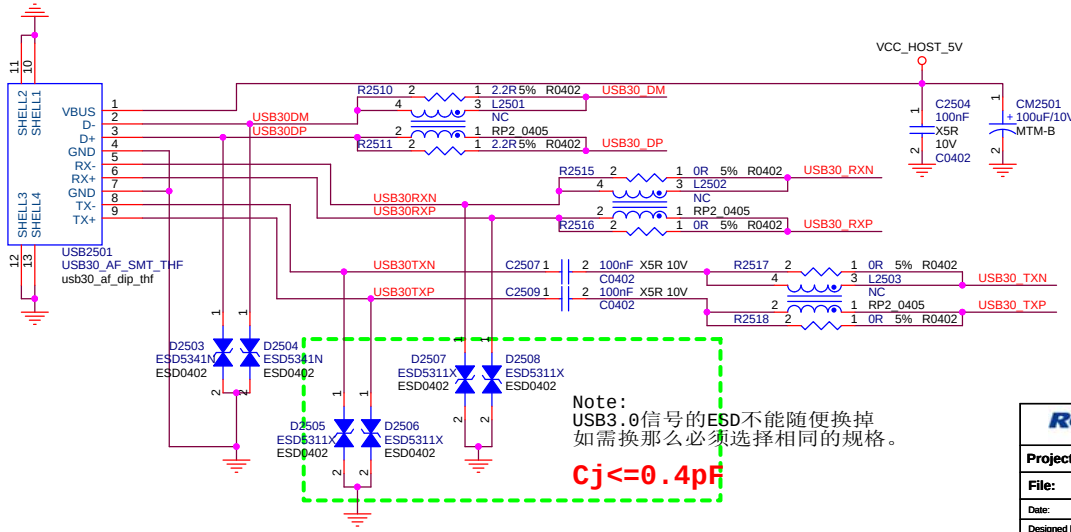


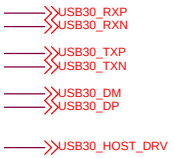
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Demo4		
File:	Flash-eMMC		
Date:	Tuesday, July 18, 2017	Rev:	V1.1
Designed by:	Zhangdz	Sheet:	16 of 24











Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Demo4		
File:	USB Port		
Date:	Tuesday, July 18, 2017	Rev:	V1.1
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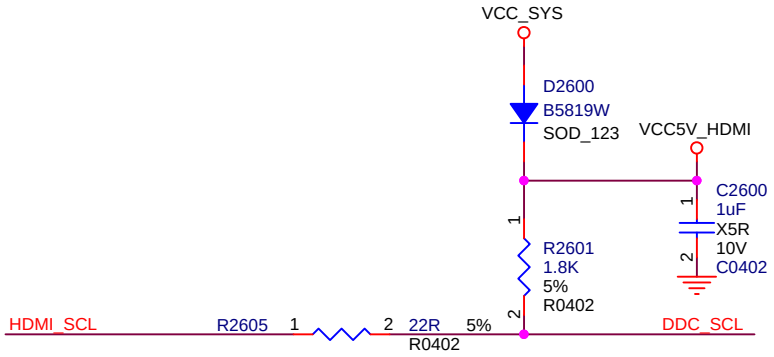
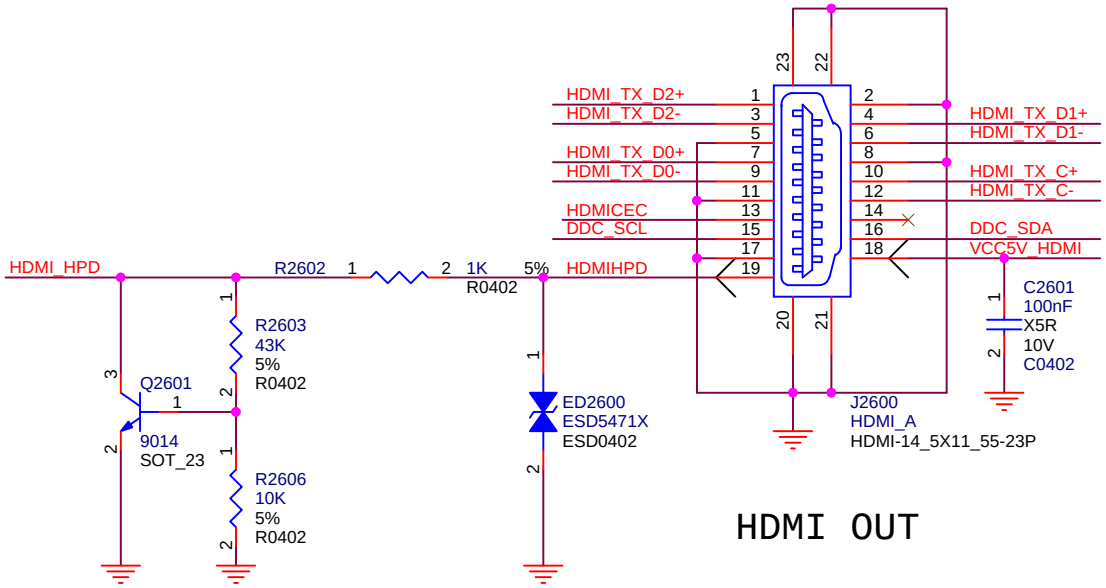
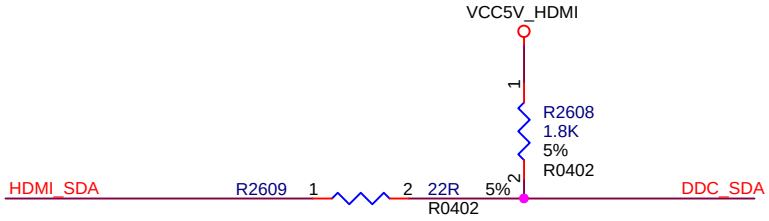
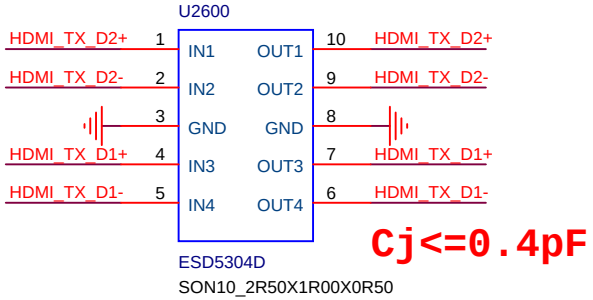


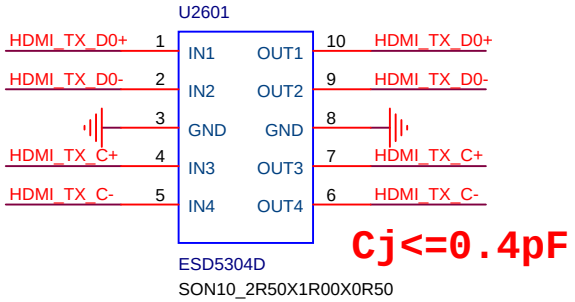


HDMI OUT





Cj<=0.4pF



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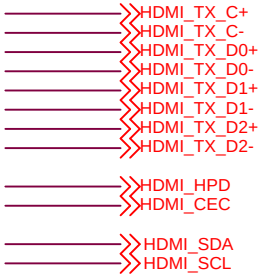

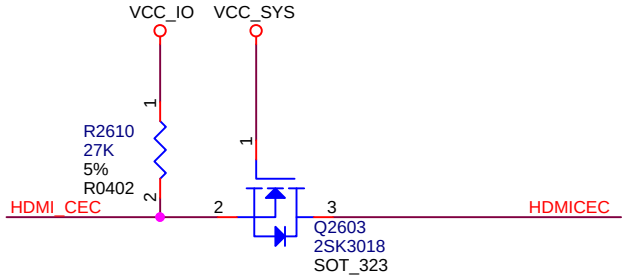

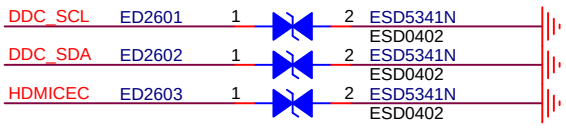

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Demo4		
File:	HDMI OUT Port		
Date:	Tuesday, July 18, 2017	Rev:	V1.1
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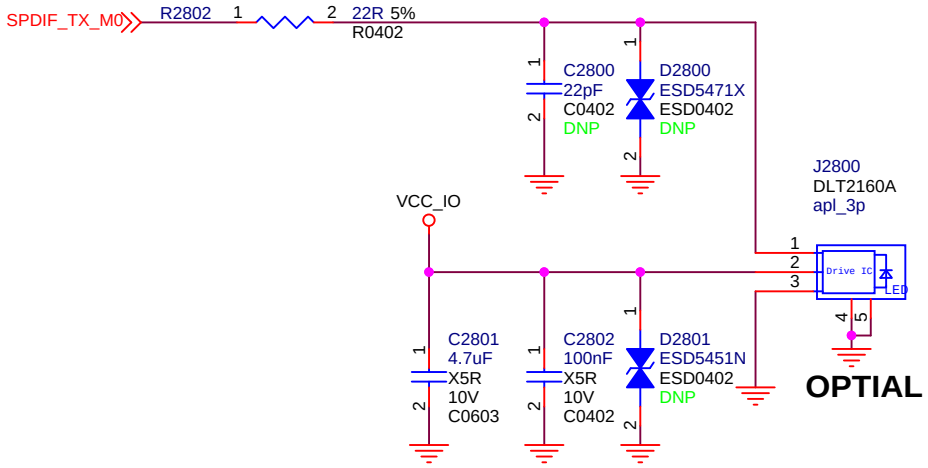
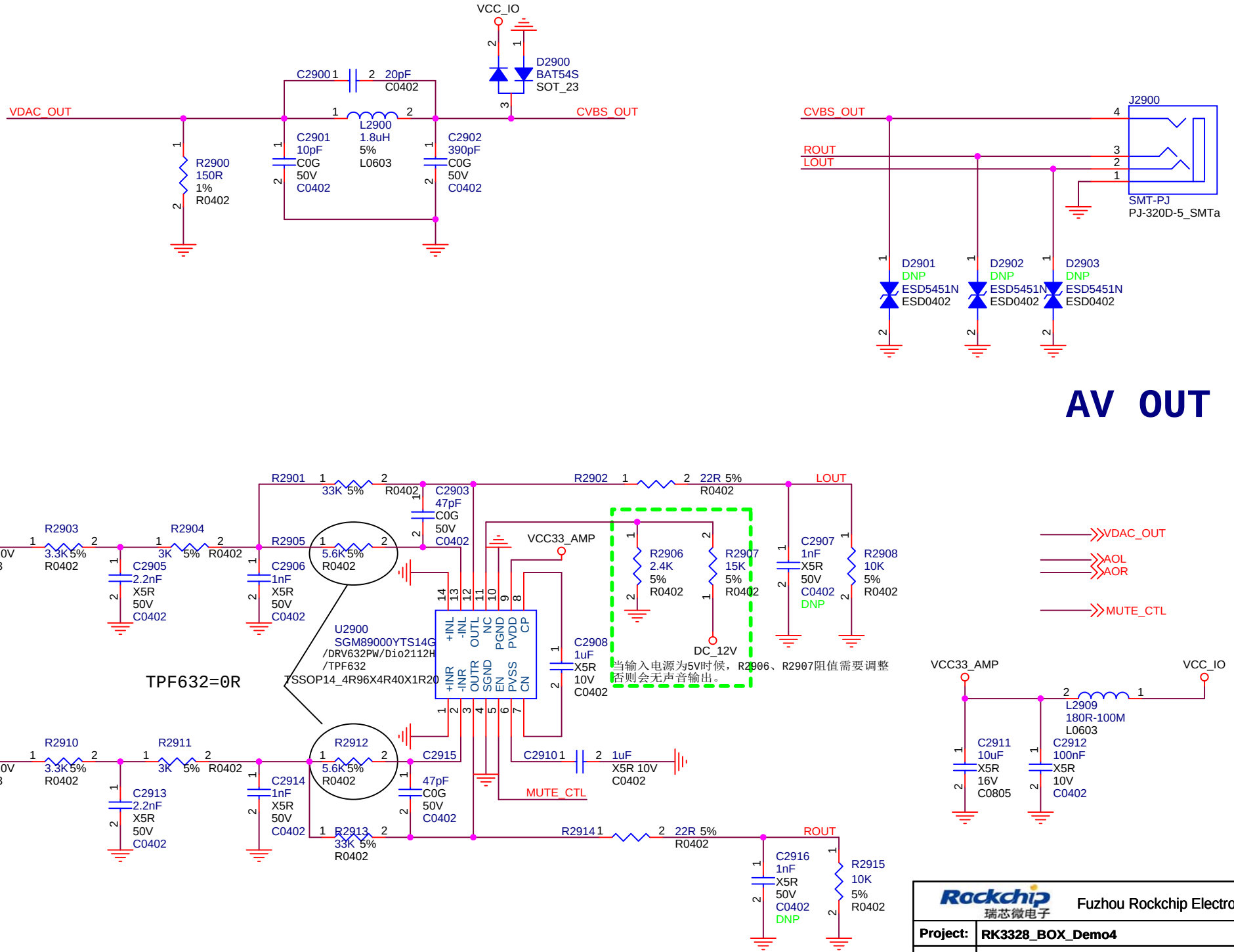


Optical SPDIF OUT

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Demo4		
File:	S/PDIF Port		
Date:	Tuesday, July 18, 2017	Rev:	V1.1
Designed by:	Zhangdz	Sheet:	19 of 24


VCC_IO
D2900
BAT54S
SOT_23
C2900 20pF
C0402
VDAC_OUT
CVBS_OUT
L2900
1.8uH
5%
L0603
R2900
150R
1%
R0402
C2901
10pF
C0G
50V
C0402
C2902
390pF
C0G
50V
C0402
CVBS_OUT
ROUT
LOUT
J2900
SMT-PJ
PJ-320D-5_SMTa
D2901
DNP
ESD5451N
ESD0402
D2902
DNP
ESD5451N
ESD0402
D2903
DNP
ESD5451N
ESD0402
AV OUT
AOL
C2904 4.7uF
X5R 10V
C0603
R2903
3.3K 5%
R0402
R2904
3K 5% R0402
R2905
5.6K 5%
R0402
R2901
33K 5%
R0402
C2903
47pF
C0G
50V
C0402
C2905
2.2nF
X5R
50V
C0402
C2906
1nF
X5R
50V
C0402
R2902 22R 5%
R0402
LOUT
VCC33_AMP
R2906
2.4K
5%
R0402
R2907
15K
5%
R0402
DC_12V
C2907
1nF
X5R
50V
C0402
DNP
R2908
10K
5%
R0402
U2900
SGM89000YTS14G
/DRV632PW/Dio2112H
/TPF632
TSSOP14_4R96X4R40X1R20
+INL
-INL
OUTL
NC
PGND
PVDD
CP
+INR
-INR
OUTR
SGND
EN
PVSS
CN
C2908
1uF
X5R
10V
C0402
TPF632=0R
当输入电源为5V时候，R2906、R2907阻值需要调整
否则会无声音输出。
VDAC_OUT
AOL
AOR
MUTE_CTL
VCC33_AMP
VCC_IO
L2909
180R-100M
L0603
C2911
10uF
X5R
16V
C0805
C2912
100nF
X5R
10V
C0402
AOR
C2909 4.7uF
X5R 10V
C0603
R2910
3.3K 5%
R0402
R2911
3K 5% R0402
R2912
5.6K 5%
R0402
C2913
2.2nF
X5R
50V
C0402
C2914
1nF
X5R
50V
C0402
C2915
47pF
C0G
50V
C0402
C2910 1uF
X5R 10V
C0402
MUTE_CTL
R2913
33K 5%
R0402
R2914 22R 5%
R0402
ROUT
C2916
1nF
X5R
50V
C0402
DNP
R2915
10K
5%
R0402
2-Vrms Audio Line Driver
Rockchip 瑞芯微电子
Fuzhou Rockchip Electronics
Project: RK3328_BOX_Demo4
File: AV OUT Port
Date: Tuesday, July 18, 2017
Rev: V1.1
Designed by: Zhangdz
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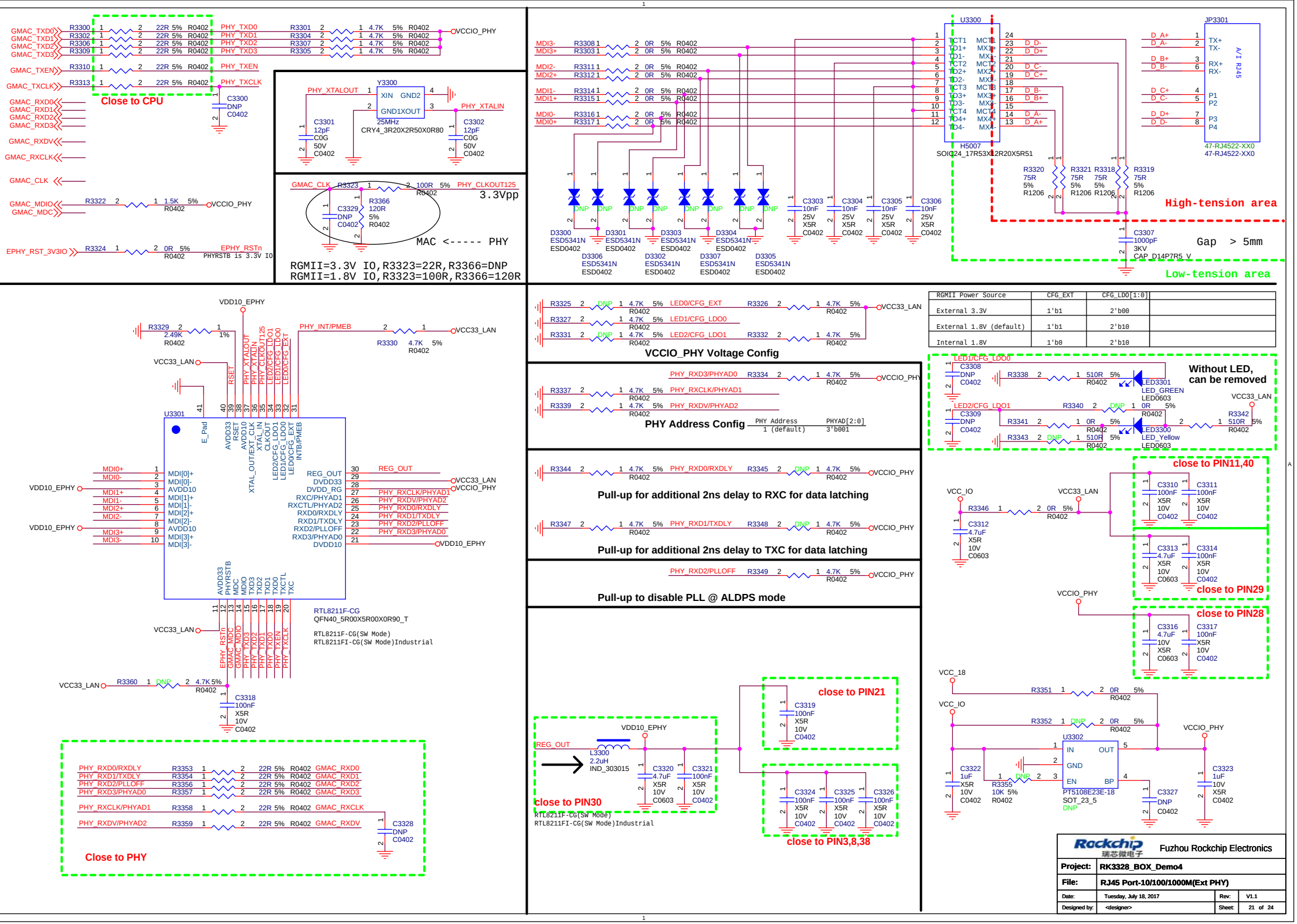
GMAC_TXD0
GMAC_TXD1
GMAC_TXD2
GMAC_TXD3
GMAC_TXEN
GMAC_TXCLK
PHY_TXD0
PHY_TXD1
PHY_TXD2
PHY_TXD3
PHY_TXEN
PHY_TXCLK
VCCIO_PHY
Close to CPU
GMAC_RXD0
GMAC_RXD1
GMAC_RXD2
GMAC_RXD3
GMAC_RXDV
GMAC_RXCLK
GMAC_CLK
GMAC_MDIO
GMAC_MDC
EPHY_RST_3V3IO
EPHY_RST_n
PHYRSTB is 3.3V IO
Y3300
PHY_XTALOUT
PHY_XTALIN
25MHz
CRY4_3R20X2R50X0R80
GMAC_CLK
PHY_CLKOUT125
3.3Vpp
MAC <----- PHY
RGMII=3.3V IO,R3323=22R,R3366=DNP
RGMII=1.8V IO,R3323=100R,R3366=120R
U3300
MDI3-
MDI3+
MDI2-
MDI2+
MDI1-
MDI1+
MDI0-
MDI0+
H5007
SOIC24_17R53X12R20X5R51
JP3301
47-RJ4522-XX0
High-tension area
Low-tension area
Gap > 5mm
VDD10_EPHY
VCC33_LAN
PHY_INT/PMEB
U3301
RTL8211F-CG
QFN40_5R00X5R00X0R90_T
RTL8211F-CG(SW Mode)
RTL8211FI-CG(SW Mode)Industrial
Close to PHY
VCCIO_PHY Voltage Config
PHY Address Config
PHY Address
1 (default)
PHYAD[2:0]
3'b001
Pull-up for additional 2ns delay to RXC for data latching
Pull-up for additional 2ns delay to TXC for data latching
Pull-up to disable PLL @ ALDPS mode
RGMII Power Source
CFG_EXT
CFG_LDO[1:0]
External 3.3V
1'b1
2'b00
External 1.8V (default)
1'b1
2'b10
Internal 1.8V
1'b0
2'b10
Without LED, can be removed
close to PIN11,40
close to PIN29
close to PIN28
close to PIN21
close to PIN30
close to PIN3,8,38
Rockchip
Fuzhou Rockchip Electronics
Project: RK3328_BOX_Demo4
File: RJ45 Port-10/100/1000M(Ext PHY)
Date: Tuesday, July 18, 2017
Rev: V1.1
Designed by: <designer>
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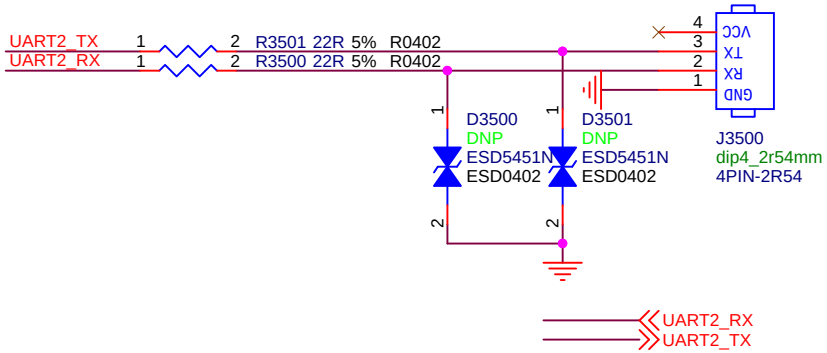
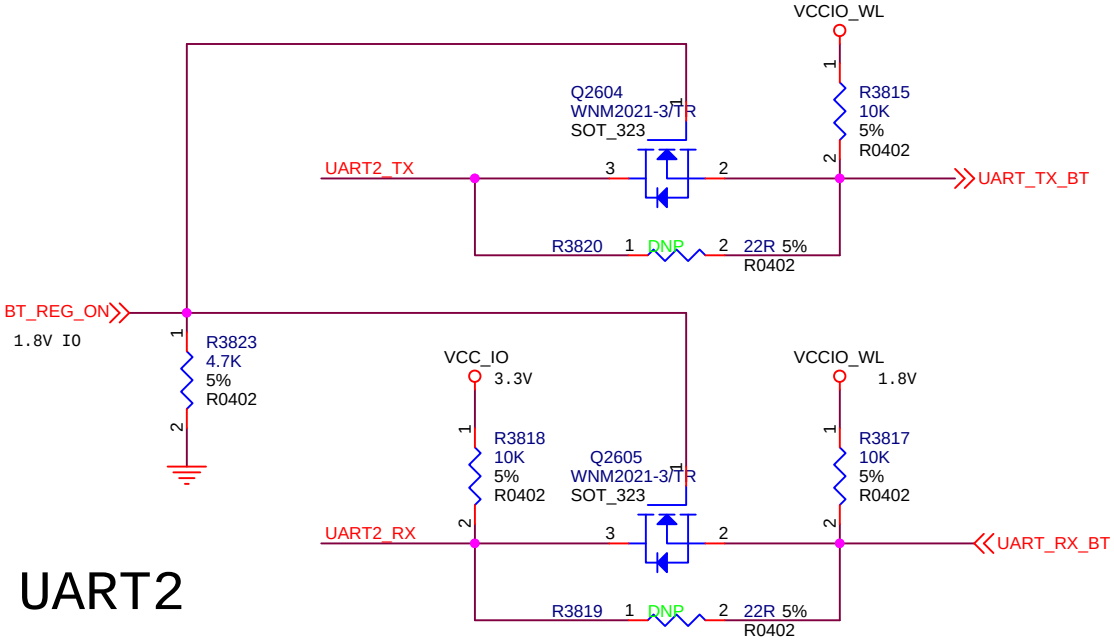


Debug UART2

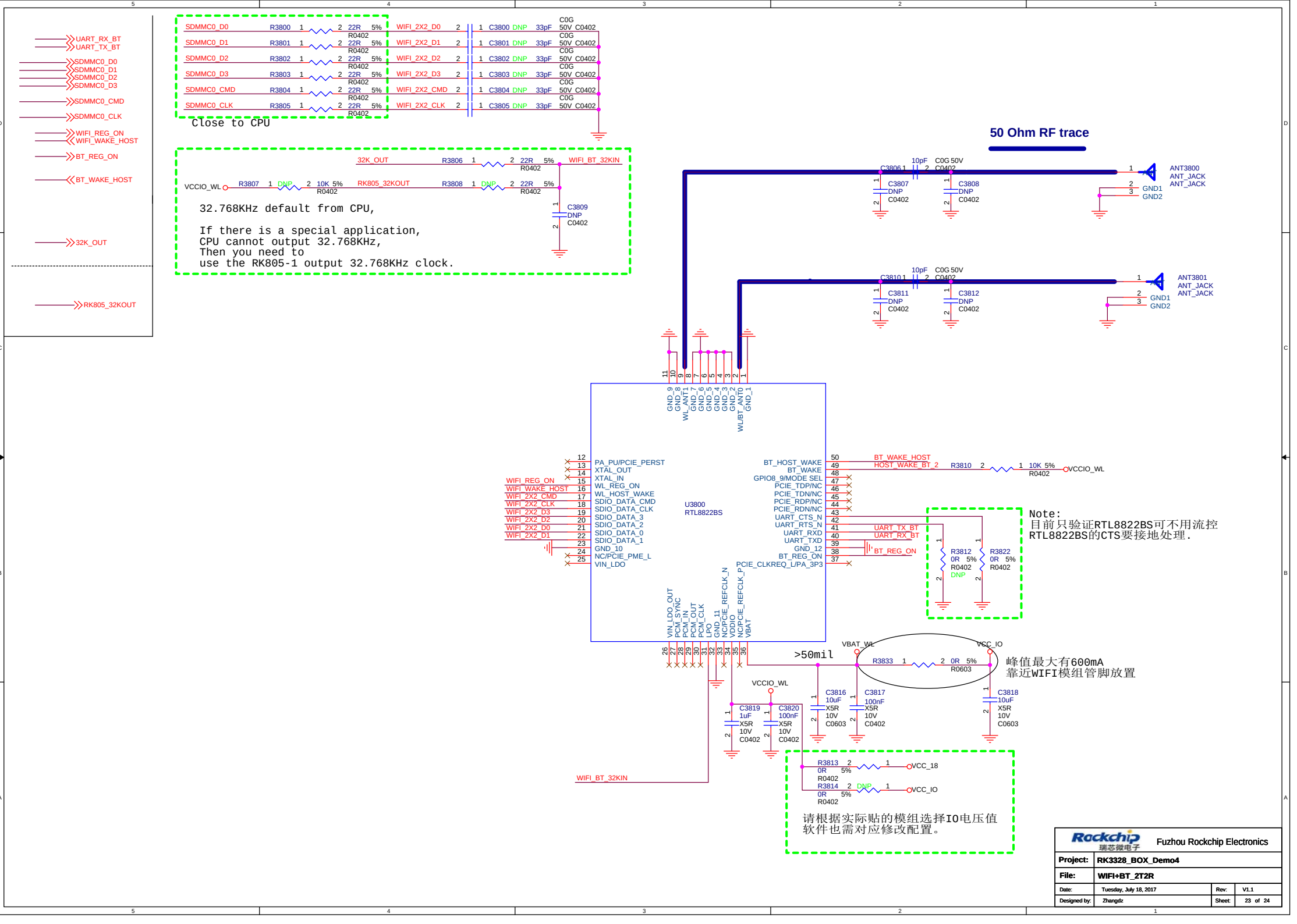


BT UART2

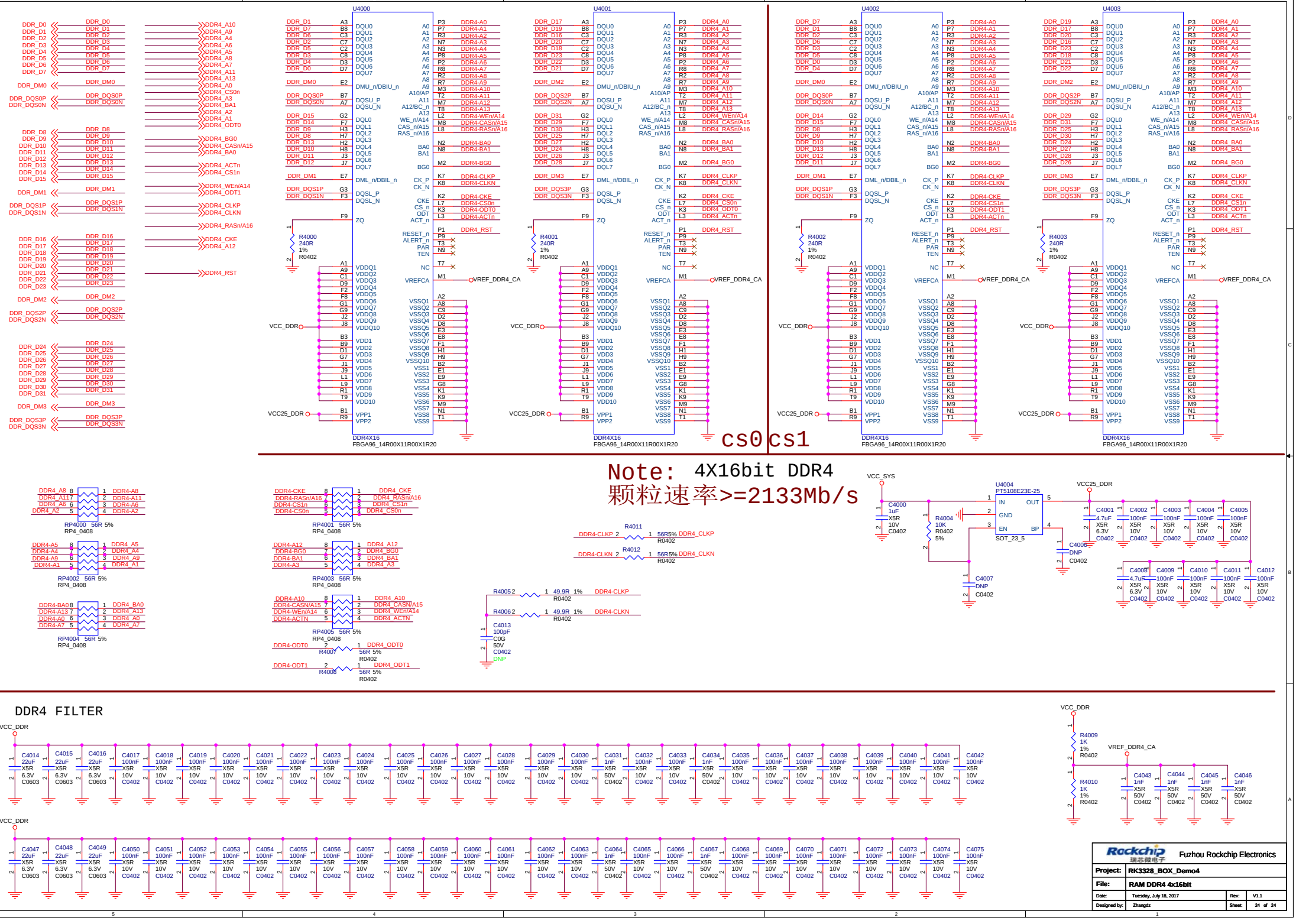
BT ON: BT UART,需移除Debug uart小板

BT OFF: Debug UART2，可接debug uart小板

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Demo4		
File:	Debug UART2/JTAG		
Date:	Tuesday, July 18, 2017	Rev:	V1.1
Designed by:	<designer>	Sheet:	22 of 24



Fuzhou Rockchip Electronics	
Project:	RK3328_BOX_Demo4
File:	WIFI+BT_2T2R
Date: Tuesday, July 18, 2017	Rev: V1.1
Designed by: Zhangdz	Sheet: 23 of 24


U4000
U4001
U4002
U4003
DDR4X16
FBGA96_14R00X11R00X1R20
cs0 cs1
Note: 4X16bit DDR4
颗粒速率>=2133Mb/s
DDR4 FILTER
VCC_DDR
VCC25_DDR
VCC_SYS
VREF_DDR4_CA
U4004
PT5108E23E-25
SOT_23_5
Rockchip
瑞芯微电子
Fuzhou Rockchip Electronics
Project: RK3328_BOX_Demo4
File: RAM DDR4 4x16bit
Date: Tuesday, July 18, 2017
Rev: V1.1
Designed by: Zhangdz
Sheet: 24 of 24