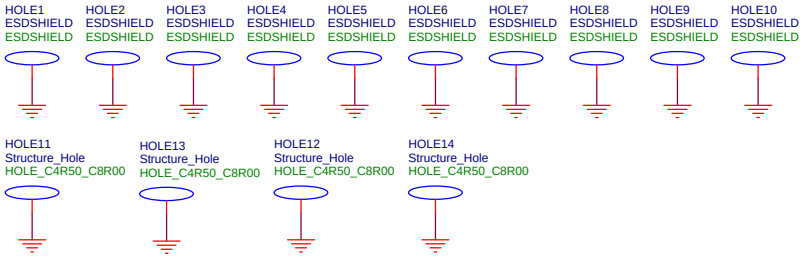
RK3328

Content Indexing



Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Note：
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Demo6		
File:	Index		
Date:	Wednesday, July 19, 2017	Rev:	V1.1
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Version	Date	Author	Change Note	Approved
V1.0	20170718	ZDZ	First edictor	

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Demo6		
File:	Change List		
Date:	Tuesday, July 18, 2017	Rev:	V1.1
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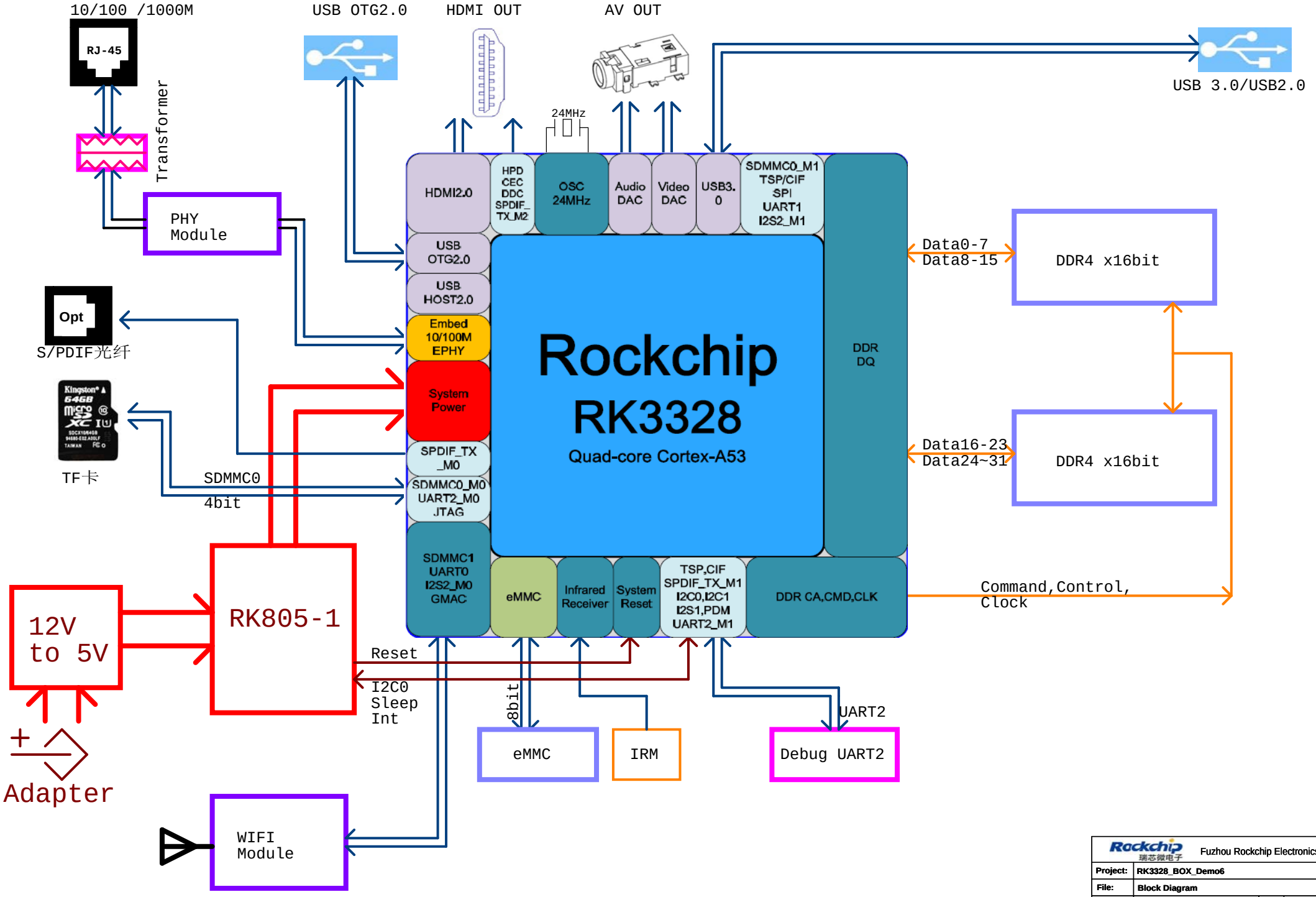

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Demo6		
File:	Block Diagram		
Date:	Wednesday, July 19, 2017	Rev:	V1.1
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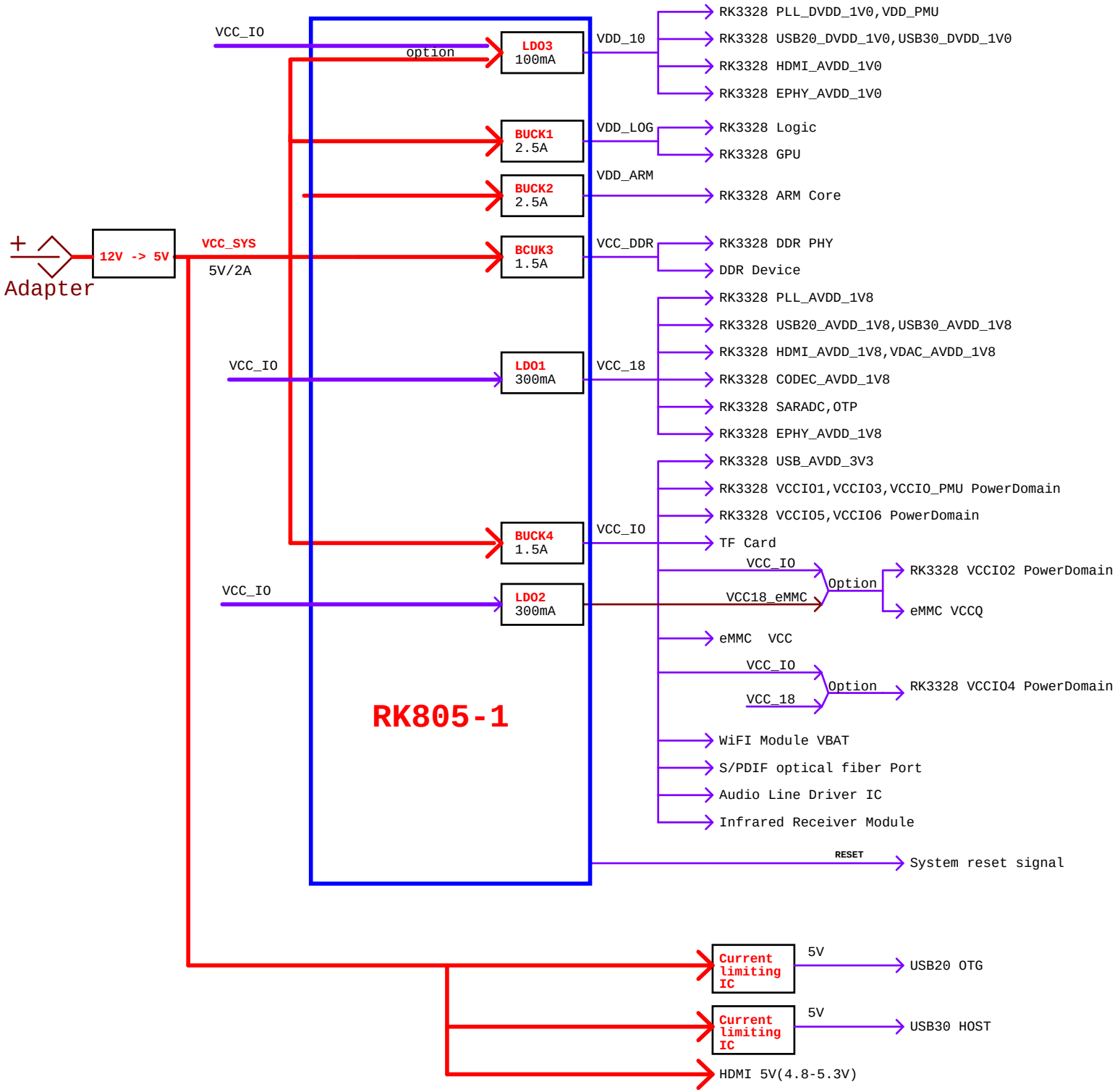

Power Timing

TYPE	VOLT	STEP	PowerName
BUCK1	1.1V		VDD_LOG
BUCK2	1.1V		VDD_ARM
BUCK3	FB=0.8V		VCC_DDR
BUCK4	3.3V		VCC_IO
LDO1	1.8V		VCC_18
LDO2	1.8V		VCC18_eMMC
LDO3	1.0V		VDD_10

IO电源域电压	IO电压＝3.3V	IO电压＝1.8V
VCCIO_PMU	3.3V	不支持
VCCIO1	3.3V	不支持
VCCIO2		1.8V（默认） eMMC
VCCIO3	3.3V（默认）	
VCCIO4	3.3V（默认） WIFI:RTL8723BS	
VCCIO5	3.3V（默认）	
VCCIO6	3.3V（默认）	

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics
Project:	RK3328_BOX_Demo6
File:	Power tree-RK805-1
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Designed by:	Zhangzb
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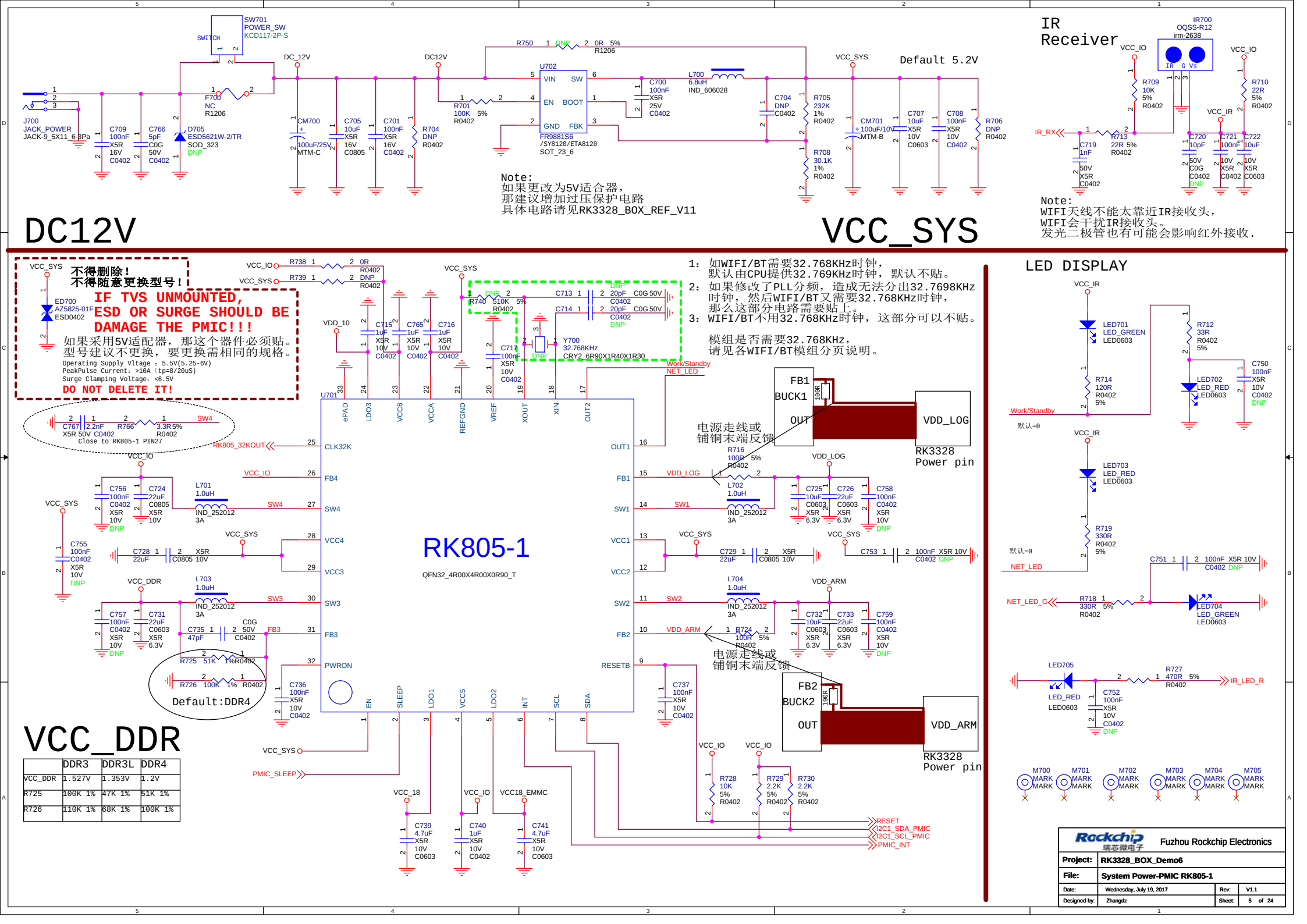
DC12V
VCC_SYS
Default 5.2V
Note:
如果更改为5V适合器，
那建议增加过压保护电路
具体电路请见RK3328_BOX_REF_V11
IR Receiver
Note:
WIFI天线不能太靠近IR接收头，
WIFI会干扰IR接收头。
发光二极管也有可能会影响红外接收.
不得删除！
不得随意更换型号！
IF TVS UNMOUNTED,
ESD OR SURGE SHOULD BE
DAMAGE THE PMIC!!!
如果采用5V适配器，那这个器件必须贴。
型号建议不更换，要更换需相同的规格。
Operating Supply Vltage : 5.5V(5.25-6V)
PeakPulse Current: >10A (tp=8/20uS)
Surge Clamping Voltage: <6.5V
DO NOT DELETE IT!
1：如WIFI/BT需要32.768KHz时钟，
默认由CPU提供32.769KHz时钟，默认不贴。
2：如果修改了PLL分频，造成无法分出32.7698KHz
时钟，然后WIFI/BT又需要32.768KHz时钟，
那么这部分电路需要贴上。
3：WIFI/BT不用32.768KHz时钟，这部分可以不贴。
模组是否需要32.768KHz，
请见各WIFI/BT模组分页说明。
RK805-1
QFN32_4R00X4R00X0R90_T
电源走线或
铺铜末端反馈
RK3328
Power pin
VDD_LOG
VDD_ARM
LED DISPLAY
VCC_DDR
Default:DDR4
DDR3 DDR3L DDR4
VCC_DDR 1.527V 1.353V 1.2V
R725 100K 1% 47K 1% 51K 1%
R726 110K 1% 68K 1% 100K 1%
Rockchip 瑞芯微电子 Fuzhou Rockchip Electronics
Project: RK3328_BOX_Demo6
File: System Power-PMIC RK805-1
Date: Wednesday, July 19, 2017
Rev: V1.1
Designed by: Zhangdz
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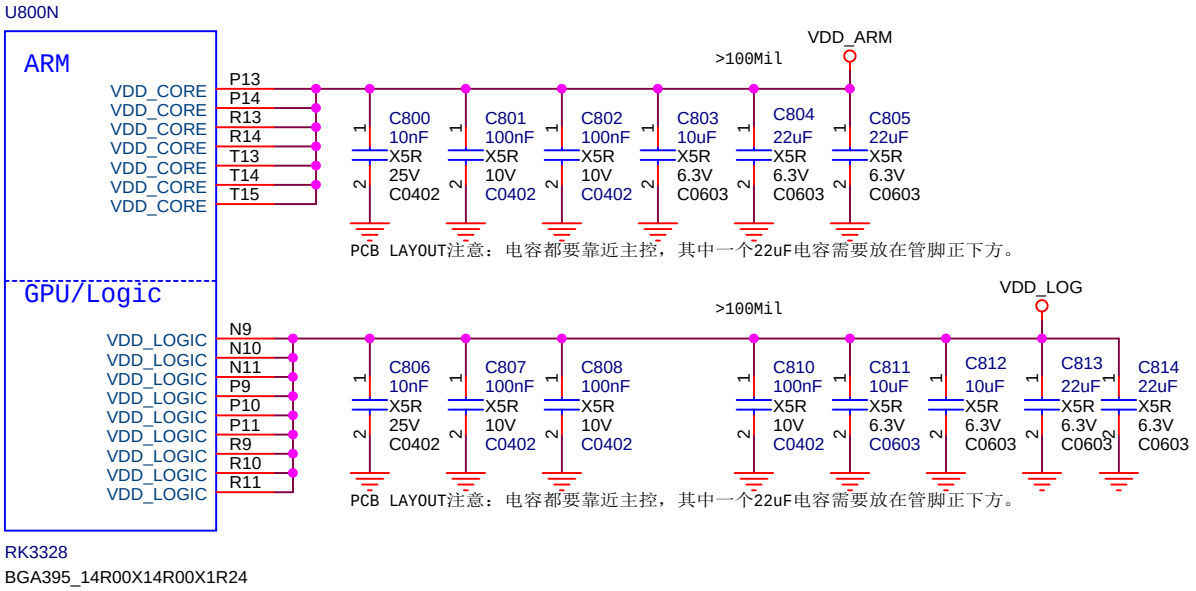

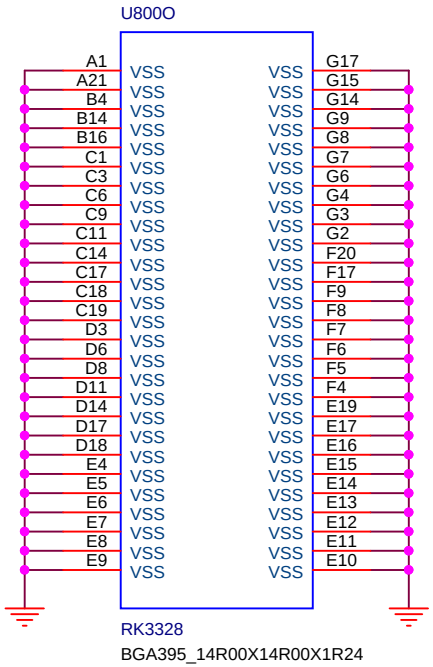

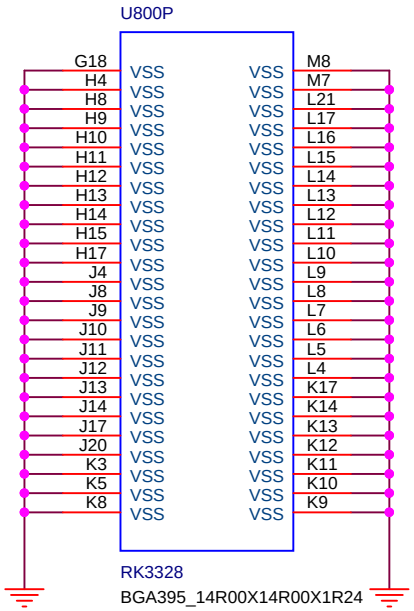

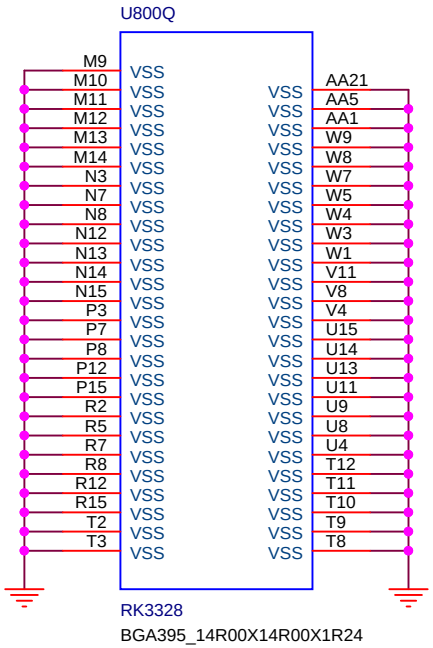

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Demo6		
File:	RK3328 Power		
Date:	Tuesday, July 18, 2017	Rev:	V1.1
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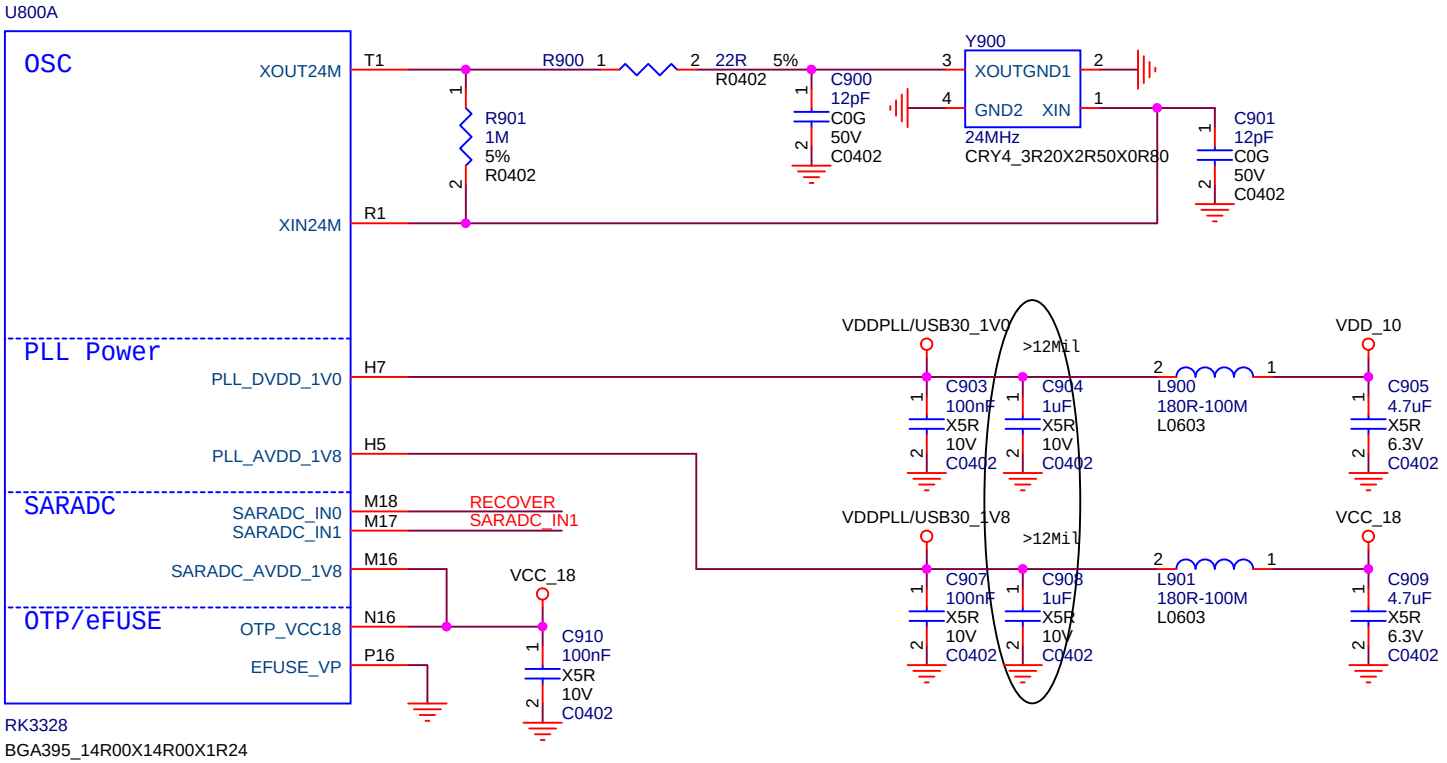

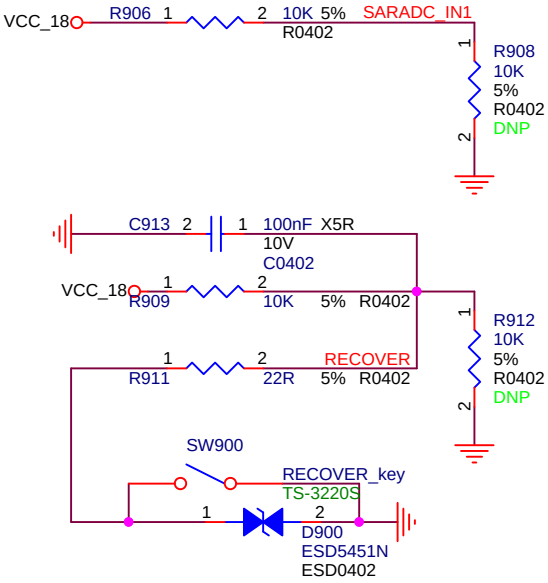

SARADC_IN0 BOM版本	SARADC_IN1 PCB版本	Up阻值	Down阻值	
Recover		DNP	10K	
BOM1		110K	10K	
BOM2		100K	20K	
BOM3		100K	33K	
BOM4		36K	18K	
BOM5		51K	36K	
BOM6		51K	51K	
BOM7		36K	51K	
BOM8		18K	36K	
BOM9		33K	100K	
BOM10		20K	100K	
BOM11		10K	110K	
BOM12		10K	DNP	

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Demo6		
File:	RK3328 OSC/PLL/OTP/SARADC		
Date:	Tuesday, July 18, 2017	Rev:	V1.1
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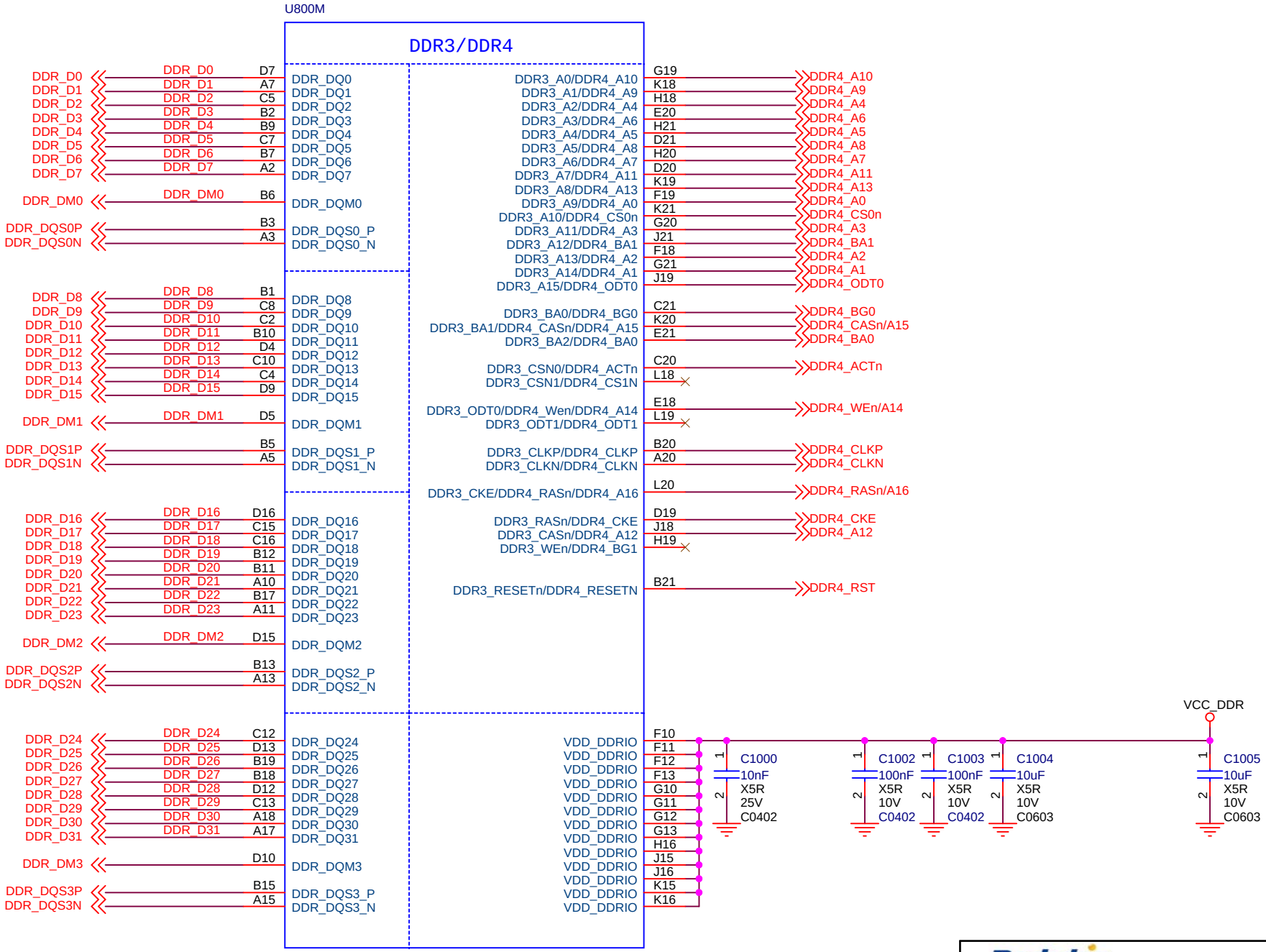

Fuzhou Rockchip Electronics			
Project:	RK3328_BOX_Demo6		
File:	RK3328 DDR Controler		
Date:	Tuesday, July 18, 2017	Rev:	V1.1
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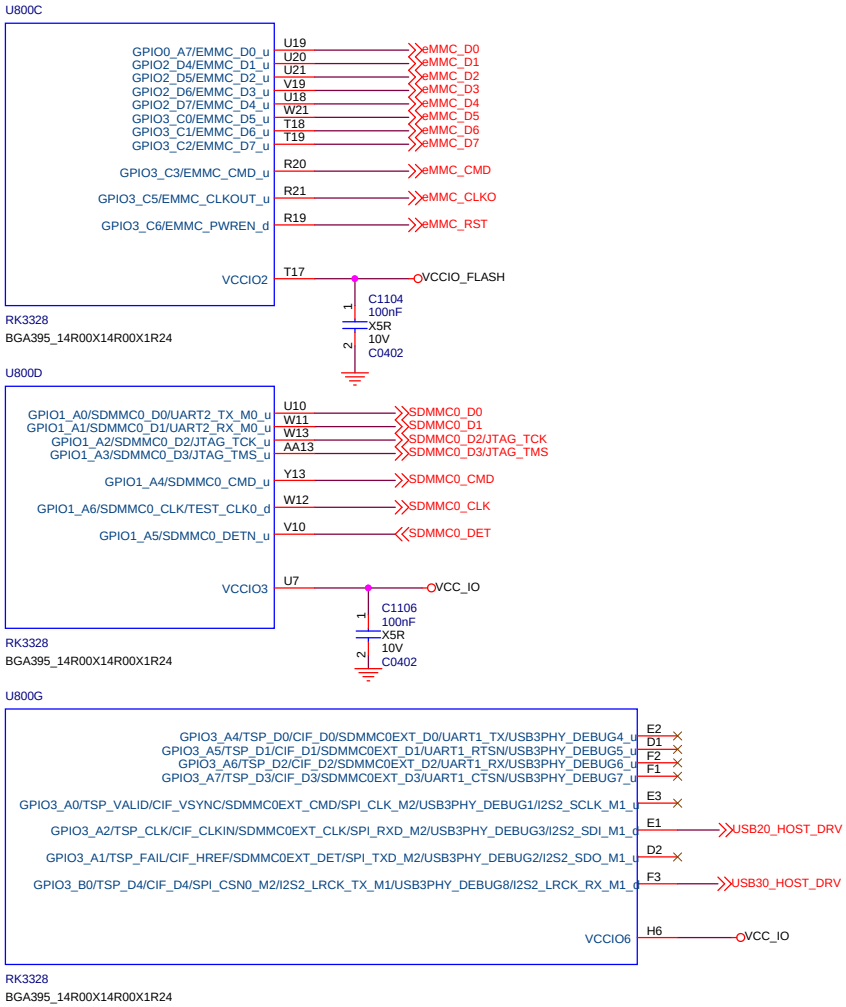

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Demo6		
File:	RK3328 FLASH Controler/TF		
Date:	Tuesday, July 18, 2017	Rev:	V1.1
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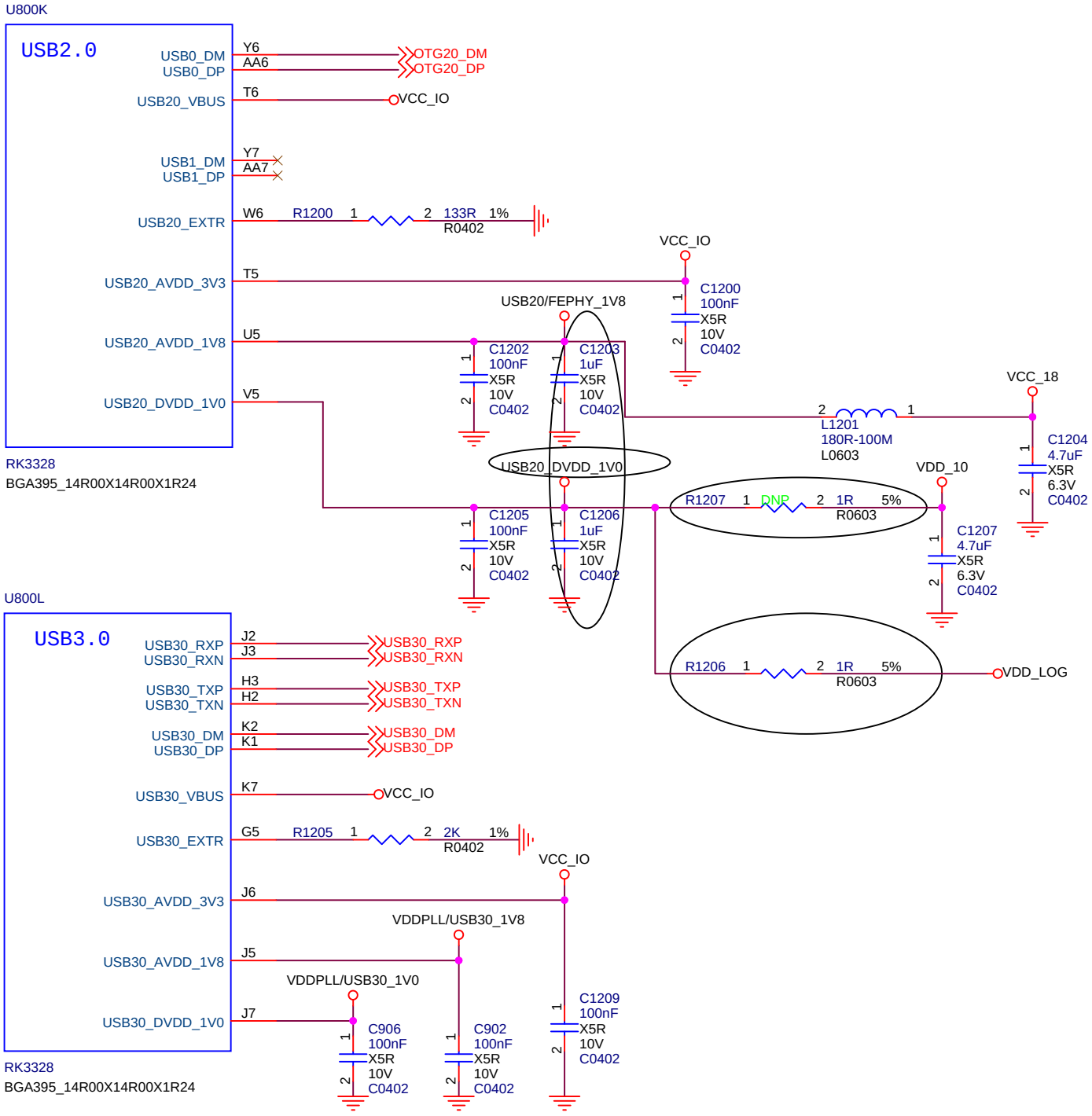

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Demo6		
File:	RK3328 USB2 PHY/USB3 PHY		
Date:	Tuesday, July 18, 2017	Rev:	V1.1
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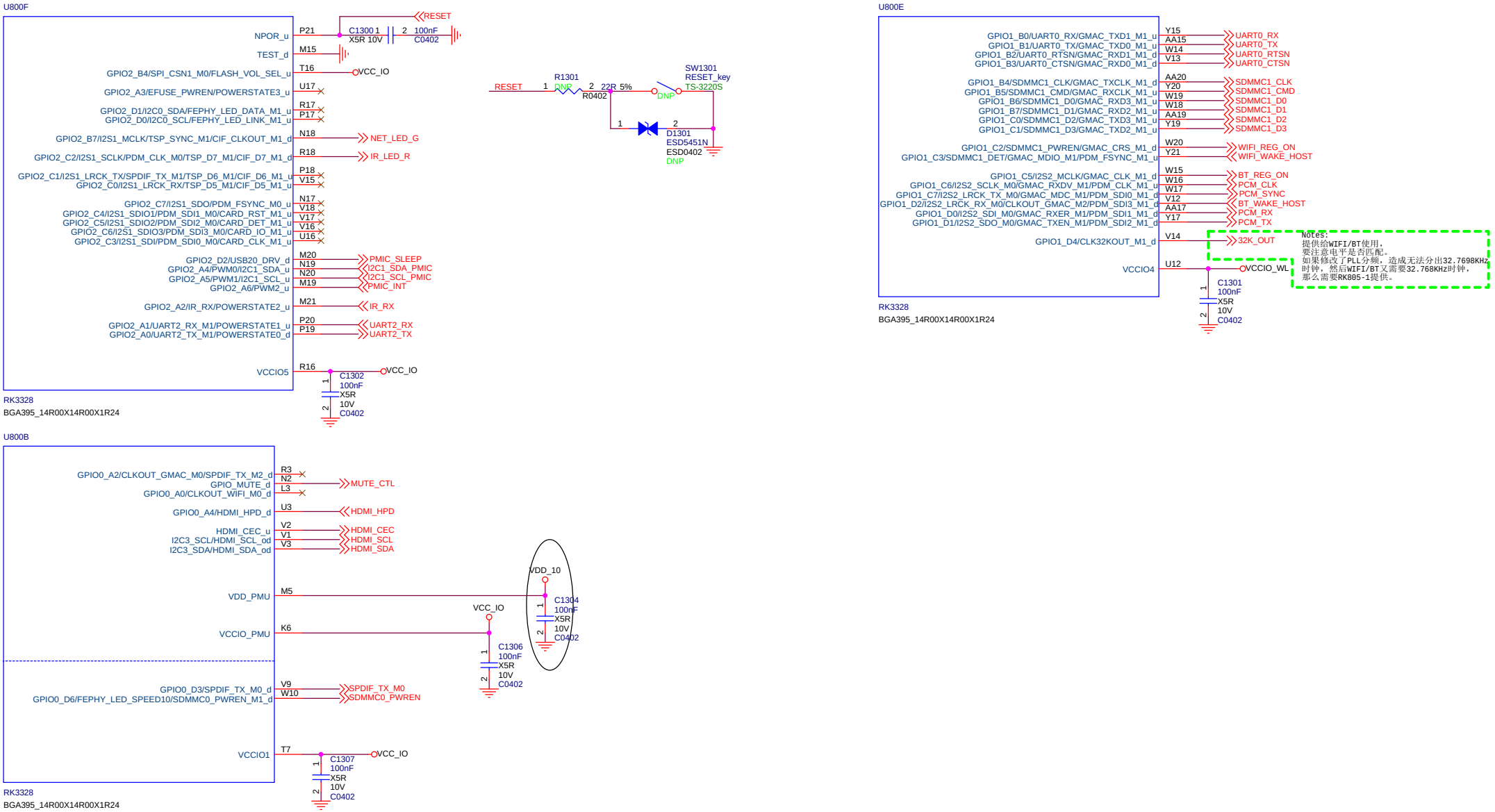

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Demo6		
File:	RK3328 SDIO/UART/I2C/I2S/IR		
Date:	Tuesday, July 18, 2017	Rev:	V1.1
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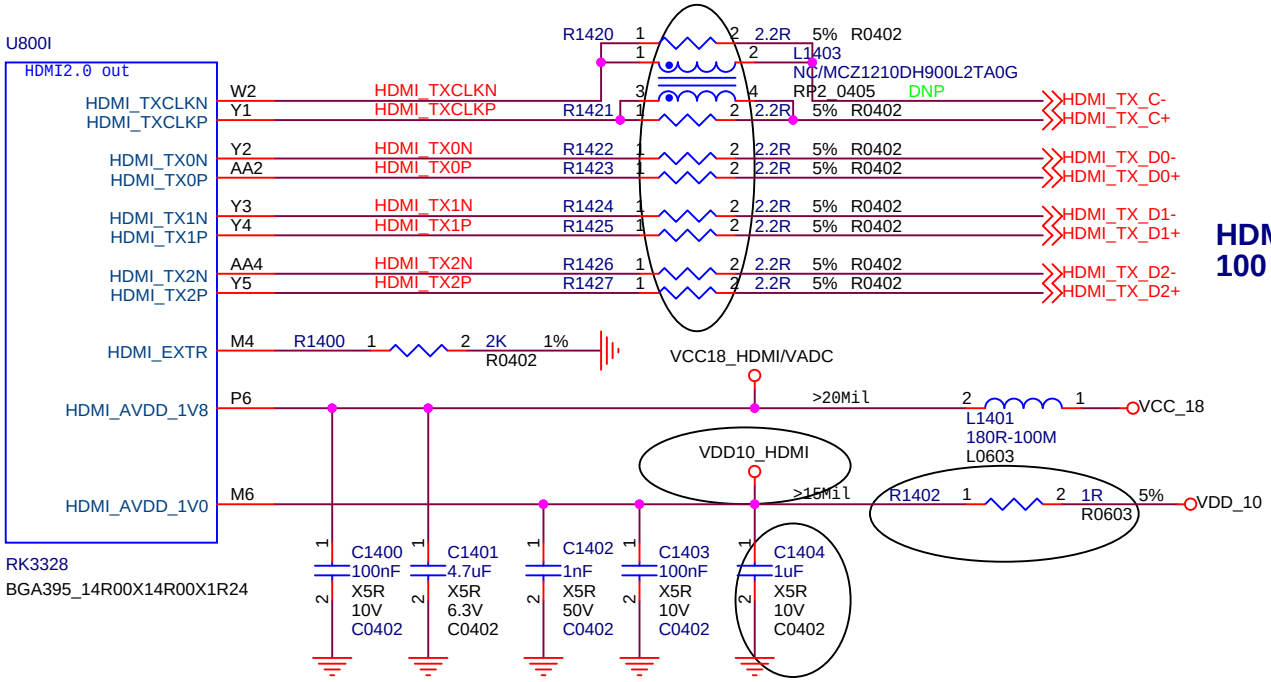

HDMI TMDS trace
100 Ohm +-10%

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Demo6		
File:	RK3328 HDMI PHY		
Date:	Tuesday, July 18, 2017	Rev:	V1.1
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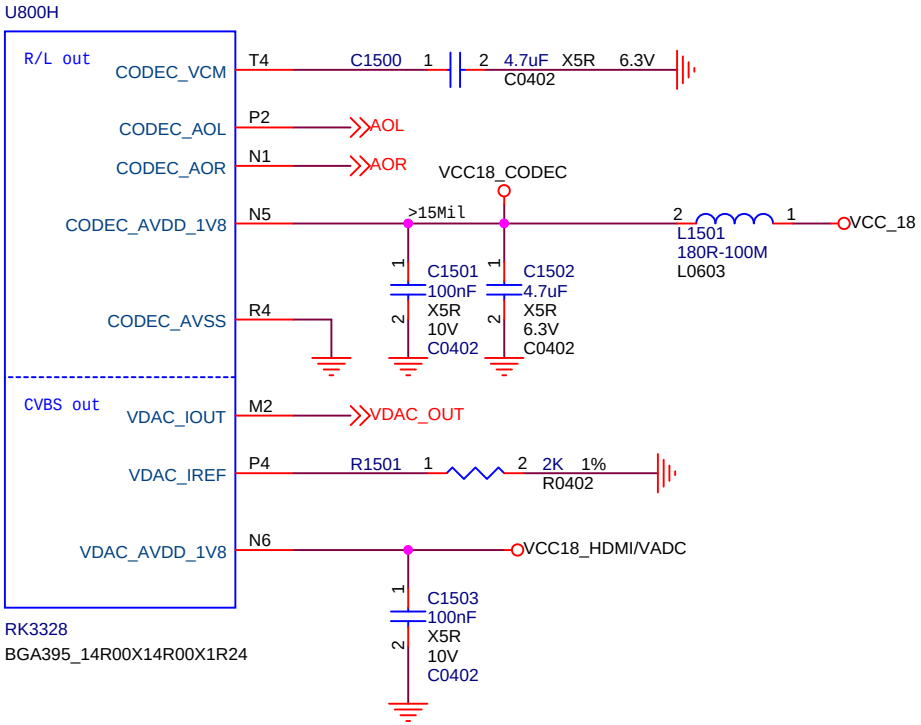

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	**RK3328_BOX_Demo6**		
File:	**RK3328 AV Interface**		
Date:	Tuesday, July 18, 2017	Rev:	V1.1
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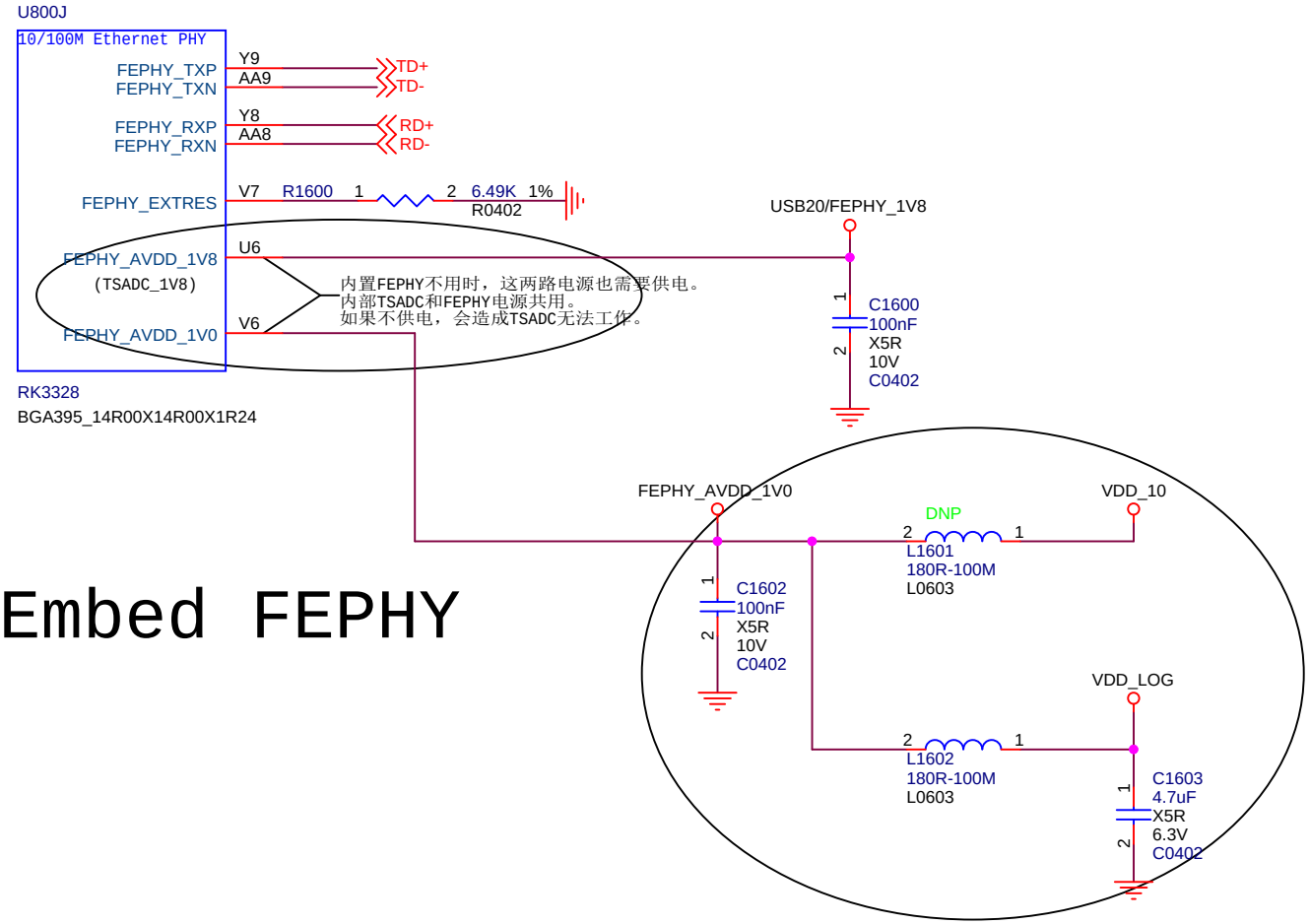

Embed FEPHY

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Demo6		
File:	RK3328 FEPHY		
Date:	Tuesday, July 18, 2017	Rev:	V1.1
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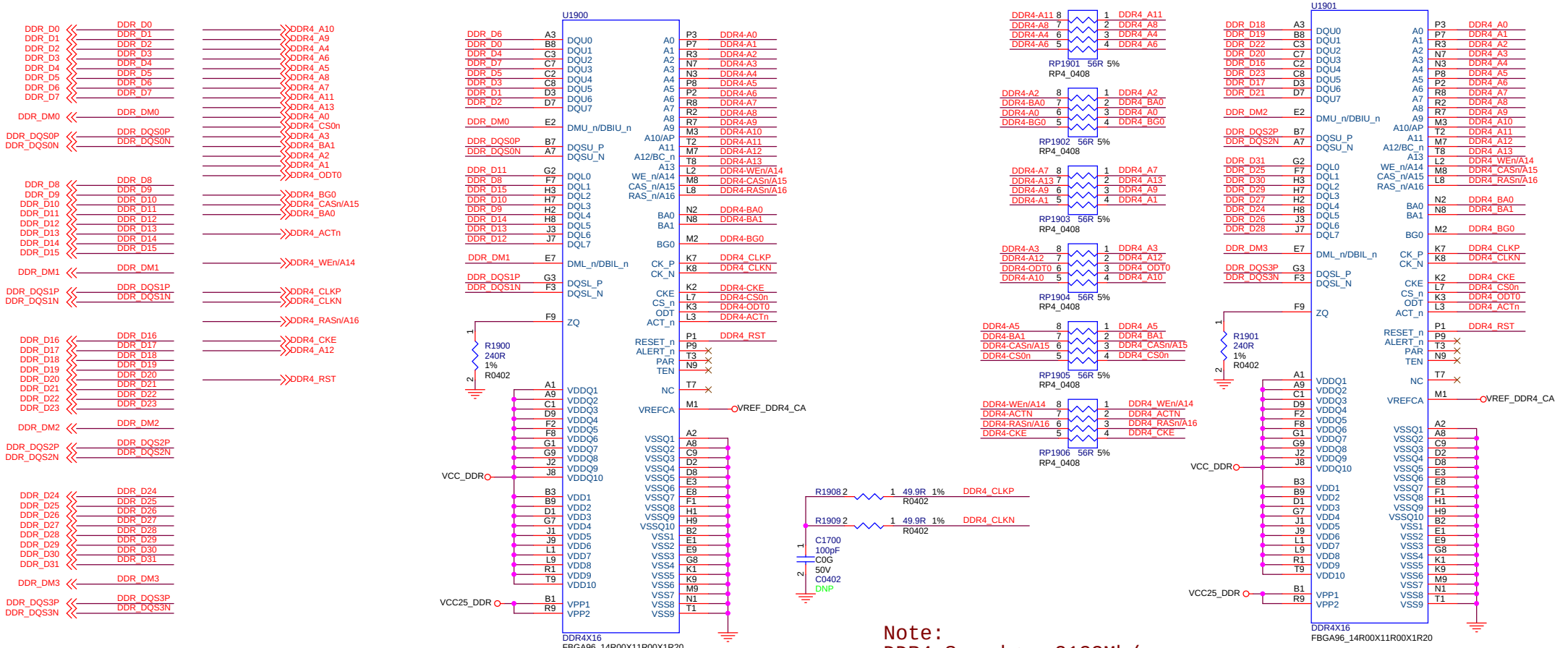
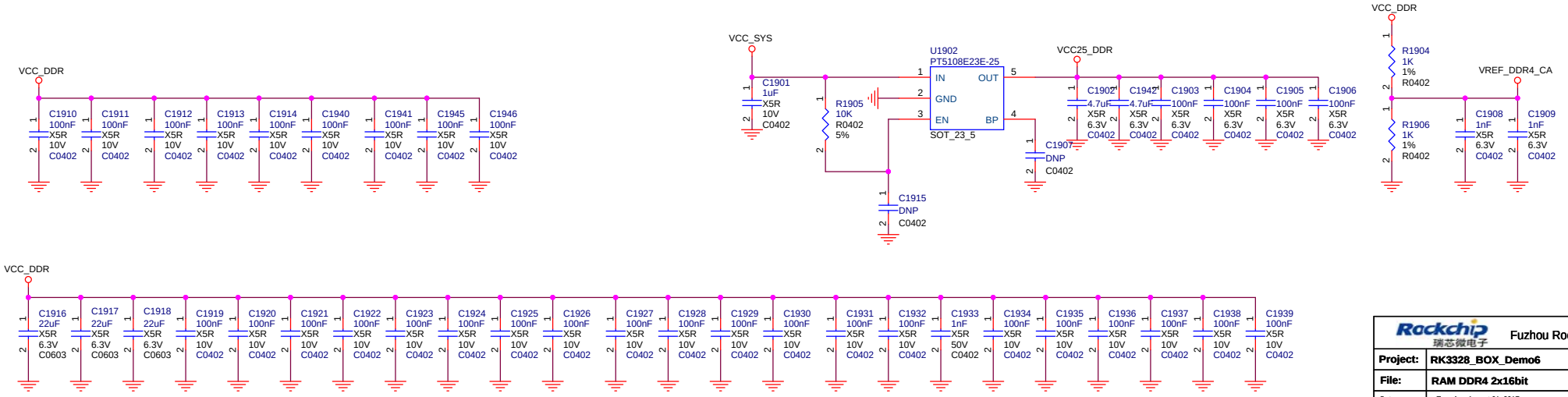


2X16bit DDR4

Note:
DDR4 Speed > =2133Mb/s
4 layer board



Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Demo6		
File:	RAM DDR4 2x16bit		
Date:	Tuesday, August 01, 2017	Rev:	V1.0
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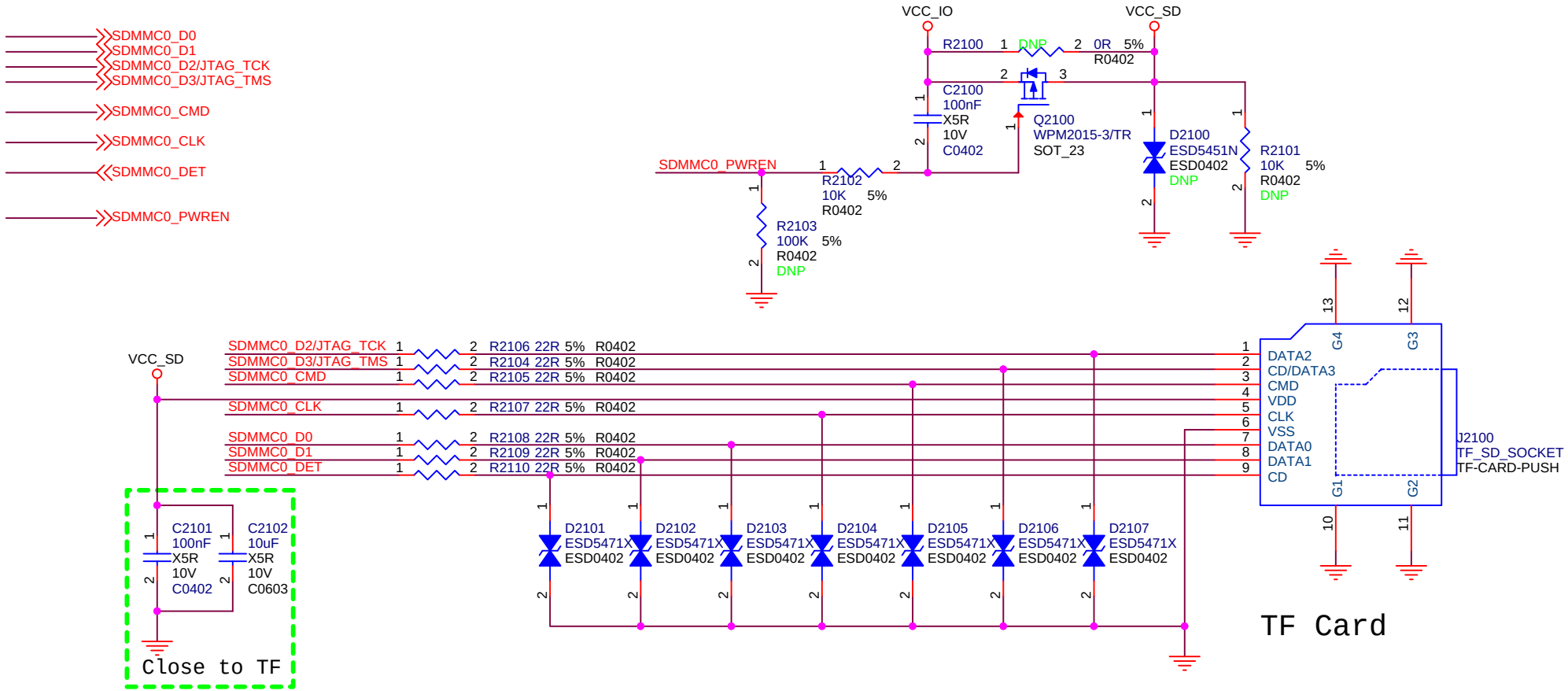

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Demo6		
File:	TF/SD Card		
Date:	Tuesday, July 18, 2017	Rev:	V1.1
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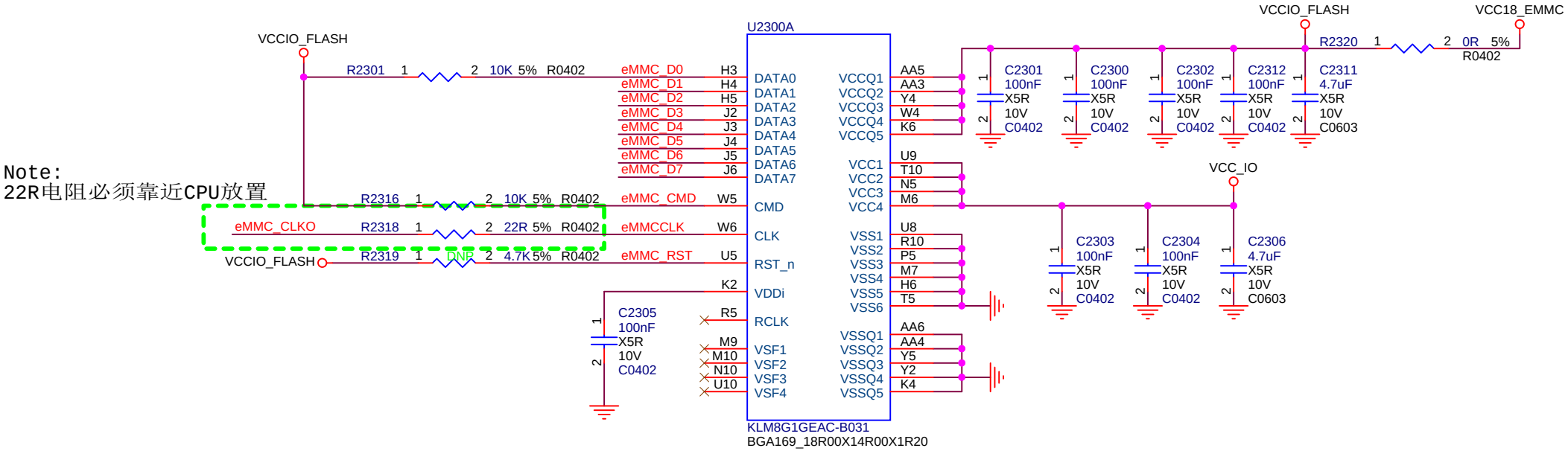
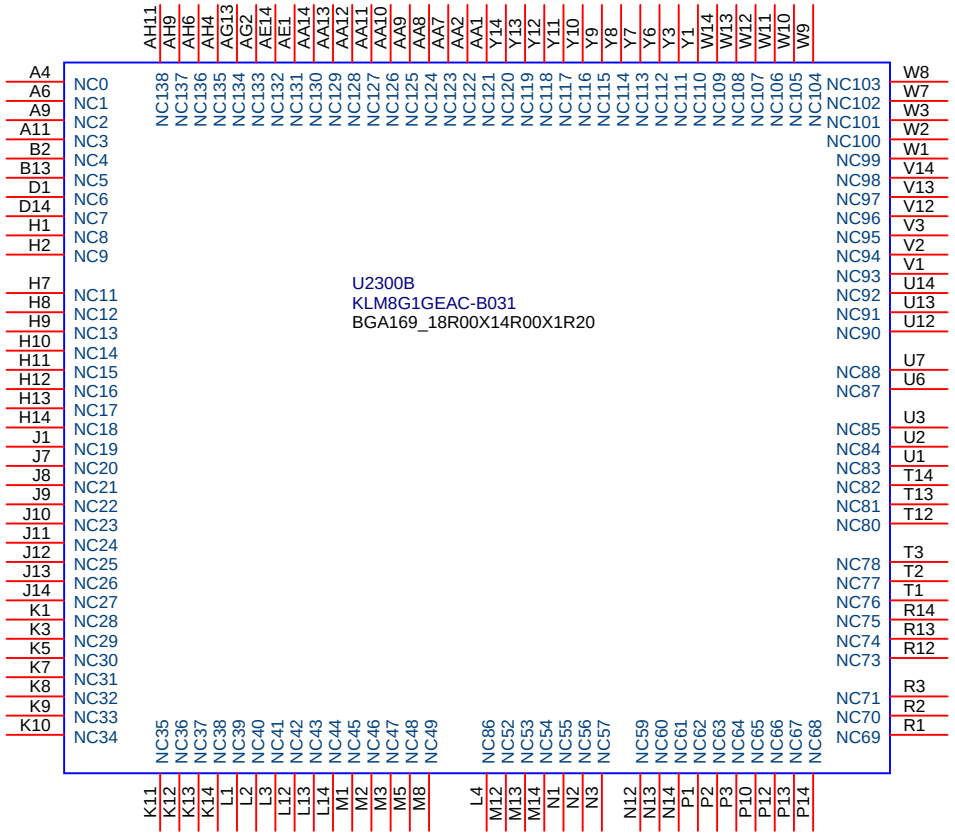
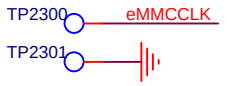
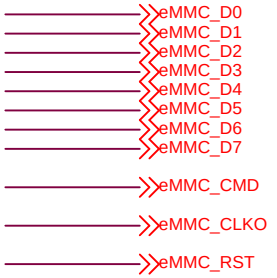






Note:
eMMC Update.



Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Demo6		
File:	Flash-eMMC		
Date:	Tuesday, July 18, 2017	Rev:	V1.1
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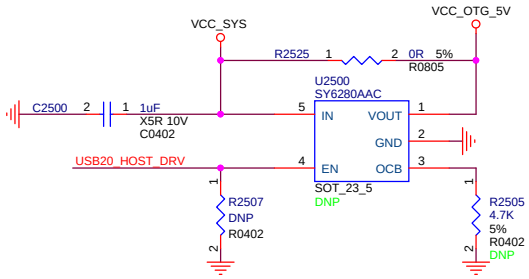

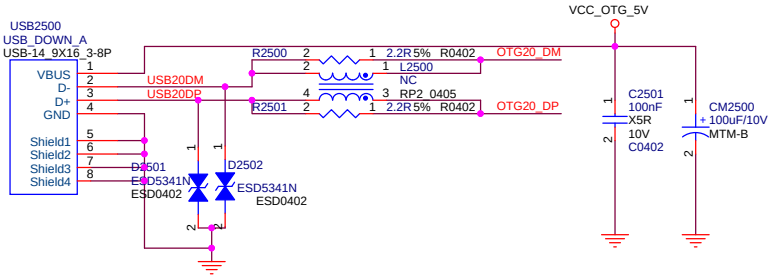

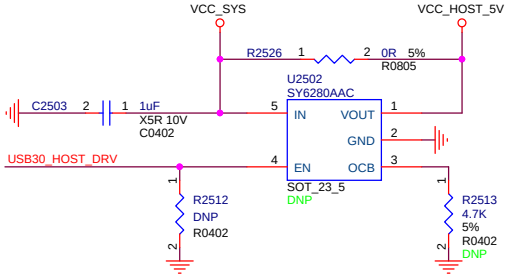

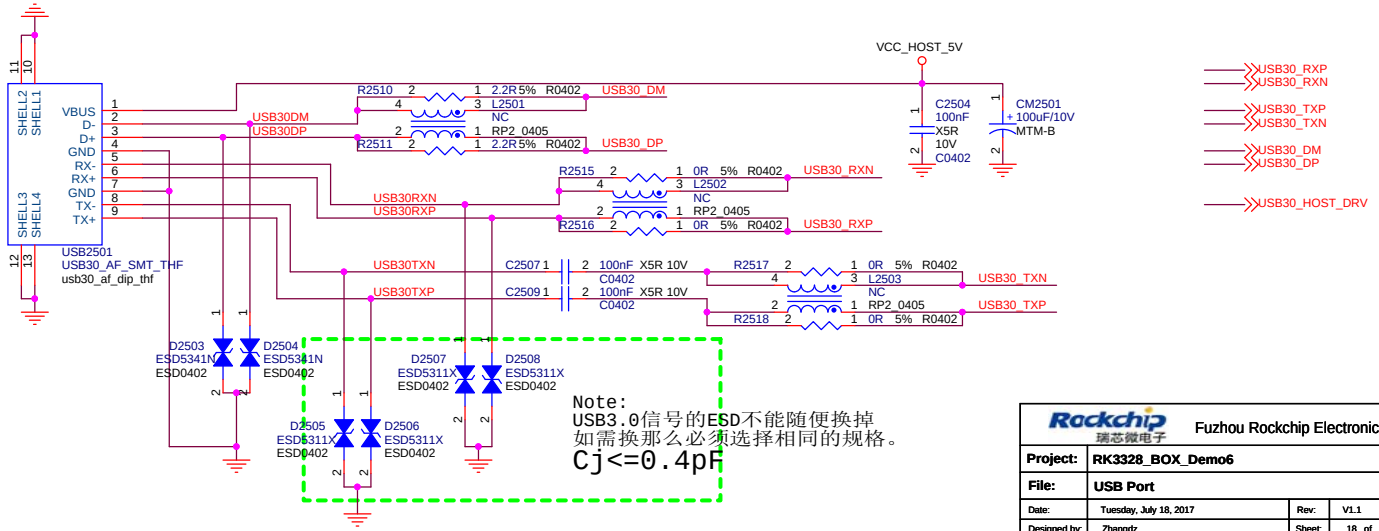

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Demo6		
File:	USB Port		
Date:	Tuesday, July 18, 2017	Rev:	V1.1
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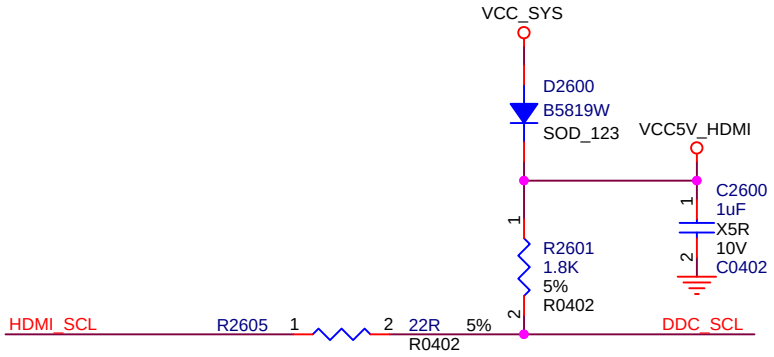
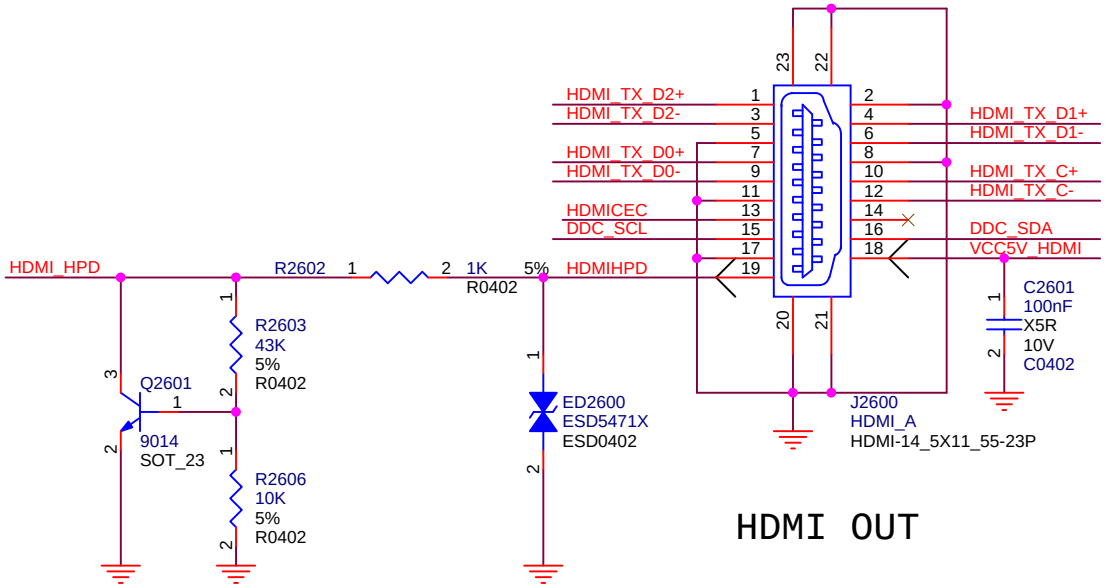
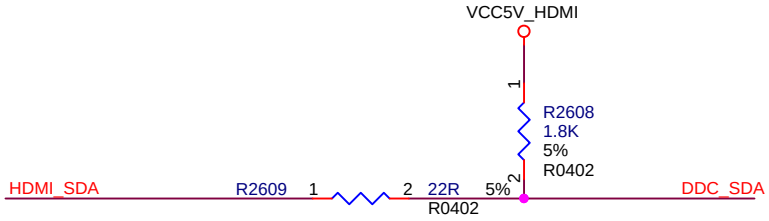
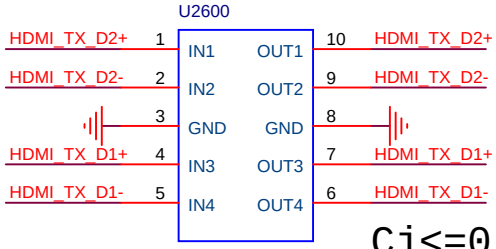




HDMI OUT





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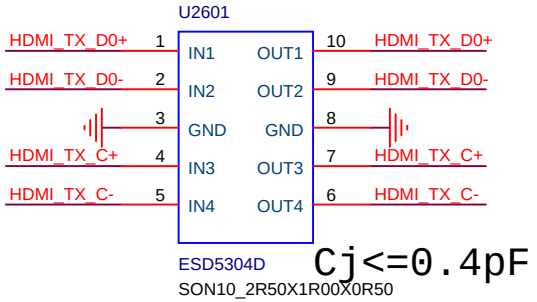

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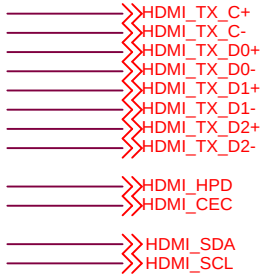

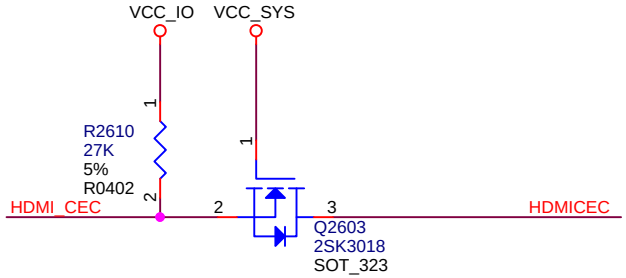

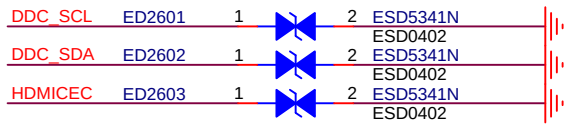

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Demo6		
File:	HDMI OUT Port		
Date:	Tuesday, July 18, 2017	Rev:	V1.1
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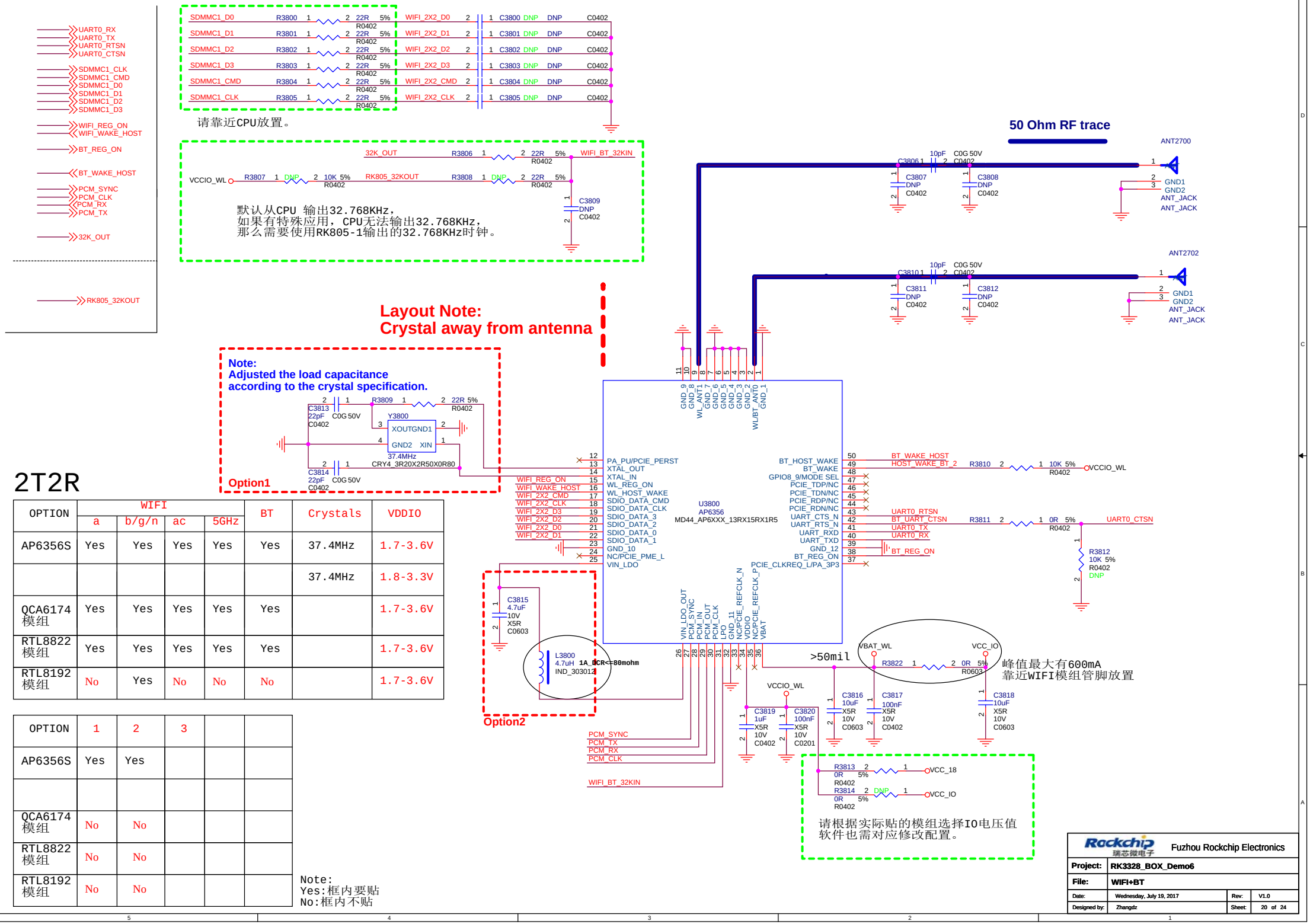


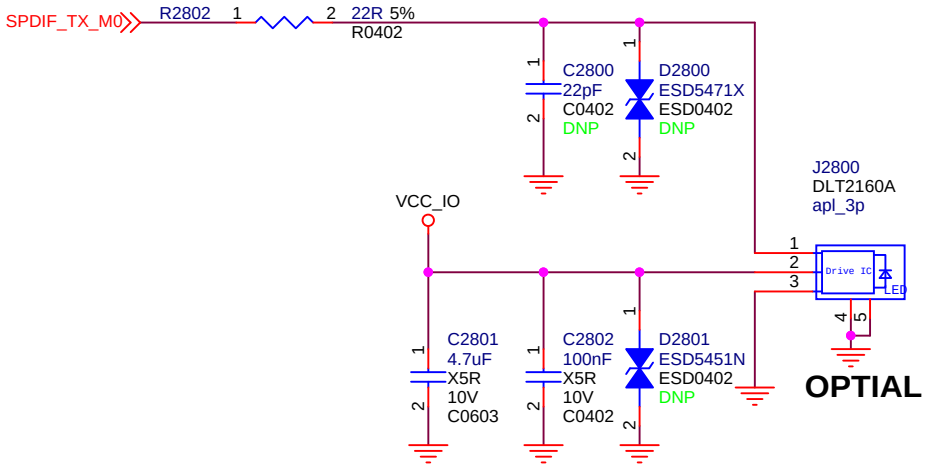
2T2R

OPTION	WIFI				BT	Crystals	VDDIO
	a	b/g/n	ac	5GHz			
AP6356S	Yes	Yes	Yes	Yes	Yes	37.4MHz	1.7-3.6V
						37.4MHz	1.8-3.3V
QCA6174模组	Yes	Yes	Yes	Yes	Yes		1.7-3.6V
RTL8822模组	Yes	Yes	Yes	Yes	Yes		1.7-3.6V
RTL8192模组	No	Yes	No	No	No		1.7-3.6V

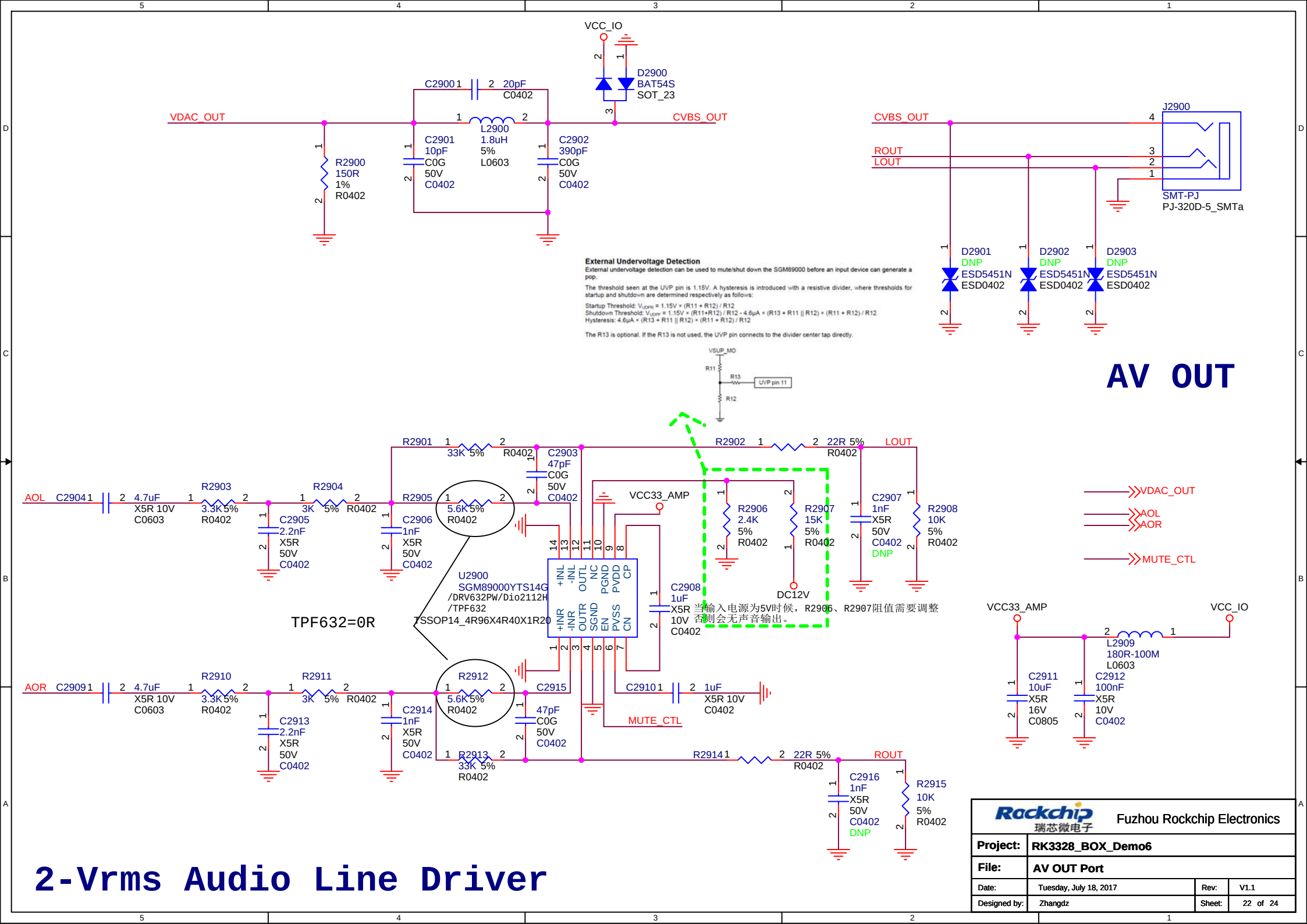
OPTION	1	2	3		
AP6356S	Yes	Yes			
QCA6174模组	No	No			
RTL8822模组	No	No			
RTL8192模组	No	No			

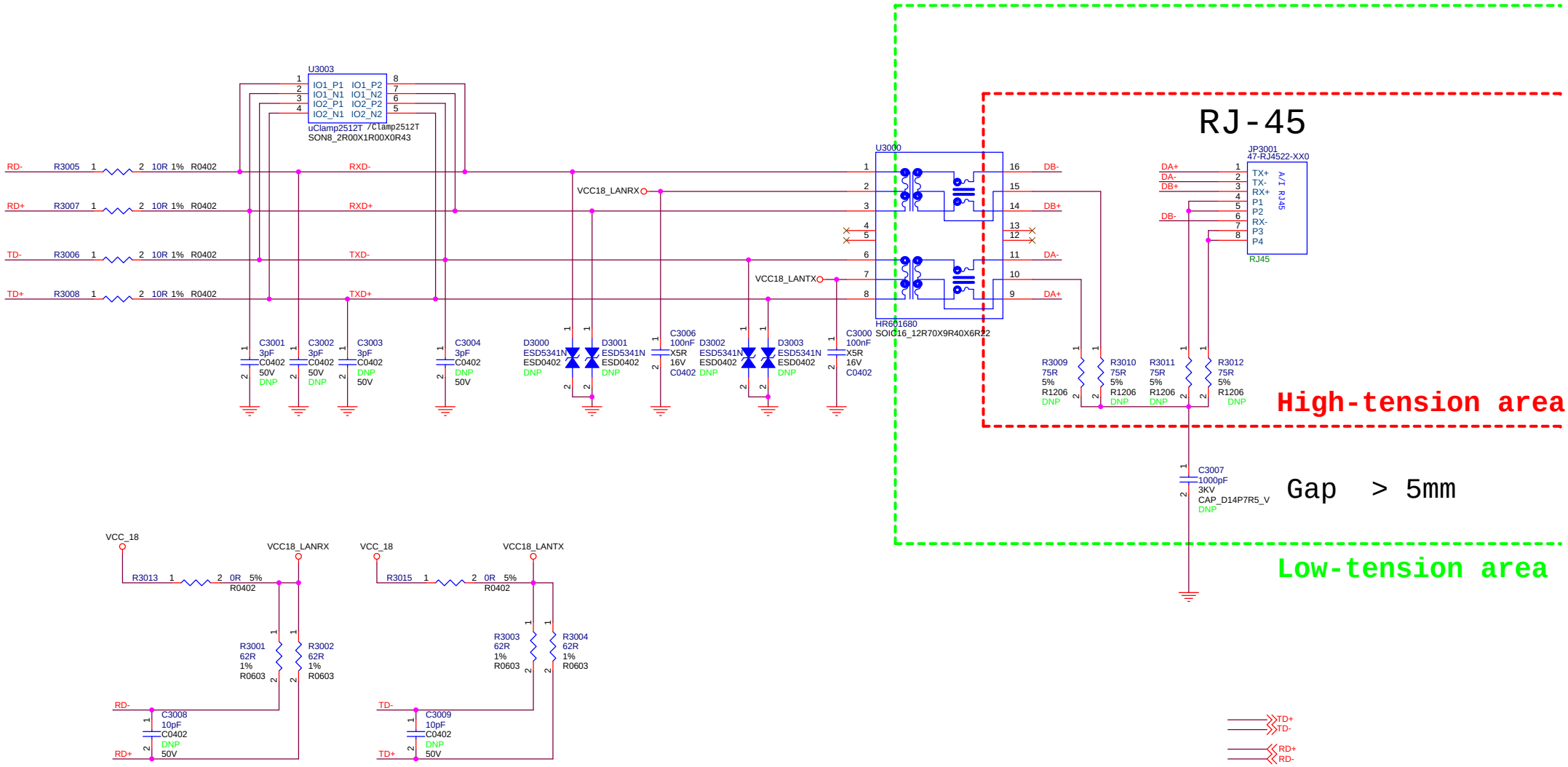
Note:
Yes:框内要贴
No:框内不贴

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Demo6		
File:	WIFI+BT		
Date:	Wednesday, July 19, 2017	Rev:	V1.0
Designed by:	Zhangdz	Sheet:	20 of 24



Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Demo6		
File:	S/PDIF Port		
Date:	Tuesday, July 18, 2017	Rev:	V1.1
Designed by:	Zhangdz	Sheet:	21 of 24


VCC_IO
D2900
BAT54S
SOT_23
C2900 1 2 20pF
C0402
VDAC_OUT
CVBS_OUT
L2900
1.8uH
5%
L0603
R2900
150R
1%
R0402
C2901
10pF
C0G
50V
C0402
C2902
390pF
C0G
50V
C0402
J2900
CVBS_OUT
ROUT
LOUT
SMT-PJ
PJ-320D-5_SMTa
D2901
DNP
ESD5451N
ESD0402
D2902
DNP
ESD5451N
ESD0402
D2903
DNP
ESD5451N
ESD0402
External Undervoltage Detection
External undervoltage detection can be used to mute/shut down the SGM89000 before an input device can generate a pop.
The threshold seen at the UVP pin is 1.15V. A hysteresis is introduced with a resistive divider, where thresholds for startup and shutdown are determined respectively as follows:
Startup Threshold: V_UDRR = 1.15V × (R11 + R12) / R12
Shutdown Threshold: V_UDF = 1.15V × (R11+R12) / R12 - 4.6μA × (R13 + R11 || R12) × (R11 + R12) / R12
Hysteresis: 4.6μA × (R13 + R11 || R12) × (R11 + R12) / R12
The R13 is optional. If the R13 is not used, the UVP pin connects to the divider center tap directly.
VSUP_MO
R11
R13
UVP pin 11
R12
AV OUT
R2901 1 33K 5% 2 R0402
C2903
47pF
C0G
50V
C0402
R2902 1 22R 5% 2 R0402
LOUT
AOL
C2904 1 2 4.7uF
X5R 10V
C0603
R2903
3.3K 5%
R0402
R2904
3K 5% R0402
R2905 1 5.6K 5% 2 R0402
C2905
2.2nF
X5R
50V
C0402
C2906
1nF
X5R
50V
C0402
VCC33_AMP
R2906
2.4K
5%
R0402
R2907
15K
5%
R0402
DC12V
C2907
1nF
X5R
50V
C0402
DNP
R2908
10K
5%
R0402
VDAC_OUT
AOL
AOR
MUTE_CTL
U2900
SGM89000YTS14G
/DRV632PW/Dio2112H
/TPF632
TSSOP14_4R96X4R40X1R20
+INL
-INL
OUTL
NC
PGND
PVDD
CP
+INR
-INR
OUTR
SGND
EN
PVSS
CN
C2908
1uF
X5R
10V
C0402
TPF632=0R
当输入电源为5V时候，R2906、R2907阻值需要调整
否则会无声音输出。
VCC33_AMP
VCC_IO
L2909
180R-100M
L0603
C2911
10uF
X5R
16V
C0805
C2912
100nF
X5R
10V
C0402
AOR
C2909 1 2 4.7uF
X5R 10V
C0603
R2910
3.3K 5%
R0402
R2911
3K 5% R0402
R2912 1 5.6K 5% 2 R0402
C2913
2.2nF
X5R
50V
C0402
C2914
1nF
X5R
50V
C0402
C2915
47pF
C0G
50V
C0402
C2910 1 2 1uF
X5R 10V
C0402
MUTE_CTL
R2913 1 33K 5% 2 R0402
R2914 1 2 22R 5% R0402
ROUT
C2916
1nF
X5R
50V
C0402
DNP
R2915
10K
5%
R0402
2-Vrms Audio Line Driver
Rockchip 瑞芯微电子
Fuzhou Rockchip Electronics
Project: RK3328_BOX_Demo6
File: AV OUT Port
Date: Tuesday, July 18, 2017
Rev: V1.1
Designed by: Zhangdz
Sheet: 22 of 24



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Project:	RK3328_BOX_Demo6		
File:	10/100M-Embed PHY		
Date:	Tuesday, July 18, 2017	Rev:	V1.1
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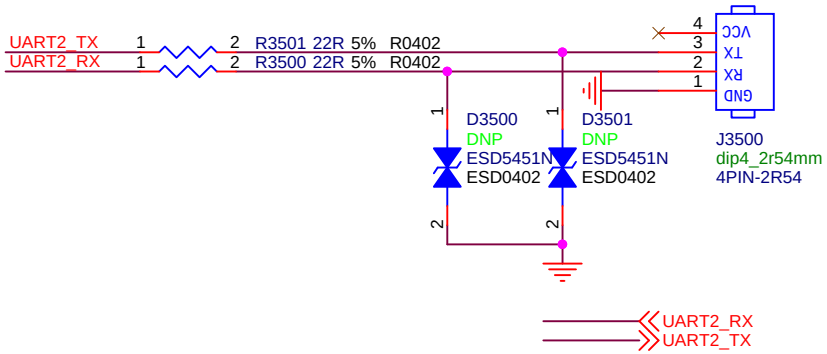

Debug UART2

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Demo6		
File:	Debug UART2/JTAG		
Date:	Tuesday, July 18, 2017	Rev:	V1.1
Designed by:	<designer>	Sheet:	24 of 24