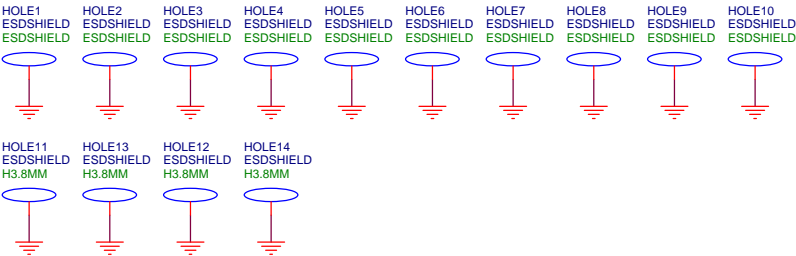


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RK3328



Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

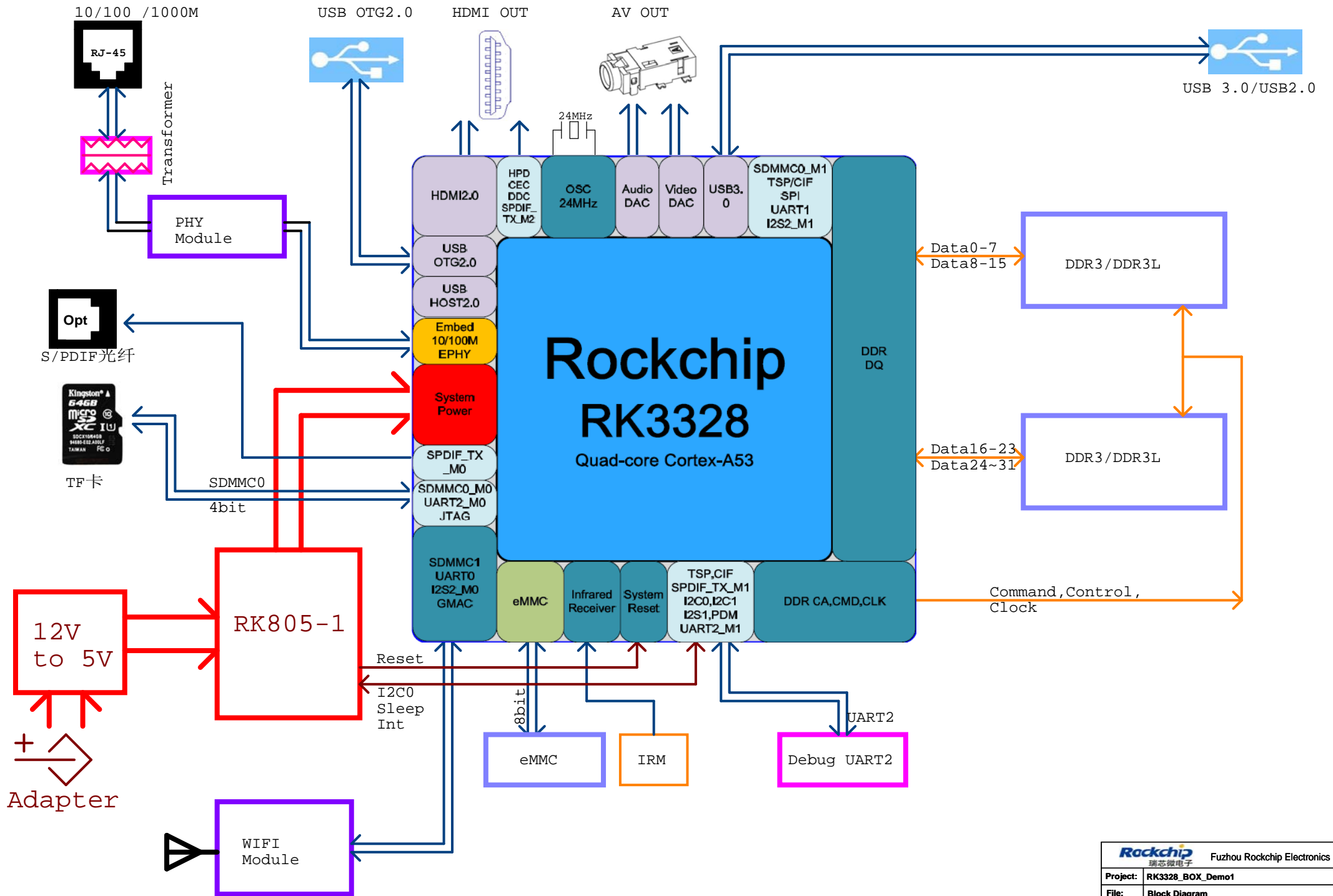
Note:

Component parameter description

- 1. DNP stands for component not mounted temporarily
- 2. If Value or option is DNP, which means the area is reserved without being mounted

Version	Date	Author	Change Note	Approved
V1.0	20170223	ZDZ	First edictor	
V1.1	20170718	ZDZ	1: 修改记录请见: RK3328_BOX_DEMO1_RK805-1_DDR3P216SD4_V11_SCH_Modify_Notes	

 <div style="display: inline-block; vertical-align: middle; margin-left: 10px;"> <b>Fuzhou Rockchip Electronics</b>          瑞芯微电子       </div>	
<b>Project:</b>	<b>RK3328_BOX_Demo1</b>
<b>File:</b>	<b>Change List</b>
<b>Date:</b>	Wednesday, July 19, 2017
<b>Rev:</b>	V1.1
<b>Designed by:</b>	Zhangdz
<b>Sheet:</b>	2 of 24



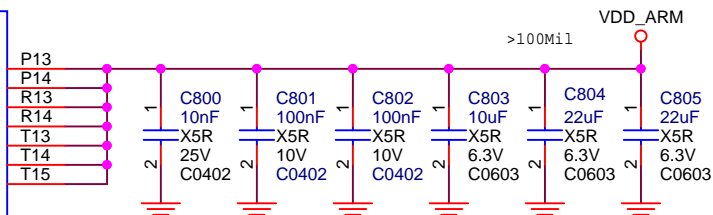




U800N

ARM

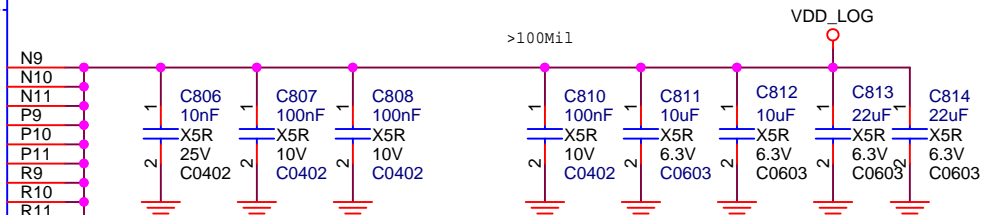
VDD\_CORE  
VDD\_CORE  
VDD\_CORE  
VDD\_CORE  
VDD\_CORE  
VDD\_CORE  
VDD\_CORE



PCB LAYOUT注意: 电容都要靠近主控, 其中一个22uF电容需要放在管脚正下方。

GPU/Logic

VDD\_LOGIC  
VDD\_LOGIC  
VDD\_LOGIC  
VDD\_LOGIC  
VDD\_LOGIC  
VDD\_LOGIC  
VDD\_LOGIC  
VDD\_LOGIC  
VDD\_LOGIC  
VDD\_LOGIC

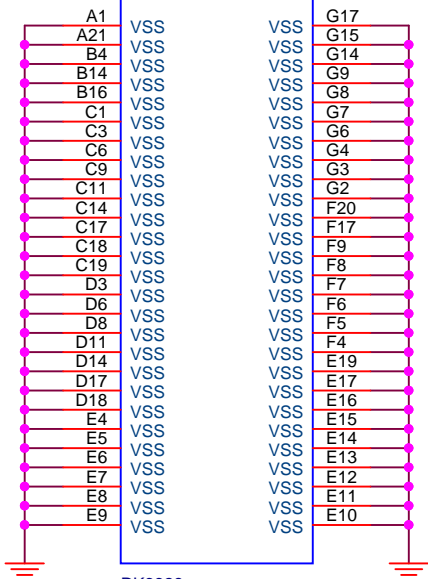


PCB LAYOUT注意: 电容都要靠近主控, 其中一个22uF电容需要放在管脚正下方。

RK3328

BGA395\_14R00X14R00X1R24

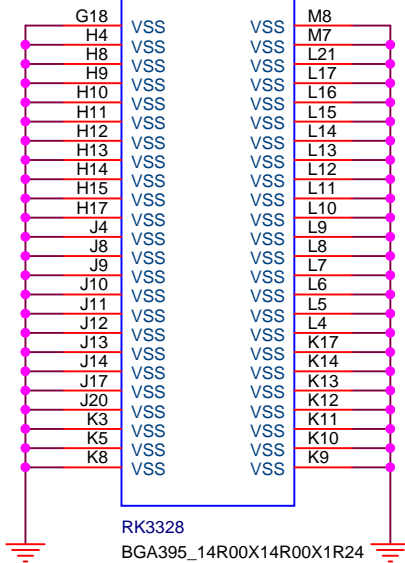
U800O



RK3328

BGA395\_14R00X14R00X1R24

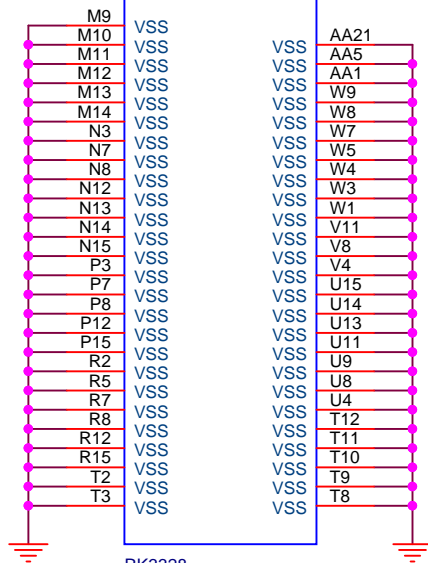
U800P



RK3328

BGA395\_14R00X14R00X1R24

U800Q



RK3328

BGA395\_14R00X14R00X1R24



Fuzhou Rockchip Electronics

Project:	RK3328_BOX_Demo1		
File:	RK3328 Power		
Date:	Tuesday, July 18, 2017	Rev:	V1.1
Designed by:	Zhangdz	Sheet:	6 of 24

U800A

OSC

XOUT24M

T1

R900

1

2

22R

5%

R0402

1

5%

C900

12pF

C0G

50V

C0402

4

3

Y900

XOUTGND1

2

1

GND2

XIN

1

24MHz

CRY4\_3R20X2R50X0R80

1

C901

12pF

C0G

50V

C0402

2

XIN24M

R1

PLL Power

PLL\_DVDD\_1V0

H7

PLL\_AVDD\_1V8

H5

SARADC

SARADC\_IN0

SARADC\_IN1

SARADC\_AVDD\_1V8

M18

RECOVER

SARADC\_IN1

M17

M16

VCC\_18

N16

P16

C910

100nF

X5R

10V

C0402

VDDPLL/USB30\_1V0

>12Mil

C903

100nF

X5R

10V

C0402

C904

1uF

X5R

10V

C0402

L900

180R-100M

L0603

VDD\_10

C905

4.7uF

X5R

6.3V

C0402

VDDPLL/USB30\_1V8

>12Mil

C907

100nF

X5R

10V

C0402

C908

1uF

X5R

10V

C0402

L901

180R-100M

L0603

VCC\_18

C909

4.7uF

X5R

6.3V

C0402

RK3328

BGA395\_14R00X14R00X1R24

VCC\_18 R906 1 2 10K 5% SARADC\_IN1

R0402

R908

10K

5%

R0402

DNP

C913 2 1 100nF X5R

10V

C0402

VCC\_18 R909 1 2 10K 5% R0402

R0402

RECOVER

R911

22R

5%

R0402

1

2

SW900

RECOVER\_key

TS-3220S

D900

ESD5451N

ESD0402

SARADC_IN0 BOM版本	SARADC_IN1 PCB版本	Up阻值	Down阻值	
Recover		DNP	10K	
BOM1		110K	10K	
BOM2		100K	20K	
BOM3		100K	33K	
BOM4		36K	18K	
BOM5		51K	36K	
BOM6		51K	51K	
BOM7		36K	51K	
BOM8		18K	36K	
BOM9		33K	100K	
BOM10		20K	100K	
BOM11		10K	110K	
BOM12		10K	DNP	

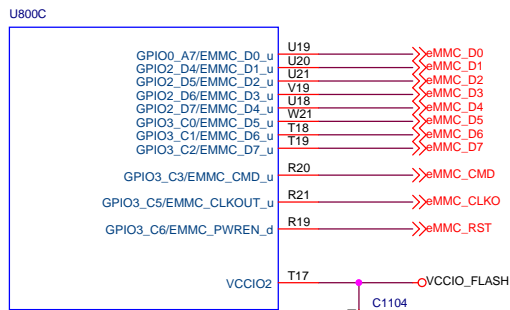
**Rockchip**  
瑞芯微电子

Fuzhou Rockchip Electronics

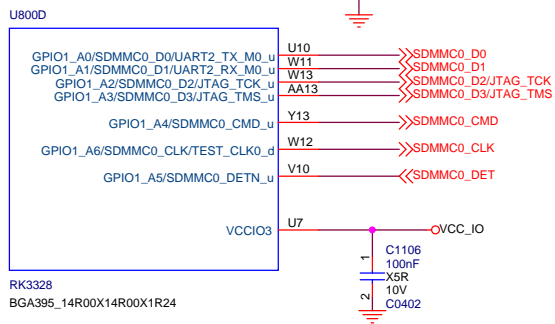
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<b>File:</b>	RK3328 OSC/PLL/OTP/SARADC		
<b>Date:</b>	Tuesday, July 18, 2017	<b>Rev:</b>	V1.1
<b>Designed by:</b>	Zhangdz	<b>Sheet:</b>	7 of 24



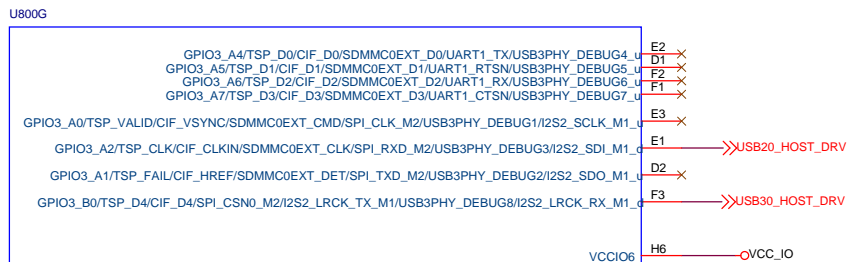




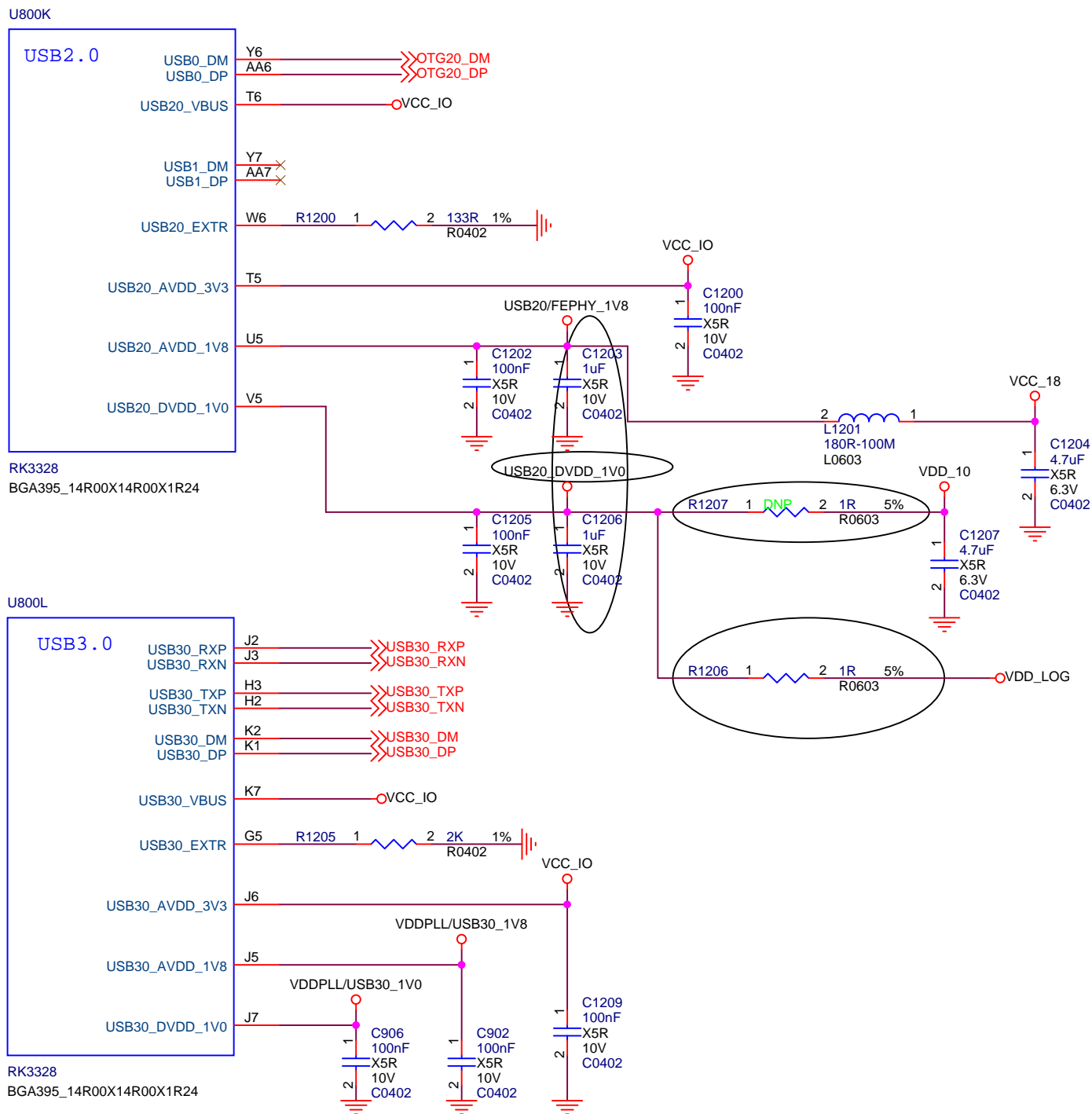
RK3328  
BGA395\_14R00X14R00X1R24



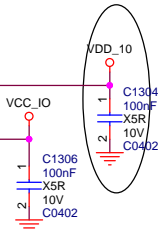
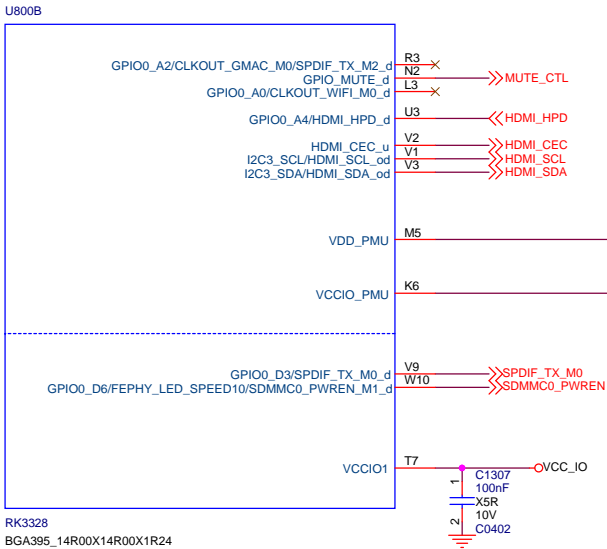
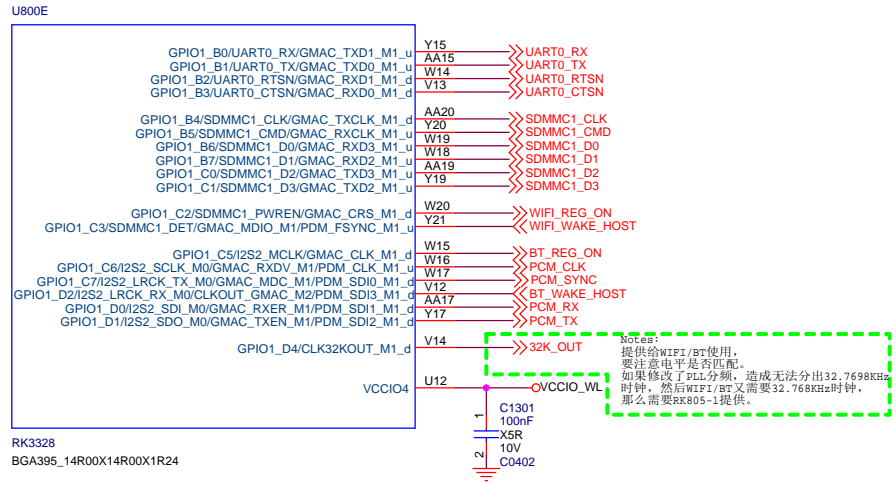
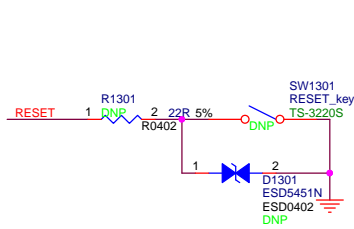
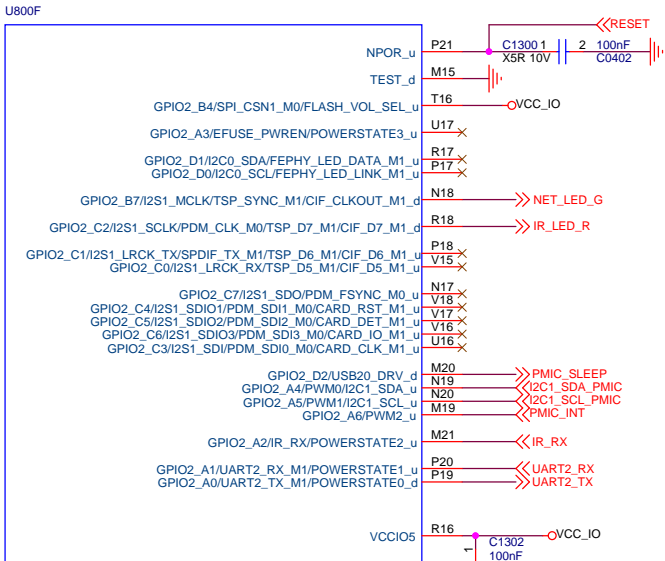
RK3328  
BGA395\_14R00X14R00X1R24



RK3328  
BGA395\_14R00X14R00X1R24



 瑞芯微电子		Fuzhou Rockchip Electronics	
Project:	RK3328_BOX_Demo1		
File:	RK3328 USB2 PHY/USB3 PHY		
Date:	Tuesday, July 18, 2017	Rev:	V1.1
Designed by:	Zhangdz	Sheet:	10 of 24



U800I

HDMI2.0 out

HDMI\_TXCLKN  
HDMI\_TXCLKP

HDMI\_TX0N  
HDMI\_TX0P

HDMI\_TX1N  
HDMI\_TX1P

HDMI\_TX2N  
HDMI\_TX2P

HDMI\_EXTR

HDMI\_AVDD\_1V8

HDMI\_AVDD\_1V0

RK3328

BGA395\_14R00X14R00X1R24

R1420 1 2 2.2R 5% R0402

L1403

NC/MCZ1210DH900L2TA0G

RP2\_0405 DNP

R1421 1 2 2.2R 5% R0402

R1422 1 2 2.2R 5% R0402

R1423 1 2 2.2R 5% R0402

R1424 1 2 2.2R 5% R0402

R1425 1 2 2.2R 5% R0402

R1426 1 2 2.2R 5% R0402

R1427 1 2 2.2R 5% R0402

HDMI\_TX\_C-  
HDMI\_TX\_C+

HDMI\_TX\_D0-  
HDMI\_TX\_D0+

HDMI\_TX\_D1-  
HDMI\_TX\_D1+

HDMI\_TX\_D2-  
HDMI\_TX\_D2+

HDMI TMDS trace  
100 Ohm +-10%

VCC18\_HDMI/VADC

>20Mil

VCC\_18

VDD10\_HDMI

>15Mil

VDD\_10

1

C1400

100nF

X5R

10V

C0402

2

1

C1401

4.7uF

X5R

6.3V

C0402

2

1

C1402

1nF

X5R

50V

C0402

2

1

C1403

100nF

X5R

10V

C0402

2

1

C1404

1uF

X5R

10V

C0402

2

2

L1401

180R-100M

L0603

1

R1402

1

2

1R

5%

R0603

2

1



Fuzhou Rockchip Electronics

Project: RK3328\_BOX\_Demo1

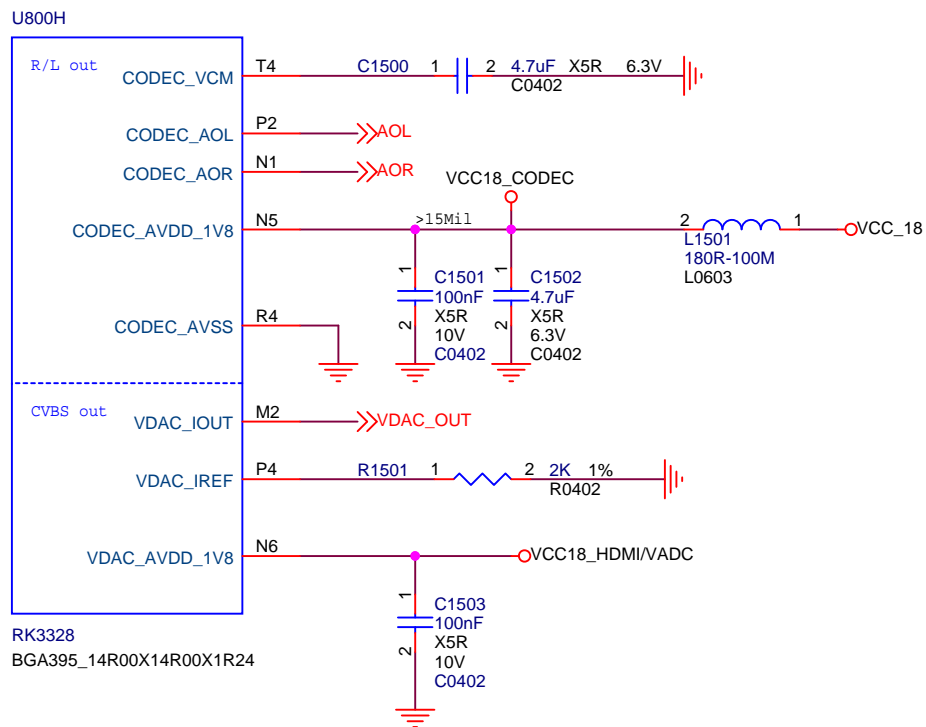
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Date: Tuesday, July 18, 2017

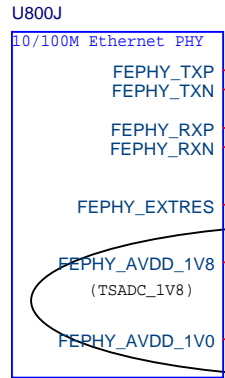
Rev: V1.1

Designed by: Zhangdz

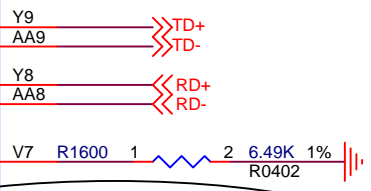
Sheet: 12 of 24



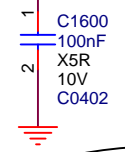
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Project:	RK3328_BOX_Demo1		
File:	RK3328 AV Interface		
Date:	Tuesday, July 18, 2017	Rev:	V1.1
Designed by:	Zhangdz	Sheet:	13 of 24



RK3328  
BGA395\_14R00X14R00X1R24



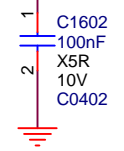
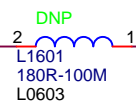
USB20/FEPHY\_1V8



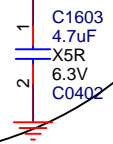
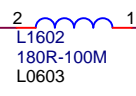
内置FEPHY不用时，这两路电源也需要供电。  
内部TSADC和FEPHY电源共用。  
如果不供电，会造成TSADC无法工作。

FEPHY\_AVDD\_1V0


VDD\_10

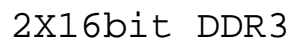


VDD\_LOG



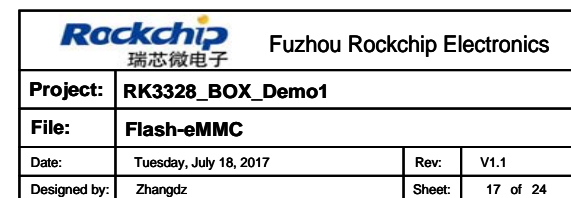
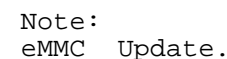
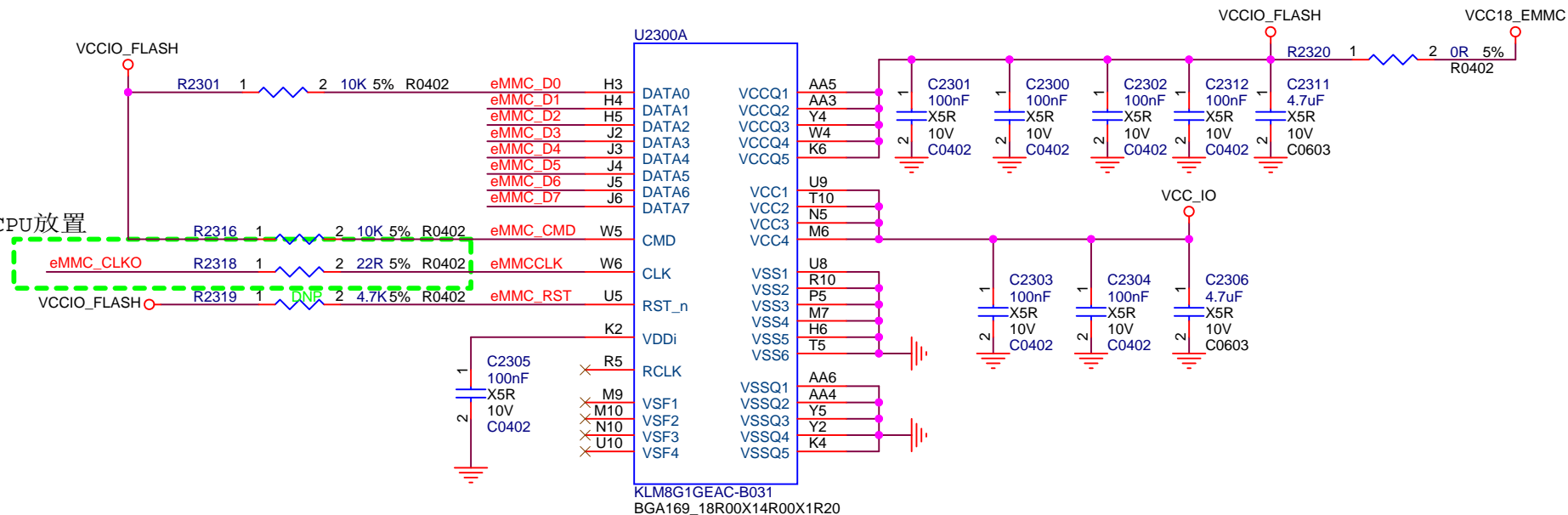
Embed FEPHY

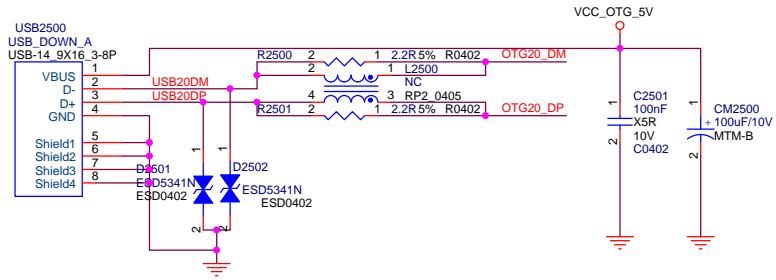
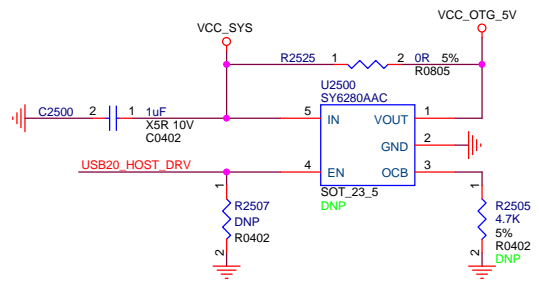
 瑞芯微电子		Fuzhou Rockchip Electronics	
Project:	RK3328_BOX_Demo1		
File:	RK3328 FEPHY		
Date:	Tuesday, July 18, 2017	Rev:	V1.1
Designed by:	Zhangdz	Sheet:	14 of 24



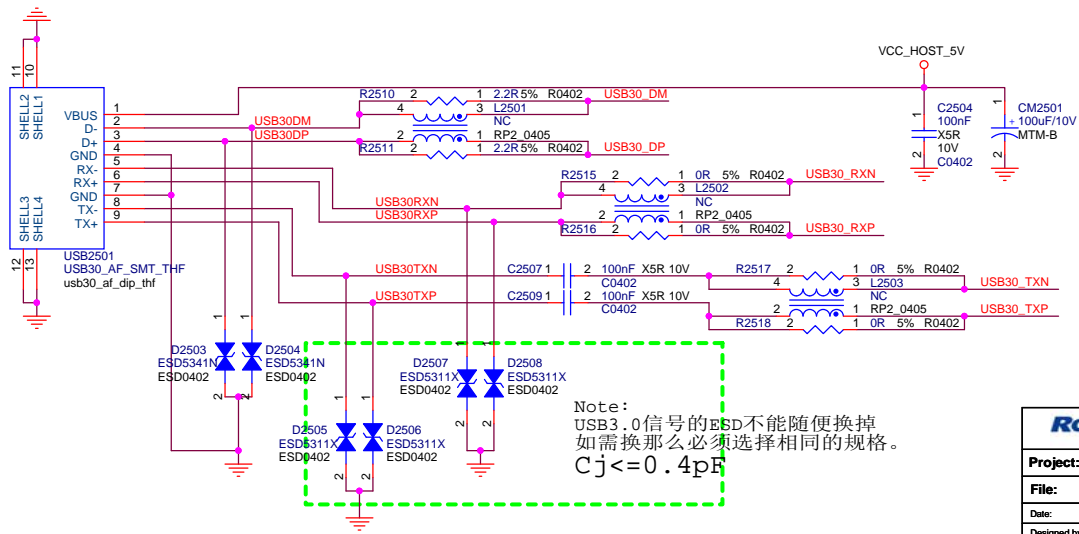
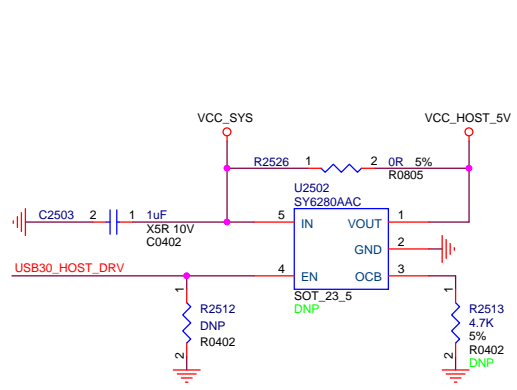






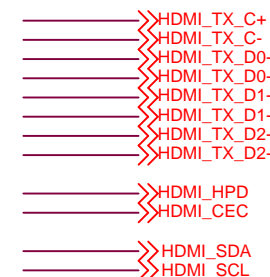
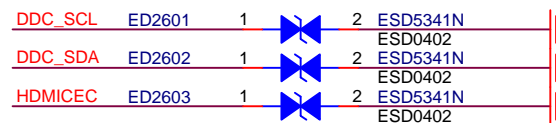
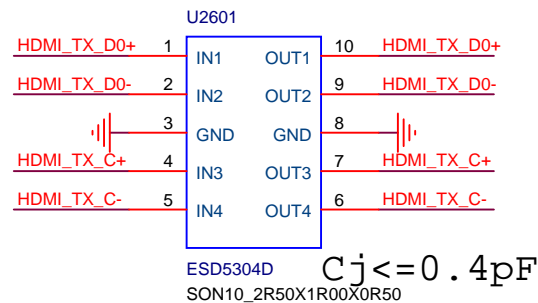
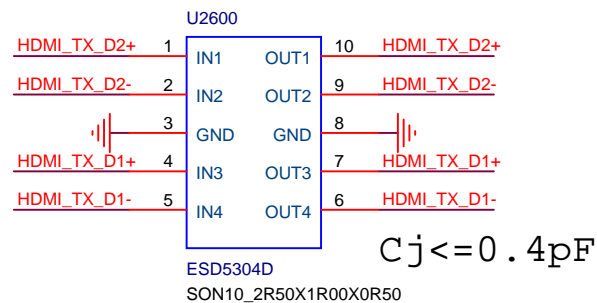
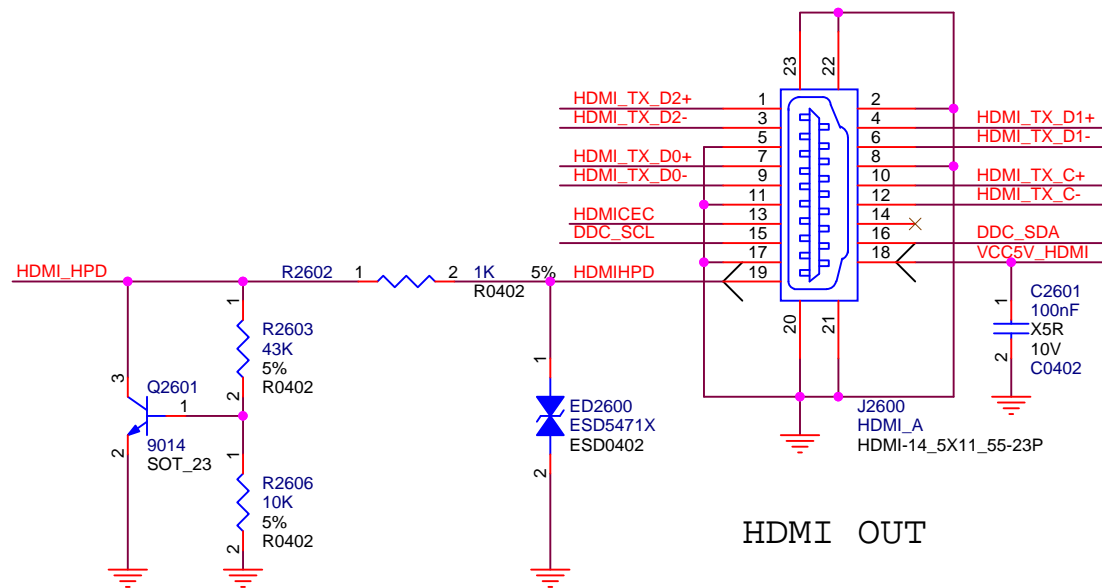
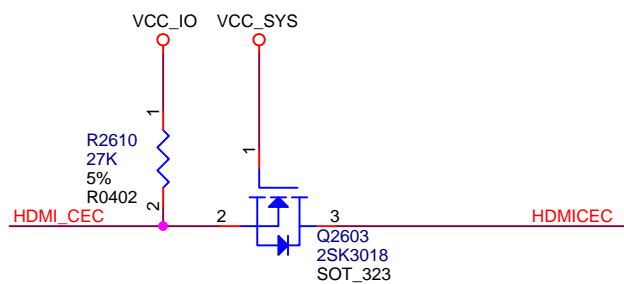
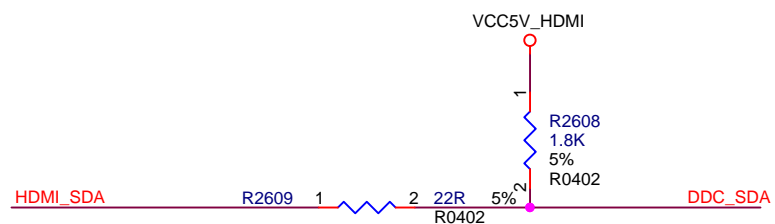
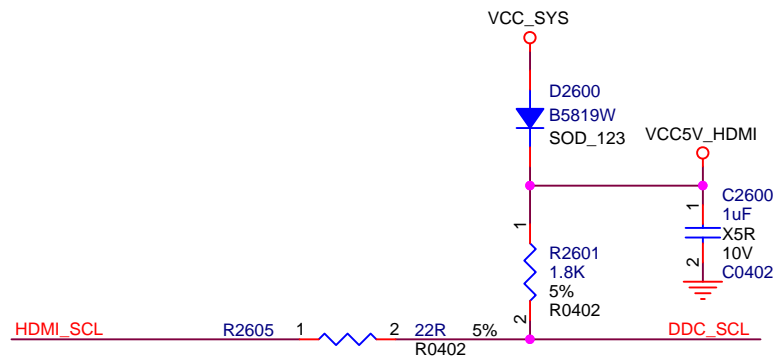


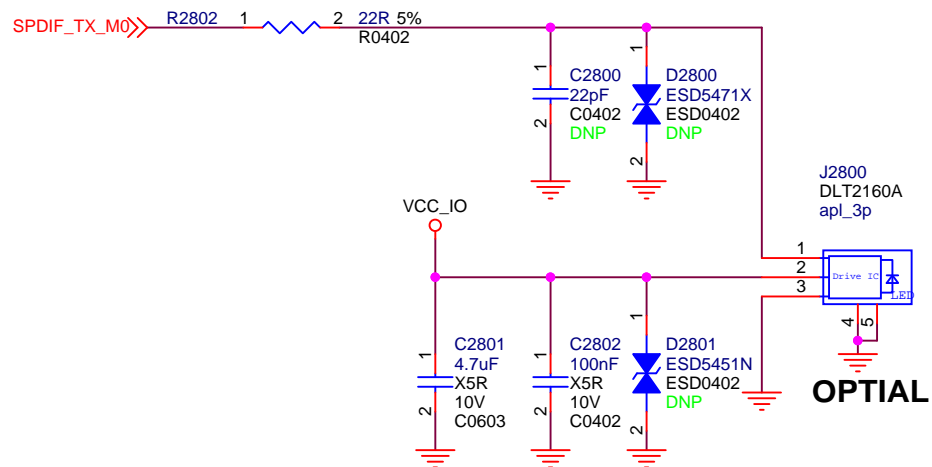
OTG20\_DM  
OTG20\_DP  
USB20\_HOST\_DRV




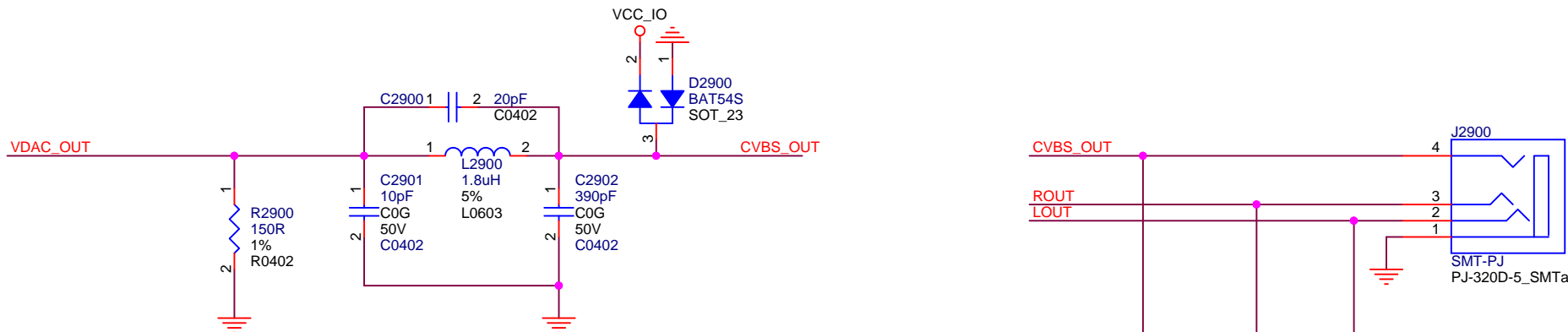
USB30\_RXP  
USB30\_RXN  
USB30\_TXP  
USB30\_TXN  
USB30\_DM  
USB30\_DP  
USB30\_HOST\_DRV

Note:  
USB3.0信号的ESD不能随便换掉  
如需换那么必须选择相同的规格。  
 $C_j \leq 0.4pF$





 瑞芯微电子		Fuzhou Rockchip Electronics	
Project:	RK3328_BOX_Demo1		
File:	S/PDIF Port		
Date:	Tuesday, July 18, 2017	Rev:	V1.1
Designed by:	Zhangdz	Sheet:	20 of 24



#### External Undervoltage Detection

External undervoltage detection can be used to mute/shut down the SGM89000 before an input device can generate a pop.

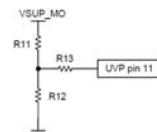
The threshold seen at the UVP pin is 1.15V. A hysteresis is introduced with a resistive divider, where thresholds for startup and shutdown are determined respectively as follows:

Startup Threshold:  $V_{UP} = 1.15V \times (R11 + R12) / R12$

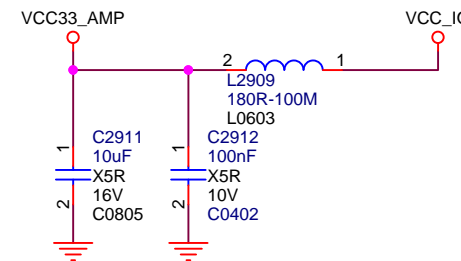
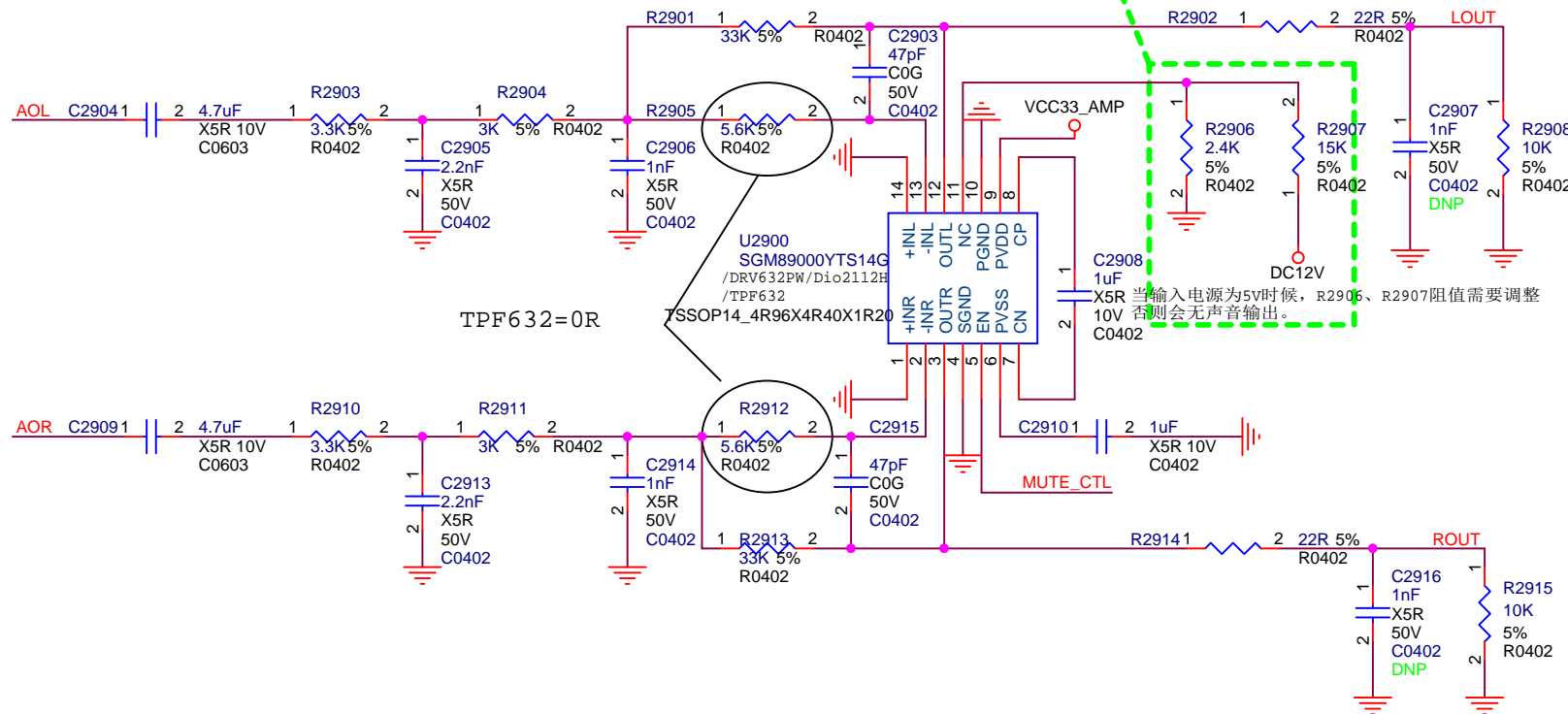
Shutdown Threshold:  $V_{UP} = 1.15V \times (R11 + R12) / R12 - 4.6\mu A \times (R13 + R11) / R12$

Hysteresis:  $4.6\mu A \times (R13 + R11) / R12$


The R13 is optional. If the R13 is not used, the UVP pin connects to the divider center tap directly.

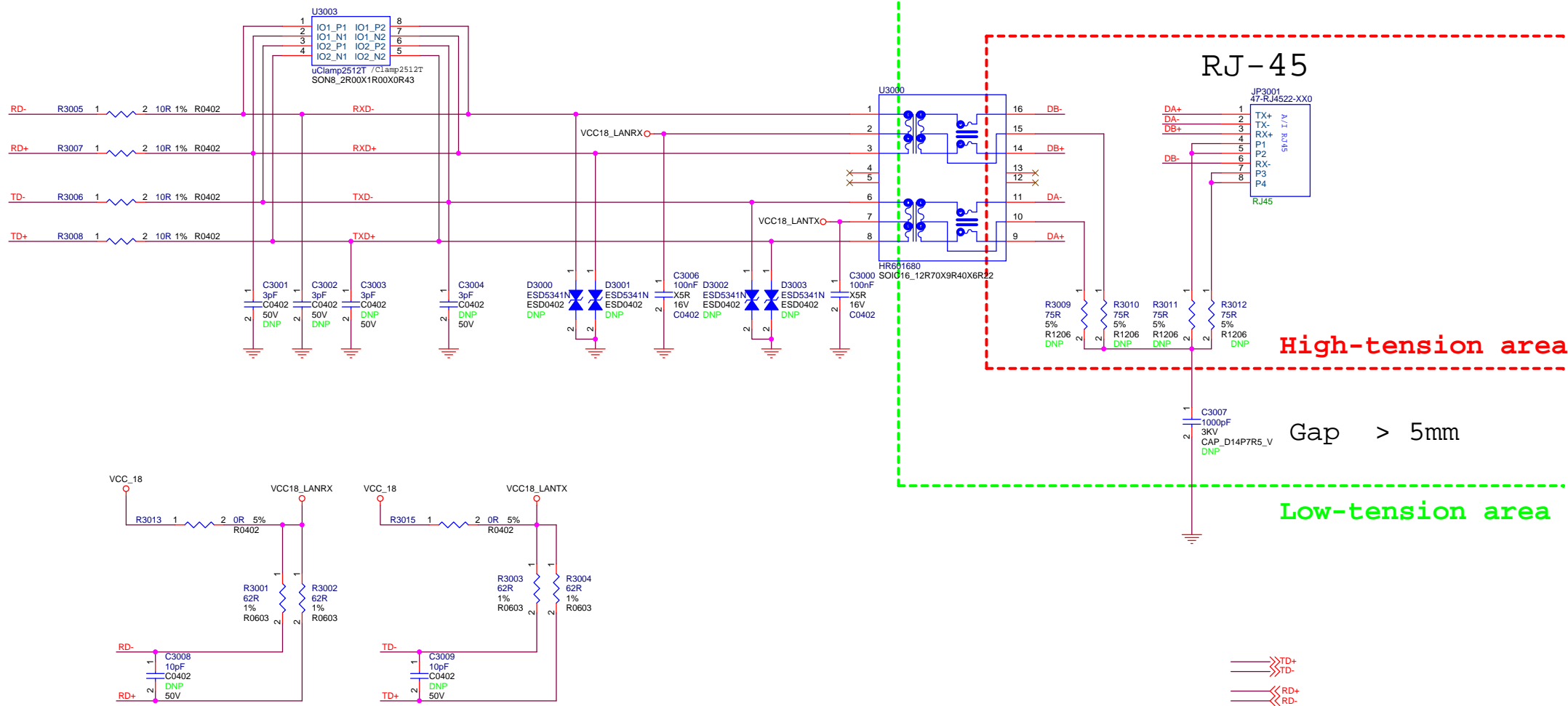


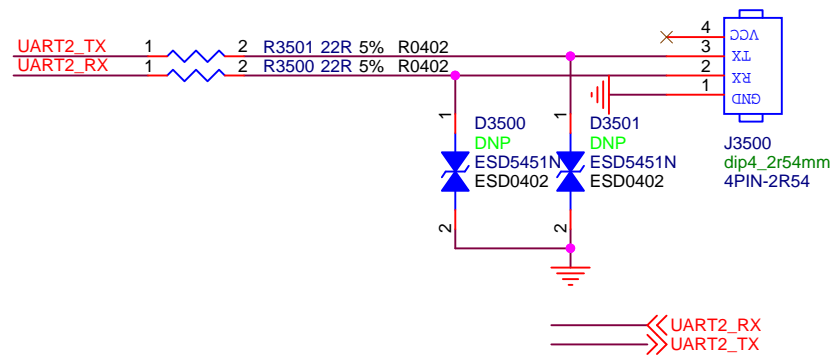
AV OUT




2-Vrms Audio Line Driver

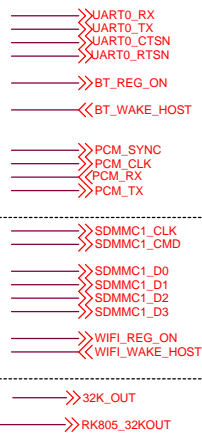
 瑞芯微电子		Fuzhou Rockchip Electronics	
Project:	RK3328_BOX_Demo1		
File:	AV OUT Port		
Date:	Tuesday, July 18, 2017	Rev:	V1.1
Designed by:	Zhangdz	Sheet:	21 of 24



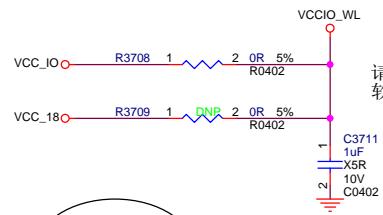
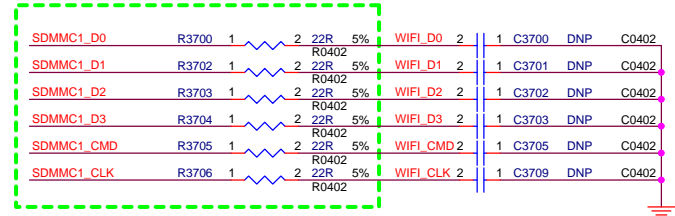


Debug UART2

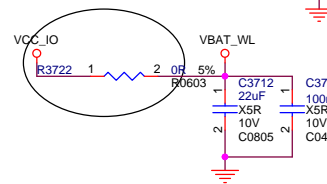
 瑞芯微电子		Fuzhou Rockchip Electronics	
Project:	RK3328_BOX_Demo1		
File:	Debug UART2/JTAG		
Date:	Tuesday, July 18, 2017	Rev:	V1.1
Designed by:	<designer>	Sheet:	23 of 24



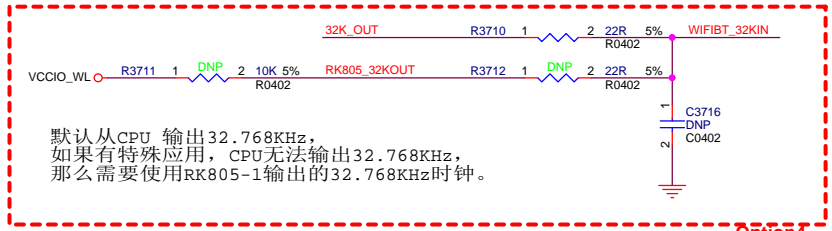
请靠近CPU放置。



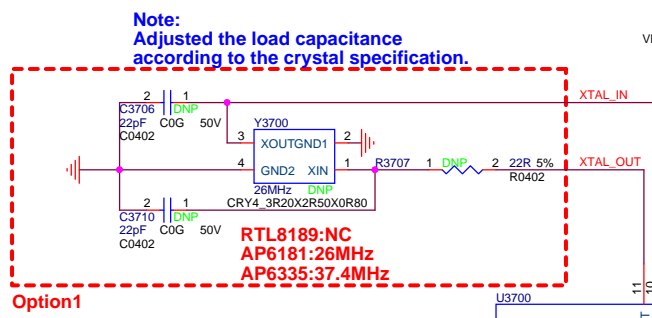
请根据实际贴的模组选择IO电压值  
软件也需对应修改配置。



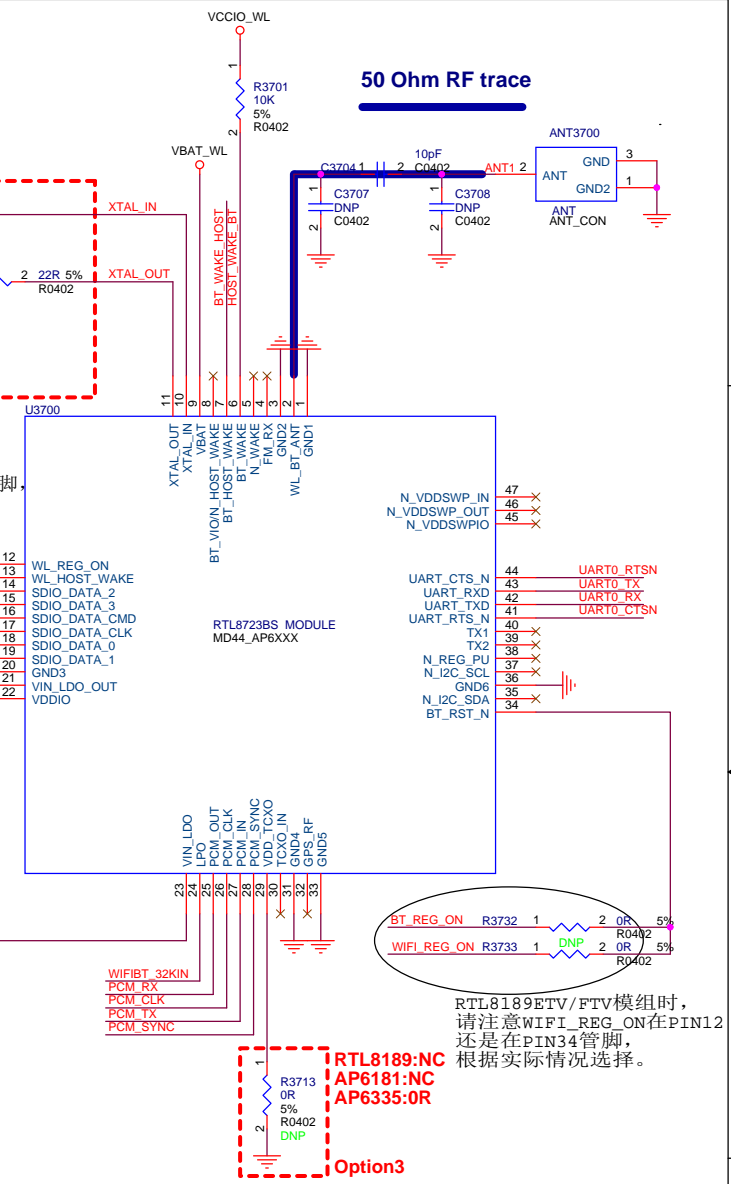
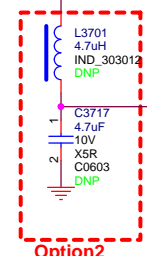
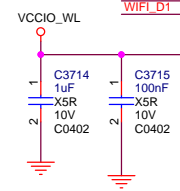
峰值最大有600mA  
靠近WIFI模组管脚放置



默认从CPU 输出32.768KHz，  
如果有特殊应用，CPU无法输出32.768KHz，  
那么需要使用RK805-1输出的32.768KHz时钟。



RTL8189ETV/FTV模组时，  
请注意WIFI\_REG\_ON在PIN12还是在PIN34管脚，  
根据实际情况选择。



RTL8189ETV/FTV模组时，  
请注意WIFI\_REG\_ON在PIN12  
还是在PIN34管脚，  
根据实际情况选择。

# 1X1 WIFI

## AP6181/AP6212/AP6330/AP6335/RTL8189FTV/AP6255

## RTL8723BS/XZ3538/XZ3660

OPTION	WIFI				BT	Crystals	VDDIO
	a	b/g/n	ac	5GHz			
AP6181	No	Yes	No	No	No	26MHz	1.71-3.6V
AP6212	No	Yes	No	No	Yes	26MHz	1.71-3.6V
XZ3538							
AP6330	Yes	Yes	No	Yes	Yes	26MHz	1.2-2.9V
XZ3660							
AP6335	Yes	Yes	Yes	Yes	Yes	37.4MHz	1.71-3.63V
AP6255							
RTL8189FTV MODULE	No	Yes	No	No	No	40MHz On the module	3.3V
RTL8723BS	No	Yes	No	No	Yes		1.71-3.63V

OPTION	1	2	3	4	5
AP6181	Yes	Yes	No	Yes	
AP6212	Yes	Yes	No	Yes	
AP6330	Yes	Yes	No	Yes	
AP6335	Yes	Yes	Yes	Yes	
AP6255					
RTL8189FTV MODULE	No	No	No	No	
RTL8723BS	No	No	No	Yes	