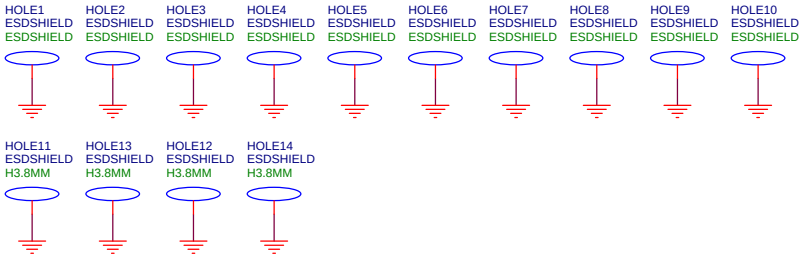
RK3328

Content Indexing



Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

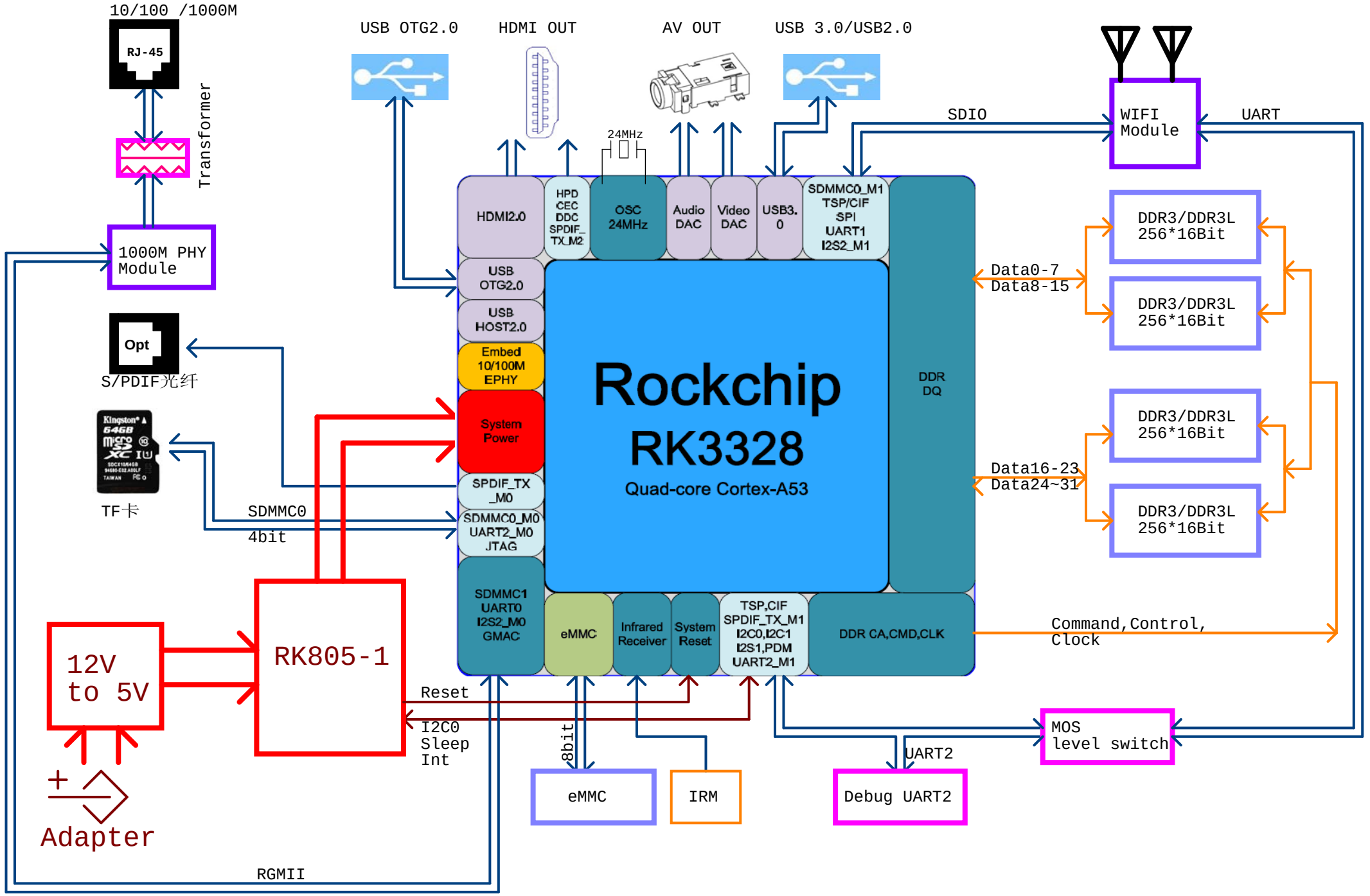
{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Note：
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

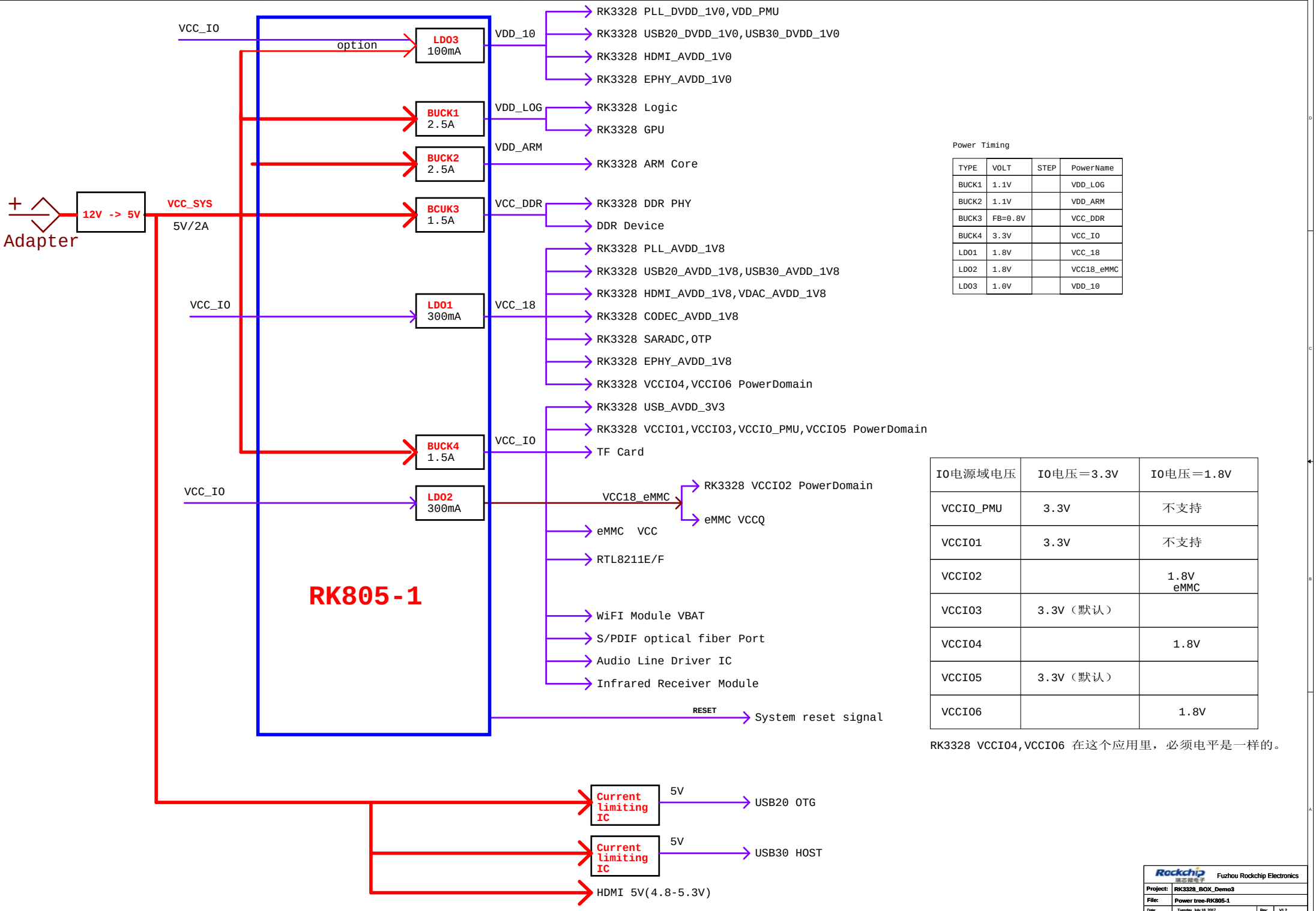
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Demo3		
File:	Index		
Date:	Tuesday, July 18, 2017	Rev:	V1.2
Designed by:	Zhangdz	Sheet:	1 of 24

Version	Date	Author	Change Note	Approved
V1.0	20170309	ZDZ	First edictor	
V1.1	20170421	ZDZ	1：C3820封装由0201更新为0402 2：为了配合参考PCB模具，SDMMC0EXT更改接SD/TF卡，SDMMC0接WIFI （这点更改前提是客户不要求支持SD Boot功能） 由于IO电平关系，WIFI_REG_ON原先F3管脚GPIO3_B0，更新为W20管脚GPIO1_C2	
V1.2	20170718	ZDZ	1：修改记录请见：RK3328_BOX_DEMO3_RK805-1_DDR3P416DD4_V12_SCH_Modify_Notes	

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Demo3		
File:	Change List		
Date:	Tuesday, July 18, 2017	Rev:	V1.2
Designed by:	Zhangdz	Sheet:	2 of 24



Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Demo3		
File:	Block Diagram		
Date:	Tuesday, July 18, 2017	Rev:	V1.2
Designed by:	Zhangdz	Sheet:	3 of 24



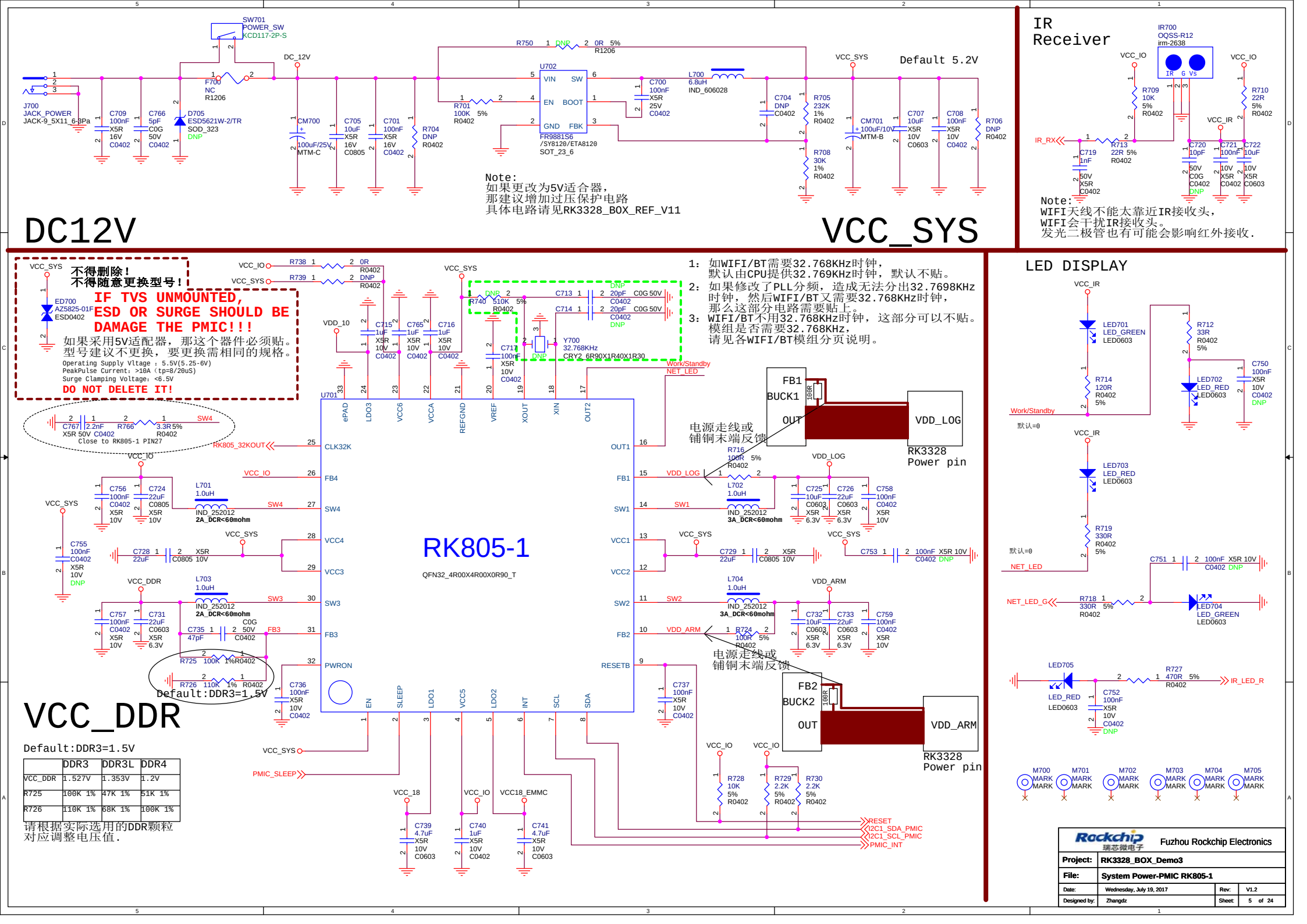
Power Timing

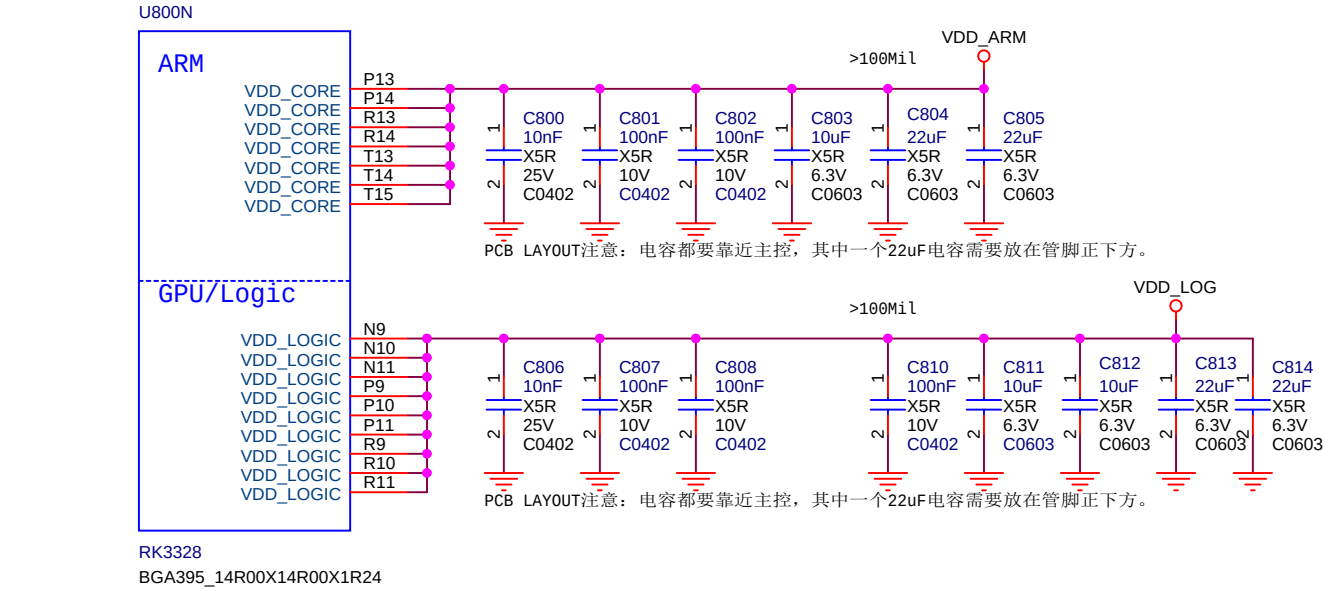
TYPE	VOLT	STEP	PowerName
BUCK1	1.1V		VDD_LOG
BUCK2	1.1V		VDD_ARM
BUCK3	FB=0.8V		VCC_DDR
BUCK4	3.3V		VCC_IO
LDO1	1.8V		VCC_18
LDO2	1.8V		VCC18_eMMC
LDO3	1.0V		VDD_10

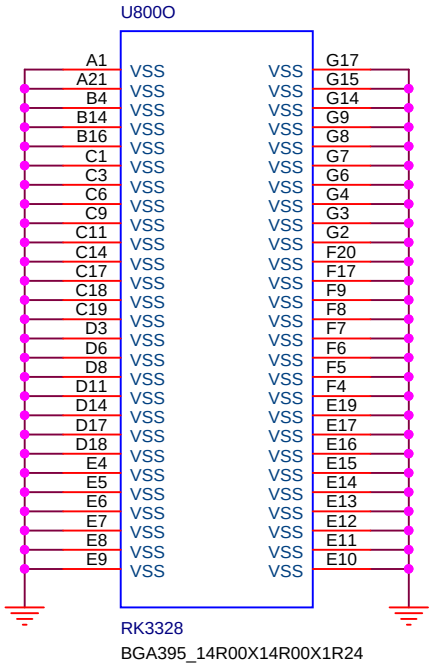
IO电源域电压	IO电压＝3.3V	IO电压＝1.8V
VCCIO_PMU	3.3V	不支持
VCCIO1	3.3V	不支持
VCCIO2		1.8V eMMC
VCCIO3	3.3V（默认）	
VCCIO4		1.8V
VCCIO5	3.3V（默认）	
VCCIO6		1.8V

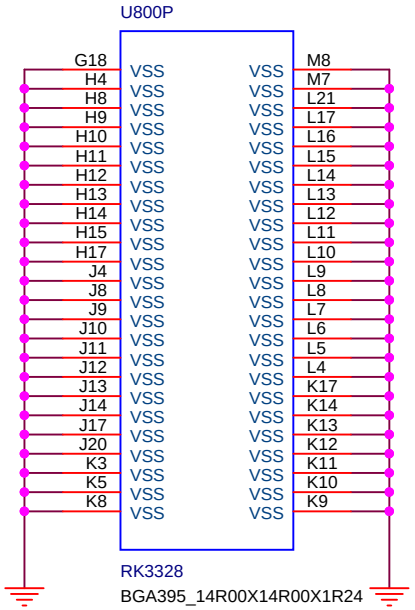
RK3328 VCCIO4,VCCIO6 在这个应用里，必须电平是一样的。

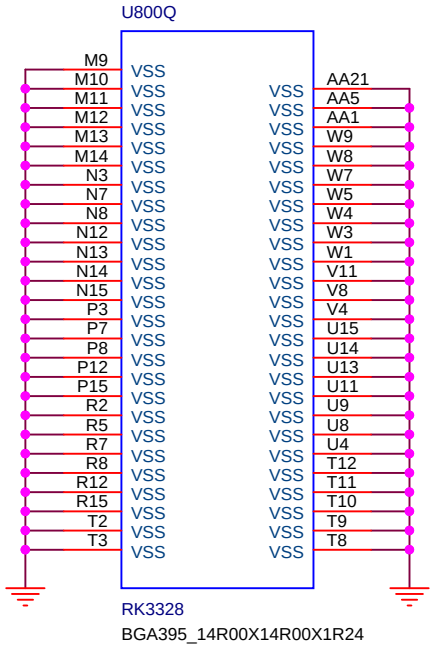
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics
Project:	RK3328_BOX_Demo3
File:	Power tree-RK805-1
Date:	Tuesday, July 18, 2017
Rev:	V1.2
Designed by:	Zhangzb
Sheet:	4 of 24


DC12V
VCC_SYS
Default 5.2V
Note:
如果更改为5V适合器，
那建议增加过压保护电路
具体电路请见RK3328_BOX_REF_V11
IR Receiver
Note:
WIFI天线不能太靠近IR接收头，
WIFI会干扰IR接收头。
发光二极管也有可能会影响红外接收.
不得删除！
不得随意更换型号！
IF TVS UNMOUNTED,
ESD OR SURGE SHOULD BE
DAMAGE THE PMIC!!!
如果采用5V适配器，那这个器件必须贴。
型号建议不更换，要更换需相同的规格。
Operating Supply Vltage : 5.5V(5.25-6V)
PeakPulse Current: >10A (tp=8/20uS)
Surge Clamping Voltage: <6.5V
DO NOT DELETE IT!
1：如WIFI/BT需要32.768KHz时钟，
默认由CPU提供32.769KHz时钟，默认不贴。
2：如果修改了PLL分频，造成无法分出32.7698KHz
时钟，然后WIFI/BT又需要32.768KHz时钟，
那么这部分电路需要贴上。
3：WIFI/BT不用32.768KHz时钟，这部分可以不贴。
模组是否需要32.768KHz，
请见各WIFI/BT模组分页说明。
RK805-1
QFN32_4R00X4R00X0R90_T
电源走线或
铺铜末端反馈
RK3328
Power pin
VDD_LOG
VDD_ARM
LED DISPLAY
VCC_DDR
Default:DDR3=1.5V
Default:DDR3=1.5V
DDR3 DDR3L DDR4
VCC_DDR 1.527V 1.353V 1.2V
R725 100K 1% 47K 1% 51K 1%
R726 110K 1% 68K 1% 100K 1%
请根据实际选用的DDR颗粒
对应调整电压值.
Rockchip 瑞芯微电子 Fuzhou Rockchip Electronics
Project: RK3328_BOX_Demo3
File: System Power-PMIC RK805-1
Date: Wednesday, July 19, 2017
Rev: V1.2
Designed by: Zhangdz
Sheet: 5 of 24

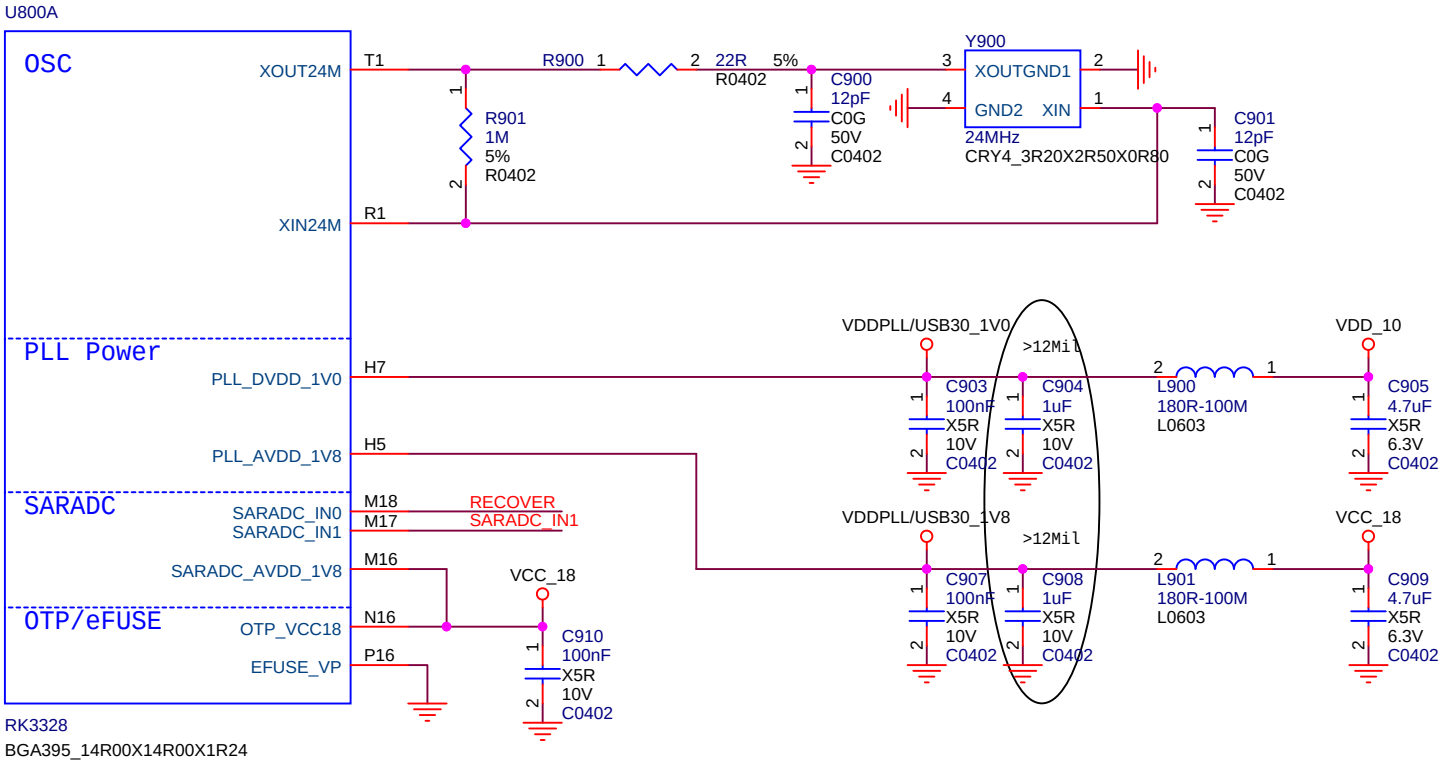


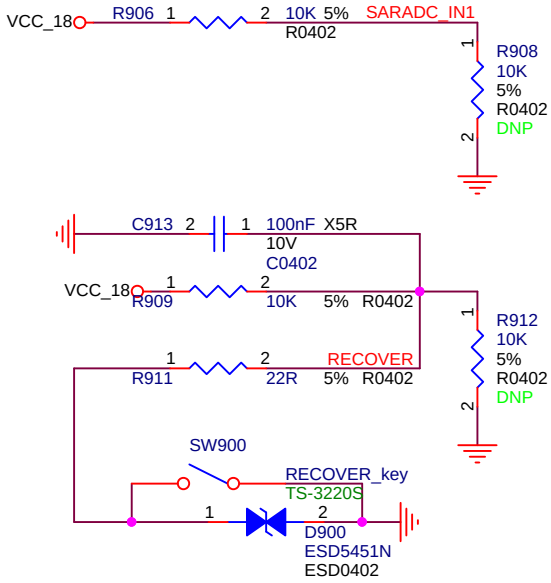






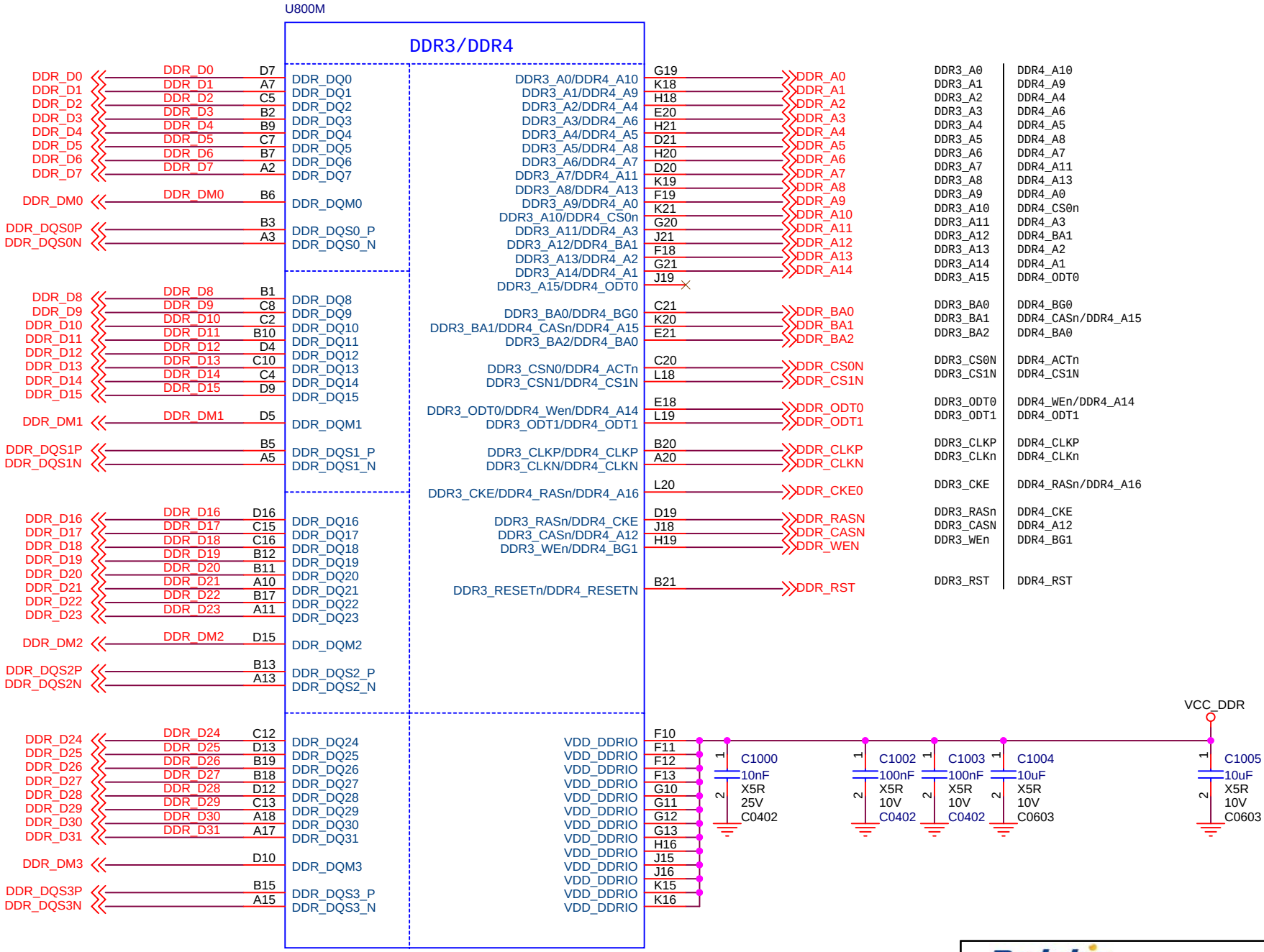
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Demo3		
File:	RK3328 Power		
Date:	Tuesday, July 18, 2017	Rev:	V1.2
Designed by:	Zhangdz	Sheet:	6 of 24

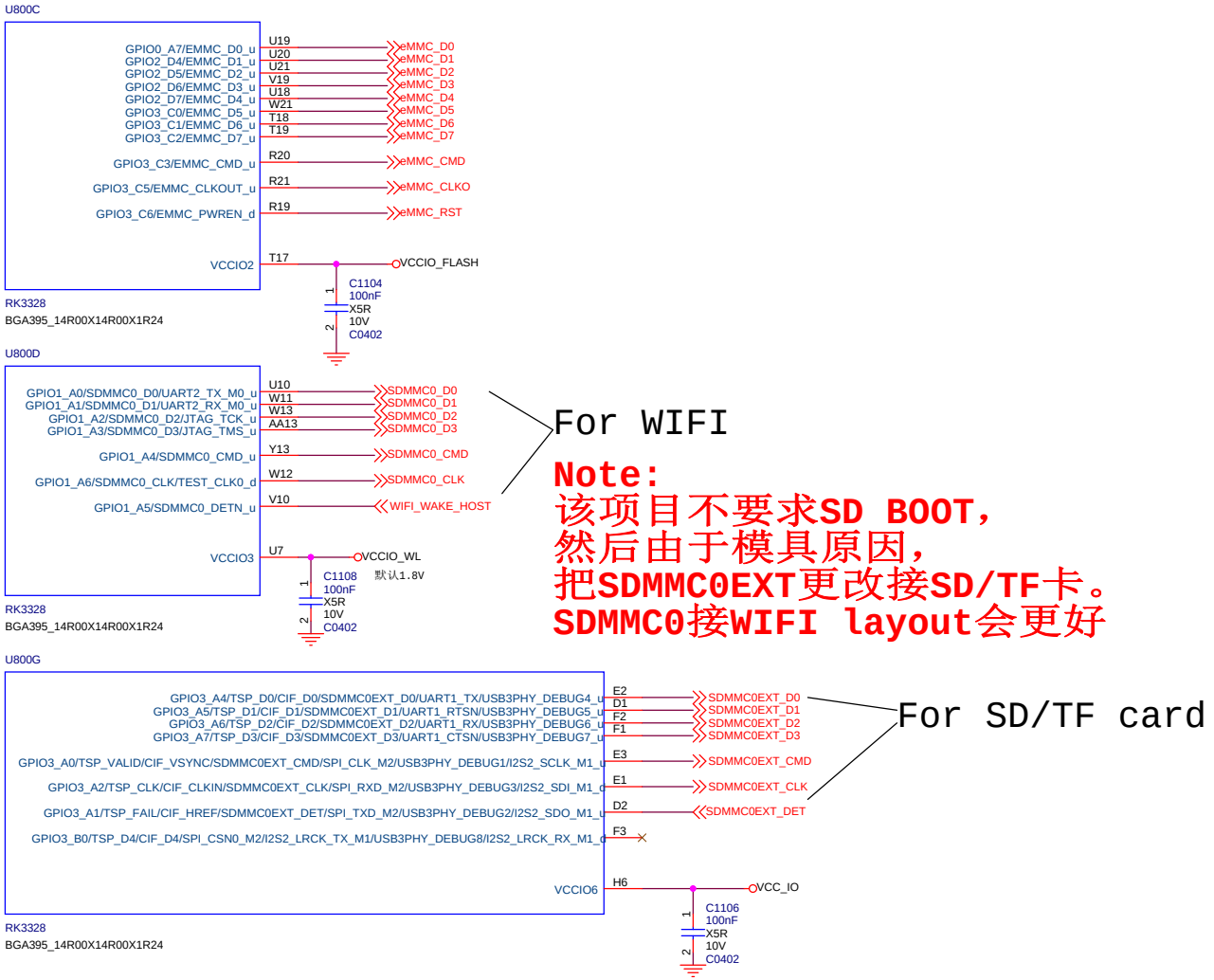




SARADC_IN0 BOM版本	SARADC_IN1 PCB版本	Up阻值	Down阻值	
Recover		DNP	10K	
BOM1		110K	10K	
BOM2		100K	20K	
BOM3		100K	33K	
BOM4		36K	18K	
BOM5		51K	36K	
BOM6		51K	51K	
BOM7		36K	51K	
BOM8		18K	36K	
BOM9		33K	100K	
BOM10		20K	100K	
BOM11		10K	110K	
BOM12		10K	DNP	

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Demo3		
File:	RK3328 OSC/PLL/OTP/SARADC		
Date:	Tuesday, July 18, 2017	Rev:	V1.2
Designed by:	Zhangdz	Sheet:	7 of 24


U800M
DDR3/DDR4
DDR_D0
DDR_D1
DDR_D2
DDR_D3
DDR_D4
DDR_D5
DDR_D6
DDR_D7
DDR_DM0
DDR_DQS0P
DDR_DQS0N
DDR_D8
DDR_D9
DDR_D10
DDR_D11
DDR_D12
DDR_D13
DDR_D14
DDR_D15
DDR_DM1
DDR_DQS1P
DDR_DQS1N
DDR_D16
DDR_D17
DDR_D18
DDR_D19
DDR_D20
DDR_D21
DDR_D22
DDR_D23
DDR_DM2
DDR_DQS2P
DDR_DQS2N
DDR_D24
DDR_D25
DDR_D26
DDR_D27
DDR_D28
DDR_D29
DDR_D30
DDR_D31
DDR_DM3
DDR_DQS3P
DDR_DQS3N
DDR_DQ0
DDR_DQ1
DDR_DQ2
DDR_DQ3
DDR_DQ4
DDR_DQ5
DDR_DQ6
DDR_DQ7
DDR_DQM0
DDR_DQS0_P
DDR_DQS0_N
DDR_DQ8
DDR_DQ9
DDR_DQ10
DDR_DQ11
DDR_DQ12
DDR_DQ13
DDR_DQ14
DDR_DQ15
DDR_DQM1
DDR_DQS1_P
DDR_DQS1_N
DDR_DQ16
DDR_DQ17
DDR_DQ18
DDR_DQ19
DDR_DQ20
DDR_DQ21
DDR_DQ22
DDR_DQ23
DDR_DQM2
DDR_DQS2_P
DDR_DQS2_N
DDR_DQ24
DDR_DQ25
DDR_DQ26
DDR_DQ27
DDR_DQ28
DDR_DQ29
DDR_DQ30
DDR_DQ31
DDR_DQM3
DDR_DQS3_P
DDR_DQS3_N
DDR3_A0/DDR4_A10
DDR3_A1/DDR4_A9
DDR3_A2/DDR4_A4
DDR3_A3/DDR4_A6
DDR3_A4/DDR4_A5
DDR3_A5/DDR4_A8
DDR3_A6/DDR4_A7
DDR3_A7/DDR4_A11
DDR3_A8/DDR4_A13
DDR3_A9/DDR4_A0
DDR3_A10/DDR4_CS0n
DDR3_A11/DDR4_A3
DDR3_A12/DDR4_BA1
DDR3_A13/DDR4_A2
DDR3_A14/DDR4_A1
DDR3_A15/DDR4_ODT0
DDR3_BA0/DDR4_BG0
DDR3_BA1/DDR4_CASn/DDR4_A15
DDR3_BA2/DDR4_BA0
DDR3_CSN0/DDR4_ACTn
DDR3_CSN1/DDR4_CS1N
DDR3_ODT0/DDR4_Wen/DDR4_A14
DDR3_ODT1/DDR4_ODT1
DDR3_CLKP/DDR4_CLKP
DDR3_CLKN/DDR4_CLKN
DDR3_CKE/DDR4_RASn/DDR4_A16
DDR3_RASn/DDR4_CKE
DDR3_CASn/DDR4_A12
DDR3_WEn/DDR4_BG1
DDR3_RESETn/DDR4_RESETN
DDR_A0
DDR_A1
DDR_A2
DDR_A3
DDR_A4
DDR_A5
DDR_A6
DDR_A7
DDR_A8
DDR_A9
DDR_A10
DDR_A11
DDR_A12
DDR_A13
DDR_A14
DDR_BA0
DDR_BA1
DDR_BA2
DDR_CS0N
DDR_CS1N
DDR_ODT0
DDR_ODT1
DDR_CLKP
DDR_CLKN
DDR_CKE0
DDR_RASN
DDR_CASN
DDR_WEN
DDR_RST
DDR3_A0 DDR4_A10
DDR3_A1 DDR4_A9
DDR3_A2 DDR4_A4
DDR3_A3 DDR4_A6
DDR3_A4 DDR4_A5
DDR3_A5 DDR4_A8
DDR3_A6 DDR4_A7
DDR3_A7 DDR4_A11
DDR3_A8 DDR4_A13
DDR3_A9 DDR4_A0
DDR3_A10 DDR4_CS0n
DDR3_A11 DDR4_A3
DDR3_A12 DDR4_BA1
DDR3_A13 DDR4_A2
DDR3_A14 DDR4_A1
DDR3_A15 DDR4_ODT0
DDR3_BA0 DDR4_BG0
DDR3_BA1 DDR4_CASn/DDR4_A15
DDR3_BA2 DDR4_BA0
DDR3_CS0N DDR4_ACTn
DDR3_CS1N DDR4_CS1N
DDR3_ODT0 DDR4_WEn/DDR4_A14
DDR3_ODT1 DDR4_ODT1
DDR3_CLKP DDR4_CLKP
DDR3_CLKn DDR4_CLKn
DDR3_CKE DDR4_RASn/DDR4_A16
DDR3_RASn DDR4_CKE
DDR3_CASN DDR4_A12
DDR3_WEn DDR4_BG1
DDR3_RST DDR4_RST
VDD_DDRIO
C1000 10nF X5R 25V C0402
C1002 100nF X5R 10V C0402
C1003 100nF X5R 10V C0402
C1004 10uF X5R 10V C0603
C1005 10uF X5R 10V C0603
VCC_DDR
RK3328
BGA395_14R00X14R00X1R24
Rockchip 瑞芯微电子
Fuzhou Rockchip Electronics
Project: RK3328_BOX_Demo3
File: RK3328 DDR Controler
Date: Tuesday, July 18, 2017
Rev: V1.2
Designed by: Zhangdz
Sheet: 8 of 24



For WIFI

Note:
该项目不要求SD BOOT，
然后由于模具原因，
把SDMMC0EXT更改接SD/TF卡。
SDMMC0接WIFI layout会更好

For SD/TF card

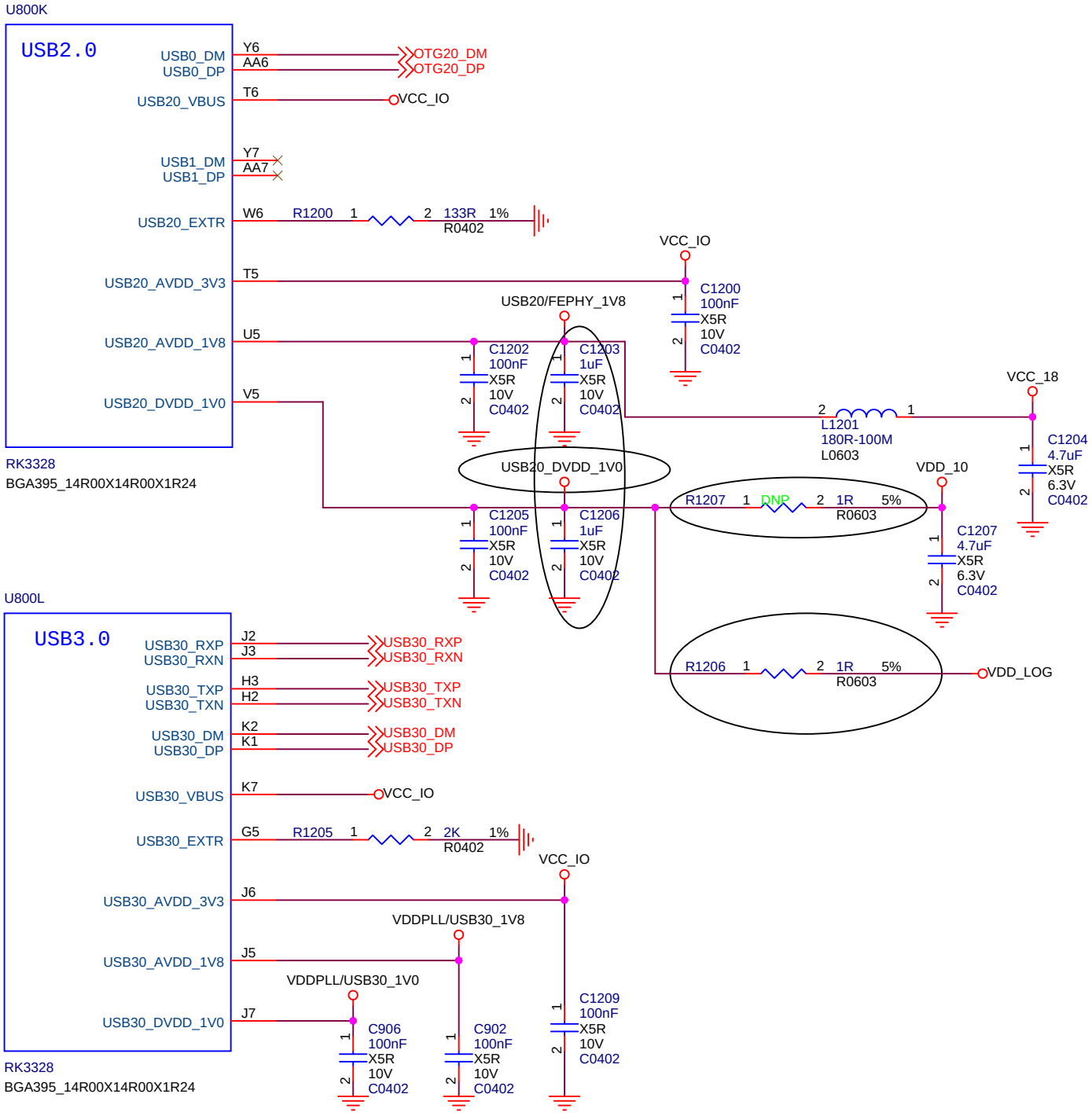
Note:
SDMMC0支持SD Boot，Max 150MHz
SDMMC0EXT不支持SD Boot，Max 100MHz

```
SDMMC0_D0          --------------------  SD_D0
SDMMC0_D1          --------------------  SD_D1
SDMMC0_D2/JTAG_TCK --------------------  SD_D2
SDMMC0_D3/JTAG_TMS --------------------  SD_D3
SDMMC0_CMD         --------------------  SD_CMD
SDMMC0_CLK         --------------------  SD_CLK
SDMMC0_DET         --------------------  SD_DET
VCCIO3             --------------------  VCC_IO

SDMMC0EXT_D0       --------------------  WIFI_D0_EXT
SDMMC0EXT_D1       --------------------  WIFI_D1_EXT
SDMMC0EXT_D2       --------------------  WIFI_D2_EXT
SDMMC0EXT_D3       --------------------  WIFI_D3_EXT
SDMMC0EXT_CMD      --------------------  WIFI_CMD_EXT
SDMMC0EXT_CLK      --------------------  WIFI_CLK_EXT
GPIO3_A1           --------------------  WIFI_WAKE_HOST_EXT
VCCIO6             --------------------  VCCIO_WL_EXT
```

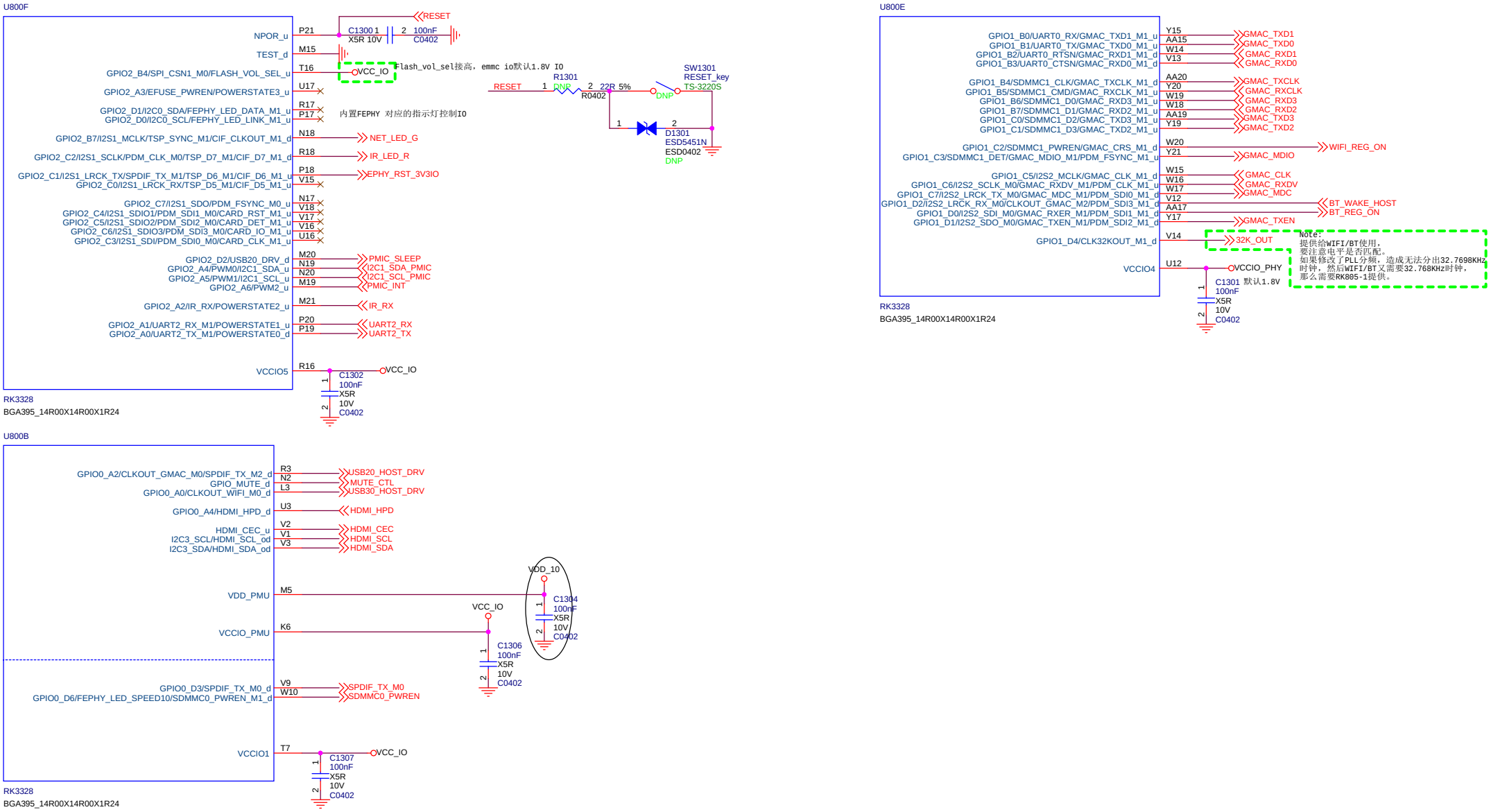
```
SDMMC0_D0          --------------------  WIFI_D0_EXT
SDMMC0_D1          --------------------  WIFI_D1_EXT
SDMMC0_D2/JTAG_TCK --------------------  WIFI_D2_EXT
SDMMC0_D3/JTAG_TMS --------------------  WIFI_D3_EXT
SDMMC0_CMD         --------------------  WIFI_CMD_EXT
SDMMC0_CLK         --------------------  WIFI_CLK_EXT
SDMMC0_DET         --------------------  WIFI_WAKE_HOST_EXT
VCCIO3             --------------------  VCCIO_WL_EXT

SDMMC0EXT_D0       --------------------  SD_D0
SDMMC0EXT_D1       --------------------  SD_D1
SDMMC0EXT_D2       --------------------  SD_D2
SDMMC0EXT_D3       --------------------  SD_D3
SDMMC0EXT_CMD      --------------------  SD_CMD
SDMMC0EXT_CLK      --------------------  SD_CLK
SDMMC0EXT_DET      --------------------  SD_DET
VCCIO6             --------------------  VCC_IO
```

如果WIFI需要高性能，前提是不需要支持SD Boot功能
WIFI SDIO接到SDMMC0口上。
SDMMC0EXT接SD卡

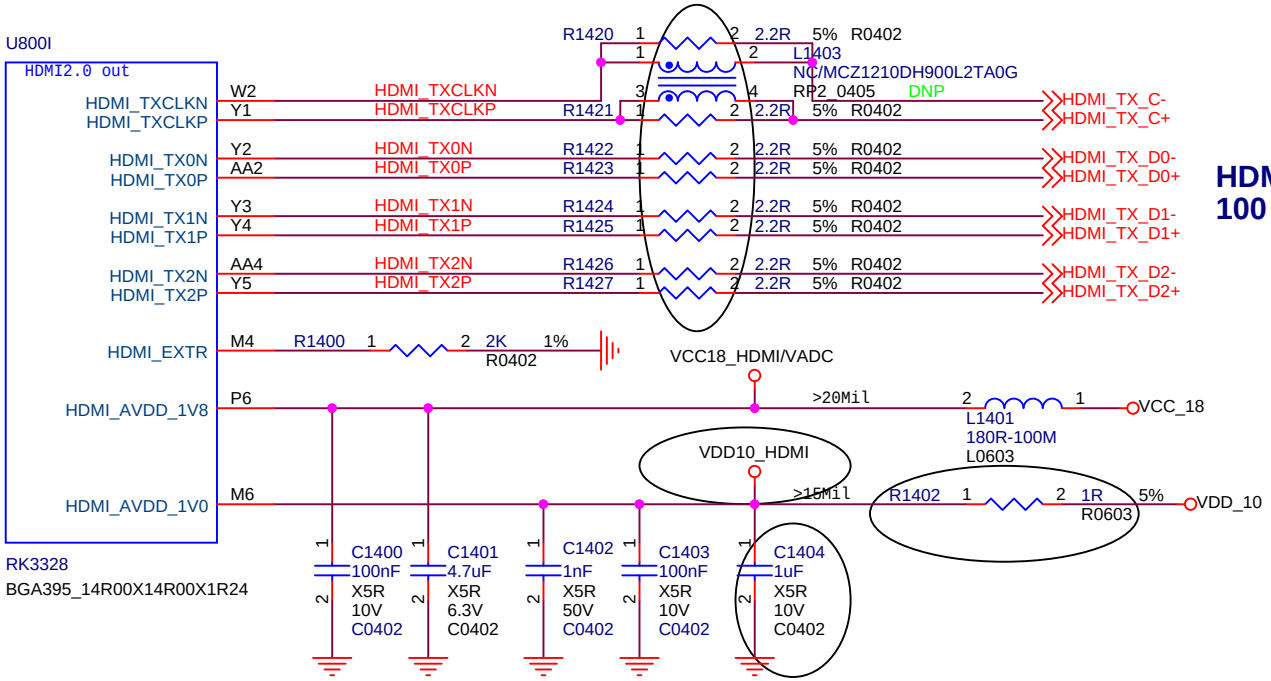
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Demo3		
File:	RK3328 eMMC Controler/TF		
Date:	Wednesday, August 16, 2017	Rev:	V1.2
Designed by:	Zhangdz	Sheet:	9 of 24



Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Demo3		
File:	RK3328 USB2 PHY/USB3 PHY		
Date:	Tuesday, July 18, 2017	Rev:	V1.2
Designed by:	Zhangdz	Sheet:	10 of 24

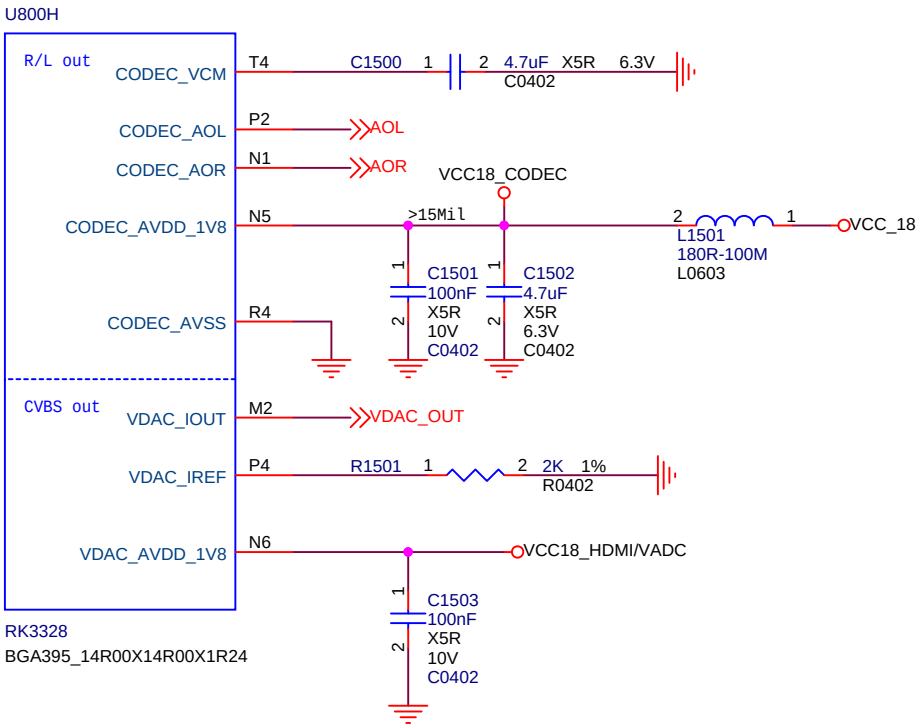


Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Demo3		
File:	RK3328 SDIO/UART/I2C/I2S/IR		
Date:	Tuesday, July 18, 2017	Rev:	V1.2
Designed by:	Zhangdz	Sheet:	11 of 24

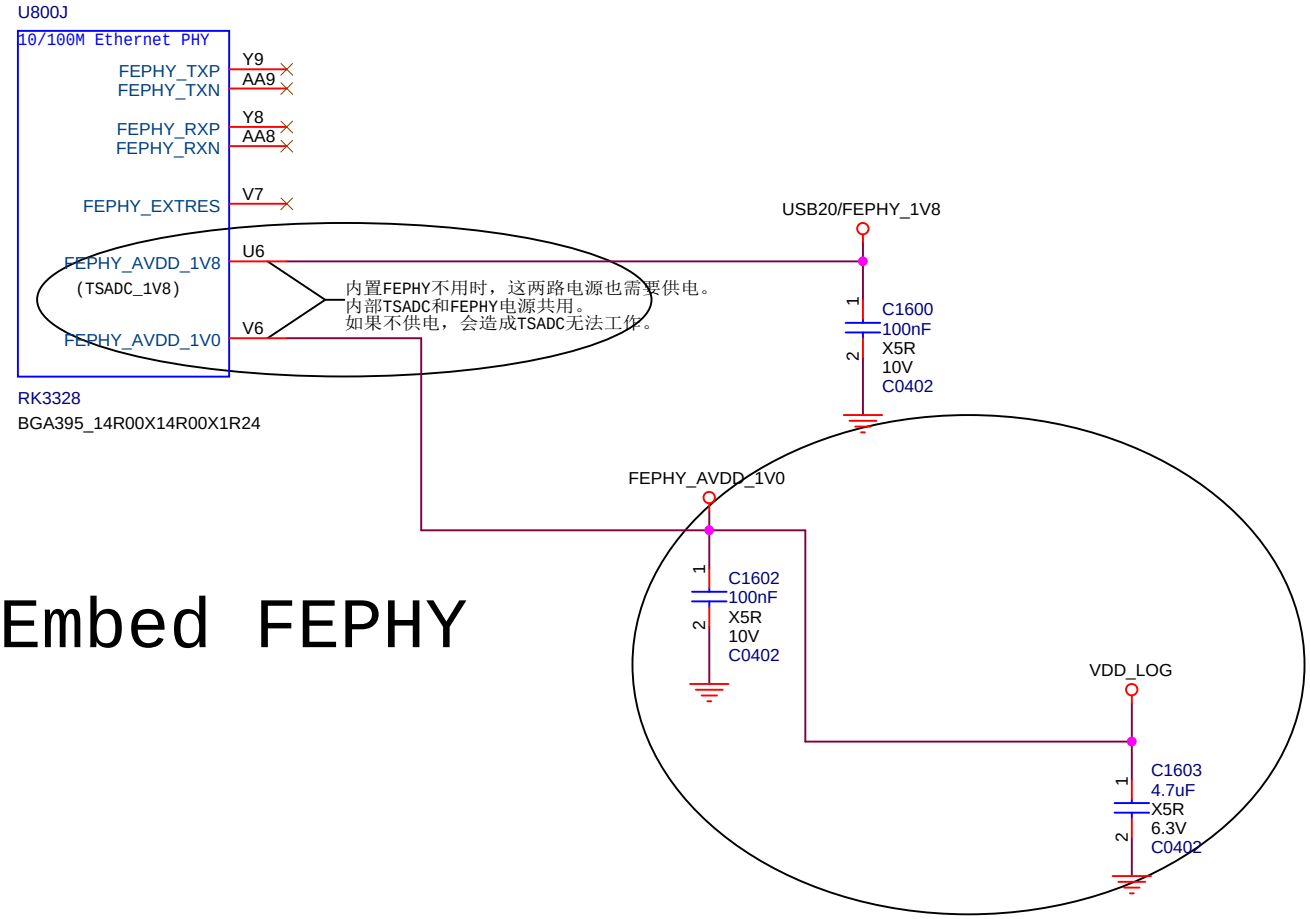


HDMI TMDS trace
100 Ohm +-10%

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Demo3		
File:	RK3328 HDMI PHY		
Date:	Tuesday, July 18, 2017	Rev:	V1.2
Designed by:	Zhangdz	Sheet:	12 of 24



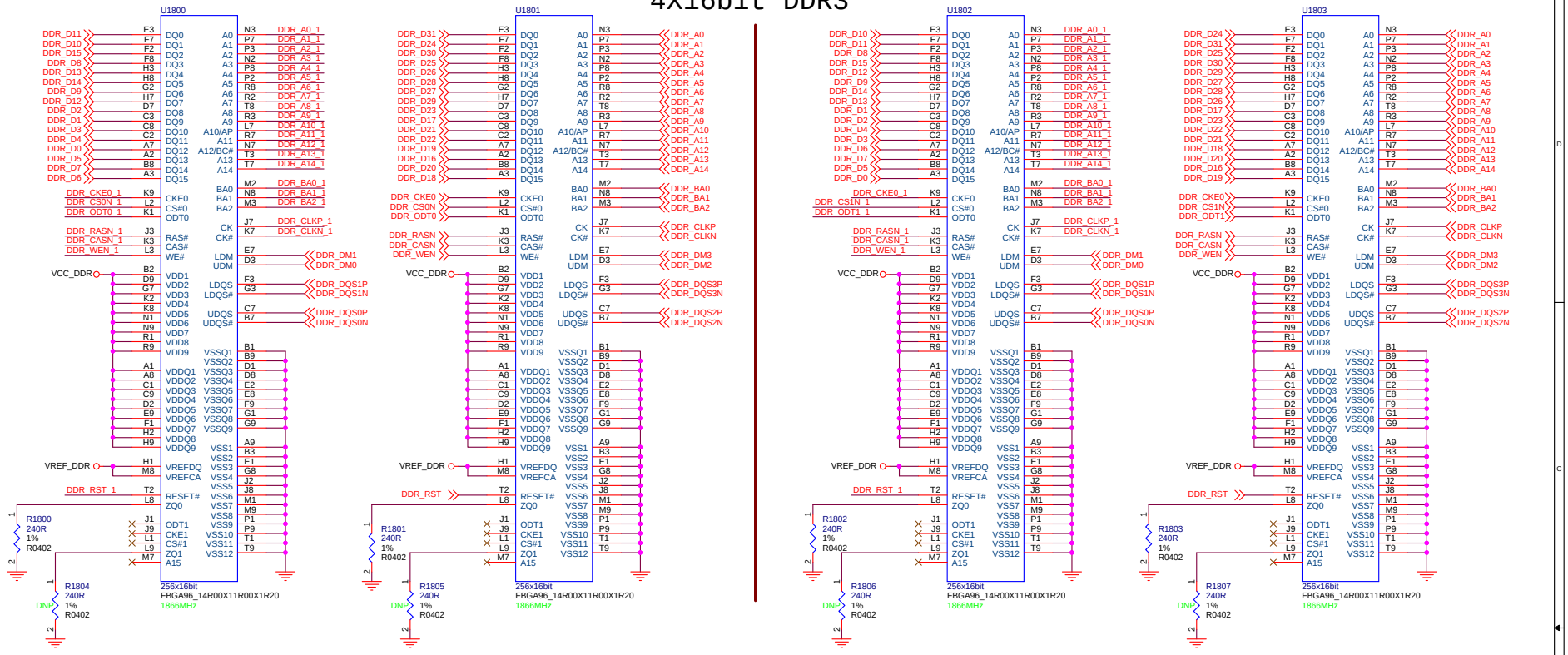
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	**RK3328_BOX_Demo3**		
File:	**RK3328 AV Interface**		
Date:	Tuesday, July 18, 2017	Rev:	V1.2
Designed by:	Zhangdz	Sheet:	13 of 24

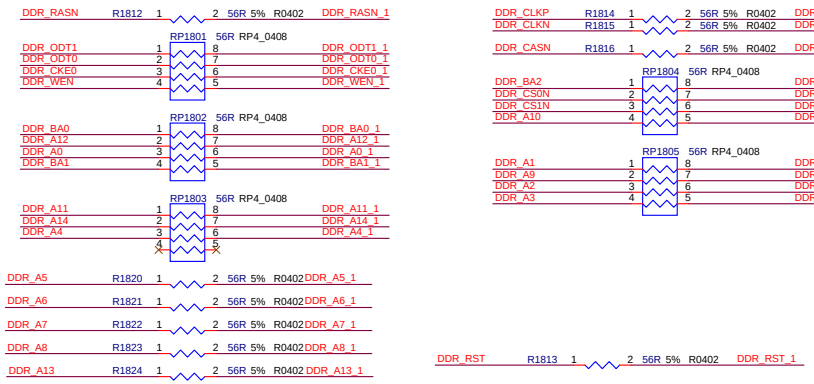


Embed FEPHY

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Demo3		
File:	RK3328 FEPHY		
Date:	Tuesday, July 18, 2017	Rev:	V1.2
Designed by:	Zhangdz	Sheet:	14 of 24

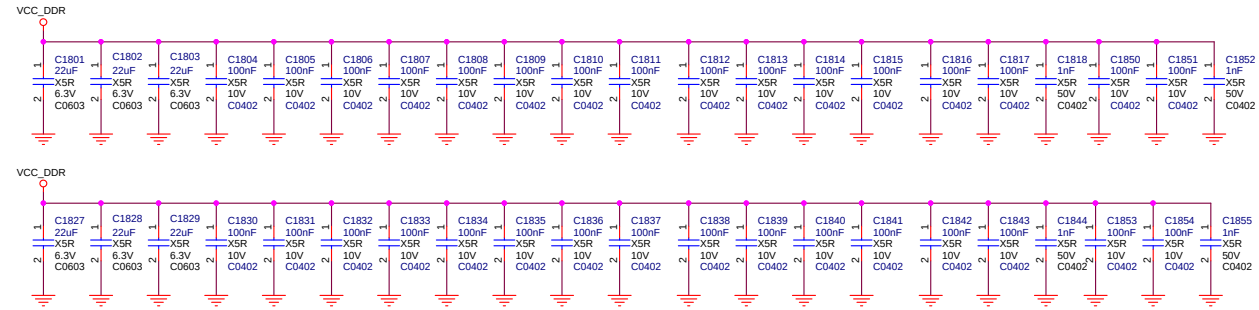
4X16bit DDR3

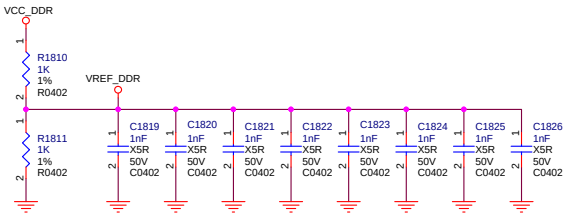




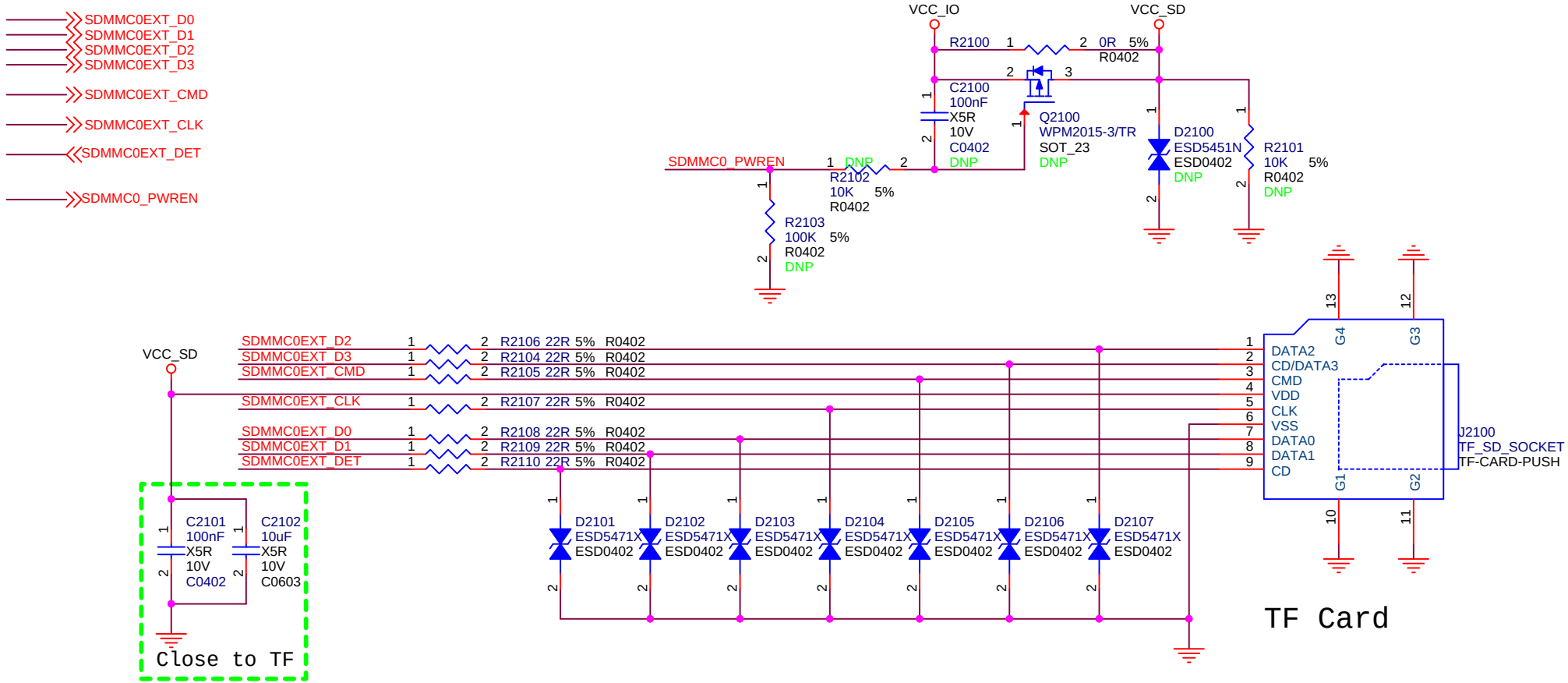
Note:
颗粒速率>=1600Mb/s

DDR3 FILTER

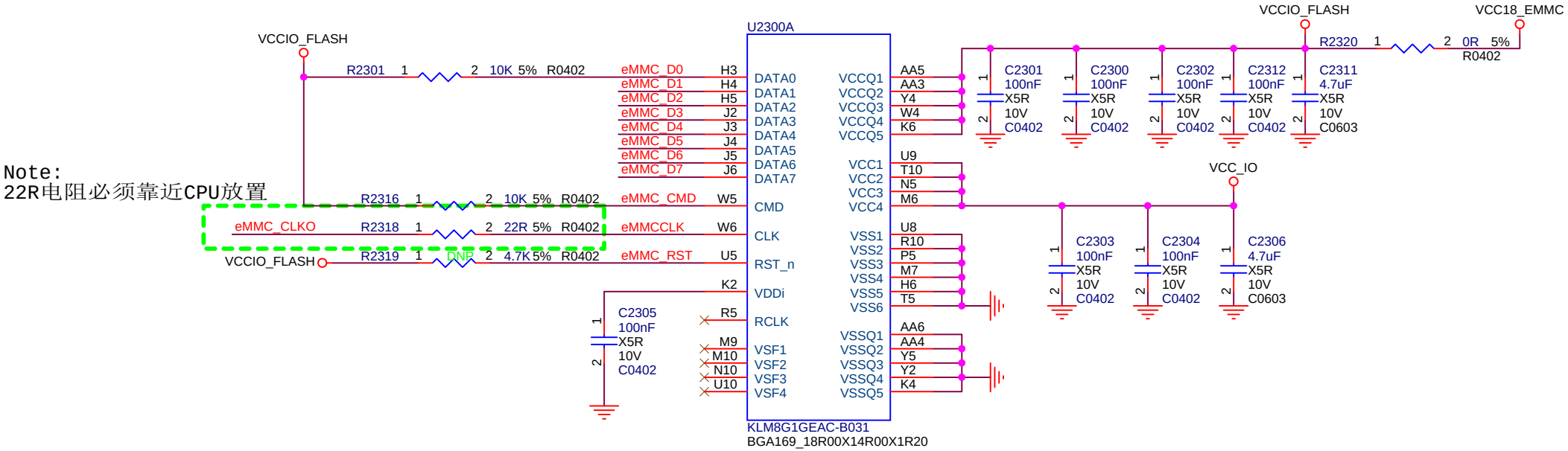


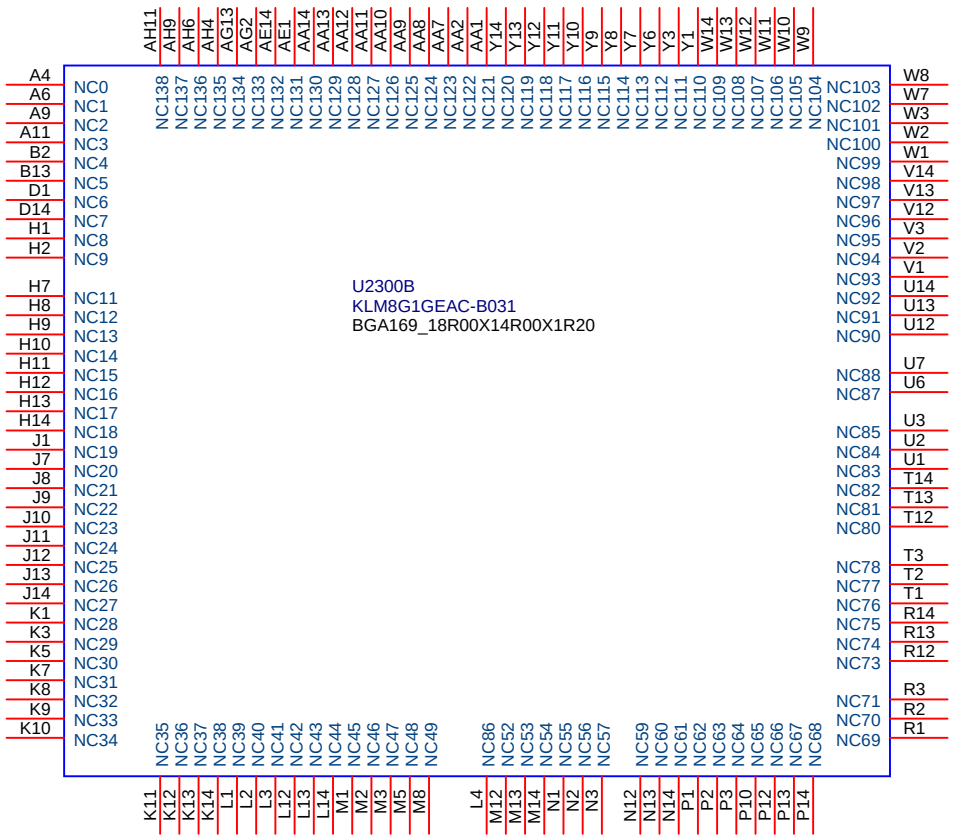


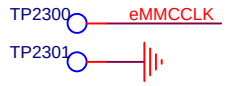
Fuzhou Rockchip Electronics	
Project:	RK3328_BOX_Demo3
File:	RAM DDR3 4x16bit
Date:	Tuesday, July 18, 2017
Rev:	V1.2
Designed by:	Zhangdz
Sheet:	15 of 24



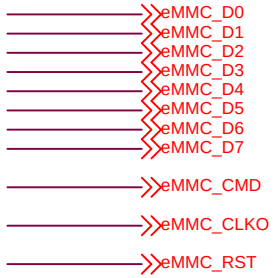
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Demo3		
File:	TF/SD Card		
Date:	Tuesday, July 18, 2017	Rev:	V1.2
Designed by:	Zhangdz	Sheet:	16 of 24



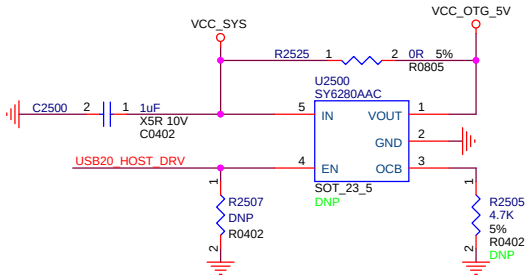


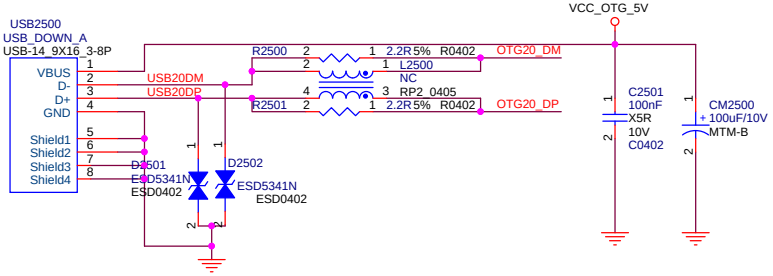


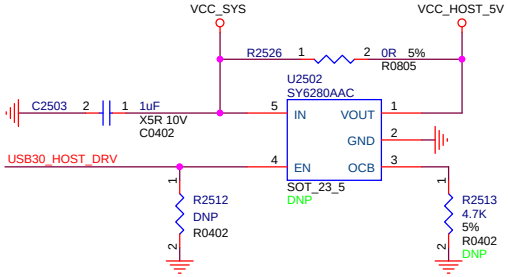
Note:
eMMC Update.

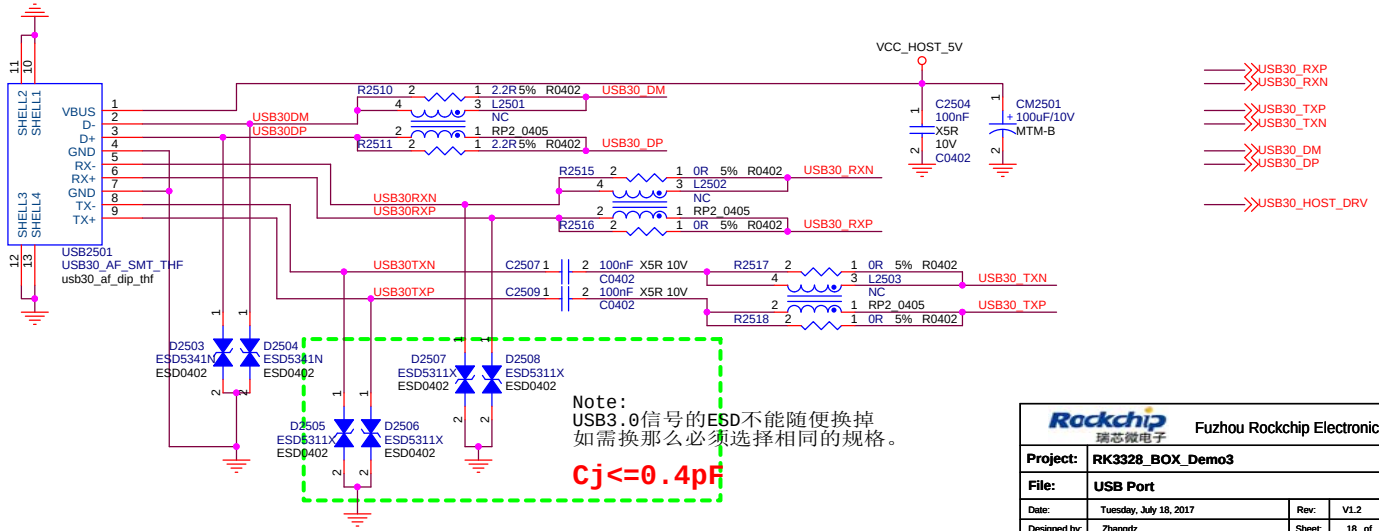


Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics
Project:	RK3328_BOX_Demo3
File:	Flash-eMMC
Date:	Tuesday, July 18, 2017
Rev:	V1.2
Designed by:	Zhangdz
Sheet:	17 of 24

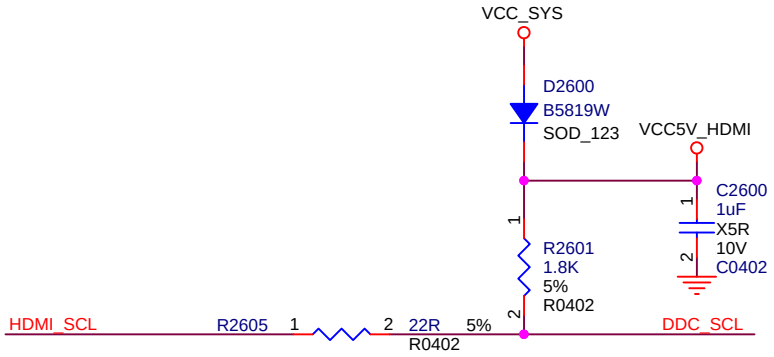


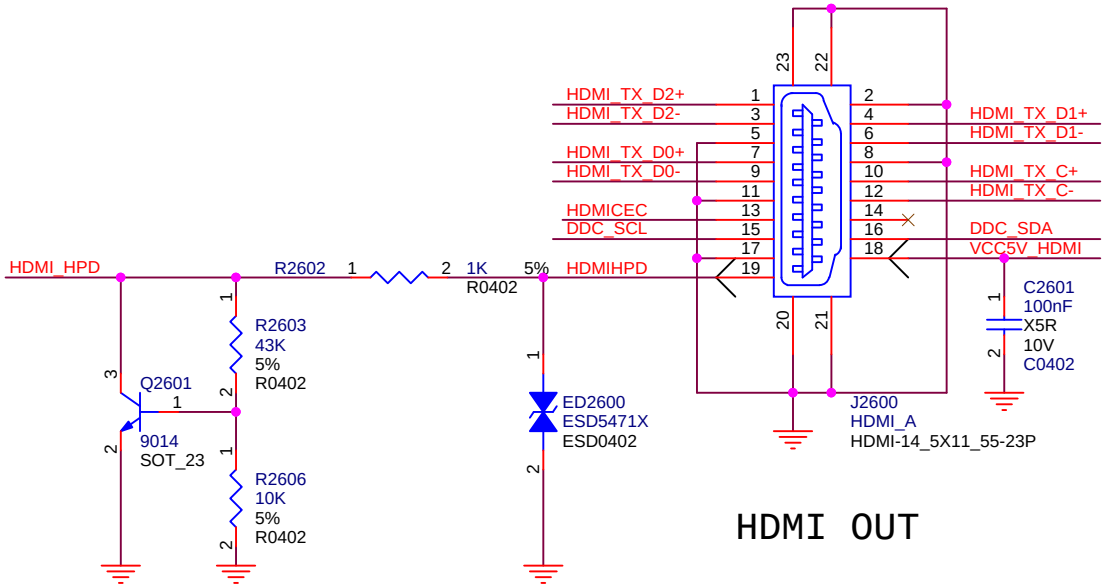




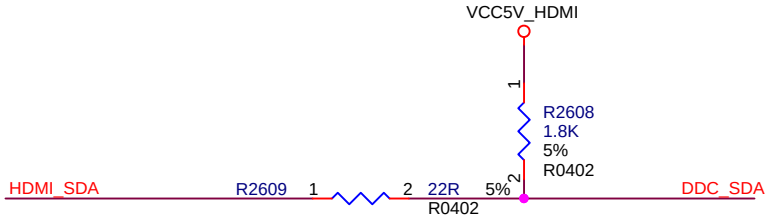


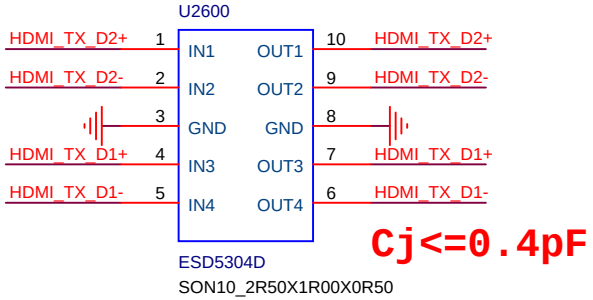
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Demo3		
File:	USB Port		
Date:	Tuesday, July 18, 2017	Rev:	V1.2
Designed by:	Zhangdz	Sheet:	18 of 24



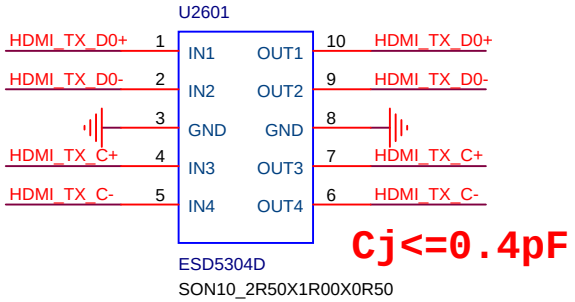


HDMI OUT





Cj<=0.4pF



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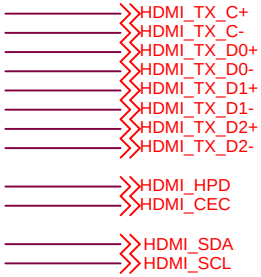
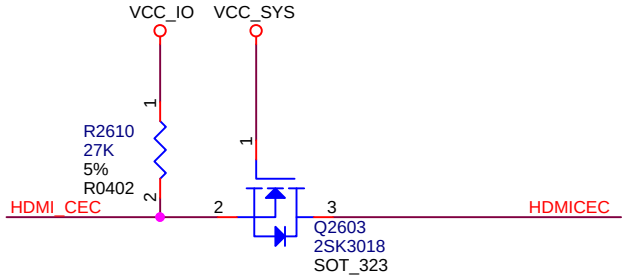
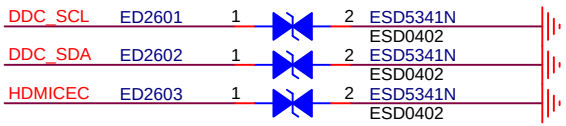
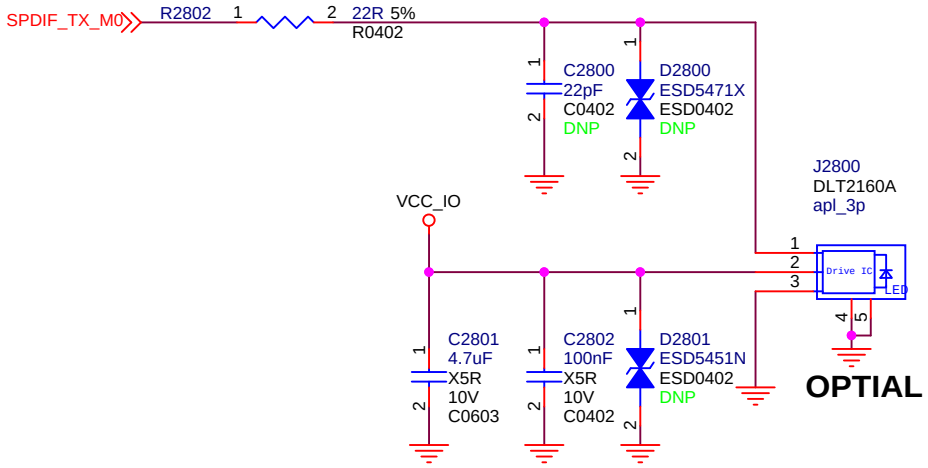






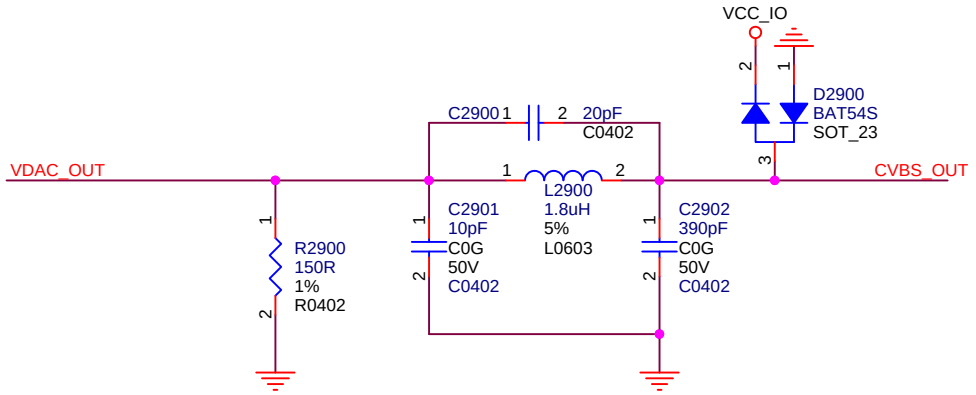
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Demo3		
File:	HDMI OUT Port		
Date:	Tuesday, July 18, 2017	Rev:	V1.2
Designed by:	Zhangdz	Sheet:	19 of 24

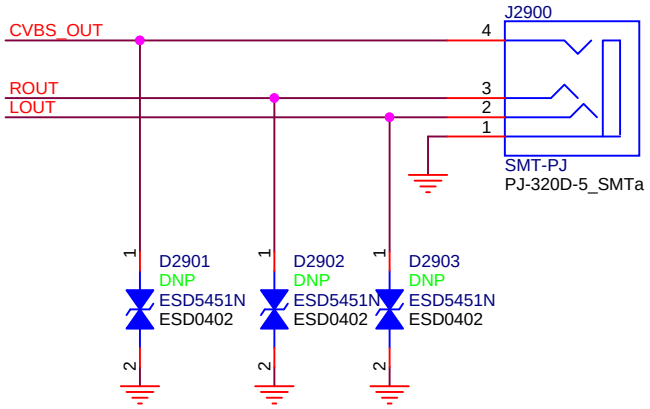


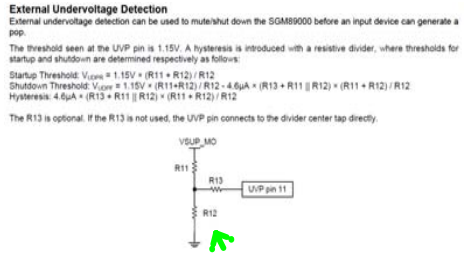
Optical SPDIF OUT

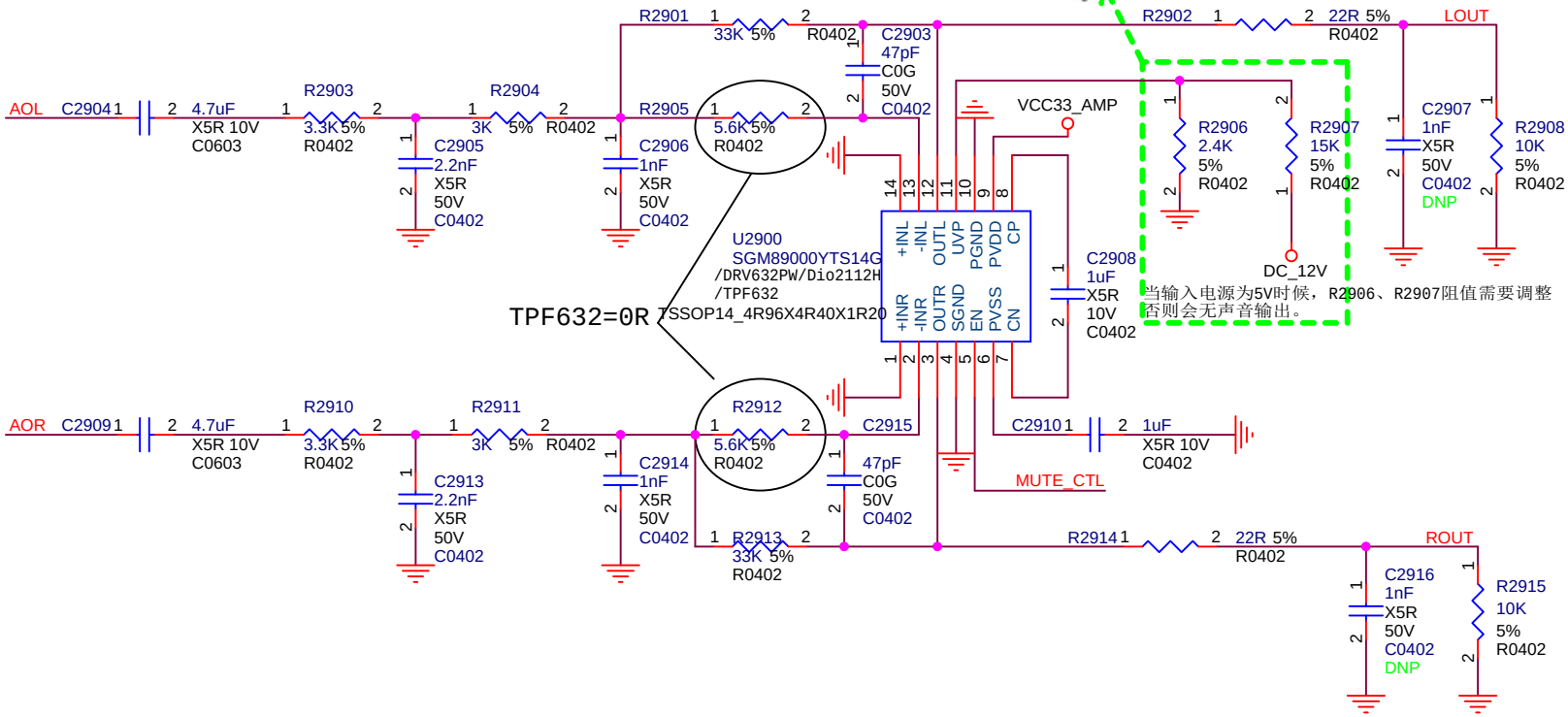
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Demo3		
File:	S/PDIF Port		
Date:	Tuesday, July 18, 2017	Rev:	V1.2
Designed by:	Zhangdz	Sheet:	20 of 24

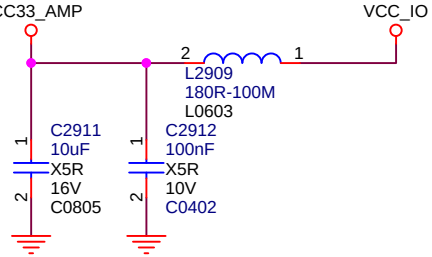
AV OUT





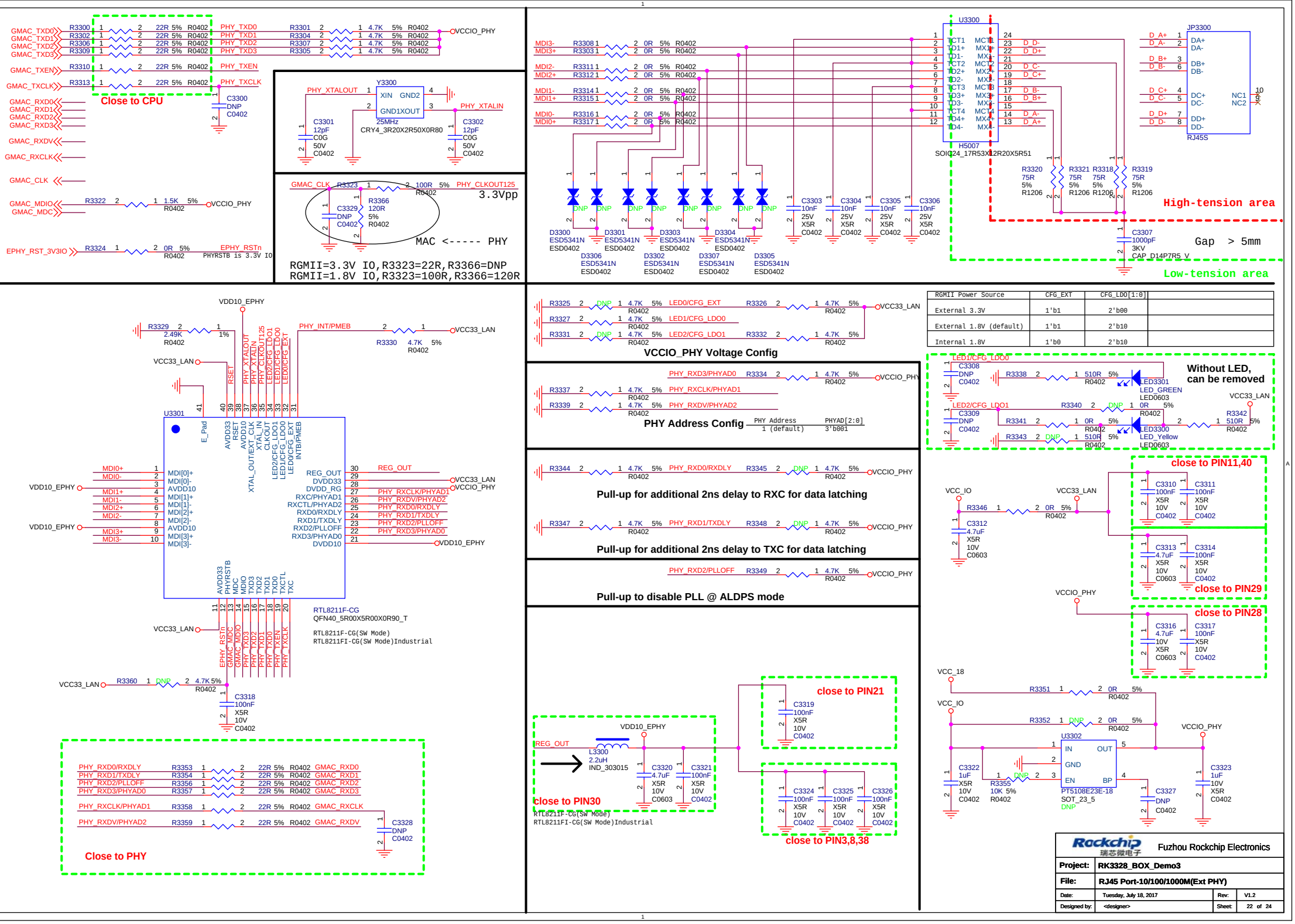






2-Vrms Audio Line Driver

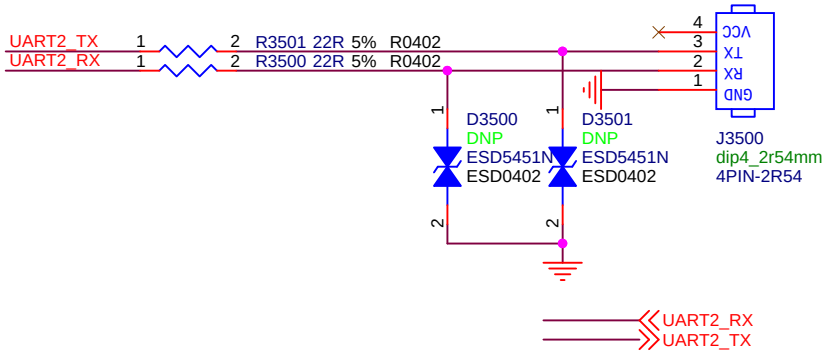
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Demo3		
File:	AV OUT Port		
Date:	Tuesday, July 18, 2017	Rev:	V1.2
Designed by:	Zhangdz	Sheet:	21 of 24



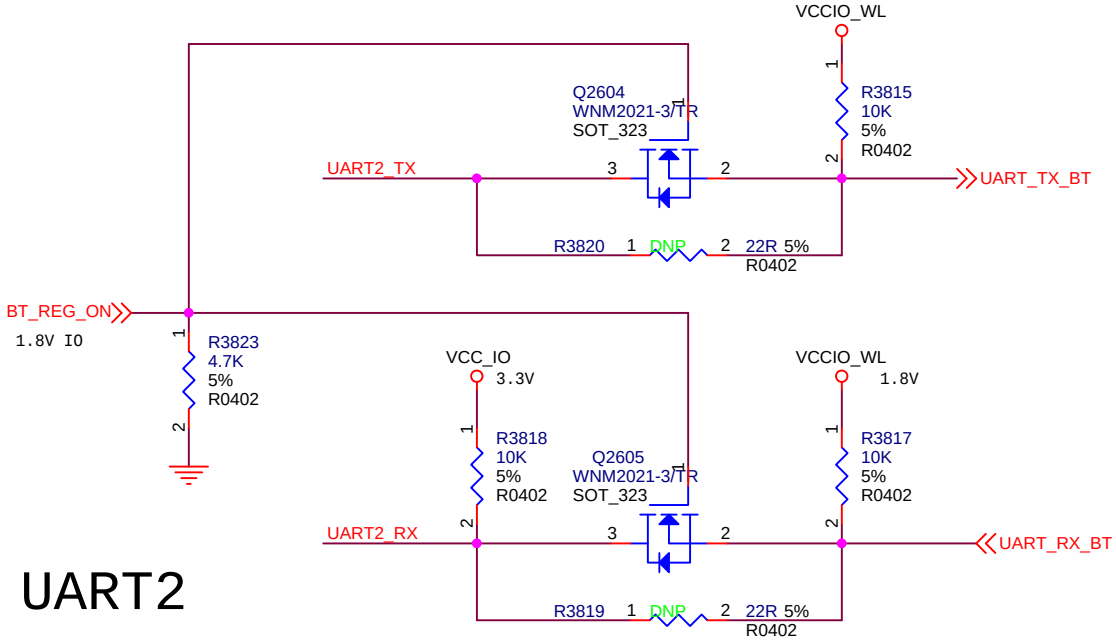
RGMII Power Source	CFG_EXT	CFG_LDO[1:0]	
External 3.3V	1'b1	2'b00	
External 1.8V (default)	1'b1	2'b10	
Internal 1.8V	1'b0	2'b10	

PHY Address	PHYAD[2:0]
1 (default)	3'b001

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Demo3		
File:	RJ45 Port-10/100/1000M(Ext PHY)		
Date:	Tuesday, July 18, 2017	Rev:	V1.2
Designed by:	<designer>	Sheet:	22 of 24



Debug UART2

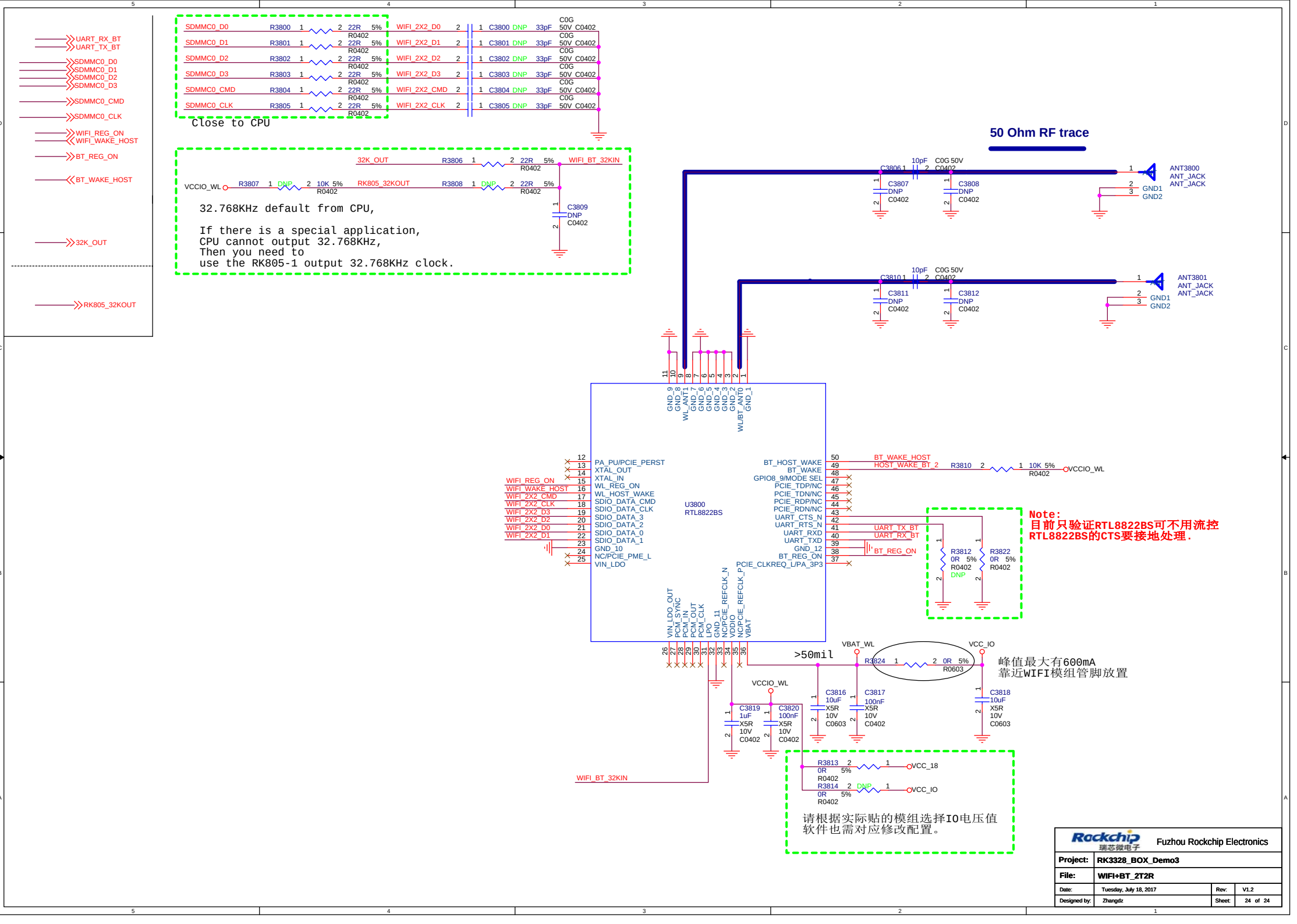


BT UART2

BT ON: BT UART,需移除Debug uart小板

BT OFF: Debug UART2，可接debug uart小板

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Demo3		
File:	Debug UART2/JTAG		
Date:	Tuesday, July 18, 2017	Rev:	V1.2
Designed by:	<designer>	Sheet:	23 of 24


UART_RX_BT
UART_TX_BT
SDMMC0_D0
SDMMC0_D1
SDMMC0_D2
SDMMC0_D3
SDMMC0_CMD
SDMMC0_CLK
WIFI_REG_ON
WIFI_WAKE_HOST
BT_REG_ON
BT_WAKE_HOST
32K_OUT
RK805_32KOUT
Close to CPU
32.768KHz default from CPU,
If there is a special application,
CPU cannot output 32.768KHz,
Then you need to
use the RK805-1 output 32.768KHz clock.
50 Ohm RF trace
U3800
RTL8822BS
Note:
目前只验证RTL8822BS可不用流控
RTL8822BS的CTS要接地处理.
>50mil
峰值最大有600mA
靠近WIFI模组管脚放置
请根据实际贴的模组选择IO电压值
软件也需对应修改配置。
Rockchip 瑞芯微电子
Fuzhou Rockchip Electronics
Project: RK3328_BOX_Demo3
File: WIFI+BT_2T2R
Date: Tuesday, July 18, 2017
Rev: V1.2
Designed by: Zhangdz
Sheet: 24 of 24