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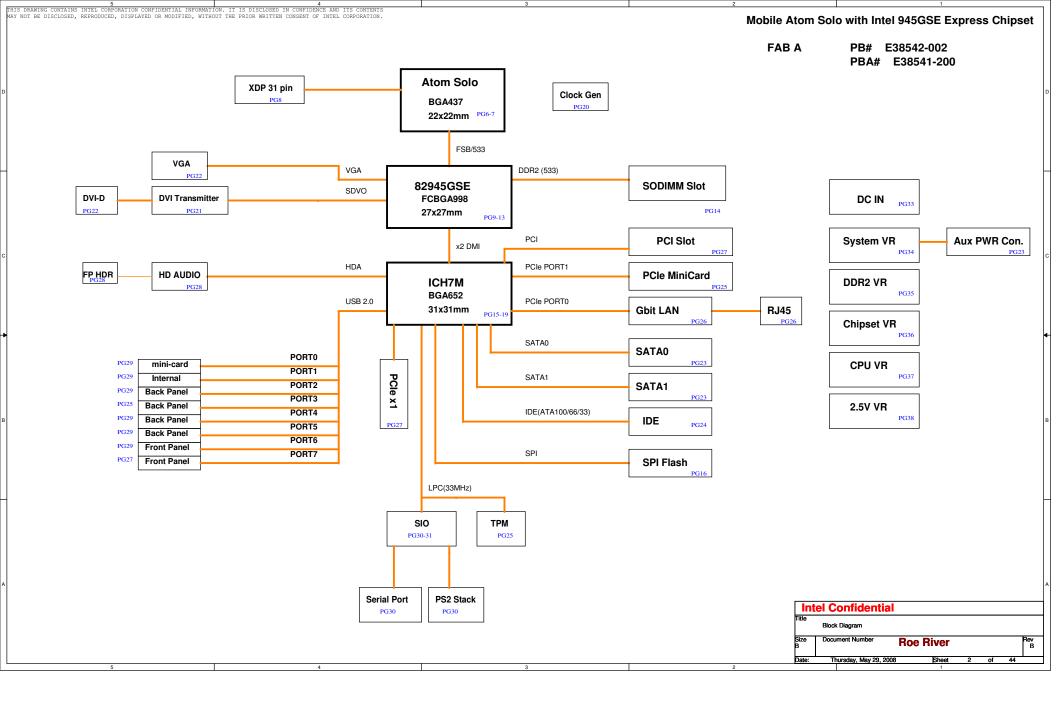
Mobile Atom Solo Processor for Mini-ITX Form Factor with Intel 945GSE Express Chipset

Prototype Schematics

For Roe River Reference Board

Intel Confidential

Int	el Confidential					
Title	Cover					
Size B	Document Number	Roe River				Rev B
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Voltage Rails

Power Plane	Description	Voltage	S0	S3	S4	S
DCIN	Adapter power supply	12V	V	V	~	V
+VCC_CORE	Core voltage for CPU	0.5-1.2V	1	X	X	×
+V1.05S	Chipset Power Rail	1.05V	1	X	X	X
+V0.9	0.9V Reserved for DDR2 SSTL Term and COMP	0.9V	1	1	X	X
+V1.8	DDR2 SM	1.8V	~	~	X	X
+V1.5S	Chipset Power Rail	1.5V	V	X	X	X
+V2.5S	Chipset Int Gfx Power Rail lout = 2.5A	2.5V	1	X	X	X
V3.3A_LAN	LAN power lout = 100mA	3.3V	1	~	~	V
+V3.3A	3.3V Standby	3.3V	~	~	V	V
+V3.3S	Peripheral Circuit (VCC3)	3.3V	1	X	X	X
+V5A	5V Standby	5V	1	1	V	V
+V5S	Peripheral Circuit (VCC)	5V	1	X	X	X
+5VDUAL	USB POWER	5V	1	~	·X	×
+V15A	Not Used	15V	V	V	V	X

CPU Core Power VID

X OFF

Vcc	Boot '	Volta	ge ty	pical	equal	L 1.1	7
VID6	VID5	VID4	VID3	VID2	VID1	VID0	Vcc (V)
0	0	1	1	0	0	0	1.2000
0	0	1	1	0	0	1	1.1875
0	0	1	1	0	1	0	1.1750
~~~~	~~~~	~~~~		-~~~	-~~~	-~~~	~~~~~
1	0	0	1	1	1	0	0.5250
1	0	0	1	1	1	1	0.5125
1	0	1	0	0	0	0	0.5000

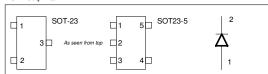
#### Net Naming Conventions

Suffix
# = Active Low Signal
DN and DP are differential pairs
Prefix
H = Host
M = DDR Memory
TP = Test Point (does not connect anywhere else)
· · ·

# Schematic Conventions



# PCB Footprints



# I ² C / SMB / SDVO Addresses

Device	Address	Hex	Bus
Clock Generator	1101 001x	D2	SMB_ICH_S
SO-DIMM0	1010 000x	A0	SMB_ICH_S
PCIE Mini Slot	TBD	TBD	SMB_ICH_A
TPM	1001 100x	98	SMB_EC_S
XDP	TBD		SMB_MAIN
DVI	70h		SDVO

#### Jumper Settings

-2	Chassis Intrusion
-2	Clear CMOS
-2	BIOS Config
	-2

# Test Notes

0.002 Ohm resistors for current measurement in Fab A, to be removed in Fab B  $\,$ 

#### LEDs

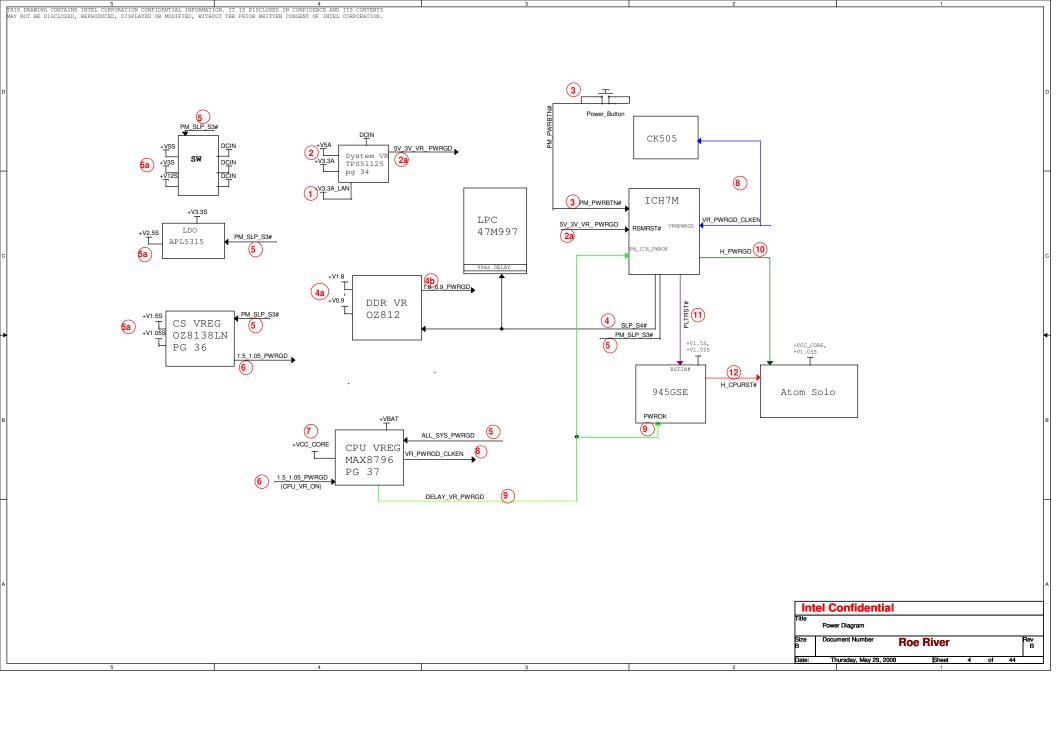
LED							Pa	ge				R	efere	ence	
DCIN - RED +5VA - RED +5VS - YELLOW +2.5S - GREEN +V3.3S- YELLOW	=	=	=	=	=	=	32 32 32 32 32 32	=	=	=	=	=	D2 D3 D4 D5 D6		_

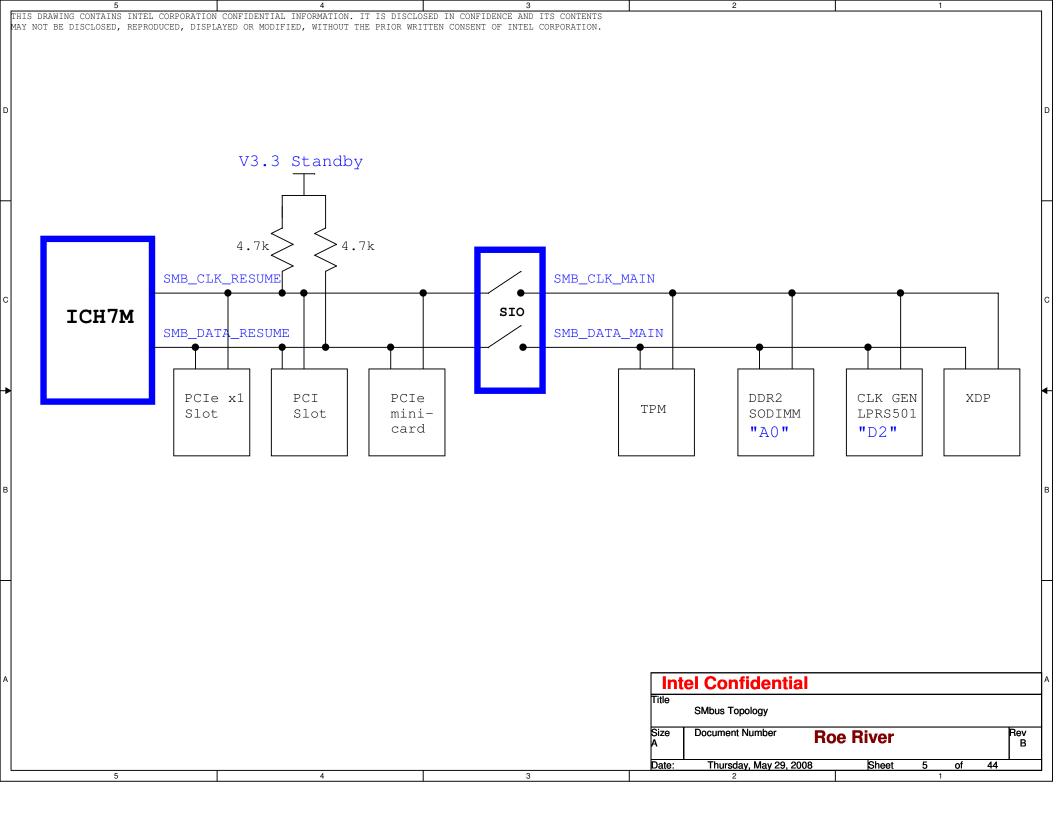
### Buttons

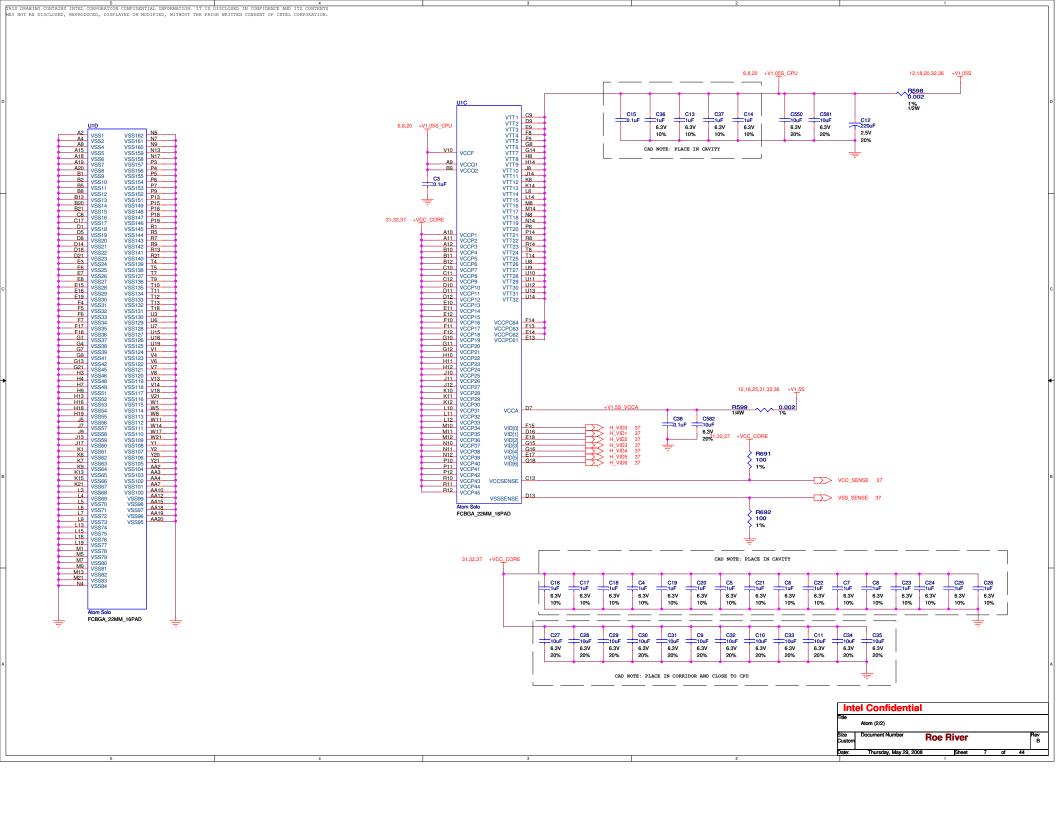
Reference	Description	Page
SW2	Power Button	31

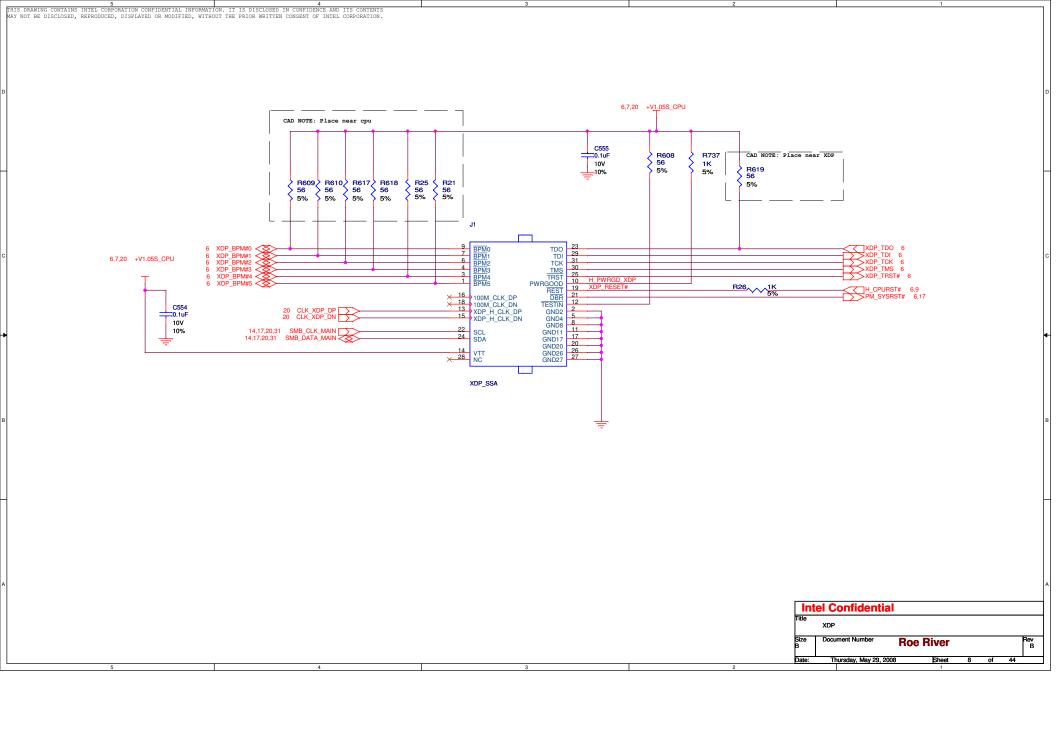
#### Power States

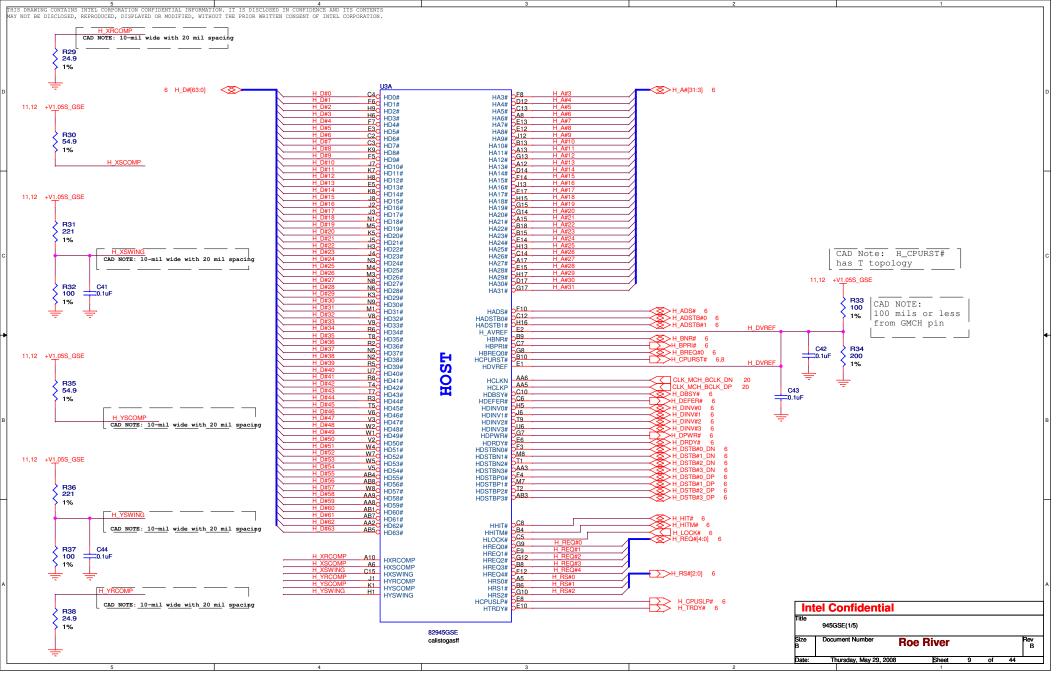
SIGNAL	PM_EN_5VA_3VA#	PM_SLP_S4#	PM_SLP_S3#	+V*A	+V*	+V*S	Clocks
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	HIGH	HIGH	LOW	ON	ON	OFF	OFF
S4 (Suspend To Disk)	HIGH	LOW	LOW	ON	OFF	OFF	OFF
S5 / Soft OFF	LOW	LOW	LOW	OFF	OFF	OFF	OFF

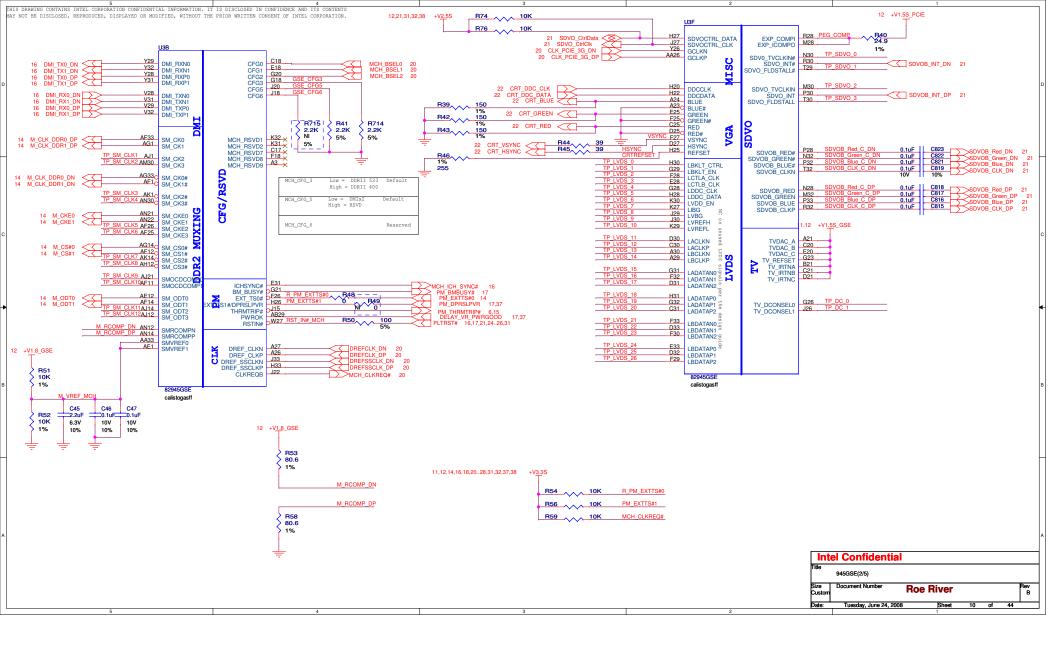


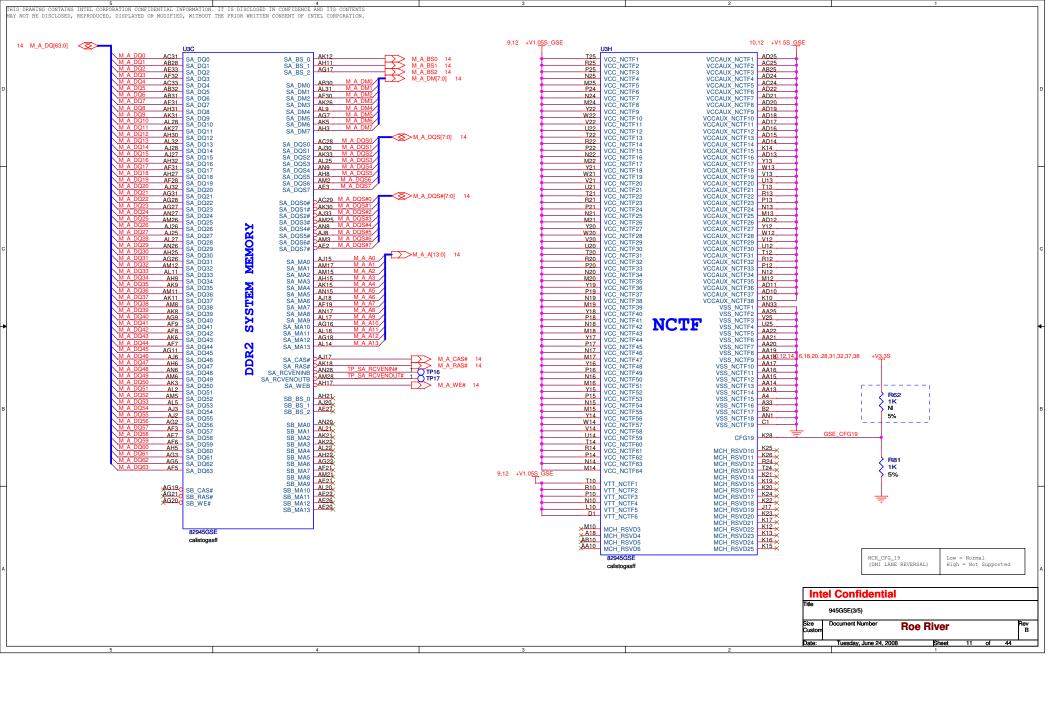


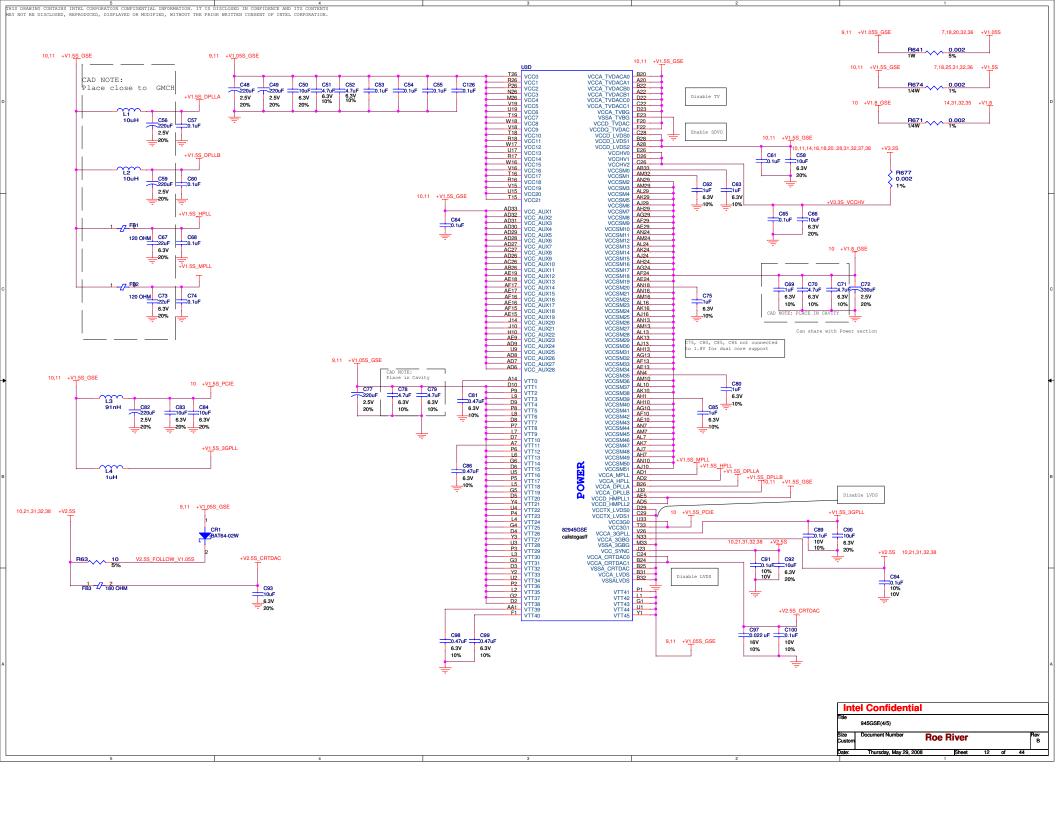


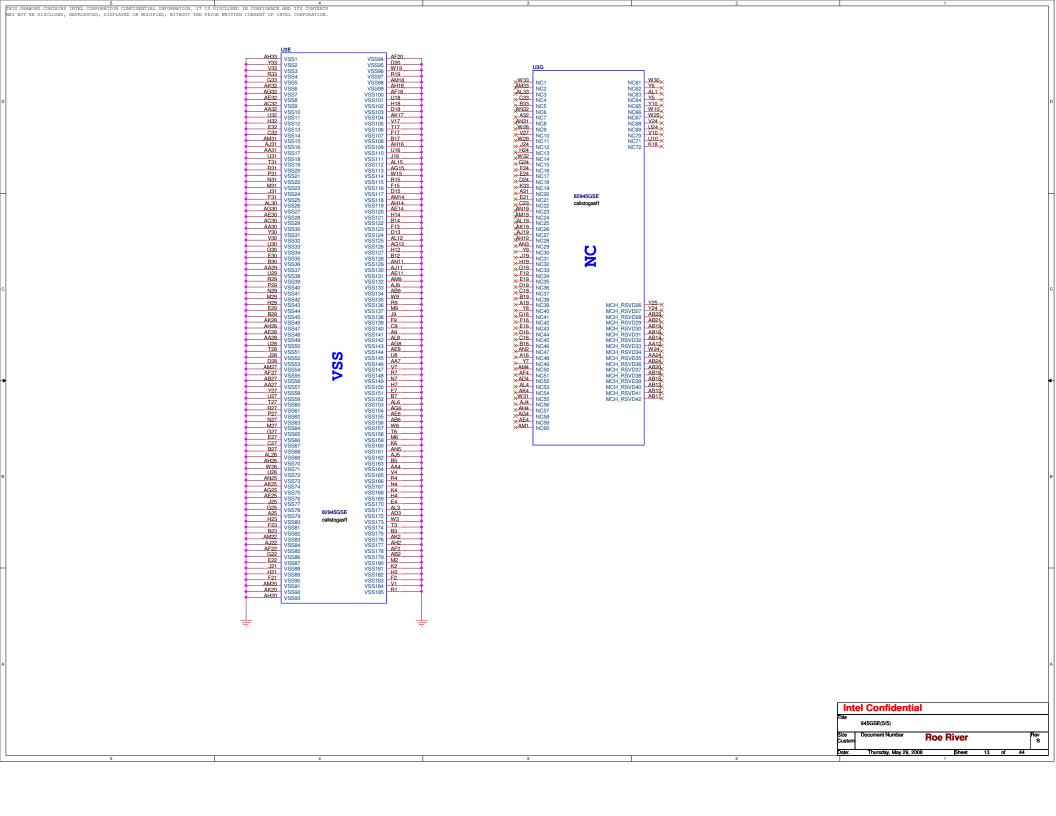


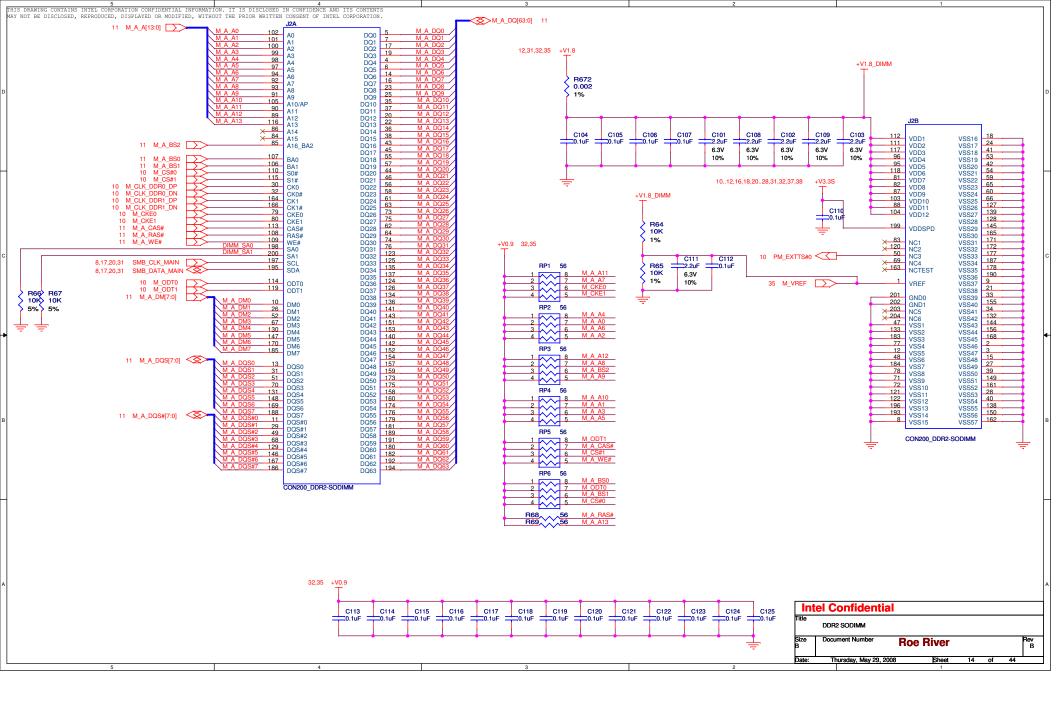


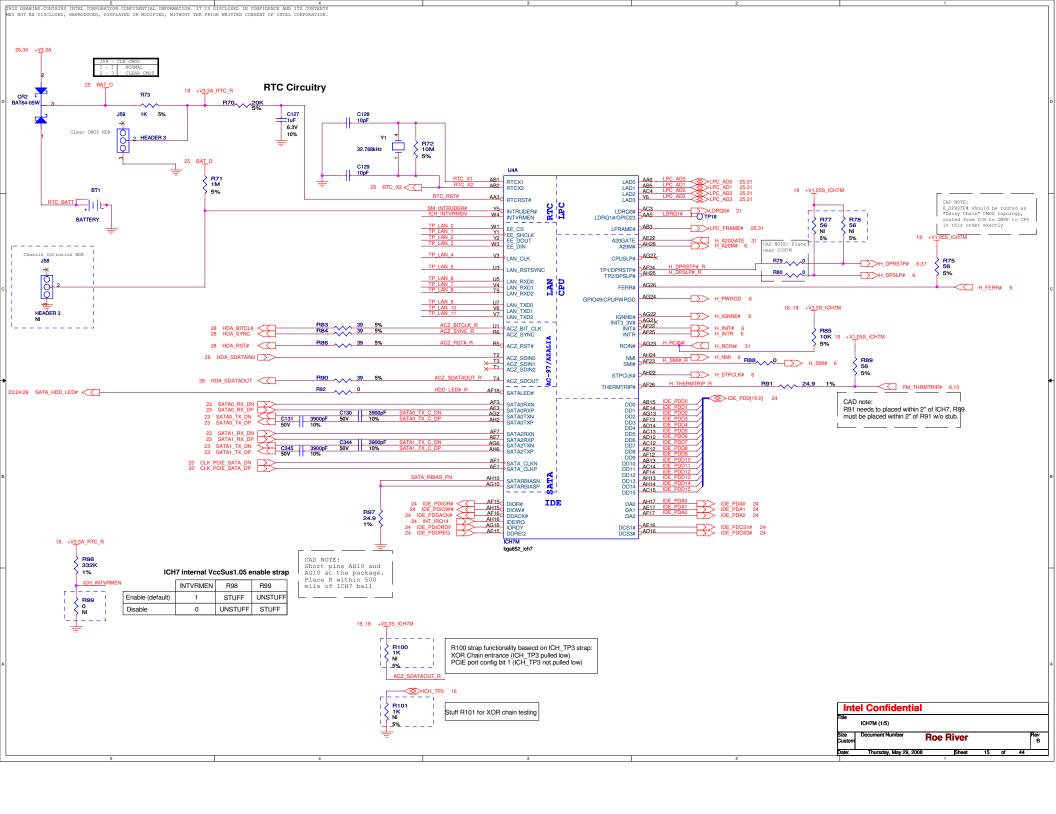


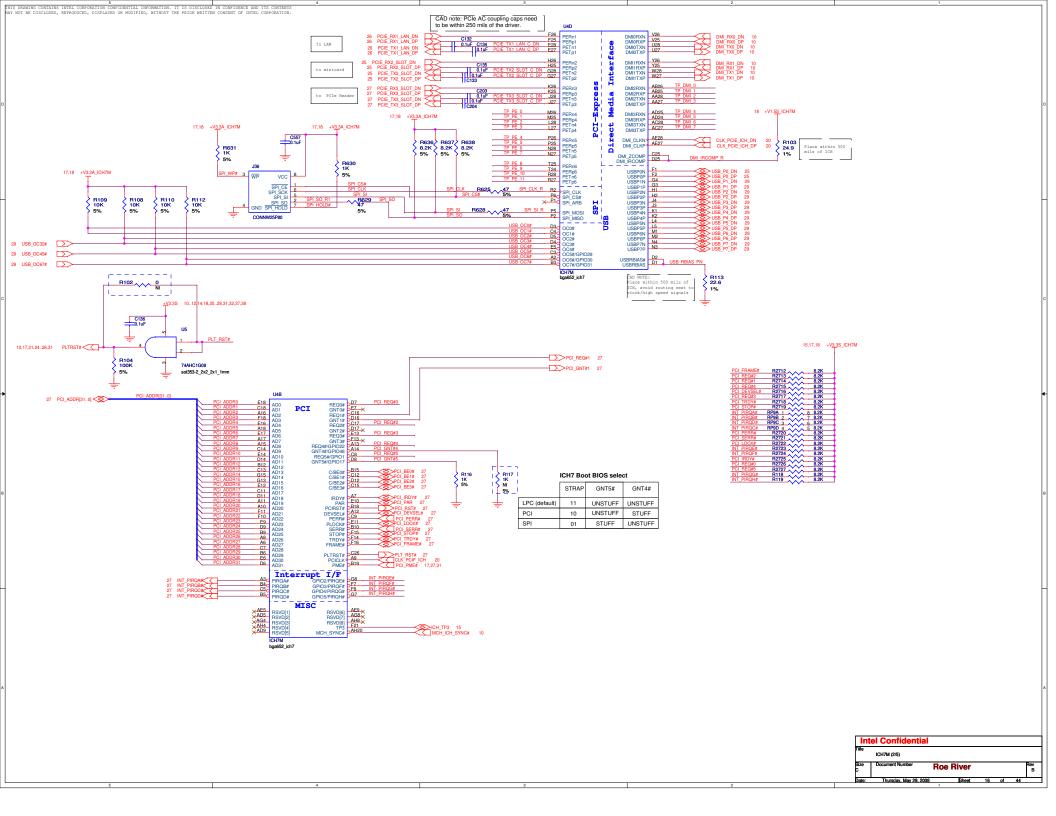




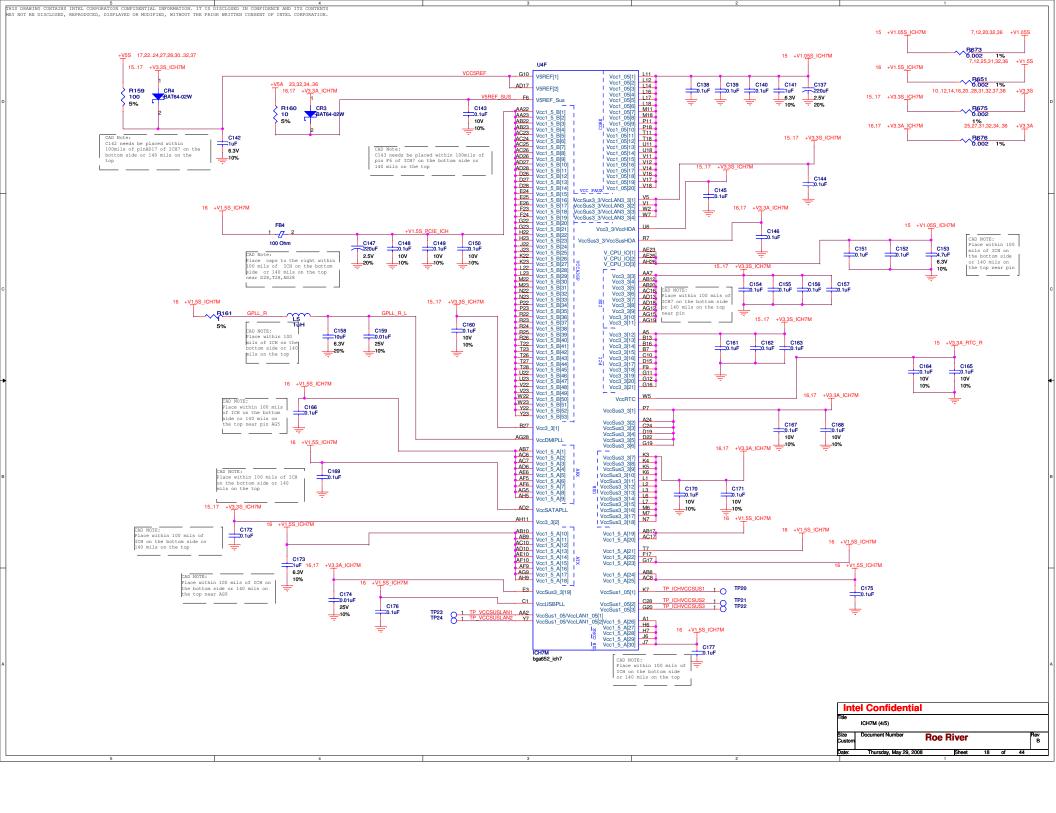


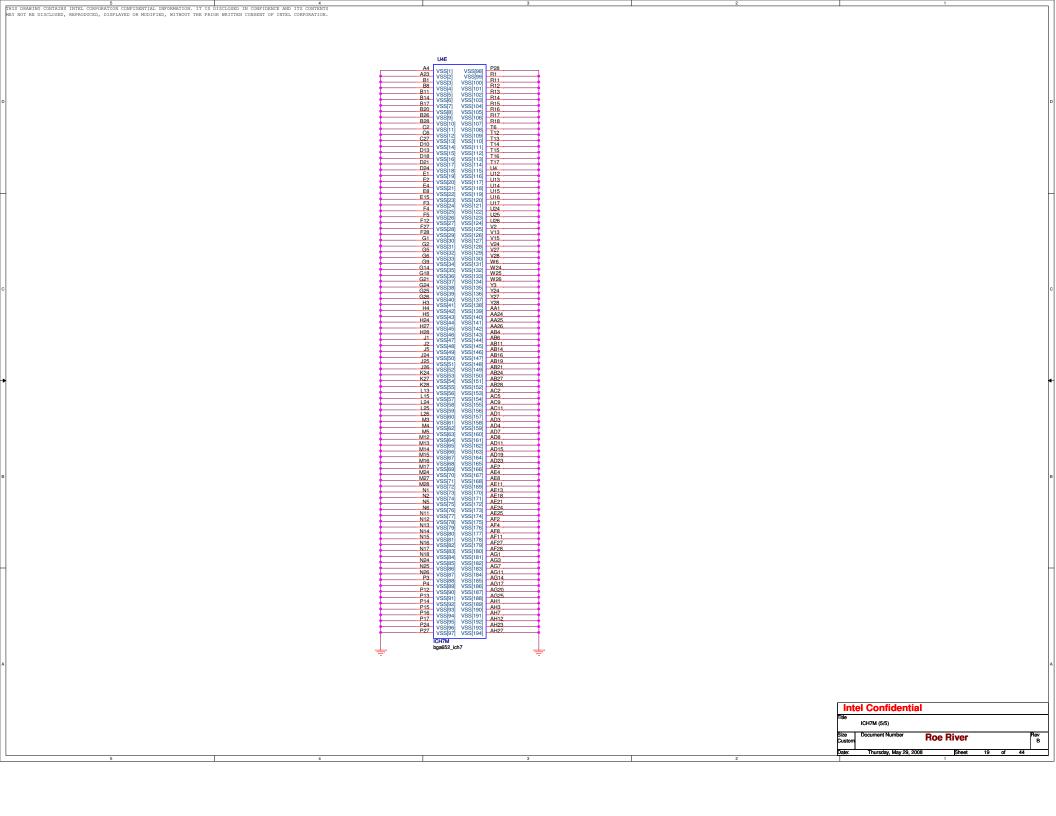


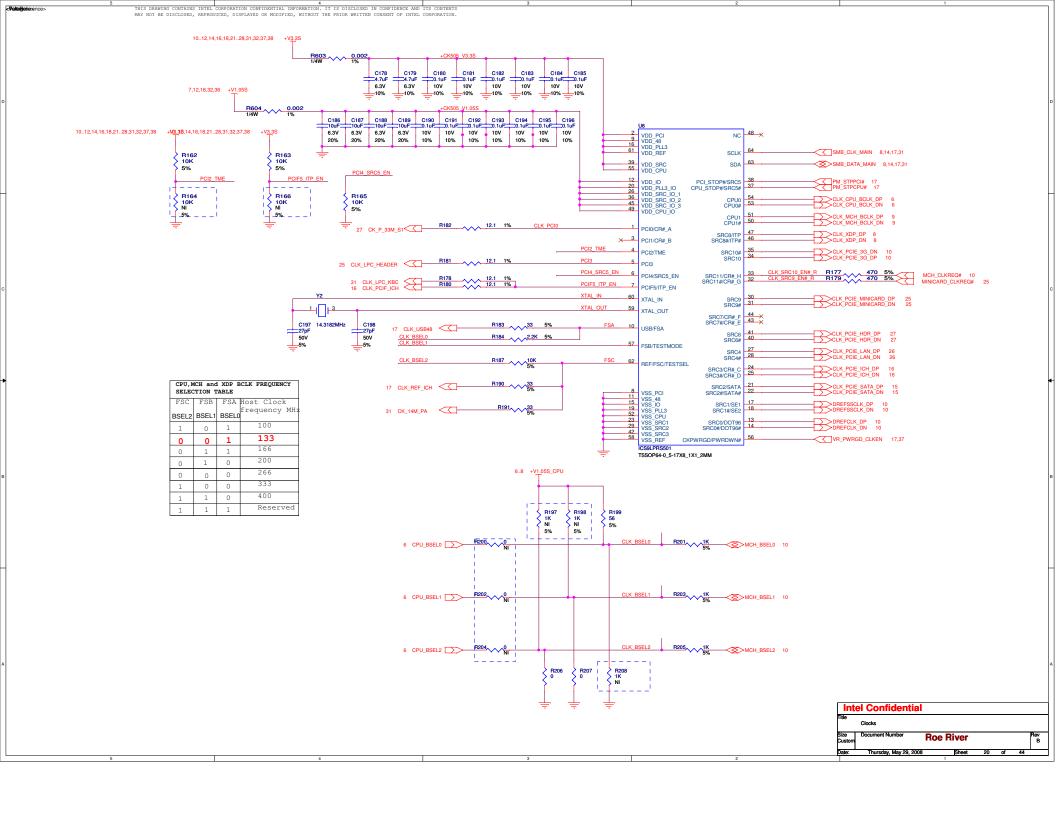




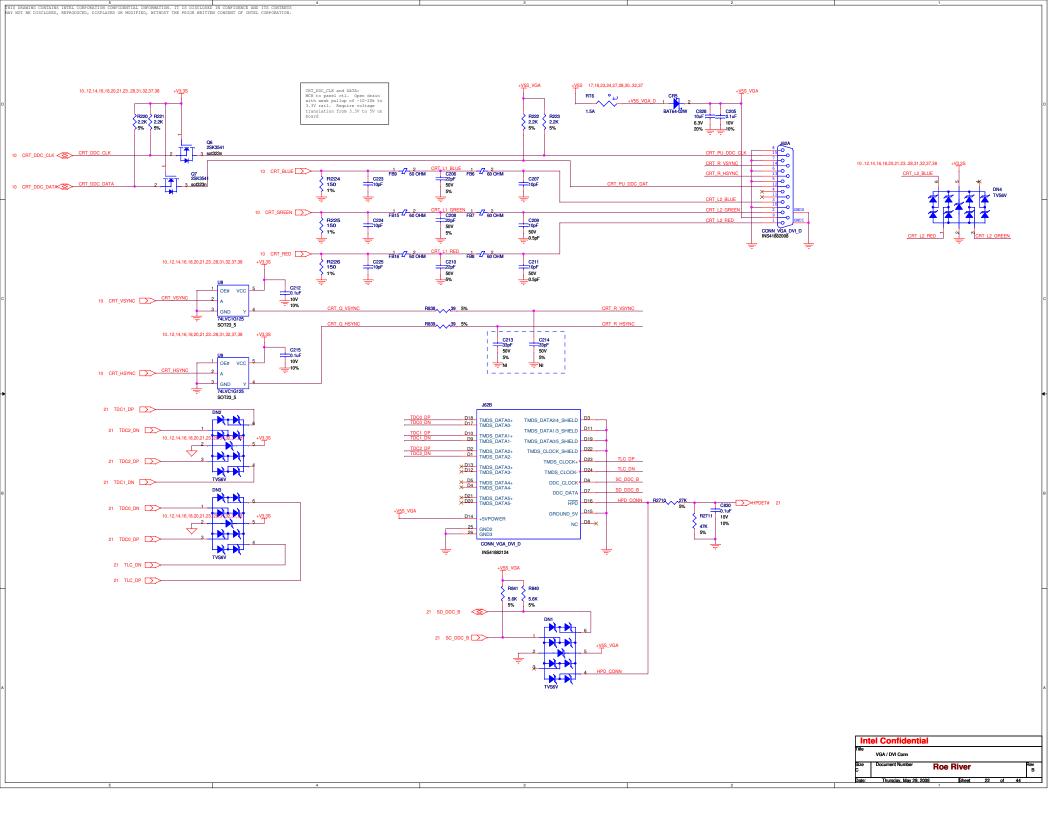
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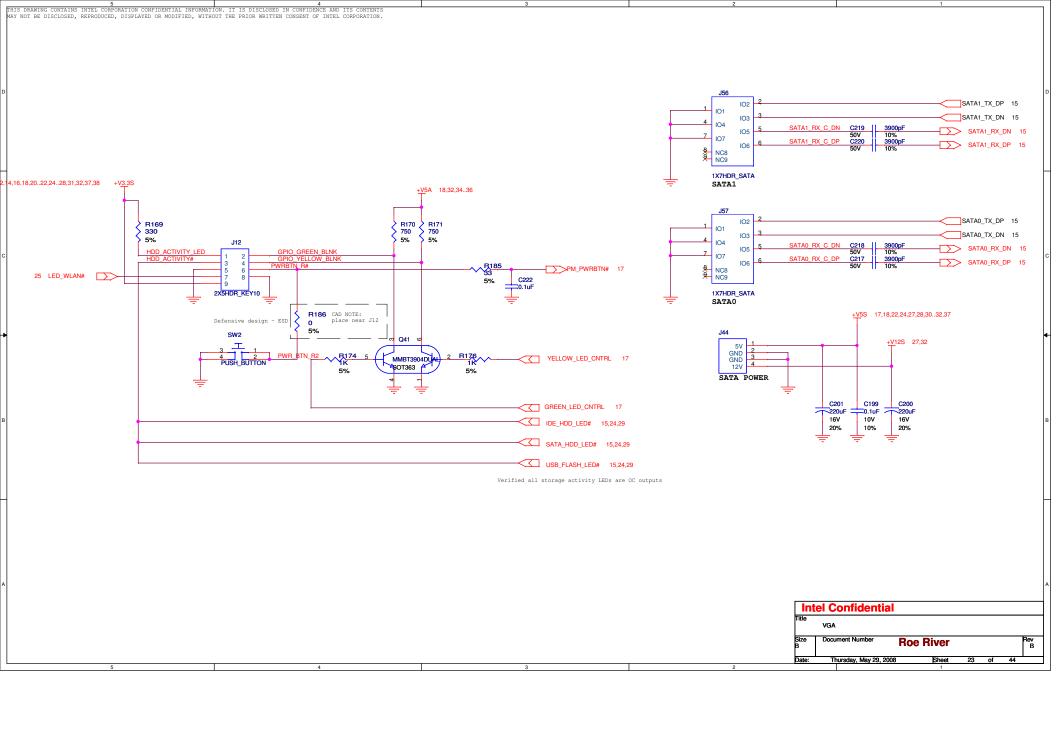


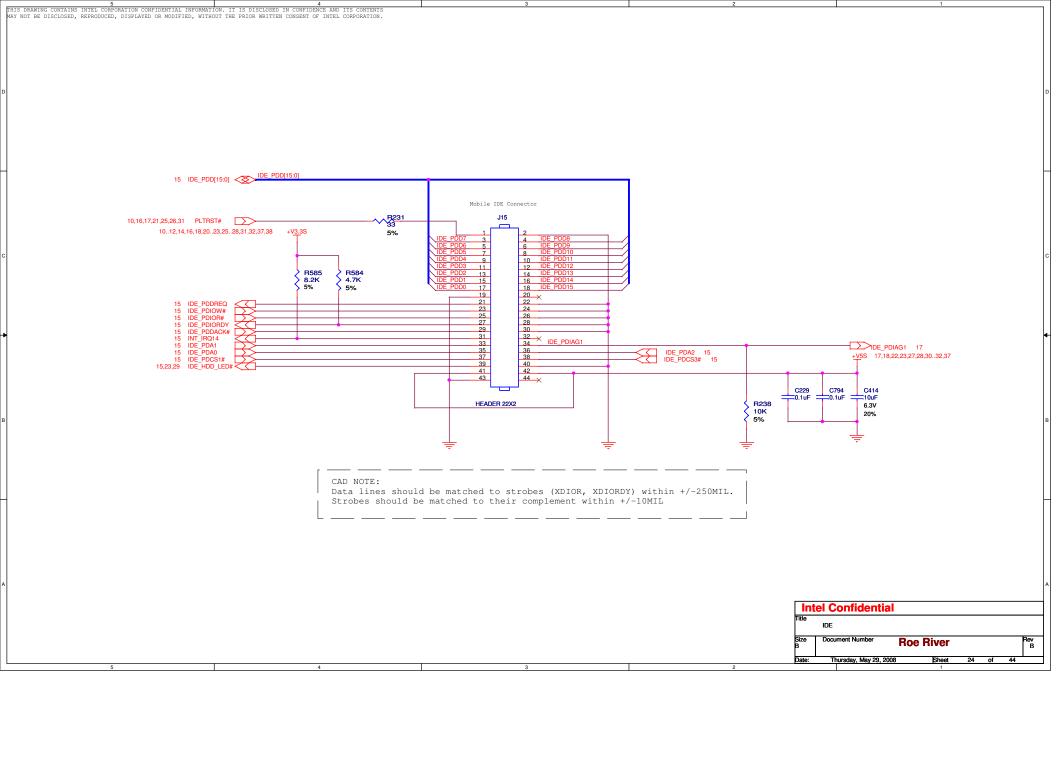


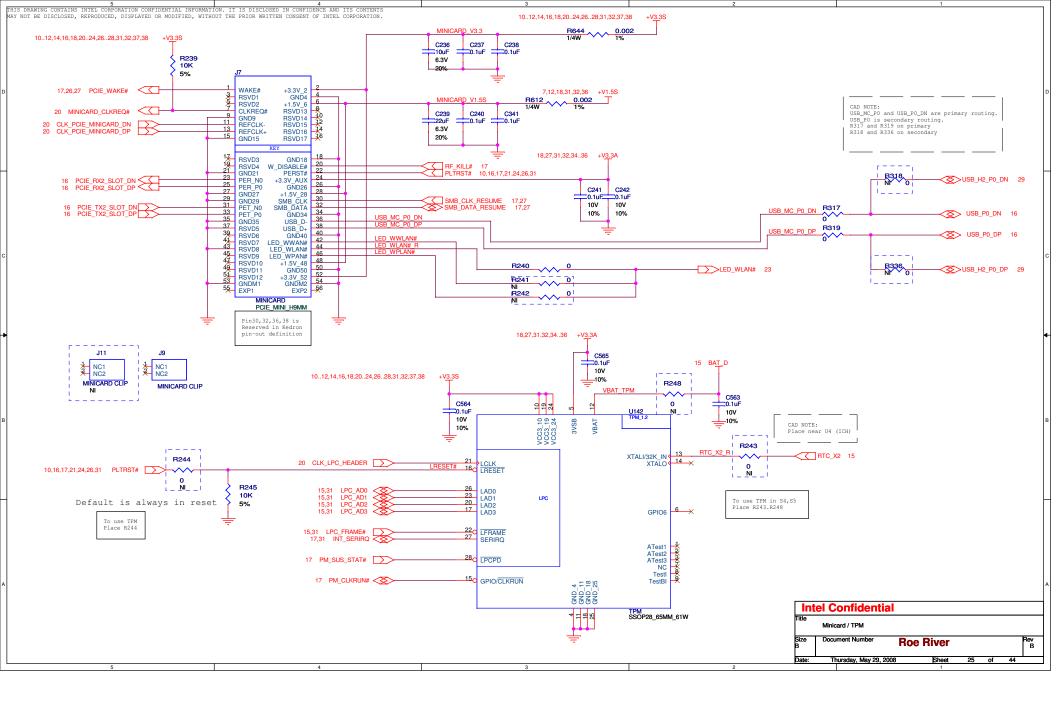


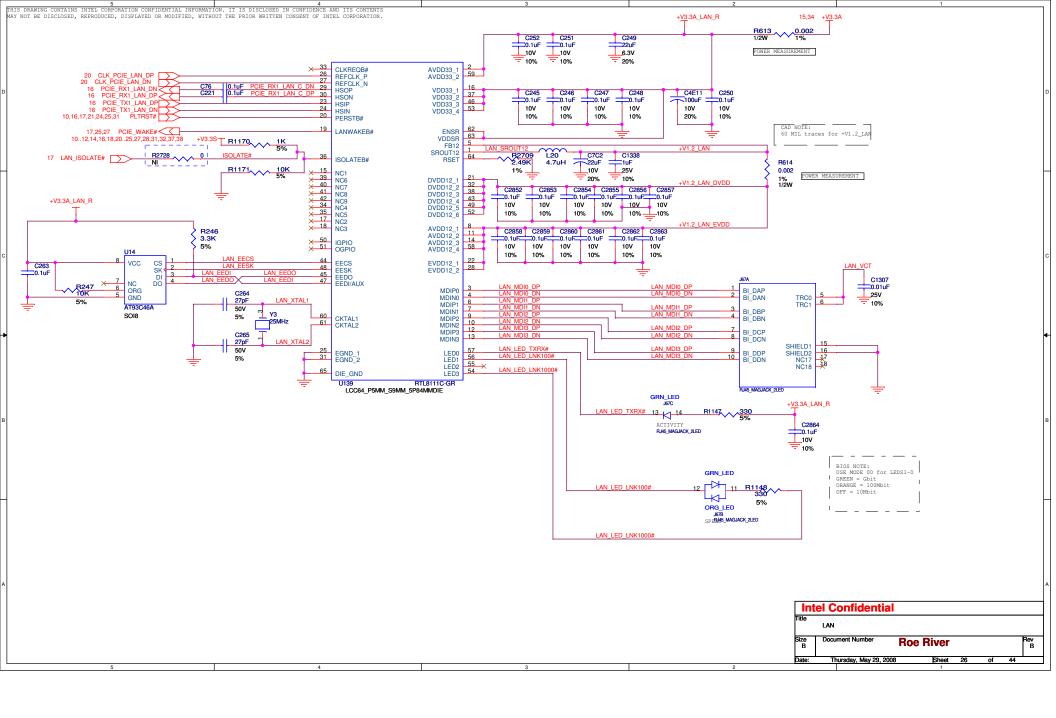
0.1uF C796 SDVOB INT C DP 10 SDVOB_INT_DP 0.1uF C797 10 SDVOB_INT_DN 10 SDVOB_Green_DP 10 SDVOB_Green_DN 10 SDVOB_Blue_DP 10 SDVOB_Blue_DN SDVOB_CLK_DN 10 10,12,31,32,38 +V2.5S SDVOB_CLK_DP 10 C798 C799 C800 C801 10uF 0.1uF 0.1uF 0.1uF EU48 6.3V 20% AVDD_48 AVDD_48 BOANGS FB12 C803 C802 C804 10uF 0.1uF 0.1uF 0.5pF R817 0 TDC0_DN 22 120 OHM 6.3V +V3.3S FB13 TDC0
TDC0*
TDC1*
TDC1*
TDC2*
TDC2*
TLC
TLC* C807 C808 C809
120 OHM 10uF 0.1uF 0.1uF
6.3V
FB14 TVDD_15 TVDD_21 15 21 5% CH7307C 0.5pF R823 0 TDC2_DN 22 10..12,14,16,18,20,22..28,31,32,37,38 +V3.3S AVDD_PLL PQFP48_5MM_GNDPAD217 R824 0 TLC_DP 22 R826 C813 R827 0 TIC_DN 22 22 HPDET# 10,16,17,24..26,31 PLTRST# R835 R836 VSWING 5.6K 5.6K 5% 5% 7 | R837 0 AGND 31 AGND 39 AGND 45 AGND 7 DGND 7 DGND 24 TGND 18 DIE_PAD 99 R833 C814 0.1uF 10K 5% ADD2 PROM shall be attached to the SDVO device that responds to an address of 70h. Intel Confidential Roe River

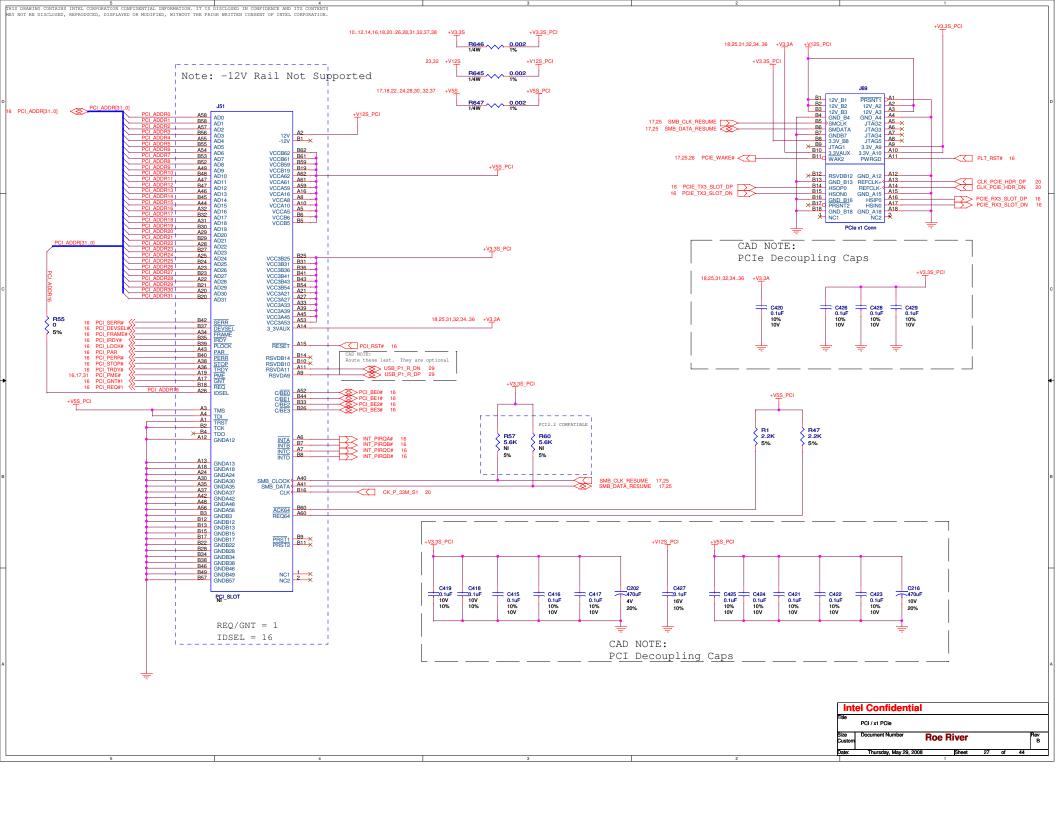


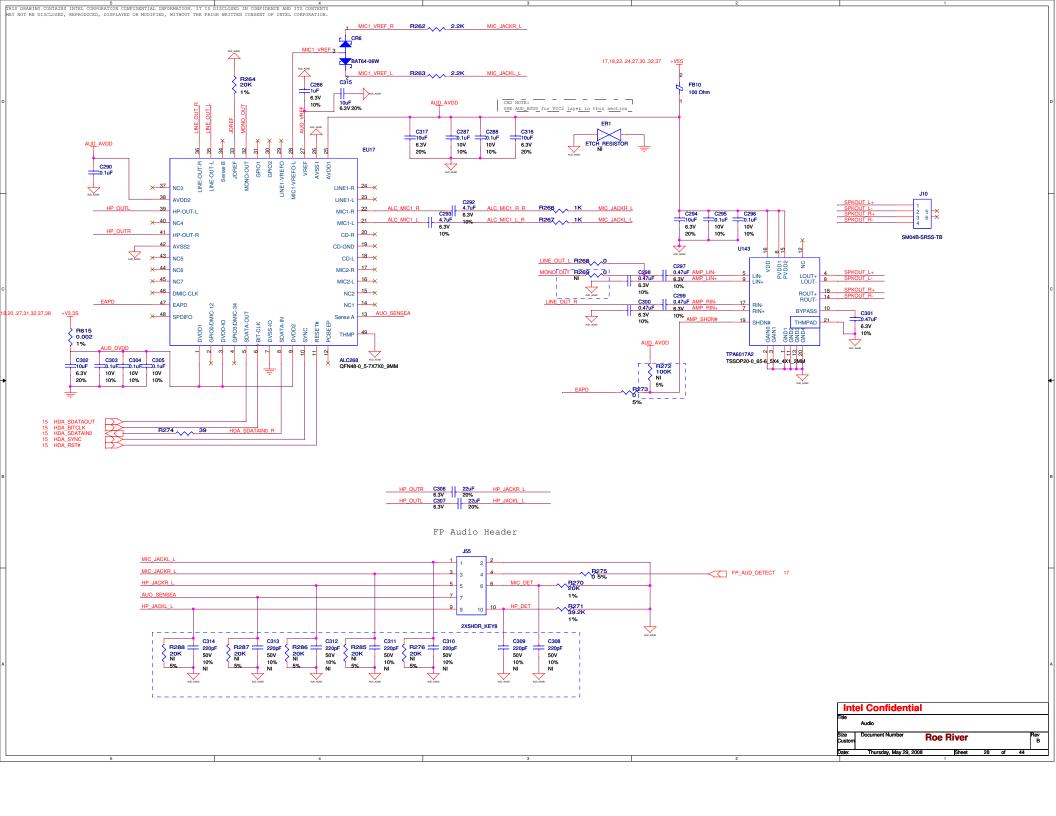


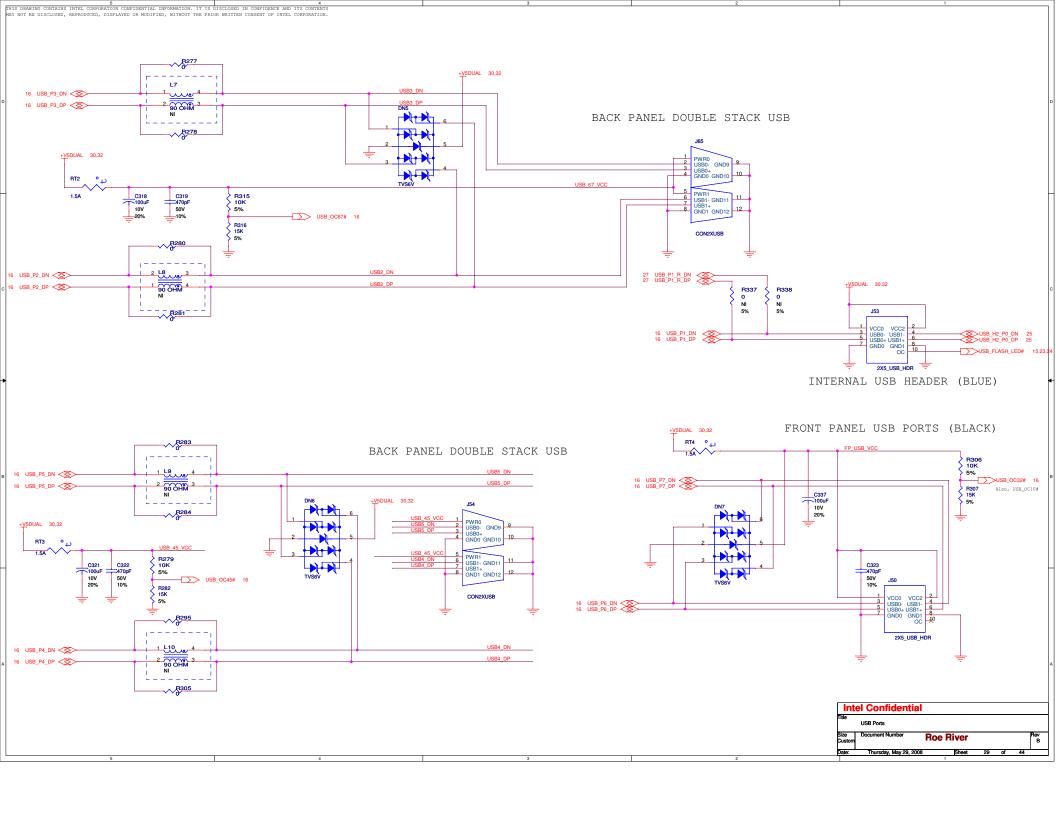


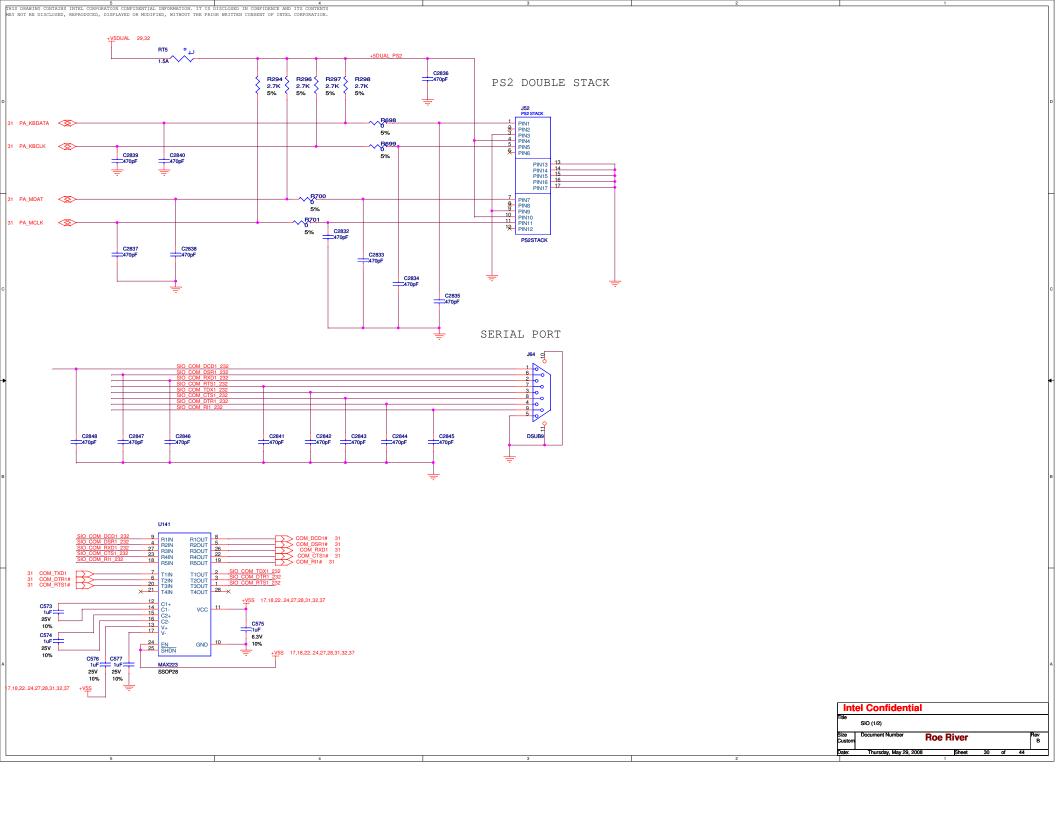


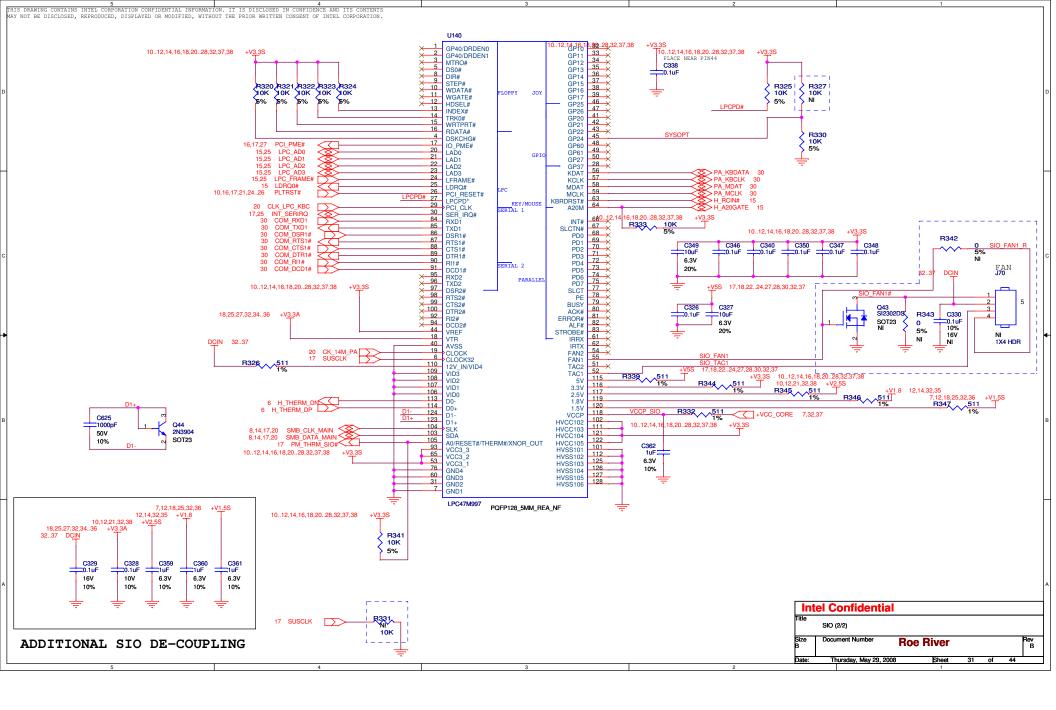


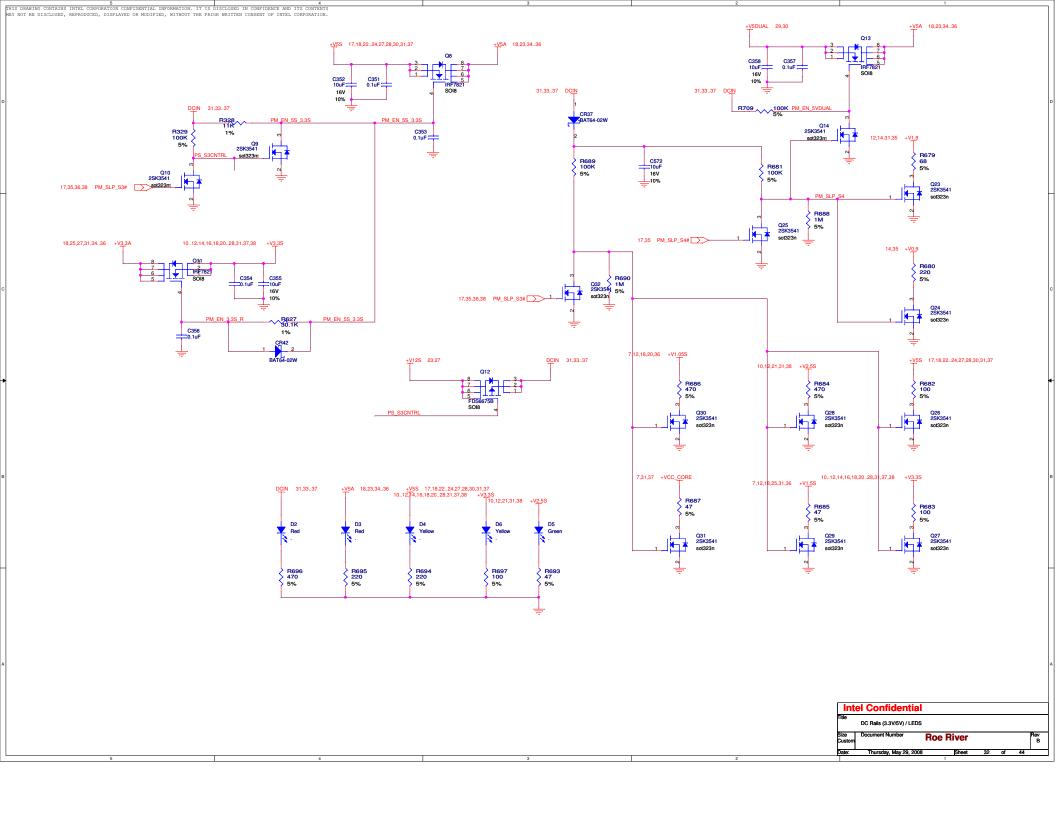


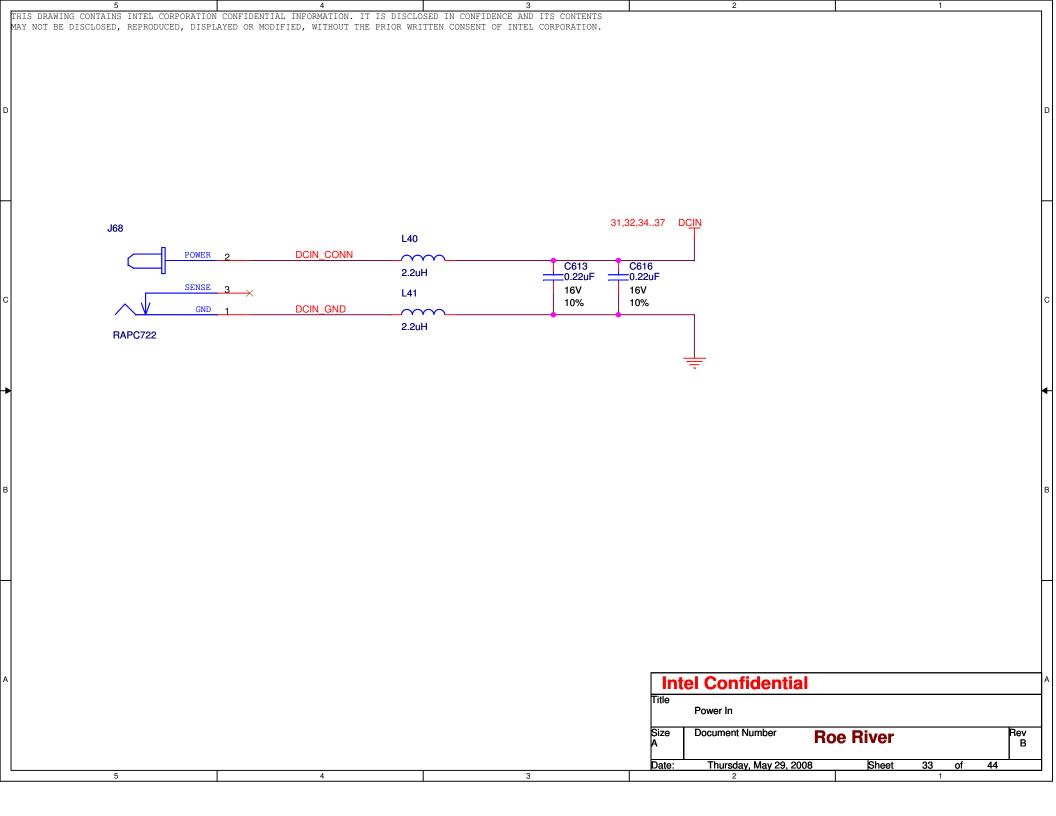




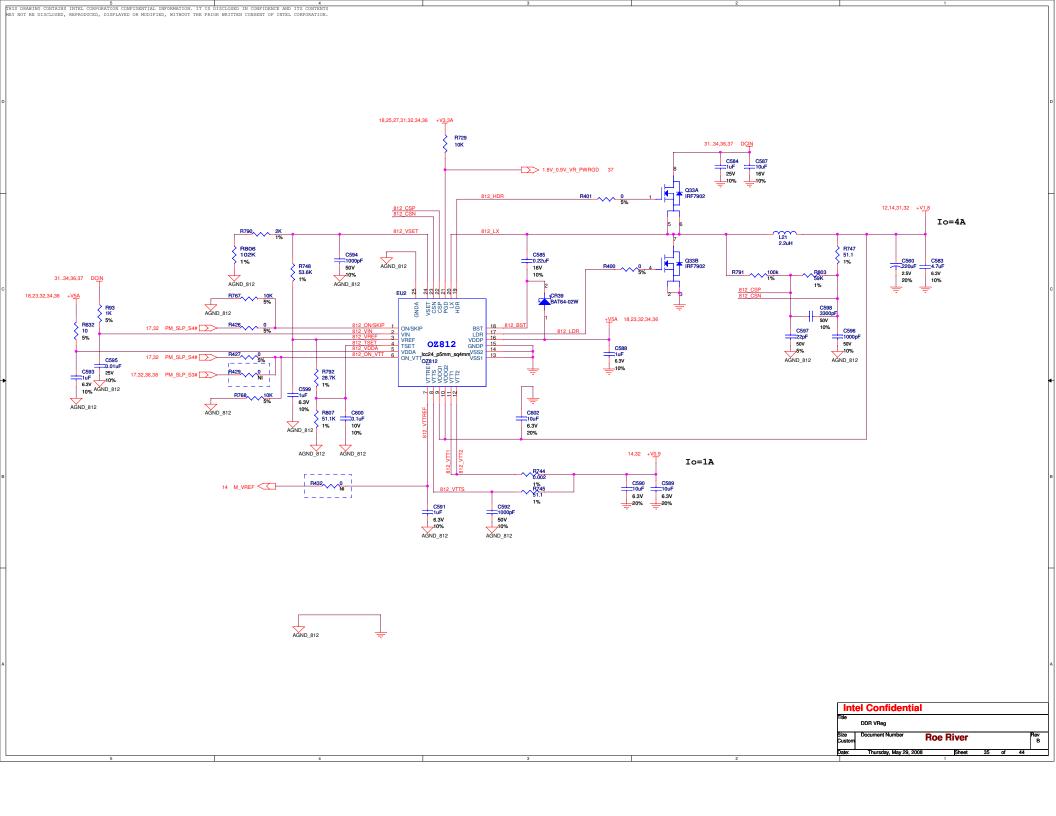


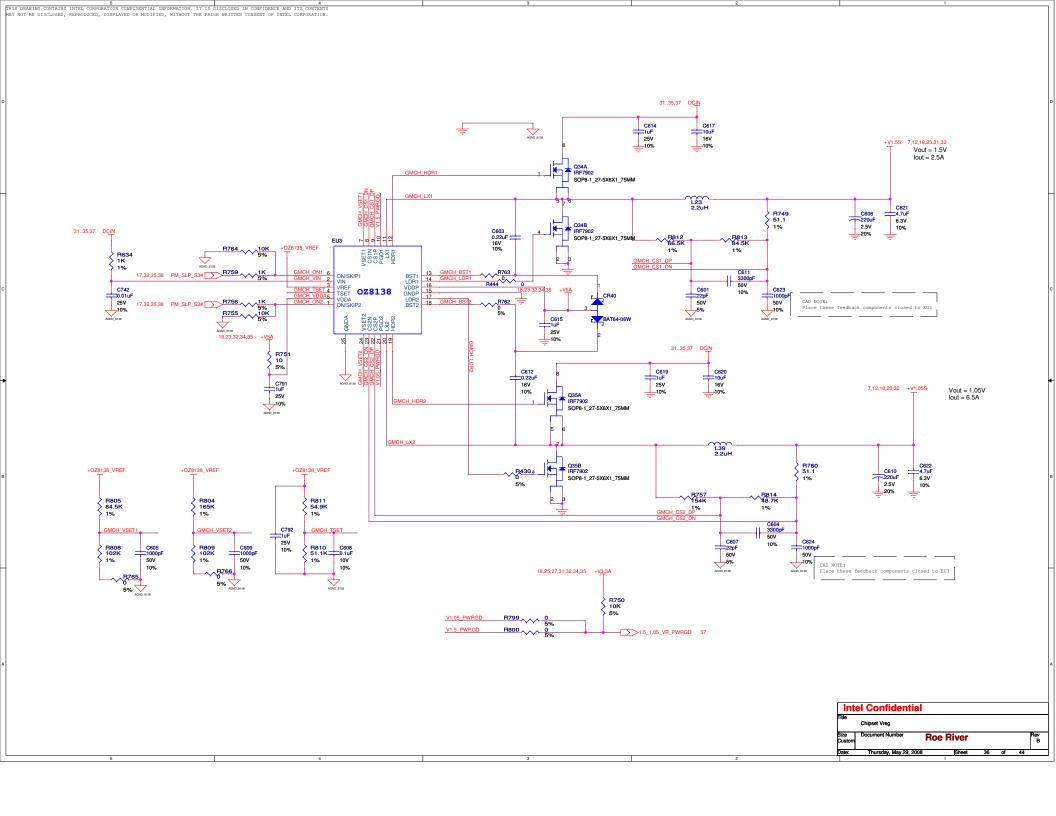


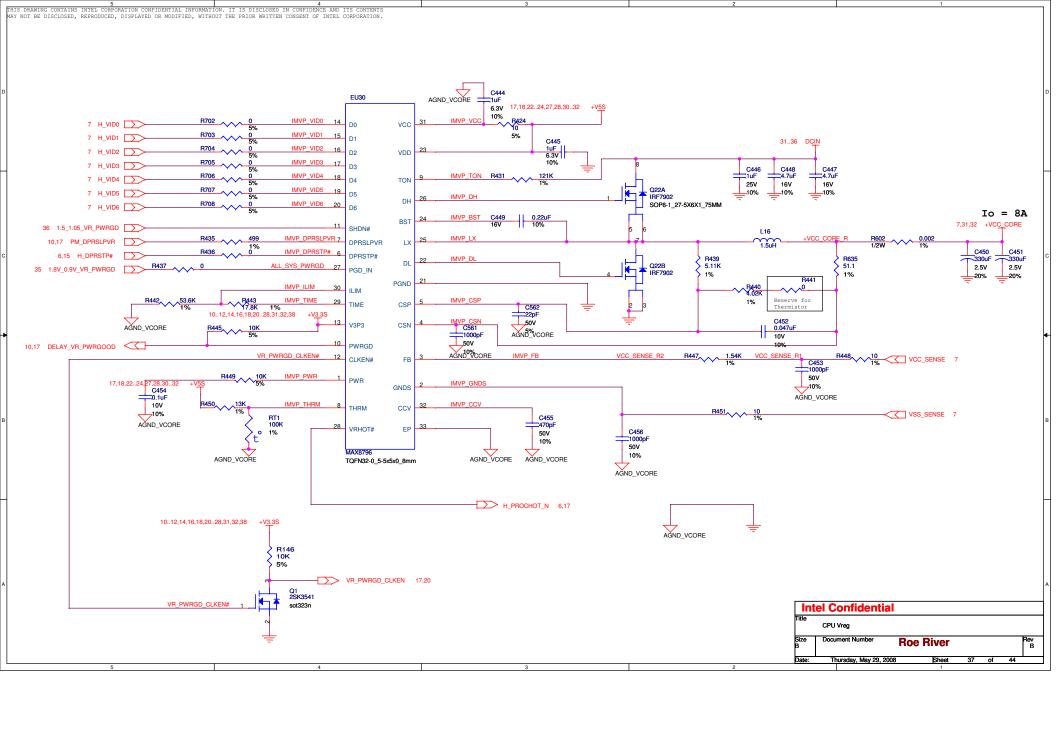


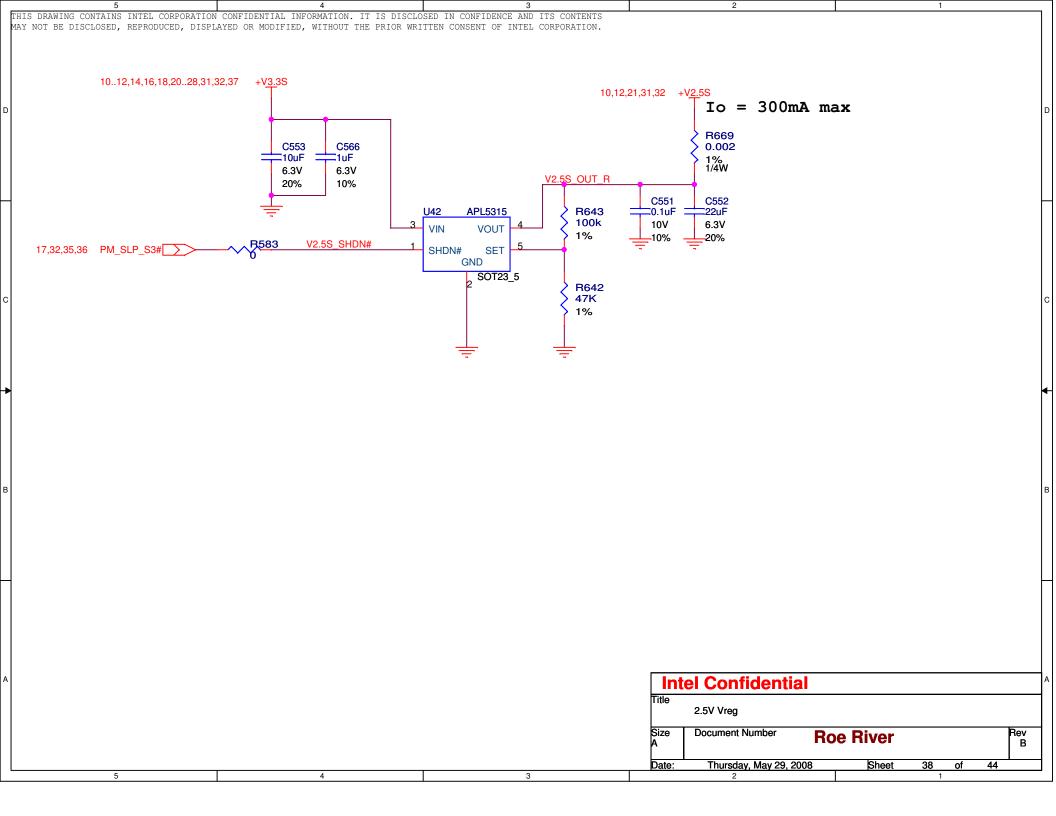


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	Pages	Do	Data			
Item  MH1 - MH4	Reason  Update solder stencil to allow solder paste on MH1 - MH4 for mounting nut attachment	Page	<b>Date</b> May 5, 2008			
mii - mid	opuace Solder Scendir to allow solder pasce on mini - min4 for moduliting flut attachment	44	May 3, 2008			
U139: RealTek LAN	Change IPN to E1115-001. Changes part from RTL8111B to RTL8111C.	26	May 7, 2008			
R24: 22 ohm resistor	In series with PROCHOT signal to be consistent with reference designs	6	May 16, 2008			
R608-R610,R617-R619: 56 ohm resistor	Change XDP resistors from 62 ohm to 56 ohm	8	May 16, 2008			
73,R94: 1K resistors	Removed R94 and moved R73 after diode	15	May 16, 2008			
PM RTC power	Placed TPM power on BAT_D vs RTC to avoid losing power when CMOS is cleared	25	May 16, 2008			
2, Q3: SMB FETs	3: SMB FETs Changed from +V3.3S rail to +V5S rail to avoid Vgs drop					
613: 0.002 OHM Res	Moved to other side of 22uF cap, power entire LAN chip through this res	26	May 16, 2008			
R614: 0.002 OHM Res	Power all +V1.2_LAN through this resistor	26	May 16, 2008			
Back Panel USB	Was connected to +V3.3S, now connected to +5VDUAL	29	May 16, 2008			
LL USB PORTS	Was connected to +V5A, now connected to +5VDUAL	29	May 16, 2008			
5VDUAL	Created +5VDUAL rail for USB	32	May 16, 2008			
EDs	Swapped LED / res placement to allow easier voltage probing	32	May 16, 2008			
339: 0 Ohm res	+V15A not used, resistor removed	32	May 16, 2008			
383,R438: 0 Ohm res	Was NI, not used	37	May 16, 2008			
v_3v_pwrgood	Connected to PM_RSMRST#_ICH. Was missing.	17	May 16, 2008			
4_ICH_PWROK and DELAY_PWR_GOOD	Connected together.	17	May 16, 2008			
.28: 10K resistor	Changed to NI. 10K pulldown also has 10K pullup, so one not required	17	May 16, 2008			
58: RAPC722	Swapped pins 1 and 2	33	May 16, 2008			
513,C616: 0.22uF caps	Changed from NI to stuffed due to issue with HP 12V power supply	33	May 16, 2008			
12: FET	Changed from N-channel to P-channel due to Vgs voltage droop	32	May 16, 2008			
1: XDP Connector	Corrected symbol (TMS and TCK swapped)	08	May 16, 2008			
20: 4.8uH inductor	Changed out to 0805 from 0603	09	May 19, 2008			
52: +5VA_PS2> +5VDUAL_PS2	5V PS2 changed from +V5A to +5VDUAL	30	May 19, 2008			
N7: +5VDUAL> FP_USB_VCC	USB FP Diode network changed from +5VDUAL to associated FP_USB_VCC power for ease in routing	29	May 20, 2008			
114: RealTek EEPROM	Swapped EEDI and EEDO	26	May 20, 2008			
74: ICH GPI012	TCH CDIO12 is now IAM ICOLATE# signal	17,26	Marr 20 2000			
	ICH GPI012 is now LAN_ISOLATE# signal	26	May 20, 2008			
139: LAN_ISOLATE#	LAN_ISOLATE# pulled to +V3.3S instead of +V3.3A so that LAN is isolated in S3 and lower		May 20, 2008			
N1: +V5S_VGA	Diode network connected to +5VS_VGA instead of +5VS to prevent back driving +V5S line	22	May 20, 2008			
AN: +V3.3A	3.3V LAN changed from LDO to switching Vreg	26	May 27, 2008			
J67: MagJack	Center tap pins 5&6 moved from +V3.3_LAN to LAN_VCT	26	May 28, 2008			
SIO	Added 511 ohm resistors in series with voltage sources	31	May 28, 2008			
SIO	Added thermal diode	32	May 28, 2008			

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