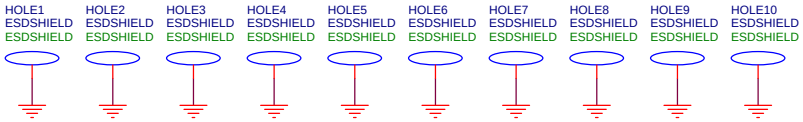
RK3328 BOX Ref

Content Indexing



Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

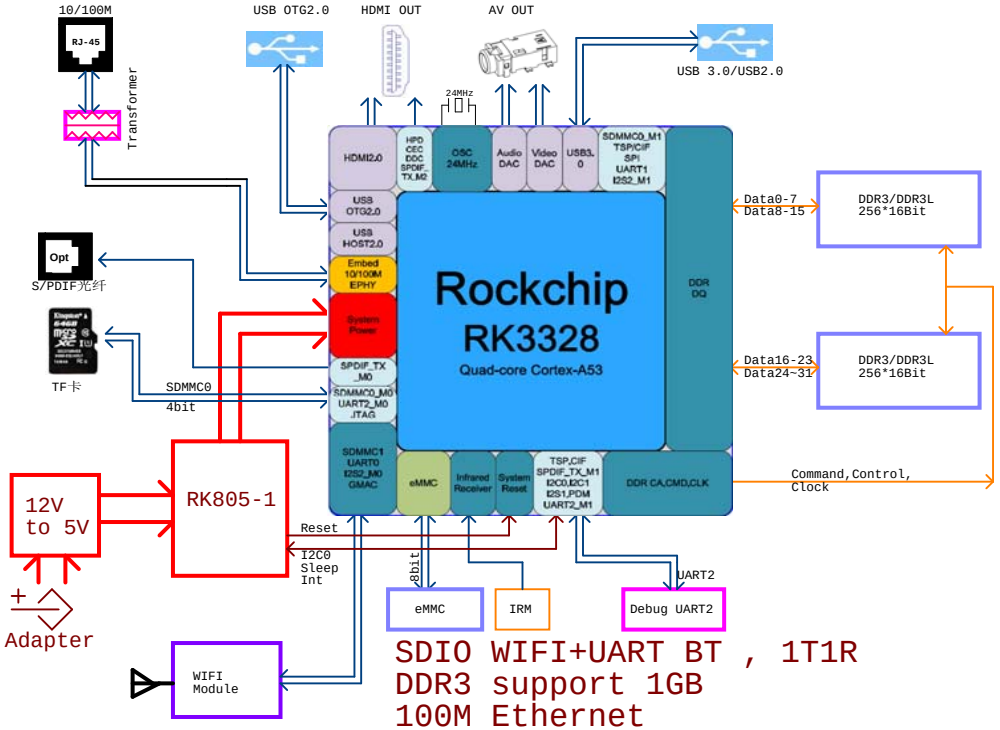
{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Note:
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Ref		
File:	Index		
Date:	Tuesday, August 01, 2017	Rev:	V1.1
Designed by:	Zhangdz	Sheet:	1 of 31

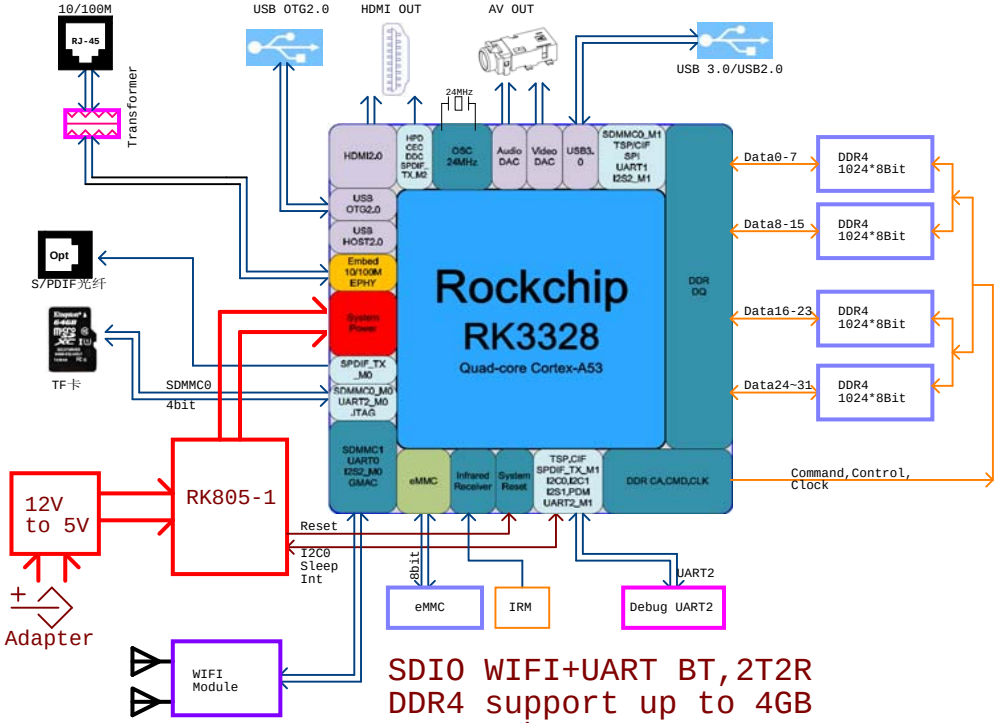
Version	Date	Author	Change Note	Approved
V1.0	20170224	ZDZ	First edictor	
V1.1	20170711	ZDZ	Change History Please Refer : RK3328_BOX_REF_V11_SCH_Modify_Notes	

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Ref		
File:	Change List		
Date:	Monday, July 31, 2017	Rev:	V1.1
Designed by:	Zhangdz	Sheet:	2 of 31



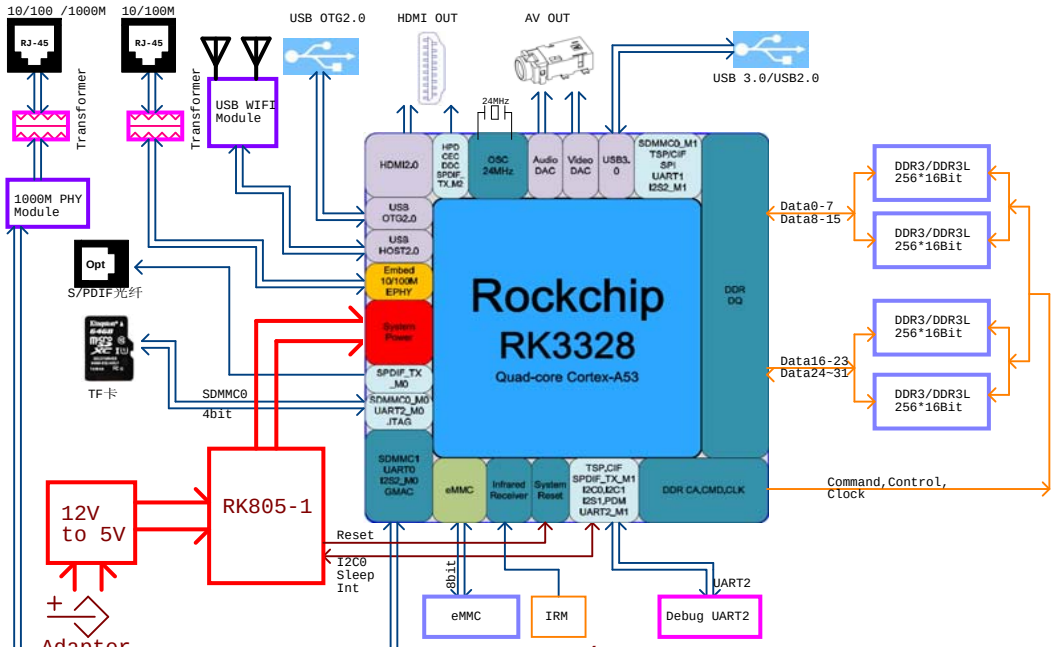
SDIO WIFI+UART BT , 1T1R
DDR3 support 1GB
100M Ethernet

Default config



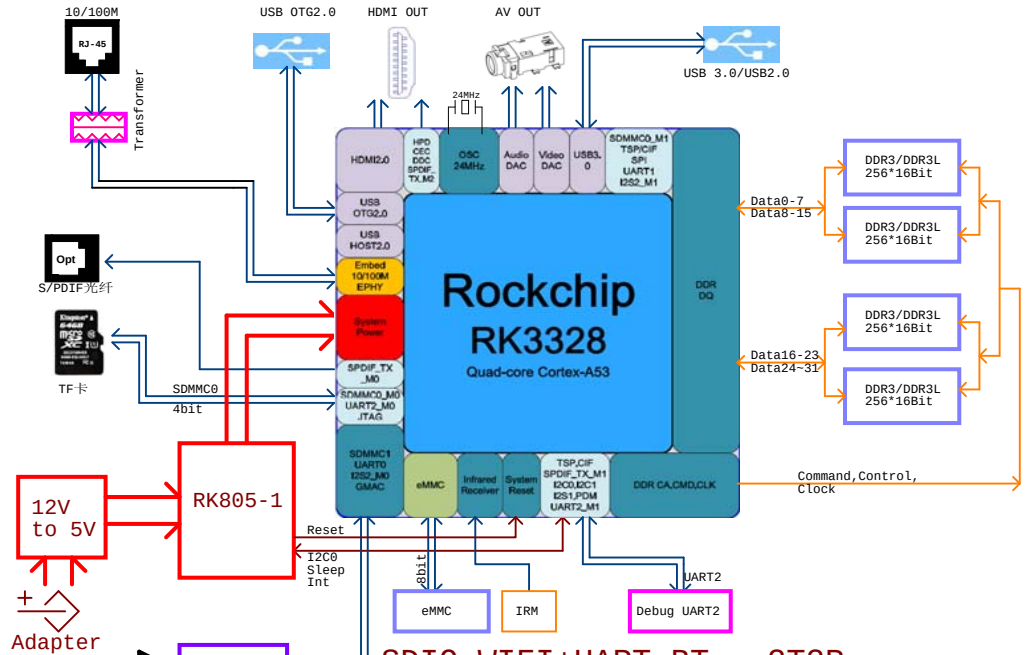
SDIO WIFI+UART BT,2T2R
DDR4 support up to 4GB
100M Ethernet

Config4



USB WIFI/BT ,
DDR3 support up to 2GB
100M+1000M Ethernet

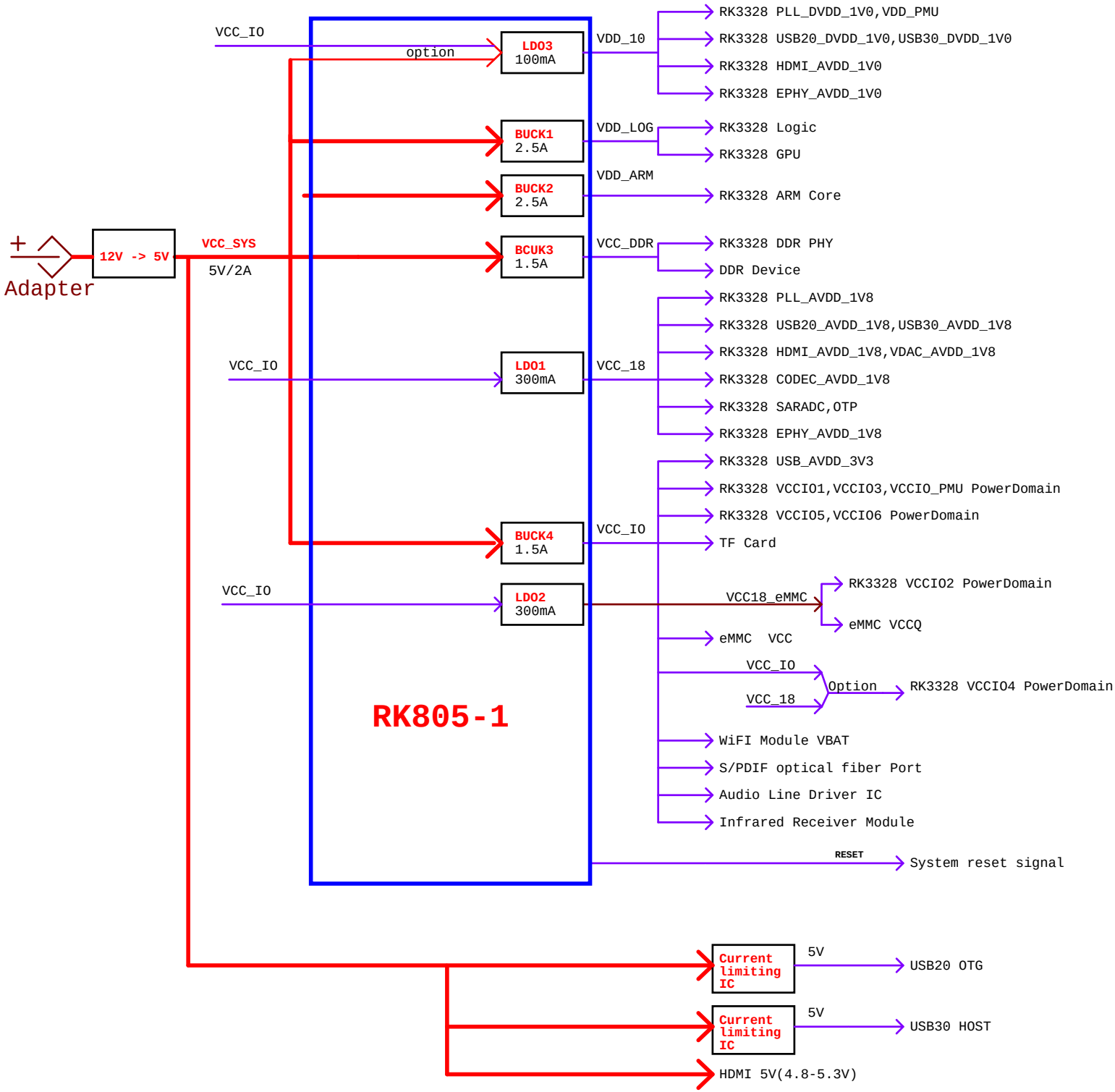
Config2



SDIO WIFI+UART BT , 2T2R
DDR3 support up to 2GB
100M Ethernet

Config3

Rockchip	Fuzhou Rockchip Electronics
Project:	RK3328_BOX_Ref
File:	Block Diagram
Date:	Monday, July 31, 2017
Designed by:	Zhengh
Rev:	V1.1
Sheet:	3 of 31

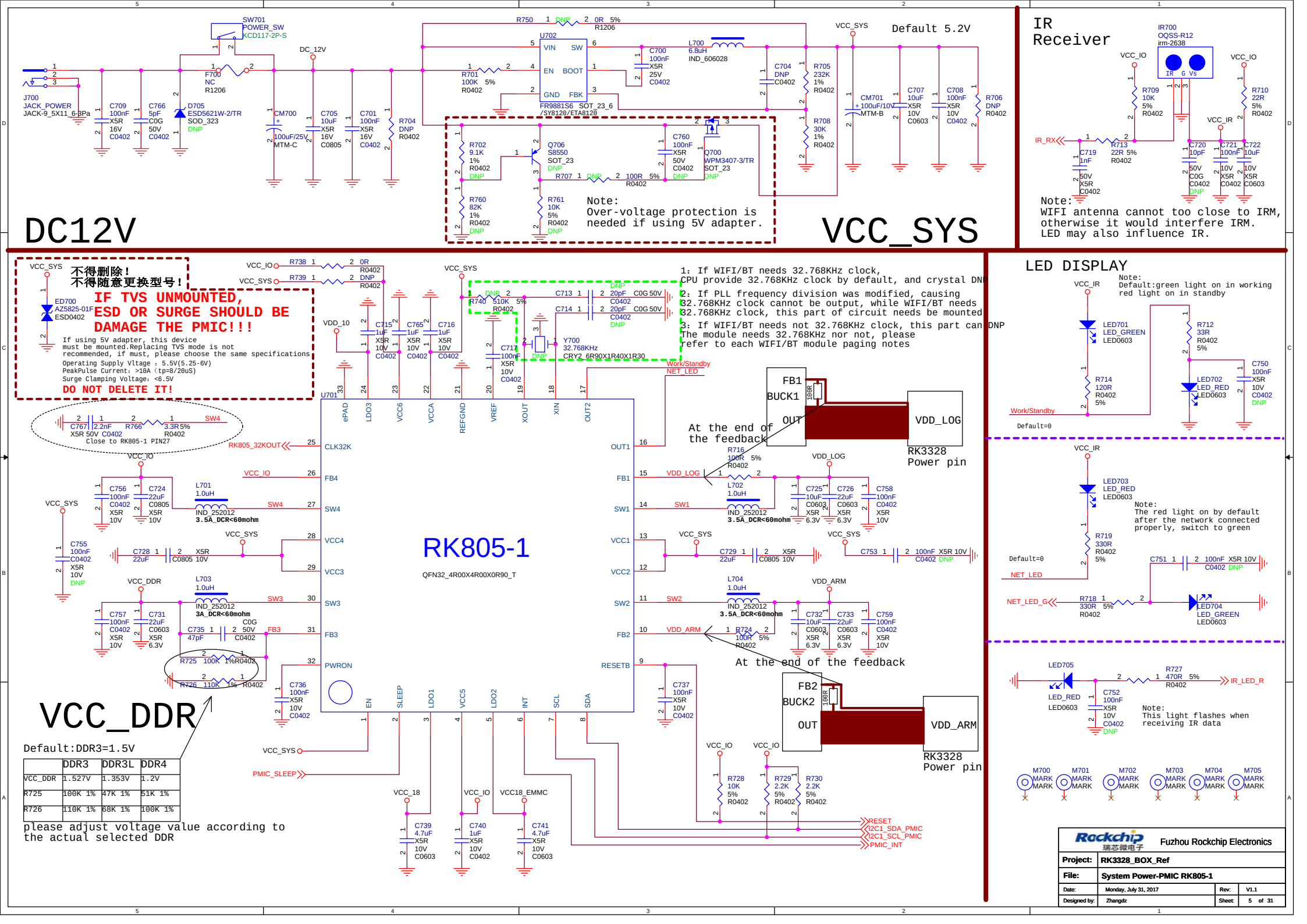


Power Timing

TYPE	VOLT	STEP	PowerName
BUCK1	1.1V		VDD_LOG
BUCK2	1.1V		VDD_ARM
BUCK3	FB=0.8V		VCC_DDR
BUCK4	3.3V		VCC_IO
LDO1	1.8V		VCC_18
LDO2	1.8V		VCC18_eMMC
LDO3	1.0V		VDD_10

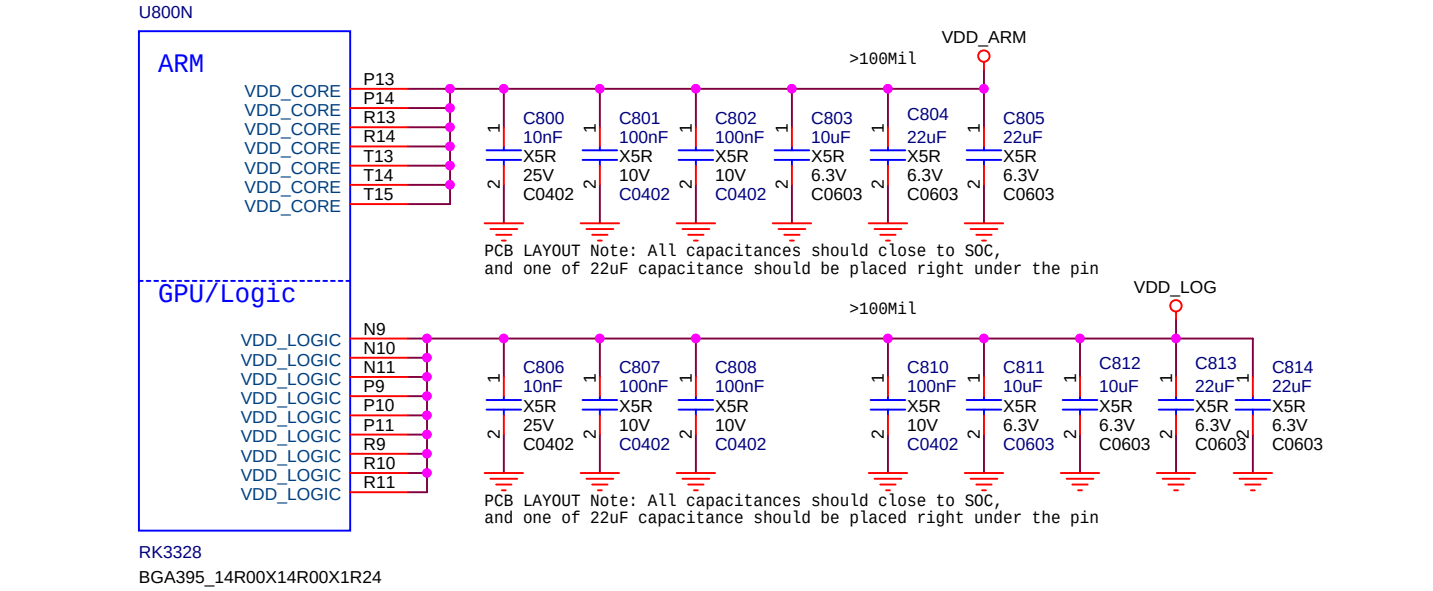
IO Domain Voltage	IO Voltage=3.3V	IO Voltage=1.8V
VCCIO_PMU	3.3V	Not Support
VCCIO1	3.3V	Not Support
VCCIO2		1.8V（Default） eMMC
VCCIO3	3.3V（Default）	
VCCIO4	3.3V（Default） WIFI:RTL8723BS	
VCCIO5	3.3V（Default）	
VCCIO6	3.3V（Default）	

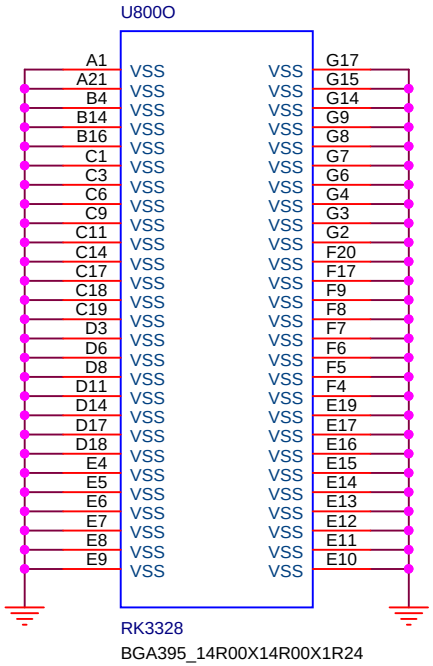
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics	
Project:	RK3328_BOX_Ref	
File:	Power tree-RK805-1	
Date:	Wednesday, August 16, 2017	Rev: V1.1
Designed by:	Zhangqb	Sheet: 4 of 31

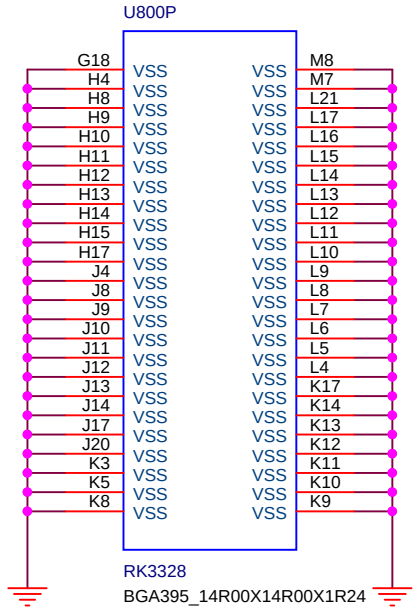


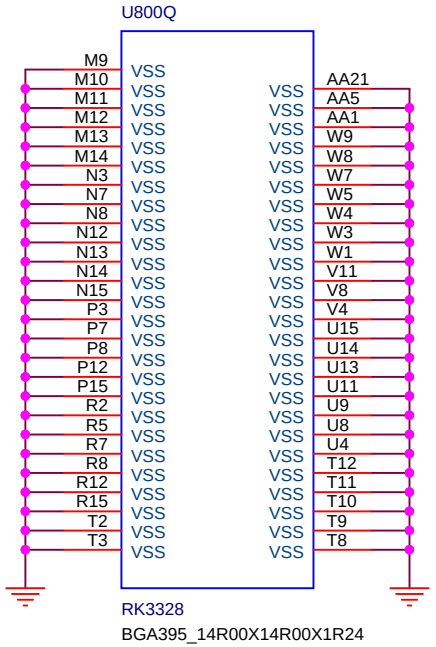
	DDR3	DDR3L	DDR4
VCC_DDR	1.527V	1.353V	1.2V
R725	100K 1%	47K 1%	51K 1%
R726	110K 1%	68K 1%	100K 1%

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics
Project:	RK3328_BOX_Ref
File:	System Power-PMIC RK805-1
Date: Monday, July 31, 2017	Rev: V1.1
Designed by: Zhangdz	Sheet: 5 of 31

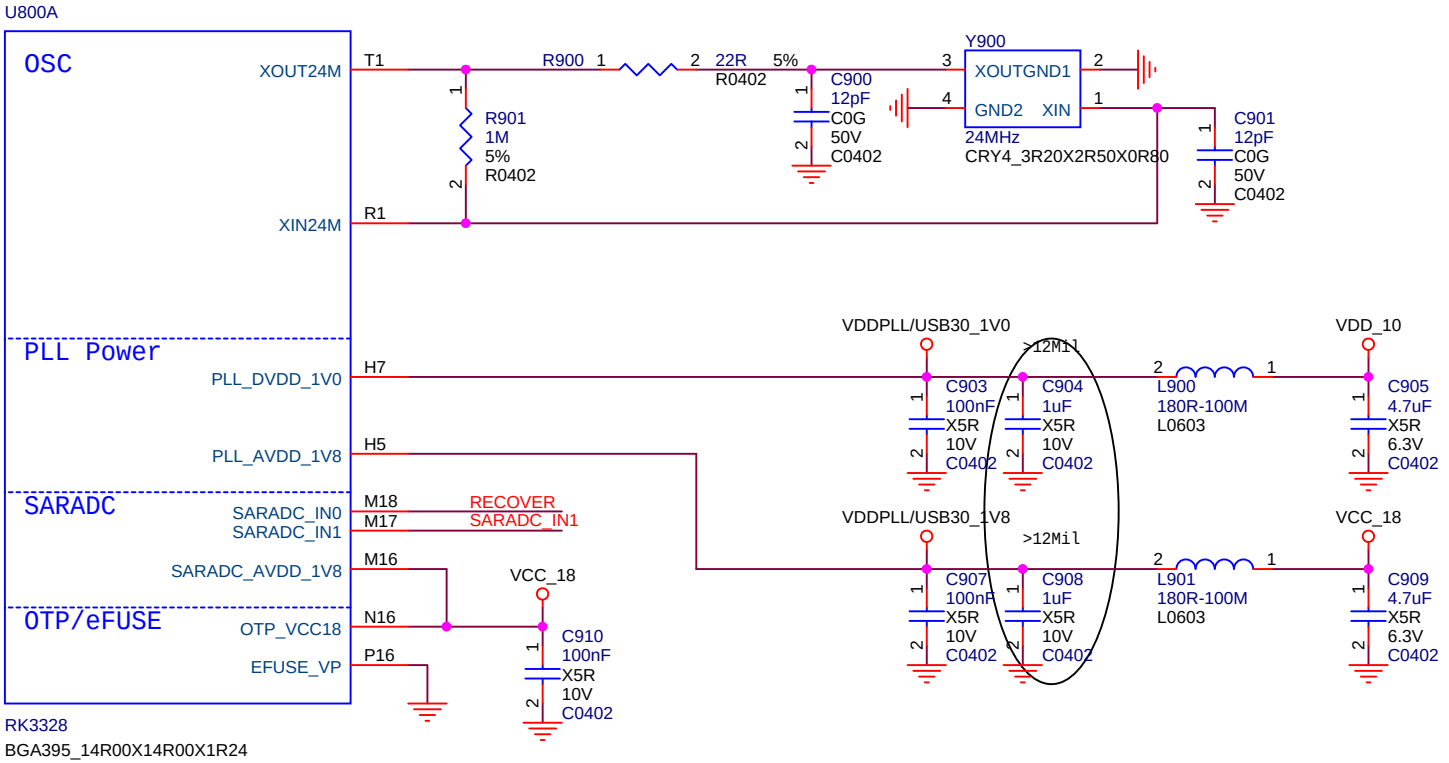


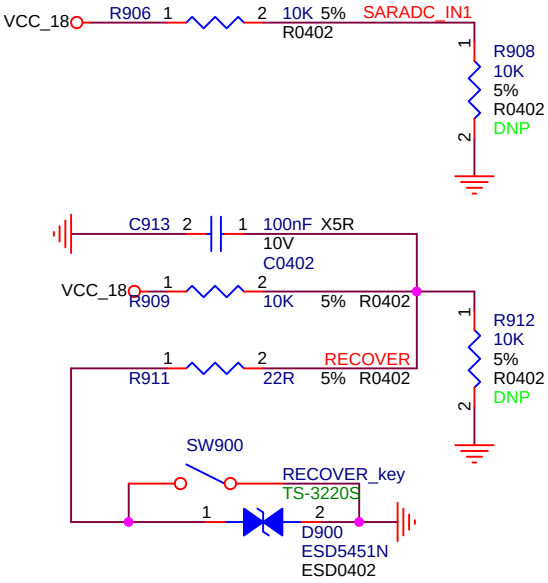






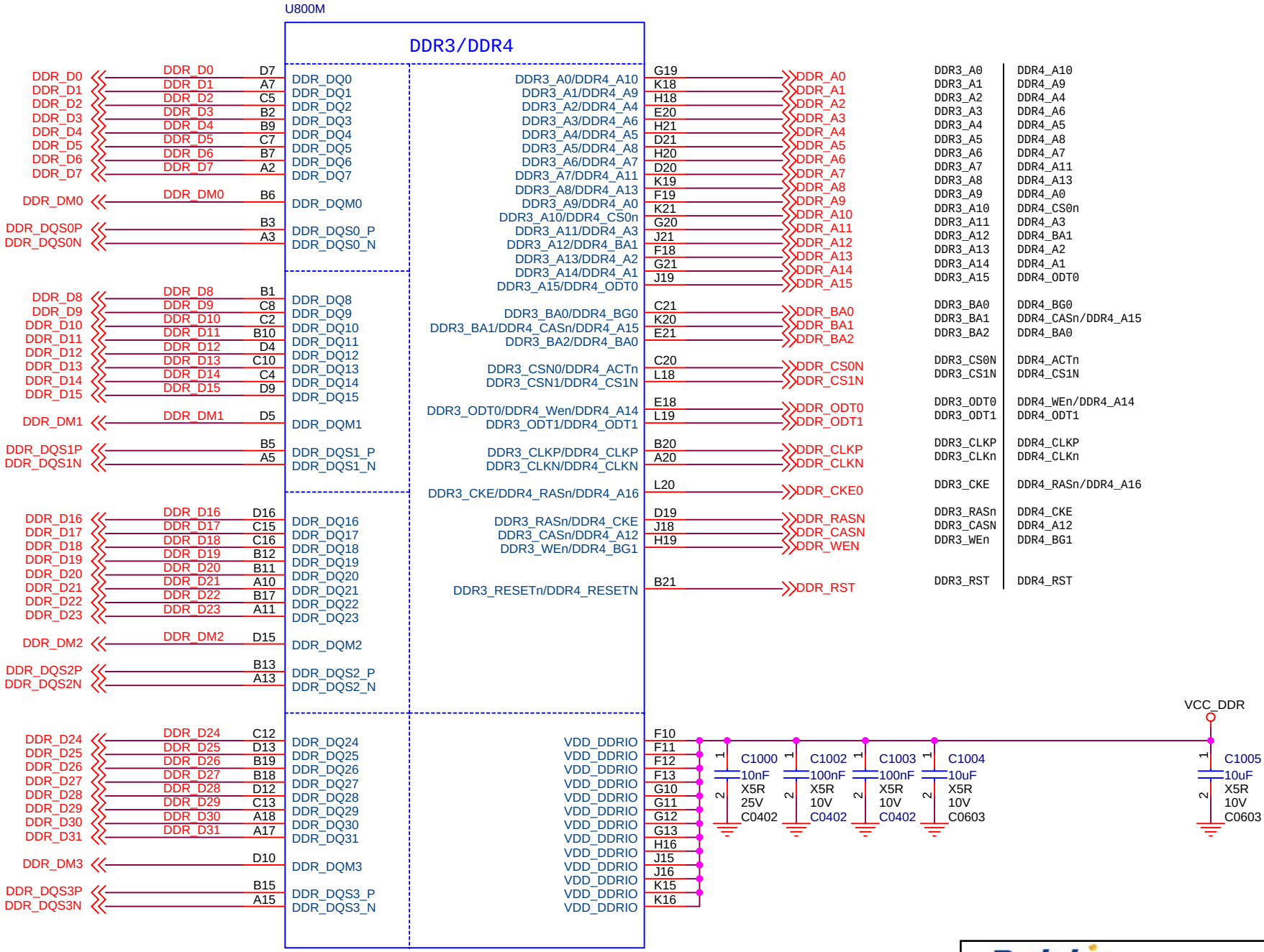
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	**RK3328_BOX_Ref**		
File:	**RK3328 Power**		
Date:	Monday, July 31, 2017	Rev:	V1.1
Designed by:	Zhangdz	Sheet:	6 of 31



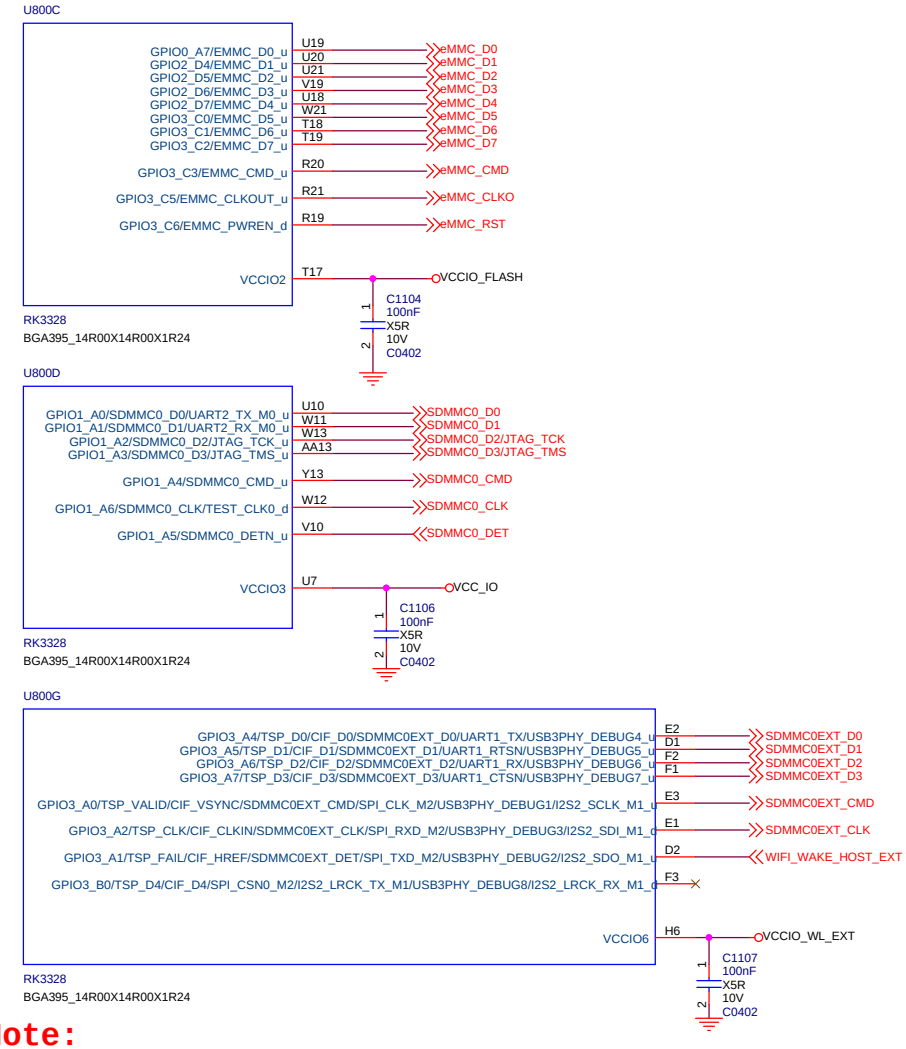


SARADC_IN0	SARADC_IN1	Up Resistance	Down Resistance	
Recover		DNP	10K	
BOM1		110K	10K	
BOM2		100K	20K	
BOM3		100K	33K	
BOM4		36K	18K	
BOM5		51K	36K	
BOM6		51K	51K	
BOM7		36K	51K	
BOM8		18K	36K	
BOM9		33K	100K	
BOM10		20K	100K	
BOM11		10K	110K	
BOM12		10K	DNP	

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Ref		
File:	RK3328 OSC/PLL/OTP/SARADC		
Date:	Monday, July 31, 2017	Rev:	V1.1
Designed by:	Zhangdz	Sheet:	7 of 31



Fuzhou Rockchip Electronics			
Project:	RK3328_BOX_Ref		
File:	RK3328 DDR Controler		
Date:	Tuesday, August 01, 2017	Rev:	V1.1
Designed by:	Zhangdz	Sheet:	8 of 31




```
SDMMC0_D0           ---------------------  SD_D0
SDMMC0_D1           ---------------------  SD_D1
SDMMC0_D2/JTAG_TCK  ---------------------  SD_D2
SDMMC0_D3/JTAG_TMS  ---------------------  SD_D3
SDMMC0_CMD          ---------------------  SD_CMD
SDMMC0_CLK          ---------------------  SD_CLK
SDMMC0_DET          ---------------------  SD_DET
VCCIO3              ---------------------  VCC_IO

SDMMC0EXT_D0        ---------------------  WIFI_D0_EXT
SDMMC0EXT_D1        ---------------------  WIFI_D1_EXT
SDMMC0EXT_D2        ---------------------  WIFI_D2_EXT
SDMMC0EXT_D3        ---------------------  WIFI_D3_EXT
SDMMC0EXT_CMD       ---------------------  WIFI_CMD_EXT
SDMMC0EXT_CLK       ---------------------  WIFI_CLK_EXT
GPIO3_A1            ---------------------  WIFI_WAKE_HOST_EXT
VCCIO6              ---------------------  VCCIO_WL_EXT
```

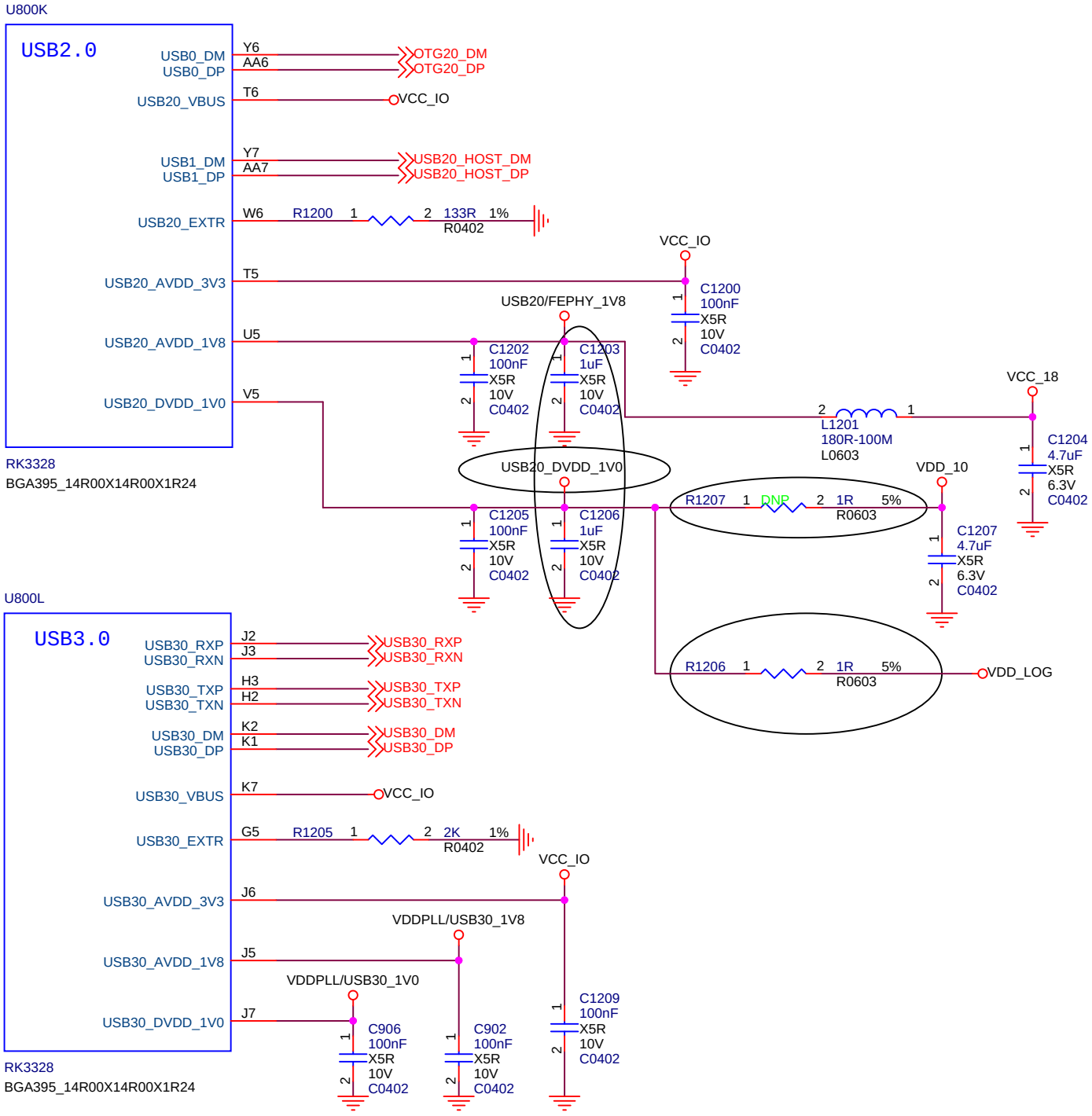
```
SDMMC0_D0           ---------------------  WIFI_D0_EXT
SDMMC0_D1           ---------------------  WIFI_D1_EXT
SDMMC0_D2/JTAG_TCK  ---------------------  WIFI_D2_EXT
SDMMC0_D3/JTAG_TMS  ---------------------  WIFI_D3_EXT
SDMMC0_CMD          ---------------------  WIFI_CMD_EXT
SDMMC0_CLK          ---------------------  WIFI_CLK_EXT
SDMMC0_DET          ---------------------  WIFI_WAKE_HOST_EXT
VCCIO3              ---------------------  VCCIO_WL_EXT

SDMMC0EXT_D0        ---------------------  SD_D0
SDMMC0EXT_D1        ---------------------  SD_D1
SDMMC0EXT_D2        ---------------------  SD_D2
SDMMC0EXT_D3        ---------------------  SD_D3
SDMMC0EXT_CMD       ---------------------  SD_CMD
SDMMC0EXT_CLK       ---------------------  SD_CLK
SDMMC0EXT_DET       ---------------------  SD_DET
VCCIO6              ---------------------  VCC_IO
```

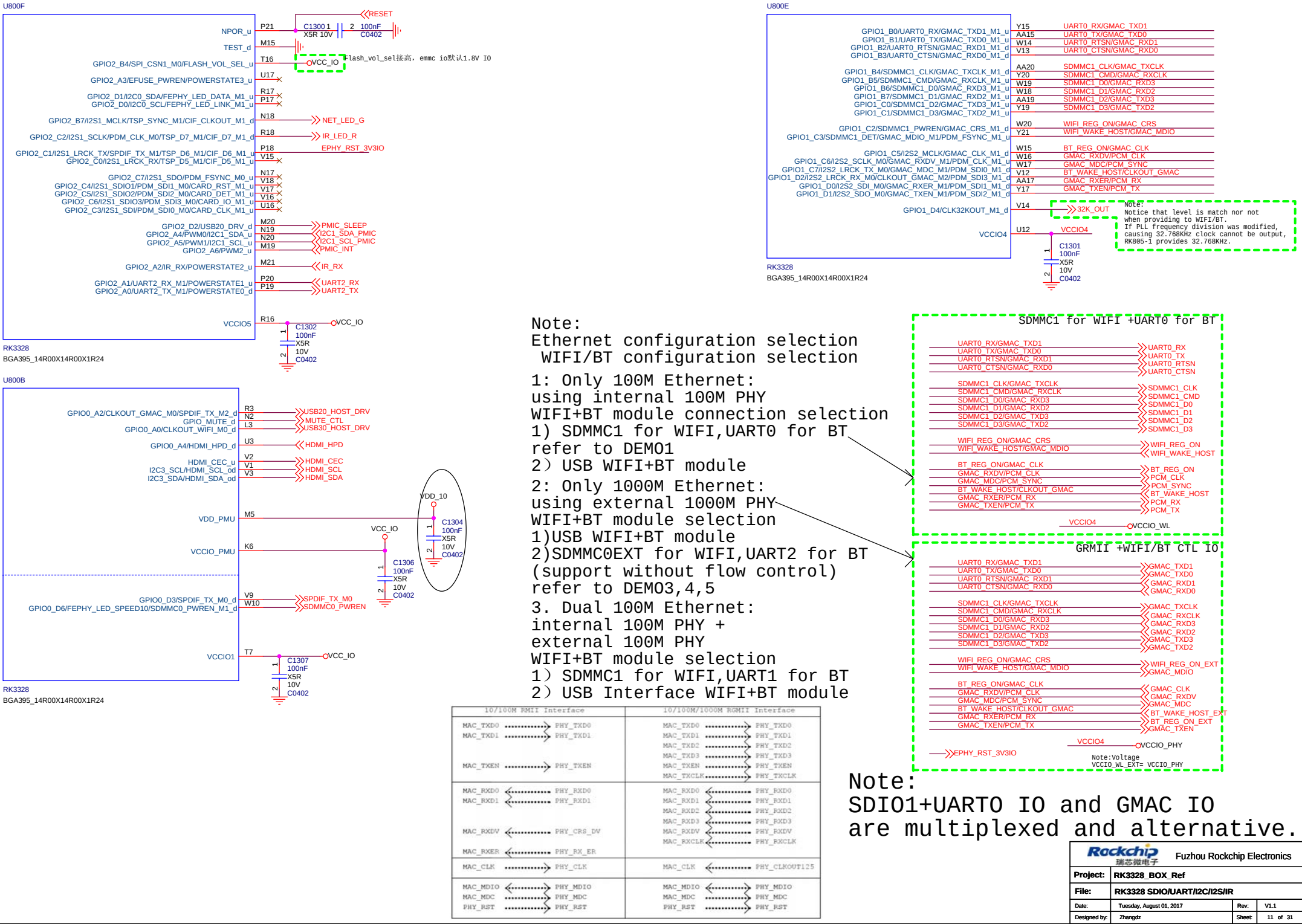
Note:
SDMMC0 support SD Boot, Max 150MHz
SDMMC0EXT does not support SD Boot, Max 100MHz

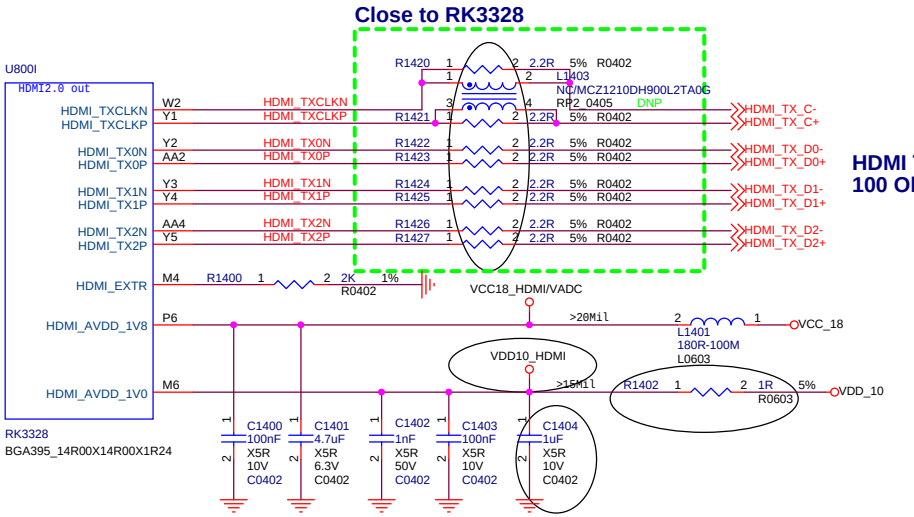
In gigabit Ethernet requirements:
If requiring high performance WIFI, WIFI SDIO connects to SDMMC0 port, causing without supporting SD Boot
And SDMMC0EXT connects to SD Card

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Ref		
File:	RK3328 eMMC Controler/TF		
Date:	Tuesday, August 01, 2017	Rev:	V1.1
Designed by:	Zhangdz	Sheet:	9 of 31



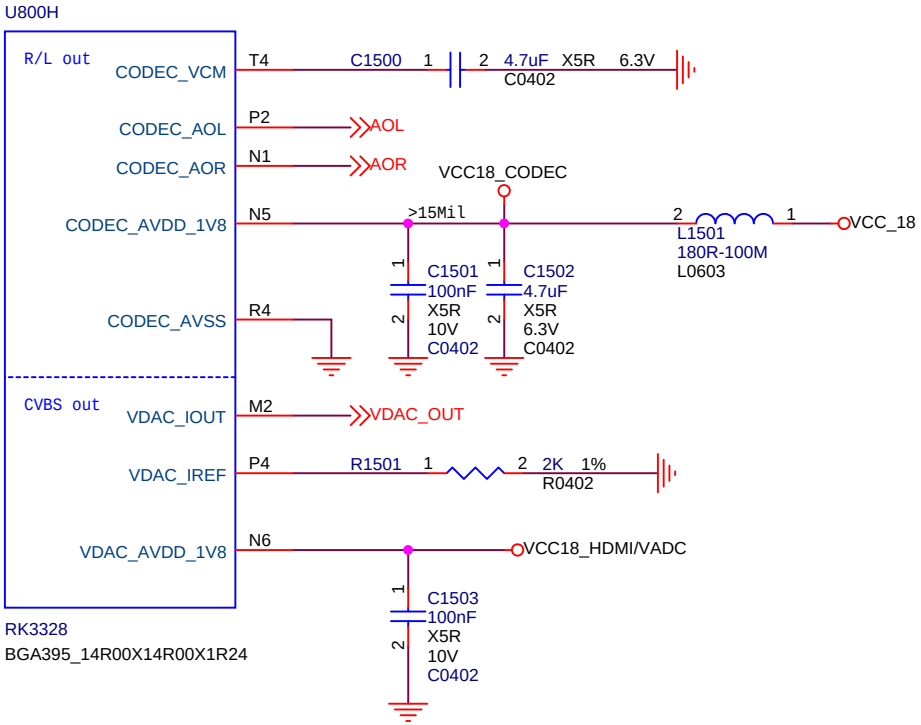
Fuzhou Rockchip Electronics			
Project:	RK3328_BOX_Ref		
File:	RK3328 USB2 PHY/USB3 PHY		
Date:	Tuesday, July 18, 2017	Rev:	V1.1
Designed by:	Zhangdz	Sheet:	10 of 31


U800F
NPOR_u
TEST_d
GPIO2_B4/SPI_CSN1_M0/FLASH_VOL_SEL_u
GPIO2_A3/EFUSE_PWREN/POWERSTATE3_u
GPIO2_D1/I2C0_SDA/FEPHY_LED_DATA_M1_u
GPIO2_D0/I2C0_SCL/FEPHY_LED_LINK_M1_u
GPIO2_B7/I2S1_MCLK/TSP_SYNC_M1/CIF_CLKOUT_M1_d
GPIO2_C2/I2S1_SCLK/PDM_CLK_M0/TSP_D7_M1/CIF_D7_M1_d
GPIO2_C1/I2S1_LRCK_TX/SPDIF_TX_M1/TSP_D6_M1/CIF_D6_M1_u
GPIO2_C0/I2S1_LRCK_RX/TSP_D5_M1/CIF_D5_M1_u
GPIO2_C7/I2S1_SDO/PDM_FSYNC_M0_u
GPIO2_C4/I2S1_SDIO1/PDM_SDI1_M0/CARD_RST_M1_u
GPIO2_C5/I2S1_SDIO2/PDM_SDI2_M0/CARD_DET_M1_u
GPIO2_C6/I2S1_SDIO3/PDM_SDI3_M0/CARD_IO_M1_u
GPIO2_C3/I2S1_SDI/PDM_SDI0_M0/CARD_CLK_M1_u
GPIO2_D2/USB20_DRV_d
GPIO2_A4/PWM0/I2C1_SDA_u
GPIO2_A5/PWM1/I2C1_SCL_u
GPIO2_A6/PWM2_u
GPIO2_A2/IR_RX/POWERSTATE2_u
GPIO2_A1/UART2_RX_M1/POWERSTATE1_u
GPIO2_A0/UART2_TX_M1/POWERSTATE0_d
VCCIO5
RESET
C1300 1 2 100nF X5R 10V C0402
VCC_IO
flash_vol_sel接高，emmc io默认1.8V IO
NET_LED_G
IR_LED_R
EPHY_RST_3V3IO
PMIC_SLEEP
I2C1_SDA_PMIC
I2C1_SCL_PMIC
PMIC_INT
IR_RX
UART2_RX
UART2_TX
C1302 100nF X5R 10V C0402
RK3328
BGA395_14R00X14R00X1R24
U800B
GPIO0_A2/CLKOUT_GMAC_M0/SPDIF_TX_M2_d
GPIO_MUTE_d
GPIO0_A0/CLKOUT_WIFI_M0_d
GPIO0_A4/HDMI_HPD_d
HDMI_CEC_u
I2C3_SCL/HDMI_SCL_od
I2C3_SDA/HDMI_SDA_od
VDD_PMU
VCCIO_PMU
GPIO0_D3/SPDIF_TX_M0_d
GPIO0_D6/FEPHY_LED_SPEED10/SDMMC0_PWREN_M1_d
VCCIO1
USB20_HOST_DRV
MUTE_CTL
USB30_HOST_DRV
HDMI_HPD
HDMI_CEC
HDMI_SCL
HDMI_SDA
VDD_10
C1304 100nF X5R 10V C0402
C1306 100nF X5R 10V C0402
SPDIF_TX_M0
SDMMC0_PWREN
C1307 100nF X5R 10V C0402
RK3328
BGA395_14R00X14R00X1R24
U800E
GPIO1_B0/UART0_RX/GMAC_TXD1_M1_u
GPIO1_B1/UART0_TX/GMAC_TXD0_M1_u
GPIO1_B2/UART0_RTSN/GMAC_RXD1_M1_d
GPIO1_B3/UART0_CTSN/GMAC_RXD0_M1_d
GPIO1_B4/SDMMC1_CLK/GMAC_TXCLK_M1_d
GPIO1_B5/SDMMC1_CMD/GMAC_RXCLK_M1_u
GPIO1_B6/SDMMC1_D0/GMAC_RXD3_M1_u
GPIO1_B7/SDMMC1_D1/GMAC_RXD2_M1_u
GPIO1_C0/SDMMC1_D2/GMAC_TXD3_M1_u
GPIO1_C1/SDMMC1_D3/GMAC_TXD2_M1_u
GPIO1_C2/SDMMC1_PWREN/GMAC_CRS_M1_d
GPIO1_C3/SDMMC1_DET/GMAC_MDIO_M1/PDM_FSYNC_M1_u
GPIO1_C5/I2S2_MCLK/GMAC_CLK_M1_d
GPIO1_C6/I2S2_SCLK_M0/GMAC_RXDV_M1/PDM_CLK_M1_u
GPIO1_C7/I2S2_LRCK_TX_M0/GMAC_MDC_M1/PDM_SDI0_M1_d
GPIO1_D2/I2S2_LRCK_RX_M0/CLKOUT_GMAC_M2/PDM_SDI3_M1_d
GPIO1_D0/I2S2_SDI_M0/GMAC_RXER_M1/PDM_SDI1_M1_d
GPIO1_D1/I2S2_SDO_M0/GMAC_TXEN_M1/PDM_SDI2_M1_d
GPIO1_D4/CLK32KOUT_M1_d
VCCIO4
UART0_RX/GMAC_TXD1
UART0_TX/GMAC_TXD0
UART0_RTSN/GMAC_RXD1
UART0_CTSN/GMAC_RXD0
SDMMC1_CLK/GMAC_TXCLK
SDMMC1_CMD/GMAC_RXCLK
SDMMC1_D0/GMAC_RXD3
SDMMC1_D1/GMAC_RXD2
SDMMC1_D2/GMAC_TXD3
SDMMC1_D3/GMAC_TXD2
WIFI_REG_ON/GMAC_CRS
WIFI_WAKE_HOST/GMAC_MDIO
BT_REG_ON/GMAC_CLK
GMAC_RXDV/PCM_CLK
GMAC_MDC/PCM_SYNC
BT_WAKE_HOST/CLKOUT_GMAC
GMAC_RXER/PCM_RX
GMAC_TXEN/PCM_TX
32K_OUT
Note:
Notice that level is match nor not when providing to WIFI/BT.
If PLL frequency division was modified, causing 32.768KHz clock cannot be output, RK805-1 provides 32.768KHz.
C1301 100nF X5R 10V C0402
RK3328
BGA395_14R00X14R00X1R24
Note:
Ethernet configuration selection
WIFI/BT configuration selection
1: Only 100M Ethernet:
using internal 100M PHY
WIFI+BT module connection selection
1) SDMMC1 for WIFI,UART0 for BT
refer to DEMO1
2) USB WIFI+BT module
2: Only 1000M Ethernet:
using external 1000M PHY
WIFI+BT module selection
1)USB WIFI+BT module
2)SDMMC0EXT for WIFI,UART2 for BT
(support without flow control)
refer to DEMO3,4,5
3. Dual 100M Ethernet:
internal 100M PHY +
external 100M PHY
WIFI+BT module selection
1) SDMMC1 for WIFI,UART1 for BT
2) USB Interface WIFI+BT module
SDMMC1 for WIFI +UART0 for BT
UART0_RX
UART0_TX
UART0_RTSN
UART0_CTSN
SDMMC1_CLK
SDMMC1_CMD
SDMMC1_D0
SDMMC1_D1
SDMMC1_D2
SDMMC1_D3
WIFI_REG_ON
WIFI_WAKE_HOST
BT_REG_ON
PCM_CLK
PCM_SYNC
BT_WAKE_HOST
PCM_RX
PCM_TX
VCCIO4
VCCIO_WL
GRMII +WIFI/BT CTL IO
GMAC_TXD1
GMAC_TXD0
GMAC_RXD1
GMAC_RXD0
GMAC_TXCLK
GMAC_RXCLK
GMAC_RXD3
GMAC_RXD2
GMAC_TXD3
GMAC_TXD2
WIFI_REG_ON_EXT
GMAC_MDIO
GMAC_CLK
GMAC_RXDV
GMAC_MDC
BT_WAKE_HOST_EXT
BT_REG_ON_EXT
GMAC_TXEN
VCCIO4
VCCIO_PHY
EPHY_RST_3V3IO
Note:Voltage
VCCIO_WL_EXT= VCCIO_PHY
10/100M RMII Interface
10/100M/1000M RGMII Interface
MAC_TXD0
MAC_TXD1
MAC_TXEN
MAC_RXD0
MAC_RXD1
MAC_RXDV
MAC_RXER
MAC_CLK
MAC_MDIO
MAC_MDC
PHY_RST
PHY_TXD0
PHY_TXD1
PHY_TXD2
PHY_TXD3
PHY_TXEN
PHY_TXCLK
PHY_RXD0
PHY_RXD1
PHY_RXD2
PHY_RXD3
PHY_RXDV
PHY_RXCLK
PHY_CRS_DV
PHY_RX_ER
PHY_CLK
PHY_CLKOUT125
PHY_MDIO
PHY_MDC
PHY_RST
Note:
SDIO1+UARTO IO and GMAC IO
are multiplexed and alternative.
Rockchip 瑞芯微电子
Fuzhou Rockchip Electronics
Project: RK3328_BOX_Ref
File: RK3328 SDIO/UART/I2C/I2S/IR
Date: Tuesday, August 01, 2017
Rev: V1.1
Designed by: Zhangdz
Sheet: 11 of 31

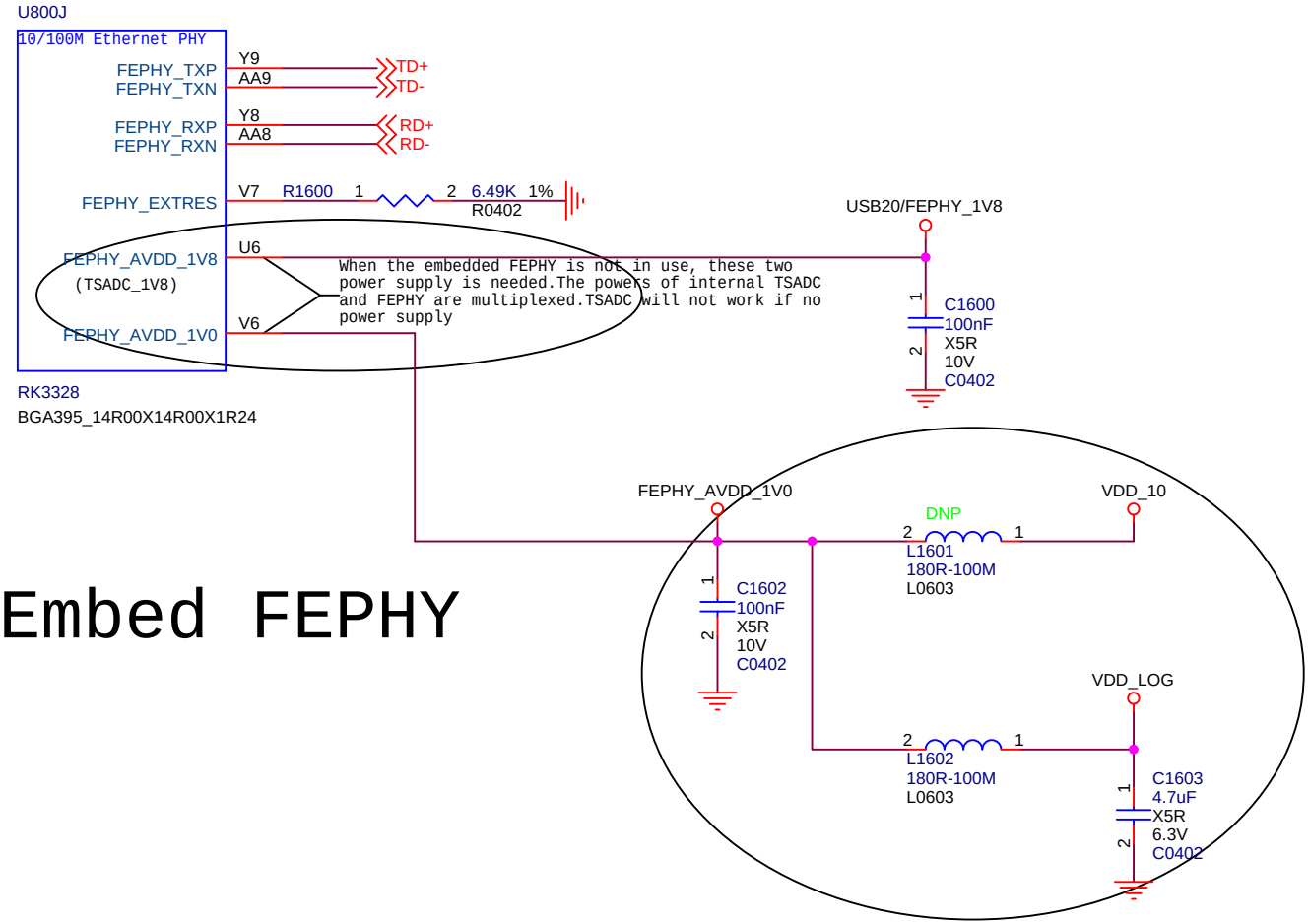


HDMI TMDS trace
100 Ohm +-10%

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Ref		
File:	RK3328 HDMI PHY		
Date:	Wednesday, July 26, 2017	Rev:	V1.1
Designed by:	Zhangdz	Sheet:	12 of 31

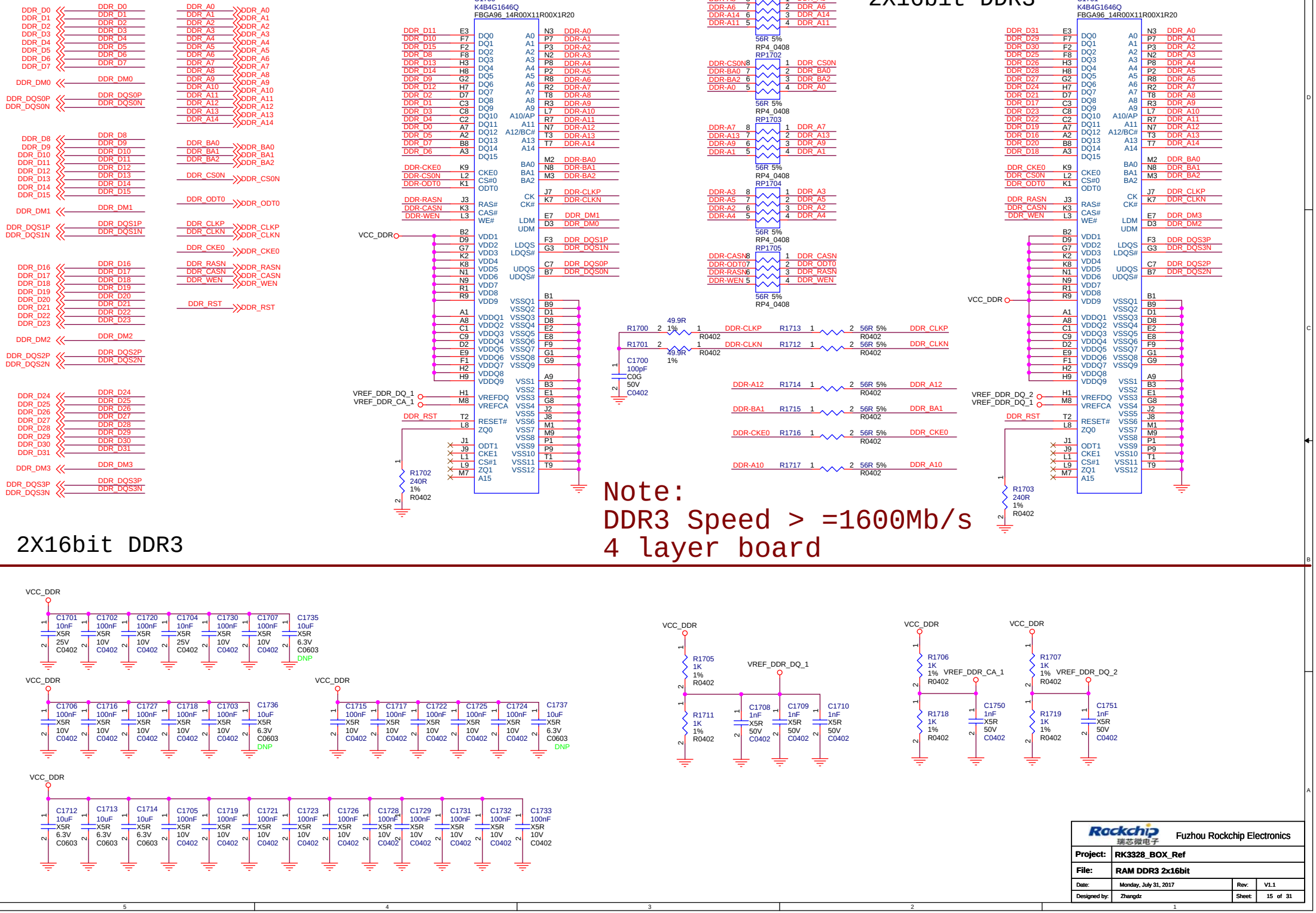


Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Ref		
File:	RK3328 AV Interface		
Date:	Tuesday, July 18, 2017	Rev:	V1.1
Designed by:	Zhangdz	Sheet:	13 of 31



Embed FEPHY

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Ref		
File:	RK3328 FEPHY		
Date:	Tuesday, August 01, 2017	Rev:	V1.1
Designed by:	Zhangdz	Sheet:	14 of 31


2X16bit DDR3
U1700
K4B4G1646Q
FBGA96_14R00X11R00X1R20
U1701
K4B4G1646Q
FBGA96_14R00X11R00X1R20
RP1701
RP1702
RP1703
RP1704
RP1705
RP4_0408
56R 5%
R1700
R1701
49.9R 1%
R0402
C1700
100pF
C0G
50V
C0402
R1702
240R
1%
R0402
R1703
240R
1%
R0402
VCC_DDR
VREF_DDR_DQ_1
VREF_DDR_CA_1
VREF_DDR_DQ_2
DDR_RST
Note:
DDR3 Speed > =1600Mb/s
4 layer board
2X16bit DDR3
C1701 10nF X5R 25V C0402
C1702 100nF X5R 10V C0402
C1720 100nF X5R 10V C0402
C1704 10nF X5R 25V C0402
C1730 100nF X5R 10V C0402
C1707 100nF X5R 10V C0402
C1735 10uF X5R 6.3V C0603 DNP
C1706 100nF X5R 10V C0402
C1716 100nF X5R 10V C0402
C1727 100nF X5R 10V C0402
C1718 100nF X5R 10V C0402
C1703 100nF X5R 10V C0402
C1736 10uF X5R 6.3V C0603 DNP
C1715 100nF X5R 10V C0402
C1717 100nF X5R 10V C0402
C1722 100nF X5R 10V C0402
C1725 100nF X5R 10V C0402
C1724 100nF X5R 10V C0402
C1737 10uF X5R 6.3V C0603 DNP
C1712 10uF X5R 6.3V C0603
C1713 10uF X5R 6.3V C0603
C1714 10uF X5R 6.3V C0603
C1705 100nF X5R 10V C0402
C1719 100nF X5R 10V C0402
C1721 100nF X5R 10V C0402
C1723 100nF X5R 10V C0402
C1726 100nF X5R 10V C0402
C1728 100nF X5R 10V C0402
C1729 100nF X5R 10V C0402
C1731 100nF X5R 10V C0402
C1732 100nF X5R 10V C0402
C1733 100nF X5R 10V C0402
R1705 1K 1% R0402
R1711 1K 1% R0402
C1708 1nF X5R 50V C0402
C1709 1nF X5R 50V C0402
C1710 1nF X5R 50V C0402
R1706 1K 1% R0402
R1718 1K 1% R0402
C1750 1nF X5R 50V C0402
R1707 1K 1% R0402
R1719 1K 1% R0402
C1751 1nF X5R 50V C0402
Rockchip 瑞芯微电子
Fuzhou Rockchip Electronics
Project: RK3328_BOX_Ref
File: RAM DDR3 2x16bit
Date: Monday, July 31, 2017
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Designed by: Zhangdz
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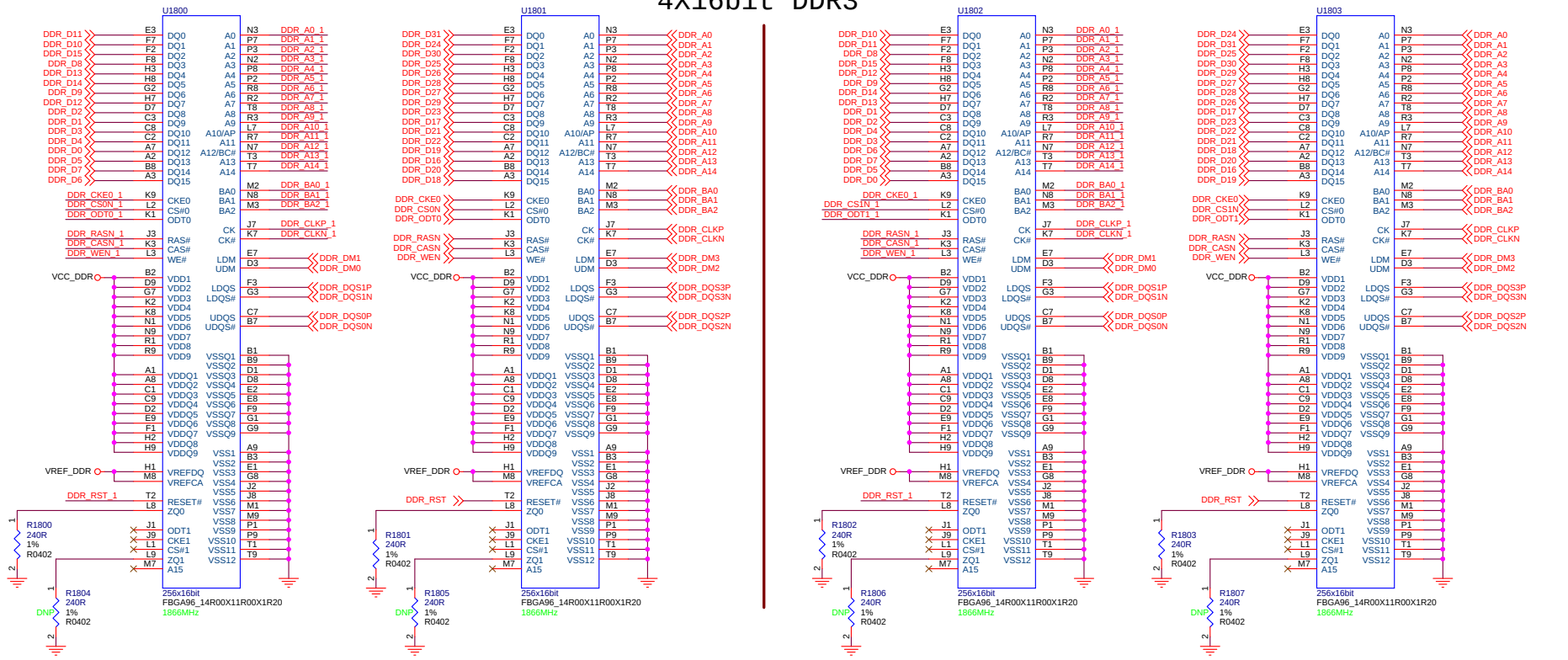
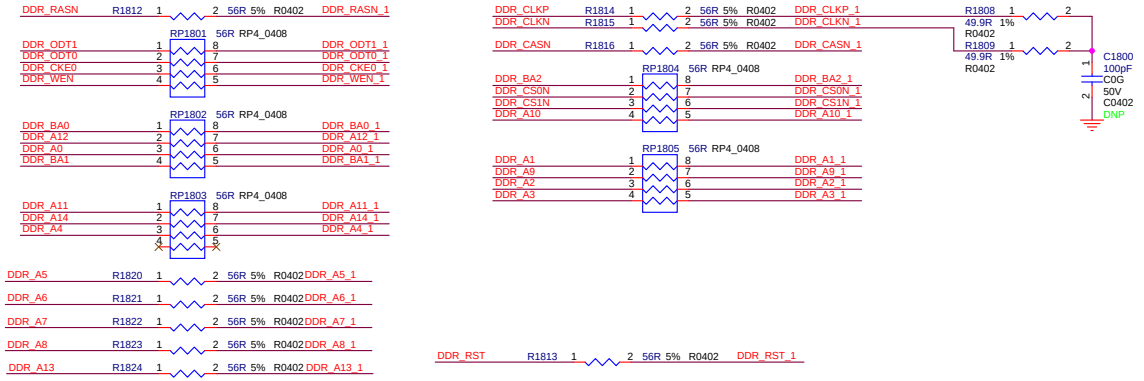
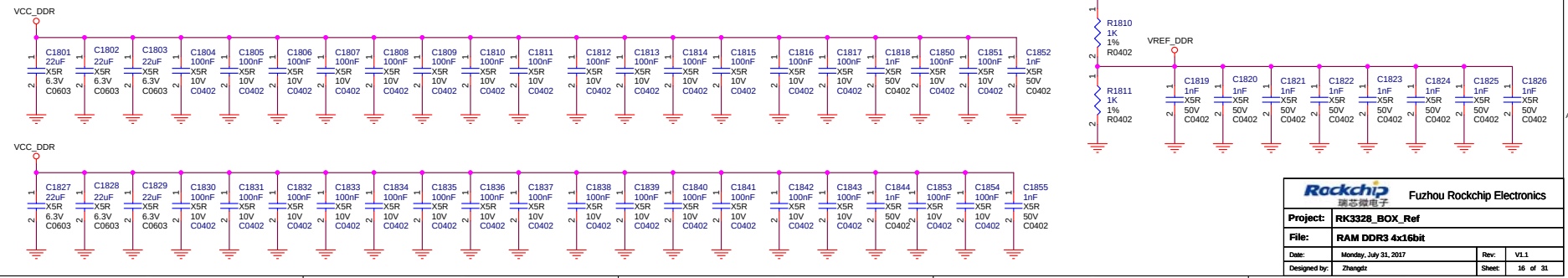
4X16bit DDR3





Note:
DDR3 Speed > =1600Mb/s
4 layer board

DDR3 FILTER



Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics
Project:	RK3328_BOX_Ref
File:	RAM DDR3 4x16bit
Date:	Monday, July 31, 2017
Rev:	V1.1
Designed by:	Zhangdz
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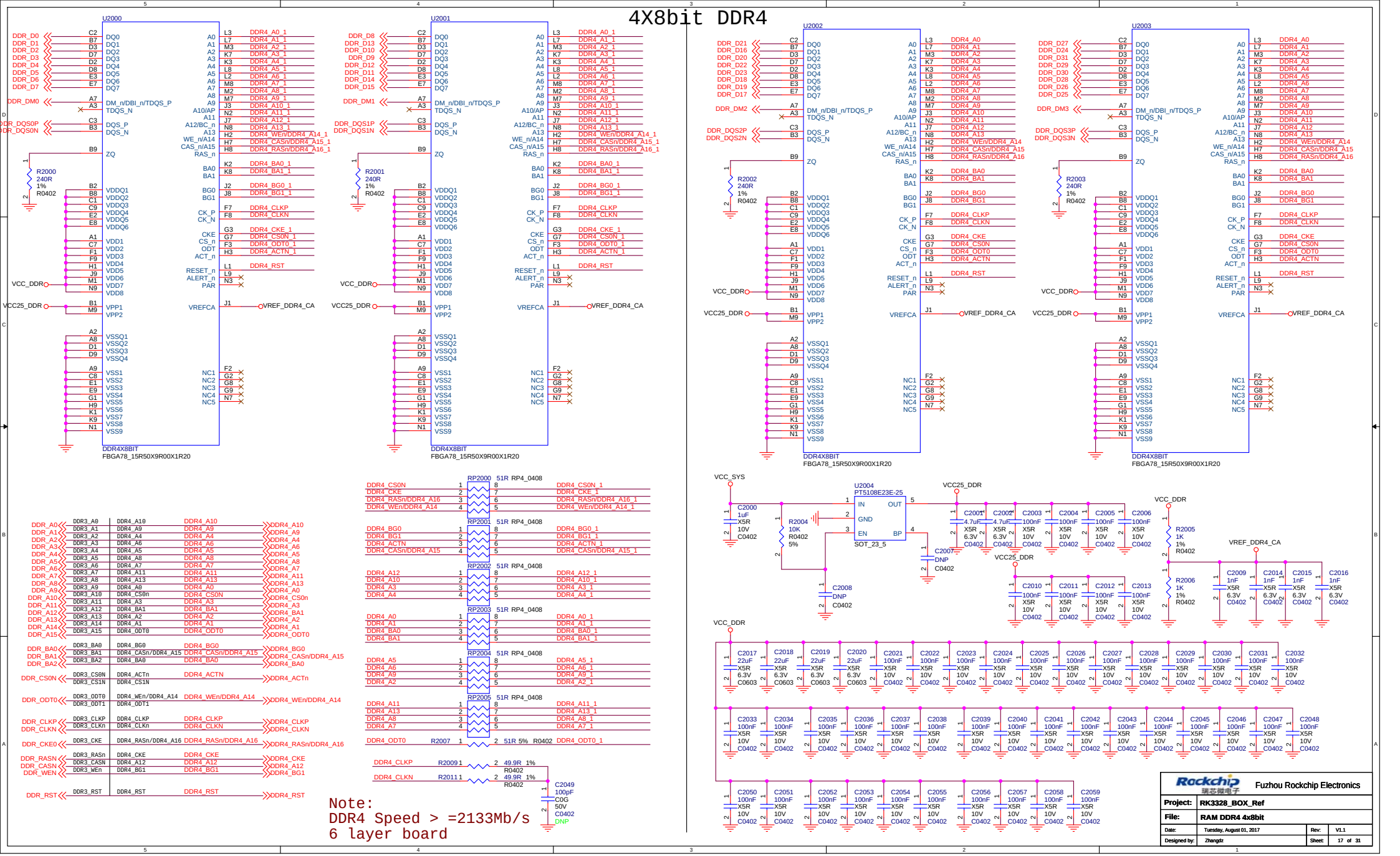
4X8bit DDR4



Note:
DDR4 Speed > =2133Mb/s
6 layer board

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics
Project:	RK3328_BOX_Ref
File:	RAM DDR4 4x8bit
Date:	Tuesday, August 01, 2017
Rev:	V1.1
Designed by:	Zhangdz
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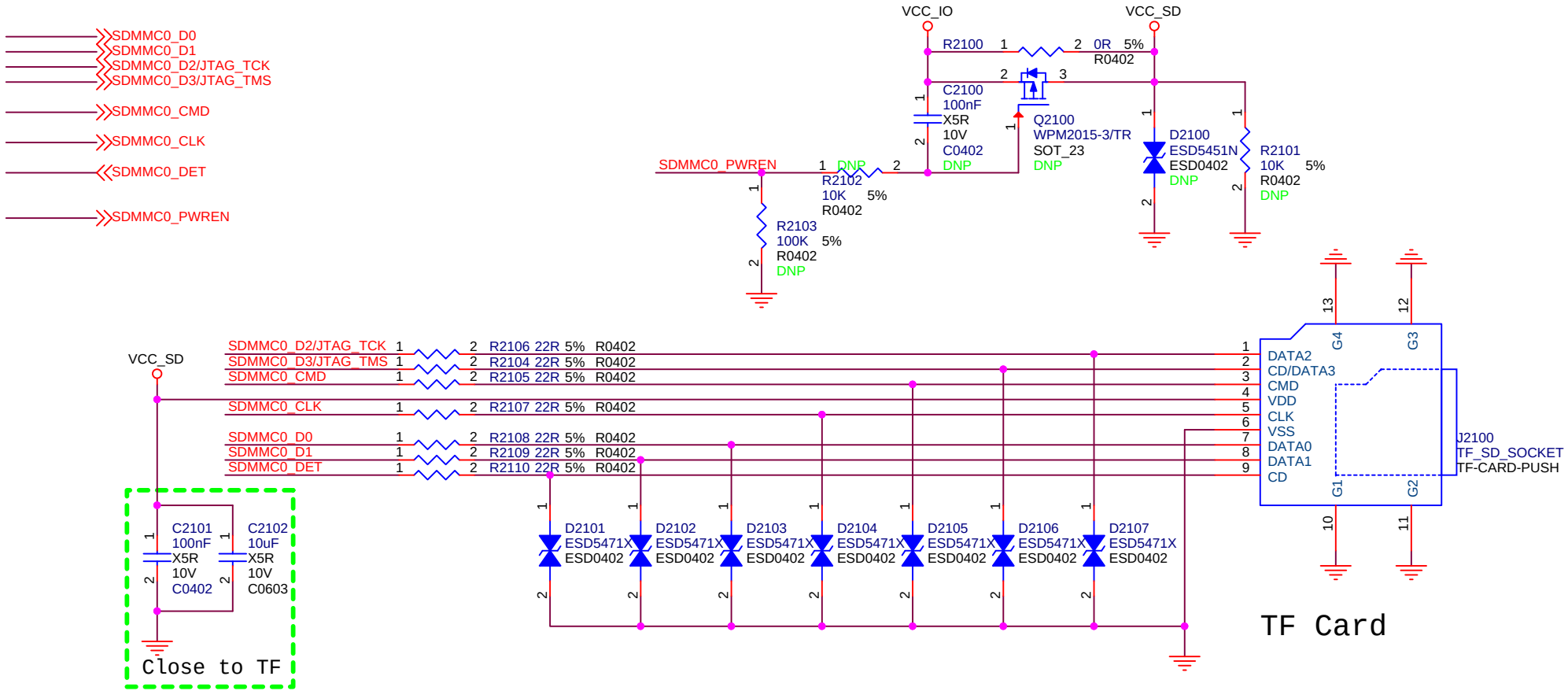
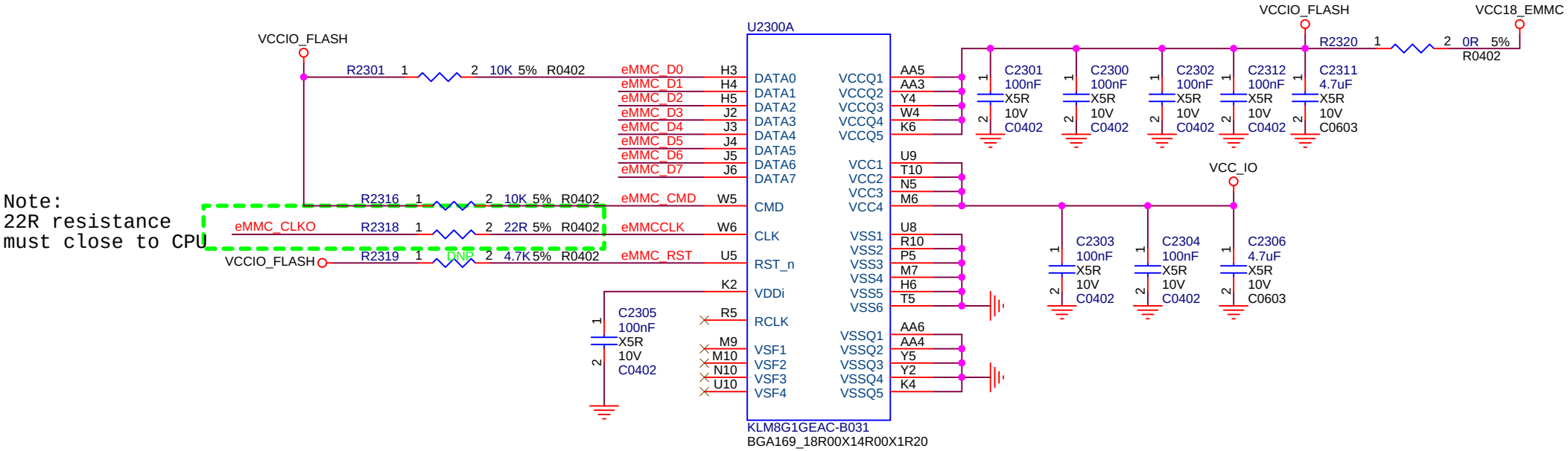
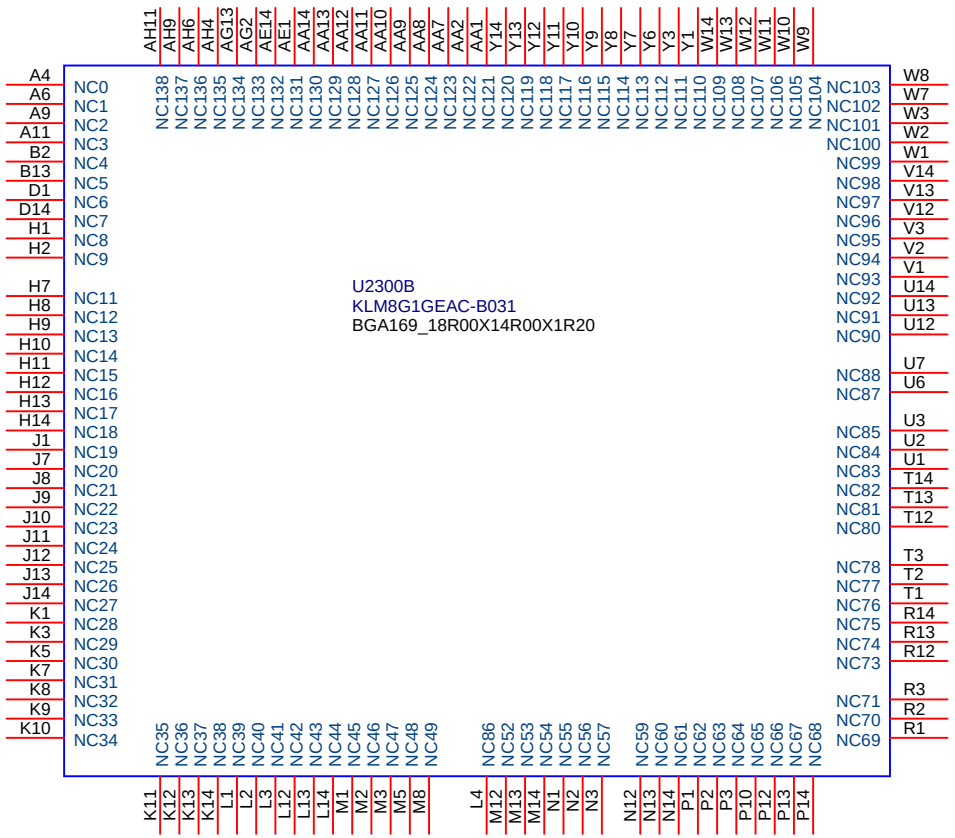
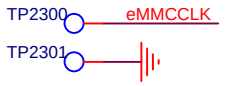


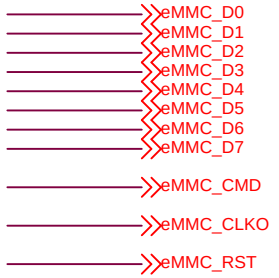
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Ref		
File:	TF/SD Card		
Date:	Tuesday, July 18, 2017	Rev:	V1.1
Designed by:	Zhangdz	Sheet:	18 of 31



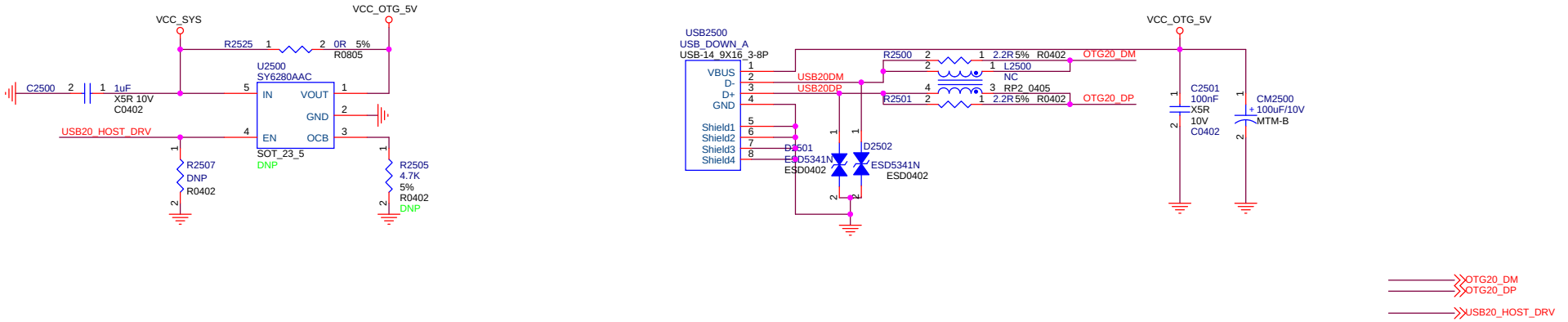


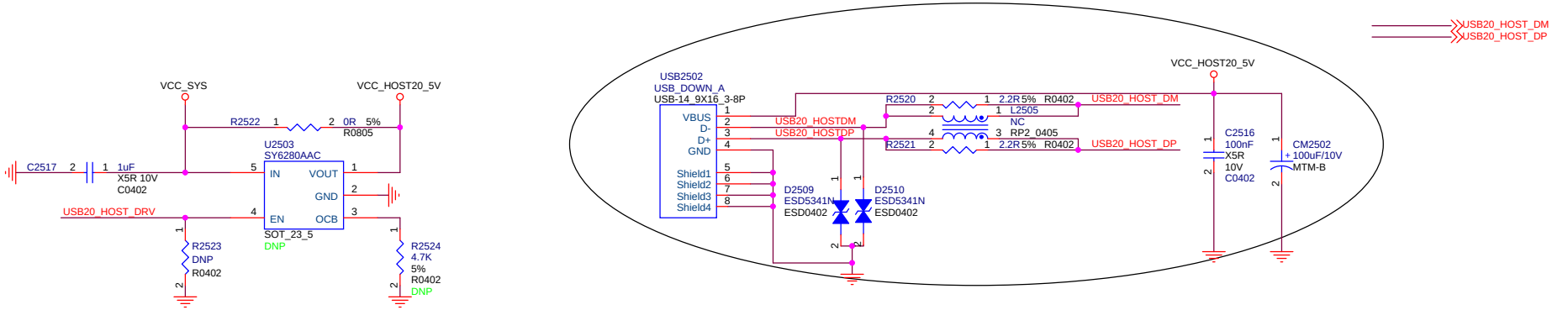


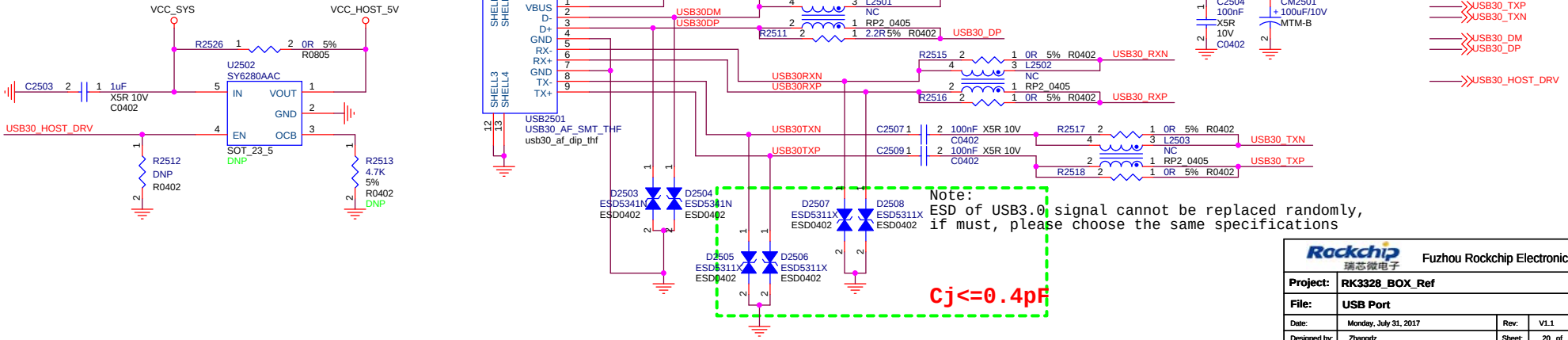
Note:
eMMC Update.



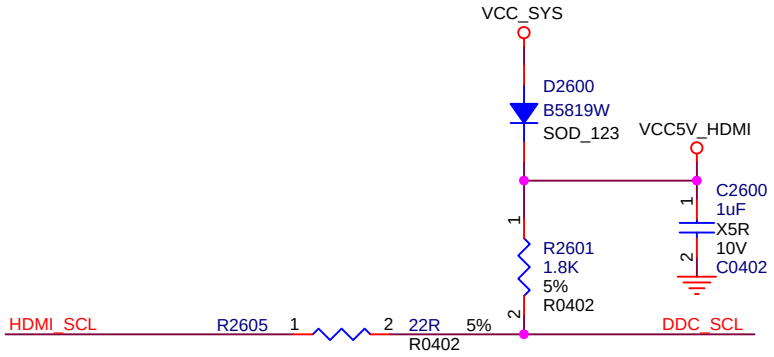
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Ref		
File:	Flash-eMMC		
Date:	Monday, July 31, 2017	Rev:	V1.1
Designed by:	Zhangdz	Sheet:	19 of 31

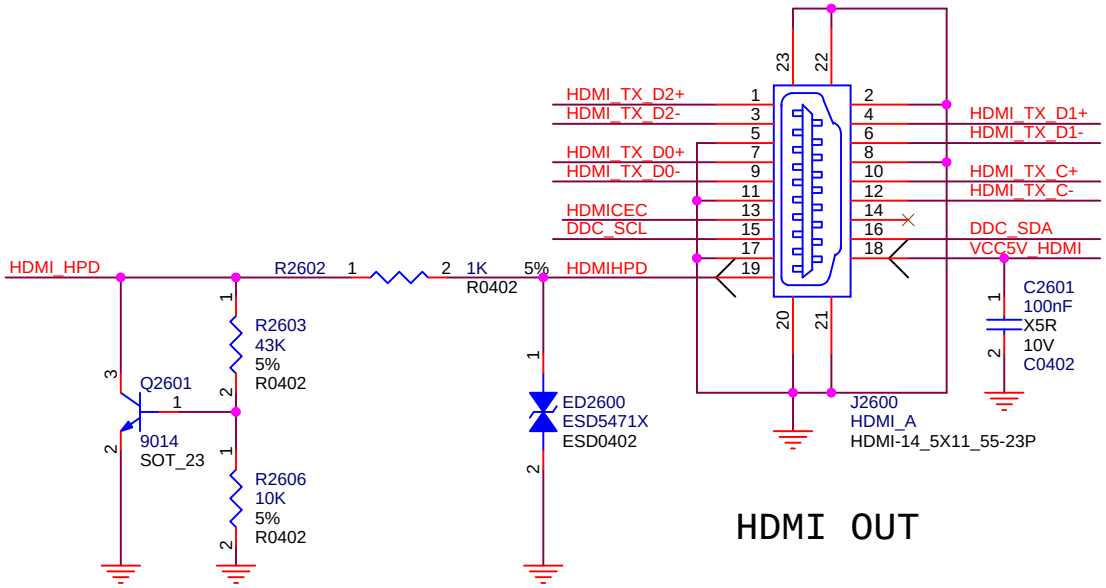




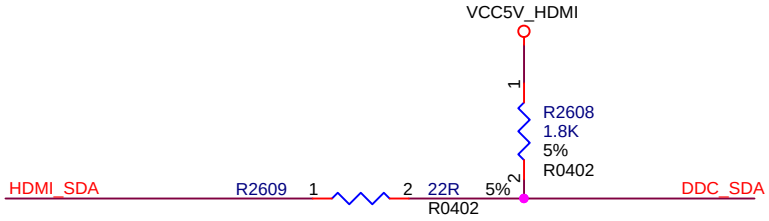


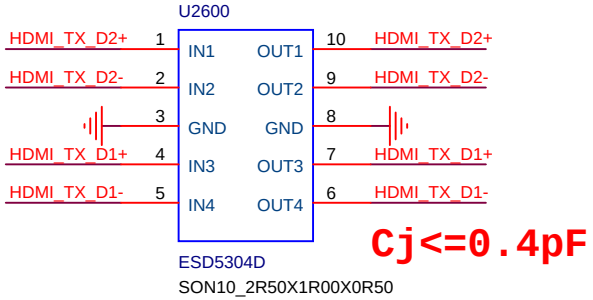
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Ref		
File:	USB Port		
Date:	Monday, July 31, 2017	Rev:	V1.1
Designed by:	Zhangdz	Sheet:	20 of 31



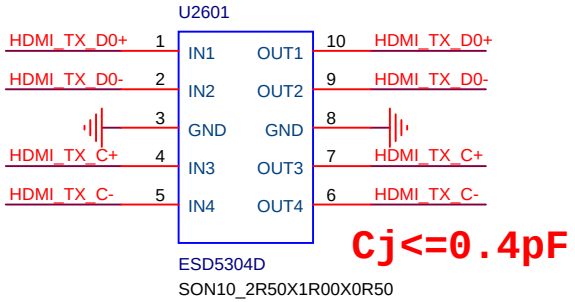


HDMI OUT

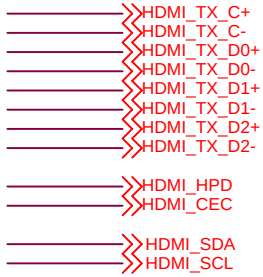


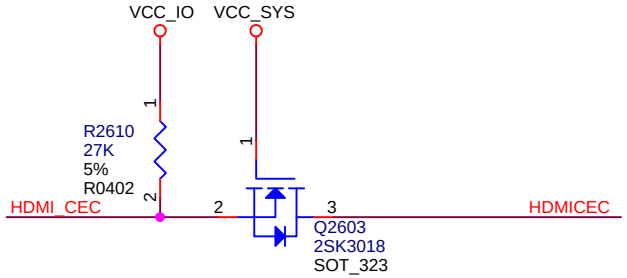


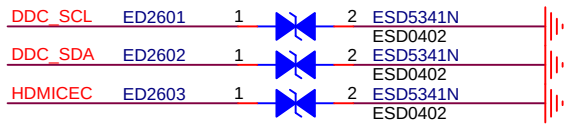
Cj<=0.4pF



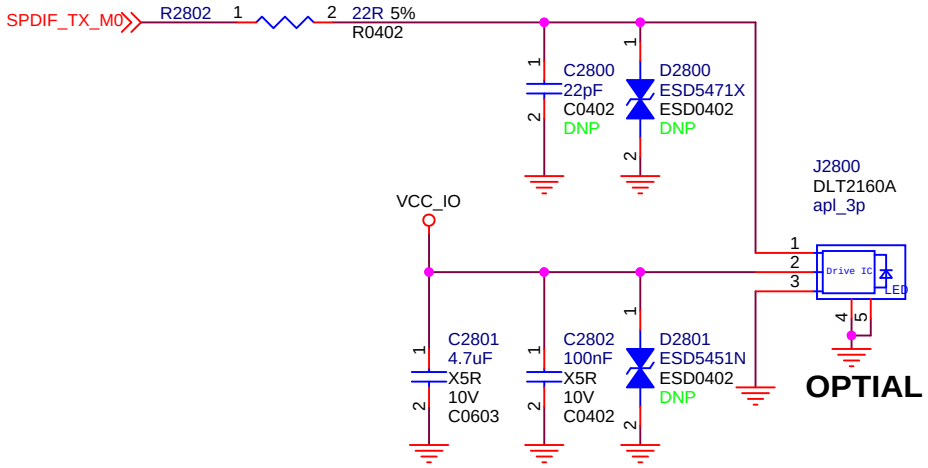
Cj<=0.4pF





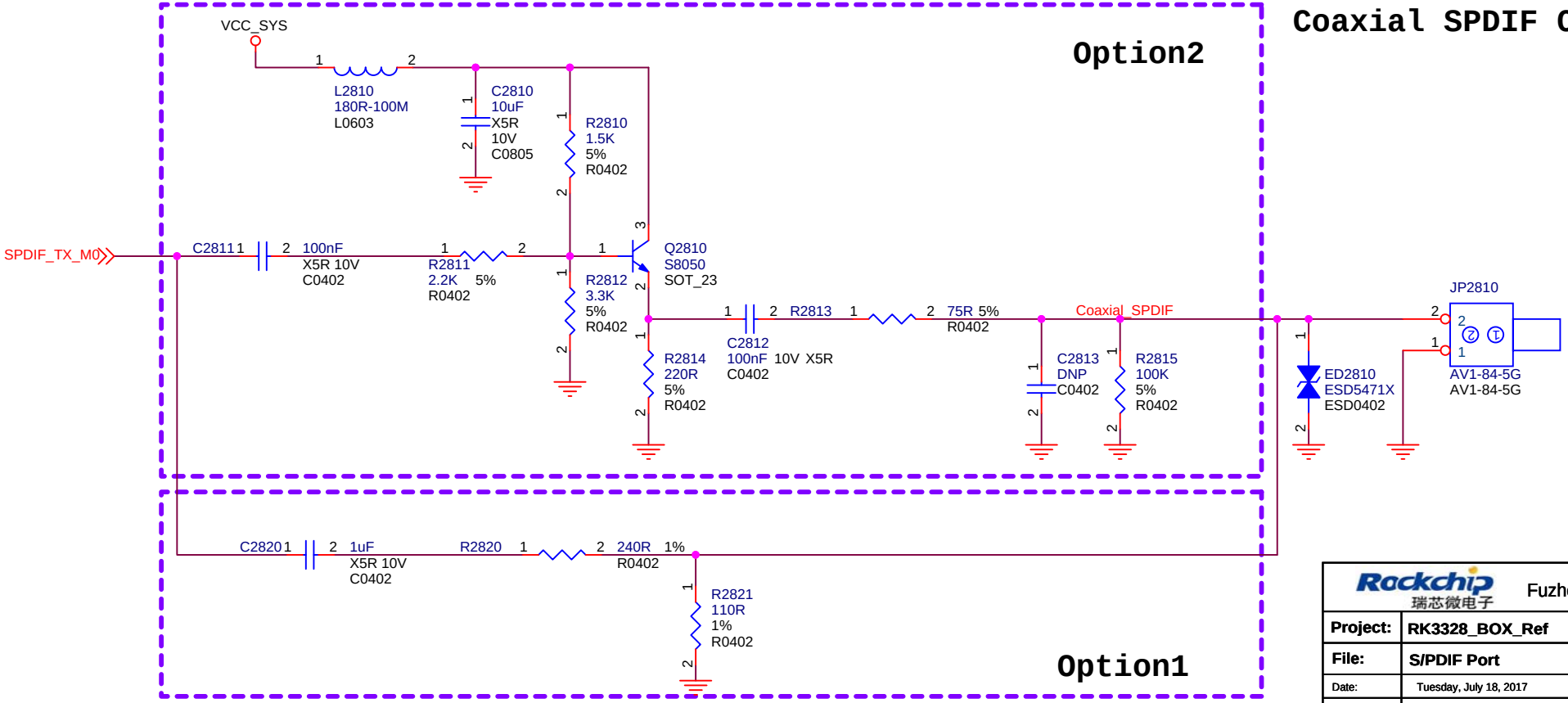


Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Ref		
File:	HDMI OUT Port		
Date:	Tuesday, July 18, 2017	Rev:	V1.1
Designed by:	Zhangdz	Sheet:	21 of 31

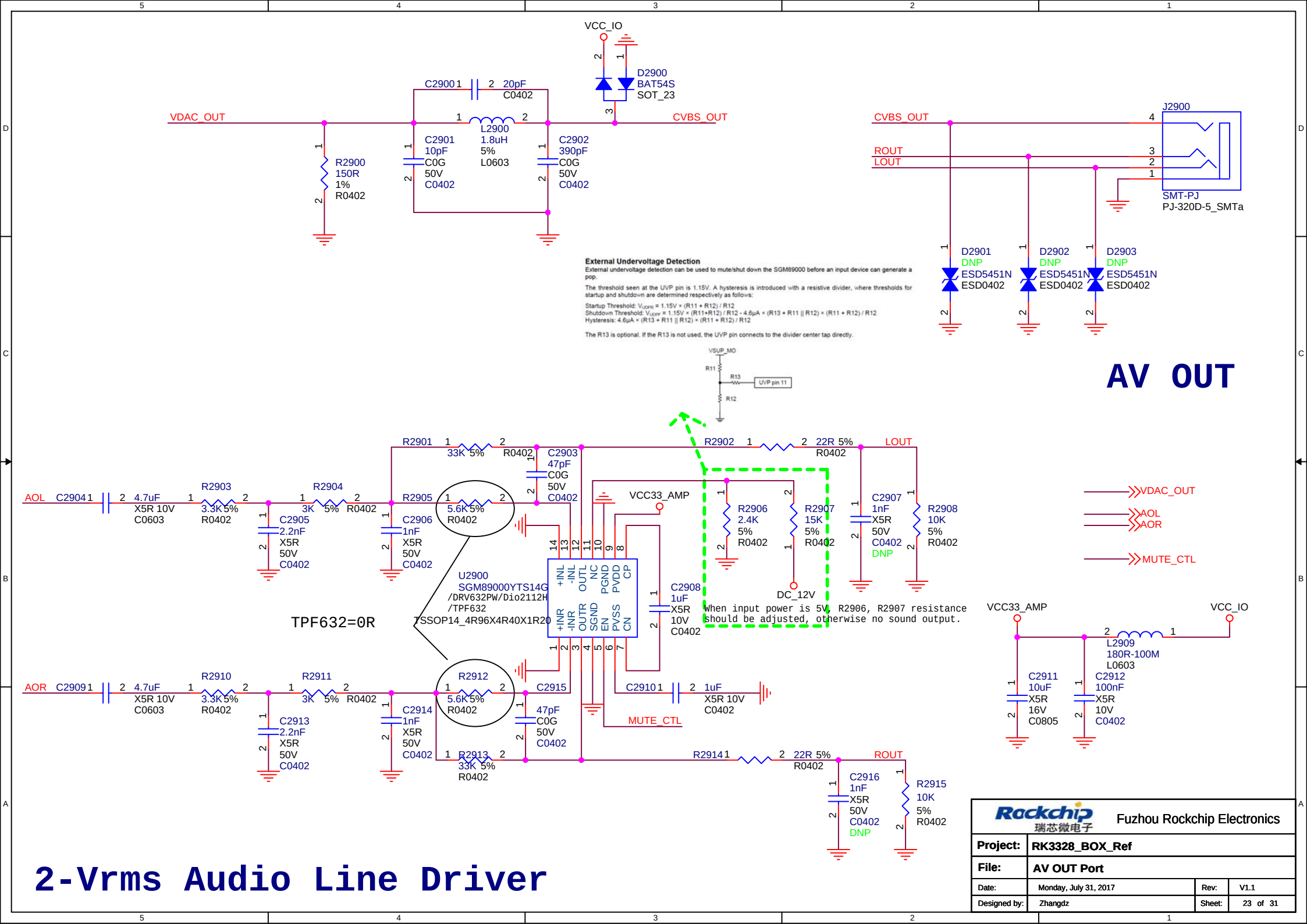


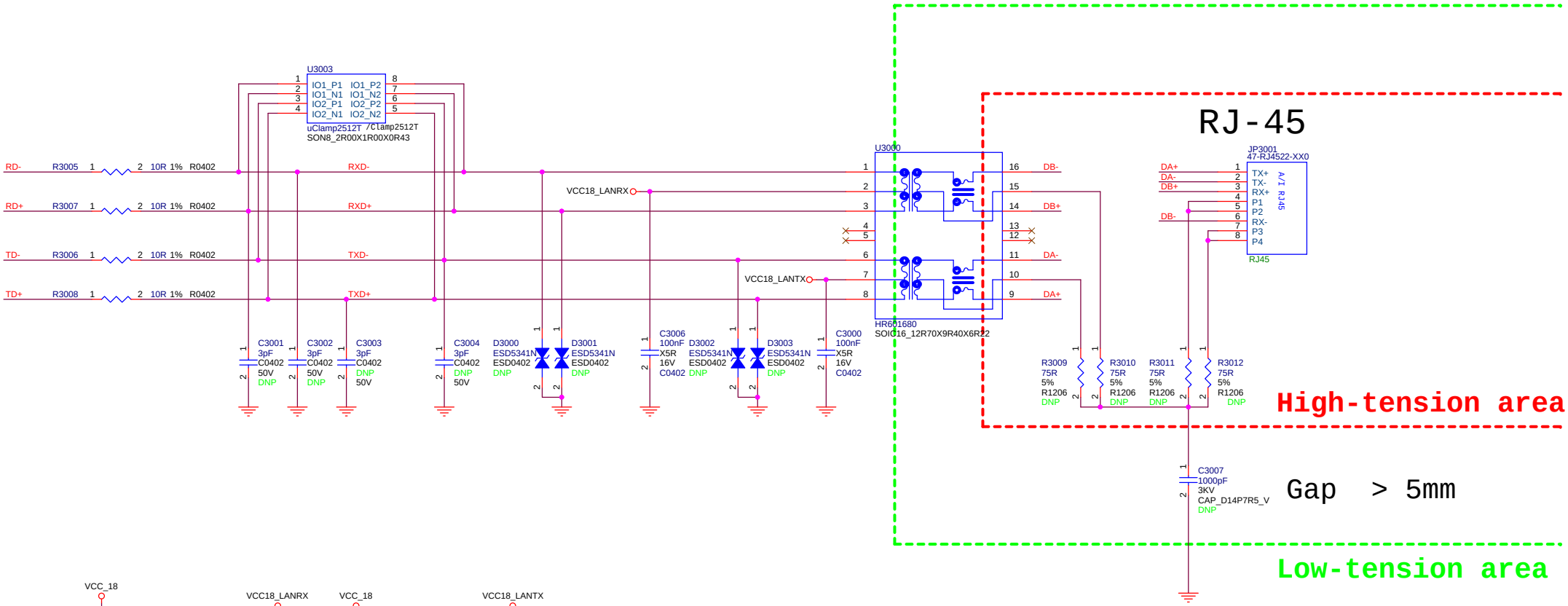
Optical SPDIF OUT

Coaxial SPDIF OUT

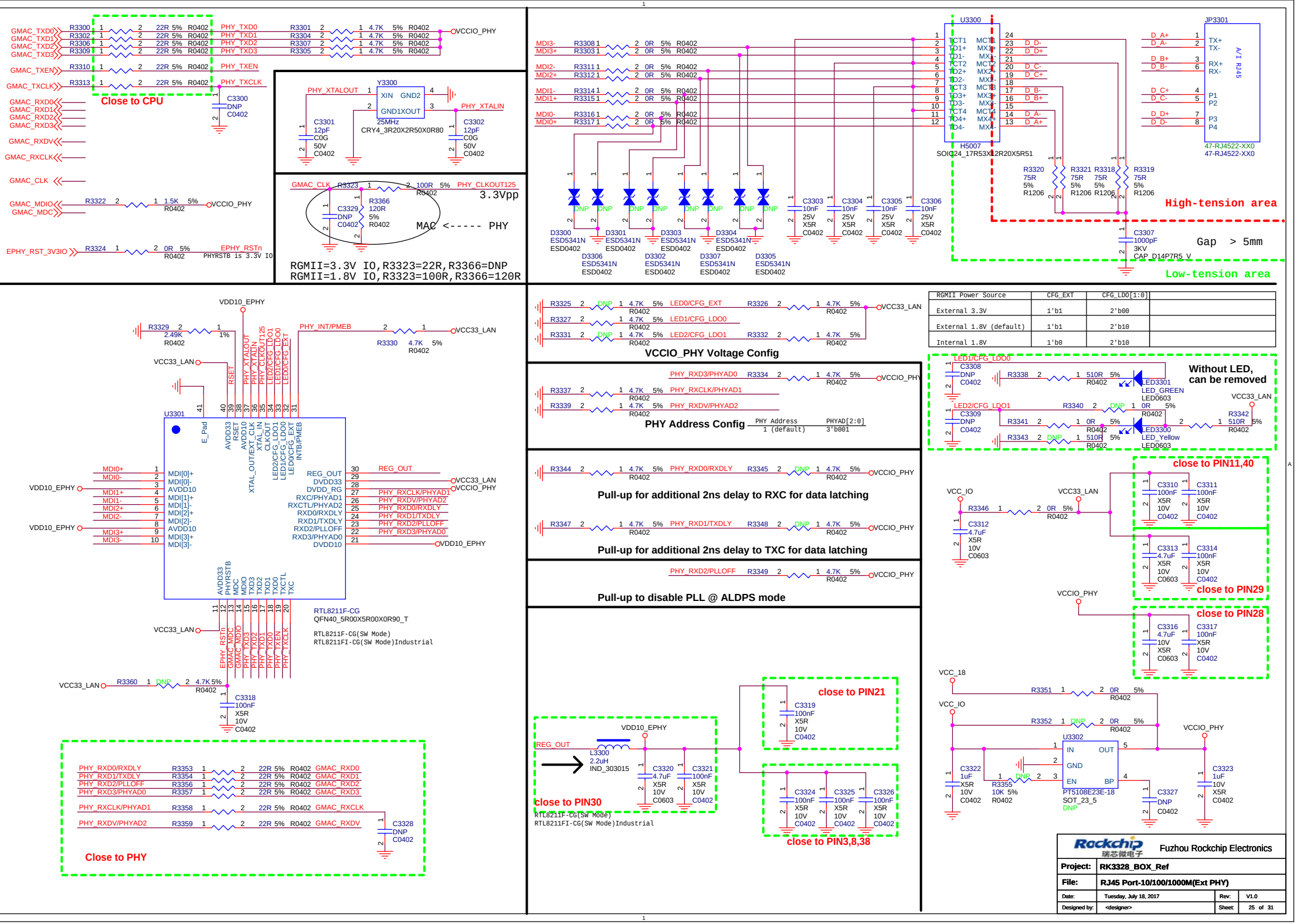


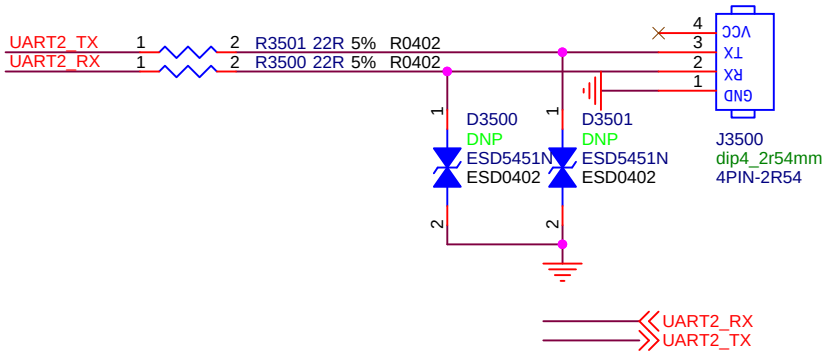
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Ref		
File:	S/PDIF Port		
Date:	Tuesday, July 18, 2017	Rev:	V1.1
Designed by:	Zhangdz	Sheet:	22 of 31


VCC_IO
D2900
BAT54S
SOT_23
C2900 1 2 20pF
C0402
VDAC_OUT
CVBS_OUT
L2900
1.8uH
5%
L0603
R2900
150R
1%
R0402
C2901
10pF
C0G
50V
C0402
C2902
390pF
C0G
50V
C0402
J2900
CVBS_OUT
ROUT
LOUT
SMT-PJ
PJ-320D-5_SMTa
D2901
DNP
ESD5451N
ESD0402
D2902
DNP
ESD5451N
ESD0402
D2903
DNP
ESD5451N
ESD0402
External Undervoltage Detection
External undervoltage detection can be used to mute/shut down the SGM89000 before an input device can generate a pop.
The threshold seen at the UVP pin is 1.15V. A hysteresis is introduced with a resistive divider, where thresholds for startup and shutdown are determined respectively as follows:
Startup Threshold: V_UOPR = 1.15V × (R11 + R12) / R12
Shutdown Threshold: V_UOPF = 1.15V × (R11+R12) / R12 - 4.6μA × (R13 + R11 || R12) × (R11 + R12) / R12
Hysteresis: 4.6μA × (R13 + R11 || R12) × (R11 + R12) / R12
The R13 is optional. If the R13 is not used, the UVP pin connects to the divider center tap directly.
VSUP_MO
R11
R13
UVP pin 11
R12
AV OUT
R2901 1 33K 5% 2 R0402
C2903
47pF
C0G
50V
C0402
R2902 1 2 22R 5% R0402
LOUT
AOL
C2904 1 2 4.7uF
X5R 10V
C0603
R2903
3.3K 5%
R0402
R2904
3K 5% R0402
R2905 1 5.6K 5% 2
R0402
C2905
2.2nF
X5R
50V
C0402
C2906
1nF
X5R
50V
C0402
VCC33_AMP
R2906
2.4K
5%
R0402
R2907
15K
5%
R0402
C2907
1nF
X5R
50V
C0402
DNP
R2908
10K
5%
R0402
DC_12V
U2900
SGM89000YTS14G
/DRV632PW/Dio2112H
/TPF632
TSSOP14_4R96X4R40X1R20
+INL
-INL
OUTL
NC
PGND
PVDD
CP
+INR
-INR
OUTR
SGND
EN
PVSS
CN
C2908
1uF
X5R
10V
C0402
When input power is 5V, R2906, R2907 resistance should be adjusted, otherwise no sound output.
TPF632=0R
VDAC_OUT
AOL
AOR
MUTE_CTL
VCC33_AMP
VCC_IO
L2909
180R-100M
L0603
C2911
10uF
X5R
16V
C0805
C2912
100nF
X5R
10V
C0402
AOR
C2909 1 2 4.7uF
X5R 10V
C0603
R2910
3.3K 5%
R0402
R2911
3K 5% R0402
R2912 1 5.6K 5% 2
R0402
C2913
2.2nF
X5R
50V
C0402
C2914
1nF
X5R
50V
C0402
C2915
47pF
C0G
50V
C0402
C2910 1 2 1uF
X5R 10V
C0402
MUTE_CTL
R2913 1 33K 5% 2
R0402
R2914 1 2 22R 5%
R0402
ROUT
C2916
1nF
X5R
50V
C0402
DNP
R2915
10K
5%
R0402
2-Vrms Audio Line Driver
Rockchip 瑞芯微电子
Fuzhou Rockchip Electronics
Project: RK3328_BOX_Ref
File: AV OUT Port
Date: Monday, July 31, 2017
Rev: V1.1
Designed by: Zhangdz
Sheet: 23 of 31



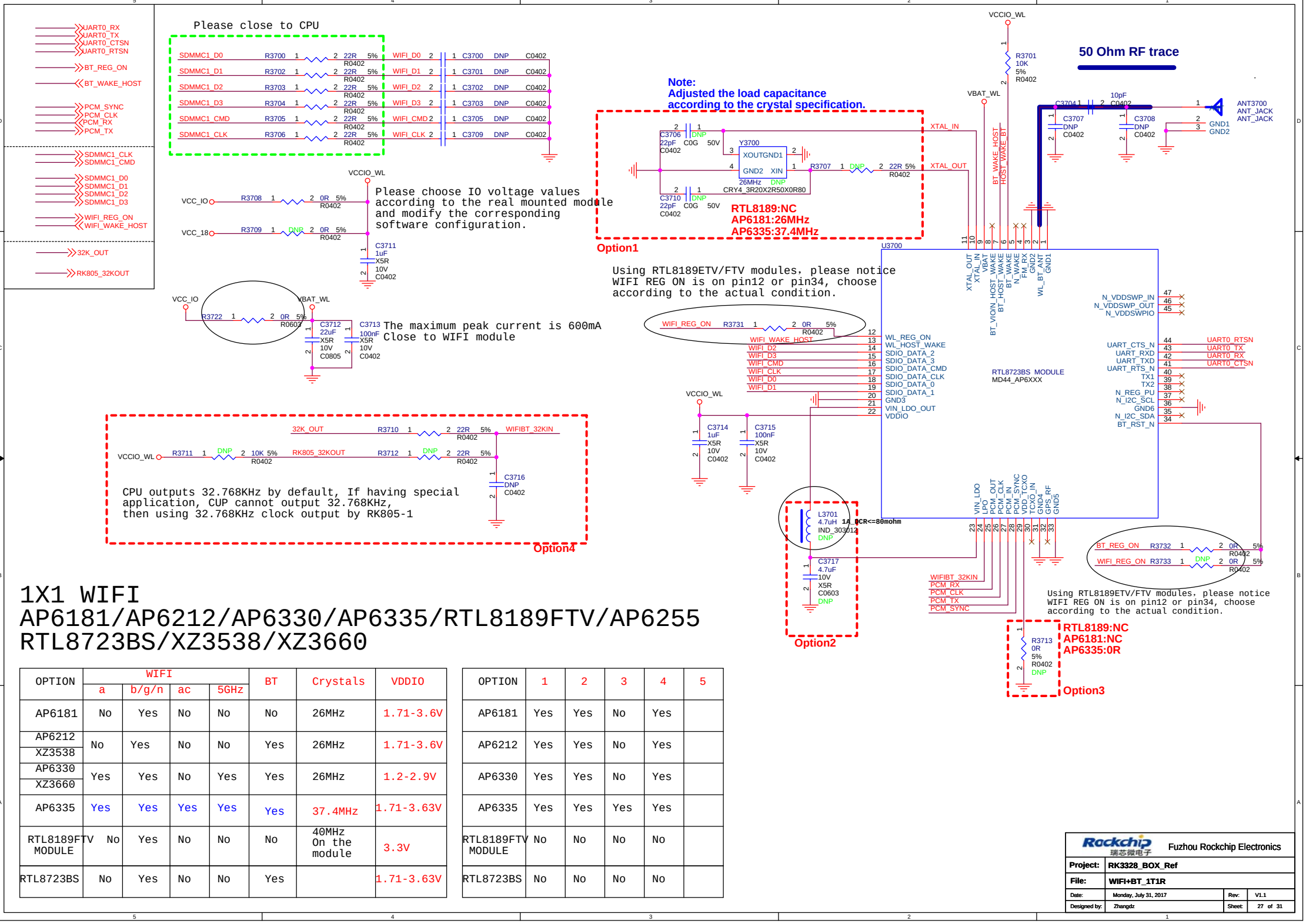
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Ref		
File:	10/100M-Embed PHY		
Date:	Tuesday, July 18, 2017	Rev:	V1.1
Designed by:	Zhangdz	Sheet:	24 of 31


GMAC_TXD0
GMAC_TXD1
GMAC_TXD2
GMAC_TXD3
GMAC_TXEN
GMAC_TXCLK
PHY_TXD0
PHY_TXD1
PHY_TXD2
PHY_TXD3
PHY_TXEN
PHY_TXCLK
VCCIO_PHY
Close to CPU
GMAC_RXD0
GMAC_RXD1
GMAC_RXD2
GMAC_RXD3
GMAC_RXDV
GMAC_RXCLK
GMAC_CLK
GMAC_MDIO
GMAC_MDC
EPHY_RST_3V3IO
EPHY_RST_n
PHYRSTB is 3.3V IO
Y3300
PHY_XTALOUT
PHY_XTALIN
25MHz
CRY4_3R20X2R50X0R80
GMAC_CLK
PHY_CLKOUT125
3.3Vpp
MAC <----- PHY
RGMII=3.3V IO,R3323=22R,R3366=DNP
RGMII=1.8V IO,R3323=100R,R3366=120R
U3300
H5007
SOIC24_17R53X12R20X5R51
JP3301
47-RJ4522-XX0
High-tension area
Low-tension area
Gap > 5mm
VDD10_EPHY
VCC33_LAN
U3301
RTL8211F-CG
QFN40_5R00X5R00X0R90_T
RTL8211F-CG(SW Mode)
RTL8211FI-CG(SW Mode)Industrial
Close to PHY
VCCIO_PHY Voltage Config
PHY Address Config
Pull-up for additional 2ns delay to RXC for data latching
Pull-up for additional 2ns delay to TXC for data latching
Pull-up to disable PLL @ ALDPS mode
RGMII Power Source
CFG_EXT
CFG_LDO[1:0]
External 3.3V
External 1.8V (default)
Internal 1.8V
Without LED, can be removed
close to PIN11,40
close to PIN29
close to PIN28
close to PIN21
close to PIN30
close to PIN3,8,38
Rockchip
Fuzhou Rockchip Electronics
Project: RK3328_BOX_Ref
File: RJ45 Port-10/100/1000M(Ext PHY)
Date: Tuesday, July 18, 2017
Rev: V1.0
Designed by: <designer>
Sheet: 25 of 31



Debug UART2

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3328_BOX_Ref		
File:	Debug UART2/JTAG		
Date:	Tuesday, July 18, 2017	Rev:	V1.1
Designed by:	<designer>	Sheet:	26 of 31



1X1 WIFI
AP6181/AP6212/AP6330/AP6335/RTL8189FTV/AP6255
RTL8723BS/XZ3538/XZ3660

OPTION	WIFI				BT	Crystals	VDDIO
	a	b/g/n	ac	5GHz			
AP6181	No	Yes	No	No	No	26MHz	1.71-3.6V
AP6212 / XZ3538	No	Yes	No	No	Yes	26MHz	1.71-3.6V
AP6330 / XZ3660	Yes	Yes	No	Yes	Yes	26MHz	1.2-2.9V
AP6335	Yes	Yes	Yes	Yes	Yes	37.4MHz	1.71-3.63V
RTL8189FTV MODULE	No	Yes	No	No	No	40MHz On the module	3.3V
RTL8723BS	No	Yes	No	No	Yes		1.71-3.63V

OPTION	1	2	3	4	5
AP6181	Yes	Yes	No	Yes	
AP6212	Yes	Yes	No	Yes	
AP6330	Yes	Yes	No	Yes	
AP6335	Yes	Yes	Yes	Yes	
RTL8189FTV MODULE	No	No	No	No	
RTL8723BS	No	No	No	No	

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics
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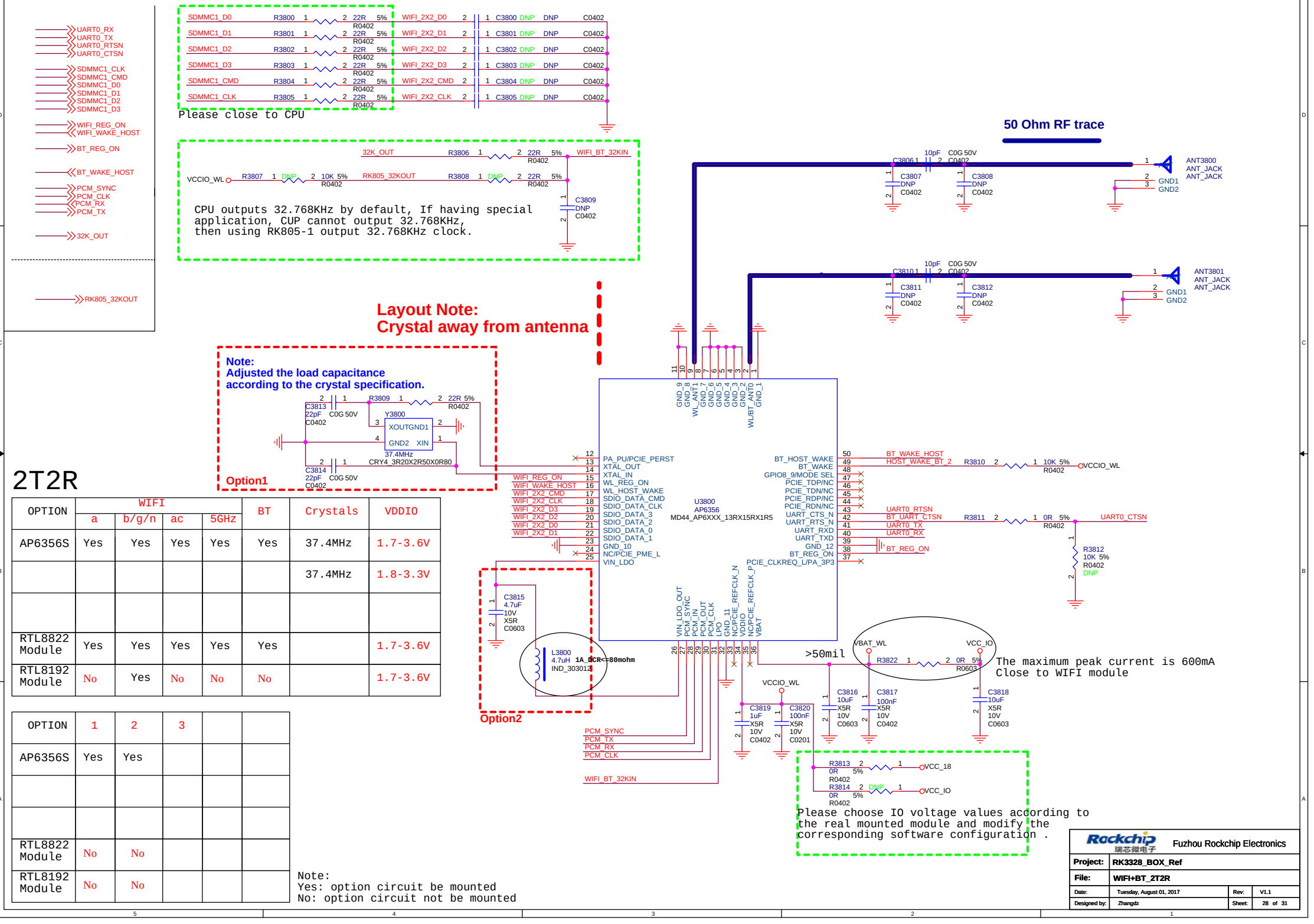

2T2R

OPTION	WIFI				BT	Crystals	VDDIO
	a	b/g/n	ac	5GHz			
AP6356S	Yes	Yes	Yes	Yes	Yes	37.4MHz	1.7-3.6V
						37.4MHz	1.8-3.3V
RTL8822 Module	Yes	Yes	Yes	Yes	Yes		1.7-3.6V
RTL8192 Module	No	Yes	No	No	No		1.7-3.6V

OPTION	1	2	3		
AP6356S	Yes	Yes			
RTL8822 Module	No	No			
RTL8192 Module	No	No			

Note:
Yes: option circuit be mounted
No: option circuit not be mounted

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics
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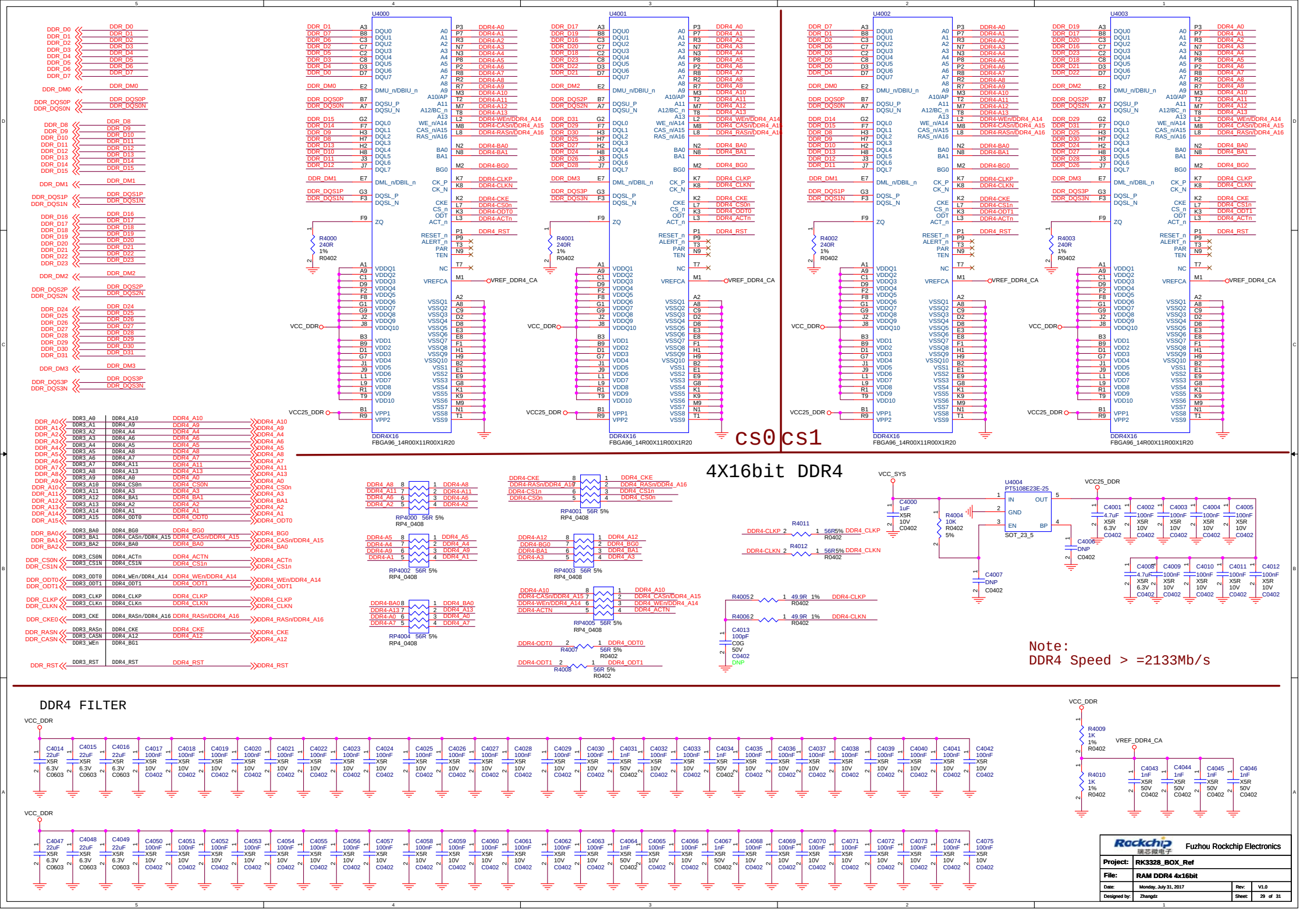
U4000
U4001
U4002
U4003
DDR4X16
FBGA96_14R00X11R00X1R20
cs0 cs1
4X16bit DDR4
Note:
DDR4 Speed > =2133Mb/s
DDR4 FILTER
U4004
PT5108E23E-25
SOT_23_5
VCC_DDR
VCC25_DDR
VCC_SYS
VREF_DDR4_CA
Rockchip
Fuzhou Rockchip Electronics
Project: RK3328_BOX_Ref
File: RAM DDR4 4x16bit
Date: Monday, July 31, 2017
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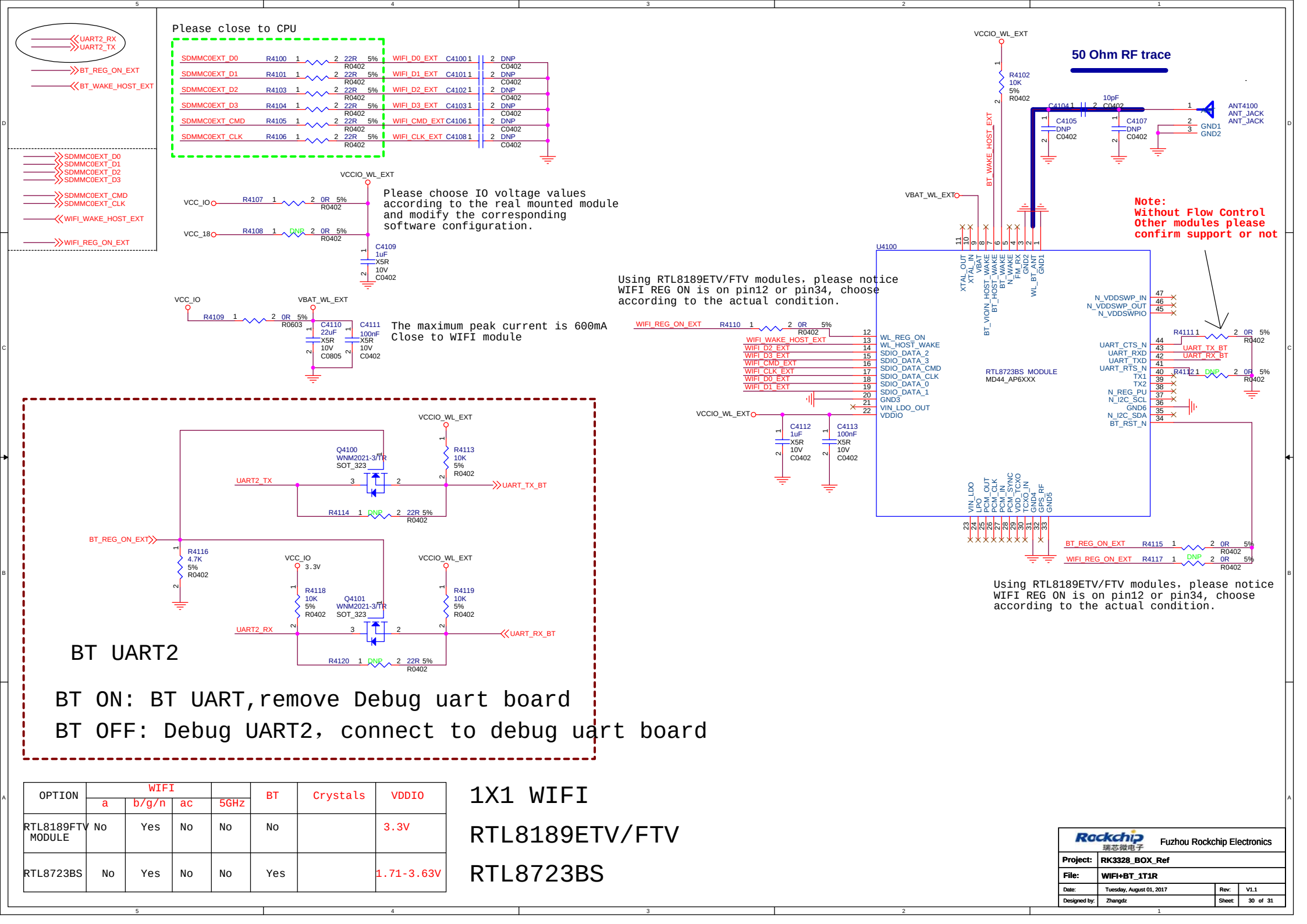

OPTION	WIFI				BT	Crystals	VDDIO
	a	b/g/n	ac	5GHz			
RTL8189FTV MODULE	No	Yes	No	No	No		3.3V
RTL8723BS	No	Yes	No	No	Yes		1.71-3.63V

1X1 WIFI

RTL8189ETV/FTV

RTL8723BS

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
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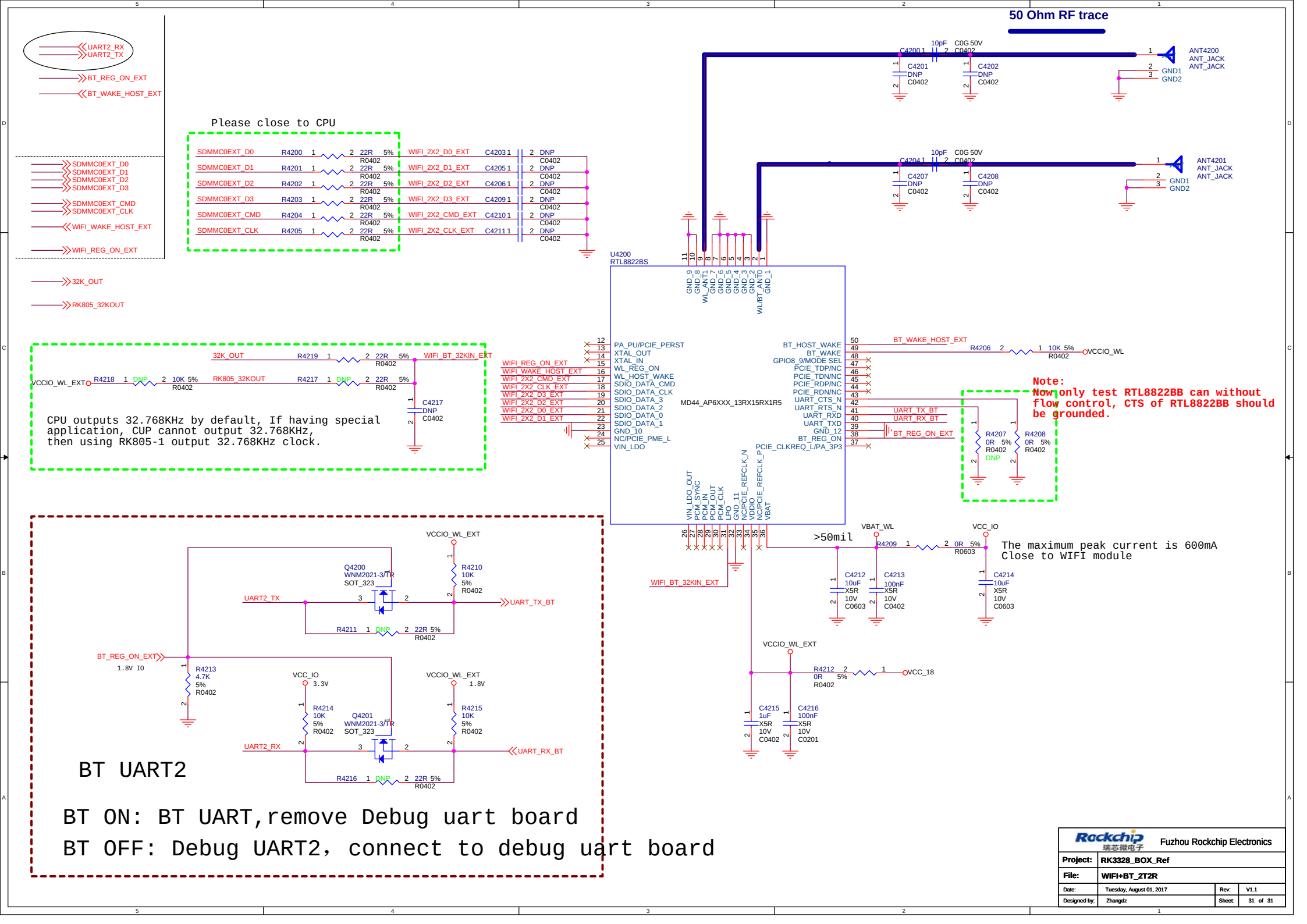
50 Ohm RF trace
UART2_RX
UART2_TX
BT_REG_ON_EXT
BT_WAKE_HOST_EXT
SDMMC0EXT_D0
SDMMC0EXT_D1
SDMMC0EXT_D2
SDMMC0EXT_D3
SDMMC0EXT_CMD
SDMMC0EXT_CLK
WIFI_WAKE_HOST_EXT
WIFI_REG_ON_EXT
32K_OUT
RK805_32KOUT
Please close to CPU
SDMMC0EXT_D0 R4200 22R 5% R0402 WIFI_2X2_D0_EXT C4203 DNP C0402
SDMMC0EXT_D1 R4201 22R 5% R0402 WIFI_2X2_D1_EXT C4205 DNP C0402
SDMMC0EXT_D2 R4202 22R 5% R0402 WIFI_2X2_D2_EXT C4206 DNP C0402
SDMMC0EXT_D3 R4203 22R 5% R0402 WIFI_2X2_D3_EXT C4209 DNP C0402
SDMMC0EXT_CMD R4204 22R 5% R0402 WIFI_2X2_CMD_EXT C4210 DNP C0402
SDMMC0EXT_CLK R4205 22R 5% R0402 WIFI_2X2_CLK_EXT C4211 DNP C0402
C4200 10pF C0G 50V C0402
C4201 DNP C0402
C4202 DNP C0402
ANT4200 ANT_JACK ANT_JACK
GND1 GND2
C4204 10pF C0G 50V C0402
C4207 DNP C0402
C4208 DNP C0402
ANT4201 ANT_JACK ANT_JACK
GND1 GND2
U4200
RTL8822BS
GND_9 GND_8 WL_ANT1 GND_7 GND_6 GND_5 GND_4 GND_3 GND_2 WL/BT_ANT0 GND_1
PA_PU/PCIE_PERST
XTAL_OUT
XTAL_IN
WL_REG_ON
WL_HOST_WAKE
SDIO_DATA_CMD
SDIO_DATA_CLK
SDIO_DATA_3
SDIO_DATA_2
SDIO_DATA_0
SDIO_DATA_1
GND_10
NC/PCIE_PME_L
VIN_LDO
MD44_AP6XXX_13RX15RX1R5
BT_HOST_WAKE
BT_WAKE
GPIO8_9/MODE SEL
PCIE_TDP/NC
PCIE_TDN/NC
PCIE_RDP/NC
PCIE_RDN/NC
UART_CTS_N
UART_RTS_N
UART_RXD
UART_TXD
GND_12
BT_REG_ON
PCIE_CLKREQ_L/PA_3P3
VIN_LDO_OUT PCM_SYNC PCM_IN PCM_OUT PCM_CLK LPO GND_11 NC/PCIE_REFCLK_N VDDIO NC/PCIE_REFCLK_P VBAT
BT_WAKE_HOST_EXT
R4206 10K 5% R0402 VCCIO_WL
UART_TX_BT
UART_RX_BT
BT_REG_ON_EXT
R4207 0R 5% R0402 DNP
R4208 0R 5% R0402
Note:
Now only test RTL8822BB can without flow control, CTS of RTL8822BB should be grounded.
32K_OUT R4219 22R 5% R0402 WIFI_BT_32KIN_EXT
VCCIO_WL_EXT R4218 DNP 10K 5% R0402 RK805_32KOUT R4217 DNP 22R 5% R0402
C4217 DNP C0402
CPU outputs 32.768KHz by default, If having special application, CUP cannot output 32.768KHz, then using RK805-1 output 32.768KHz clock.
WIFI_REG_ON_EXT
WIFI_WAKE_HOST_EXT
WIFI_2X2_CMD_EXT
WIFI_2X2_CLK_EXT
WIFI_2X2_D3_EXT
WIFI_2X2_D2_EXT
WIFI_2X2_D0_EXT
WIFI_2X2_D1_EXT
WIFI_BT_32KIN_EXT
>50mil
VBAT_WL
R4209 0R 5% R0603
VCC_IO
The maximum peak current is 600mA
Close to WIFI module
C4212 10uF X5R 10V C0603
C4213 100nF X5R 10V C0402
C4214 10uF X5R 10V C0603
VCCIO_WL_EXT
R4212 0R 5% R0402 VCC_18
C4215 1uF X5R 10V C0402
C4216 100nF X5R 10V C0201
VCCIO_WL_EXT
Q4200 WNM2021-3/TR SOT_323
R4210 10K 5% R0402
UART2_TX
UART_TX_BT
R4211 DNP 22R 5% R0402
BT_REG_ON_EXT
1.8V IO
R4213 4.7K 5% R0402
VCC_IO 3.3V
VCCIO_WL_EXT 1.8V
R4214 10K 5% R0402
Q4201 WNM2021-3/TR SOT_323
R4215 10K 5% R0402
UART2_RX
UART_RX_BT
R4216 DNP 22R 5% R0402
BT UART2
BT ON: BT UART,remove Debug uart board
BT OFF: Debug UART2, connect to debug uart board
Rockchip 瑞芯微电子 Fuzhou Rockchip Electronics
Project: RK3328_BOX_Ref
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