Micro−Research Finland Oy

Event Generator EVG-110 plus
Event Receiver EVR-100

Users Manual
version 3.0

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1. Introduction to Event System

Synchrotron light sources as well as other accelerator facilities require a means of distributing timing information with a very high level of precision. Timing events and clock signals are needed to synchronize technical subsystems of the machine for example controlling the injection and acceleration and provide timing information to beamline experiments.

The Event System provides a complete timing distribution system including timing signal generation with only a few components. Throughout the design of the Event System especially requirements of synchrotron light sources were taken into consideration, however, the system may be applied also to other facilities.

Usually timing events are synchronized to a master clock reference e.g. the main acceleration frequency. Synchronization to the mains voltage phase is required, too, to keep the beam intensity and quality on the same level on consecutive triggers.

The Event System is capable of generating and distributing ring revolution frequencies, trigger signals and sequences of events, etc. synchronous to an externally provided master clock reference and mains voltage phase signal. Support for timestamps makes the system a global timebase and allows attaching timestamps to collected data and performed actions.

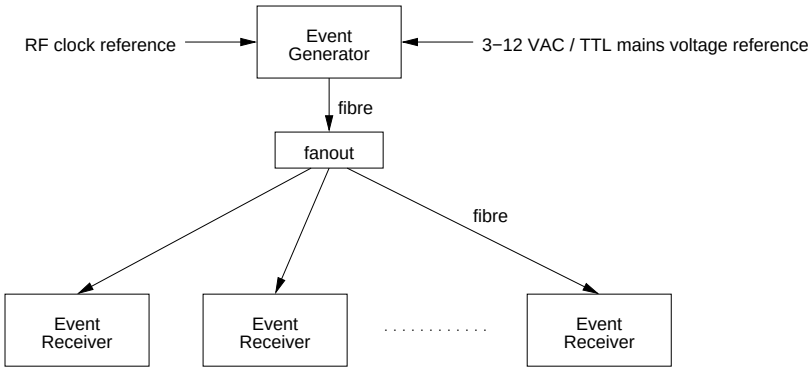

Figure 1: Event Distribution Priciple.

Generally only one Event Generator is required to generate and provide all timing signals to various subsystems. The Event Generator is located close to the master timing reference. The timing signals are distributed by a multimode fiber network in star topology. Event Receivers receive the *event stream* sent by the Event Generators and generate hardware and software signals.

1.1. Event Stream

The structure of the event stream is described to help understand the functioning of the event system. The event stream should be considered as an event frame of two bytes sent out at the rate of the system event clock. The event frame consists of one event code and the state of eight distributed bus signals. The transmission of the event stream from the event generator over the fiber to the event receivers is transparent to the user.

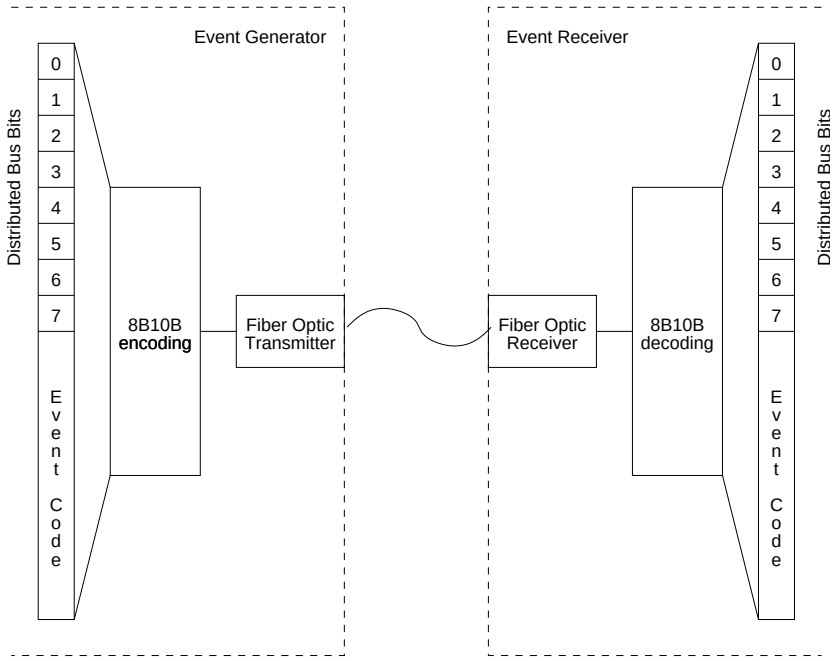

Figure 2: Event Frame Composition

There are 256 event codes from which a few have special functions. The special function event codes are listed below. All other codes are user defined. Only one event code may be transferred at a time.

Table 1: Special Function Event Codes

Event Code	Function
0x00	Null Event Code
0x7a	EVR Reset Heartbeat Monitor
0x7b	EVR Reset/Sync Prescaler Outputs
0x7c	EVR Timestamp Counter Increment
0x7d	EVR Timestamp Counter Reset
0x7e	EVG Sequence RAM Freeze Sequence Code
0x7f	EVG Sequence RAM End Sequence Code

The distributed bus allows transmission of eight simultaneous signals with the event clock rate time resolution. The source for distributed bus signals may come from an external output or the

signal may be generated with a programmable counter inside the event generator. The distributed bus signals are available as hardware outputs on the event receiver.

1.2. Introduction to Light Sources

Figure 3: Swiss Light Source (SLS)

The main component of a synchrotron light source is the electron storage ring. Powerful electric and magnetic fields control the travel of particle bunches around a ring-shaped tube. The particles accelerated to a high energy are stored in a stable orbit around the ring. As the electrons travel around the ring close to the speed of light they lose energy which is emitted as light with wavelengths from infrared to high-energy X-rays.

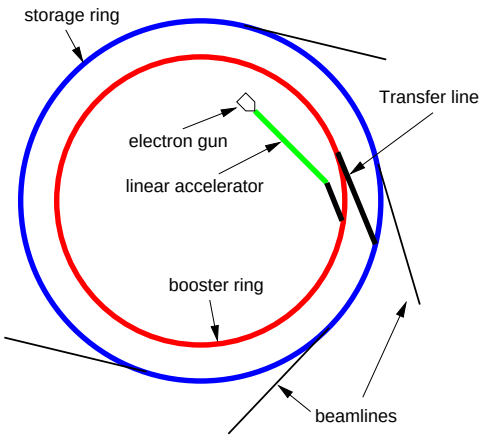

Figure 4: Synchrotron light source layout.

Electrons are first fired from a particle source (gun) into a linear accelerator and then injected into a booster which accelerates the electrons even further. After acceleration the electrons are extracted from the booster and injected into the storage ring to fill up the RF buckets and maintain the number of electrons in the storage ring constant.

1.3. Light Source Timing

Synchrotron light sources as well as other accelerator facilities require a means of distributing timing information with a very high level of precision. Timing events and clock signals are needed

to synchronize technical subsystems of the machine for example controlling the injection and acceleration.

Timing signals of a synchrotron light source are derived from a master radio frequency (RF) oscillator which provides the accelerating frequency to the booster and storage rings. With many light sources the RF frequency is around 500 MHz. The following table represents machine parameters of the Swiss Light Source (SLS).

Table 2: Machine parameters of the Swiss Light Source (SLS)

Accelerating frequency	499.652 MHz
Accelerating period	2 ns
Storage ring circumference	288 m
Number of bunches (SR)	480
Orbit frequency (SR)	1.042 MHz
Booster ring circumference	270 m
Number of bunches (Booster)	450
Orbit frequency (Booster)	1.111 MHz
Coincidence frequency	69.444 kHz

Usually, the injection cycle of a synchrotron light source operates at rate of a few hertz e.g. at SLS the injection cycle is 320 ms (3.125 Hz = 50/16 Hz). The injection cycle is synchronized to both the mains voltage (50 Hz) and the coincidence frequency which depends on relationship of the number of buckets in the booster and storage ring. The coincidence frequency is the rate at which the same RF buckets in the booster and storage ring are aligned.

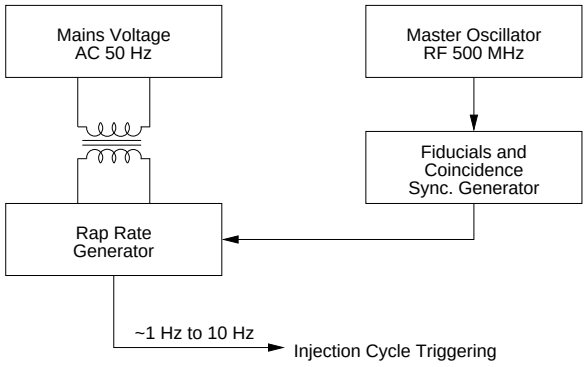

Figure 5: Synchrotron light source injection timing.

Synchronization to the mains voltage is required to keep the beam intensity and quality on the same level on consecutive triggers. Synchronization to the coincidence frequency is necessary to be able to target the electrons of a single trigger to a specific RF bucket in the storage ring.

There are also beamline experiments that require synchronization to the storage ring revolution frequency.

1.4. Event System - Event Generator (EVG)

Figure 6: Event Generator Module

The Event Generator (EVG) is responsible of creating and sending out timing events to an array of Event Receivers. High configurability makes it feasible to build a whole timing system with a single Event Generator without external counters etc.

Events are sent out by the event generator as event frames (words) which consist of an eight bit event code and an eight bit distributed bus data byte. The event transfer rate is derived from an external RF clock or optionally an on-board crystal oscillator. The transceiver gigabit bit rate is phase locked to the clock reference.

There are several sources of events: trigger events, sequence RAM events, VME events and events received from an upstream Event Generator. Events from different sources have different priority which is resolved in a priority encoder.

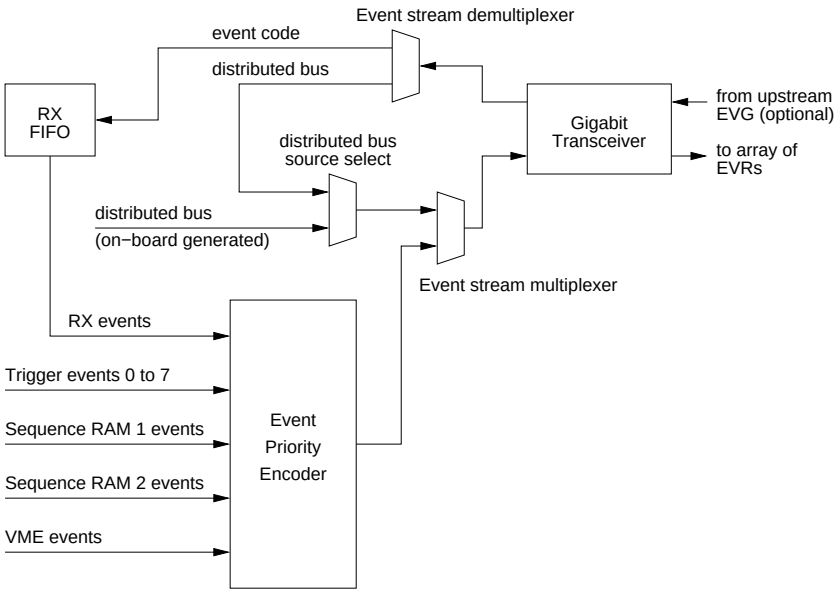

Figure 7: Event Generator Block Diagram 1. Priority Encoder and Trancseiver

Event Generators may be cascaded e.g. to create a sub-branch with all the main timing information available and adding events needed for this sub-branch only.

1.4.1. Event System - Event Generation

Events may generated from external signals, internal prescalers/counters, sequence RAMs or by VME software access.

Synchronization to mains voltage is provided by a 50 to 60 Hz <!–TTL or–> 3-12 VAC input. The event transfer rate is determined by downconverting (dividing) from an externally applied high precision RF reference, optionally an on-board reference may be used as a main sychronization clock.

1.4.1.1. Event Triggers

Eight independent TTL level edge sensitive signals trigger the transmission of programmable event codes. Each event trigger has its own enable bit. Each event trigger may be programmed to trigger from a multiplexed counter output.

The output of the mains voltage synchronization logic may be programmed to trigger an event. The output is hard-wired to event trigger 0.

1.4.1.2. Event Sequence RAMs

Event sequence RAMs provide a method of transmitting or playing back sequences of events stored in random access memory. The sequence RAM clock may be selected to be applied externally or downconverted directly from the event clock with a 16-bit prescaler.

The triggering of an event sequence RAM may be initiated by an external input, multiplexed counter output, the mains voltage synchronization logic output or a software trigger from VME.

There are two sequence RAM allowing altering the contents of the first one while the other one is used for playback.

1.4.1.3. VME Events

Events may be transmitted flexibly by software with a single write operation to a byte wide event register.

1.4.2. Distributed Bus

The Event System allows transmission of only one event code per event cycle, so simultaneous events cannot be transmitted. However, there may be need to distribute simultaneous signals in a timing system. To overcome this, a distributed bus was implemented. The state of an eight bit wide bus is transmitted at the event rate. This allows up to eight signals to be transmitted simultaneously with the event rate time resolution.

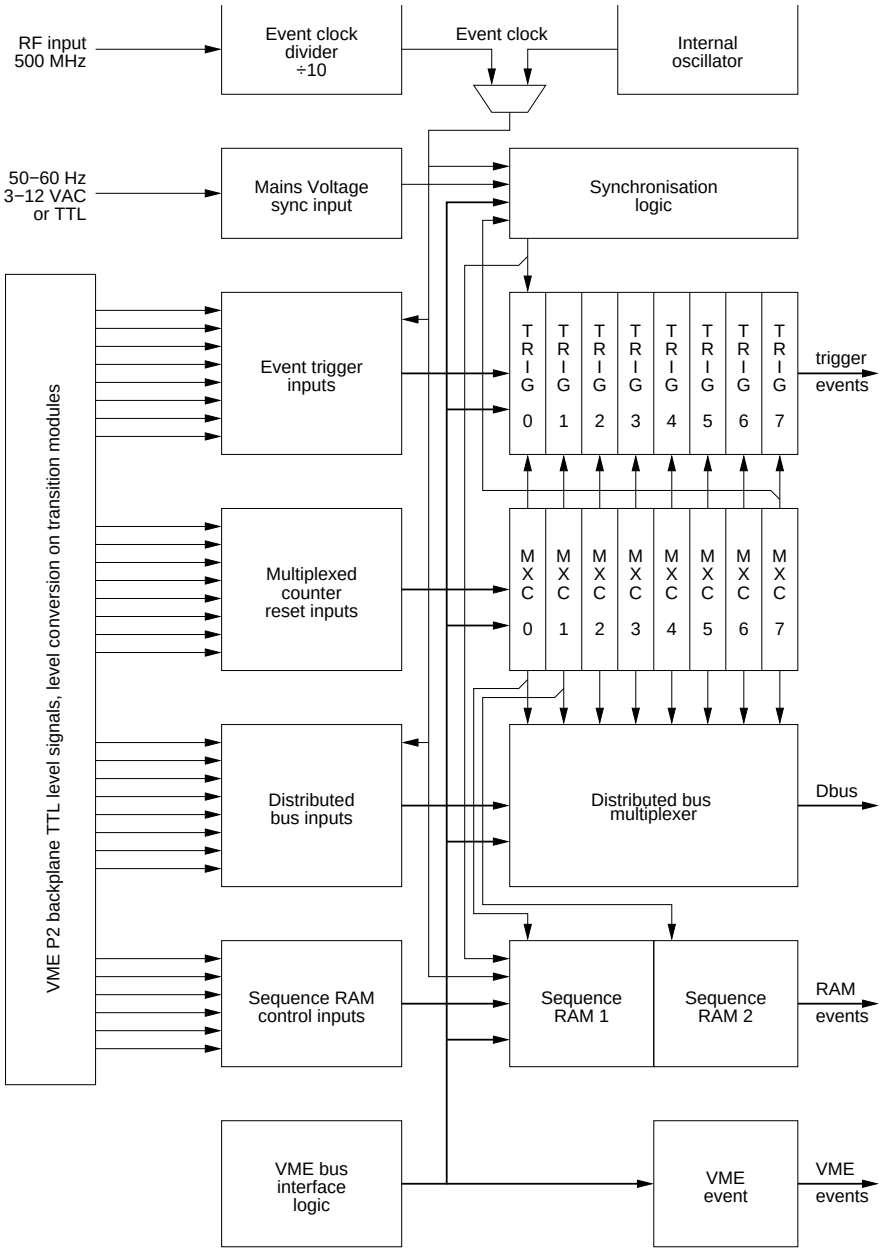

Figure 8: Event Generator Block Diagram 2. Event Sources, Multiplexed counters, Distributed bus generation

The bits of the distributed bus are sampled at the event rate from external signals, alternatively the distributed bus signals may be generated by multiplexed counters. If there as an upstream EVG, the state of the distributed bus may be forwarded by the EVG.

1.4.3. Multiplexed Counters

Eight 32-bit multiplexed counters generate clock signals with programmable frequencies from event clock/2^32+1 to event clock/2. Even divisors create 50% duty cycle signals. The counter outputs may be programmed to trigger events, drive distributed bus signals and trigger sequence RAMs. The output of multiplexed counter 7 is hard-wired to the mains voltage synchronization logic.

1.4.4. Mains Voltage Synchronization

The Event Generator provides synchronization to the mains voltage frequency. The mains voltage frequency is divided by an eight bit programmable divider. The output of the divider may be delayed by 0 to 25.5 ms by a phase shifter in 0.1 ms steps to be able to adjust the triggering position relative to mains voltage phase. After this the signal synchronized to the event clock or the output of multiplexed counter 7.

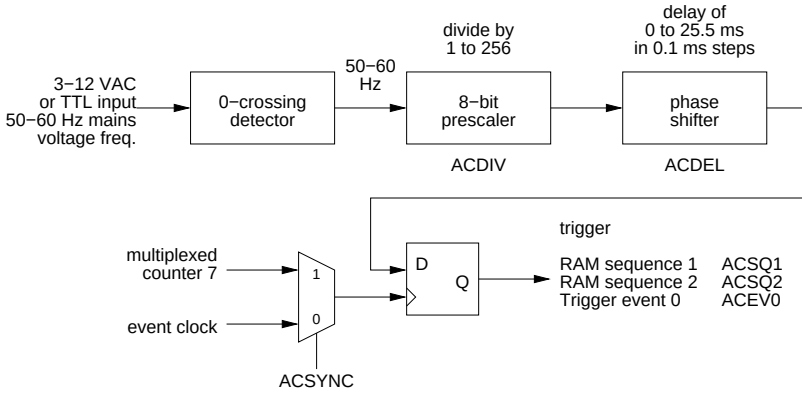

Figure 9: Mains Voltage Synchronization Logic.

The output signal of the mains voltage synchronization logic may be used to trigger an event sequence RAM or trigger event 0.

1.5. Event System - Event Receiver (EVR)

Event Receivers recover the clock signal from the event stream transmitted by an Event Generator and generate an event clock that is phase locked to the Event Generator event clock and thus to the RF reference. Event Receivers convert event codes transmitted by an Event Generator to hardware outputs. They can also generate VME interrupts and store the event codes with globally distributed timestamps into FIFO memory to be read by a CPU module from the VME bus.

After recovering the event clock the Event Receiver demultiplexes the event stream to the 8-bit distributed bus and the 8-bit event code. The Event Receiver provides two mapping RAMs. While

Figure 10: Event Receiver Module

one of the RAMs is active, the other one may be modified from VME. The event code is applied to the address lines of the active mapping RAM. The 16-bit data programmed into a specific memory location pointed to by the event code determines what actions will be taken. In addition to the mapping RAMs each of bit 0 to 6 of the event code may generate a trigger event which is a pulse with the length of a single event cycle. There are also a few special event codes to reset prescaler outputs, control the timestamp event counter and reset the heartbeat timeout counter.

A heartbeat monitor is provided to receive heartbeat events (event code 0x7A). The heartbeat counter is reset upon receiving the heartbeat event code. If no heartbeat is received the counter times out (approx. 1.6 s) and a heartbeat flag is set. The Event Receiver may be programmed to generate a heartbeat interrupt.

1.5.1. Global Timebase with Timestamp Events

The Event System provides a global timebase to attach timestamps to collected data and performed actions. The timestamping system consists of a 32-bit timestamp event counter which either counts received timestamp counter clock events or runs freely with a clock derived from the event clock. The timestamp event counter is cleared upon receiving a timestamp event counter reset event.

The timestamp event counter contents may be latched into a timestamp latch. Latching is determined by the active event map RAM and may be enabled for any event code.

1.5.2. Event FIFO

An event FIFO memory is implemented to store selected event codes with attached timing information. The 32-bit wide FIFO can hold up to 511 events. The recorded event is stored along with 24 least significant bits of the timestamp event counter contents at the time of reception. The event FIFO as well as the timestamp counter and latch are accessible from VME.

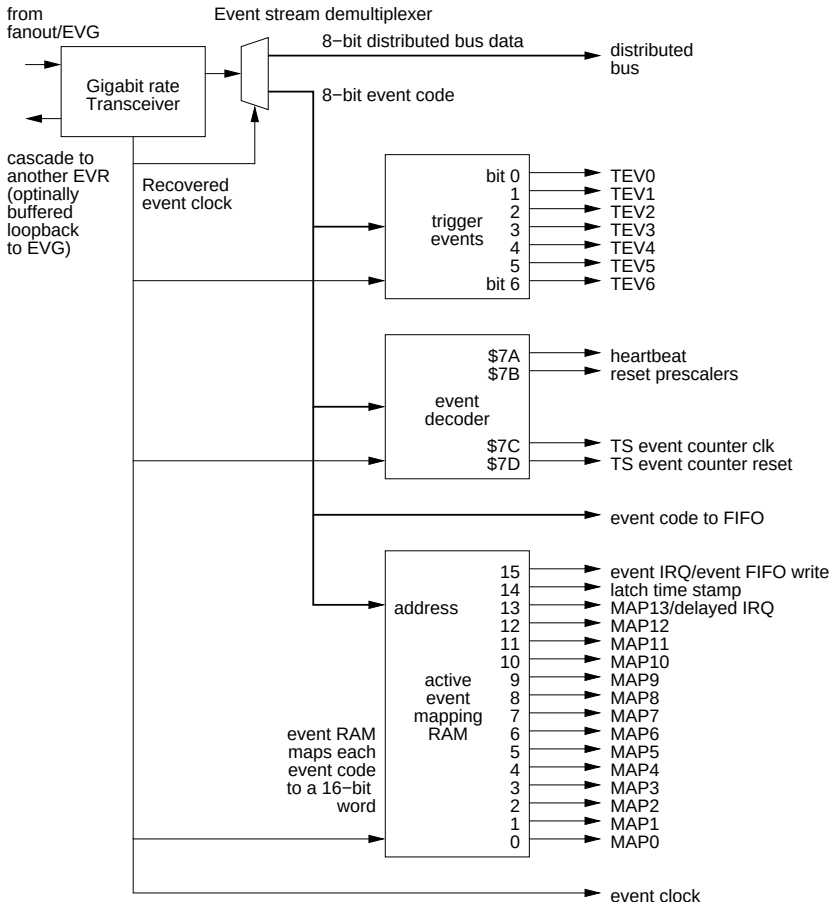

Figure 11: Event Receiver Event Decoding.

1.5.3. Event Receiver - Hardware Outputs

The Event Receiver can generate up to 32 simultanous outputs on the VME P2 connector. Transition modules provide NIM/TTL and optical outputs. The outputs may be selected from multiple sources. There are also a few outputs available in the front panel.

1.5.4. Pulse Outputs of Programmable Width

There are fourteen pulse outputs of programmable width and polarity. The pulse width may be adjusted independently from 1 to 32768 event cycles. Eight pulse outputs share the output pin with the distributed bus signals. The source of each of the shared pins may be selected independently.

1.5.5. Set/Reset Flip Flop Outputs

Flip flop outputs may be programmed to change their state on desired event codes.

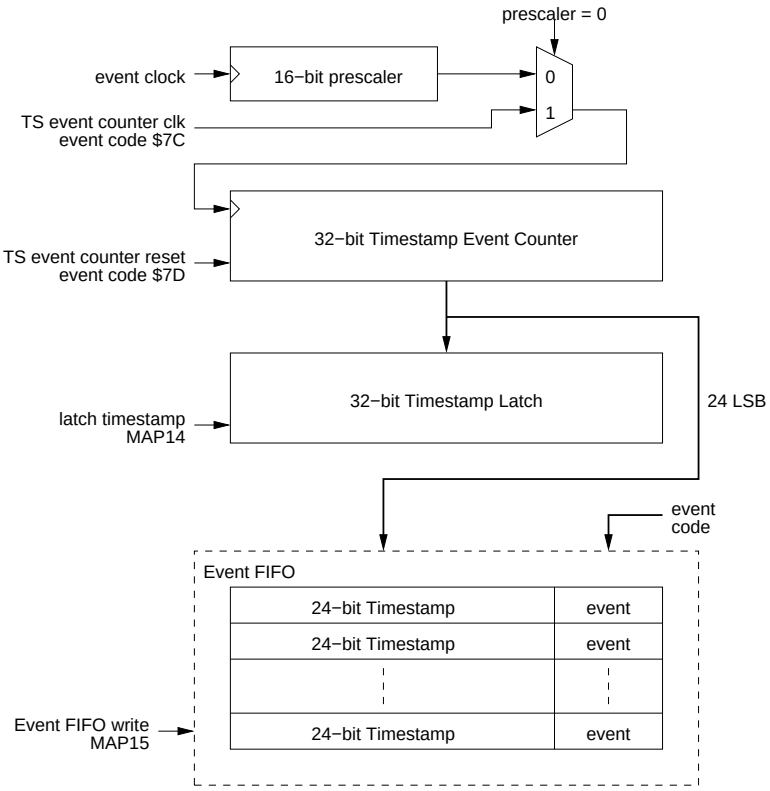

Figure 12: Event FIFO and Timestamps.

1.5.6. Delayed Pulse Outputs

Four delayed pulse outputs provide programmable delay, width and polarity. The delay and width counters share a 16-bit programmable prescaler which generates counting frequencies from event clock/65536 to the event clock rate. The delay and width counters both are 16-bit wide.

1.5.7. Trigger Event Outputs

Bits 0 to 6 of the received event code may be used to generate trigger event outputs. The width of a trigger event is one event clock cycle.

1.5.8. Front Panel Prescaler Outputs

The Event Receiver provides three prescaler outputs. The frequencies are phase locked to the event clock. A special event code reset prescalers 0x7B causes the prescalers to be synchronously reset, so the frequency outputs will be in same phase across all event receivers.

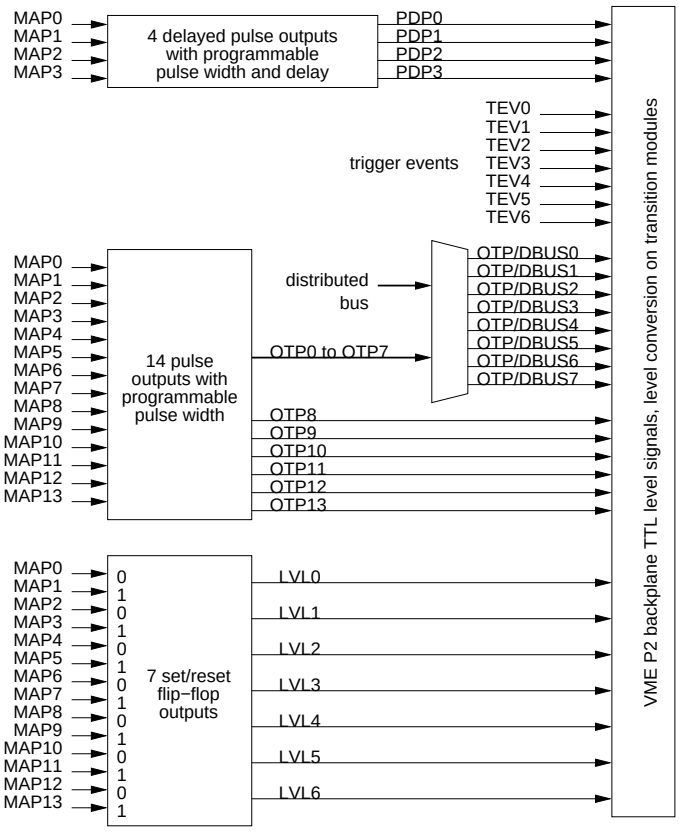

Figure 13: Event Receiver Hardware Outputs.

1.5.9. Event Receiver - VME Interrupts

The Event Receiver has multiple interrupt sources which all have their own enable and flag bits. The following events may be programmed to generate a VME interrupt:

- Receiver violation: bit error or the loss of signal.
- Lost heartbeat: heartbeat monitor timeout.
- Write operation of an event to the event FIFO.
- Event FIFO is full.

1.5.10. Delayed interrupt

In addition to the events listed above a delayed interrupt is provided. The delayed interrupt is triggered by event map RAM bit 13. A 16-bit prescaler running with the event clock frequency and a 16-bit delay counter determine the interrupt delay.

2. Event Generator Details

2.1. Event Clock

All operations on the event generator are synchronized to the event clock which is derived from an externally provided clock reference. For laboratory testing purposes an on board oscillator may be used. The front panel RF input is 50 ohm terminated and AC coupled to an PECL logic input, so an ECL level clock signal or a sine-wave signal with level of around +10 dBm should be enough.

The externally provided reference clock is divided by 10 to generate the event clock. In future versions (Event System Series 200) there will be different divider combinations available.

The fiber optic link bit rate is determined by the event clock rate. The link operates synchronous to the event clock (and RF clock) with a bit rate of 20 times the event clock rate. If the RF clock frequence is for example 500 MHz, the event clock frequency is 50 MHz and the fiber optic link bit rate is 1 Gbit/s.

2.2. Event Generation

There are several sources of events: trigger events, sequence RAM events, VME events and events received from an upstream Event Generator. Events from different sources have different priority which is resolved in a priority encoder.

2.2.1. Trigger Events

There are eight trigger event sources that send out an event code on a stimulus. Each trigger event has its own programmable event code register and various enable bits. The event code transmitted is determined by contents of the corresponding event code register. The stimulus may be a detected rising edge on an external signal or a rising edge of a multiplexed counter output.

Trigger Event 0 has also the option of being triggered by a rising edge of the AC mains voltage synchronization logic output signal.

The external input accept TTL level signals. The input logic is edge sensitive and the signals are synchronized internally to the event clock.

2.2.1.1. Configuration Bits and Registers

address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
0x02	DBUS		SSEQ1	SSEQ2	CMODE	ENEV7	ENEV6	ENEV5

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x03	ENEV4	ENEV3	ENEV2	ENEV1	ENEV0	ENSQ1	ENSQ2	ENVME

Bit	Function
ENEVx	Master enable for trigger event x.

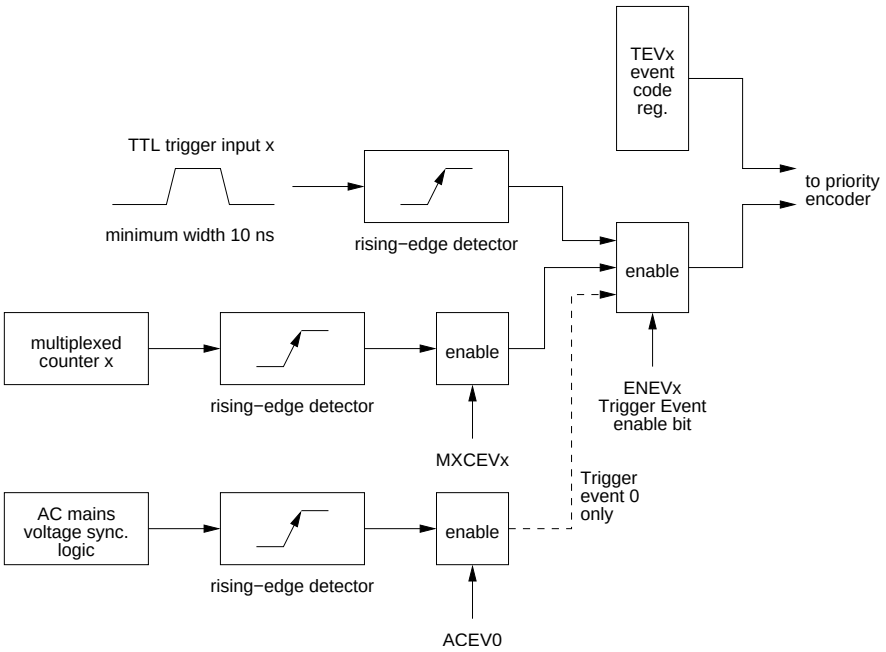

Figure 14: Trigger Event Generation

address bit 7 bit 6 bit 5 bit 4 bit 3 bit 2 bit 1 bit 0

`0x0f` Trigger Event 0 Mapping Register (TEV0)

address bit 7 bit 6 bit 5 bit 4 bit 3 bit 2 bit 1 bit 0

`0x11` Trigger Event 1 Mapping Register (TEV1)

address bit 7 bit 6 bit 5 bit 4 bit 3 bit 2 bit 1 bit 0

`0x13` Trigger Event 2 Mapping Register (TEV2)

address bit 7 bit 6 bit 5 bit 4 bit 3 bit 2 bit 1 bit 0

`0x15` Trigger Event 3 Mapping Register (TEV3)

address bit 7 bit 6 bit 5 bit 4 bit 3 bit 2 bit 1 bit 0

`0x17` Trigger Event 4 Mapping Register (TEV4)

address bit 7 bit 6 bit 5 bit 4 bit 3 bit 2 bit 1 bit 0

`0x19` Trigger Event 5 Mapping Register (TEV5)

address bit 7 bit 6 bit 5 bit 4 bit 3 bit 2 bit 1 bit 0

`0x1b` Trigger Event 6 Mapping Register (TEV6)

address bit 7 bit 6 bit 5 bit 4 bit 3 bit 2 bit 1 bit 0

`0x1d` Trigger Event 7 Mapping Register (TEV7)

address bit 7 bit 6 bit 5 bit 4 bit 3 bit 2 bit 1 bit 0

`0x1f`

MXEV7	MXEV6	MXEV5	MXEV4	MXEV3	MXEV2	MXEV1	MXEV0

Bit	Function
MXEVx	Enable multiplexed counter output x to generate trigger events.

address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
0x28	ACSQ2	ACSQ1	ACEV0	ACSYNC				DLYSEL

Bit	Function
ACEV0	Enable AC mains voltage synchronization logic output to generate trigger event 0.

2.2.2. VME Software Events

Event codes may bu sent by software access simply by enabling VME events (bit ENVME in Event Enable Register) and writing the event code to be transmitted to the VME Event register. The event is transmitted immediately unless there are higher priority events pending. If there are higher priority events the transfer is delayed until all higher priority events have been transmitted.

2.2.2.1. Configuration Bits and Registers

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x03	ENEV4	ENEV3	ENEV2	ENEV1	ENEV0	ENSQ1	ENSQ2	ENVME

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x04	VME Event Register (write only)							

2.2.3. Upstream EVG Events

Event Generators may be cascaded. The event generator receiver includes a first-in-first-out (FIFO) memory to synchronize incoming events which may be synchronized to a clock unrelated to the event clock. Usually there are no events in the FIFO. An event code from an upstream EVG is transmitted as soon as there is no other event code to be transmitted.

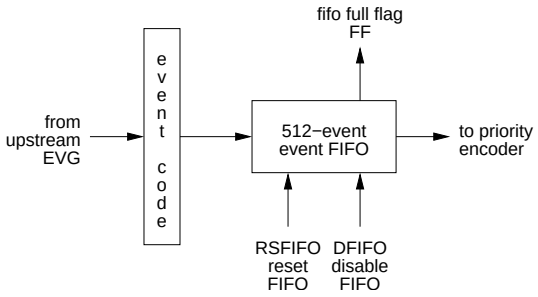

Figure 15: Upstream EVG Event FIFO

2.2.3.1. Configuration Bits and Registers

address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
0x00	MSDIS	FF	RSFIFO	DFIFO	ERRLD	AUTO1	AUTO2	VTRG1

Bit	Function
FF	FIFO full flag, write 1 to clear.
RSFIFO	Reset FIFO, write 1 to reset FIFO. The FIFO has to be disabled prior to reseting.
DFIFO	Disable FIFO/receiver, write 1 to disable upstream receiver, this disabled reception and retransmission of event codes from an upstream EVG.
ERRLD	Controls the front panel ERROR-led when the upstream receiver is disabled.

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x01	VTRG2	RCYL1	RCYL2	NFR1	NFR2	SEQ1	SEQ2	RXVIO

Bit	Function
RXVIO	Receiver violation flag, write 1 to clear flag.

2.3. Sequence RAMs

Event sequence RAMs provide a method of transmitting or playing back sequences of events stored in random access memory. There are two sequence RAMs allowing altering the contents of the first one while the other one is used for playback.

Both RAMs are 512 kbyte RAMs which allows storing for example events for one injection cycle of a synchrotron light source. In future versions larger RAMs will be supported.

2.3.1. Sequence RAM VME access

The contents of a sequence RAM may be altered only when the sequence is offline. The sequence RAMs are independent which allows modifying the contents of one RAM while the other one is used for sending events.

The sequence RAM is addressed indirectly: there are separate registers for address and data and some configuration bits to make access easier i.e. to clear the whole RAM and access consecutive memory locations automatically without supplying a new address.

Prior to accessing a sequence RAM it has to be disabled. This can be done by writing a 1 to the SEQx bit of the control register. In addition to disabling the RAM the RAM address is cleared, too.

The RAM may be access randomly by writing the address of the access to the RAM address register. Note that there are two registers, one for lower 16 bits and another for the upper bits. RAM data of the current memory location is accessible in the RAM data registers.

When the autoincrement configuration bit is set the address of the sequence RAM is incremented automatically after a read or write access from VME, otherwise the address remains unchanged.

Null filling (clearing) the RAM can be initiated by writing a 1 to the null fill configuration bit NFRx. This starts null filling the RAM from the current address up to the end of RAM. If the whole RAM is to be cleared the RAM address has to be cleared first. During null filling the NFRx

bit remains active. When null filling is completed the bit is reset. The RAM is unaccessible during null fill.

2.3.1.1. Configuration Bits and Registers

address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
0x00	MSDIS	FF	RSFIFO	DFIFO	ERRLD	AUTO1	AUTO2	VTRG1

Bit	Function
AUTO1	Auto increment sequence RAM 1.
AUTO2	Auto increment sequence RAM 2.

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x01	VTRG2	RCYL1	RCYL2	NFR1	NFR2	SEQ1	SEQ2	RXVIO

Bit	Function
NFR1	Write 1 to null fill sequence RAM 1.
NFR2	Write 1 to null fill sequence RAM 2.
SEQ1	Write 1 to disable sequence RAM 1 and reset address.
SEQ2	Write 1 to disable sequence RAM 2 and reset address.

address	bit 15							bit 0
0x06	Sequence RAM 2 address register (bits 15 - 0)							

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x09	Sequence RAM 2 data register							

address	bit 15							bit 0
0x0a	Sequence RAM 1 address register (bits 15 - 0)							

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x0d	Sequence RAM 1 data register							

address	bit 15							bit 0
0x20	Sequence RAM 1 address register (bits 18 - 16)							

address	bit 15							bit 0
0x22	Sequence RAM 2 address register (bits 18 - 16)							

2.3.2. Sequence RAM Clock

The sequence RAM clock may be selected to be applied externally or downconverted directly from the event clock with a 16-bit prescaler. The clock is selected by a 16-bit prescaler that counts from the prescaler register value down to zero. If the register value is zero an externally supplied clock is used.

Sequence RAMs have been designed for operation with a maximum frequency of 8 MHz. Both sequence RAMs have their own prescalers, but with configuration bit CMODE, sequence RAM 2 may be forced to use the same clock, trigger and reset signals as sequence RAM 1.

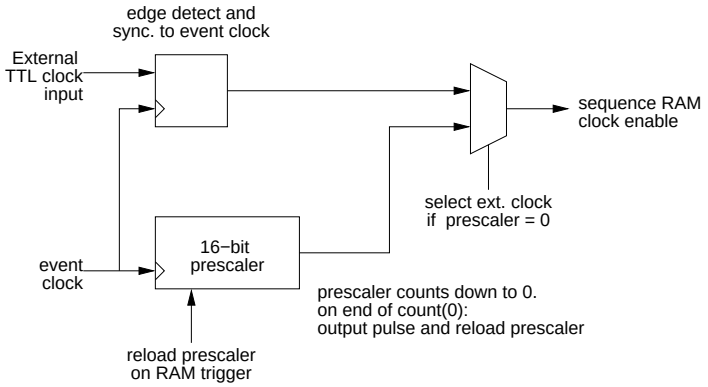

Figure 16: Sequence RAM clock

2.3.2.1. Configuration Bits and Registers

address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
0x02	DBUS		SSEQ1	SSEQ2	CMODE	ENEV7	ENEV6	ENEV5

Bit	Function
CMODE	Select RAM 1 control signals for RAM 2

address	bit 15	bit 0
0x24	Sequence RAM 1 prescaler register	

address	bit 15	bit 0
0x26	Sequence RAM 2 prescaler register	

2.3.3. Sequence RAM Trigger

Sequence RAMs may be triggered from several sources including hardware triggering from external TTL input, software triggering by VME access, triggering on a multiplexed counter output or AC mains voltage synchronization logic output. Figure 17 represents the sequence RAM triggering logic.

2.3.3.1. Configuration Bits and Registers

address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
0x02	DBUS		SSEQ1	SSEQ2	CMODE	ENEV7	ENEV6	ENEV5

Bit	Function
CMODE	Select RAM 1 control signals for RAM 2

address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
0x28	ACSQ2	ACSQ1	ACEV0	ACSYNC				DLYSEL

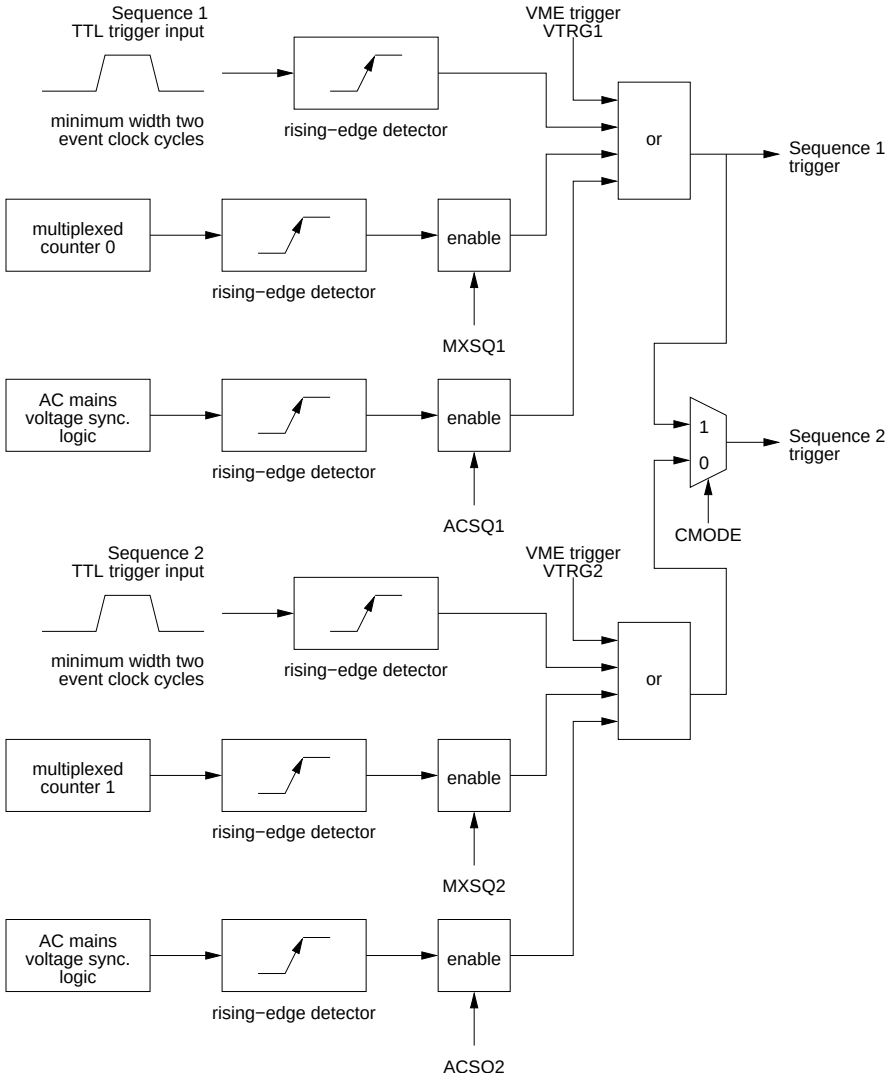

Figure 17: Sequence RAM trigger

Bit	Function
ACSQ1	Enable AC mains voltage synchronization logic output to trigger sequence RAM 1. (Note! Sequence RAM 2 triggered if CMODE is 1)
ACSQ2	Enable AC mains voltage synchronization logic output to trigger sequence RAM 2. (Note! Only when CMODE is 0)

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x2b	MXSQ2	MXSQ1			MXHSEL	MXSEL2	MXSEL1	MXSEL0

Bit	Function
MXSQ1	Enable multiplexed counter 0 output to trigger sequence RAM 1. (Note! Sequence RAM 2 triggered if CMODE is 1)
MXSQ2	Enable multiplexed counter 1 output to trigger sequence RAM 2. (Note! Only when CMODE is 0)

2.3.4. Sequence RAM Operation

Sequence RAMs are enabled by setting bit ENSQx in the Event Enable Register. The RAMs may be disabled any time by clearing the corresponding bits. Disabling sequence RAMs does not reset the address register. By setting the bit SEQx in the Control Register the sequence RAM is both disabled and the RAM address is reset. Accessing sequence RAM is only allowed when disabled.

Once enabled and triggered the sequence RAM is stepped through with a rate defined by the sequence RAM clock generator. Event codes at consecutive memory locations are sent out when clock enable is active. There are three special event codes, null (0x00), freeze sequence (0x7e) and end sequence (0x7f) event code which are not transmitted. The sequence RAM state diagram represented in figure 18. The freeze event code stops the RAM sequence until the sequence is triggered again. The end sequence code resets the sequence RAM address and depending on configuration bits, disabled the sequence RAM (single sequence, SSEQx=1) or restarts the sequence either immediately (recycle sequence, RCYLx=1) or waiting for trigger (RCYLx=0).

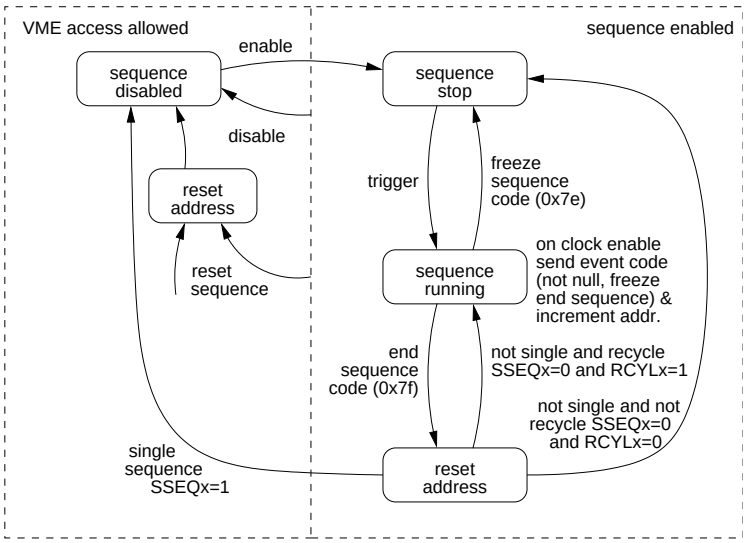

Figure 18: Sequence RAM State Diagram

2.3.4.1. Configuration Bits and Registers

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x01	VTRG2	RCYL1	RCYL2	NFR1	NFR2	SEQ1	SEQ2	RXVIO

Bit	Function
SEQ1	Write 1 to disable sequence RAM 1 and reset address.
SEQ2	Write 1 to disable sequence RAM 2 and reset address.

address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
0x02	DBUS		SSEQ1	SSEQ2	CMODE	ENEV7	ENEV6	ENEV5

Bit	Function
SSEQ1	Sequence RAM 1 Single Sequence Mode
SSEQ2	Sequence RAM 2 Single Sequence Mode

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x03	ENEV4	ENEV3	ENEV2	ENEV1	ENEV0	ENSQ1	ENSQ2	ENVME

Bit	Function
ENSQ1	Sequence RAM 1 Enable/Disable Sequence
ENSQ2	Sequence RAM 2 Enable/Disable Sequence

2.4. Distributed Bus

The bits of the distributed bus are sampled at the event rate from external signals, alternatively the distributed bus signals may be generated by multiplexed counter outputs. If there as an upstream EVG, the state of all distributed bus bits may be forwarded by the EVG.

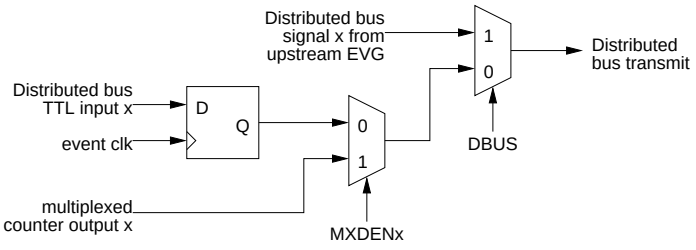

Figure 19: Distributed Bus Bit Mapping

2.4.0.2. Configuration Bits and Registers

address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
0x02	DBUS		SSEQ1	SSEQ2	CMODE	ENEV7	ENEV6	ENEV5

Bit	Function
DBUS	When set, distributed bus state of upstream EVG is forwarded.

address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
0x1e	MXDB7	MXDB6	MXDB5	MXDB4	MXDB3	MXDB2	MXDB1	MXDB0

Bit	Function
MXDBx	When set, map multiplexed counter output x to distributed bus bit x.

2.5. Multiplexed Counters

Eight 32-bit multiplexed counters generate clock signals with programmable frequencies from event clock/2^32+1 to event clock/2. Even divisors create 50% duty cycle signals. The counter outputs may be programmed to trigger events, drive distributed bus signals and trigger sequence RAMs. The output of multiplexed counter 7 is hard-wired to the mains voltage synchronization logic.

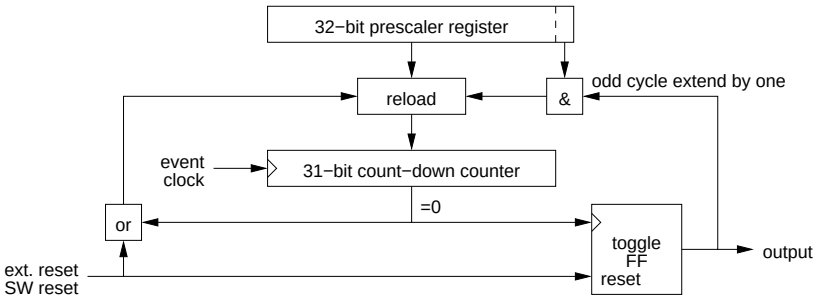

Figure 20: Multiplexed Counter

Each multiplexed counter consists of a 32-bit prescaler register and a 31-bit count-down counter which runs at the event clock rate. When count reaches zero, the output of a toggle flip-flop changes and the counter is reloaded from the prescaler register. If the least significant bit of the prescaler register is one, all odd cycles are extended by one clock cycle to support odd dividers.

The multiplexed counter prescalers are accessed through a 16-bit register. Select register bits MXHSEL and MXSEL2-0 determine which counter 0-7 and which word (MXHSEL = 0, lower) is selected.

2.5.0.3. Configuration Bits and Registers

address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
0x2a	MXRS7	MXRS6	MXRS5	MXRS4	MXRS3	MXRS2	MXRS1	MXRS0

Bit	Function
MXRSx	Write 1 to reset multiplexed counter x.

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x2b	MXSQ2	MXSQ1			MXHSEL	MXSEL2	MXSEL1	MXSEL0

Bit	Function
MXHSEL	Multiplexed counter select prescaler high word
MXSEL2-0	Multiplexed counter select resgiter

address	bit 15	bit 0
0x2c	Multiplexed counter prescaler data register.	

2.6. Mains Voltage Synchronization Logic

The Event Generator provides synchronization to the mains voltage frequency. The mains voltage frequency is divided by an eight bit programmable divider. The output of the divider may be delayed by 0 to 25.5 ms by a phase shifter in 0.1 ms steps to be able to adjust the triggering position relative to mains voltage phase. After this the signal synchronized to the event clock or the output of multiplexed counter 7.

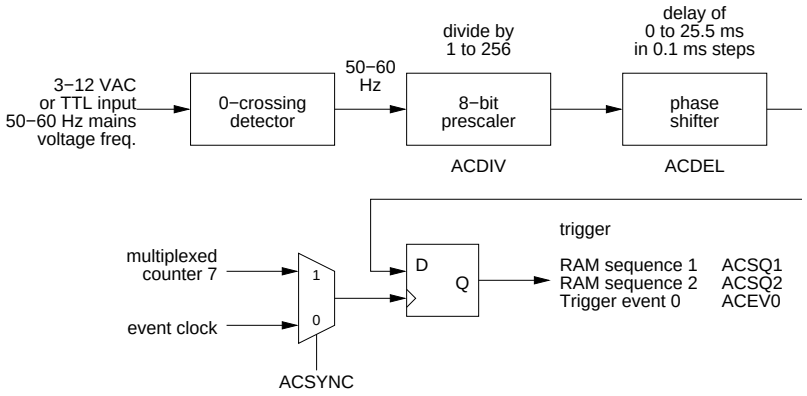

Figure 21: Mains Voltage Synchronization Logic.

AC input delay register is accessible when bit DLYSEL of the AC input enable register (0x28) is set. Note, this bit has to be changed by writing a byte only to address 0x28 (no simultaneous write to byte address 0x29 is allowed).

2.6.0.4. Configuration Bits and Registers

address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
0x28	ACSQ2	ACSQ1	ACEV0	ACSYNC				DLYSEL

Bit	Function
ACSYNC	Synchronization select (0 = event clock, 1 = multiplexed counter 7 output)
DLYSEL	AC data register select bit, 0 for divider, 1 for delay.

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x29	AC input divider (DLYSEL=0), delay (DLYSEL=1)							

2.7. I/O Connections and Front Panel

2.7.0.5. VME P2 I/O Pin Assignment

Pin	Signal
A1	EVG interface key pin (connected to ground for EVG interface)
A2	EVR interface key pin (connected to ground for EVR interface)
A3-A26	ground
A27-A32	+5V
C1	external event trigger input 0
C2	external event trigger input 1
C3	external event trigger input 2
C4	external event trigger input 3
C5	external event trigger input 4
C6	external event trigger input 5
C7	external event trigger input 6
C8	external event trigger input 7
C9	sequence RAM 1 clock
C10	sequence RAM 1 trigger
C11	sequence RAM 1 reset
C12	sequence RAM 2 clock
C13	sequence RAM 2 trigger
C14	sequence RAM 2 reset
C15	(reserved input)
C16	(reserved input)
C17	multiplexed counter 0 reset
C18	multiplexed counter 1 reset
C19	multiplexed counter 2 reset
C20	multiplexed counter 3 reset
C21	multiplexed counter 4 reset
C22	multiplexed counter 5 reset
C23	multiplexed counter 6 reset
C24	multiplexed counter 7 reset
C25	distributed bus input 0
C26	distributed bus input 1
C27	distributed bus input 2
C28	distributed bus input 3
C29	distributed bus input 4
C30	distributed bus input 5
C31	distributed bus input 6
C32	distributed bus input 7

2.7.0.6. VME A16 Address Select

Two rotary hexadecimal switches in the front panel select the VME A16 I/O address of the EVG module. The upper switch represents A16 address bits 15-12 and the lower one bits 11-8.

The rotary switched will be obsoleted in future version when the module is VME64x compatible.

2.7.0.7. Front panel LEDs

There are five front panel leds that display the status of the event generator.

LED	Function
CONF	indicates that the event generator FPGA is configured properly.
ENA	indicates that the event generator is enabled (master disable MSDIS = 0)
LINK	indicates that the link to an upstream EVG is established
EVENT	flashes when an event code is transmitted
ERROR	indicates a upstream link error or ERRLD state if receiver is disabled

2.7.0.8. AC input

A 3-12 VAC signal may be applied for AC synchronization. Connector style is Lemo EPL.00.

2.7.0.9. Fiber optic transceiver

Duplex SC connectors for two multimode fibers are provided. TX is for transmit side, to fanout or event receiver. RX is for receiver side, from an upstream event generator.

2.7.0.10. RF Clock input

The front panel RF input is 50 ohm terminated and AC coupled to an PECL logic input, so an ECL level clock signal or a sine-wave signal with level of around +10 dBm should be enough. Connector style is Lemo EPL.00.

2.8. Register Reference

2.8.0.11. Control and Status Register

address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
0x00	MSDIS	FF	RSFIFO	DFIFO	ERRLD	AUTO1	AUTO2	VTRG1

Bit	Function
FF	FIFO full flag, write 1 to clear.
RSFIFO	Reset FIFO, write 1 to reset FIFO. The FIFO has to be disabled prior to reseting.
DFIFO	Disable FIFO/receiver, write 1 to disable upstream receiver, this disabled reception and retransmission of event codes from an upstream EVG.
ERRLD	Controls the front panel ERROR-led when the upstream receiver is disabled.
AUTO1	Auto increment sequence RAM 1.
AUTO2	Auto increment sequence RAM 2.

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x01	VTRG2	RCYL1	RCYL2	NFR1	NFR2	SEQ1	SEQ2	RXVIO

Bit	Function
NFR1	Write 1 to null fill sequence RAM 1.
NFR2	Write 1 to null fill sequence RAM 2.
SEQ1	Write 1 to disable sequence RAM 1 and reset address.
SEQ2	Write 1 to disable sequence RAM 2 and reset address.
RXVIO	Receiver violation flag, write 1 to clear flag.

2.8.0.12. Event enable register

address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
0x02	DBUS		SSEQ1	SSEQ2	CMODE	ENEV7	ENEV6	ENEV5

Bit	Function
DBUS	When set, distributed bus state of upstream EVG is forwarded.
SSEQ1	Sequence RAM 1 Single Sequence Mode
SSEQ2	Sequence RAM 2 Single Sequence Mode
CMODE	Select RAM 1 control signals for RAM 2
ENEVx	Master enable for trigger event x.

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x03	ENEV4	ENEV3	ENEV2	ENEV1	ENEV0	ENSQ1	ENSQ2	ENVME

Bit	Function
ENEVx	Master enable for trigger event x.
ENSQ1	Sequence RAM 1 Enable/Disable Sequence
ENSQ2	Sequence RAM 2 Enable/Disable Sequence
ENVME	Enable VME Events.

2.8.0.13. VME event register (write only)

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x05	VME event register (write only)							

2.8.0.14. Distributed bus data register (read only)

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x05	Distributed bus data register (read only)							

2.8.0.15. Sequence RAM 2 address register (low)

address	bit 15							bit 0
0x06	Sequence RAM 2 address register (bits 15 - 0)							

2.8.0.16. Sequence RAM 2 data register

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x09	Sequence RAM 2 data register							

2.8.0.17. Sequence RAM 1 address register (low)

address	bit 15							bit 0
0x0a	Sequence RAM 1 address register (bits 15 - 0)							

2.8.0.18. Sequence RAM 1 data register

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x0d	Sequence RAM 1 data register							

2.8.0.19. Trigger event 0 mapping register

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x0f	Trigger Event 0 Mapping Register (TEV0)							

2.8.0.20. Trigger event 1 mapping register

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x11	Trigger Event 1 Mapping Register (TEV1)							

2.8.0.21. Trigger event 2 mapping register

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x13	Trigger Event 2 Mapping Register (TEV2)							

2.8.0.22. Trigger event 3 mapping register

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x15	Trigger Event 3 Mapping Register (TEV3)							

2.8.0.23. Trigger event 4 mapping register

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x17	Trigger Event 4 Mapping Register (TEV4)							

2.8.0.24. Trigger event 5 mapping register

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x19	Trigger Event 5 Mapping Register (TEV5)							

2.8.0.25. Trigger event 6 mapping register

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x1b	Trigger Event 6 Mapping Register (TEV7)							

2.8.0.26. Trigger event 7 mapping register

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x1d	Trigger Event 7 Mapping Register (TEV7)							

2.8.0.27. Multiplexed counter distributed bus enable register

address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
0x1e	MXDB7	MXDB6	MXDB5	MXDB4	MXDB3	MXDB2	MXDB1	MXDB0

Bit	Function
MXDBx	When set, map multiplexed counter output x to distributed bus bit x.

2.8.0.28. Multiplexed counter trigger event enable register

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x1f	MXEV7	MXEV6	MXEV5	MXEV4	MXEV3	MXEV2	MXEV1	MXEV0

Bit	Function
MXEVx	Enable multiplexed counter output x to generate trigger events.

2.8.0.29. Sequence RAM 1 address register (high)

address	bit 15	bit 0
0x20	Sequence RAM 1 address register (bits 18 - 16)	

2.8.0.30. Sequence RAM 2 address register (high)

address	bit 15	bit 0
0x22	Sequence RAM 2 address register (bits 18 - 16)	

2.8.0.31. Sequence RAM 1 clock select register

address	bit 15	bit 0
0x24	Sequence RAM 1 prescaler register	

2.8.0.32. Sequence RAM 2 clock select register

address	bit 15	bit 0
0x26	Sequence RAM 2 prescaler register	

2.8.0.33. AC input control register

address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
0x28	ACSQ2	ACSQ1	ACEV0	ACSYNC				DLYSEL

Bit	Function
ACSQ1	Enable AC mains voltage synchronization logic output to trigger sequence RAM 1. (Note! Sequence RAM 2 triggered if CMODE is 1)
ACSQ2	Enable AC mains voltage synchronization logic output to trigger sequence RAM 2. (Note! Only when CMODE is 0)
ACEV0	Enable AC mains voltage synchronization logic output to generate trigger event 0.
ACSYNC	Synchronization select (0 = event clock, 1 = multiplexed counter 7 output)
DLYSEL	AC data register select bit, 0 for divider, 1 for delay.

2.8.0.34. AC input data register

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x29	AC input divider (DLYSEL=0), delay (DLYSEL=1)							

2.8.0.35. Multiplexed counter reset register

address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
0x2a	MXRS7	MXRS6	MXRS5	MXRS4	MXRS3	MXRS2	MXRS1	MXRS0

Bit	Function
MXRSx	Write 1 to reset multiplexed counter x.

2.8.0.36. Multiplexed counter control register

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x2b	MXSQ2	MXSQ1			MXHSEL	MXSEL2	MXSEL1	MXSEL0

Bit	Function
MXSQ1	Enable multiplexed counter 0 output to trigger sequence RAM 1. (Note! Sequence RAM 2 triggered if CMODE is 1)
MXSQ2	Enable multiplexed counter 1 output to trigger sequence RAM 2. (Note! Only when CMODE is 0)
MXHSEL	Multiplexed counter select prescaler high word
MXSEL2-0	Multiplexed counter select resgiter

2.8.0.37. Multiplexed counter prescaler register

address	bit 15	bit 0
0x2c	Multiplexed counter prescaler register	

2.8.0.38. FPGA version register

address	bit 15	bit 0
0x2e	FPGA version register	

2.8.0.39. Extension control/status register

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x31	RESET	CONF	IFCG	IFCR				

Bit	Function
RESET	Writing a 1 to this bit reset the event generator. FPGA configuration is (re)loaded from flash memory.
CONF	writing a 1 to this bit initializes the virtex for reconfiguration. If this bit is set when reading the status register, the virtex device has been configured properly.
IFCG	a 1 indicates that an event generator interface card is plugged in to the P2 connector.
IFCR	a 1 indicates that an event receiver interface card is plugged in to the P2 connector.

2.8.0.40. FPGA programming data register

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x33	FPGA programming data register							

2.8.0.41. Flash address register (bits 20-16)

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x39	Flash address register (bits 20-16)							

2.8.0.42. Flash address register (bits 15-8)

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x3b	Flash address register (bits 15-8)							

2.8.0.43. Flash address register (bits 7-0)

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x3d	Flash address register (bits 7-0)							

2.8.0.44. Flash data register

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x3d	Flash data register (bits 7-0)							

3. Event Receiver Details

3.1. Mapping RAMs

Mapping RAMs are 256 * 16 bit RAMs that map an eight bit event code at the event clock rate to 16 MAP bits that determine what actions will be taken. There are two RAMs of which one may be active at a time. Both RAMs are based on dual port memories and may be modified at any time.

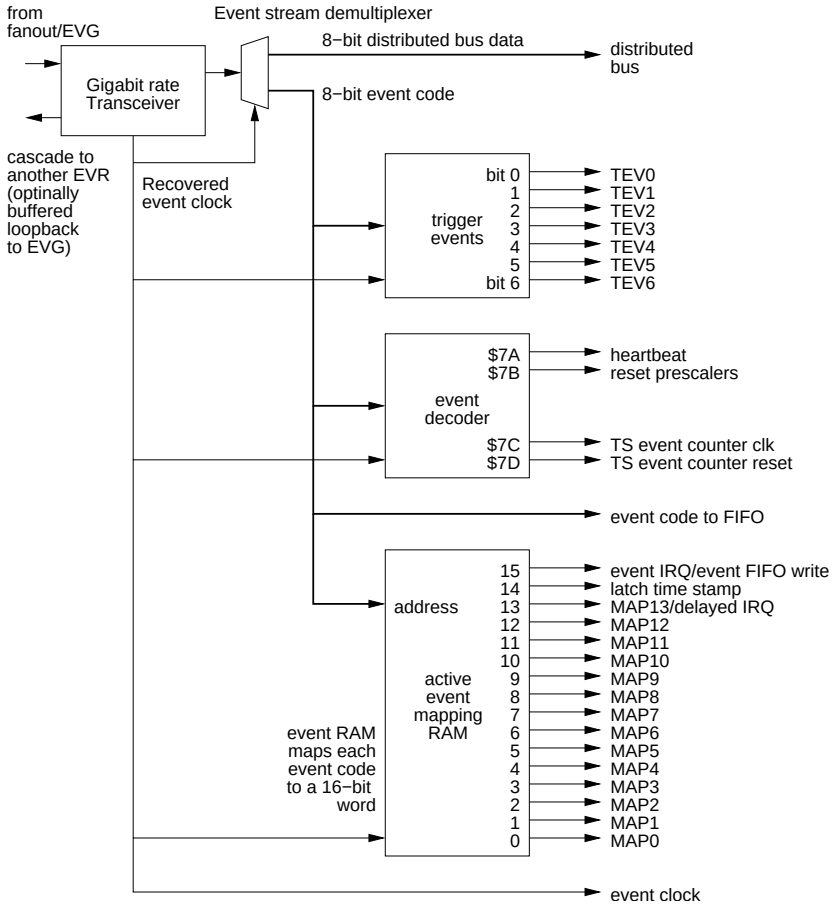

Figure 22: Event Receiver Event Decoding.

3.1.1. Mapping RAM VME access

The mapping RAMs are addressed indirectly: there are separate registers for address and data and some configuration bits to make access easier i.e. to clear the whole RAM and access consecutive memory locations automatically without supplying a new address. For VME access both RAMs share the same address, data etc. registers. There is one bit VMERS which determines which RAM is accessed.

address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
0x00	EVREN	IRQEN	RSTS	HRTBT	IRQFL	LTS	MAPEN	MAPRS

Bit	Function
MAPEN	Event mapping RAM enable.
MAPRS	Mapping RAM select bit for event decoding. 0 - mapping RAM 1, 1 - mapping RAM 2.

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x01	NFRAM	VMERS	AUTOI	RSADR DIRQ	RSFIFO	FF	FNE RSDIRQ	RXVIO

Bit	Function
NFRAM	Write 1 to null fill (clear) mapping RAM selected by VMERS. This bit changed to 0 when the selected RAM has been cleared.
VMERS	Mapping RAM select bit for VME access. 0 - mapping RAM 1, 1 - mapping RAM 2.
AUTOI	Enable mapping RAM auto increment mode. When set the address is automatically incremented by one upon every access from VME.
RSADR	Write 1 to reset mapping RAM address register (write only).

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x03	Mapping RAM common address register							

address	bit 15	bit 0
0x04	Mapping RAM common data register	

3.2. Programmable width pulse outputs

There are fourteen pulse outputs of programmable width and polarity. The pulse width may be adjusted independently from 1 to 32767 event cycles. Eight pulse outputs share the output pin with the distributed bus signals. The source of each of the shared pins may be selected independently.

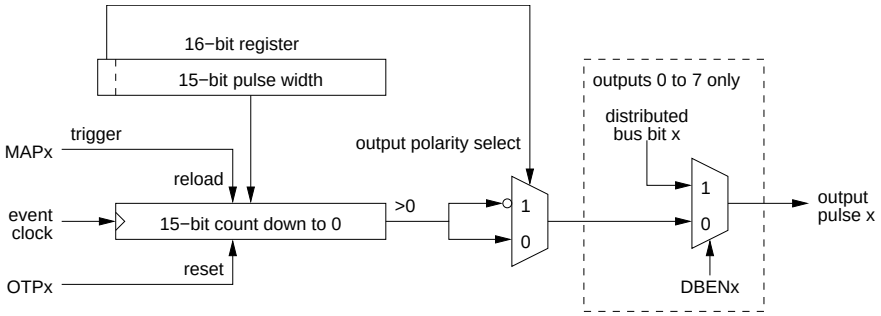

Figure 23: Programmable width pulse outputs

The pulse width registers are accessed indirectly by first selecting the register to be accessed by setting select register bits and after this the corresponding register is accessible through a common data register.

3.2.0.1. Configuration Bits and Registers

address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
0x06			OTP13	OTP12	OTP11	OTP10	OTP9	OTP8

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x07	OTP7	OTP6	OTP5	OTP4	OTP3	OTP2	OTP1	OTP0

Bit	Function
OTPx	Enable output pulse x.

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x1b				DSEL4	DSEL3	DSEL2	DSEL1	DSEL0

DSEL4-0	Register selected
10000	Programmable width pulse 0
10001	Programmable width pulse 1
10010	Programmable width pulse 2
10011	Programmable width pulse 3
10100	Programmable width pulse 4
10101	Programmable width pulse 5
10110	Programmable width pulse 6
10111	Programmable width pulse 7
11000	Programmable width pulse 8
11001	Programmable width pulse 9
11010	Programmable width pulse 10
11011	Programmable width pulse 11
11100	Programmable width pulse 12
11101	Programmable width pulse 13

address	bit 15	bit 0
0x1e	Programmable width pulse width register	

Most significant bit (bit 15) of pulse width register determines the output pulse polarity: 0 - active high, 1 - active low.

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x25	DBEN7	DBEN6	DBEN5	DBEN4	DBEN3	DBEN2	DBEN1	DBEN0

Bit	Function
DBENx	OTPx output select: 0 - programmable width pulse x, 1 - distributed bus bit x.

3.3. Set/reset flip-flop outputs

Level outputs may be programmed to change their state on specific event codes. The set and reset signals come from different mapping RAM bits.

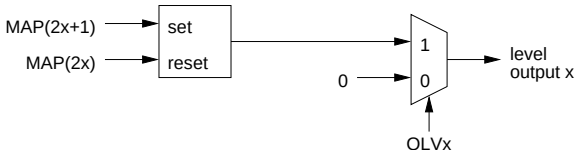

Figure 24: Level outputs

3.3.0.2. Configuration Bits and Registers

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x09		OLV6	OLV5	OLV4	OLV3	OLV2	OLV1	OLV0

Bit	Function
OLVx	Enable level output x.

3.4. Delayed pulse outputs

Four delayed pulse outputs provide programmable delay, width and polarity. The delay and width counters share a 16-bit programmable prescaler which generates counting frequencies from event clock/65536 to the event clock rate. The delay and width counters both are 16-bit wide.

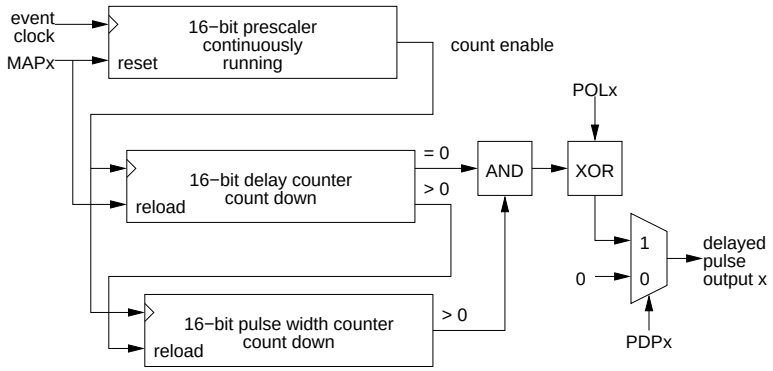

Figure 25: Delayed pulse outputs

3.4.0.3. Configuration Bits and Registers

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x19	POL3	POL2	POL1	POL0	PDP3	PDP2	PDP1	PDP0

Bit	Function
POLx	Delayed pulse output x polarity: 0 - active high, 1 - active low.
PDPx	Delayed pulse output x enable.

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x1b				DSEL4	DSEL3	DSEL2	DSEL1	DSEL0

DSEL4-0	Register selected
00000	Programmable delayed pulse 0
00001	Programmable delayed pulse 1
00010	Programmable delayed pulse 2
00011	Programmable delayed pulse 3

address	bit 15	bit 0
0x1c	Programmable delayed pulse delay register	

address	bit 15	bit 0
0x1e	Programmable delayed pulse width register	

address	bit 15	bit 0
0x28	Programmable delayed pulse prescaler register	

3.5. Trigger event outputs

Trigger event outputs map the received event code bits 0 to 6 directly to trigger event output pins if enabled. A received event code will generate a pulse on the enabled trigger event outputs. The pulse width is one event clock cycle.

3.5.0.4. Configuration Bits and Registers

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x0b	0	TEV6	TEV5	TEV4	TEV3	TEV2	TEV1	TEV0

Bit	Function
TEVx	Trigger event x output enable.

3.6. Timestamping and Event FIFO

The timestamping system consists of a 32-bit timestamp event counter and a 32-bit timestamp latch. The timestamp event counter is incremented either on a specific event code (0x7c) or with a programmable prescaler derived from the event clock. This is determined with the prescaler value:

Prescaler	Timestamp event counter clock
0x0000	Timestamp clock event (0x7c)
0x0001	Event clock / 2
0x0002	Event clock / 4
0x0003	Event clock / 6
-	-
0xffff	Event clock / 131070

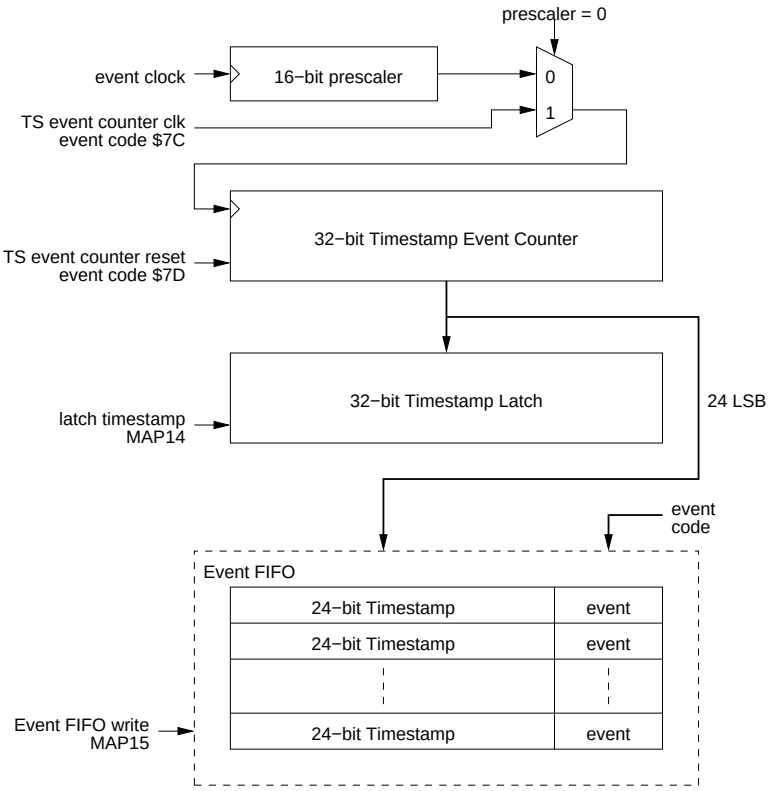

Figure 26: Event FIFO and Timestamps.

The current value of the timestamp event counter may be latched by any event code by setting the *latch timestamp* bit for the event codes in mapping RAM.

Event codes with timestamp information may be stored in an event FIFO. This is done by setting the *event FIFO write* bit for the event codes in mapping RAM.

3.6.0.5. Configuration Bits and Registers

address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
0x00	EVREN	IRQEN	RSTS	HRTBT	IRQFL	LTS	MAPEN	MAPRS

Bit	Function
RSTS	Write 1 to reset timestamp event counter and timestamp latch.
LTS	Write 1 to latch timestamp from timestamp event counter to timestamp latch.

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x01	NFRAM	VMERS	AUTOI	RSADR DIRQ	RSFIFO	FF	FNE RSDIRQ	RXVIO

Bit	Function
RSFIFO	Write 1 to clear event FIFO.
FF	Event FIFO full flag. Write 1 to reset flag.
FNE	FIFO not empty flag. Indicated whether there are event in event FIFO.

address	bit 15	bit 0
0x0c	Timestamp event counter (LSW, read only)	

address	bit 15	bit 0
0x0e	Timestamp event counter (MSW, read only)	

address	bit 15	bit 0
0x10	Timestamp event latch (LSW, read only)	

address	bit 15	bit 0
0x12	Timestamp event latch (MSW, read only)	

Note that the bus interface is 16 bits wide only and timestamp registers are volatile i.e. the contents may change between consecutive reads from the upper and lower registers.

address	bit 15	bit 0
0x14	Event FIFO data register (LSB - event code, MSB - LSB of timestamp counter)	

Note that reading from register 0x14 will automatically pop the event code and timestamp from the FIFO. When reading event codes register location 0x16 has to be read first.

address	bit 15	bit 0
0x16	Event FIFO data register (bits 23-8 of timestamp counter)	

address	bit 15	bit 0
0x2a	Timestamp counter clock prescaler register	

3.7. VME Interrupts

Interrupts may be generated from different sources. Interrupts may be generated by event codes (event interrupt, delayed interrupt), heartbeat timeout, receiver violation and when the event FIFO is full.

The heartbeat timer has a timeout of 1.6 s. The timer is reset upon reception of event code 0x7a (heartbeat event). If the heartbeat timer times out a flag is set. This flag may be enabled to generate in interrupt.

The delayed interrupt is triggered by mapping RAM bit 13 (MAP13). The delay is generated with a 16-bit delay counter which runs with a frequency determined by a 16-bit prescaler. The delay and prescaler registers are accessed similar to delayed pulse output prescaler and delay registers.

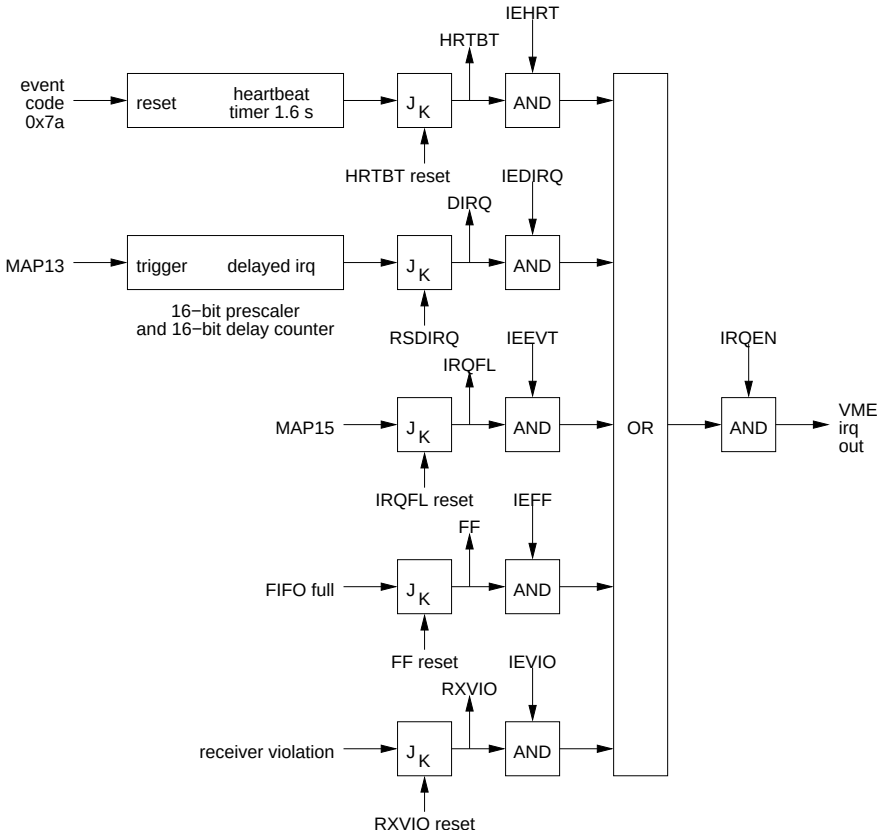

Figure 27: Event Receiver Interrupts.

Prescaler	Delay clock
0x0000	Event clock
0x0001	Event clock / 2
0x0002	Event clock / 4
0x0003	Event clock / 6
-	-
0xffff	Event clock / 131070

Delay reg.	Delay in delay clocks
0x0000	0
0x0001	1
0x0002	2
0x0003	3
-	-
0xffff	65535

3.7.0.6. Configuration Bits and Registers

address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
0x00	EVREN	IRQEN	RSTS	HRTBT	IRQFL	LTS	MAPEN	MAPRS

Bit	Function
IRQEN	VME irq enable. When 0 all interrupts are disabled.
HRTBT	Lost heartbeat flag. Write 1 to reset.
IRQFL	Event FIFO interrupt flag. Write 1 to reset.

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x01	NFRAM	VMERS	AUTOI	RSADR DIRQ	RSFIFO	FF	FNE RSDIRQ	RXVIO

Bit	Function
DIRQ	Delayed interrupt flag.
RSDIRQ	Write 1 to clear delayed interrupt flag.
RXVIO	Receiver violation flag. Write 1 to clear.

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x21	VME interrupt vector register							

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x23				IEDIRQ	IEEVT	IEHRT	IEFF	IEVIO

Bit	Function
IEDIRQ	Delayed interrupt enable.
IEEVT	Event interrupt enable.
IEHRT	Lost heartbeat interrupt enable.
IEFF	Event FIFO full interrupt enable.
IEVIO	Receiver violation interrupt enable.

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x1b				DSEL4	DSEL3	DSEL2	DSEL1	DSEL0

DSEL4-0	Register selected
00100	Delayed interrupt

address	bit 15	bit 0
0x1c	Delayed interrupt delay register	

address	bit 15	bit 0
0x28	Delayed interrupt prescaler register	

3.8. I/O Connections and Front Panel

3.8.0.7. VME P2 I/O Pin Assignment

Pin	Signal
A1	EVG interface key pin (connected to ground for EVG interface)
A2	EVR interface key pin (connected to ground for EVR interface)
A3-A26	ground
A27-A32	+5V
C1	delayed pulse output 0
C2	delayed pulse output 0
C3	delayed pulse output 0
C4	delayed pulse output 0
C5	trigger event output 0
C6	trigger event output 1
C7	trigger event output 2
C8	trigger event output 3
C9	trigger event output 4
C10	trigger event output 5
C11	trigger event output 6
C12	programmable width pulse / distributed bus output 0
C13	programmable width pulse / distributed bus output 1
C14	programmable width pulse / distributed bus output 2
C15	programmable width pulse / distributed bus output 3
C16	programmable width pulse / distributed bus output 4
C17	programmable width pulse / distributed bus output 5
C18	programmable width pulse / distributed bus output 6
C19	programmable width pulse / distributed bus output 7
C20	programmable width pulse output 8
C21	programmable width pulse output 9
C22	programmable width pulse output 10
C23	programmable width pulse output 11
C24	programmable width pulse output 12
C25	programmable width pulse output 13
C26	level output 0
C27	level output 1
C28	level output 2
C29	level output 3
C30	level output 4
C31	level output 5
C32	level output 6

3.8.0.8. VME A16 Address Select

Two rotary hexadecimal switches in the front panel select the VME A16 I/O address of the EVR module. The upper switch represents A16 address bits 15-12 and the lower one bits 11-8.

The rotary switched will be obsoleted in future version when the module is VME64x compatible.

3.8.0.9. Front panel LEDs

There are five front panel leds that display the status of the event generator.

LED	Function
CONF	indicates that the event receiver FPGA is configured properly.
ENA	indicates that the event receiver is enabled (EVREN = 1)
LINK	indicates that the link to an EVG is established
EVENT	flashes when an event code is received
ERROR	indicates a receiver link error

3.8.0.10. Front panel clock outputs

There are three clock outputs in the EVR front panel CLK1, CLK2 and CLK3. The frequencies of the clock outputs are derived from the event clock. A special event code *reset prescalers* (0x7b) may be used to synchronize the clock outputs of several EVRs. The clock output frequencies are:

output	Frequency
CLK1	event clock / 50
CLK2	event clock / 5
CLK3	event clock * 2

The outputs are TTL level. In future versions the clock outputs will be replaced by programmable outputs.

3.9. Board jumpers

There are jumpers to select VME interrupt level JP3 selects the VME interrupt request level and JP6 the VME interrupt acknowledge level.

3.10. Register Reference

3.10.0.11. Control and Status Register

address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
0x00	EVREN	IRQEN	RSTS	HRTBT	IRQFL	LTS	MAPEN	MAPRS

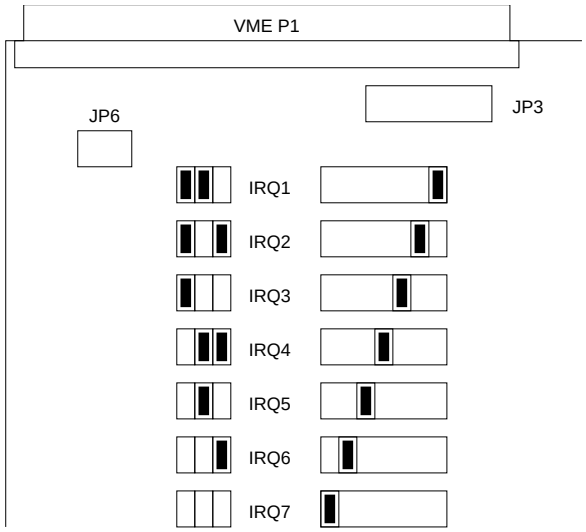

Figure 28: Event Receiver Interrupt level selection.

Bit	Function
EVREN	Event Receiver Master enable.
IRQEN	VME irq enable. When 0 all interrupts are disabled.
RSTS	Write 1 to reset timestamp event counter and timestamp latch.
HRTBT	Lost heartbeat flag. Write 1 to reset.
IRQFL	Event FIFO interrupt flag. Write 1 to reset.
LTS	Write 1 to latch timestamp from timestamp event counter to timestamp latch.
MAPEN	Event mapping RAM enable.
MAPRS	Mapping RAM select bit for event decoding. 0 - mapping RAM 1, 1 - mapping RAM 2.

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x01	NFRAM	VMERS	AUTOI	RSADR DIRQ	RSFIFO	FF	FNE RSDIRQ	RXVIO

Bit	Function
NFRAM	Write 1 to null fill (clear) mapping RAM selected by VMERS. This bit changed to 0 when the selected RAM has been cleared.
VMERS	Mapping RAM select bit for VME access. 0 - mapping RAM 1, 1 - mapping RAM 2.
AUTOI	Enable mapping RAM auto increment mode. When set the address is automatically incremented by one upon every access from VME.
RSADR	Write 1 to reset mapping RAM address register (write only).
DIRQ	Delayed interrupt flag.
RSFIFO	Write 1 to clear event FIFO.
FF	Event FIFO full flag. Write 1 to reset flag.
FNE	FIFO not empty flag. Indicated whether there are event in event FIFO.
RSDIRQ	Write 1 to clear delayed interrupt flag.
RXVIO	Receiver violation flag. Write 1 to clear.

3.10.0.12. Mapping RAM address register

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x03	Mapping RAM common address register							

3.10.0.13. Mapping RAM data register

address	bit 15	bit 0
0x04	Mapping RAM common data register	

3.10.0.14. Output pulse enable register

address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
0x06			OTP13	OTP12	OTP11	OTP10	OTP9	OTP8

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x07	OTP7	OTP6	OTP5	OTP4	OTP3	OTP2	OTP1	OTP0

Bit	Function
OTPx	Enable output pulse x.

3.10.0.15. Output level enable register

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x09		OLV6	OLV5	OLV4	OLV3	OLV2	OLV1	OLV0

Bit	Function
OLVx	Enable level output x.

3.10.0.16. Trigger event enable register

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x0b	0	TEV6	TEV5	TEV4	TEV3	TEV2	TEV1	TEV0

Bit	Function
TEVx	Trigger event x output enable.

3.10.0.17. Timestamp event counter register

address	bit 15	bit 0
0x0c	Timestamp event counter (LSW, read only)	

address	bit 15	bit 0
0x0e	Timestamp event counter (MSW, read only)	

3.10.0.18. Timestamp event latch register

address	bit 15	bit 0
0x10	Timestamp event latch (LSW, read only)	

address	bit 15	bit 0
0x12	Timestamp event latch (MSW, read only)	

3.10.0.19. Event FIFO data register

address	bit 15	bit 0
0x14	Event FIFO data register (LSB - event code, MSB - LSB of timestamp counter)	

address	bit 15	bit 0
0x16	Event FIFO data register (bits 23-8 of timestamp counter)	

3.10.0.20. Programmable delayed pulse output enable register

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x19	POL3	POL2	POL1	POL0	PDP3	PDP2	PDP1	PDP0

Bit	Function
POLx	Delayed pulse output x polarity: 0 - active high, 1 - active low.
PDPx	Delayed pulse output x enable.

3.10.0.21. Programmable pulse / delay select register

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x1b				DSEL4	DSEL3	DSEL2	DSEL1	DSEL0

DSEL4-0	Register selected
00000	Programmable delayed pulse 0
00001	Programmable delayed pulse 1
00010	Programmable delayed pulse 2
00011	Programmable delayed pulse 3
00100	Delayed interrupt
10000	Programmable width pulse 0
10001	Programmable width pulse 1
10010	Programmable width pulse 2
10011	Programmable width pulse 3
10100	Programmable width pulse 4
10101	Programmable width pulse 5
10110	Programmable width pulse 6
10111	Programmable width pulse 7
11000	Programmable width pulse 8
11001	Programmable width pulse 9
11010	Programmable width pulse 10
11011	Programmable width pulse 11
11100	Programmable width pulse 12
11101	Programmable width pulse 13

address	bit 15	bit 0
0x1c	Programmable delayed pulse delay register	

address	bit 15	bit 0
0x1e	Programmable width pulse width register	

3.10.0.22. Interrupt configuration registers

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x21	VME interrupt vector register							

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x23				IEDIRQ	IEEVT	IEHRT	IEFF	IEVIO

Bit	Function
IEDIRQ	Delayed interrupt enable.
IEEVT	Event interrupt enable.
IEHRT	Lost heartbeat interrupt enable.
IEFF	Event FIFO full interrupt enable.
IEVIO	Receiver violation interrupt enable.

3.10.0.23. Distributed bus enable register

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x25	DBEN7	DBEN6	DBEN5	DBEN4	DBEN3	DBEN2	DBEN1	DBEN0

Bit	Function
DBENx	OTPx output select: 0 - programmable width pulse x, 1 - distributed bus bit x.

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x27	Distributed bus data register (read only)							

address	bit 15	bit 0
0x28	Programmable delayed pulse prescaler register	

address	bit 15	bit 0
0x2a	Timestamp counter clock prescaler register	

3.10.0.24. FPGA version register

address	bit 15	bit 0
0x2e	FPGA version register	

3.10.0.25. Extension control/status register

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x31	RESET	CONF	IFCG	IFCR				

Bit	Function
RESET	Writing a 1 to this bit reset the event receiver. FPGA configuration is (re)loaded from flash memory.
CONF	writing a 1 to this bit initializes the virtex for reconfiguration. If this bit is set when reading the status register, the virtex device has been configured properly.
IFCG	a 1 indicates that an event generator interface card is plugged in to the P2 connector.
IFCR	a 1 indicates that an event receiver interface card is plugged in to the P2 connector.

3.10.0.26. FPGA programming data register

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x33	FPGA programming data register							

3.10.0.27. Flash address register (bits 20-16)

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x39	Flash address register (bits 20-16)							

3.10.0.28. Flash address register (bits 15-8)

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x3b	Flash address register (bits 15-8)							

3.10.0.29. Flash address register (bits 7-0)

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x3d	Flash address register (bits 7-0)							

3.10.0.30. Flash data register

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x3d	Flash data register (bits 7-0)							

4. Synchrotron Light Source Timing with Event System

A complete timing event distribution system of a synchrotron light source may be build using one Event Generator (EVG) and a number of fanout modules and Event Receivers (EVR). The Event Generator is able to generate machine fiducial frequencies and the coincidence (superperiod) clock by only providing a RF clock reference and a low voltage mains voltage synchronization signal.

4.1. Timing Resolution

Injection timing requires synchronization to both the mains voltage phase and coincidence (superperiod) frequency. The coincidence frequency is determined by the machine fiducials i.e. the number of bunches in the booster ring and storage ring. To find the coincidence frequency the fiducials have to be factorized first. Below we show the fiducials of the Swiss Light Source (SLS):

Table 3: Light Source Harmonic Numbers (SLS)

Number of bunches (SR)	480	= 2 * 2 * 2 * 2 * 2 * 3 * 5
Number of bunches (Booster)	450	= 2 * 3 * 3 * 5 * 5

When we divide both numbers by the common factor 30 (2 * 3 * 5) we get 16 for storage ring and 15 for booster i.e. the same buckets in booster and storage ring are aligned every 16 booster turns and 15 storage ring turns. The accelerating frequency for SLS is 499.654 MHz i.e. the coincidence frequency is 499.654 MHz / (450 * 16) = 69.396 kHz.

The event transfer rate has to be selected so that both the booster and storage ring revolution clocks may be distributed. The ideal case would be to have an event distribution frequency of the rate of the event clock, but the technology is currently too expensive. The common factor of the revolution frequencies of SLS is 30, so an event transfer rate of 499.654 MHz / 30 would be sufficient, however, a multiple of this 499.654 MHz / 10 was chosen. The event frame which is transfered at the event transfer rate consists of two 8B10B encoded bytes i.e. 20 bits are transfered on each event clock cycle. This leads to a bit rate of 1 Gbit/s for an event transfer rate of 50 MHz. The transfer rate should be optimized keeping in mind that the jitter is decreased with a higher bit rate. Unfortunately, the bit rate does correlate with the system price.

4.2. Injection Timing

The event system may be put up by providing the accelerating frequency RF clock reference and a 3 to 12 VAC signal from a mains voltage transformer to the Event Generator (EVG). The EVG is capable of generating booster and storage ring revolution clocks and coincidence (superperiod) clock. The AC input is divided by a programmable divider to provide the injection cycle frequency which is usually a few hertz. The output of the AC line sync divider may be delayed by 0 to 25.5 ms in 0.1 ms steps to be able to adjust the triggering position relative to mains voltage phase. After this the signal is synchronized to the coincidence clock (when buckets in booster and SR are aligned).

The generated injection signal trigger may be used to trigger a RAM sequence that contains event codes for the injection process. The sequence RAMs run at the booster ring revolution frequency,

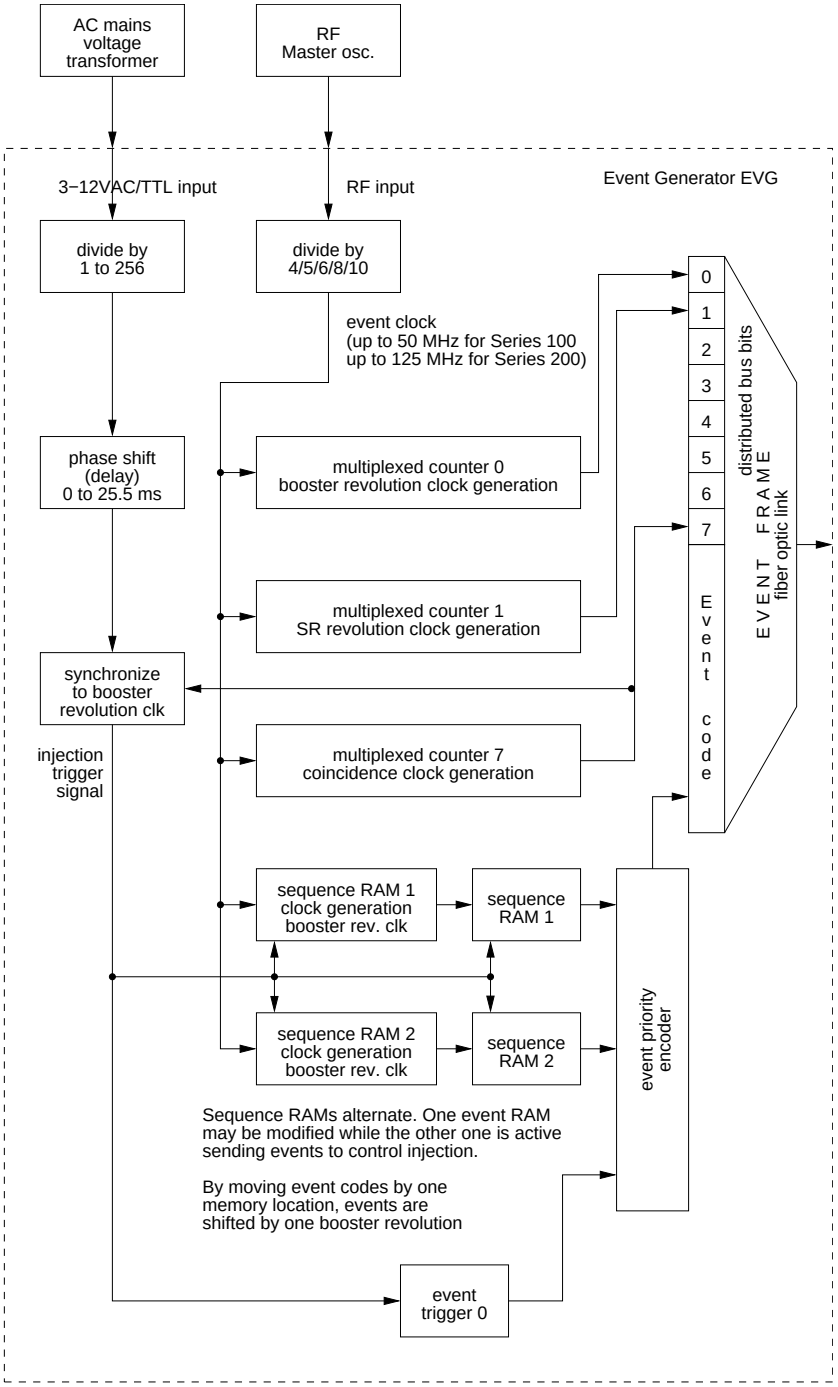

Figure 29: Fiducials and trigger generation.

so moving the *extract beam from booster* event in sequence RAM memory for example by one memory location will shift the extraction by one booster ring revolution. By moving the extraction by the number of booster revolution in one superperiod brings us back to the same alignment. That means that we can select the target buckets with a precision of the number of buckets in booster ring divided by the number of booster revolutions in one superperiod by modifying the extraction delay. For smaller steps the linac gun triggering has to be adjusted.

Distributed bus signals may be used to distribute the booster revolution, storage ring revolution and coincidence (superperiod) clocks i.e. the clocks are distributed by fiber and are available at all event receivers as TTL outputs.

The setup described above occupies 3 multiplexed counters and both sequence RAMs. Five multiplexed counters and eigth external hardware trigger inputs are still left for other signals.