CSI3131 – Operating Systems
Tutorial 7 – Memory Management

1. Describe two differences between logical and physical addresses.

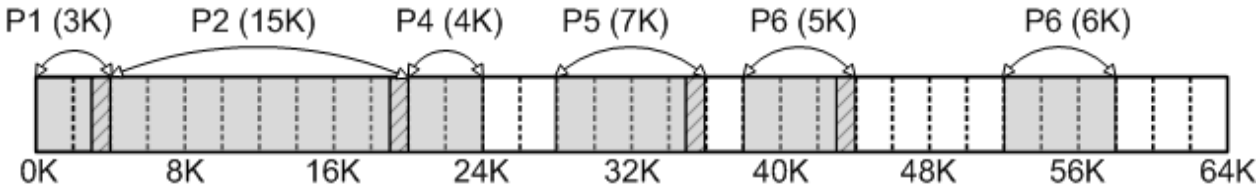
2. Consider a system in which a program can be separated into two parts: code and data. The CPU knows whether it wants an instruction (instruction fetch) or data(data fetch or store). Therefore, two base–limit register pairs are provided: one for instructions and one for data. The instruction base–limit register pair is automatically read-only, so programs can be shared among different users. Discuss the advantages and disadvantages of this scheme.

3. Why are page/frame sizes always powers of 2?

4. Consider a logical address space of eight pages of 1024 bytes each, mapped onto a physical memory of 32 frames.
   How many bits are there in the logical address? Identify in the logical address the bits used as an offset and the bits used as the page number.

   How many bits are there in the physical address? Identify in the physical address the bits used as an offset and the bits used as the frame number.

5. Consider a computer using dynamic contiguous allocation, where each allocated block is a multiple of 2kb. Consider the following situation:



   Consider the following sequence of allocating/deallocating
   - Allocate process P7, size 7kb
   - Deallocate process P2
   - Deallocate process P5
   - Allocate process P8, size 12 kb
   - Allocate process P9, size 11 kb
   - Allocate process P10, size 5k

   a) Draw pictures describing the final allocation using first-fit and best-fit allocation algorithms.

   b) What is the internal fragmentation at the end? What about external fragmentation?

6. Consider a memory containing 16 blocks, with the allocation described by the following Inverted Page Table (An entry contains Process number and block number within the process:

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
P1,4	P2,2	P2,4	P1,1	P1,0	P2,3	P3,1	P1,3	P2,1		P1,5	P3,0		P2,0	P1,2	

From the above Inverted Page Table, complete the Page tables for Processes P1 and P2 below.

P1	
Frame #	**Valid (1/0)**

P2	
Frame #	**Valid (1/0)**

7. Consider a computer with 24 bit logical address space, 64MB of physical memory, 1kb pages, with each page table entry taking 4 bytes.

Describe the format of logical address for this computer, by answering the following questions:

a) Draw a bar, indicating how many bits define the offset and how many bits define the logical page #.

b) Do you need hierarchical page tables? In not, explain why. If yes, separate the bits for the logical page # into the corresponding parts (in the answer for a)). How many levels of hierarchy do you need?

c) Assume you have decided to use Inverted Page Tables (IPT) instead. How big should the IPT be? (assume that 2 bytes are sufficient to store PID, you have to answer for yourself how many bytes you need to store the logical page #).

8. Consider the following simple memory management system combining segmentation and paging (illustrated in the figure to the right):

   A process consists of at most 4 segments, where each segment itself is paged, with pages/frames of size 2kb. The page table of each segment contains 8 entries, each storing reference to the corresponding physical frame. The segment table entries refer to the page tables of the corresponding segments.

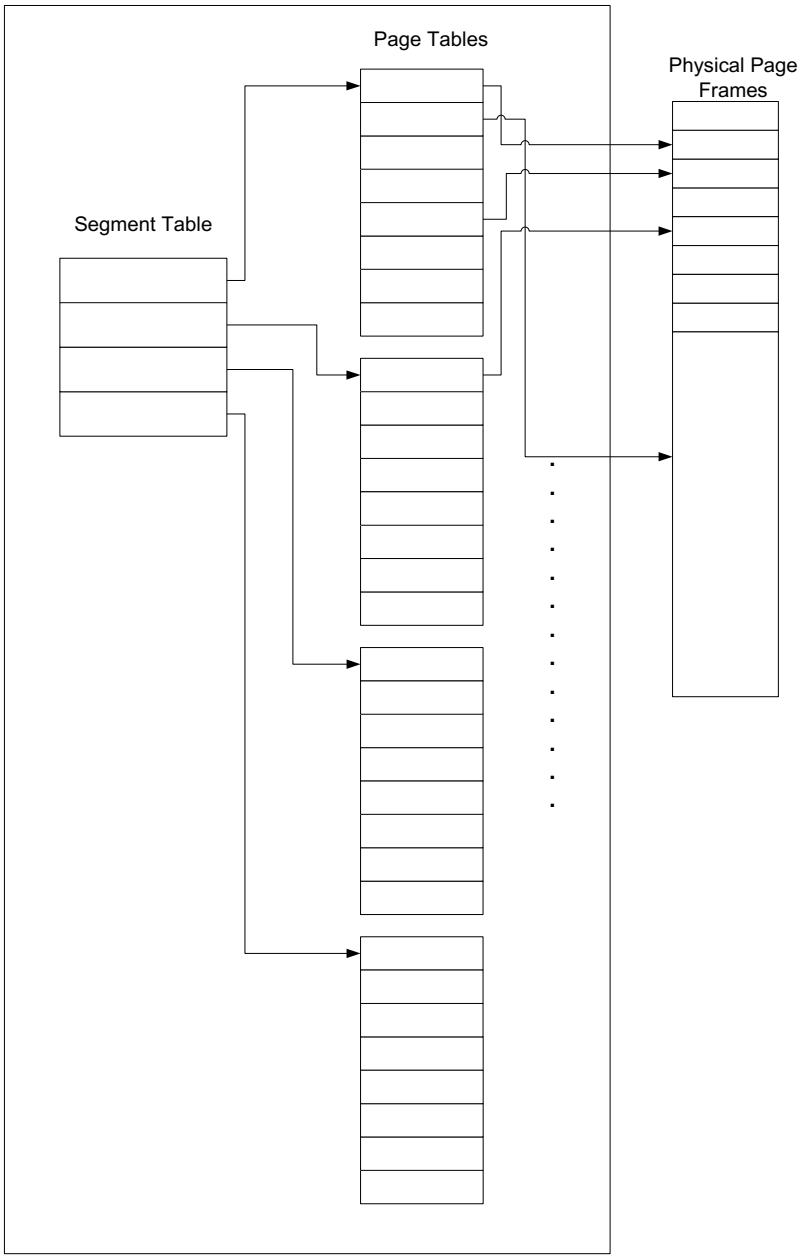
   Because of relatively small size, both segment table and segment page tables are stored directly in the process's PCB (process control block), without occupying another physical frames.

   Answer the following questions:

   a. What is the maximum size of each segment?

   b. What is the largest logical address for the process?

   c. Give the format of the logical address.



   d. Explain how the logical address is translated to the physical address.