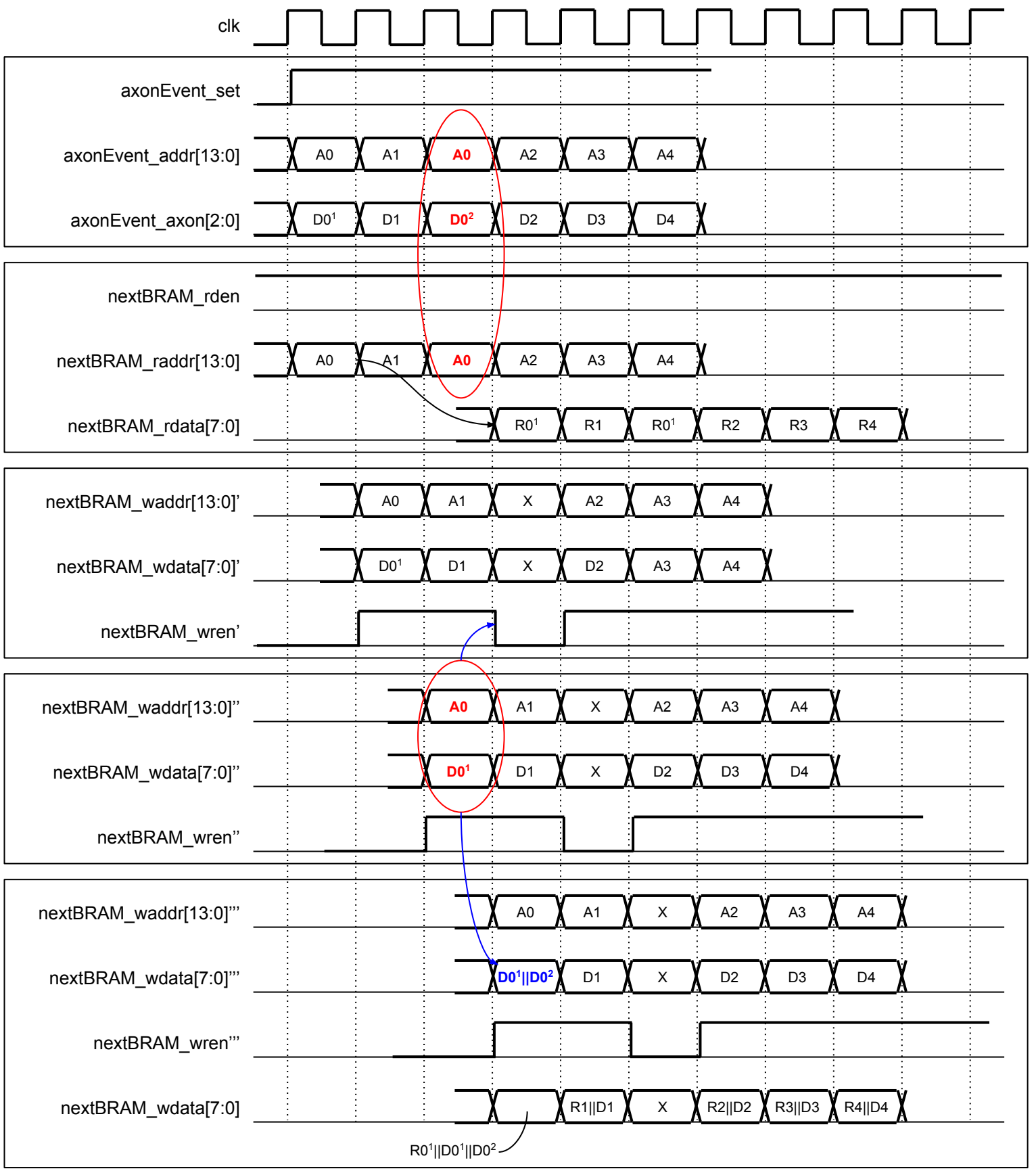
Next/Future BRAM process



Axon event
17-bit axon address split as:
14-bit nextBRAM row address
3-bit specific axon in row

nextBRAM:read
14-bit nextBRAM row address
8-bit axon states in row address

always active (rden=1)
raddr=axonEvent_addr
rdata pipeline depth=3

nextBRAM:write pipeline stage 1

nextBRAM:write pipeline stage 2

axonEvent_addr collision with stage 2 address:
1) set wren=0 @ stage 1
2) combine registered data with input @ stage 3

nextBRAM:write pipeline stage 3

waddr = wraddr'''
wdata = rdata || wdata'''
wren = wren'''

Properties

- The Future BRAM receives axon events from other cores and is continuously running (during and after Phases 1 and 2).
- There are 2^{17} axons in each core. The future and current BRAMs are configured as 2^{14} rows of 8 bits each. Each bit in the BRAMs indicates if the axon is on/off.
- An incoming axon event comprises of the 14-bit BRAM row address and a 3-bit axon address, indicating which of the 8 axons in the row must be toggled from 0 to 1. To toggle from 0 to 1, the 8-bit data that is already present in the specific BRAM row must be OR'ed with a one-hot mask whose active bit is defined by the 3-bit axon address.
- Since there is a pipeline when reading data from BRAM, and consecutive events may be destined for the same BRAM row address, it is necessary to compare the incoming data with what is currently being "backed up" in the pipeline. If an address collision occurs, then the data must be treated accordingly.