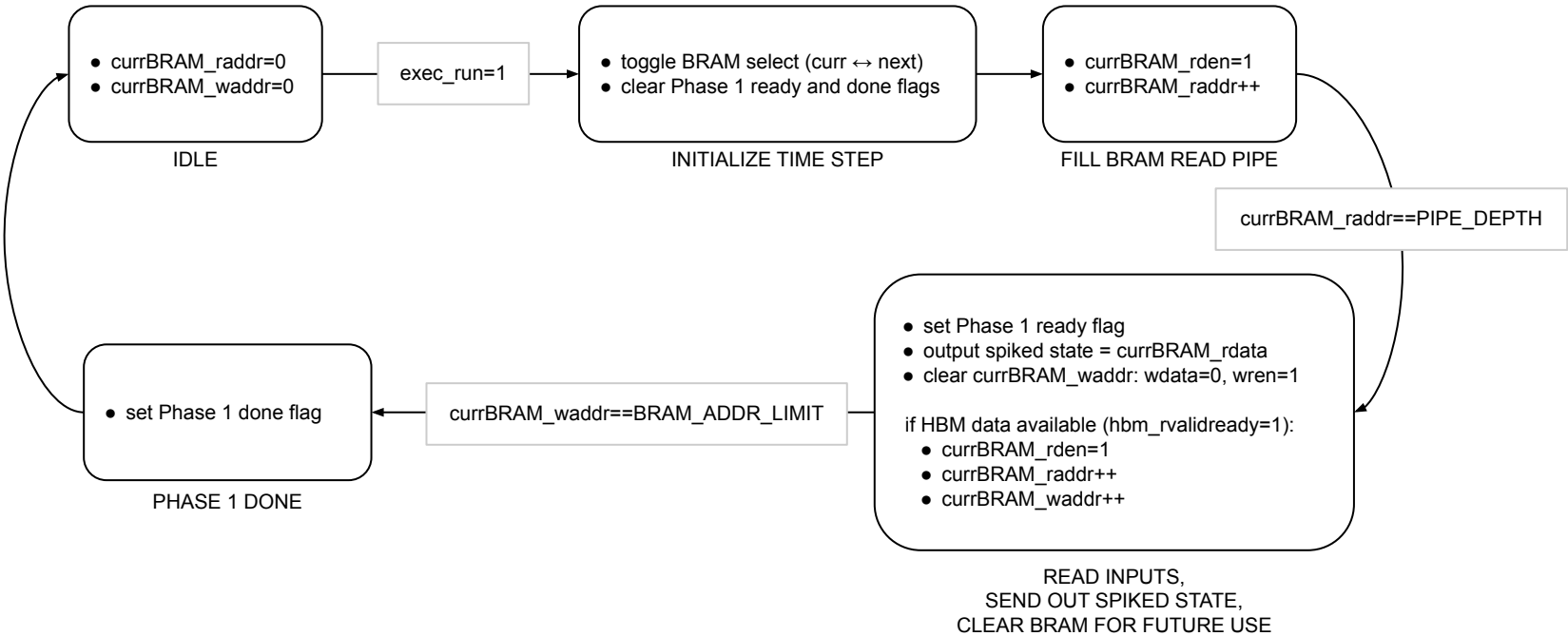
Current/Present BRAM process



Properties

- At the onset of a new time step, the read and write addresses are reset and the Phase 1 flags are cleared.
- The current/present BRAM is read until the pipeline has been filled (currBRAM_raddr==PIPE_DEPTH). Set Phase 1 ready flag.
- If HBM data available: clear currBRAM_waddr (for future use in next time step), send out spiked state, and advance read and write pointers.
- Once currBRAM_waddr reaches the limit (defined by the user as number of inputs), the Phase 1 done flag is set and the machine returns to the idle state (waiting for the next time step).