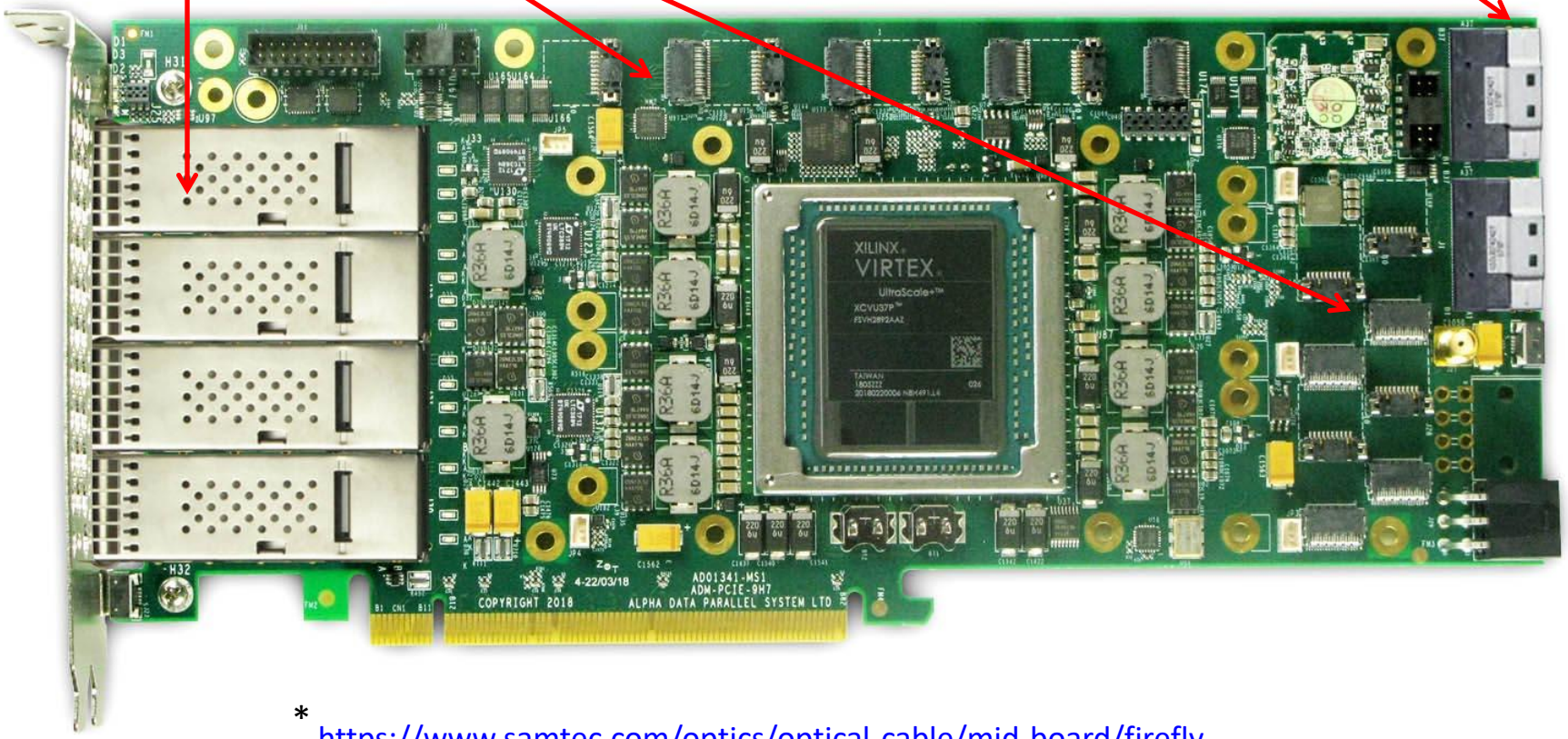
Alpha-Data ADM-PCIE-9H7

8 Firefly ports, 4 QSFP, 2 Slim SAS, PCIex16

4 QSFP28s, 8 Fireflys*, each 4 bidi lanes x 28Gbps/lane/dir (or 14, 16, 25 Gbps), 2 Slim SAS 100Gbps



* https://www.samtec.com/optics/optical-cable/mid-board/firefly

Bandwidth theoretical maximum estimate:

100Gbps @ ~33b/spike => 3G spikes per sec (sps).
TX & RX: 3G sps in and out each Firefly port
4 FireFly ports per spike processing board.
>10G sps combined TX & RX bandwidth *per board.*

Each FPGA will be incapable of generating or processing that many off-board in or out spikes per second which is good news for the NIC(s). [1]

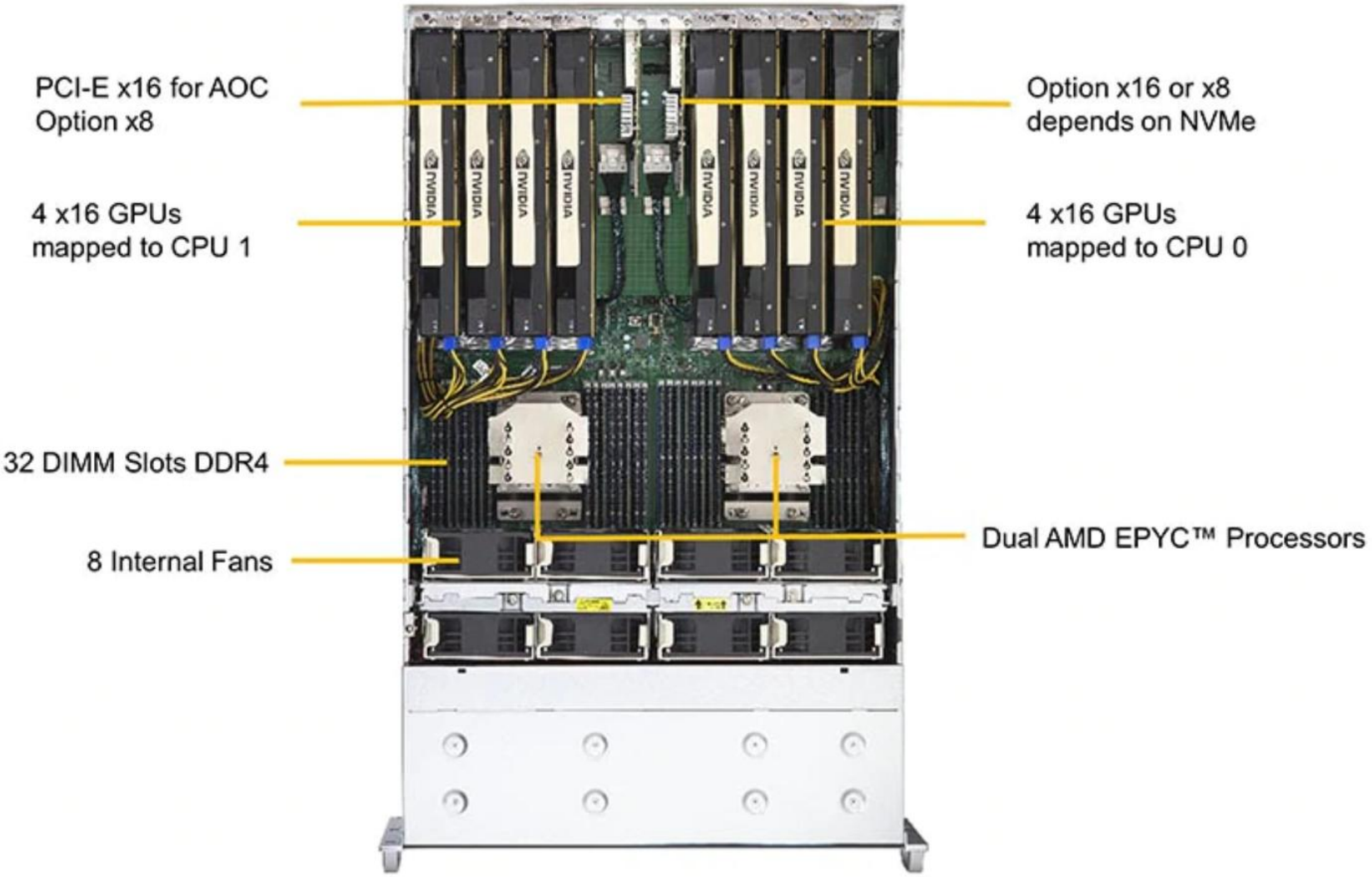
So we can run the Fireflys at a lower speed to save power and improve BER if either is a problem.

The NIC needs to act as mini 12 port switch (SW) for spike events routing below wire speeds using simple fifos, pipelining, muxing, demuxing, and also forwarding to the SW. The 12 ports are the 8 FPGAs, 3 to the other 3 server chassis, and 1 100GigE port.

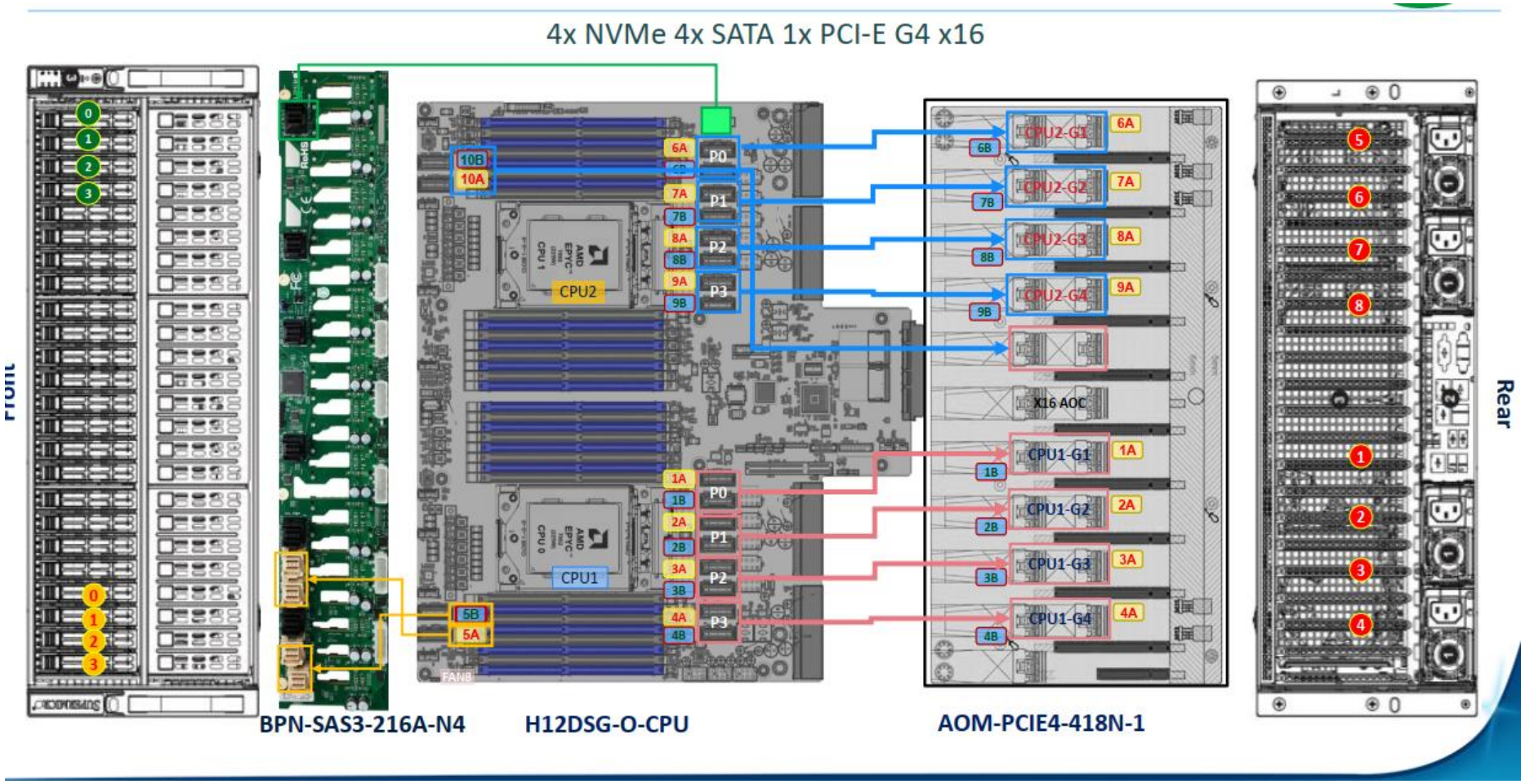
[1] ***"You want Bandwidth? You can't handle the bandwidth."***
https://www.youtube.com/watch?v=NkiyAZ63RT8&ab_channel=TopGear ☺

AS -4124GS-TNR

(Top View – System)



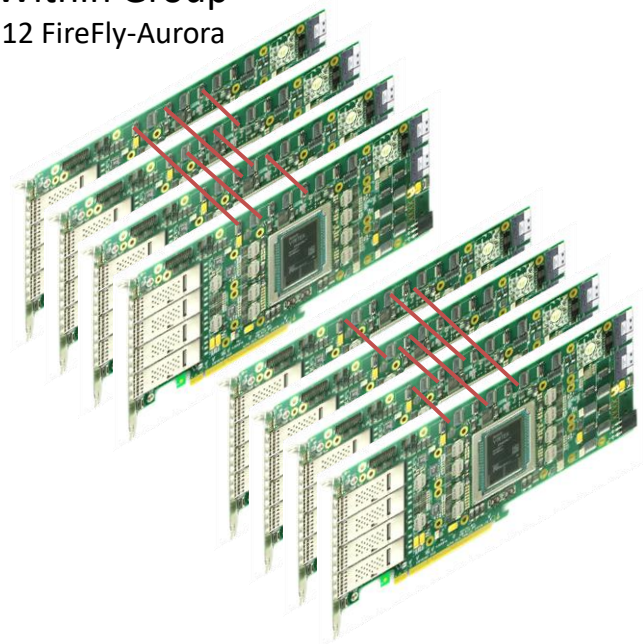
This is what we bought – Standard supported configuration



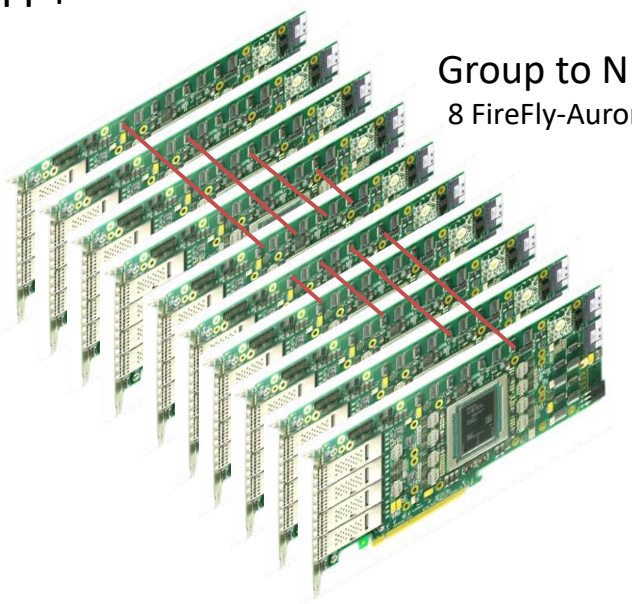
Recommended Wiring Diagram for ***Dual*** NIC Option

20 FFLY, 1 SAS, 8 QSFP+
times 4 servers

Within Group
12 FireFly-Aurora



Group to NIC
8 FireFly-Aurora



NIC to SW
1 Eth-UDP/TCIP

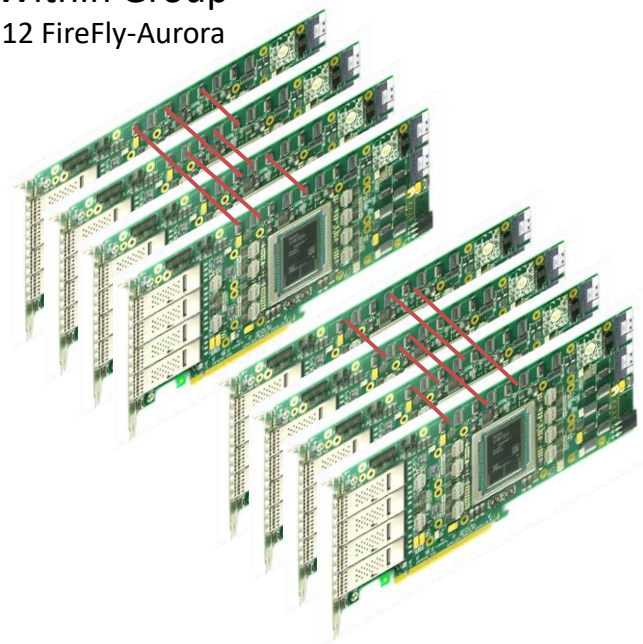
NIC to NIC
3 Aurora on QSFP+

NIC to NIC
SAS Option

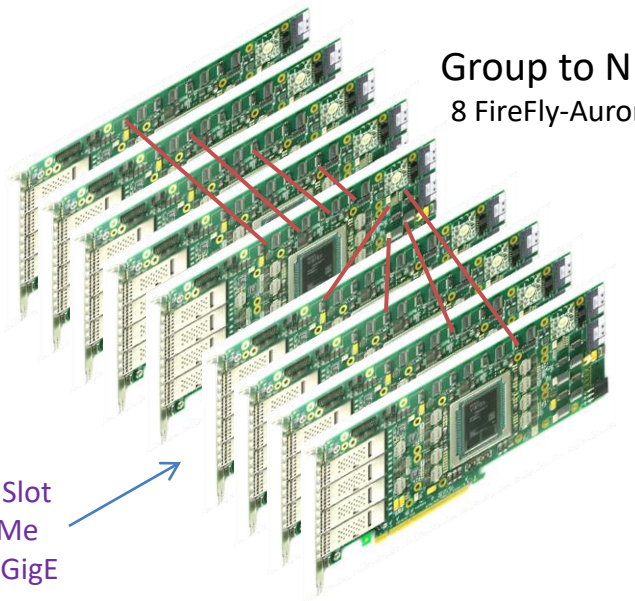
Recommended Wiring Diagram for ***Single*** NIC option

20 FFLY, 4 QSFP+
times 4 servers

Within Group
12 FireFly-Aurora



Group to NIC
8 FireFly-Aurora



Empty Slot
for NVMe
Or 100GigE

NIC to SW
1 Eth-UDP/TCIP

NIC to NIC
3 Aurora on QSFP+

Recommended Wiring Diagram for ***1-Hop*** NIC option

8 FFLY, 4 QSFP+
times 4 servers