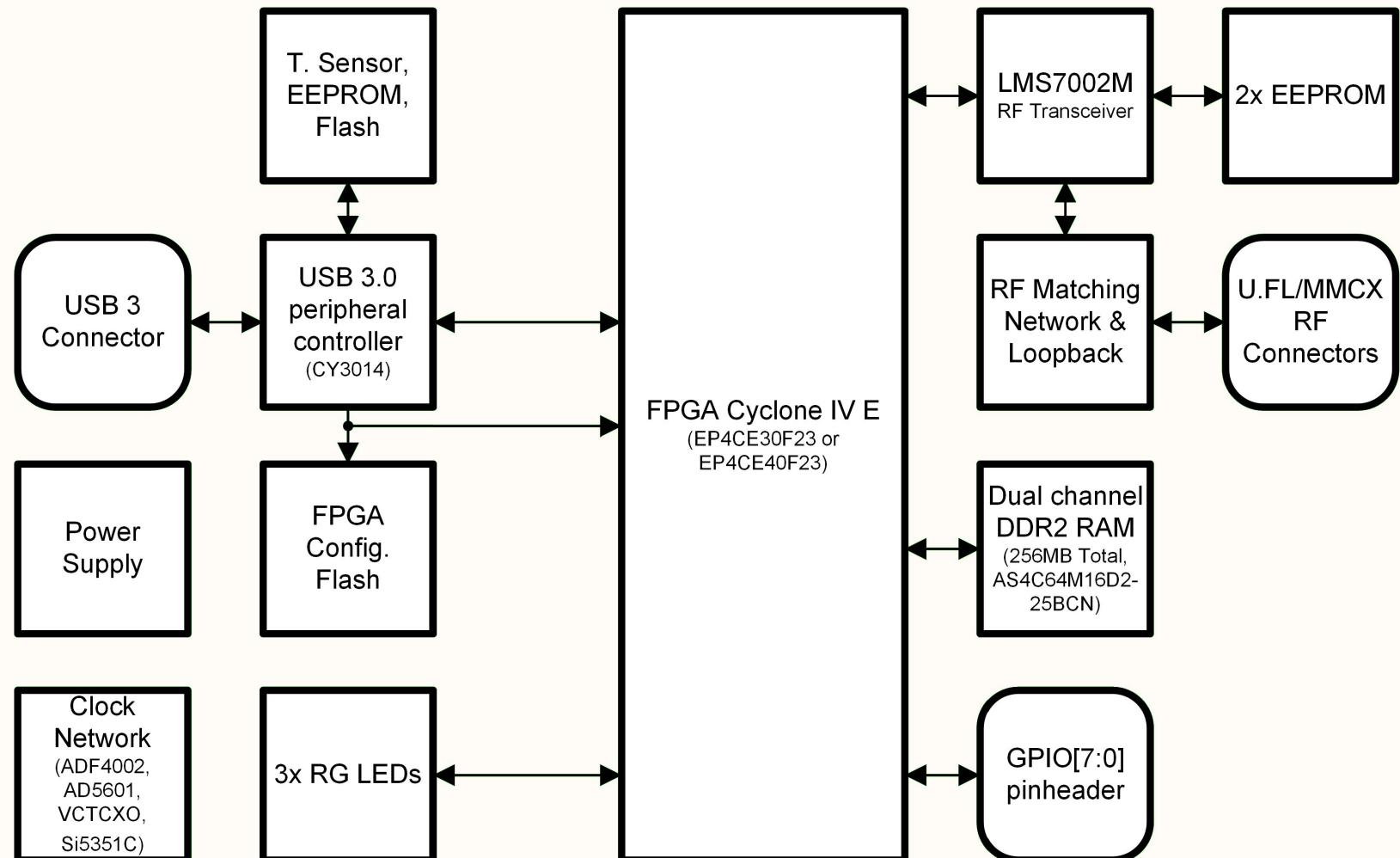


Block diagram



Project name: [LimeSDR-USB_Iv4s.PrjPcb](#)

Title: **Block diagram**

Size: **A4** Revision: **v1.4s**

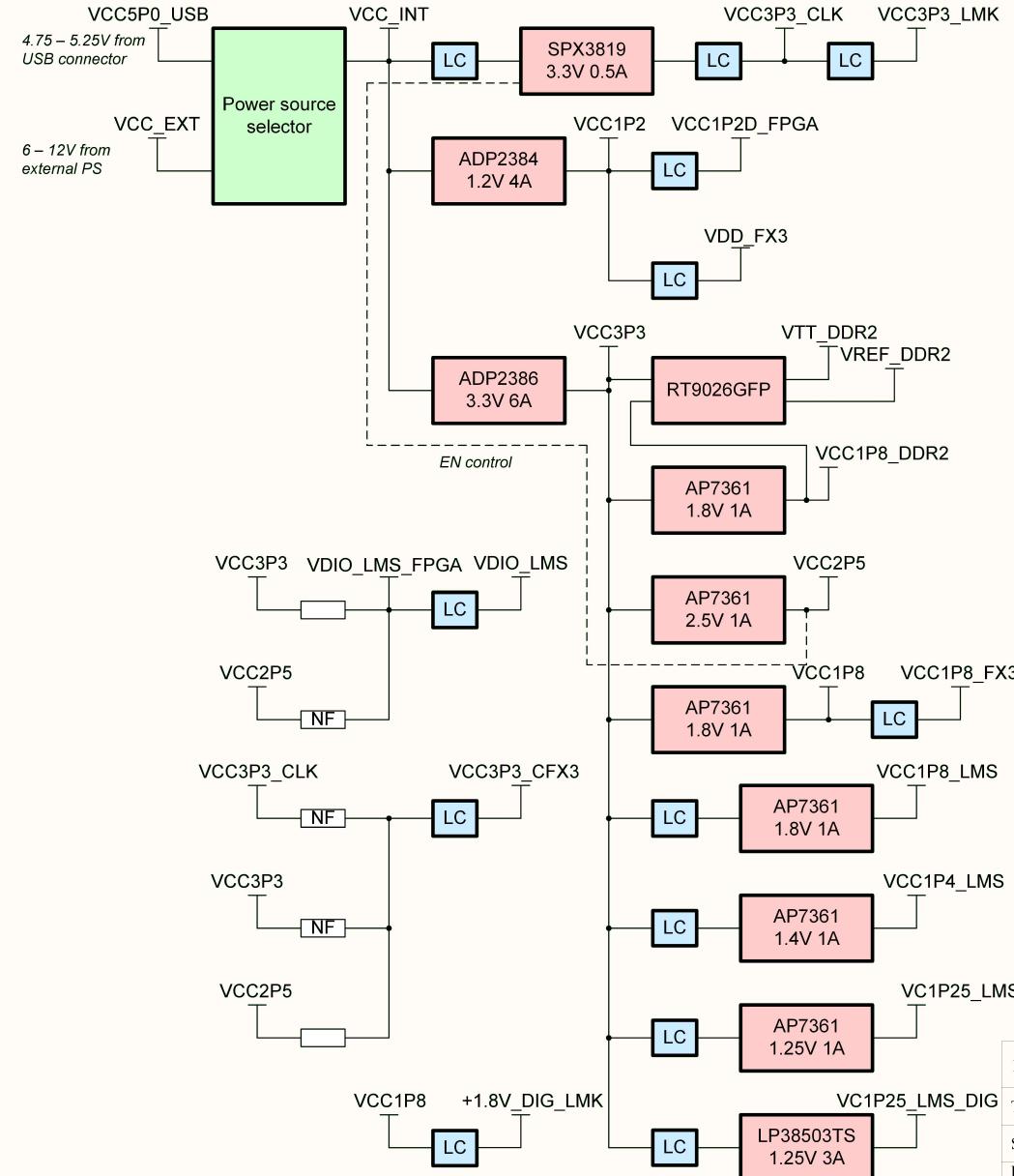
Date: **2020-09-30** Time: **13:56:05** Sheet**1** of **15**

File: [01_BlockDiagram.SchDoc](#)

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Power diagram



Project name: **LimeSDR-USB_Iv4s.PrfPcb**

Title: **Power diagram**

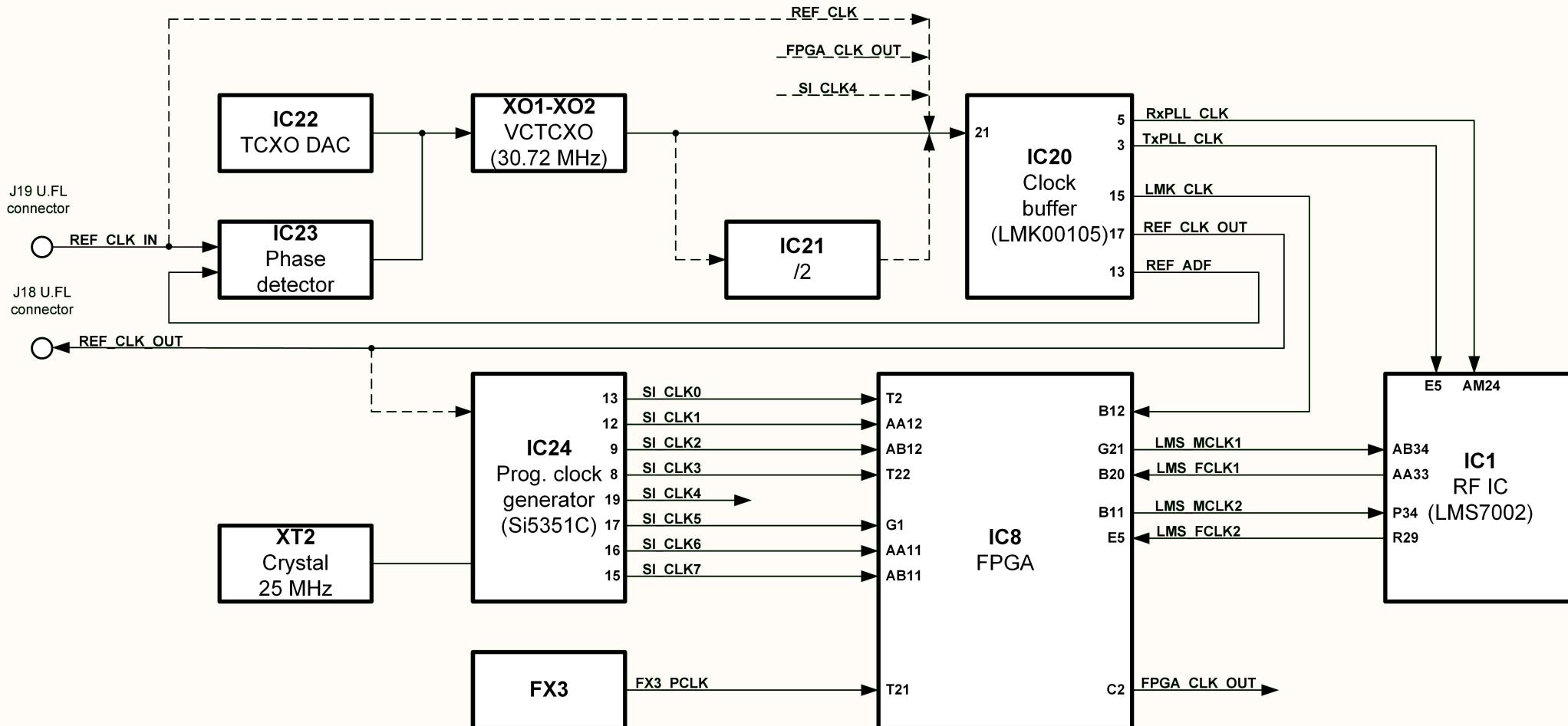
Size: **A4** Revision: **v1.4s**

Date: **2020-09-30** Time: **13:56:12** Sheet**2** of **15**

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Clock diagram



Project name: *LimeSDR-USB_Iv4s.PrfPcb*

Title: *Clock diagram*

Size: **A4** Revision: **v1.4s**

Date: **2020-09-30** Time: **13:56:24** Sheet**3** of **15**

File: **03_ClockDiagram.SchDoc**

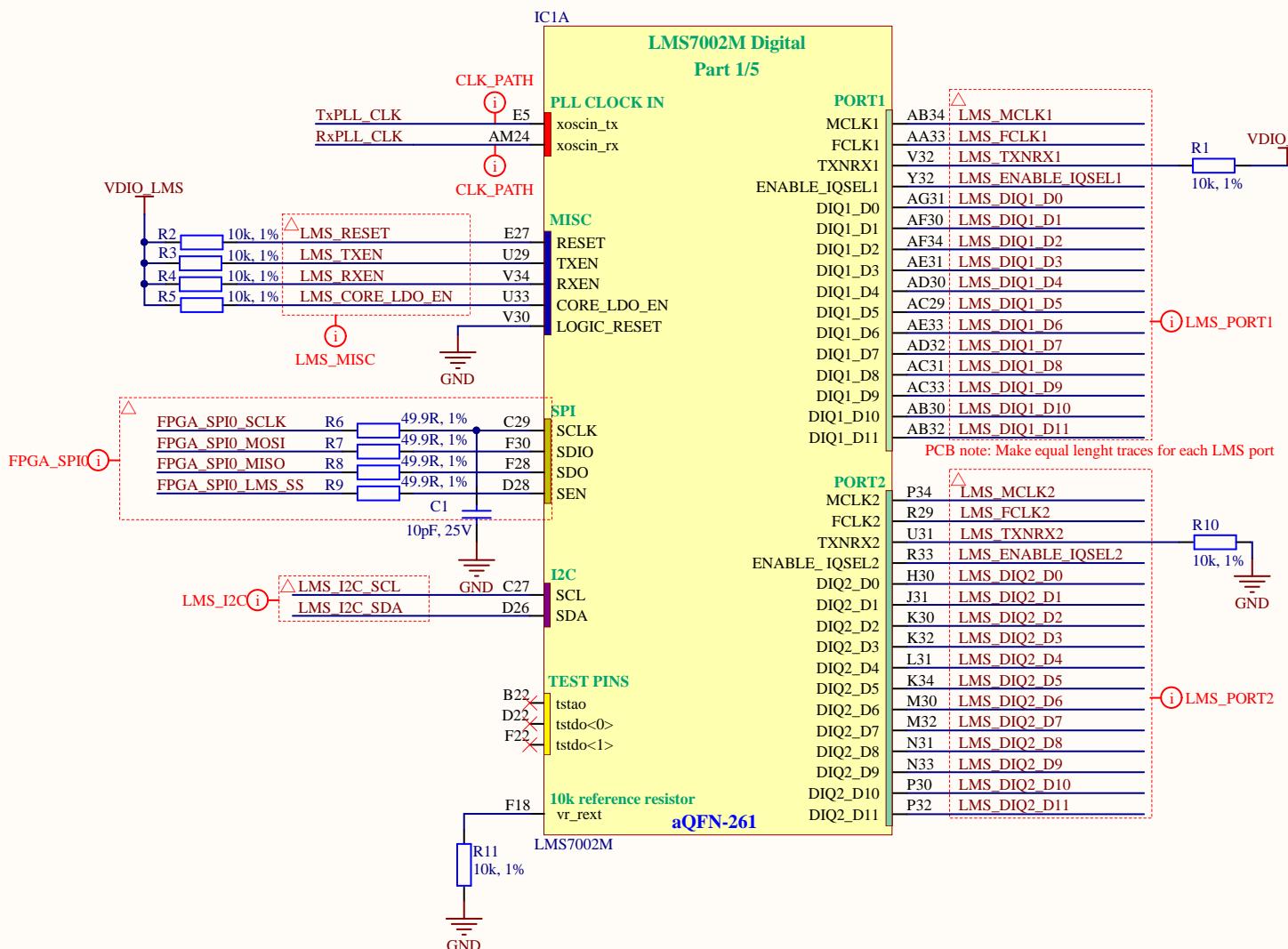
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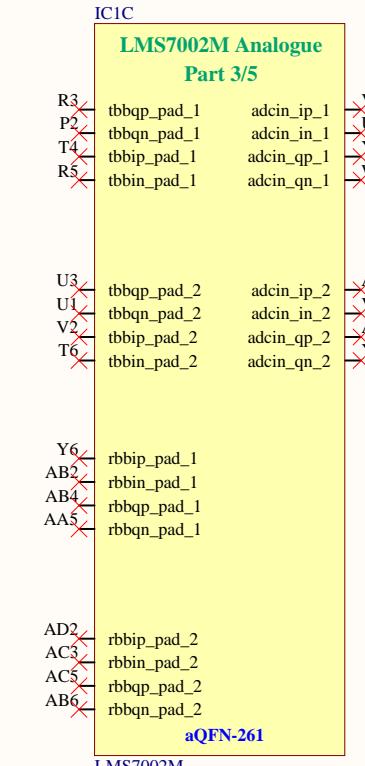
NF elements on sheet: -
Number of NF elements on sheet: 0

LMS7002M miso

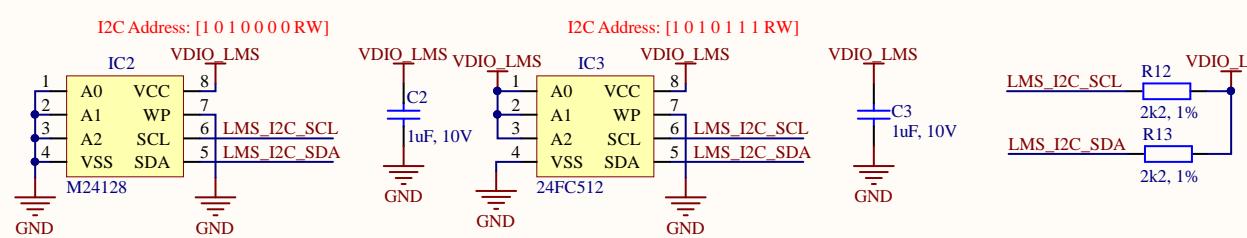
Digital interfaces



Baseband external IO



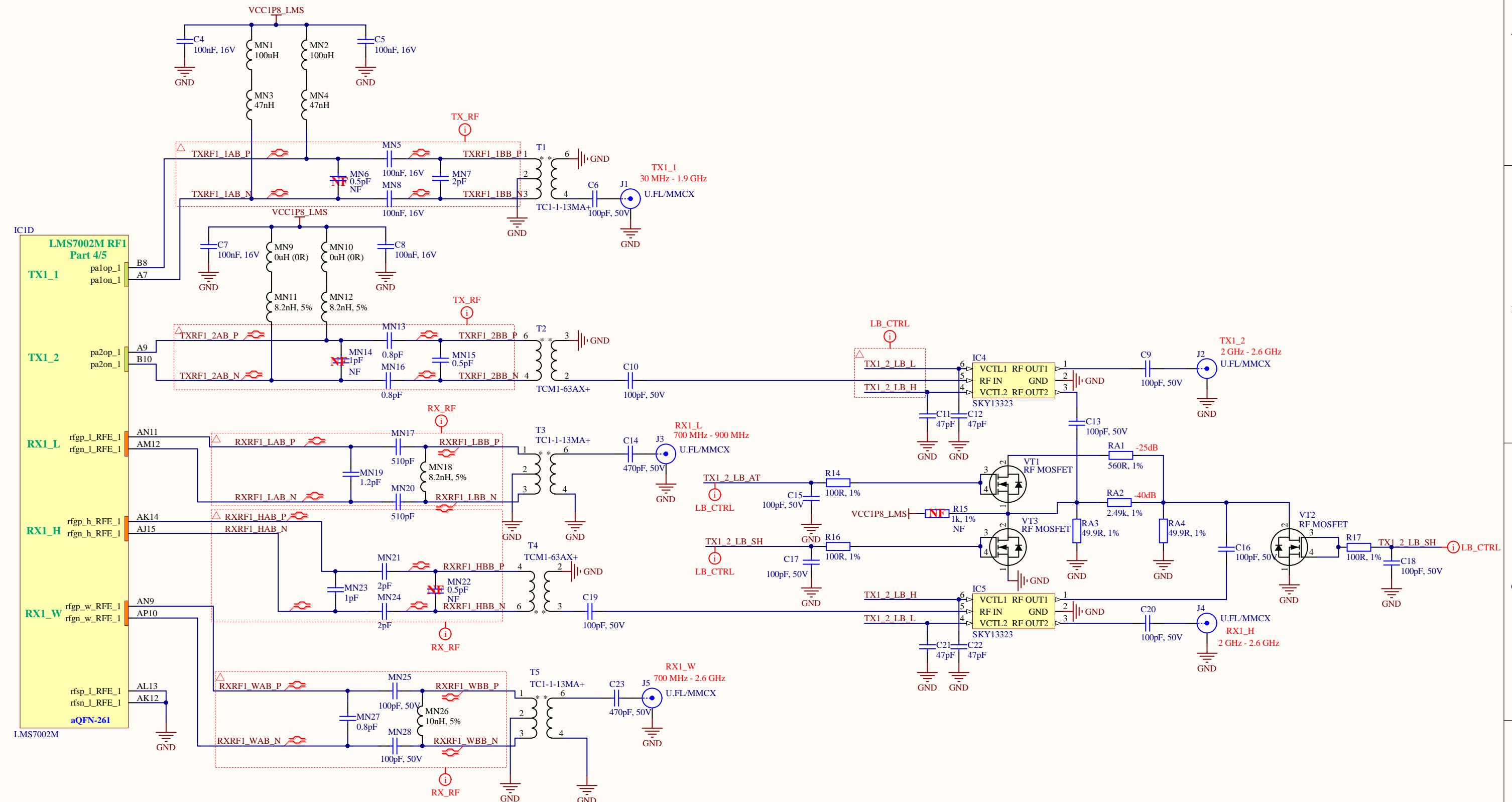
LMS EEPROMS



Project name:	LimeSDR-USB_1v4s.PrjPcb		
Title:	LMS7002M misc		
Size:	A3	Revision:	v1.4s
Date:	2020-09-30	Time:	13:56:33
File:	04_LMS7002M_Misc.SchDoc		

NF elements on sheet: MN6, MN14, MN22, R15
 Number of NF elements on sheet: 4

LMS7002M RF1 circuits



Project name: LimeSDR-USB_1v4s.PnjPcb

Title: LMS7002M RF

Size: A3 Revision: v1.4s

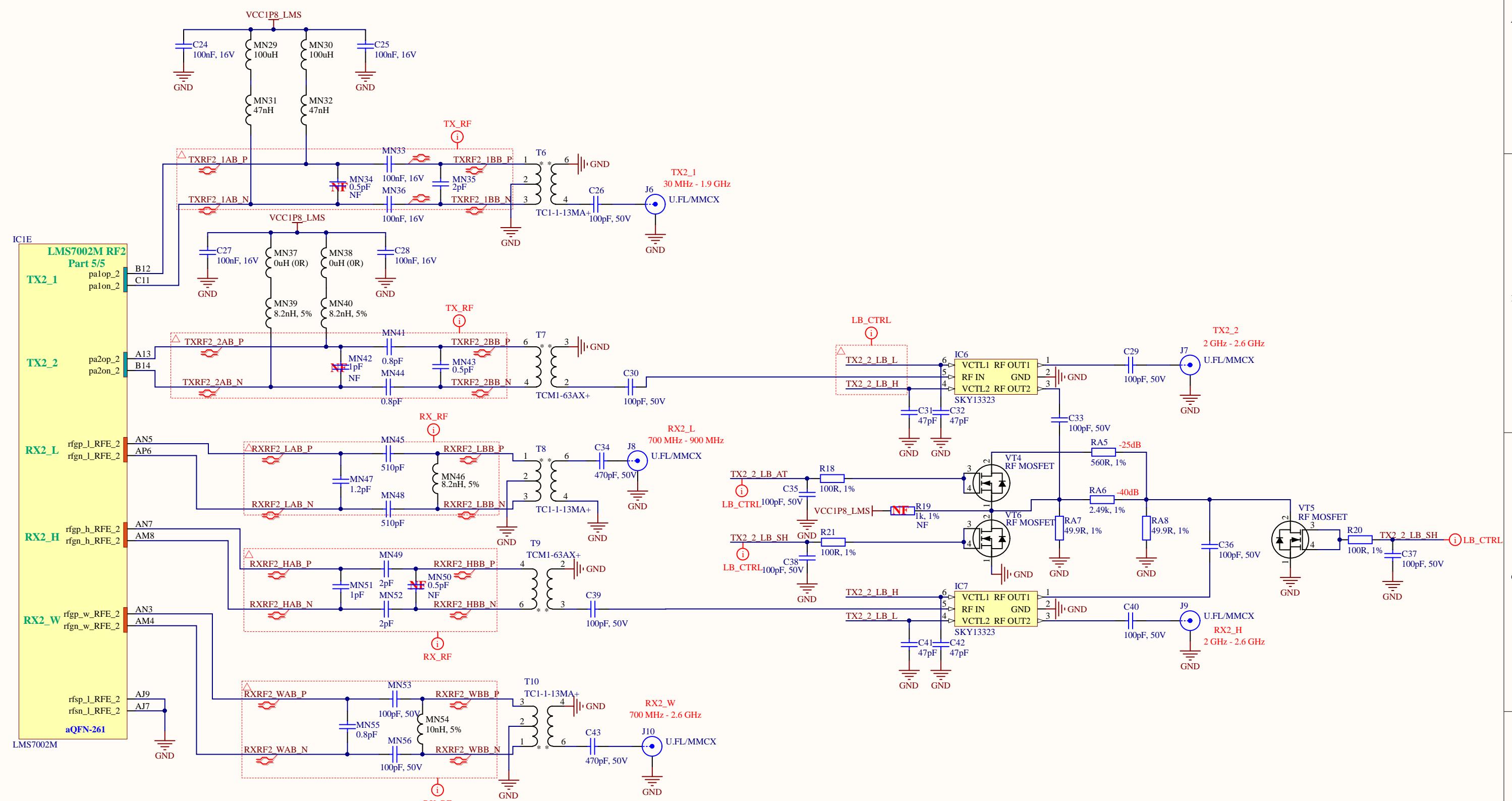
Date: 2020-09-30 Time: 13:56:38 Sheet 5 of 15

File: 05_LMS7002M_RF1.SchDoc



NF elements on sheet: MN34, MN42, MN50, R19
 Number of NF elements on sheet: 4

LMS7002M RF2 circuits



Project name: LimeSDR-USB_1v4s.PnjPcb

Title: LMS7002M RF

Size: A3 Revision: v1.4s

Date: 2020-09-30 Time: 13:56:42 Sheet 6 of 15

File: 06_LMS7002M_RF2.SchDoc

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LMS7002M power supply circuit

NF elements on sheet: FR18, FR25
Number of NF elements on sheet: 2

A

B

C

D

E

F

G

H

A

B

C

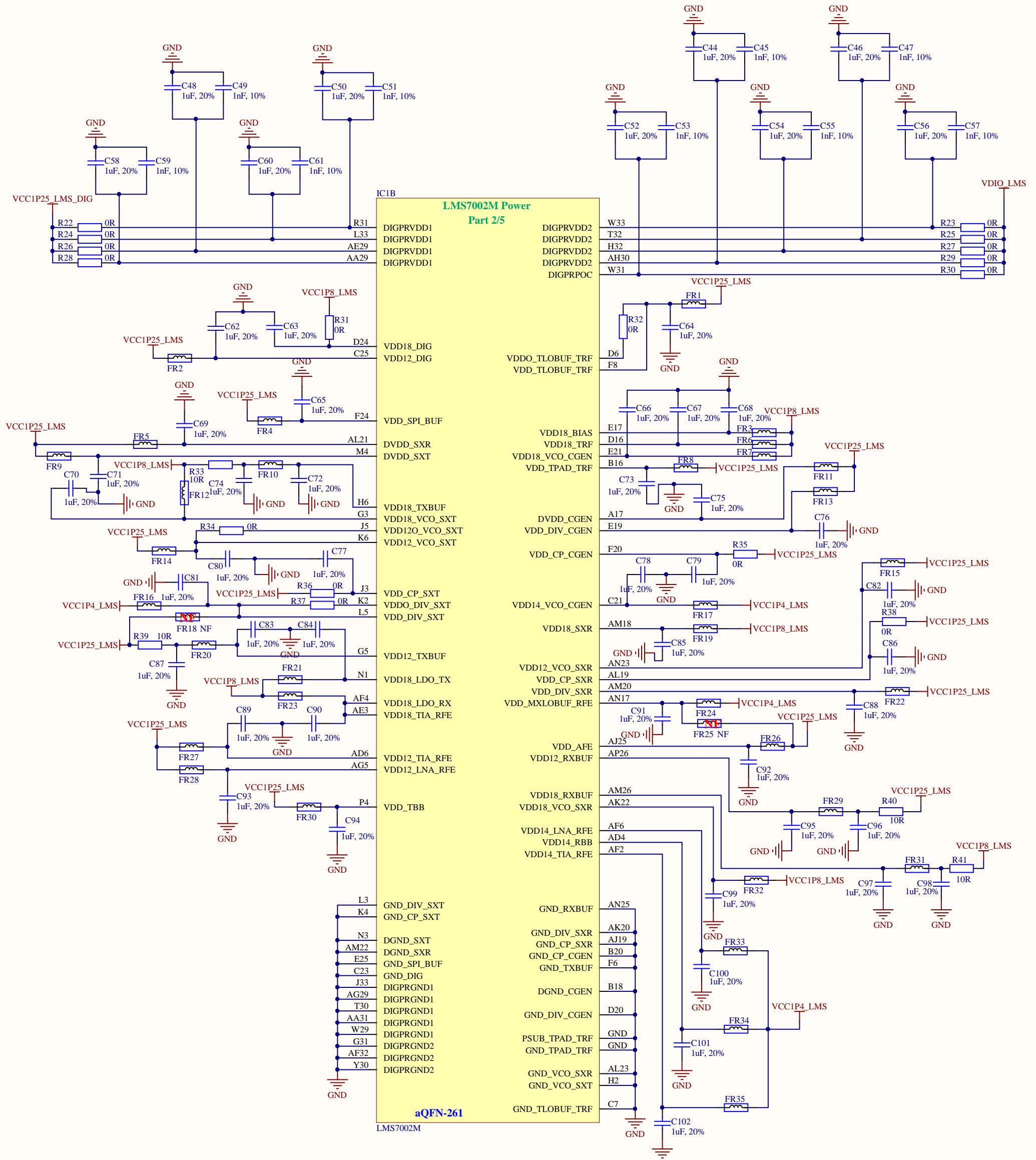
D

E

F

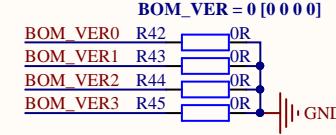
G

H



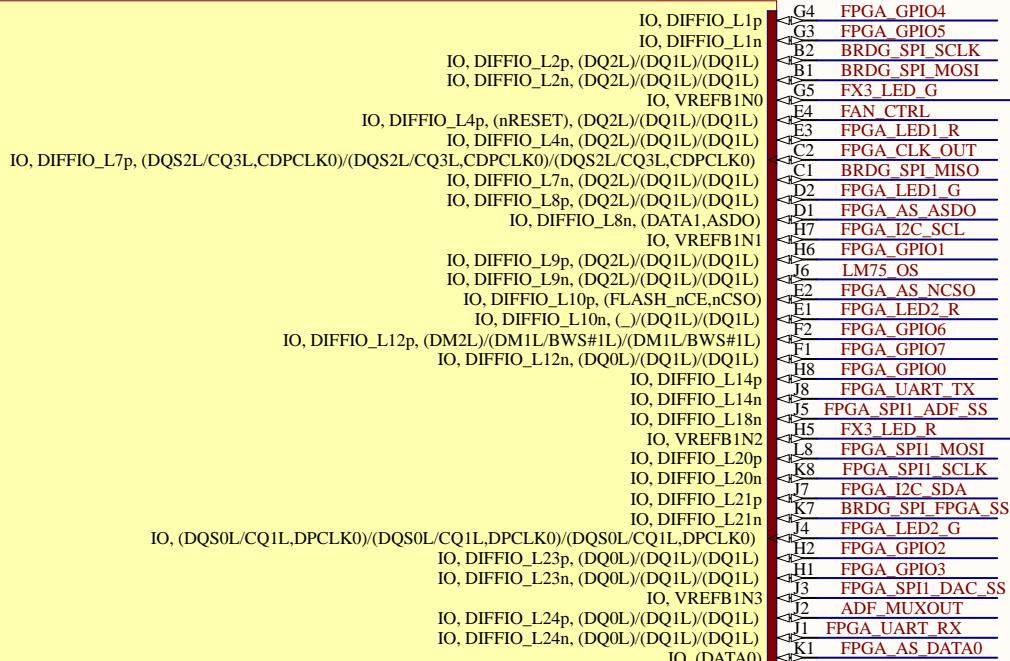
FPGA banks 1, 2, 3, 4

NF elements on sheet: -
Number of NF elements on sheet: 0



A

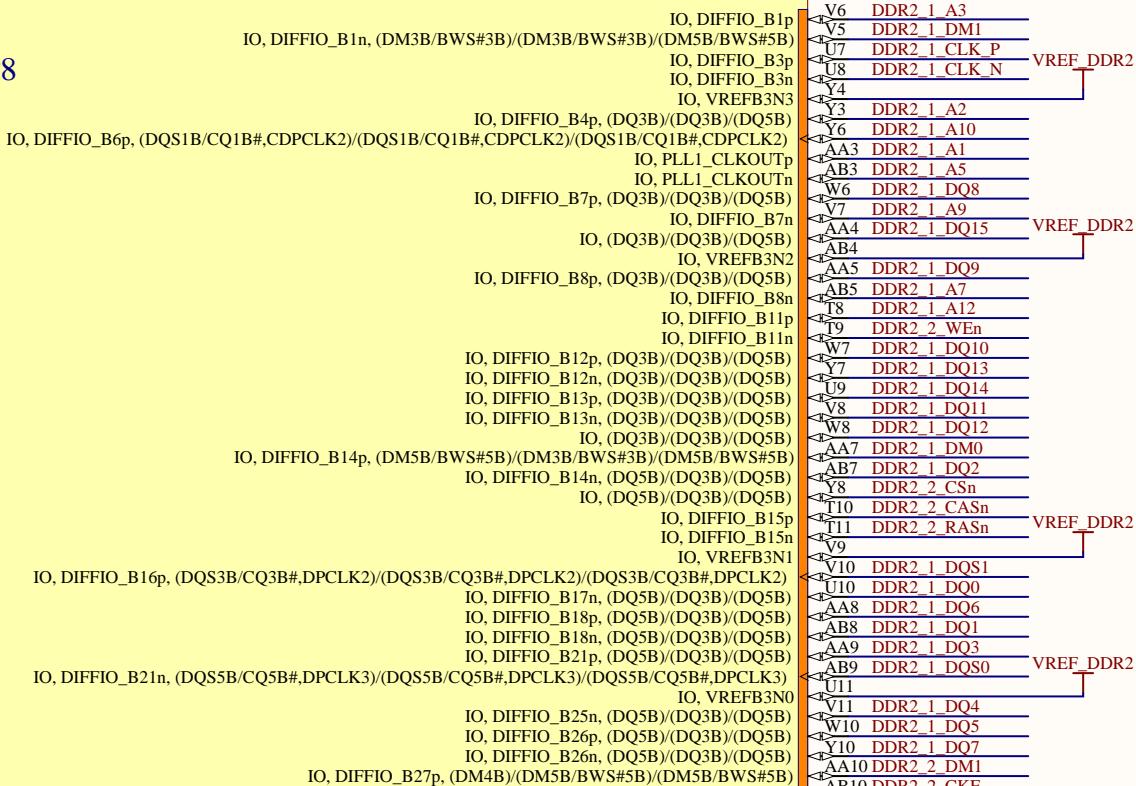
IC8A
BANK 1
VCC3P3



EP4CE40F23C8N

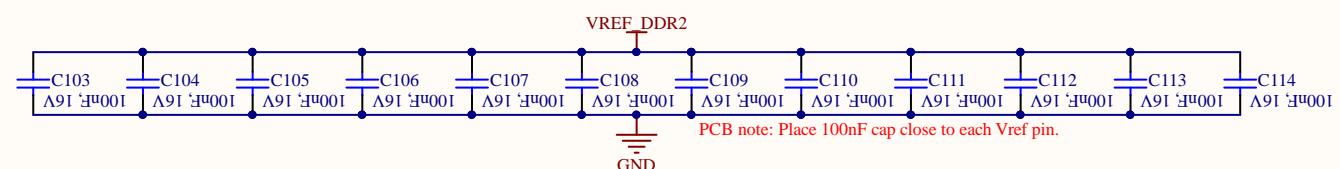
B

IC8C
BANK 3
VCC1P8

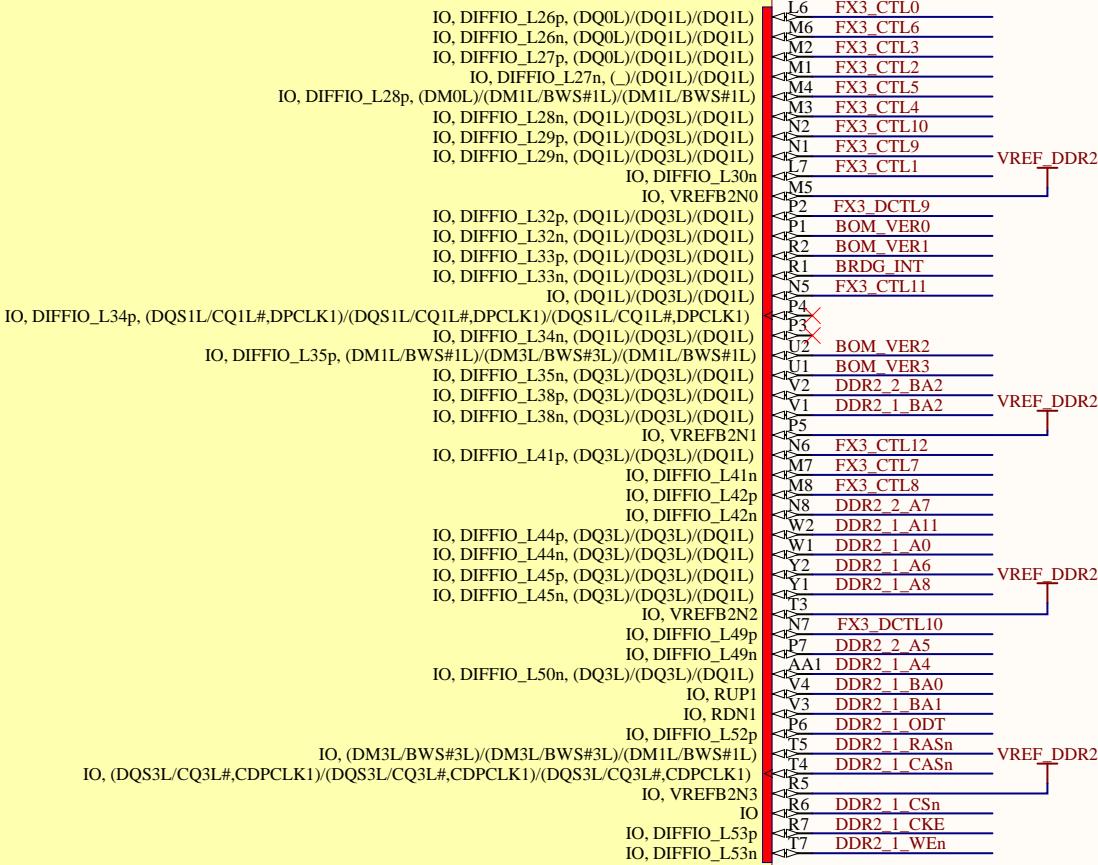


EP4CE40F23C8N

D

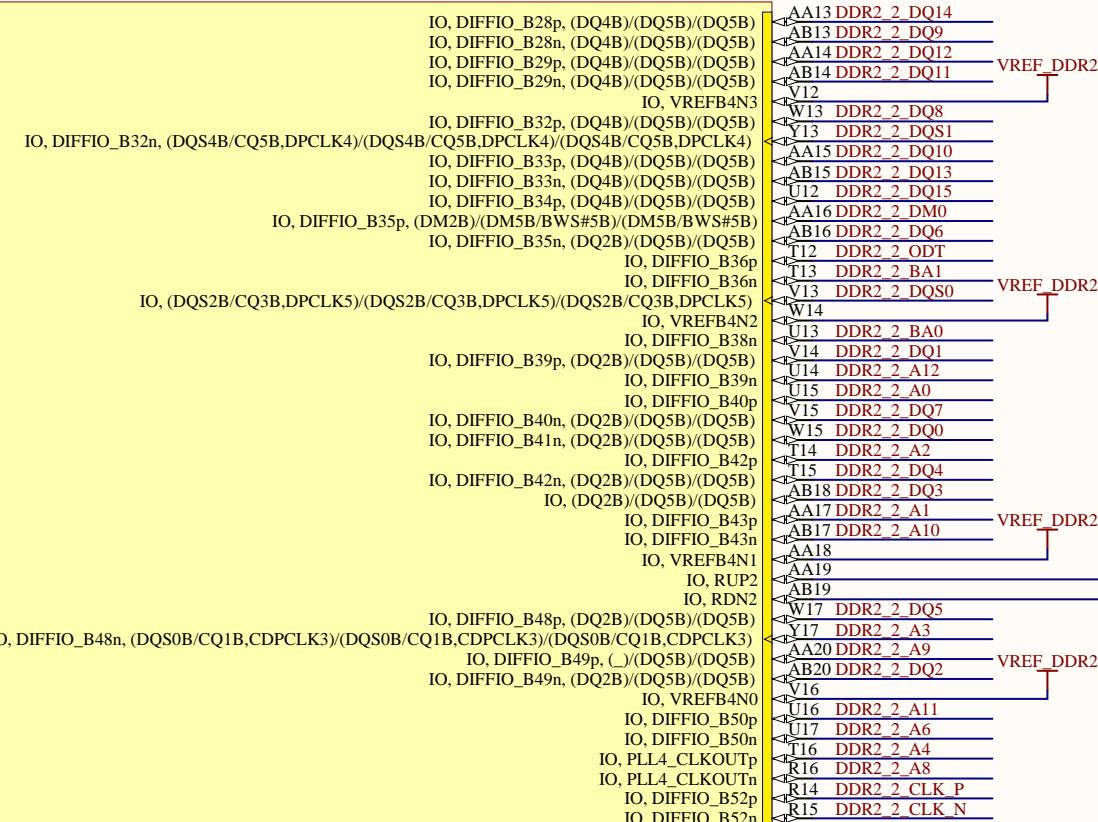


IC8B
BANK 2
VCC1P8



EP4CE40F23C8N

IC8D
BANK 4
VCC1P8



EP4CE40F23C8N

Project name: **LimeSDR-USB_1v4s.PrbPcb**

Title: **FPGA banks 1, 2, 3, 4**

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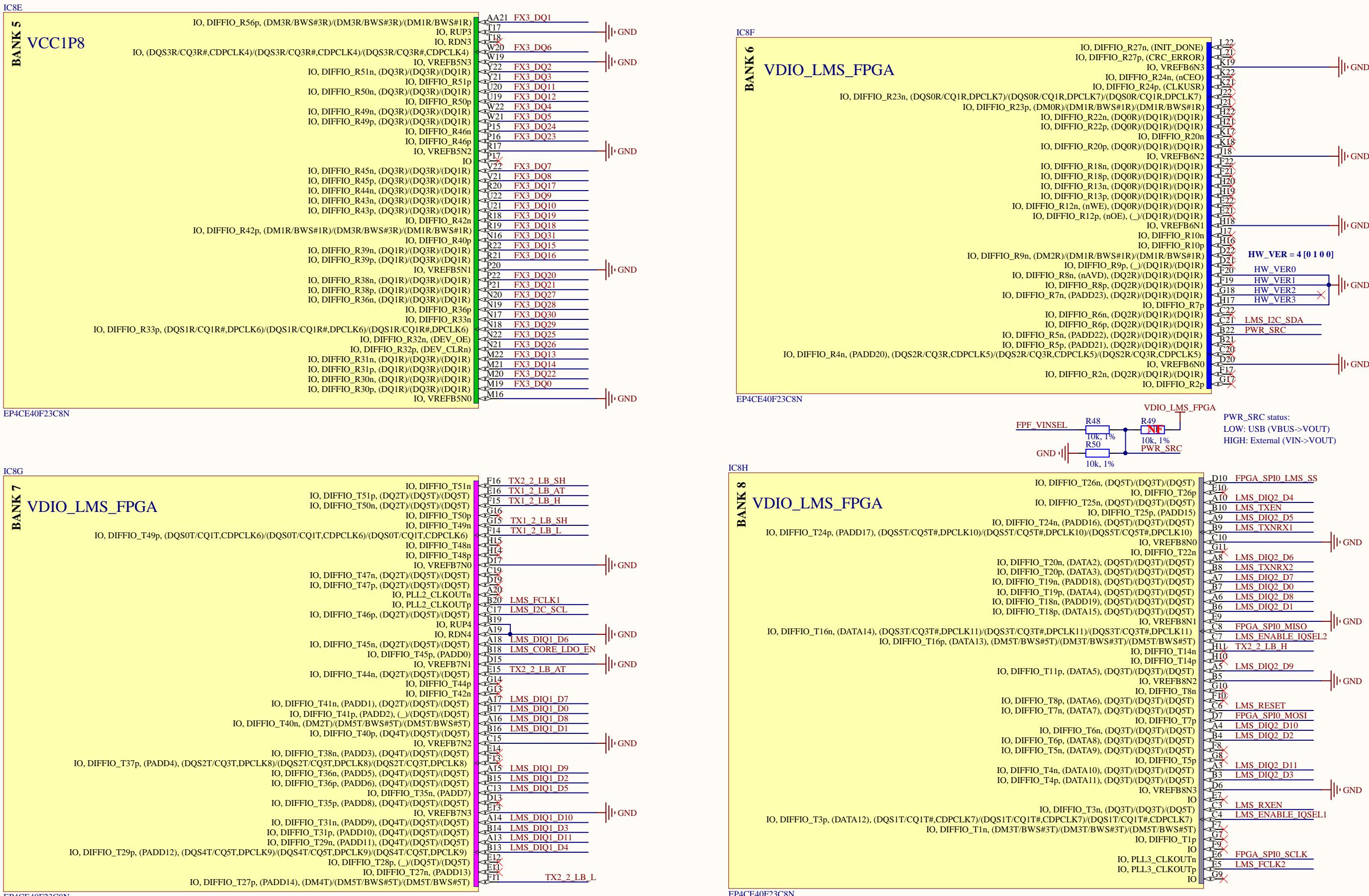
Size: **A3** Revision: **v1.4s**

Date: **2020-09-30** Time: **13:56:52** Sheet **8** of **15**

File: **08_FPGA_banks_1_2_3_4.SchDoc**

NF elements on sheet: R49
Number of NF elements on sheet: 1

FPGA banks 5, 6, 7, 8



Project name: LimeSDR-USB_1v4s.PrfPcb

Title: **FPGA banks 5, 6, 7, 8**

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Size: **A3** Revision: **v1.4s**

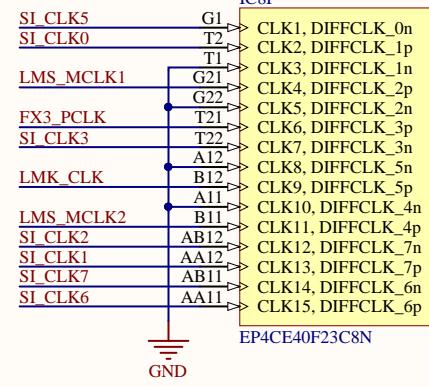
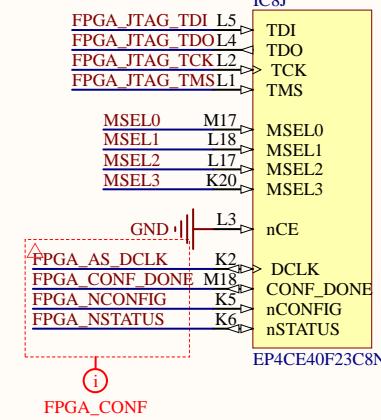
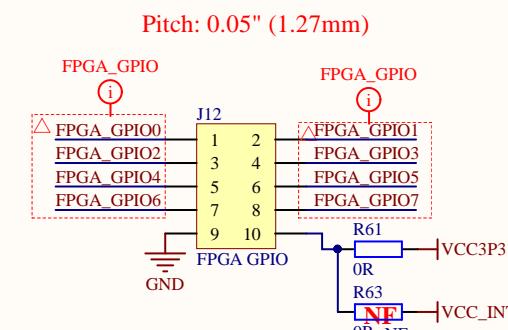
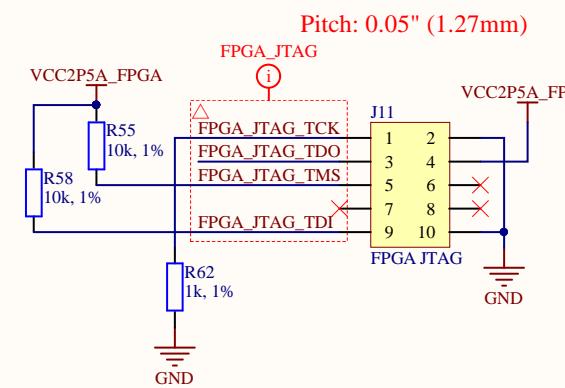
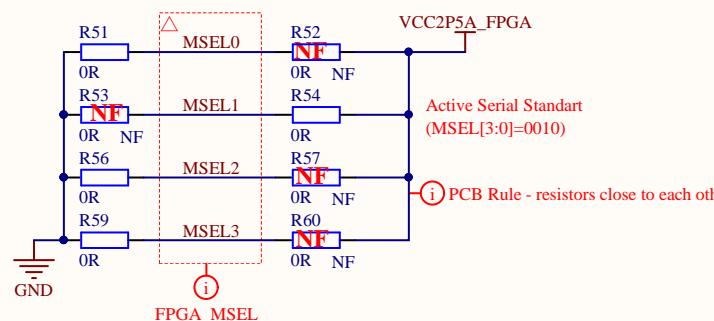
Date: 2020-09-30 Time: 13:56:56 Sheet 9 of 15

File: **09_FPGA_banks_5_6_7_8.SchDoc**

NF elements on sheet: R52, R53, R57, R60, R63, R65, R74, J13, C142
Number of NF elements on sheet: 9

FPGA misc (power, clocks, config)

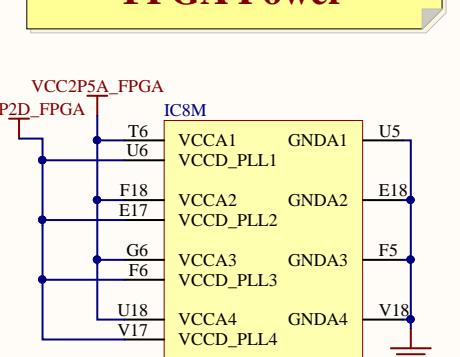
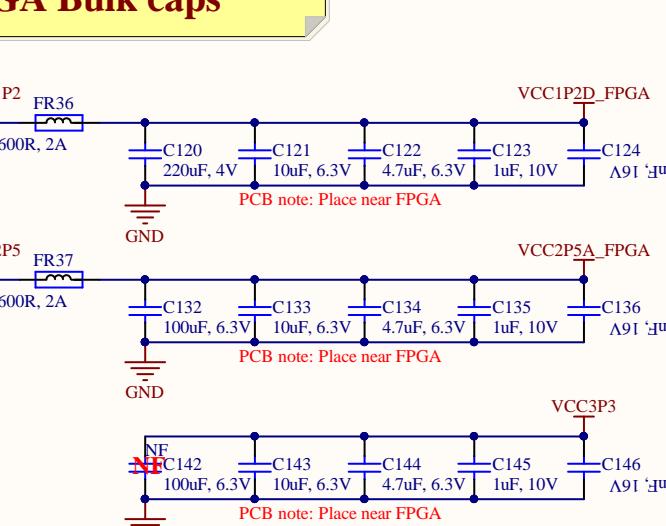
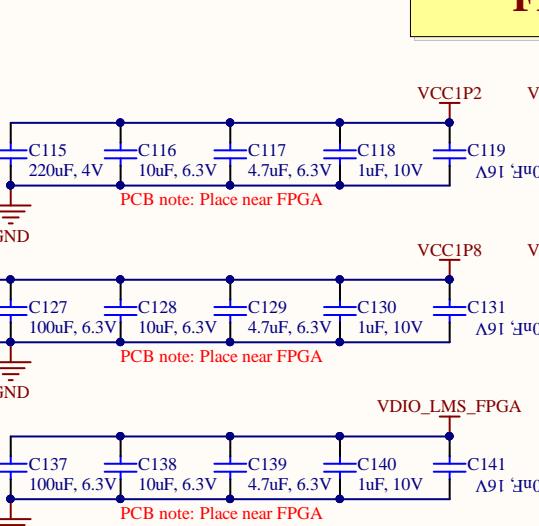
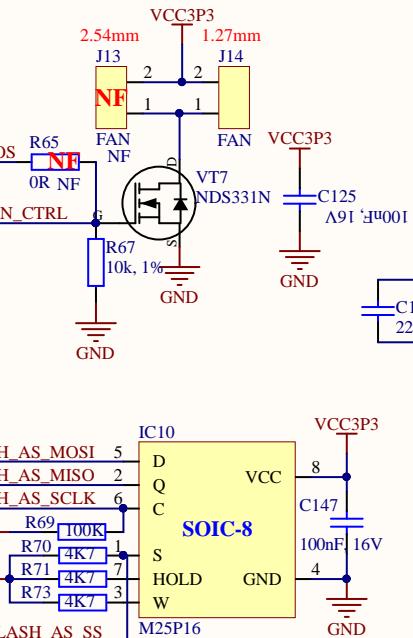
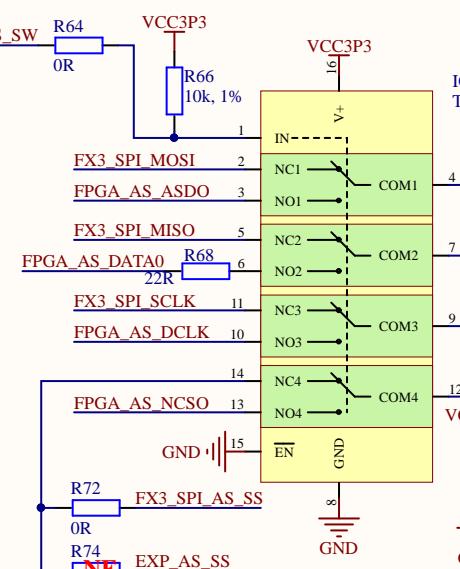
MSEL config



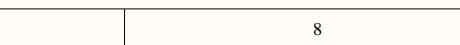
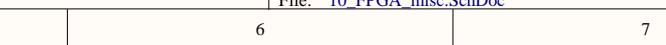
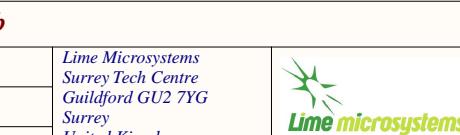
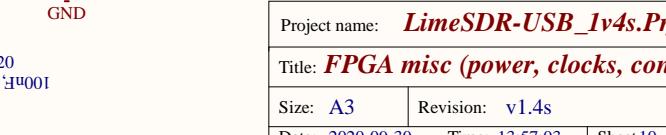
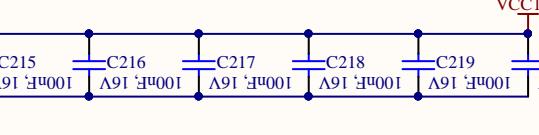
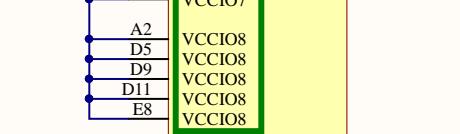
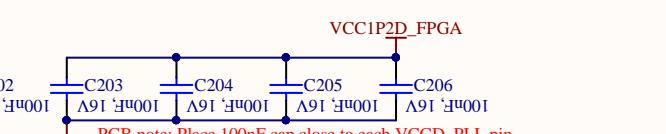
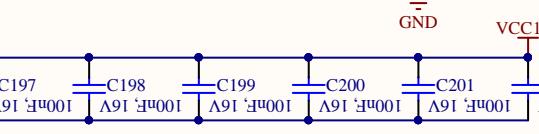
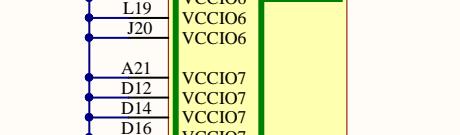
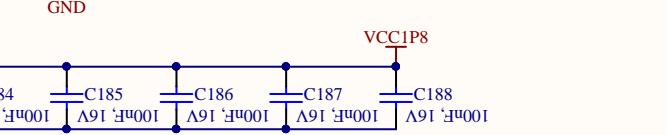
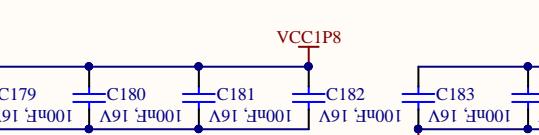
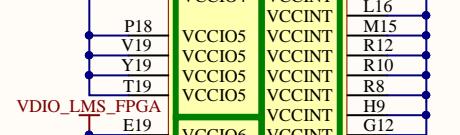
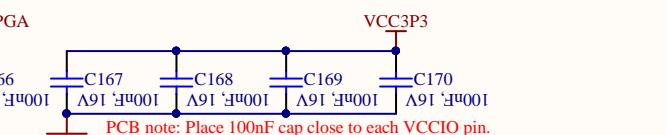
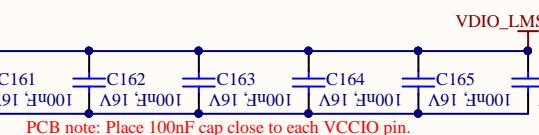
FPGA AS FLASH + Switch

IN:

- 0: FLASH connected to FX3 (NC to COM)
- 1: FLASH connected to FPGA (NO to COM)



FPGA Bulk caps



Project name: LimeSDR-USB_1v4s.PrjPcb

Title: FPGA misc (power, clocks, config)

Size: A3 Revision: v1.4s

Date: 2020-09-30 Time: 13:57:03 Sheet 10 of 15

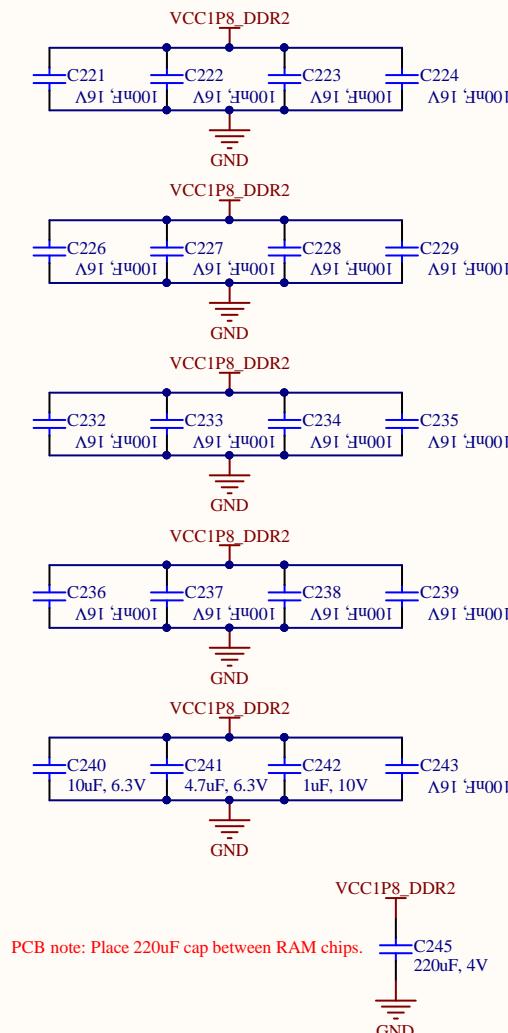
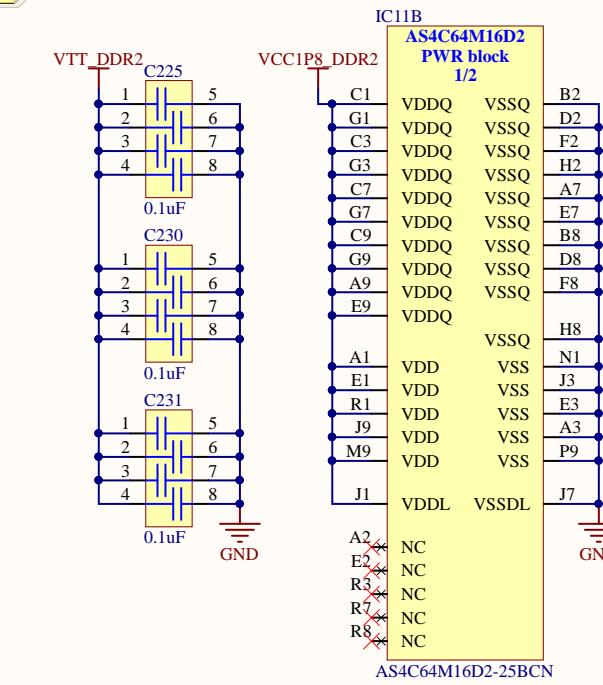
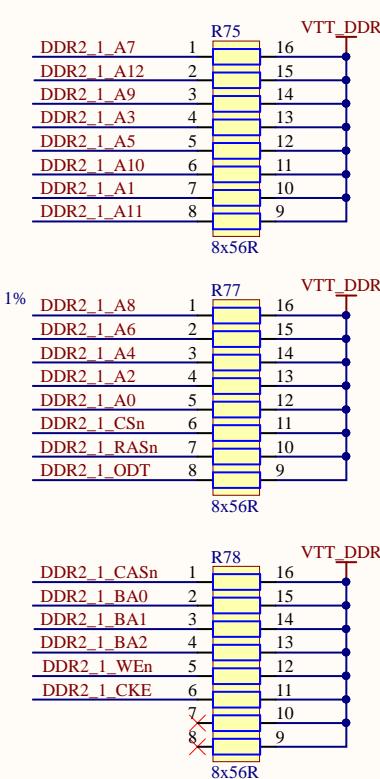
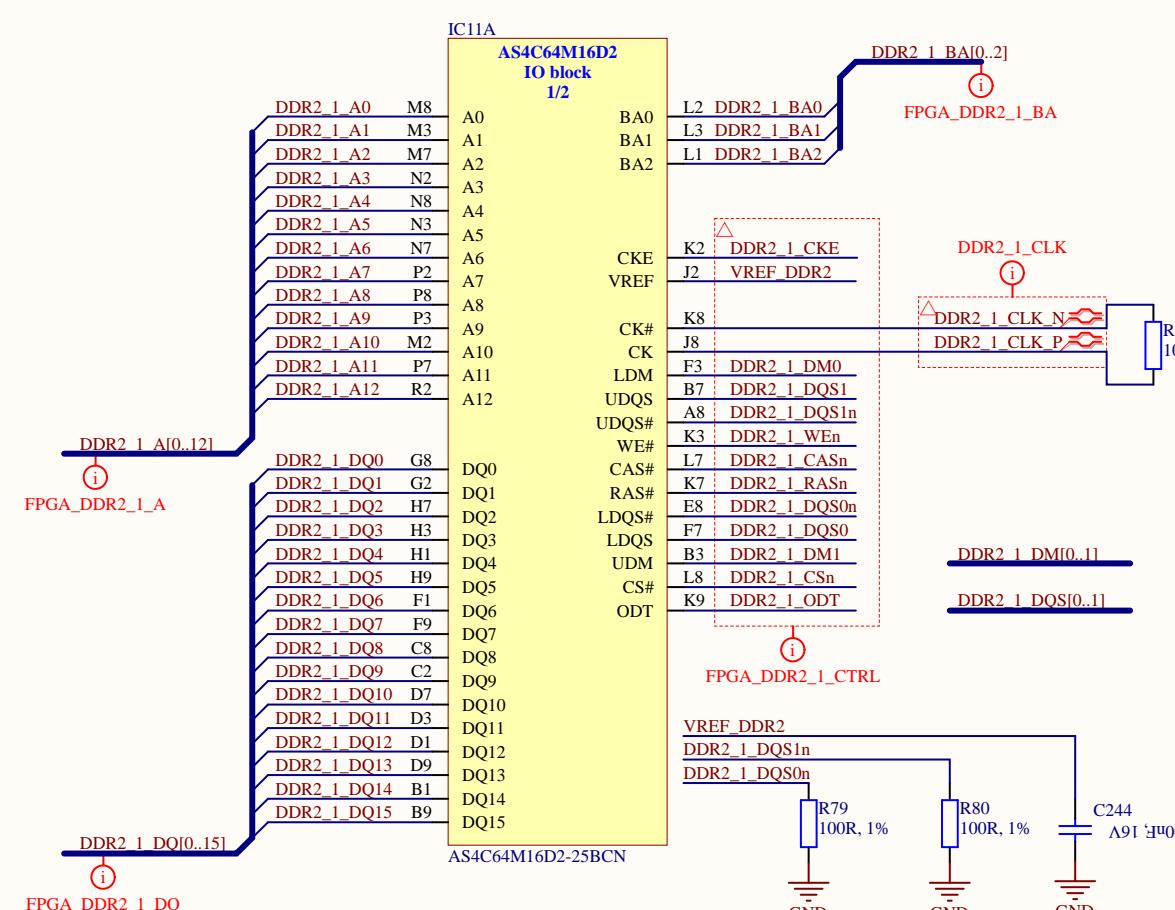
File: 10_FPGA_msc.SchDoc

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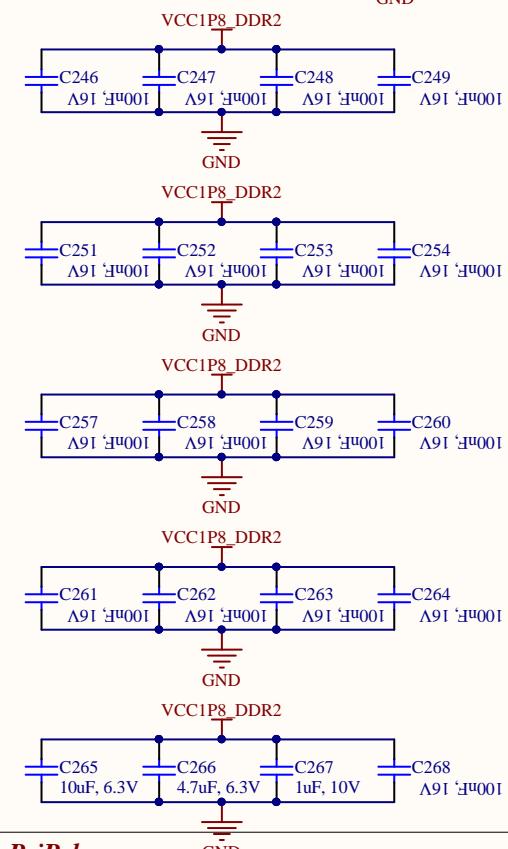
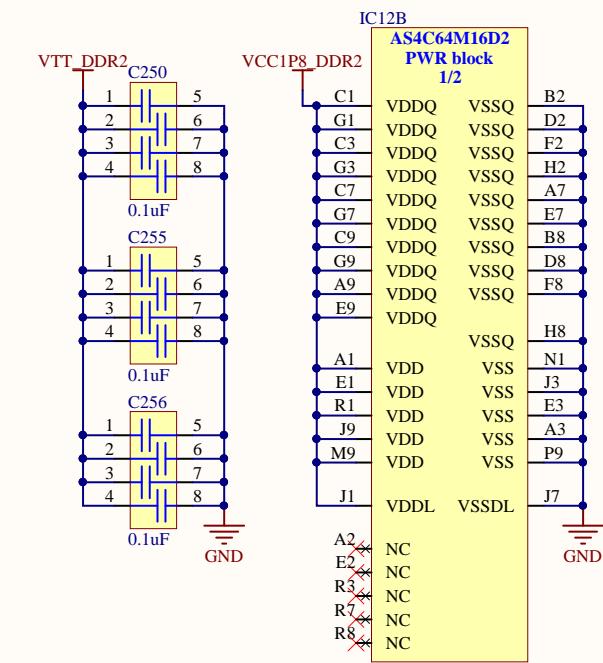
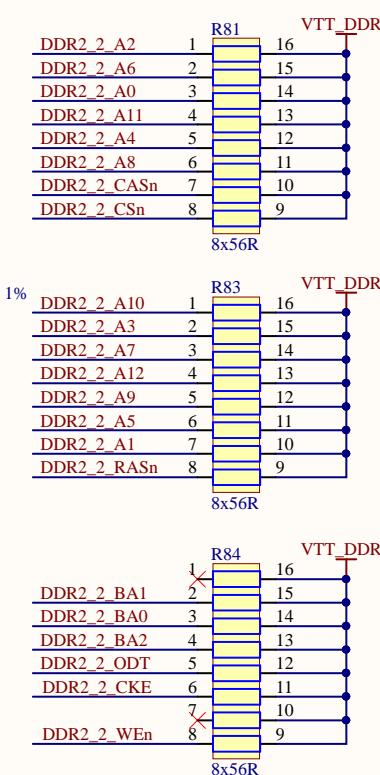
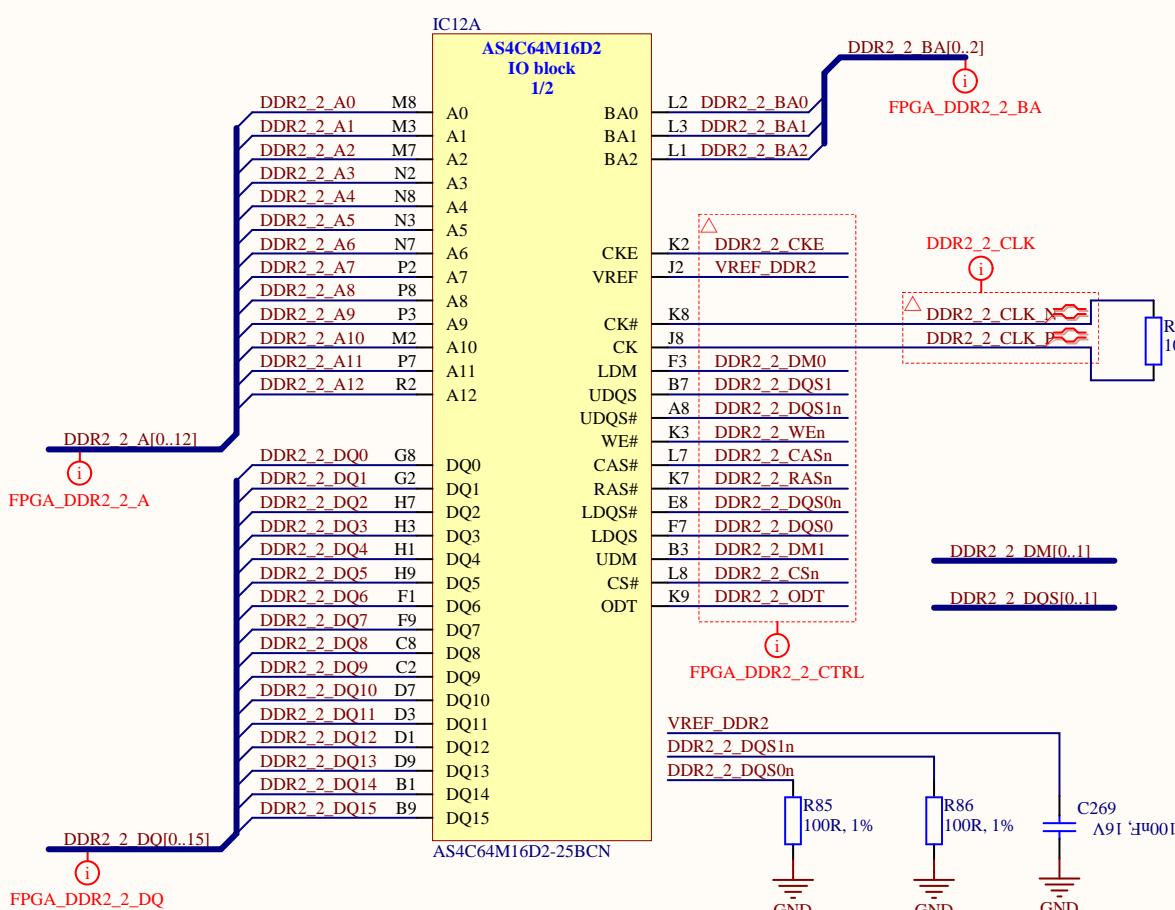


NF elements on sheet: -
Number of NF elements on sheet: 0

DDR2_1 (BOT L)



DDR2_2 (BOT R)



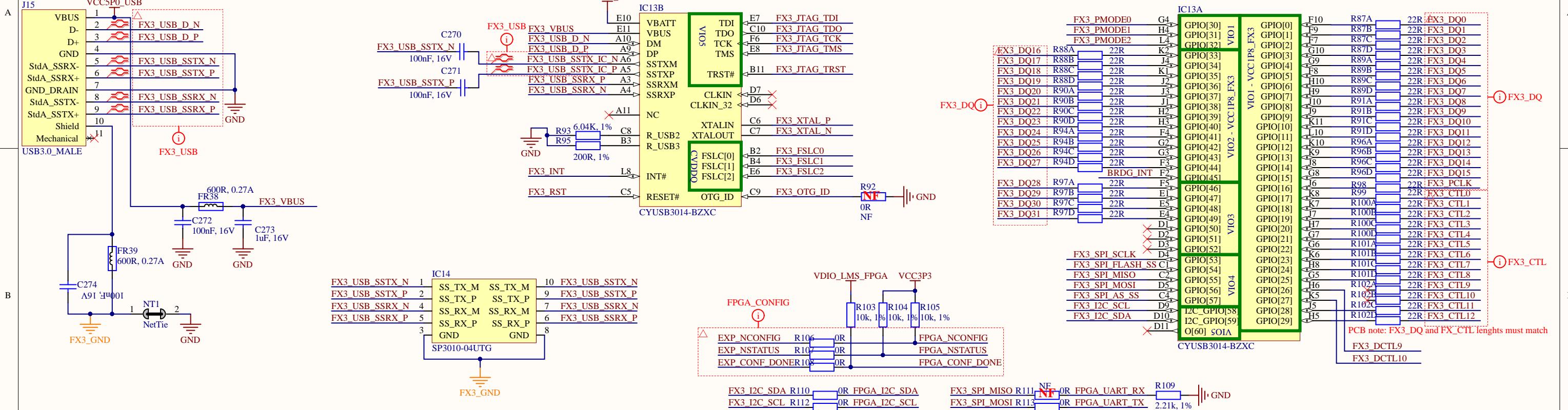
PCB note: Place 220uF cap between RAM chips.

Project name: **LimeSDR-USB_1v4s.PrjPcb**

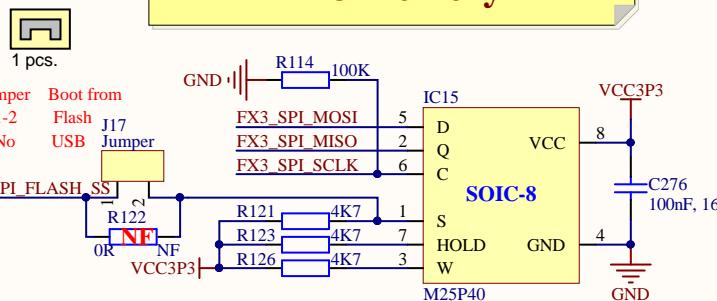
Title: RAM DDR2		<i>Lime Microsystems Surrey Tech Centre Guildford GU2 7YG Surrey United Kingdom</i>	
Size: A3	Revision: v1.4s		
Date: 2020-09-30	Time: 13:57:09	Sheet 11 of 15	
File: 11_DDR2.SchDoc			

NF elements on sheet: R92, R111, R116, R119, R120, R122, R124, IC19
Number of NF elements on sheet: 8

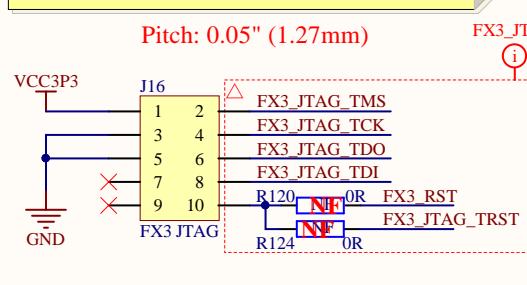
FX3 (USB3) core



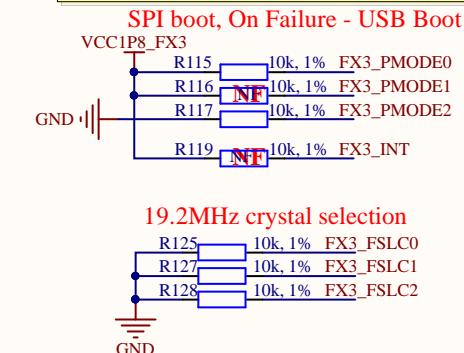
FX3 memory



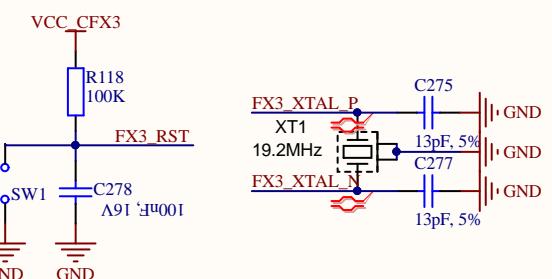
FX3 JTAG (10 pin)



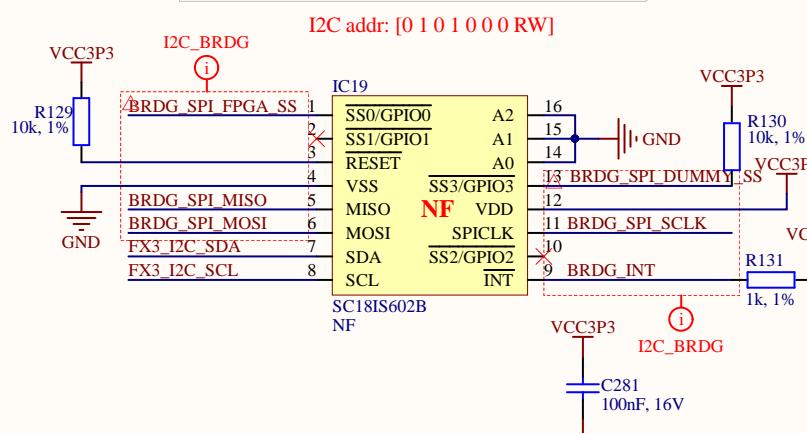
FX3 Config



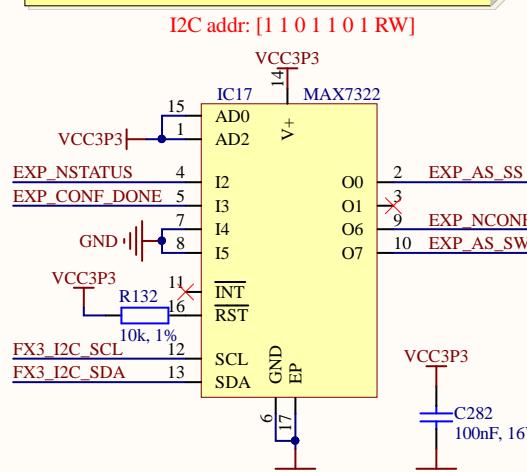
FX3 Misc



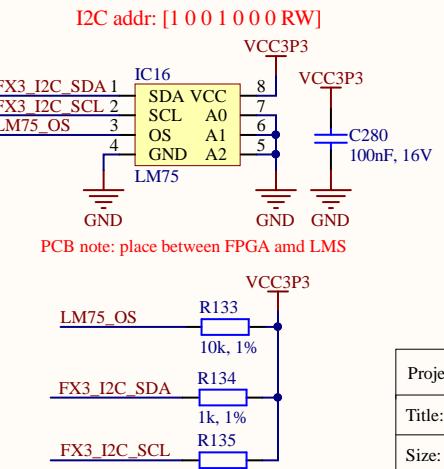
I2C SPI Bridge



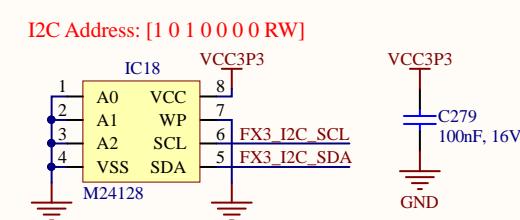
I2C Port Expander



I2C Temperature sensor



I2C EEPROM



Project name: LimeSDR-USB_1v4s.PrbPcb

Title: **USB3.0 device**

Size: **A3** Revision: **v1.4s**

Date: 2020-09-30 Time: 13:57:16 Sheet 12 of 15

File: 12_USB3_0_device.SchDoc

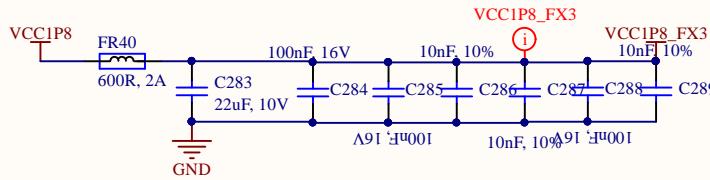
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United Kingdom



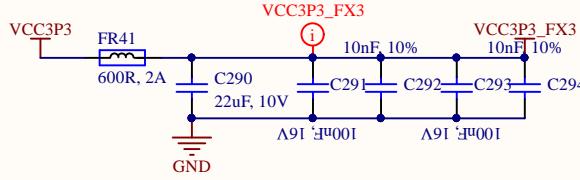
NF elements on sheet: FR42, FR43
Number of NF elements on sheet: 2

USB3 power

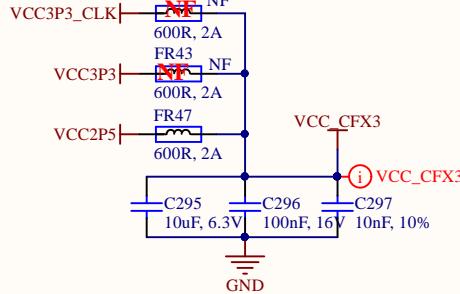
A



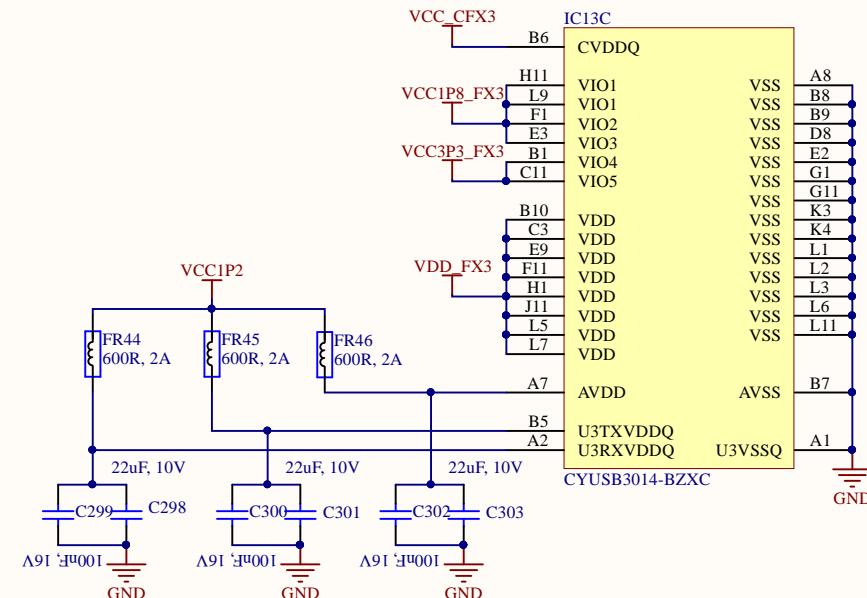
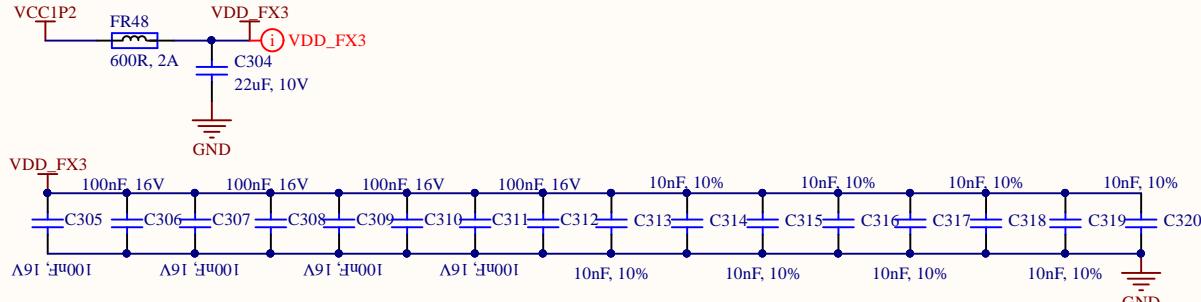
B



C



D



Project name: **LimeSDR-USB_Iv4s.PrfPcb**

Title: **USB3.0 power**

Size: **A4** Revision: **v1.4s**

Date: **2020-09-30** Time: **13:57:23** Sheet**13** of **15**

File: **13_USB3_0_power.SchDoc**

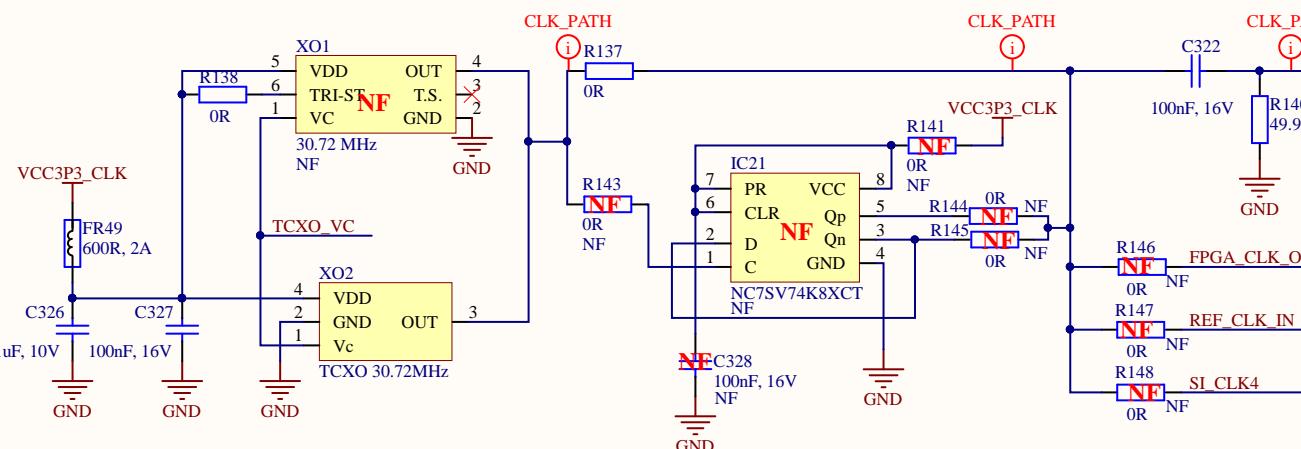
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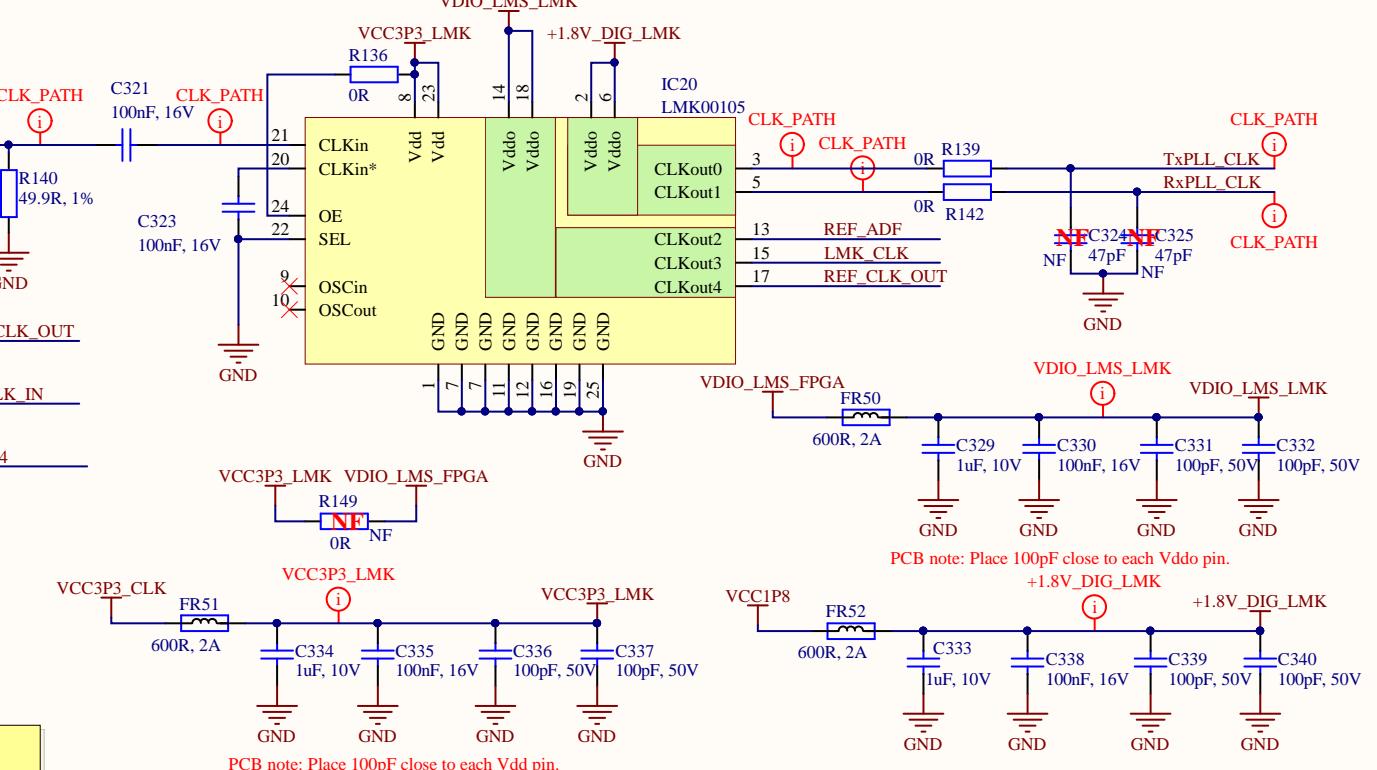
NF elements on sheet: XO1, R141, R143, R144, R145, R146, R147, R148, R149, R151, R155, C324, C325, C328, C341, IC21
Number of NF elements on sheet: 16

Clock circuits

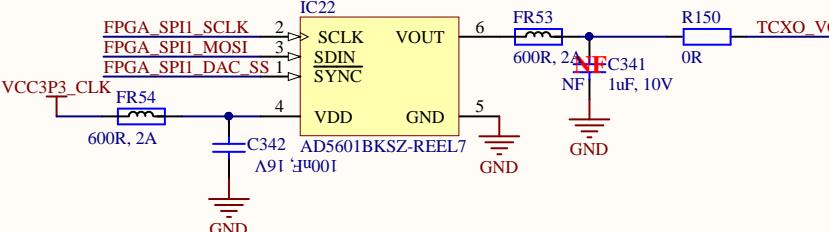
(VC)TCXO



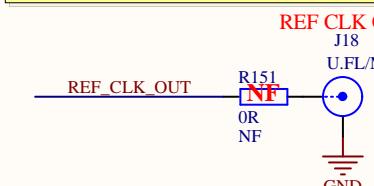
Clock buffer



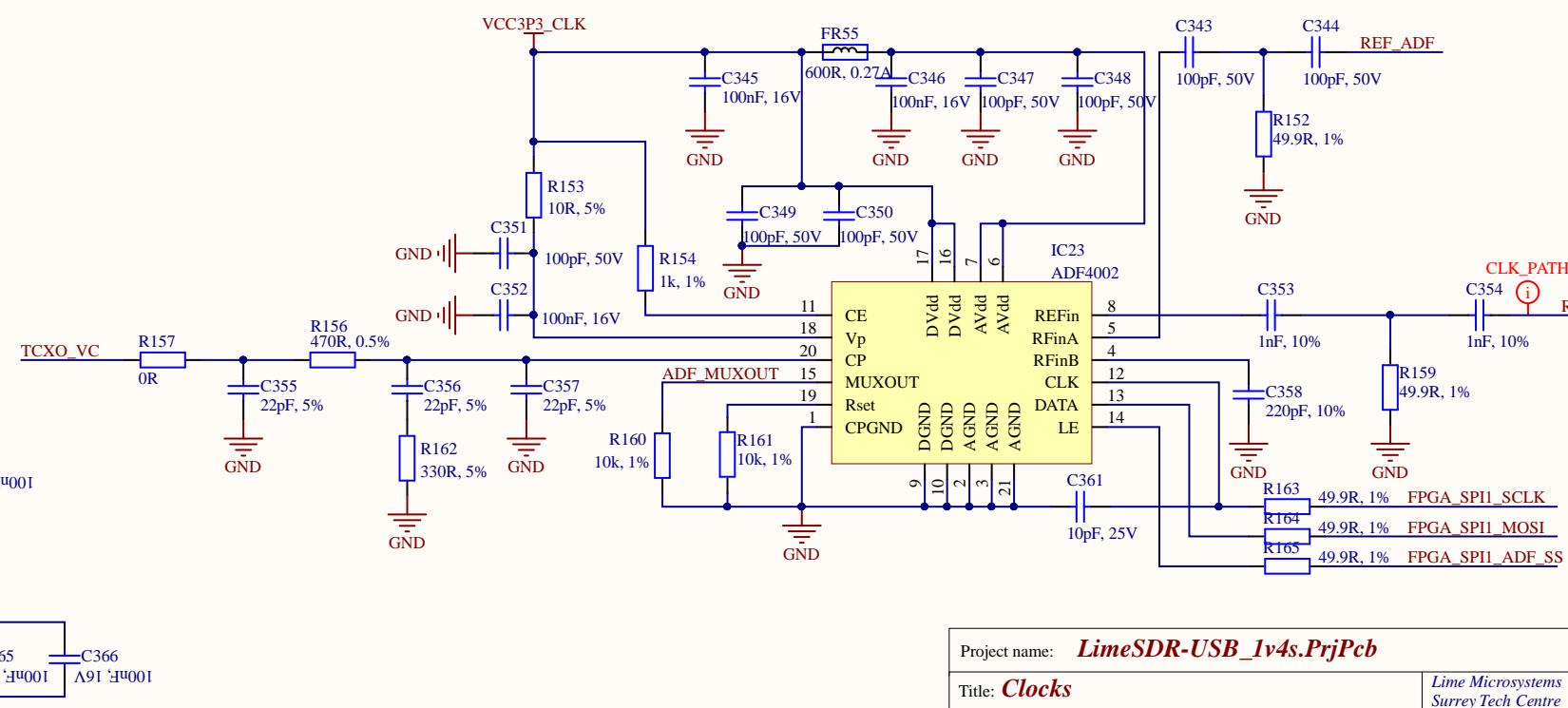
TCXO DAC



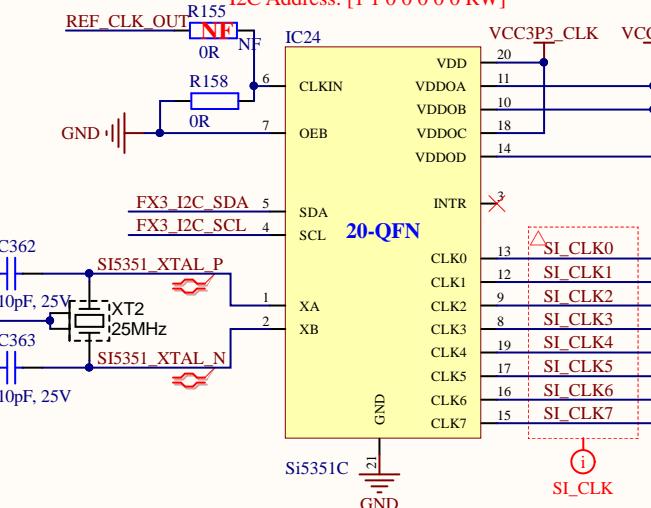
REF CLK OUT



Phase detector



Clock generator



Project name: LimeSDR-USB_1v4s.PrbPcb

Title: Clocks

Size: A3

Revision: v1.4s

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Date: 2020-09-30

Time: 13:57:28

Sheet 14 of 15

File: 14_Clocks.SchDoc

