Indian Institute of Information Technology
Sonepat

Digital System Design Lab
(CSL-309)
Practical File

Submitted To
Dr. Rajiv Verma

Submitted By-
Shivansh Joshi
Branch- CSE
Roll No.: 12011042

EXPERIMENT No.08

AIM

To implement J-K Flip Flop in VHDL.

CODE

```
library IEEE;
use IEEE.STD_Logic_1164.ALL;


entity jkflipflop is
        Port(clk, j, k : in STD_logic;
        q, qbar : out STD_logic);
end jkflipflop;
architecture Behavioral of jkflipflop is
begin
        process(j,k,clk)
        variable temp:std_logic;
        begin
                if(clk = '1' and clk'event) then
                        if(j='0' and k ='0')then
                                temp:=temp;
                                elsif(j='1' and k='1')then
                                temp:=not temp;
                                elsif(j='0' and k='1')then
                                        temp:='0';
```

```
        else
            temp:='1';
        end if;
        end if;
        q<=temp;
        qbar<=not temp;
    end process;
    end Behavioral;
```

OUTPUT