Indian Institute of Information Technology
Sonepat

Digital System Design Lab
(CSL-309)
Practical File

Submitted To
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Submitted By-
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EXPERIMENT No.07

AIM:

To implement D Flip Flop using VHDL.

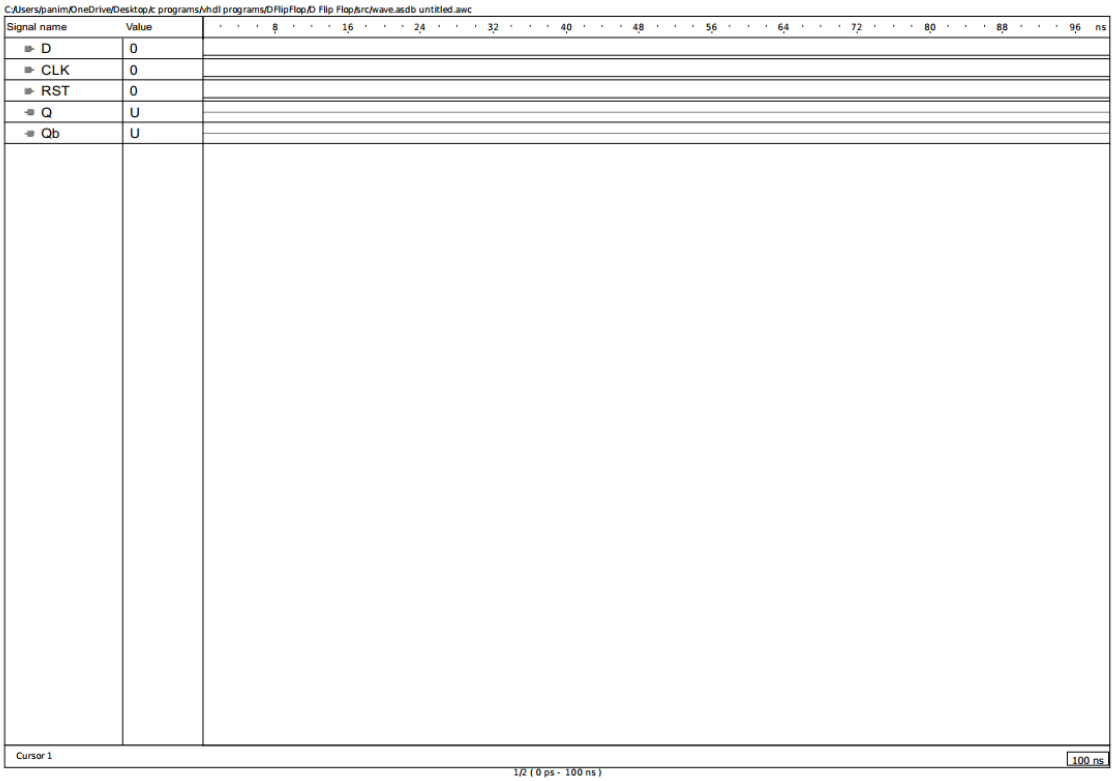
CODE:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity D_FLIPFLOP_SOURCE is
Port ( D, CLK, RST : in  STD_LOGIC;
Q, Qb : out  STD_LOGIC);
end D_FLIPFLOP_SOURCE;
architecture Behavioral of D_FLIPFLOP_SOURCE is
begin
process (D, CLK, RST)
begin
if (RST = '1') then
Q <= '0';
elsif (rising_edge(CLK)) then ---this is for data flip-flop, for delay flip-flop
use negative edge
Q <= D;
Qb <= not D;
end if;
end process;
```

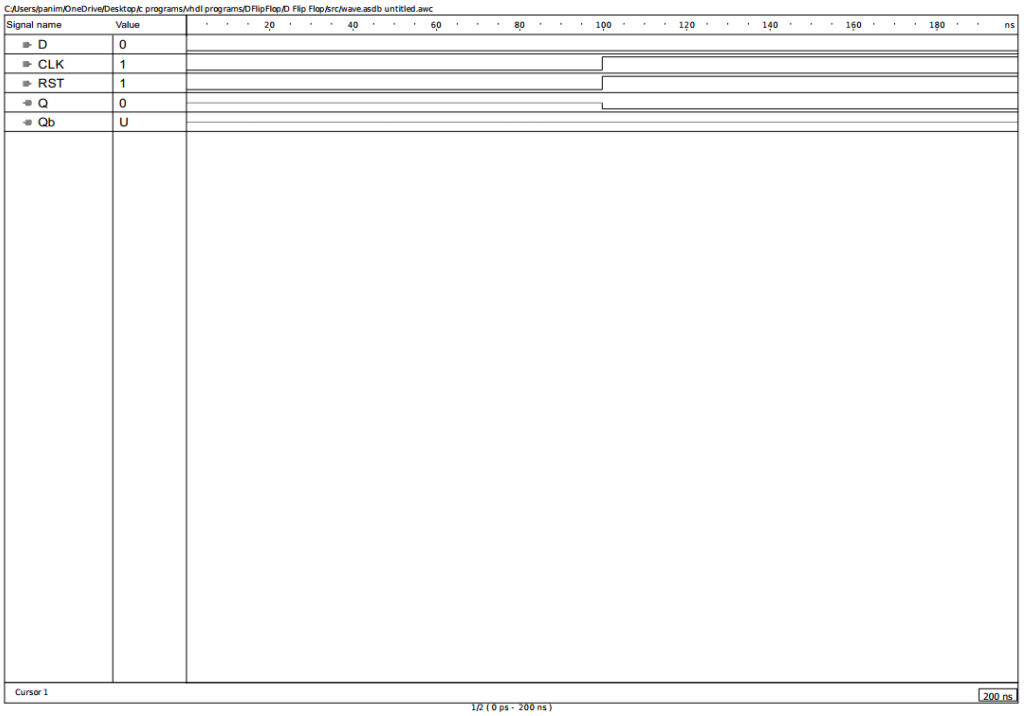
end Behavioral;

OUTPUT

- **When D = 0, Clock = 0, Reset = 0**



- **When D = 0, Clock = 1, Reset = 1**



- **When D = 1, Clock = 1, Reset = 0**