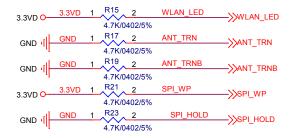
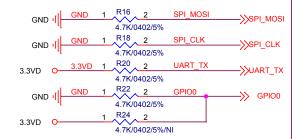


## MTK7620N BOOT





## MT7620N Boot Up Strapping

Pin Name	Description	Value
WLED_N	DRAM_FROM_EE For non scan mode:	0: DRAM configuration from EEPROM 1: DRAM configuration from Auto Detect
ANT_TRN	DBG_JTAG_MODE	0: EPHY_LED 1: JTAG MODE
ANT_TRNB	XTAL_FREQ_SEL	0: 20MHz 1: 40MHz
{SPI_WP, SPI_HOLD}	DRAM_TYPE	01: DDR1 (CPU/3) TSOP Package 10: DDR2 (CPU/3) FBGA Package * 11: SDRAM (CPU/5) (LVTTL 3.3 V) TSOP Package
{SPI_MOSI SPI_CLK, TXD2, GPIO0 }	CHIP_MODE[3:0]	A vector to set chip function/test/debug modes. In non-test/debug operation,  0010: Normal mode (boot from SPI 3Byte Addr)

## MTK7620N Ethernet Close to MT7620N U1E 3.3VD 117 117 119 122 EPHY\_V33A EPHY\_V33A MDI\_TN\_P4 MDI\_TP\_P4 MDI\_RN\_P4 MDI\_RP\_P4 100nF/0402 EPHY\_V33A ~ C46 SOC\_1.2VD GND MDI\_TN\_P3 MDI\_TP\_P3 MDI\_RN\_P3 MDI\_RP\_P3 114 123 120 EPHY\_V12A EPHY\_V12A 100nF/0402 2 1 2 873 EPHY\_PLL\_V12A R25 2 GND 43 EPHY RES VBG 6.19K/0402/1% MDI\_TN\_P2 MDI\_TP\_P2 MDI\_RN\_P2 MDI\_RP\_P2 ->>TXON2 ->>TXOP2 GND JTAG\_TRST\_D29 </-JTAG\_TCK\_D26 </-> JTAG\_TMS\_D25 </-> 9 7 EPHY\_LED3\_N\_JTCLK SRXIN2 EPHY LED2 N JTMS JTAG\_TDI\_D27 82 EPHY\_LED1\_N\_JTDI EPHY\_LED0\_N\_JTDO JTAG\_TDO\_D28 38 MDI\_RP\_P0 MDI\_RP\_P0 MDI\_TP\_P0 MDI\_TN\_P0 MT7620N Close to MT7620N 深圳市摩仑科技有限公司 Custom Intorobot Document Number <Doc> 2.0 Sheet 5 of 9 Rev Sunday, June 28, 2015

Design By: Hardware Team

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