National Semiconductor

DM54S189/DM74S189 64-Bit (16 x 4) TRI-STATE® RAM DM54S189A/DM74S189A High Speed 64-Bit TRI-STATE RAM

General Description

These 64-bit active-element memories are monolithic Schottky-clamped transistor-transistor logic (TTL) arrays organized as 16 words of 4 bits each. They are fully decoded and feature a chip-enable input to simplify decoding required to achieve the desired system organization. The memories feature PNP input transistors that reduce the low level input current requirement to a maximum of −0.25 mA, only one-eighth that of a DM74S standard load factor. The chip-enable circuitry is implemented with minimal delay times to compensate for added system decoding.

The TRI-STATE output combines the convenience of an open-collector with the speed of a totem-pole output; it can be bus-connected to other similar outputs; yet it retains the fast rise time characteristics of the TTL totem-pole output. Systems utilizing data bus lines with a defined pull-up impedance can employ the open-collector DM74S289.

Write Cycle: The complement of the information at the data input is written into the selected location when both the chip-enable input and the read/write input are low. While the read/write input is low, the outputs are in the high-impedance state. When a number of the DM74S189 outputs are bus connected, this high-impedance state will neither load nor drive the bus line, but it will allow the bus line to be driven by another active output or a passive pull-up if desired.

Read Cycle: The stored information (complement of information applied at the data inputs during the write cycle) is available at the outputs when the read/write input is high and the chip-enable is low. When the chip-enable is high, the outputs will be in the high-impedance state.

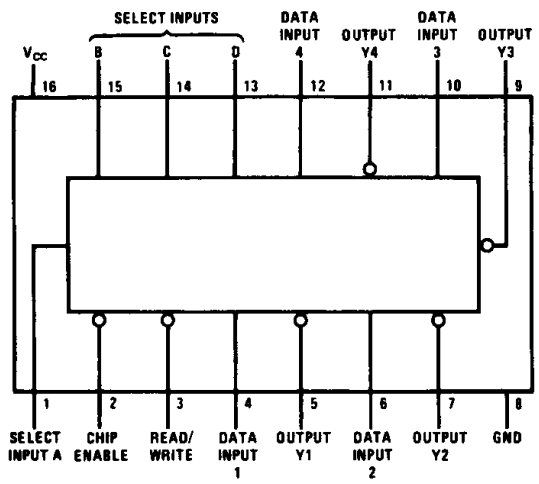
The fast access time of the DM74S189A makes it particularly attractive for implementing high-performance memory functions requiring access times less than 25 ns. The high capacitive drive capability of the outputs permits expansion without additional output buffering. The unique functional capability of the DM74S189A outputs being at a high-impedance during writing, combined with the data inputs being inhibited during reading, means that both data inputs and outputs can be connected to the data lines of a bus-organized system without the need for interface circuits.

Features

- Schottky-clamped for high speed applications (S189A)
  - Access from chip-enable input 17 ns max
  - Access from address inputs 25 ns max
- TRI-STATE outputs drive bus-organized systems and/or high capacitive loads (S189, S189A)
- DM74S289 are functionally equivalent and have open-collector outputs
- DM54SXXX is guaranteed for operation over the full military temperature range of −55°C to +125°C
- Compatible with most TTL circuits
- Chip-enable input simplifies system decoding

Connection Diagram

Dual-In-Line Package



TL/D/9232–1

Top View

Truth Table

Function	Inputs		Output
	Chip-Enable	Read/Write	
Write (Store Complement of Data)	L	L	High-Impedance
Read	L	H	Stored Data
Inhibit	H	X	High-Impedance

H = High Level, L = Low Level, X = Don't Care

Order Number DM54S189J, DM54S189AJ, DM74S189J, DM74S189AJ, DM74S189N or DM74S189AN
See NS Package Number J16A or N16E

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC}	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DM54S189	4.5	5.5	V
DM74S189	4.75	5.25	V
Temperature (T_A)			
DM54S189	−55	+125	°C
DM74S189	0	+70	°C

DM54S189, DM74S189 Electrical Characteristics

over recommended operating free-air temperature range unless otherwise noted (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
V_{OH}	High Level Output Voltage	V_{CC} = Min	I_{OH} = −2.0 mA, DM54S189	2.4	3.4		V
			I_{OH} = −6.5 mA, DM74S189	2.4	3.2		V
I_{CEX}	High Level Output Current Open Collector Only	V_{CC} = Min	V_{OH} = 2.4V			40	μA
			V_{OH} = 5.5V			100	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA	DM54S189			0.5	V
			DM74S189			0.45	V
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				25	μA
I_I	High Level Input Current at Maximum Voltage	V_{CC} = Max, V_I = 5.5V				1.0	mA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.45V				−250	μA
I_{OS}	Short Circuit Output Current (Note 4)	V_{CC} = Max, V_O = 0V	DM54S189, DM74S189	−30		−100	mA
I_{CC}	Supply Current (Note 5)	V_{CC} = Max			75	110	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
I_{OZH}	TRI-STATE Output Current, High Level Voltage Applied	V_{CC} = Max, V_O = 2.4V	DM54S189, DM74S189			50	μA
I_{OZL}	TRI-STATE Output Current, Low Level Voltage Applied	V_{CC} = Max, V_O = 0.45V	DM54S189, DM74S189	−50			μA
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz			4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "Off"			6.0		pF

5

DM74S189 Switching Characteristics

over recommended operating ranges of T_A and V_{CC} unless otherwise noted

Symbol	Parameter		Conditions	DM54S189			DM74S189			Units
				Min	Typ (Note 2)	Max	Min	Typ (Note 2)	Max	
t_{AA}	Access Times from Address		C_L = 30 pF, R_L = 280Ω *(Figure 4)*		25	50		25	35	ns
t_{CZH}	Output Enable Time to High Level	Access Times from Chip-Enable			12	25		12	17	ns
t_{CZL}	Output Enable Time to Low Level				12	25		12	17	ns
t_{WZH}	Output Enable Time to High Level	Sense Recovery Times from Read/Write			13	35		13	25	ns
t_{WZL}	Output Enable Time to Low Level				13	35		13	25	ns
t_{CHZ}	Output Disable Time from High Level	Disable Times from Chip-Enable	C_L = 5 pF, R_L = 280Ω *(Figure 4)*		12	25		12	17	ns
t_{CLZ}	Output Disable Time from Low Level				12	25		12	17	ns
t_{WHZ}	Output Disable Time from High Level	Disable Times from Read/Write			15	35		15	25	ns
t_{WLZ}	Output Disable Time from Low Level				15	35		15	25	ns
t_{WP}	Width of Write Enable Pulse (Read/Write Low)			25			25			ns
t_{ASW}	Set-Up Time *(Figure 1)*	Address to Read/Write		0			0			ns
t_{DSW}		Data to Read/Write		25			25			ns
t_{CSW}		Chip-Enable to Read/Write		0			0			ns
t_{AHW}	Hold Time *(Figure 1)*	Address from Read/Write		0			0			ns
t_{DHW}		Data from Read/Write		0			0			ns
t_{CHW}		Chip-Enable from Read/Write		0			0			ns

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC}	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	+300°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DM54S189(A)	4.5	5.5	V
DM74S189(A)	4.75	5.25	V
Temperature (T_A)			
DM54S189(A)	−55	+125	°C
DM74S189(A)	0	+70	°C

DM54S189A, DM74S189A Electrical Characteristics

over recommended operating free-air temperature range unless otherwise noted (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
V_{OH}	High Level Output Voltage	V_{CC} = Min	I_{OH} = −2.0 mA, DM54S189A	2.4	3.4		V
			I_{OH} = −6.5 mA, DM74S189A	2.4	3.2		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min	I_{OL} = 16 mA			0.45	V
			I_{OL} = 20 mA			0.5	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				10	μA
I_I	High Level Input Current at Maximum Voltage	V_{CC} = Max, V_I = 5.5V				1.0	mA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.40V				−250	μA
I_{OS}	Short Circuit Output Current (Note 4)	V_{CC} = Max, V_O = 0V		−20		−90	mA
I_{CC}	Supply Current (Note 5)	V_{CC} = Max			75	100	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
I_{OZH}	TRI-STATE Output Current, High Level Voltage Applied	V_{CC} = Max, V_O = 2.4V				40	μA
I_{OZL}	TRI-STATE Output Current, Low Level Voltage Applied	V_{CC} = Max, V_O = 0.4V		−40			μA
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz			4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "Off"			6.0		pF

DM54S189A, DM74S189A Switching Characteristics

over recommended operating ranges of T_A and V_{CC} unless otherwise noted

Symbol	Parameter		Conditions	DM54S189A			DM74S189A			Units
				Min	Typ (Note 2)	Max	Min	Typ (Note 2)	Max	
t_{AA}	Access Time from Address		C_L = 30 pF, R_L = 280Ω *(Figure 4)*		20	30		20	25	ns
t_{CZH}	Output Enable Time to High Level	Access Times from Chip-Enable			11	25		11	17	ns
t_{CZL}	Output Enable Time to Low Level				11	25		11	17	ns
t_{WZH}	Output Enable Time to High Level	Sense Recovery Times from Read/Write			13	35		13	25	ns
t_{WZL}	Output Enable Time to Low Level				13	35		13	25	ns
t_{CHZ}	Output Disable Time from High Level	Disable Times from Chip-Enable	C_L = 5 pF, R_L = 280Ω *(Figure 4)*		12	25		12	17	ns
t_{CLZ}	Output Disable Time from Low Level				12	25		12	17	ns
t_{WHZ}	Output Disable Time from High Level	Disable Times from Read/Write			15	35		15	25	ns
t_{WLZ}	Output Disable Time from Low Level				15	35		15	25	ns
t_{WP}	Width of Write Enable Pulse (Read/Write Low)			25			20			ns
t_{ASW}	Set-Up Time *(Figure 1)*	Address to Read/Write		0			0			ns
t_{DSW}		Data to Read/Write		25			20			ns
t_{CSW}		Chip-Enable to Read/Write		0			0			ns
t_{AHW}	Hold Time *(Figure 1)*	Address from Read/Write		0			0			ns
t_{DHW}		Data from Read/Write		0			0			ns
t_{CHW}		Chip-Enable from Read/Write		0			0			ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM54S189(A) and across the 0°C to +70°C range for the DM74S189(A). All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

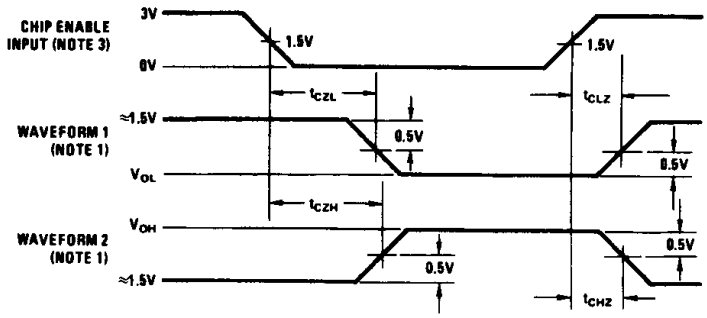
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: I_{CC} is measured with all inputs grounded; and the outputs open.

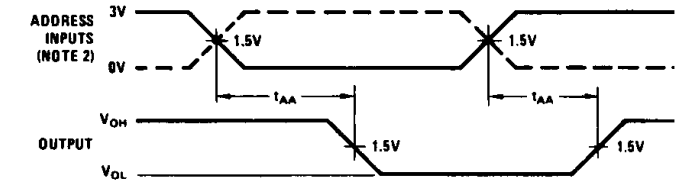
DM54S189(A), DM74S189(A) Switching Time Waveforms

Enable and Disable Time from Chip-Enable



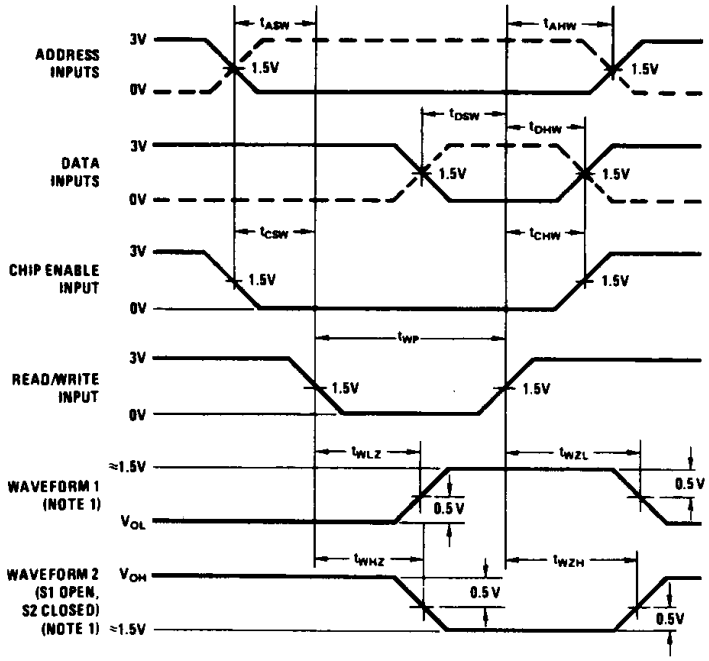
TL/D/9232-2

Access Time from Address Inputs



TL/D/9232-3

Write Cycle



TL/D/9232-4

FIGURE 1

Note 1: Waveform 1 is for the output with internal conditions such that the output is low except when disabled. Waveform 2 is for the output with internal conditions such that the output is high except when disabled.

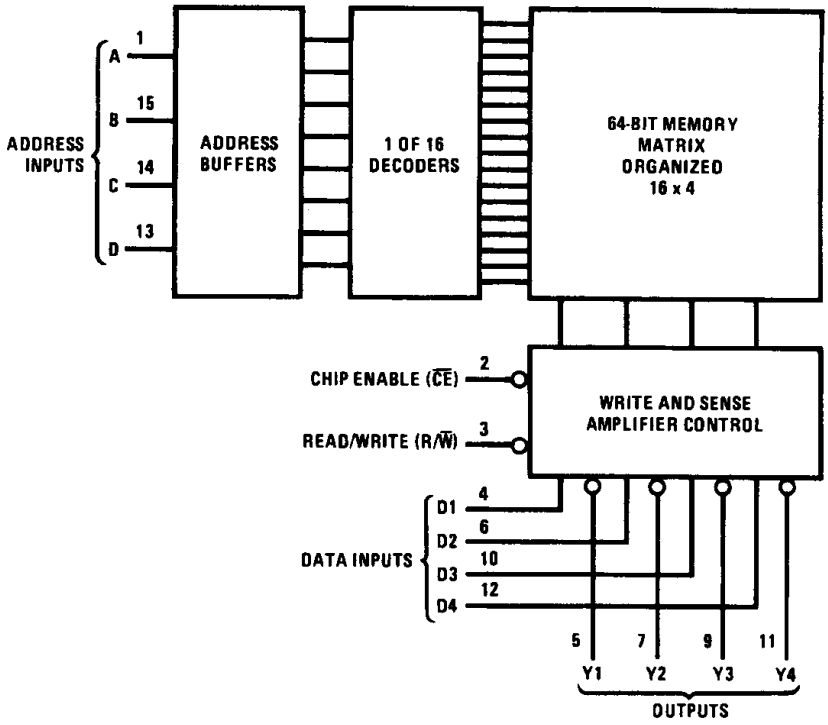
Note 2: When measuring delay times from address inputs, the chip-enable input is low and the read/write input is high.

Note 3: When measuring delay times from chip-enable input, the address inputs are steady-state and the read/write input is high.

Note 4: Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns, PRR ≤ 1 MHz and $Z_{OUT} = \approx 50\Omega$.

5

Block Diagram

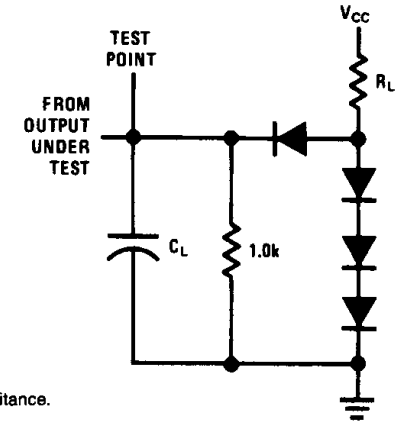


TL/D/9232–5

FIGURE 3

AC Test Circuits

DM54S189(A)/DM74S189(A)



C_L includes probe and jig capacitance.
All diodes are 1N3064.

TL/D/9232–6

FIGURE 4

National Semiconductor was acquired by Texas Instruments.

http://www.ti.com/corp/docs/investor_relations/pr_09_23_2011_national_semiconductor.html

This file is the datasheet for the following electronic components:

DM54S189AJ - http://www.ti.com/product/dm54s189aj?HQS=TI-null-null-dscatalog-df-pf-null-wwe

DM74S189N - http://www.ti.com/product/dm74s189n?HQS=TI-null-null-dscatalog-df-pf-null-wwe

DM74S189J - http://www.ti.com/product/dm74s189j?HQS=TI-null-null-dscatalog-df-pf-null-wwe

DM54S189J - http://www.ti.com/product/dm54s189j?HQS=TI-null-null-dscatalog-df-pf-null-wwe

DM74S189AN - http://www.ti.com/product/dm74s189an?HQS=TI-null-null-dscatalog-df-pf-null-wwe

DM74S189AJ - http://www.ti.com/product/dm74s189aj?HQS=TI-null-null-dscatalog-df-pf-null-wwe