

# Dual 4-Stage Binary Ripple Counter

## High-Performance Silicon-Gate CMOS

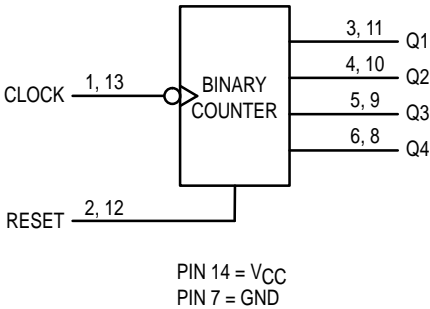
The MC54/74HC393 is identical in pinout to the LS393. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of two independent 4-bit binary ripple counters with parallel outputs from each counter stage. A ÷ 256 counter can be obtained by cascading the two binary counters.

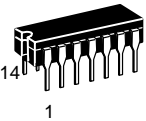
Internal flip-flops are triggered by high-to-low transitions of the clock input. Reset for the counters is asynchronous and active-high. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used as clocks or as strobes except when gated with the Clock of the HC393.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 236 FETs or 59 Equivalent Gates

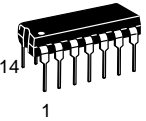
LOGIC DIAGRAM



# MC54/74HC393



**J SUFFIX**  
CERAMIC PACKAGE  
CASE 632-08



**N SUFFIX**  
PLASTIC PACKAGE  
CASE 646-06



**D SUFFIX**  
SOIC PACKAGE  
CASE 751A-03

### ORDERING INFORMATION

MC54HCXXXJ	Ceramic
MC74HCXXXN	Plastic
MC74HCXXXD	SOIC

### PIN ASSIGNMENT

CLOCK a	1	14	V <sub>CC</sub>
RESET a	2	13	CLOCK b
Q1 <sub>a</sub>	3	12	RESET b
Q2 <sub>a</sub>	4	11	Q1 <sub>b</sub>
Q3 <sub>a</sub>	5	10	Q2 <sub>b</sub>
Q4 <sub>a</sub>	6	9	Q3 <sub>b</sub>
GND	7	8	Q4 <sub>b</sub>

### FUNCTION TABLE

Inputs		Outputs
Clock	Reset	
X	H	L
H	L	No Change
L	L	No Change
	L	No Change
	L	Advance to Next State



## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
$V_{in}$	DC Input Voltage (Referenced to GND)	– 1.5 to $V_{CC} + 1.5$	V
$V_{out}$	DC Output Voltage (Referenced to GND)	– 0.5 to $V_{CC} + 0.5$	V
$I_{in}$	DC Input Current, per Pin	$\pm 20$	mA
$I_{out}$	DC Output Current, per Pin	$\pm 25$	mA
$I_{CC}$	DC Supply Current, $V_{CC}$ and GND Pins	$\pm 50$	mA
$P_D$	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
$T_{stg}$	Storage Temperature	– 65 to + 150	°C
$T_L$	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic or SOIC DIP) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

\* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

† Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C  
Ceramic DIP: – 10 mW/°C from 100° to 125°C  
SOIC Package: – 7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	− 55	+ 125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time	V <sub>CC</sub> = 2.0 V	0	1000	ns
	(Figure 1)	V <sub>CC</sub> = 4.5 V	0	500	
		V <sub>CC</sub> = 6.0 V	0	400	

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	$V_{CC}$ V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
$V_{IH}$	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
$V_{IL}$	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
$V_{OH}$	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \leq 4.0 \text{ mA}$ $ I_{out}  \leq 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
$V_{OL}$	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \leq 4.0 \text{ mA}$ $ I_{out}  \leq 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
$I_{in}$	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or } GND$	6.0	$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
$I_{CC}$	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or } GND$ $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	$\mu\text{A}$

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

**AC ELECTRICAL CHARACTERISTICS** ( $C_L = 50$  pF, Input  $t_r = t_f = 6$  ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
$f_{max}$	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 3)	2.0 4.5 6.0	5.4 27 32	4.4 22 26	3.6 18 21	MHz
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Clock to Q1 (Figures 1 and 3)	2.0 4.5 6.0	120 24 20	150 30 26	180 36 31	ns
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Clock to Q2 (Figures 1 and 3)	2.0 4.5 6.0	190 38 32	240 48 41	285 57 48	ns
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Clock to Q3 (Figures 1 and 3)	2.0 4.5 6.0	240 48 41	300 60 51	360 72 61	ns
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Clock to Q4 (Figures 1 and 3)	2.0 4.5 6.0	290 58 49	365 73 62	435 87 74	ns
$t_{PHL}$	Maximum Propagation Delay, Reset to any Q (Figures 2 and 3)	2.0 4.5 6.0	165 33 28	205 41 35	250 50 43	ns
$t_{TLH}$ , $t_{THL}$	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
$C_{in}$	Maximum Input Capacitance	—	10	10	10	pF

## NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).
2. Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

C <sub>PD</sub>	Power Dissipation Capacitance (Per Counter)*	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		40	

\* Used to determine the no-load dynamic power consumption:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ . For load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

**TIMING REQUIREMENTS** (Input  $t_r = t_f = 6$  ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
$t_{rec}$	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0 4.5 6.0	50 10 9	65 13 11	75 15 13	ns
$t_w$	Minimum Pulse Width, Clock (Figure 1)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
$t_w$	Minimum Pulse Width, Reset (Figure 2)	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
$t_r$ , $t_f$	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

## PIN DESCRIPTIONS

## INPUTS

**Clock (Pins 1, 13)**

Clock input. The internal flip-flops are toggled and the counter state advances on high-to-low transitions of the clock input.

**CONTROL INPUTS****Reset (Pins 2, 12)**

Active-high, asynchronous reset. A separate reset is pro-

vided for each counter. A high at the Reset input prevents counting and forces all four outputs low.

**OUTPUTS****Q1, Q2, Q3, Q4 (Pins 3, 4, 5, 6, 8, 9, 10, 11)**

Parallel binary outputs Q4 is the most significant bit.

## SWITCHING WAVEFORMS

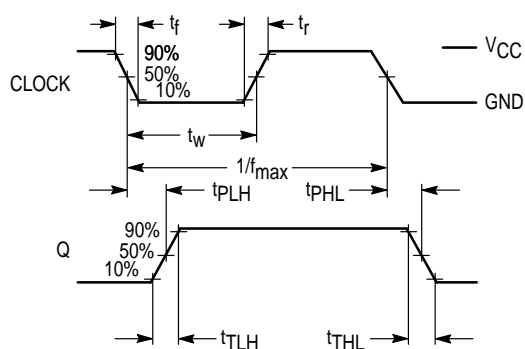


Figure 1.

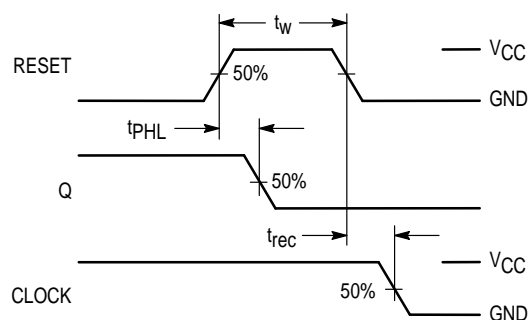
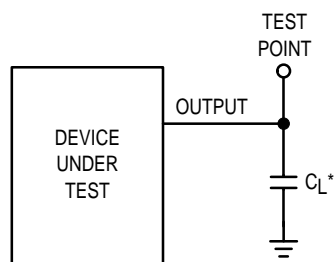


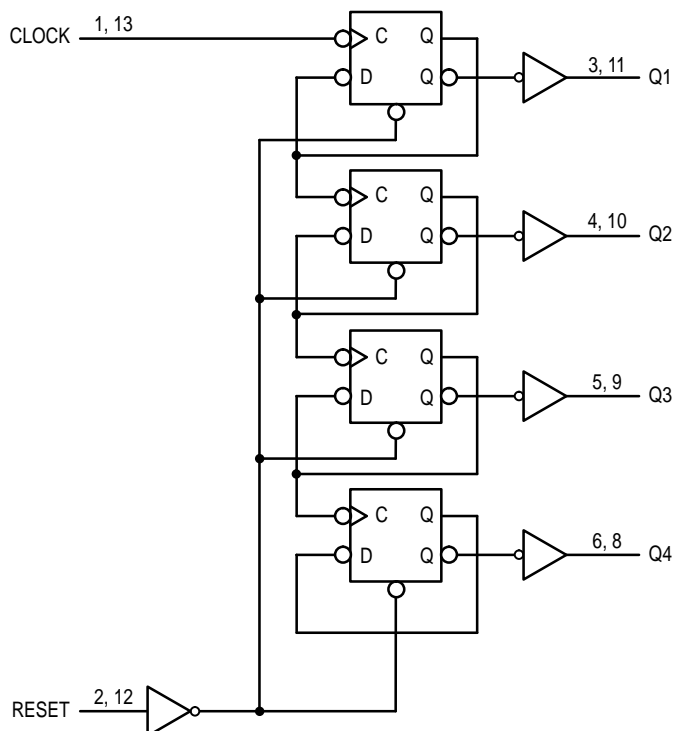
Figure 2.

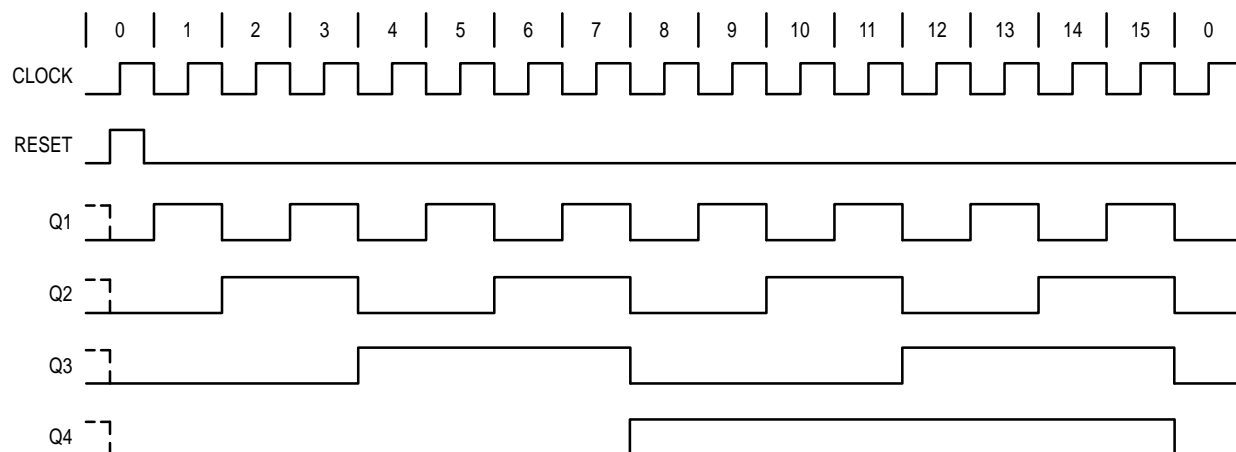


\* Includes all probe and jig capacitance

Figure 3. Test Circuit

## EXPANDED LOGIC DIAGRAM

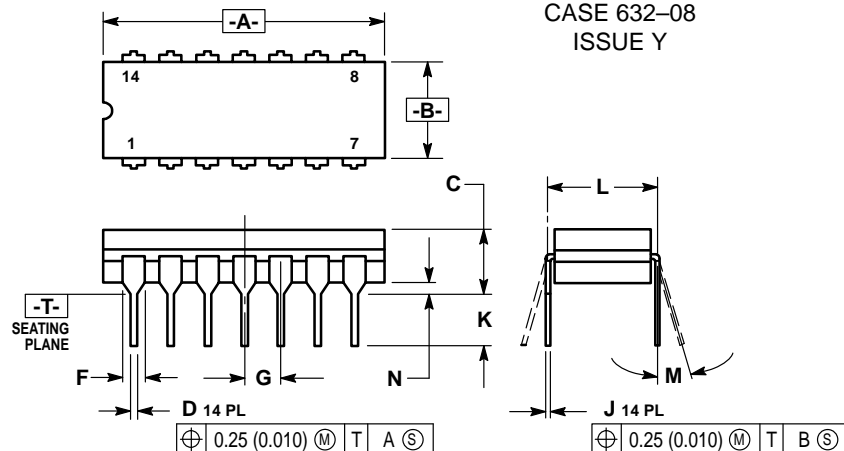


**TIMING DIAGRAM****COUNT SEQUENCE**

Count	Outputs			
	Q4	Q3	Q2	Q1
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

## OUTLINE DIMENSIONS

**J SUFFIX**  
CERAMIC DIP PACKAGE  
CASE 632-08  
ISSUE Y

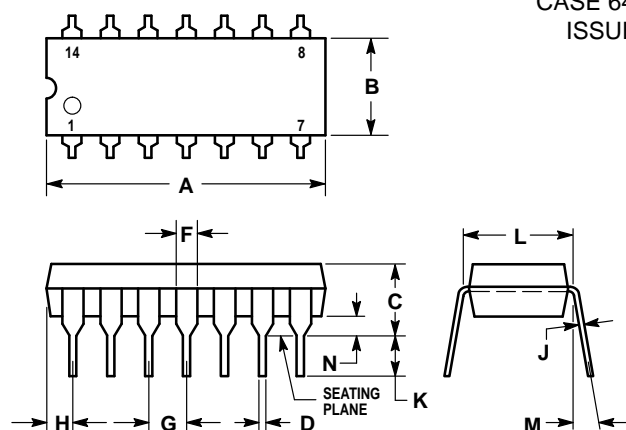


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.94
B	0.245	0.280	6.23	7.11
C	0.155	0.200	3.94	5.08
D	0.015	0.020	0.39	0.50
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

**N SUFFIX**  
PLASTIC DIP PACKAGE  
CASE 646-06  
ISSUE L

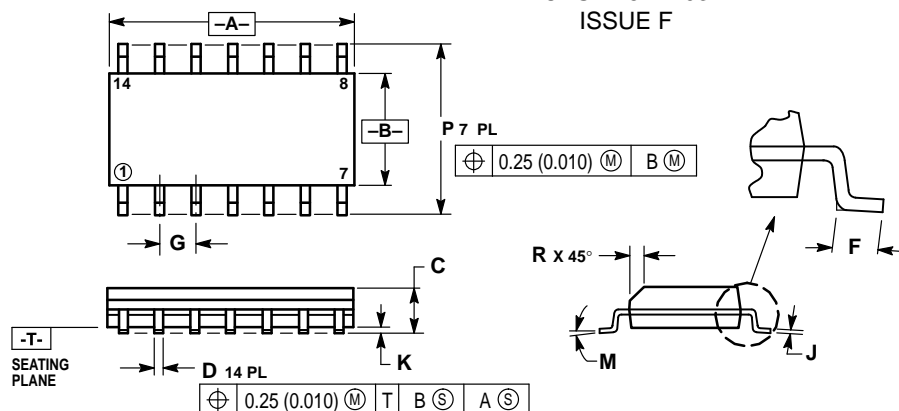


NOTES:

1. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	10°	0°	10°
N	0.015	0.039	0.39	1.01


**D SUFFIX**  
PLASTIC SOIC PACKAGE  
CASE 751A-03  
ISSUE F



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters can and do vary in different applications. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part. Motorola and  are registered trademarks of Motorola, Inc. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

**How to reach us:**

**USA/EUROPE:** Motorola Literature Distribution;  
P.O. Box 20912; Phoenix, Arizona 85036. 1-800-441-2447

**MFAX:** RMFAX0@email.sps.mot.com -TOUCHTONE (602) 244-6609  
**INTERNET:** <http://Design-NET.com>

**JAPAN:** Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, Toshikatsu Otsuki,  
6F Seibu-Butsuryu-Center, 3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 03-3521-8315

**HONG KONG:** Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,  
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298



This datasheet has been download from:

[www.datasheetcatalog.com](http://www.datasheetcatalog.com)

Datasheets for electronics components.