

## 8-Bit Static Shift Register

The MC14014B and MC14021B 8-bit static shift registers are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These shift registers find primary use in parallel-to-serial data conversion, synchronous and asynchronous parallel input, serial output data queueing; and other general purpose register applications requiring low power and/or high noise immunity.

- Synchronous Parallel Input/Serial Output (MC14014B)
- Asynchronous Parallel Input/Serial Output (MC14021B)
- Synchronous Serial Input/Serial Output
- Full Static Operation
- “Q” Outputs from Sixth, Seventh, and Eighth Stages
- Double Diode Input Protection
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- MC14014B Pin-for-Pin Replacement for CD4014B
- MC14021B Pin-for-Pin Replacement for CD4021B

**MAXIMUM RATINGS\*** (Voltages Referenced to  $V_{SS}$ )

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	− 0.5 to + 18.0	V
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage (DC or Transient)	− 0.5 to V <sub>DD</sub> + 0.5	V
I <sub>in</sub> , I <sub>out</sub>	Input or Output Current (DC or Transient), per Pin	± 10	mA
P <sub>D</sub>	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	− 65 to + 150	°C
T <sub>L</sub>	Lead Temperature (8–Second Soldering)	260	°C

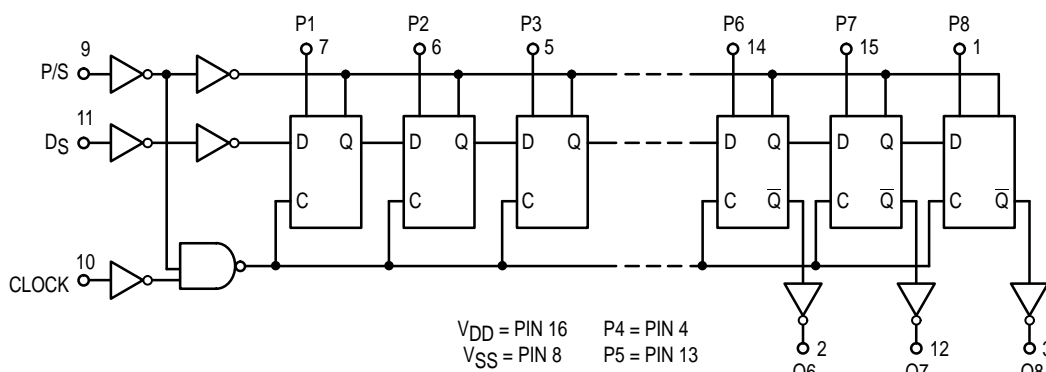
\* Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating:

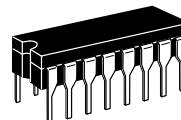
Plastic "P and D/DW" Packages:  $-7.0 \text{ mW}/^{\circ}\text{C}$  From  $65^{\circ}\text{C}$  To  $125^{\circ}\text{C}$

Ceramic "L" Packages: – 12 mW/°C From 100°C To 125°C

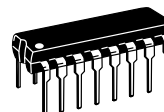
### LOGIC DIAGRAM



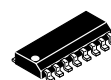
**MC14014B**  
**MC14021B**



**L SUFFIX**  
CERAMIC  
CASE 620



**P SUFFIX**  
PLASTIC  
CASE 648



**D SUFFIX**  
SOIC  
CASE 751B






## ORDERING INFORMATION

MC14XXXBCP	Plastic
MC14XXXBCL	Ceramic
MC14XXXBD	SOIC



$T_A = -55^{\circ}$  to  $125^{\circ}\text{C}$  for all packages.

### TRUTH TABLE

**SERIAL OPERATION:**

t	Clock	D <sub>S</sub>	P/S	Q6 t=n+6	Q7 t=n+7	Q8 t=n+8
n		0	0	0	?	?
n+1		1	0	1	0	?
n+2		0	0	0	1	0
n+3		1	0	1	0	1
		X	0	Q6	Q7	Q8

**PARALLEL OPERATION:**

Clock		D <sub>S</sub>	P/S	P <sub>n</sub>	*Q <sub>n</sub>
MC14014B	MC14021B				
	X	X	1	0	0
	X	X	1	1	1

\* Q6, Q7, & Q8 are available externally

X = Don't Care



# **ELECTRICAL CHARACTERISTICS** (Voltages Referenced to $V_{SS}$ )

Characteristic	Symbol	$V_{DD}$ Vdc	– 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage “0” Level $V_{in} = V_{DD}$ or 0	$V_{OL}$	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	$V_{OH}$	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage “0” Level ( $V_O = 4.5$ or $0.5$ Vdc) ( $V_O = 9.0$ or $1.0$ Vdc) ( $V_O = 13.5$ or $1.5$ Vdc)	$V_{IL}$	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	$V_{IH}$	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current ( $V_{OH} = 2.5$ Vdc) ( $V_{OH} = 4.6$ Vdc) ( $V_{OH} = 9.5$ Vdc) ( $V_{OH} = 13.5$ Vdc)  ( $V_{OL} = 0.4$ Vdc) ( $V_{OL} = 0.5$ Vdc) ( $V_{OL} = 1.5$ Vdc)	Source $I_{OH}$	5.0	– 3.0	—	– 2.4	– 4.2	—	– 1.7	—	mAdc
		5.0	– 0.64	—	– 0.51	– 0.88	—	– 0.36	—	
		10	– 1.6	—	– 1.3	– 2.25	—	– 0.9	—	
		15	– 4.2	—	– 3.4	– 8.8	—	– 2.4	—	
	Sink $I_{OL}$	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	$I_{in}$	15	—	$\pm 0.1$	—	$\pm 0.00001$	$\pm 0.1$	—	$\pm 1.0$	$\mu$ Adc
Input Capacitance ( $V_{in} = 0$ )	$C_{in}$	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package) $I_{DD}$		5.0	—	5.0	—	0.005	5.0	—	150	$\mu$ Adc
		10	—	10	—	0.010	10	—	300	
		15	—	15	—	0.015	15	—	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) ( $C_L = 50$ pF on all outputs, all buffers switching)	$I_T$	5.0 10 15	$I_T = (0.75 \mu A/kHz) f + I_{DD}$ $I_T = (1.50 \mu A/kHz) f + I_{DD}$ $I_T = (2.25 \mu A/kHz) f + I_{DD}$							$\mu$ Adc

#Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

\*\*The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where:  $I_T$  is in  $\mu A$  (per package),  $C_L$  in pF,  $V = (V_{DD} - V_{SS})$  in volts,  $f$  in kHz is input frequency, and  $k = 0.0015$ .

**This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .**

**Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.**

## **PIN ASSIGNMENT**

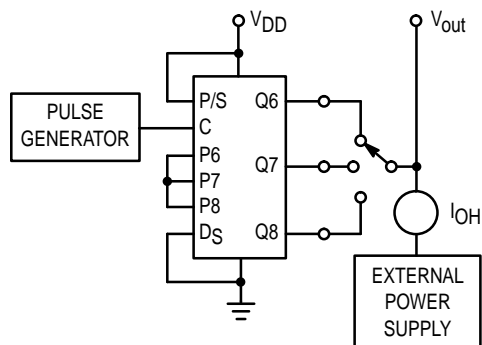
P8	1	16	$V_{DD}$
Q6	2	15	P7
Q8	3	14	P6
P4	4	13	P5
P3	5	12	Q7
P2	6	11	$D_S$
P1	7	10	C
$V_{SS}$	8	9	P/S

**SWITCHING CHARACTERISTICS** ( $C_L = 50 \text{ pF}$ ,  $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$ Vdc	Min	Typ #	Max	Unit
Output Rise and Fall Time $t_{TLH}$ , $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}$ , $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}$ , $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	$t_{TLH}$ , $t_{THL}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time (Clock to Q, P/S to Q) $t_{PHL}$ , $t_{PLH} = (1.7 \text{ ns/pF}) C_L + 315 \text{ ns}$ $t_{PHL}$ , $t_{PLH} = (0.66 \text{ ns/pF}) C_L + 137 \text{ ns}$ $t_{PHL}$ , $t_{PLH} = (0.5 \text{ ns/pF}) C_L + 90 \text{ ns}$	$t_{PLH}$ , $t_{PHL}$	5.0 10 15	— — —	400 170 115	800 340 230	ns
Clock Pulse Width	$t_{WH}$	5.0 10 15	400 175 135	150 75 40	— — —	ns
Clock Frequency	$f_{cl}$	5.0 10 15	— — —	3.0 6.0 8.0	1.5 3.0 4.0	MHz
Parallel/Serial Control Pulse Width	$t_{WH}$	5.0 10 15	400 175 135	150 75 40	— — —	ns
Setup Time P/S to Clock	$t_{su}$	5.0 10 15	200 100 80	100 50 40	— — —	ns
Hold Time Clock to P/S	$t_h$	5.0 10 15	20 20 25	– 2.5 – 10 0	— — —	ns
Setup Time Data (Parallel or Serial) to Clock or P/S	$t_{su}$	5.0 10 15	350 80 60	150 50 30	— — —	ns
Hold Time Clock to $D_S$	$t_h$	5.0 10 15	45 35 35	0 0 5	— — —	ns
Hold Time Clock to $P_n$	$t_h$	5.0 10 15	50 45 45	25 20 20	— — —	ns
Input Clock Rise Time	$t_{r(cl)}$	5.0 10 15	— — —	— — —	15 5 4	$\mu\text{s}$

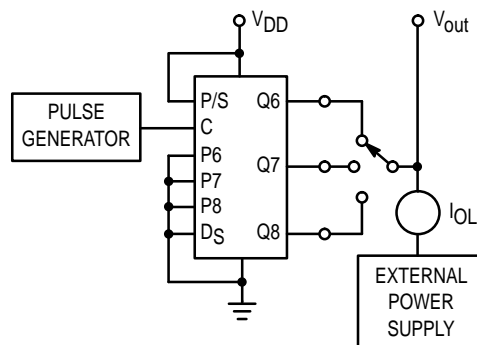
\* The formulas given are for the typical characteristics only at  $25^\circ\text{C}$ .

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.



Preset output under test to a logic "1" level.

**Figure 1. Output Source Current Test Circuit**



**Figure 2. Output Sink Current Test Circuit**

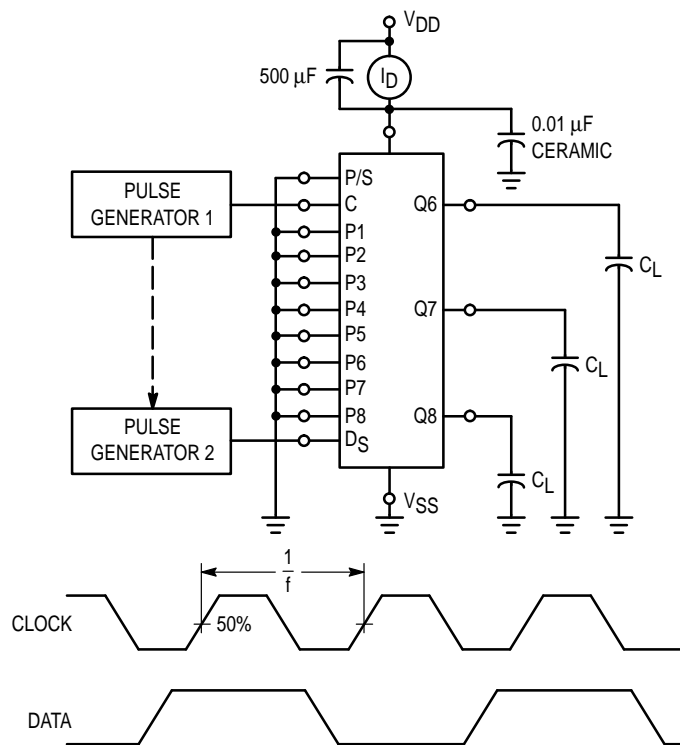


Figure 3. Power Dissipation Test Circuit and Waveform

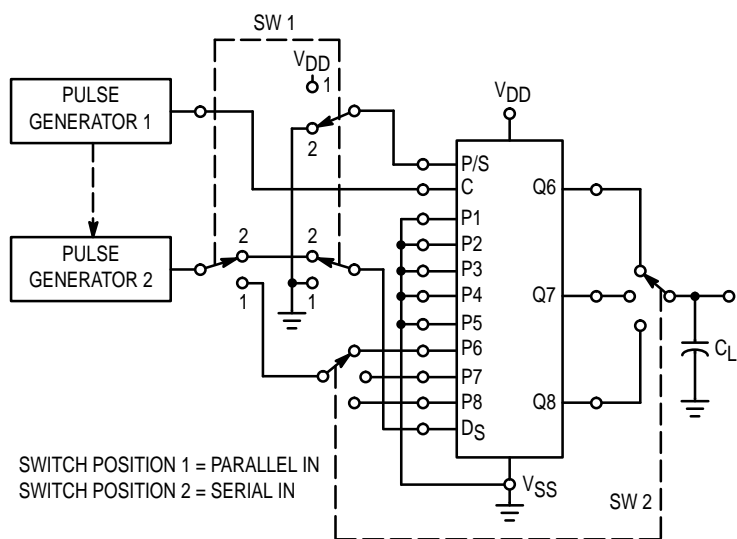
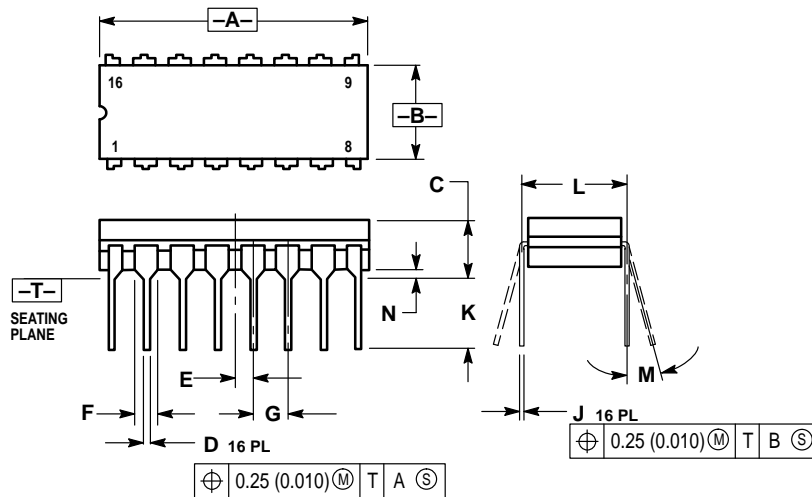


Figure 4. Switching Time Test Circuit and Waveforms

## OUTLINE DIMENSIONS

### L SUFFIX CERAMIC DIP PACKAGE CASE 620-10 ISSUE V

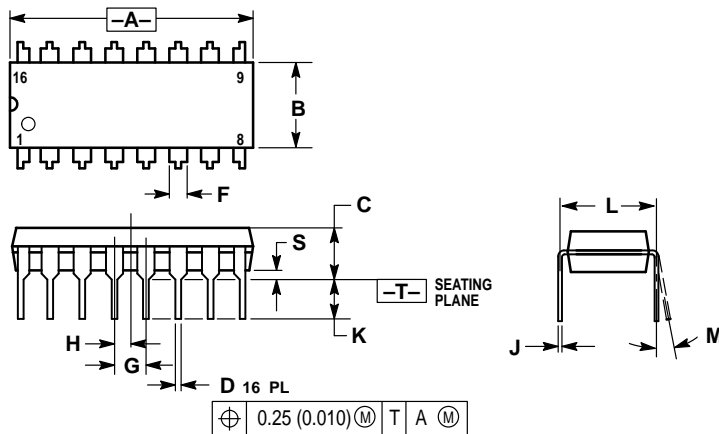


#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050	BSC	1.27	BSC
F	0.055	0.065	1.40	1.65
G	0.100	BSC	2.54	BSC
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300	BSC	7.62	BSC
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

### P SUFFIX PLASTIC DIP PACKAGE CASE 648-08 ISSUE R



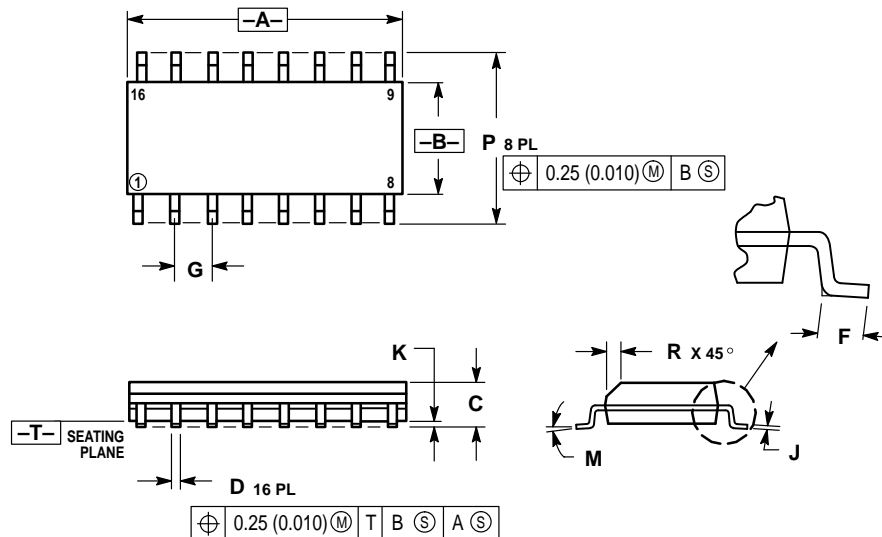
#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100	BSC	2.54	BSC
H	0.050	BSC	1.27	BSC
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

## OUTLINE DIMENSIONS

### D SUFFIX PLASTIC SOIC PACKAGE CASE 751B-05 ISSUE J



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Motorola data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part. Motorola and  are registered trademarks of Motorola, Inc. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

#### How to reach us:

**USA/EUROPE/Locations Not Listed:** Motorola Literature Distribution;  
P.O. Box 20912; Phoenix, Arizona 85036. 1-800-441-2447 or 602-303-5454

**MFAX:** RMFAX0@email.sps.mot.com – TOUCHTONE 602-244-6609  
**INTERNET:** <http://Design-NET.com>

**JAPAN:** Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, 6F Seibu-Butsuryu-Center,  
3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 03-81-3521-8315

**ASIA/PACIFIC:** Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,  
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298



MC14014B/D



