

## DM74LS90/DM74LS93 Decade and Binary Counters

### General Description

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the 'LS90 and divide-by-eight for the 'LS93.

All of these counters have a gated zero reset and the LS90 also has gated set-to-nine inputs for use in BCD nine's complement applications.

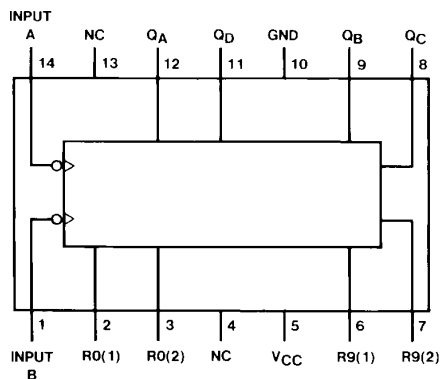
To use their maximum count length (decade or four bit binary), the B input is connected to the  $Q_A$  output. The input

count pulses are applied to input A and the outputs are as described in the appropriate truth table. A symmetrical divide-by-ten count can be obtained from the 'LS90 counters by connecting the  $Q_D$  output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output  $Q_A$ .

### Features

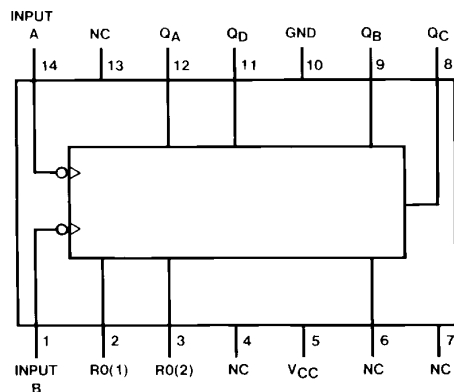
- Typical power dissipation 45 mW
- Count frequency 42 MHz

### Connection Diagrams (Dual-In-Line Packages)



TL/F/6381-1

Order Number DM74LS90M or DM74LS90N  
See NS Package Number M14A or N14A



TL/F/6381-2

Order Number DM74LS93M or DM74LS93N  
See NS Package Number M14A or N14A

## Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage (Reset)	7V
Input Voltage (A or B)	5.5V
Operating Free Air Temperature Range	
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: The “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the “Electrical Characteristics” table are not guaranteed at the absolute maximum ratings. The “Recommended Operating Conditions” table will define the conditions for actual device operation.

## Recommended Operating Conditions

Symbol	Parameter		DM74LS90			Units
			Min	Nom	Max	
V <sub>CC</sub>	Supply Voltage		4.75	5	5.25	V
V <sub>IH</sub>	High Level Input Voltage		2			V
V <sub>IL</sub>	Low Level Input Voltage				0.8	V
I <sub>OH</sub>	High Level Output Current				−0.4	mA
I <sub>OL</sub>	Low Level Output Current				8	mA
f <sub>CLK</sub>	Clock Frequency (Note 1)	A to Q <sub>A</sub>	0		32	MHz
		B to Q <sub>B</sub>	0		16	
f <sub>CLK</sub>	Clock Frequency (Note 2)	A to Q <sub>A</sub>	0		20	MHz
		B to Q <sub>B</sub>	0		10	
t <sub>W</sub>	Pulse Width (Note 1)	A	15			ns
		B	30			
		Reset	15			
t <sub>W</sub>	Pulse Width (Note 2)	A	25			ns
		B	50			
		Reset	25			
t <sub>REL</sub>	Reset Release Time (Note 1)		25			ns
t <sub>REL</sub>	Reset Release Time (Note 2)		35			ns
T <sub>A</sub>	Free Air Operating Temperature		0		70	°C

Note 1: C<sub>L</sub> = 15 pF, R<sub>L</sub> = 2 kΩ, T<sub>A</sub> = 25°C and V<sub>CC</sub> = 5V.

Note 2: C<sub>L</sub> = 50 pF, R<sub>L</sub> = 2 kΩ, T<sub>A</sub> = 25°C and V<sub>CC</sub> = 5V.

## 'LS90 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = Min, I <sub>I</sub> = −18 mA				−1.5	V
V <sub>OH</sub>	High Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = Max V <sub>IL</sub> = Max, V <sub>IH</sub> = Min		2.7	3.4		V
V <sub>OL</sub>	Low Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OL</sub> = Max V <sub>IL</sub> = Max, V <sub>IH</sub> = Min (Note 4)			0.35	0.5	V
		I <sub>OL</sub> = 4 mA, V <sub>CC</sub> = Min			0.25	0.4	
I <sub>I</sub>	Input Current @ Max Input Voltage	V <sub>CC</sub> = Max, V <sub>I</sub> = 7V	Reset			0.1	mA
		V <sub>CC</sub> = Max	A			0.2	
		V <sub>I</sub> = 5.5V	B			0.4	

## 'LS90 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted) (Continued)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
$I_{IH}$	High Level Input Current	$V_{CC} = \text{Max}, V_I = 2.7\text{V}$	Reset		20	$\mu\text{A}$
			A		40	
			B		80	
$I_{IL}$	Low Level Input Current	$V_{CC} = \text{Max}, V_I = 0.4\text{V}$	Reset		-0.4	mA
			A		-2.4	
			B		-3.2	
$I_{OS}$	Short Circuit Output Current	$V_{CC} = \text{Max}$ (Note 2)	-20		-100	mA
$I_{CC}$	Supply Current	$V_{CC} = \text{Max}$ (Note 3)		9	15	mA

**Note 1:** All typicals are at  $V_{CC} = 5\text{V}$ ,  $T_A = 25^\circ\text{C}$ .

**Note 2:** Not more than one output should be shorted at a time, and the duration should not exceed one second.

**Note 3:**  $I_{CC}$  is measured with all outputs open, both RO inputs grounded following momentary connection to 4.5V and all other inputs grounded.

**Note 4:**  $Q_A$  outputs are tested at  $I_{OL} = \text{Max}$  plus the limit value of  $I_{IL}$  for the B input. This permits driving the B input while maintaining full fan-out capability.

## 'LS90 Switching Characteristics

at  $V_{CC} = 5\text{V}$  and  $T_A = 25^\circ\text{C}$  (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R <sub>L</sub> = 2 kΩ				Units
			C <sub>L</sub> = 15 pF		C <sub>L</sub> = 50 pF		
			Min	Max	Min	Max	
f <sub>MAX</sub>	Maximum Clock Frequency	A to Q <sub>A</sub>	32		20		MHz
		B to Q <sub>B</sub>	16		10		
t <sub>PLH</sub>	Propagation Delay Time Low to High Level Output	A to Q <sub>A</sub>		16		20	ns
t <sub>PHL</sub>	Propagation Delay Time High to Low Level Output	A to Q <sub>A</sub>		18		24	ns
t <sub>PLH</sub>	Propagation Delay Time Low to High Level Output	A to Q <sub>D</sub>		48		52	ns
t <sub>PHL</sub>	Propagation Delay Time High to Low Level Output	A to Q <sub>D</sub>		50		60	ns
t <sub>PLH</sub>	Propagation Delay Time Low to High Level Output	B to Q <sub>B</sub>		16		23	ns
t <sub>PHL</sub>	Propagation Delay Time High to Low Level Output	B to Q <sub>B</sub>		21		30	ns
t <sub>PLH</sub>	Propagation Delay Time Low to High Level Output	B to Q <sub>C</sub>		32		37	ns
t <sub>PHL</sub>	Propagation Delay Time High to Low Level Output	B to Q <sub>C</sub>		35		44	ns
t <sub>PLH</sub>	Propagation Delay Time Low to High Level Output	B to Q <sub>D</sub>		32		36	ns
t <sub>PHL</sub>	Propagation Delay Time High to Low Level Output	B to Q <sub>D</sub>		35		44	ns
t <sub>PLH</sub>	Propagation Delay Time Low to High Level Output	SET-9 to Q <sub>A</sub> , Q <sub>D</sub>		30		35	ns
t <sub>PHL</sub>	Propagation Delay Time High to Low Level Output	SET-9 to Q <sub>B</sub> , Q <sub>C</sub>		40		48	ns
t <sub>PHL</sub>	Propagation Delay Time High to Low Level Output	SET-0 to Any Q		40		52	ns

## Recommended Operating Conditions

Symbol	Parameter		DM74LS93			Units
			Min	Nom	Max	
$V_{CC}$	Supply Voltage		4.75	5	5.25	V
$V_{IH}$	High Level Input Voltage		2			V
$V_{IL}$	Low Level Input Voltage				0.8	V
$I_{OH}$	High Level Output Current				−0.4	mA
$I_{OL}$	Low Level Output Current				8	mA
$f_{CLK}$	Clock Frequency (Note 1)	A to $Q_A$	0		32	MHz
		B to $Q_B$	0		16	
$f_{CLK}$	Clock Frequency (Note 2)	A to $Q_A$	0		20	
		B to $Q_B$	0		10	
$t_W$	Pulse Width (Note 1)	A	15			ns
		B	30			
		Reset	15			
$t_W$	Pulse Width (Note 2)	A	25			ns
		B	50			
		Reset	25			
$t_{REL}$	Reset Release Time (Note 1)		25			ns
$t_{REL}$	Reset Release Time (Note 2)		35			ns
$T_A$	Free Air Operating Temperature		0		70	°C

**Note 1:**  $C_L = 15$  pF,  $R_L = 2$  k $\Omega$ ,  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 5\text{V}$ .

**Note 2:**  $C_L = 50$  pF,  $R_L = 2$  k $\Omega$ ,  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 5\text{V}$ .

## 'LS93 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
$V_I$	Input Clamp Voltage	$V_{CC} = \text{Min}$ , $I_I = -18$ mA				−1.5	V
$V_{OH}$	High Level Output Voltage	$V_{CC} = \text{Min}$ , $I_{OH} = \text{Max}$ $V_{IL} = \text{Max}$ , $V_{IH} = \text{Min}$		2.7	3.4		V
$V_{OL}$	Low Level Output Voltage	$V_{CC} = \text{Min}$ , $I_{OL} = \text{Max}$ $V_{IL} = \text{Max}$ , $V_{IH} = \text{Min}$ (Note 4)			0.35	0.5	V
		$I_{OL} = 4$ mA, $V_{CC} = \text{Min}$			0.25	0.4	
$I_I$	Input Current @Max Input Voltage	$V_{CC} = \text{Max}$ , $V_I = 7\text{V}$	Reset			0.1	mA
		$V_{CC} = \text{Max}$ $V_I = 5.5\text{V}$	A			0.2	
			B			0.4	
$I_{IH}$	High Level Input Current	$V_{CC} = \text{Max}$ $V_I = 2.7\text{V}$	Reset			20	$\mu\text{A}$
			A			40	
			B			80	

## 'LS93 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted) (Continued)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
$I_{IL}$	Low Level Input Current	$V_{CC} = \text{Max}, V_I = 0.4V$	Reset		−0.4	mA
			A		−2.4	
			B		−1.6	
$I_{OS}$	Short Circuit Output Current	$V_{CC} = \text{Max}$ (Note 2)	−20		−100	mA
$I_{CC}$	Supply Current	$V_{CC} = \text{Max}$ (Note 3)		9	15	mA

**Note 1:** All typicals are at  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ .

**Note 2:** Not more than one output should be shorted at a time, and the duration should not exceed one second.

**Note 3:**  $I_{CC}$  is measured with all outputs open, both RO inputs grounded following momentary connection to 4.5V and all other inputs grounded.

**Note 4:**  $Q_A$  outputs are tested at  $I_{OL} = \text{max}$  plus the limit value of  $I_{IL}$  for the B input. This permits driving the B input while maintaining full fan-out capability.

## 'LS93 Switching Characteristics

at  $V_{CC} = 5V$  and  $T_A = 25^\circ C$  (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R <sub>L</sub> = 2 kΩ				Units
			C <sub>L</sub> = 15 pF		C <sub>L</sub> = 50 pF		
			Min	Max	Min	Max	
f <sub>MAX</sub>	Maximum Clock Frequency	A to Q <sub>A</sub>	32		20		MHz
		B to Q <sub>B</sub>	16		10		
t <sub>PLH</sub>	Propagation Delay Time Low to High Level Output	A to Q <sub>A</sub>		16		20	ns
t <sub>PHL</sub>	Propagation Delay Time High to Low Level Output	A to Q <sub>A</sub>		18		24	ns
t <sub>PLH</sub>	Propagation Delay Time Low to High Level Output	A to Q <sub>D</sub>		70		85	ns
t <sub>PHL</sub>	Propagation Delay Time High to Low Level Output	A to Q <sub>D</sub>		70		90	ns
t <sub>PLH</sub>	Propagation Delay Time Low to High Level Output	B to Q <sub>B</sub>		16		23	ns
t <sub>PHL</sub>	Propagation Delay Time High to Low Level Output	B to Q <sub>B</sub>		21		30	ns
t <sub>PLH</sub>	Propagation Delay Time Low to High Level Output	B to Q <sub>C</sub>		32		37	ns
t <sub>PHL</sub>	Propagation Delay Time High to Low Level Output	B to Q <sub>C</sub>		35		44	ns
t <sub>PLH</sub>	Propagation Delay Time Low to High Level Output	B to Q <sub>D</sub>		51		60	ns
t <sub>PHL</sub>	Propagation Delay Time High to Low Level Output	B to Q <sub>D</sub>		51		70	ns
t <sub>PHL</sub>	Propagation Delay Time High to Low Level Output	SET-0 to Any Q		40		52	ns

## Function Tables

**LS90**  
BCD Count Sequence  
(See Note A)

Count	Output			
	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

**LS90**  
Bi-Quinary (5-2)  
(See Note B)

Count	Output			
	Q <sub>A</sub>	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

**LS93**  
Count Sequence  
(See Note C)

Count	Output			
	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

**LS90**  
Reset/Count Truth Table

Reset Inputs				Output			
R0(1)	R0(2)	R9(1)	R9(2)	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

**LS93**  
Reset/Count Truth Table

Reset Inputs		Output			
R0(1)	R0(2)	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

**Note A:** Output Q<sub>A</sub> is connected to input B for BCD count.

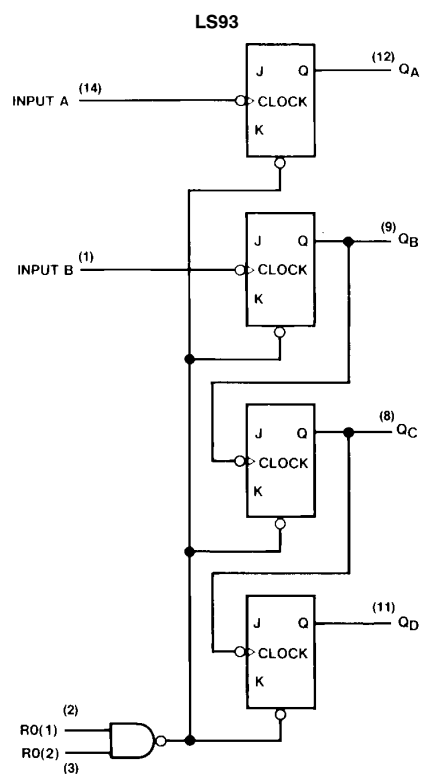
**Note B:** Output Q<sub>D</sub> is connected to input A for bi-quinary count.

**Note C:** Output Q<sub>A</sub> is connected to input B.

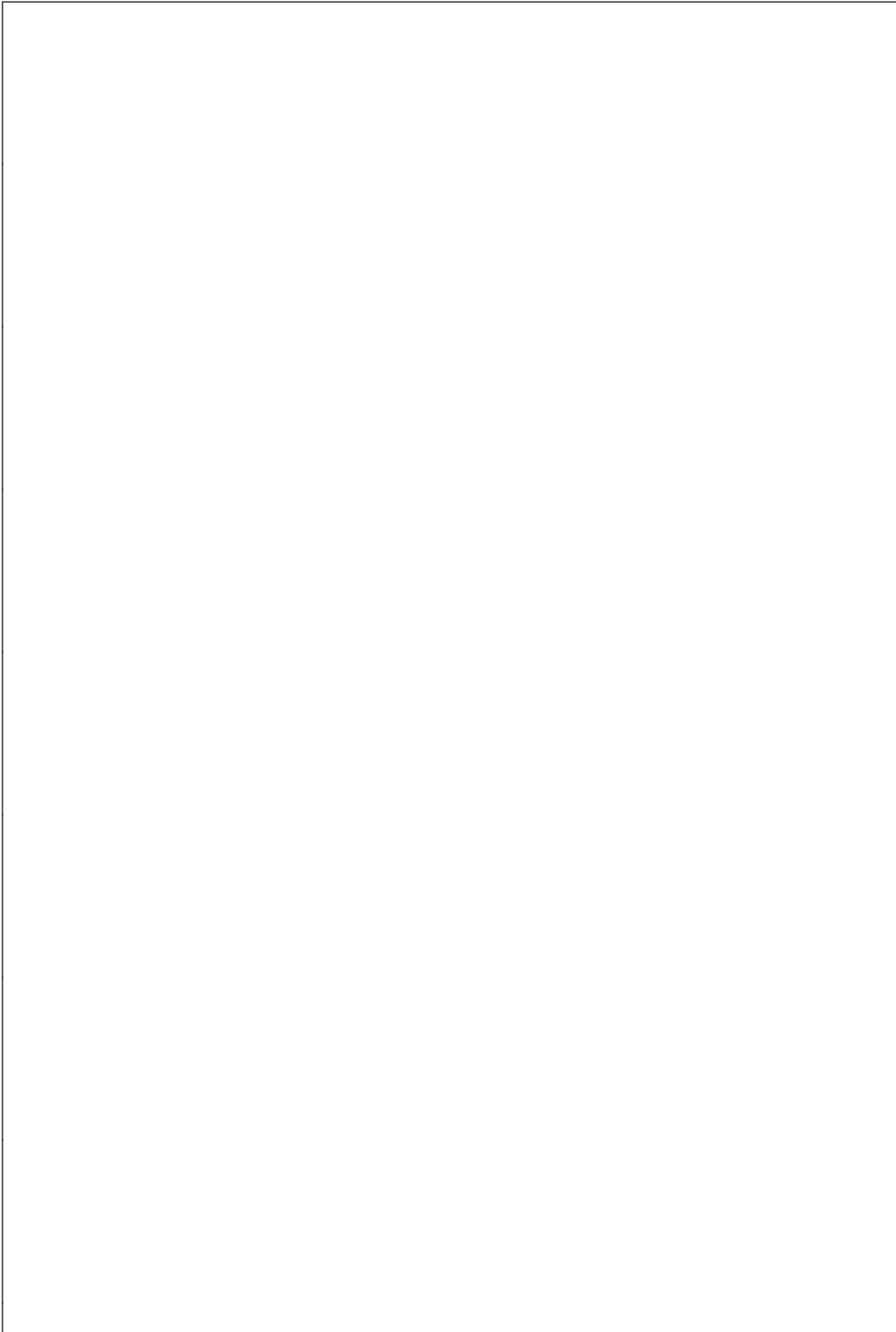
**Note D:** H = High Level, L = Low Level, X = Don't Care.

The diagram shows a 4-bit counter implemented with four LS90 J-K flip-flops. The inputs are R9(1), R9(2), INPUT A, INPUT B, R0(1), and R0(2). The outputs are QA (12), QB (9), QC (8), and QD (11). The flip-flops are connected in a cascaded manner, with the output of one flip-flop serving as the clock for the next. The J and K inputs of each flip-flop are connected to a common bus, which is driven by the inputs R9(1), R9(2), R0(1), and R0(2) through a network of AND gates and inverters. The clock inputs of the flip-flops are connected to a common bus, which is driven by INPUT A and INPUT B through a network of AND gates and inverters. The output of the first flip-flop (QA) is connected to the clock input of the second flip-flop (QB). The output of the second flip-flop (QB) is connected to the clock input of the third flip-flop (QC). The output of the third flip-flop (QC) is connected to the clock input of the fourth flip-flop (QD). The output of the fourth flip-flop (QD) is connected to the clock input of the first flip-flop (QA), forming a closed loop.

The J and K inputs shown without connection are for reference only and are functionally at a high level.

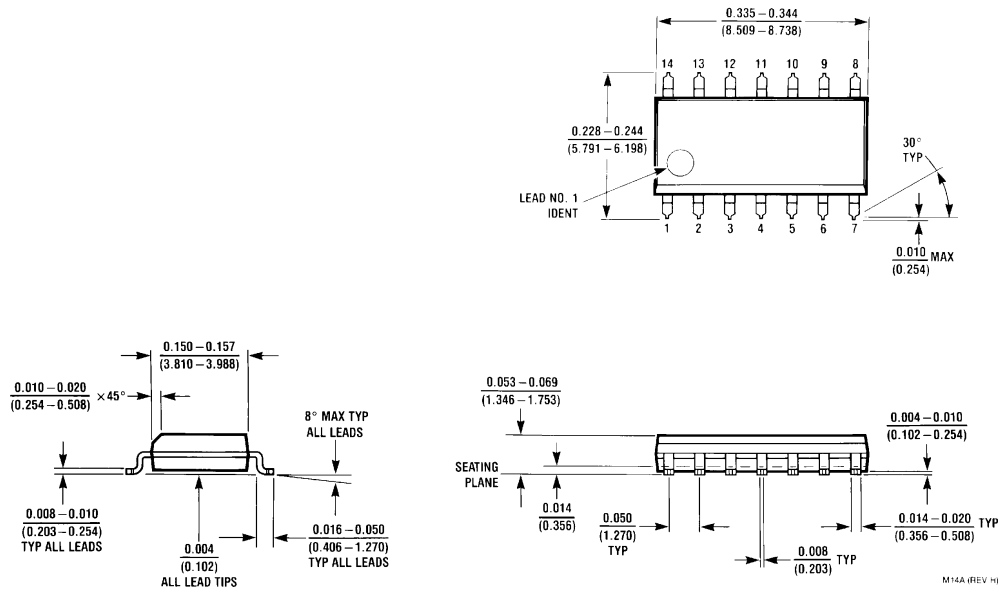


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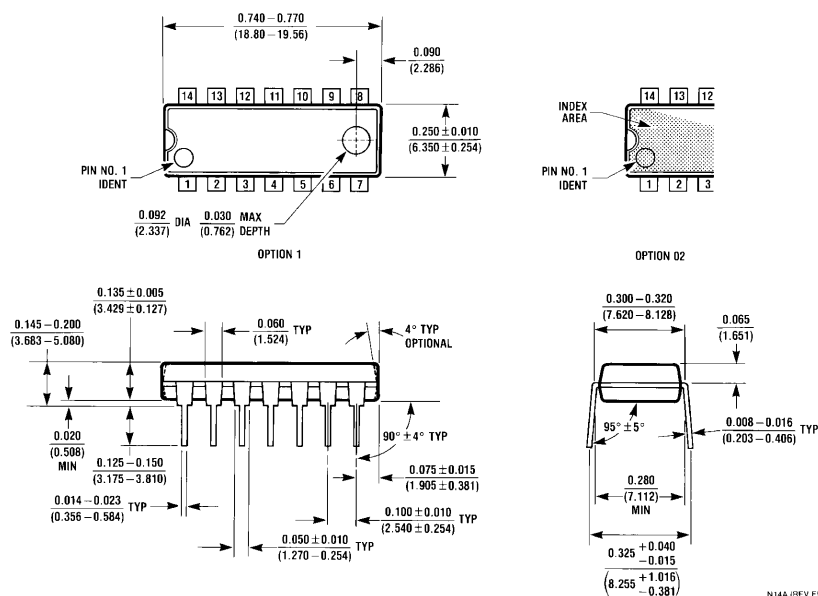


# Physical Dimensions inches (millimeters)



**14-Lead Small Outline Molded Package (M)**  
**Order Number DM74LS90M or DM74LS93M**  
**NS Package Number M14A**


M14A (REV H)



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This file is the datasheet for the following electronic components:

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