MOTOROLA

SN54LS83A
SN74LS83A

4-BIT BINARY FULL ADDER WITH FAST CARRY

LOW POWER SCHOTTKY

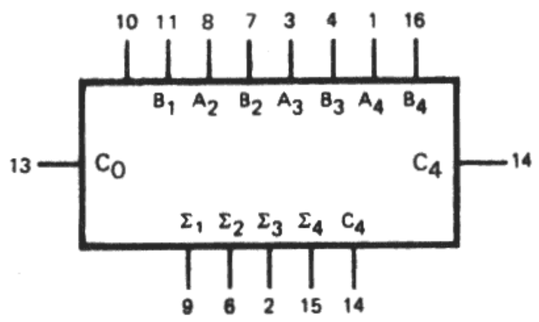
DESCRIPTION — The SN54LS/74LS83A is a high-speed 4-Bit Binary Full Adder with internal carry lookahead. It accepts two 4-bit binary words ($A_1 - A_4$, $B_1 - B_4$) and a Carry Input (C_0). It generates the binary Sum outputs ($\Sigma_1 - \Sigma_4$) and the Carry Output (C_4) from the most significant bit. The LS83A operates with either active HIGH or active LOW operands (positive or negative logic). The SN54LS/74LS283 is recommended for new designs since it is identical in function with this device and features standard corner power pins.

PIN NAMES

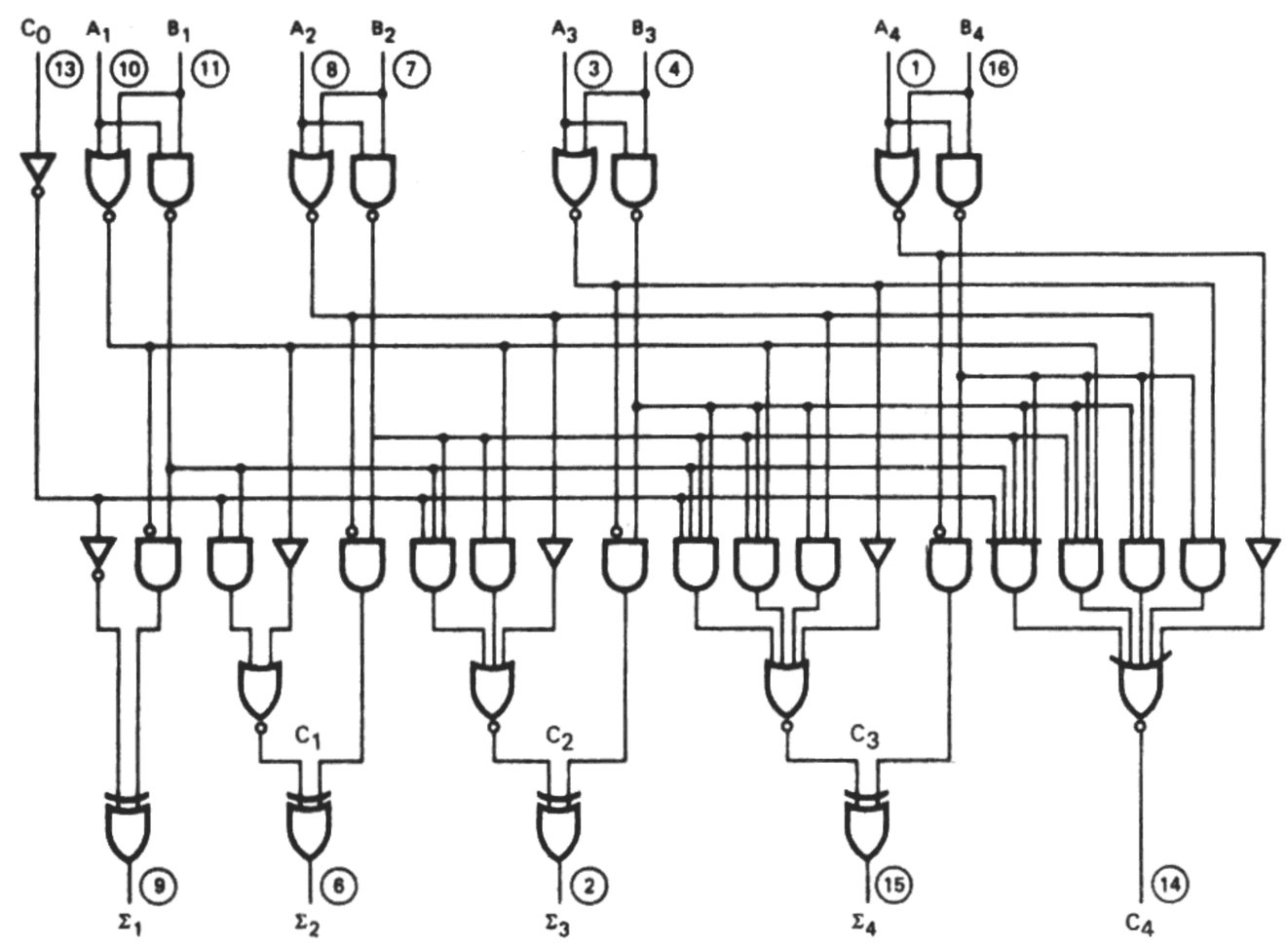
		LOADING (Note a) HIGH	LOW
$A_1 - A_4$	Operand A Inputs	1.0 U.L.	0.5 U.L.
$B_1 - B_4$	Operand B Inputs	1.0 U.L.	0.5 U.L.
C_0	Carry Input	0.5 U.L.	0.25 U.L.
$\Sigma_1 - \Sigma_4$	Sum Outputs (Note b)	10 U.L.	5(2.5) U.L.
C_4	Carry Output (Note b)	10 U.L.	5(2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for commercial (74) Temperature Ranges.

LOGIC SYMBOL



LOGIC DIAGRAM



V_{CC} = Pin 5
GND = Pin 12
○ = Pin Numbers

CONNECTION DIAGRAM DIP (TOP VIEW)

J Suffix — Case 620-08 (Ceramic)
N Suffix — Case 648-05 (Plastic)

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION — The LS83A adds two 4-bit binary words (A plus B) plus the incoming carry. The binary sum appears on the sum outputs (Σ_1 — Σ_4) and outgoing carry (C_4) outputs.

$$C_0 + (A_1+B_1)+2(A_2+B_2)+4(A_3+B_3)+8(A_4+B_4) = \Sigma_1+2\Sigma_2+4\Sigma_3+8\Sigma_4+16C_4$$

Where: (+) = plus

Due to the symmetry of the binary add function the LS83A can be used with either all inputs and outputs active HIGH (positive logic) or with all inputs and outputs active LOW (negative logic). Note that with active HIGH Inputs, Carry Input can not be left open, but must be held LOW when no carry in is intended.

Example:

	C_0	A_1	A_2	A_3	A_4	B_1	B_2	B_3	B_4	Σ_1	Σ_2	Σ_3	Σ_4	C_4	
Logic Levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H	
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1	(10+9 = 19)
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0	(carry+5+6 = 12)

Interchanging inputs of equal weight does not affect the operation, thus C_0, A_1, B_1, can be arbitrarily assigned to pins 10, 11, 13, etc.

FUNCTIONAL TRUTH TABLE

$C_{(n-1)}$	A_n	B_n	Σ_n	C_n
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

C_1 — C_3 are generated internally
C_0 — is an external input
C_4 — is an output generated internally

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current C_0 A or B				20 40	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
	C_0 A or B				0.1 0.2	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current C_0 A or B				−0.4 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current All Inputs Grounded All Inputs at 4.5 V, Except B All Inputs at 4.5 V				39 34 34	mA	V_{CC} = MAX	

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay, C_0 Input to any Σ Output		16 15	24 24	ns	V_{CC} = 5.0 V C_L = 15 pF Figures 1 and 2
t_{PLH} t_{PHL}	Propagation Delay, Any A or B Input to Σ Outputs		15 15	24 24	ns	
t_{PLH} t_{PHL}	Propagation Delay, C_0 Input to C_4 Output		11 15	17 22	ns	
t_{PLH} t_{PHL}	Propagation Delay, Any A or B Input to C_4 Output		11 12	17 17	ns	

AC WAVEFORMS

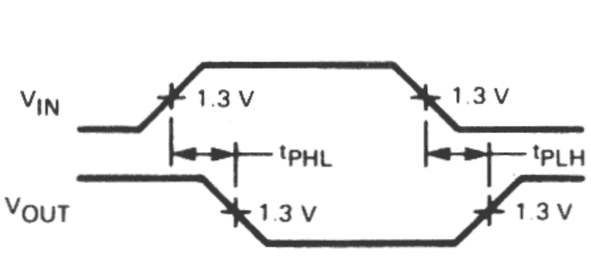


Fig. 1

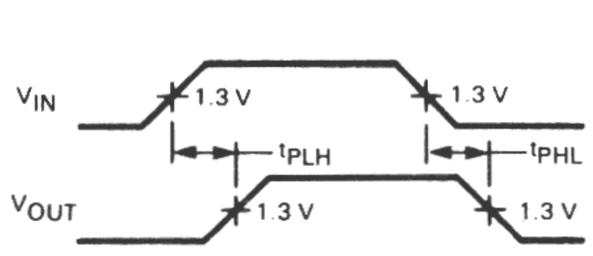


Fig. 2