MC14094B

8-Stage Shift/Store Register with Three-State Outputs

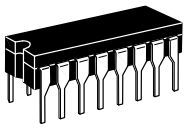
The MC14094B combines an 8–stage shift register with a data latch for each stage and a three–state output from each latch.

Data is shifted on the positive clock transition and is shifted from the seventh stage to two serial outputs. The Q_S output data is for use in high–speed cascaded systems. The Q'_S output data is shifted on the following negative clock transition for use in low–speed cascaded systems.

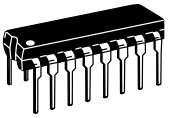
Data from each stage of the shift register is latched on the negative transition of the strobe input. Data propagates through the latch while strobe is high.

Outputs of the eight data latches are controlled by three–state buffers which are placed in the high–impedance state by a logic Low on Output Enable.

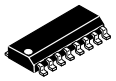
- Three–State Outputs
- Capable of Driving Two Low–Power TTL Loads or One Low–Power Schottky TTL Load Over the Rated Temperature Range
- Input Diode Protection
- Data Latch
- Dual Outputs for Data Out on Both Positive and Negative Clock Transitions
- Useful for Serial–to–Parallel Data Conversion
- Pin–for–Pin Compatible with CD4094B



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



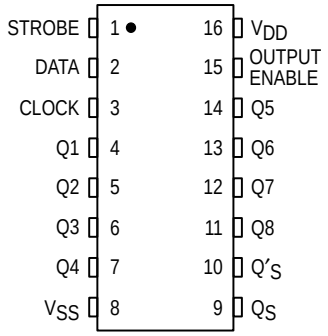
D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

MC14XXXBCP	Plastic
MC14XXXBCL	Ceramic
MC14XXXBD	SOIC

T_A = – 55° to 125°C for all packages.

PIN ASSIGNMENT



MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to + 18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	– 0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating:
Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C
Ceramic “L” Packages: – 12 mW/°C From 100°C To 125°C

Clock	Output Enable	Strobe	Data	Parallel Outputs		Serial Outputs	
				Q1	Q_N	Q_S*	Q'_S
↗	0	X	X	Z	Z	Q7	No Chg.
↘	0	X	X	Z	Z	No Chg.	Q7
↗	1	0	X	No Chg.	No Chg.	Q7	No Chg.
↗	1	1	0	0	Q_N–1	Q7	No Chg.
↗	1	1	1	1	Q_N–1	Q7	No Chg.
↘	1	1	1	No Chg.	No Chg.	No Chg.	Q7

Z = High Impedance X = Don’t Care
* At the positive clock edge, information in the 7th shift register stage is transferred to Q8 and Q_S.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

REV 3
1/94

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	– 55°C Min	– 55°C Max	25°C Min	25°C Typ #	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
V_{in} = V_{DD} or 0		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
"1" Level	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
V_{in} = 0 or V_{DD}		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	—	1.5	—	2.25	1.5	—	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	—	3.0	—	4.50	3.0	—	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	—	4.0	—	6.75	4.0	—	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	—	3.5	2.75	—	3.5	—	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	—	7.0	5.50	—	7.0	—	
(V_O = 1.5 or 13.5 Vdc)		15	11	—	11	8.25	—	11	—	
Output Drive Current	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	– 3.0	—	– 2.4	– 4.2	—	– 1.7	—	
(V_{OH} = 4.6 Vdc)		5.0	– 0.64	—	– 0.51	– 0.88	—	– 0.36	—	
(V_{OH} = 9.5 Vdc)		10	– 1.6	—	– 1.3	– 2.25	—	– 0.9	—	
(V_{OH} = 13.5 Vdc)		15	– 4.2	—	– 3.4	– 8.8	—	– 2.4	—	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	—	1.3	2.25	—	0.9	—	
(V_{OL} = 1.5 Vdc)		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0	—	5.0	—	0.005	5.0	—	150	µAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (4.1 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (14 µA/kHz) f + I_{DD}							
		15	I_T = (140 µA/kHz) f + I_{DD}							
3–State Output Leakage Current	I_{TL}	15	—	± 0.1	—	± 0.0001	± 0.1	—	± 3.0	µA

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

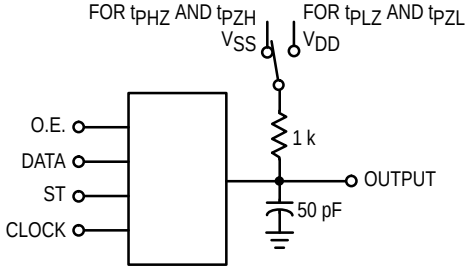
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH},					ns
t_{TLH}, t_{THL} = (1.35 ns/pF) C_L + 33 ns	t_{THL}	5.0	—	100	200	
t_{TLH}, t_{THL} = (0.6 ns/pF) C_L + 20 ns		10	—	50	100	
t_{TLH}, t_{THL} = (0.4 ns/pF) C_L + 20 ns		15	—	40	80	
Propagation Delay Time	t_{PLH},					ns
Clock to Serial out QS	t_{PHL}					
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 305 ns		5.0	—	350	600	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 107 ns		10	—	125	250	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C L + 82 ns		15	—	95	190	
Clock to Serial out Q'S						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 350 ns		5.0	—	230	460	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 149 ns		10	—	110	220	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 62 ns		15	—	75	150	
Clock to Parallel out						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 375 ns		5.0	—	420	840	
t_{PLH}, t_{PHL} = (0.35 ns/pF) C_L + 177 ns		10	—	195	390	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 122 ns		15	—	135	270	
Strobe to Parallel out						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 245 ns		5.0	—	290	580	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C L + 127 ns		10	—	145	290	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 87 ns		15	—	100	200	
Output Enable to Output						
t_{PHZ}, t_{PZL} = (0.90 ns/pF) C_L + 95 ns	t_{PHZ},	5.0	—	140	280	
t_{PHZ}, t_{PZL} = (0.36 ns/PF) C_L + 57 ns	t_{PZL}	10	—	75	150	
t_{PHZ}, t_{PZL} = (0.26 ns/pF) C_L + 42 ns		15	—	55	110	
t_{PLZ}, t_{PZH} = (0.90 ns/pF) C_L + 180 ns	t_{PLZ},	5.0	—	225	450	
t_{PLZ}, t_{PZH} = (0.36 ns/pF) C_L + 77 ns	t_{PZH}	10	—	95	190	
t_{PLZ}, t_{PZH} = (0.26 ns/pF) C_L + 57 ns		15	—	70	140	
Setup Time	t_{su}	5.0	125	60	—	ns
Data in to Clock		10	55	30	—	
		15	35	20	—	
Hold Time	t_h	5.0	0	– 40	—	ns
Clock to Data		10	20	– 10	—	
		15	20	0	—	
Clock Pulse Width, High	t_{WH}	5.0	200	100	—	ns
		10	100	50	—	
		15	83	40	—	
Clock Rise and Fall Time	$t_{r(cl)}$	5	—	—	15	µs
	$t_{f(cl)}$	10	—	—	5.0	
		15	—	—	4.0	
Clock Pulse Frequency	f_{cl}	5.0	—	2.5	1.25	MHz
		10	—	5.0	2.5	
		15	—	6.0	3.0	
Strobe Pulse Width	t_{WL}	5.0	200	100	—	ns
		10	80	40	—	
		15	70	35	—	

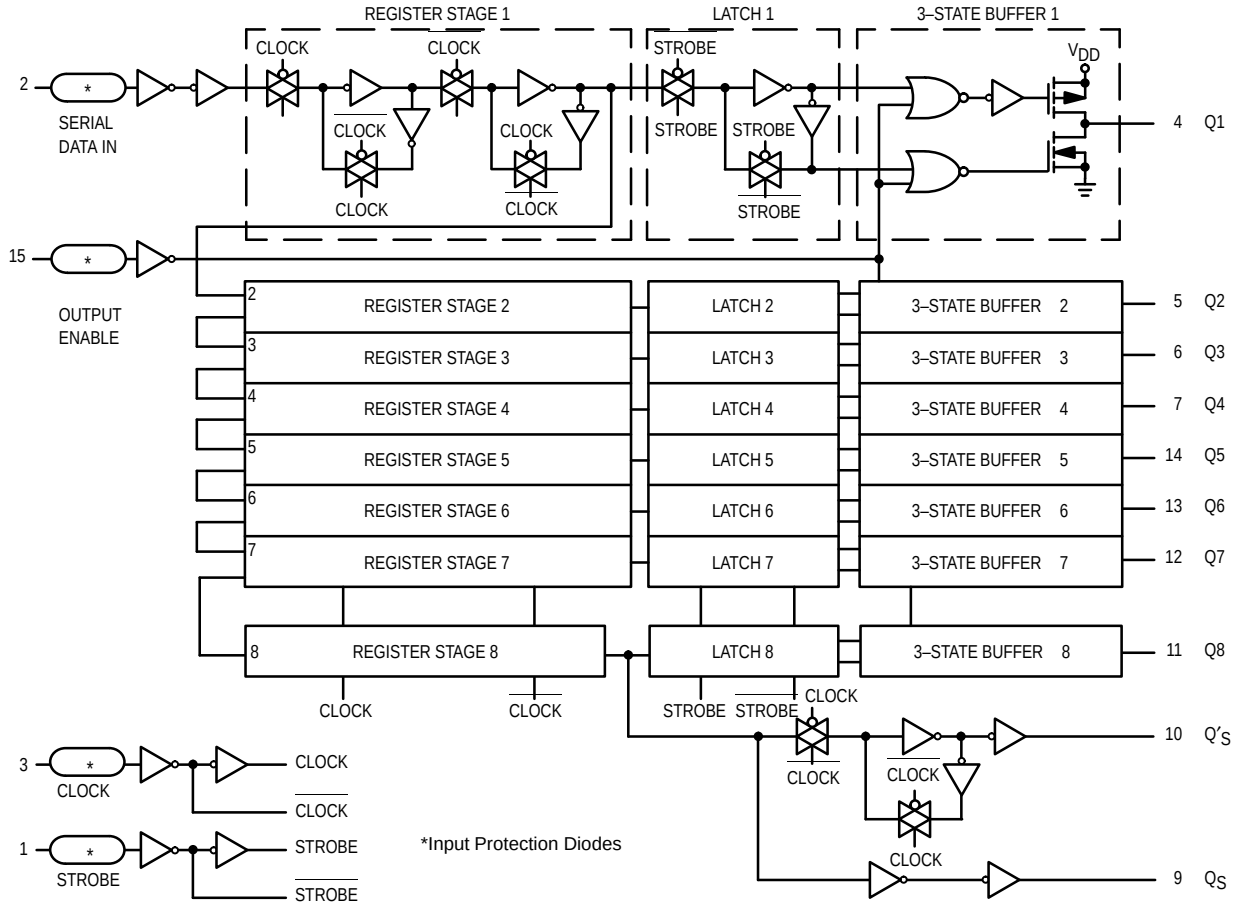
* The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

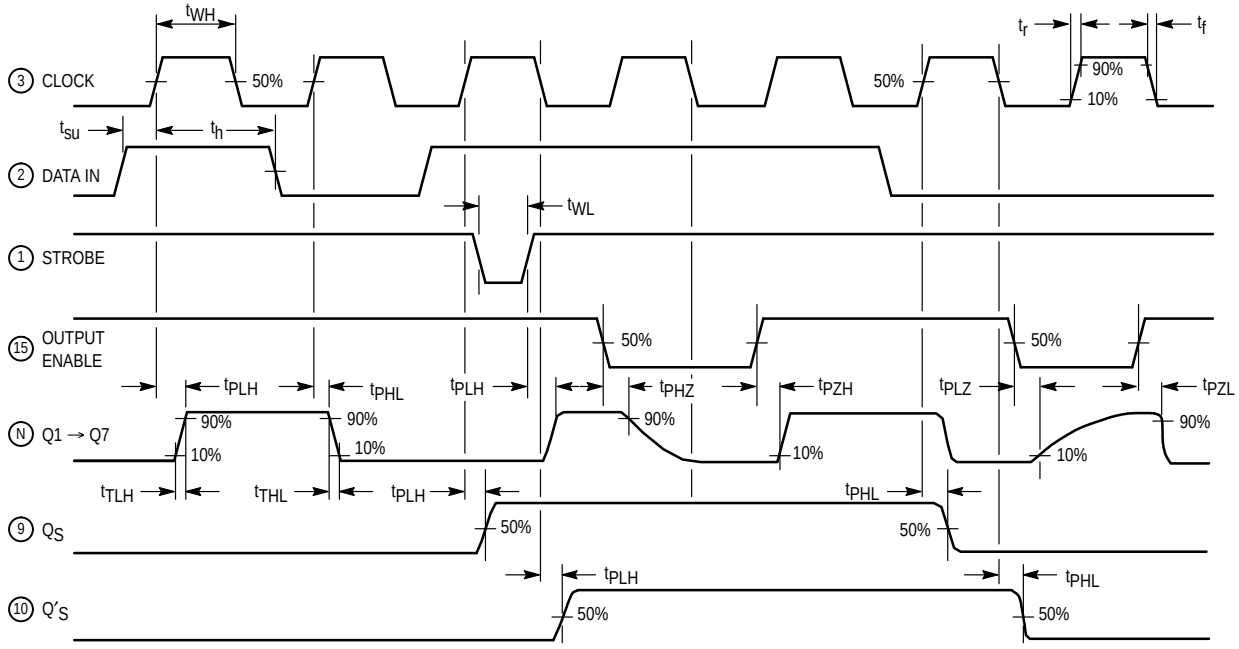
3–STATE TEST CIRCUIT



BLOCK DIAGRAM

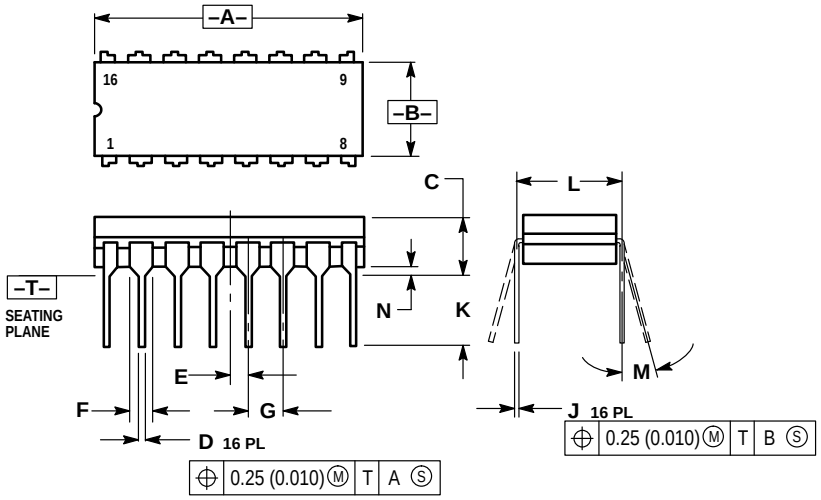


DYNAMIC TIMING DIAGRAM



OUTLINE DIMENSIONS

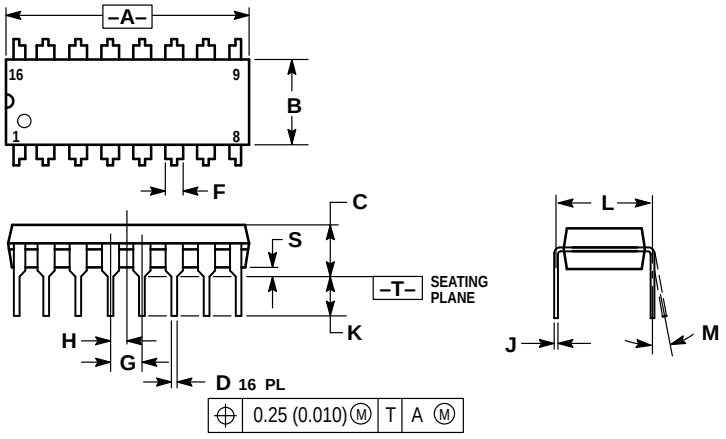
L SUFFIX
CERAMIC DIP PACKAGE
CASE 620–10
ISSUE V



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0 °	15 °	0 °	15 °
N	0.020	0.040	0.51	1.01

P SUFFIX
PLASTIC DIP PACKAGE
CASE 648–08
ISSUE R

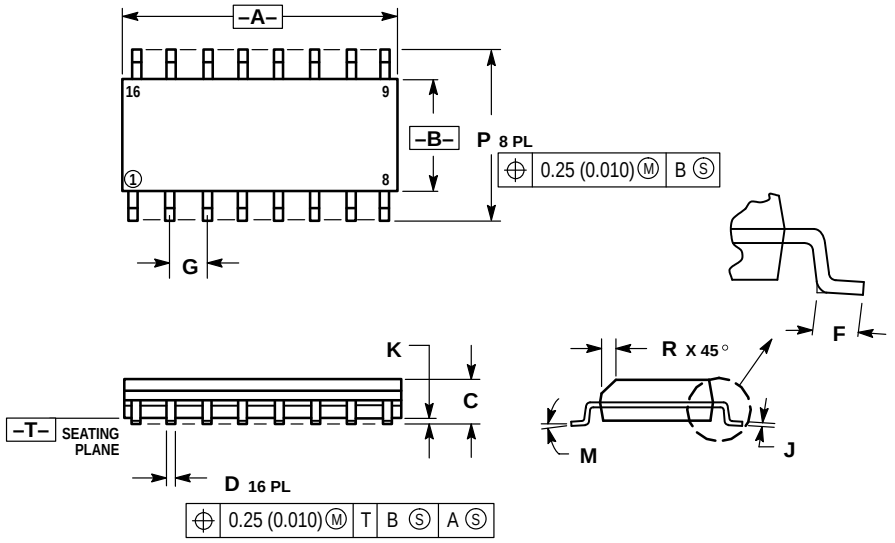


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

OUTLINE DIMENSIONS

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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