

Quad Analog Switch/Quad Multiplexer

The MC14016B quad bilateral switch is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each MC14016B consists of four independent switches capable of controlling either digital or analog signals. The quad bilateral switch is used in signal gating, chopper, modulator, demodulator and CMOS logic implementation.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Linearized Transfer Characteristics
- Low Noise — $12 \text{ nV}/\sqrt{\text{Cycle}}$, $f \geq 1.0 \text{ kHz}$ typical
- Pin-for-Pin Replacements for CD4016B, CD4066B (Note improved transfer characteristic design causes more parasitic coupling capacitance than CD4016)
- For Lower R_{ON} , Use The HC4016 High-Speed CMOS Device or The MC14066B
- This Device Has Inputs and Outputs Which Do Not Have ESD Protection. Antistatic Precautions Must Be Taken.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	- 0.5 to + 18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	- 0.5 to $V_{DD} + 0.5$	V
I_{in}	Input Current (DC or Transient), per Control Pin	± 10	mA
I_{sw}	Switch Through Current	± 25	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	- 65 to + 150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

† Temperature Derating:

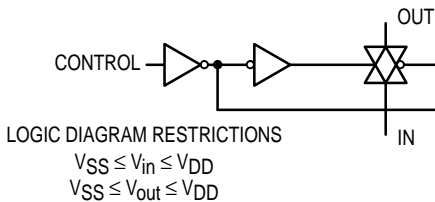
Plastic "P" and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C

Ceramic "L" Packages: - 12 mW/°C From 100°C To 125°C

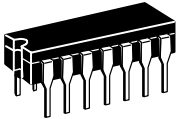
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

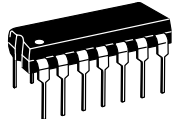
LOGIC DIAGRAM
(1/4 OF DEVICE SHOWN)



MC14016B



L SUFFIX
CERAMIC
CASE 632



P SUFFIX
PLASTIC
CASE 646



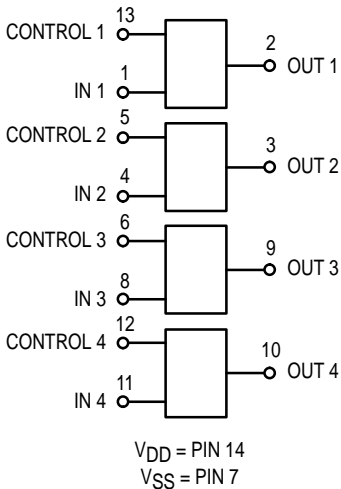
D SUFFIX
SOIC
CASE 751A

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

$T_A = -55^\circ \text{ to } 125^\circ \text{C}$ for all packages.

BLOCK DIAGRAM



Control	Switch
0 = V_{SS}	Off
1 = V_{DD}	On

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Figure	Symbol	V _{DD} Vdc	- 55°C		25°C			125°C		Unit
				Min	Max	Min	Typ #	Max	Min	Max	
Input Voltage Control Input	1	V _{IL}	5.0	—	—	—	1.5	0.9	—	—	Vdc
			10	—	—	—	1.5	0.9	—	—	
			15	—	—	—	1.5	0.9	—	—	
		V _{IH}	5.0	—	—	3.0	2.0	—	—	—	Vdc
			10	—	—	8.0	6.0	—	—	—	
			15	—	—	13	11	—	—	—	
Input Current Control	—	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	± 1.0	μAdc
Input Capacitance Control Switch Input Switch Output Feed Through	—	C _{in}	—	—	—	—	5.0	—	—	—	pF
			—	—	—	—	5.0	—	—	—	
			—	—	—	—	5.0	—	—	—	
			—	—	—	—	0.2	—	—	—	
Quiescent Current (Per Package)	2,3	I _{DD}	5.0	—	0.25	—	0.0005	0.25	—	7.5	μAdc
			10	—	0.5	—	0.0010	0.5	—	15	
			15	—	1.0	—	0.0015	1.0	—	30	
“ON” Resistance (V _C = V _{DD} , R _L = 10 kΩ) (V _{in} = + 5.0 Vdc) (V _{in} = - 5.0 Vdc) V _{SS} = - 5.0 Vdc (V _{in} = ± 0.25 Vdc) (V _{in} = + 7.5 Vdc) (V _{in} = - 7.5 Vdc) V _{SS} = - 7.5 Vdc (V _{in} = ± 0.25 Vdc) (V _{in} = + 10 Vdc) (V _{in} = + 0.25 Vdc) V _{SS} = 0 Vdc (V _{in} = + 5.6 Vdc) (V _{in} = + 15 Vdc) (V _{in} = + 0.25 Vdc) V _{SS} = 0 Vdc (V _{in} = + 9.3 Vdc)	4,5,6	R _{ON}	—	—	—	—	—	—	—	—	Ohms
			—	—	600	—	300	660	—	840	
			—	—	600	—	300	660	—	840	
			5.0	—	600	—	280	660	—	840	
			—	—	360	—	240	400	—	520	
			—	—	360	—	240	400	—	520	
			7.5	—	360	—	180	400	—	520	
			—	—	600	—	260	660	—	840	
			—	—	600	—	310	660	—	840	
			10	—	600	—	310	660	—	840	
			—	—	360	—	260	400	—	520	
			—	—	360	—	260	400	—	520	
			15	—	360	—	300	400	—	520	
Δ “ON” Resistance Between any 2 circuits in a common package (V _C = V _{DD}) (V _{in} = ± 5.0 Vdc, V _{SS} = - 5.0 Vdc) (V _{in} = ± 7.5 Vdc, V _{SS} = - 7.5 Vdc)	—	ΔR _{ON}	—	—	—	—	—	—	—	—	Ohms
			5.0	—	—	—	15	—	—	—	
			7.5	—	—	—	10	—	—	—	
Input/Output Leakage Current (V _C = V _{SS}) (V _{in} = + 7.5, V _{out} = - 7.5 Vdc) (V _{in} = - 7.5, V _{out} = + 7.5 Vdc)	—	—	—	—	—	—	—	—	—	—	μAdc
			7.5	—	±0.1	—	±0.0015	±0.1	—	± 1.0	
			7.5	—	±0.1	—	±0.0015	±0.1	—	± 1.0	

NOTE: All unused inputs must be returned to V_{DD} or V_{SS} as appropriate for the circuit application.

#Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

** For voltage drops across the switch (ΔV_{switch}) > 600 mV (> 300 mV at high temperature), excessive V_{DD} current may be drawn; i.e., the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.) Reference Figure 14.

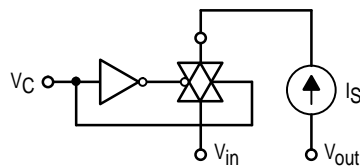
ELECTRICAL CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Figure	Symbol	V _{DD} Vdc	Min	Typ #	Max	Unit
Propagation Delay Time ($V_{SS} = 0 \text{ Vdc}$) V_{in} to V_{out} ($V_C = V_{DD}$, $R_L = 10 \text{ k}\Omega$)	7	t_{PLH} , t_{PHL}	5.0 10 15	— — —	15 7.0 6.0	45 15 12	ns
Control to Output ($V_{in} \leq 10 \text{ Vdc}$, $R_L = 10 \text{ k}\Omega$)	8	t_{PHZ} , t_{PLZ} , t_{PZH} , t_{PZL}	5.0 10 15	— — —	34 20 15	90 45 35	ns
Crosstalk, Control to Output ($V_{SS} = 0 \text{ Vdc}$) ($V_C = V_{DD}$, $R_{in} = 10 \text{ k}\Omega$, $R_{out} = 10 \text{ k}\Omega$, $f = 1.0 \text{ kHz}$)	9	—	5.0 10 15	— — —	30 50 100	— — —	mV
Crosstalk between any two switches ($V_{SS} = 0 \text{ Vdc}$) ($R_L = 1.0 \text{ k}\Omega$, $f = 1.0 \text{ MHz}$, crosstalk = $20 \log_{10} \frac{V_{out1}}{V_{out2}}$)	—	—	5.0	—	– 80	—	dB
Noise Voltage ($V_{SS} = 0 \text{ Vdc}$) ($V_C = V_{DD}$, $f = 100 \text{ Hz}$) ($V_C = V_{DD}$, $f = 100 \text{ kHz}$)	10,11	—	5.0 10 15 5.0 10 15	— — — — — —	24 25 30 12 12 15	— — — — — —	nV/ $\sqrt{\text{Cycle}}$
Second Harmonic Distortion ($V_{SS} = -5.0 \text{ Vdc}$) ($V_{in} = 1.77 \text{ Vdc}$, RMS Centered @ 0.0 Vdc , $R_L = 10 \text{ k}\Omega$, $f = 1.0 \text{ kHz}$)	—	—	5.0	—	0.16	—	%
Insertion Loss ($V_C = V_{DD}$, $V_{in} = 1.77 \text{ Vdc}$, $V_{SS} = -5.0 \text{ Vdc}$, RMS centered = 0.0 Vdc , $f = 1.0 \text{ MHz}$) $I_{loss} = 20 \log_{10} \frac{V_{out}}{V_{in}}$ ($R_L = 1.0 \text{ k}\Omega$) ($R_L = 10 \text{ k}\Omega$) ($R_L = 100 \text{ k}\Omega$) ($R_L = 1.0 \text{ M}\Omega$)	12	—	5.0	— — — —	2.3 0.2 0.1 0.05	— — — —	dB
Bandwidth (– 3.0 dB) ($V_C = V_{DD}$, $V_{in} = 1.77 \text{ Vdc}$, $V_{SS} = -5.0 \text{ Vdc}$, RMS centered @ 0.0 Vdc) ($R_L = 1.0 \text{ k}\Omega$) ($R_L = 10 \text{ k}\Omega$) ($R_L = 100 \text{ k}\Omega$) ($R_L = 1.0 \text{ M}\Omega$)	12,13	BW	5.0	— — — —	54 40 38 37	— — — —	MHz
OFF Channel Feedthrough Attenuation ($V_{SS} = -5.0 \text{ Vdc}$) ($V_C = V_{SS}$, $20 \log_{10} \frac{V_{out}}{V_{in}} = -50 \text{ dB}$) ($R_L = 1.0 \text{ k}\Omega$) ($R_L = 10 \text{ k}\Omega$) ($R_L = 100 \text{ k}\Omega$) ($R_L = 1.0 \text{ M}\Omega$)	—	—	5.0	— — — —	1250 140 18 2.0	— — — —	kHz

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

PIN ASSIGNMENT

IN 1	1	14	V _{DD}
OUT 1	2	13	CONTROL 1
OUT 2	3	12	CONTROL 4
IN 2	4	11	IN 4
CONTROL 2	5	10	OUT 4
CONTROL 3	6	9	OUT 3
V _{SS}	7	8	IN 3



V_{IL} : V_C is raised from V_{SS} until $V_C = V_{IL}$.
 at $V_C = V_{IL}$: $I_S = \pm 10 \mu A$ with $V_{in} = V_{SS}$, $V_{out} = V_{DD}$ or $V_{in} = V_{DD}$, $V_{out} = V_{SS}$.
 V_{IH} : When $V_C = V_{IH}$ to V_{DD} , the switch is ON and the R_{ON} specifications are met.

Figure 1. Input Voltage Test Circuit

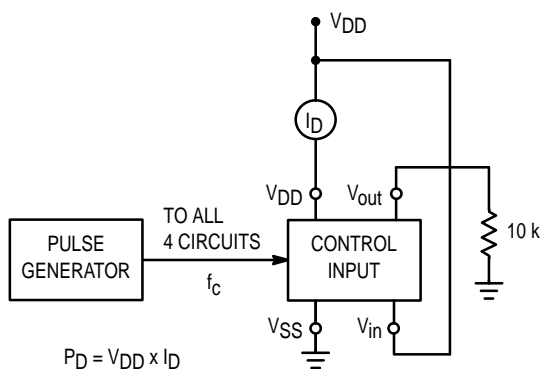


Figure 2. Quiescent Power Dissipation Test Circuit

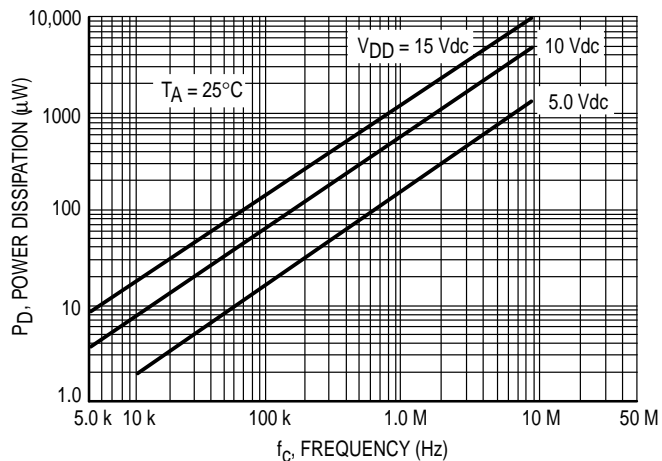


Figure 3. Typical Power Dissipation per Circuit (1/4 of device shown)

TYPICAL R_{ON} versus INPUT VOLTAGE

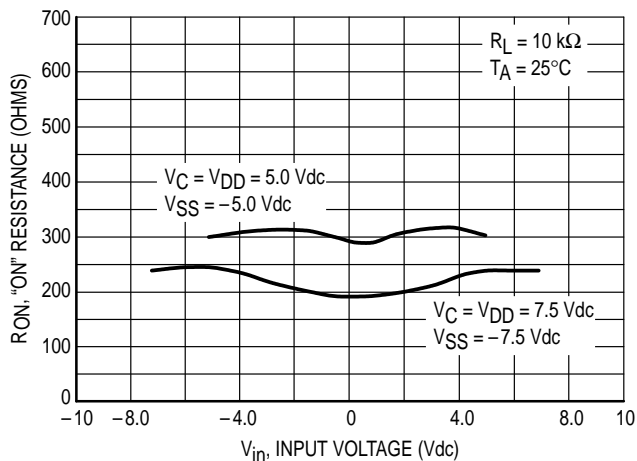


Figure 4. $V_{SS} = -5.0 V$ and $-7.5 V$

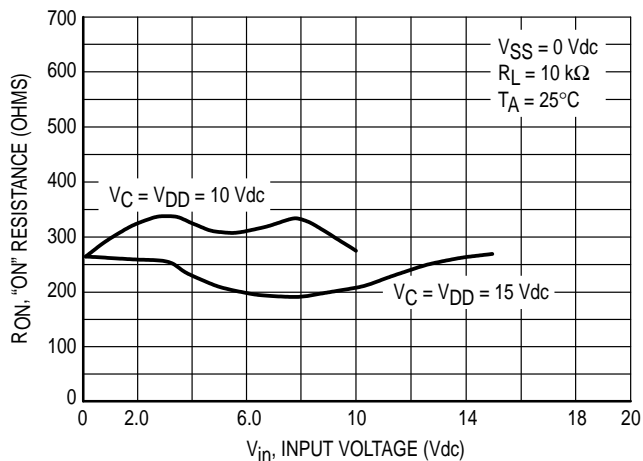


Figure 5. $V_{SS} = 0 V$

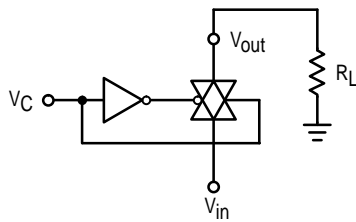


Figure 6. RON Characteristics Test Circuit

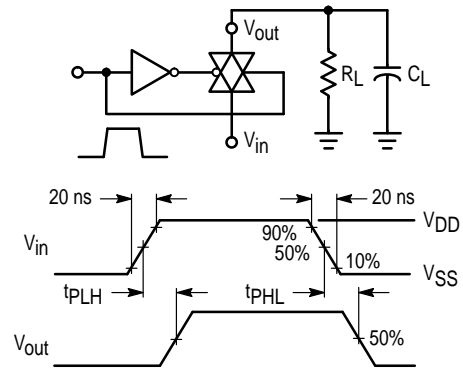


Figure 7. Propagation Delay Test Circuit and Waveforms

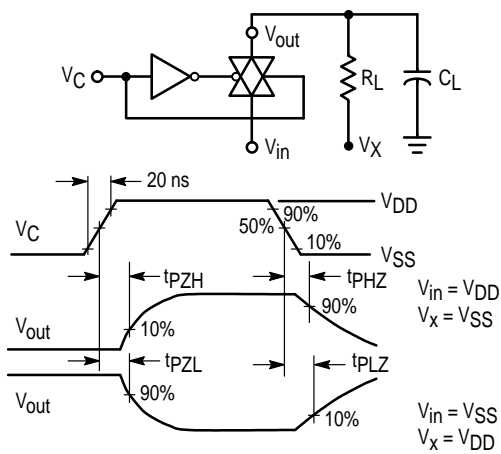


Figure 8. Turn-On Delay Time Test Circuit and Waveforms

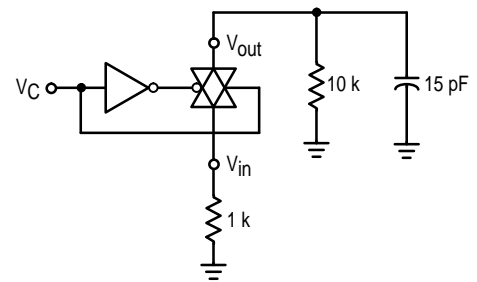


Figure 9. Crosstalk Test Circuit

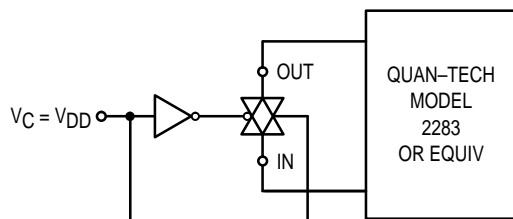


Figure 10. Noise Voltage Test Circuit

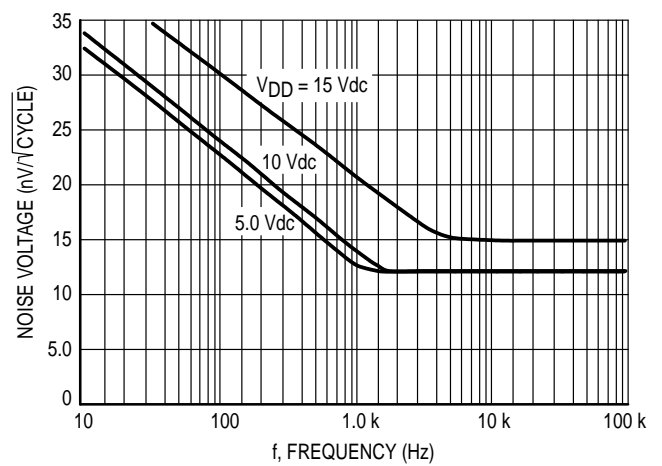


Figure 11. Typical Noise Characteristics

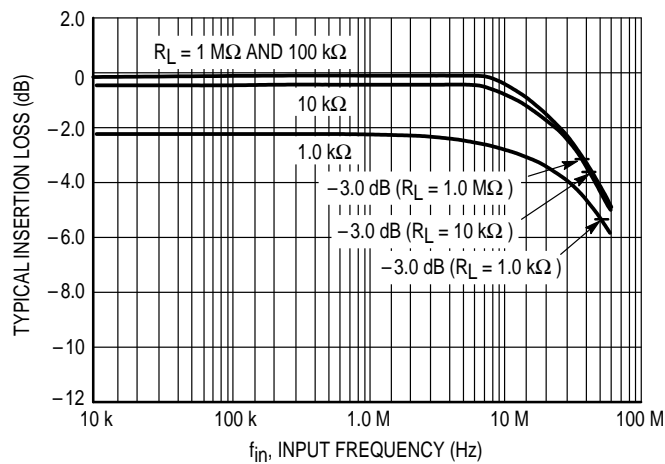


Figure 12. Typical Insertion Loss/Bandwidth Characteristics

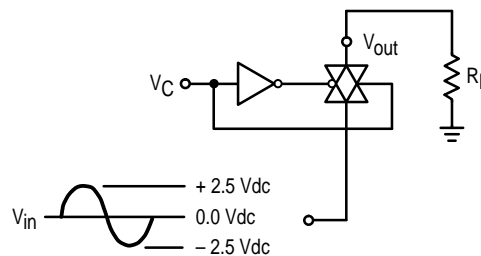


Figure 13. Frequency Response Test Circuit

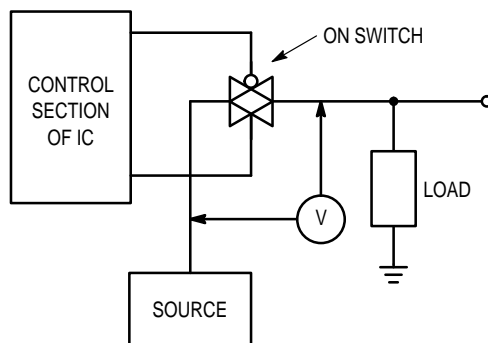


Figure 14. ΔV Across Switch

APPLICATIONS INFORMATION

Figure A illustrates use of the Analog Switch. The 0-to-5 V Digital Control signal is used to directly control a 5 V_{p-p} analog signal.

The digital control logic levels are determined by V_{DD} and V_{SS} . The V_{DD} voltage is the logic high voltage; the V_{SS} voltage is logic low. For the example, $V_{DD} = +5\text{ V}$ logic high at the control inputs; $V_{SS} = \text{GND} = 0\text{ V}$ logic low.

The maximum analog signal level is determined by V_{DD} and V_{SS} . The analog voltage must not swing higher than V_{DD} or lower than V_{SS} .

The example shows a 5 V_{p-p} signal which allows no margin at either peak. If voltage transients above V_{DD} and/or below V_{SS} are anticipated on the analog channels, external diodes (D_x) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The *absolute* maximum potential difference between V_{DD} and V_{SS} is 18.0 V. Most parameters are specified up to 15 V which is the *recommended* maximum difference between V_{DD} and V_{SS} .

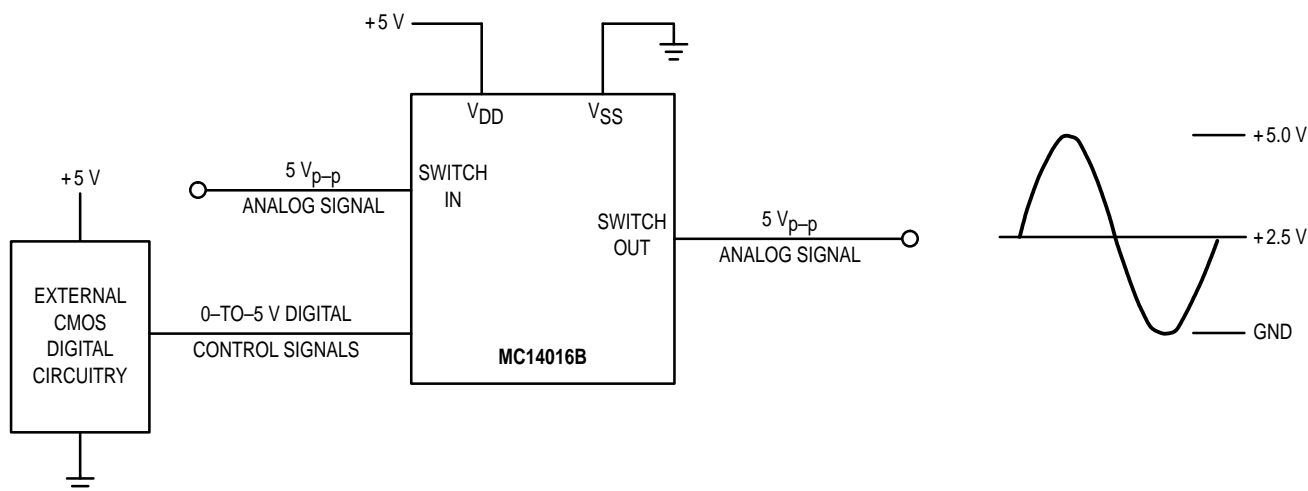


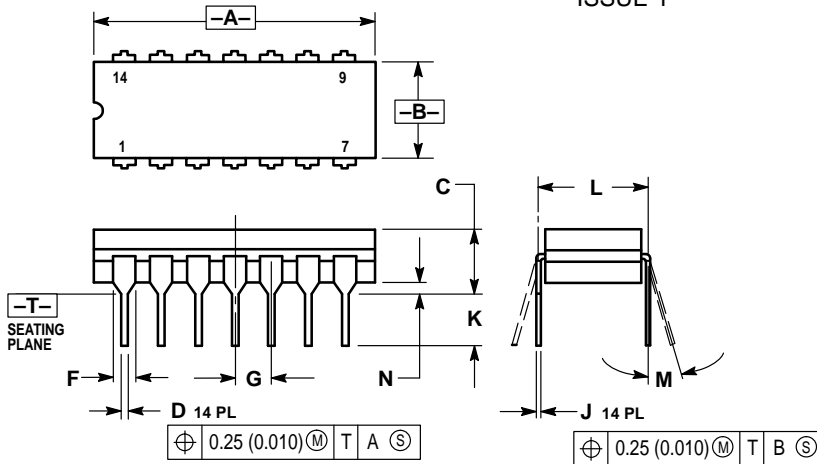
Figure A. Application Example



Figure B. External Germanium or Schottky Clipping Diodes

OUTLINE DIMENSIONS

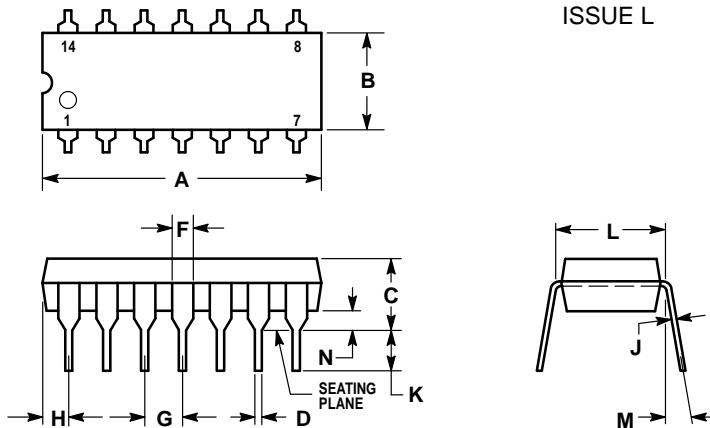
L SUFFIX CERAMIC DIP PACKAGE CASE 632-08 ISSUE Y



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
 4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.94
B	0.245	0.280	6.23	7.11
C	0.155	0.200	3.94	5.08
D	0.015	0.020	0.39	0.50
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

P SUFFIX PLASTIC DIP PACKAGE CASE 646-06 ISSUE L

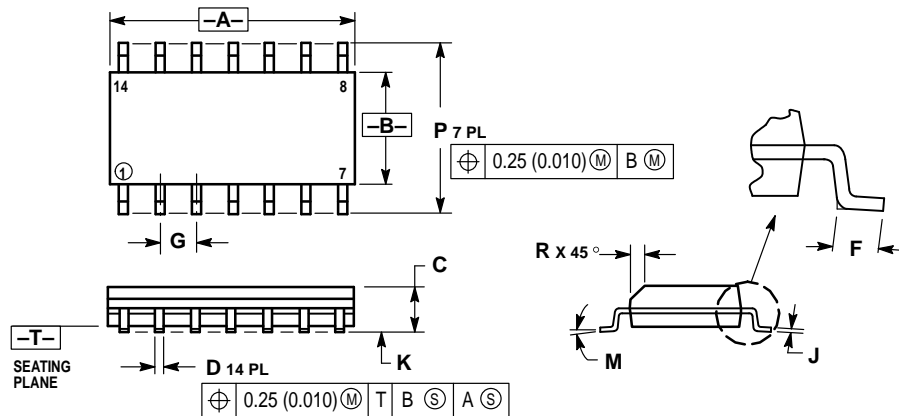


- NOTES:
1. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
 2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
 4. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	10°	0°	10°
N	0.015	0.039	0.39	1.01

OUTLINE DIMENSIONS

D SUFFIX PLASTIC SOIC PACKAGE CASE 751A-03 ISSUE F



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

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MC14016B/D



