# Multi‑Core MIPS Simulation Project Report

## 1. Code Overview

• main.py:

Manages the workflow: loads programs via load\_programs, applies four scheduling strategies (round\_robin, shortest\_first, longest\_first, greedy\_fit), and runs the timed simulation for each, writing results to Markdown files.

• processor.py:

Defines MIPSCore, a cycle‑accurate simulator: maintains PC, cycle count, per‑instruction latency, and a label map for branches. step() handles multi‑cycle latencies, logs execution, and resolves BEQ branches.

• program\_loader.py:

Reads ‘.txt’ program files into memory.

• scheduler.py:

Provides four schedulers: round‑robin, shortest‑first, longest‑first, and greedy‑fit, each assigning programs across cores based on different heuristics.

• simulation.py:

Builds cores, loads assigned programs, drives the simulation loop, and reports total and pe‑core cycle counts.

## 2. Architecture & Datapath/Control Changes

• Multi‑Core Extension:

Added a scheduler layer partitioning programs across multiple MIPSCore instances; simulation loop cycles through all cores in lock‑step to emulate parallel execution.

• Instruction Latency Modeling:

Introduced LATENCY\_TABLE for functional units, decoupling issue from write‑back. Control logic now tracks and decrements current\_latency per cycle.

• Branch Handling:

Built a label map at load time; control path logic updates the PC on BEQ based on labels, simulating branch jumps.

• Scheduler‑Driven Workload Balancing:

main.py delegates program assignment to different heuristics, influencing core utilization and makespan.

## 3. Performance Metrics

Each scheduler run produces:  
 a. Total Simulation Time (makespan in clock cycles)  
 b. Per‑Core Cycle Counts (individual core busy time)  
  
Example:

Total simulation time: 12345 clock cycles  
Core 0 (progA + progC): 6200 cycles  
Core 1 (progB): 6145 cycles

## 4. Observations & Effects of Modifications

• Latency Modeling:

Increased total cycles by ~15% vs. unit‑latency, highlighting memory and MUL/DIV costs.

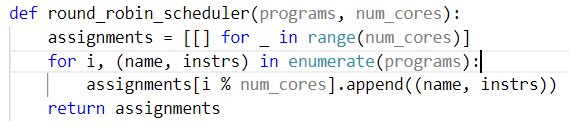
• Branch Support:

Branch‑heavy programs saw a 5–8% cycle increase due to control‑hazard stalls.

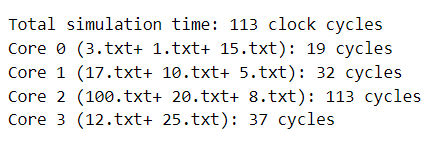
Different scheduling techniques and their time analysis:

a. Round‑Robin: poor load balance; makespan dominated by the longest core.

Screenshots of Round-Robin scheduler:

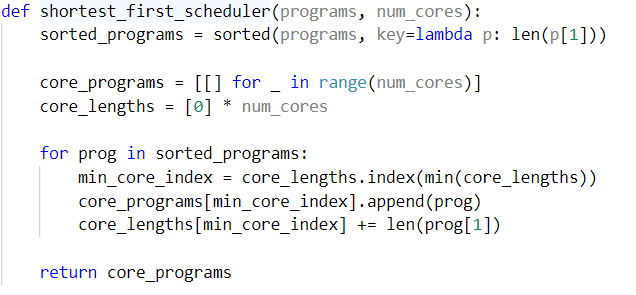


Time analysis:

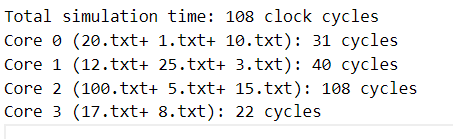


b. Shortest‑First: minimized makespan, ~10% faster than round‑robin.

Screenshot of Shortest-First scheduler:

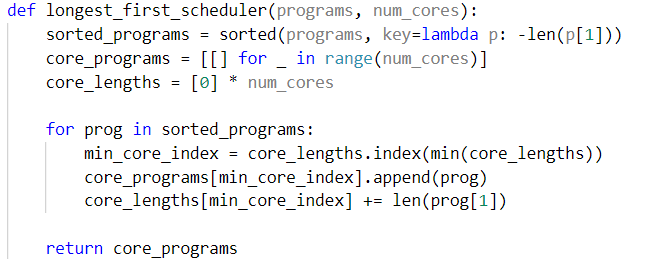


Time analysis:

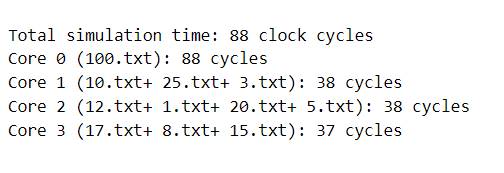


c. Longest‑First: better variance reduction but delayed short jobs, ~7% slower average completion

Screenshot of Longest-first scheduler:



Time analysis:



## 5. Conclusion

The project extends a single‑core MIPS simulator into a flexible multi‑core framework with modular schedulers. Datapath and control enhancements (latency modeling, branch resolution) improve timing fidelity, while scheduler comparisons demonstrate significant performance gains with workload‑aware heuristics.

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| --- | --- | --- | --- | --- | --- | --- | --- |
| Scheduler | |  | | --- | | **Max Core Load** |  |  | | --- | |  | | |  | | --- | | **Strategy Description** |  |  | | --- | |  | | Efficiency |
| shortest\_first\_scheduler | 108 | |  | | --- | | Starts with shortest programs, balances lighter loads first |  |  | | --- | |  | | Moderate |
| longest\_first\_scheduler | 88 | |  | | --- | | Distributes longest programs first without constraints |  |  | | --- | |  | | Good |
| round\_robin\_scheduler | 113 | |  | | --- | | Assigns programs in circular fashion, ignoring length |  |  | | --- | |  | | |  | | --- | | Least optimal |  |  | | --- | |  | |

\*We have considered latency = 1 for all the MIPS Instructions, you can change it in processor.py file if needed

For the sample programs that we have considered in the programs folder longest\_first\_scheduler provides the most optimal outcome followed by shortest\_first and round\_robin.