正基科技股份有限公司

AMPAK Technology Inc.

產品規格書

SPECIFICATION

PRODUCT NAME： AP6212 (HF)

SPEC. NO.： _____ REV： 2.3

DATE： 10.08. 2018
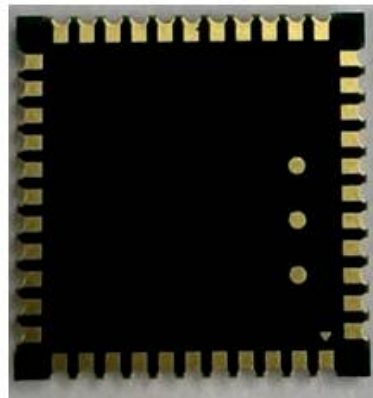
PREPARED	REVIEW		APPROVED	DCC ISSUE
	PM	**QA**		

AMPAK

AP6212

WiFi + Bluetooth 4.1 + FM

SIP Module Spec Sheet

Revision History

Date	Revision Content	Revised By	Version
2017/04/28	Refer to the earlier release for detailed revision history.	Richard	1.9
2017/06/14	- Modify FM spec. - Add BT modulation 8DPSK	Richard	2.0
2017/09/07	- Modify Recommended Reflow Profile	Richard	2.1
2017/09/29	- Add Packing Dimension photo	Beth	2.2
2018/10/08	- Modify Operating Temperature.	Richard	2.3

Contents

1. Introduction

AMPAK Technology would like to announce a low-cost and low-power consumption module which has all of the WiFi, Bluetooth functionalities. The highly integrated module makes the possibilities of web browsing, VoIP, Bluetooth headsets and other applications. With seamless roaming capabilities and advanced security, also could interact with different vendors' 802.11b/g/n Access Points in the wireless LAN.

The wireless module complies with IEEE 802.11 b/g/n standard and it can achieve up to a speed of 72.2Mbps with single stream in 802.11n draft, 54Mbps as specified in IEEE 802.11g, or 11Mbps for IEEE 802.11b to connect to the wireless LAN. The integrated module provides SDIO interface for WiFi, UART / I2S / PCM interface for Bluetooth.

This compact module is a total solution for a combination of WiFi + BT technologies. The module is specifically developed for Smart phones and Portable devices.

2. Features

- 802.11b/g/n single-band radio
- Bluetooth V4.1 with integrated Class 1.5 PA and Low Energy (BLE) support
- Concurrent Bluetooth and WLAN operation
- Simultaneous BT/WLAN receive with single antenna
- WLAN host interface options:
    - SDIO v2.0 — up to 50 MHz clock rate
- BT host digital interface:
    - UART (up to 4 Mbps)
- IEEE Co-existence technologies are integrated die solution
- ECI — enhanced coexistence support, ability to coordinate BT SCO transmissions around WLAN receives

A simplified block diagram of the module is depicted in the figure below.
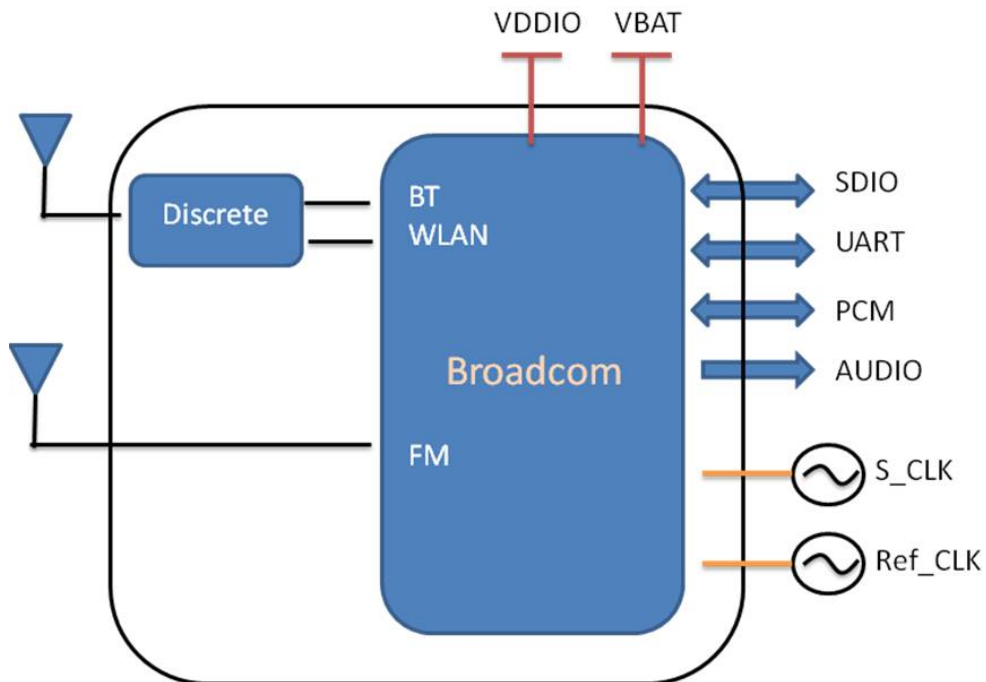
3. Deliverables

3.1 Deliverables

The following products and software will be part of the product.

- Module with packaging
- Evaluation Kits
- Software utility for integration, performance test.
- Product Datasheet.
- Agency certified pre-tested report with the adapter board.

3.2 Regulatory certifications

The product delivery is a pre-tested module, without the module level certification.
For module approval, the platform's antennas are required for the certification.

4. General Specification

4.1 General Specification

Model Name	AP6212
Product Description	Support WiFi/Bluetooth functionalities
Dimension	L x W x H: 12 x 12 x 1.5 (typical) mm
WiFi Interface	SDIOV 2.0
BT Interface	UART / PCM
Operating temperature [a,b]	-30°C to 85°C
Storage temperature	-40°C to 85°C
Humidity	Operating Humidity 10% to 95% Non-Condensing

a. Operating temperature 65 to 85°C is fesable at condictional environment. Please examine the reliability on final product.

b. Functionality is guaranteed across this range of temperature. Optimal RF performance as specified in the data sheet, however, is guaranteed only for –10°C to 55°C.

4.2 Voltages

4.2.1 Absolute Maximum Ratings

Symbol	Description	Min.	Max.	Unit
VBAT	Input supply Voltage	-0.5	5.5	V
VDDIO	Digital/Bluetooth/SDIO/ I/O Voltage	-0.5	3.6	V

4.2.2 Recommended Operating Rating

The module requires two power supplies: VBAT and VDDIO.

	Min.	Typ.	Max.	Unit
Operating Temperature	-30	25	85	deg.C
VBAT	3.0	3.3	3.8	V
VDDIO	1.7	3.3	3.6	V

5. WiFi RF Specification

5.1 2.4GHz RF Specification

Conditions : VBAT=3.3V ; VDDIO=3.3V ; Temp:25°C

Feature	Description	
WLAN Standard	IEEE 802.11b/g/n, WiFi compliant	
Frequency Range	2.400 GHz ~ 2.4835 GHz (2.4 GHz ISM Band)	
Number of Channels	2.4GHz：Ch1 ~ Ch13	
Modulation	802.11b : DQPSK, DBPSK, CCK	
	802.11 g/n : OFDM /64-QAM,16-QAM, QPSK, BPSK	
Output Power	802.11b /11Mbps : 16 dBm ± 1.5 dB @ EVM $\leq$ -9dB	
	802.11g /54Mbps : 15 dBm ± 1.5 dB @ EVM $\leq$ -25dB	
	802.11n /65Mbps : 14 dBm ± 1.5 dB @ EVM $\leq$ -27dB	
Receive Sensitivity (11n,20MHz) @10% PER	- MCS=0	PER @ -85 dBm, +/- 2dB
	- MCS=1	PER @ -84 dBm, +/- 2dB
	- MCS=2	PER @ -82 dBm, +/- 2dB
	- MCS=3	PER @ -80 dBm, +/- 2dB
	- MCS=4	PER @ -77 dBm, +/- 2dB
	- MCS=5	PER @ -73 dBm, +/- 2dB
	- MCS=6	PER @ -71 dBm, +/- 2dB
	- MCS=7	PER @ -68 dBm, +/- 2dB
Receive Sensitivity (11g) @10% PER	- 6Mbps	PER @ -86 dBm, +/- 2dB
	- 9Mbps	PER @ -85 dBm, +/- 2dB
	- 12Mbps	PER @ -85 dBm, +/- 2dB
	- 18Mbps	PER @ -83 dBm, +/- 2dB
	- 24Mbps	PER @ -81 dBm, +/- 2dB
	- 36Mbps	PER @ -78 dBm, +/- 2dB
	- 48Mbps	PER @ -73 dBm, +/- 2dB
	- 54Mbps	PER @ -71 dBm, +/- 2dB
Receive Sensitivity (11b) @8% PER	- 1Mbps	PER @ -90 dBm, +/- 2dB
	- 2Mbps	PER @ -88 dBm, +/- 2dB
	- 5.5Mbps	PER @ -87 dBm, +/- 2dB
	- 11Mbps	PER @ -84 dBm, +/- 2dB
Data Rate	802.11b : 1, 2, 5.5, 11Mbps	
	802.11g : 6, 9, 12, 18, 24, 36, 48, 54Mbps	

Data Rate (20MHz ,Long GI,800ns)	802.11n: 6.5, 13, 19.5, 26, 39, 52, 58.5, 65Mbps
Data Rate (20MHz ,short GI,400ns)	802.11n : 7.2, 14.4, 21.7, 28.9, 43.3, 57.8, 65,72.2Mbps
Maximum Input Level	802.11b : -10 dBm
	802.11g/n : -20 dBm
Antenna Reference	Small antennas with 0~2 dBi peak gain

6. Bluetooth Specification

6.1 Bluetooth Specification

Conditions : VBAT=3.3V ; VDDIO=3.3V ; Temp:25°C

Feature	Description		
General Specification			
Bluetooth Standard	Bluetooth V4.1 of 1, 2 and 3 Mbps.		
Host Interface	UART		
Antenna Reference	Small antennas with 0~2 dBi peak gain		
Frequency Band	2402MHz ~ 2480MHz		
Number of Channels	79 channels		
Modulation	FHSS, GFSK, DPSK, DQPSK, 8DPSK		
RF Specification			
	Min.	**Typical.**	**Max.**
Output Power[1]		7	
Sensitivity @ BER=0.1% for GFSK (1Mbps)		-86 dBm	
Sensitivity @ BER=0.01% for π/4-DQPSK (2Mbps)		-86 dBm	
Sensitivity @ BER=0.01% for 8DPSK (3Mbps)		-80 dBm	
Maximum Input Level	GFSK (1Mbps):-20dBm		
	π/4-DQPSK (2Mbps) :-20dBm		
	8DPSK (3Mbps) :-20dBm		

NOTE[1] : Output power can be configured by HCD firmware.

7. FM Specification

7.1 FM Specification

Conditions : VBAT=3.3V ; VDDIO=3.3V ; Temp:25°C

Feature	Description				
General Specification					
Frequency Band	65MHz-108MHz				
Host Interface	HCI UART, I2S/PCM				
Frequency step	Minimum 10 KHz				
Analog Audio output load	R_L>30KΩ, C_L>20pF				
Characteristics	**Condition**		**MIN**	**TYP**	**MAX**	**UNIT**
Receiver Spec.	FM only, Sensitivity, SNR ≧ 26dB			-5		dBuV
	Audio harmonic distortion, mono (Vin=2Mv EMF, △f=75KHz)	fmod= 1KHz			0.8	%
		fmod= 3KHz			0.8	
	Maximum SNR (fmod=1KHz,△f=22.5KHz, BW=300Hz to 15KHz)	mono		69		dB
		Stereo		64		
	Maximum input level, SNR > 26dB				107	dBuV

8. Pin Assignments

8.1 Pin Outline

< TOP VIEW >
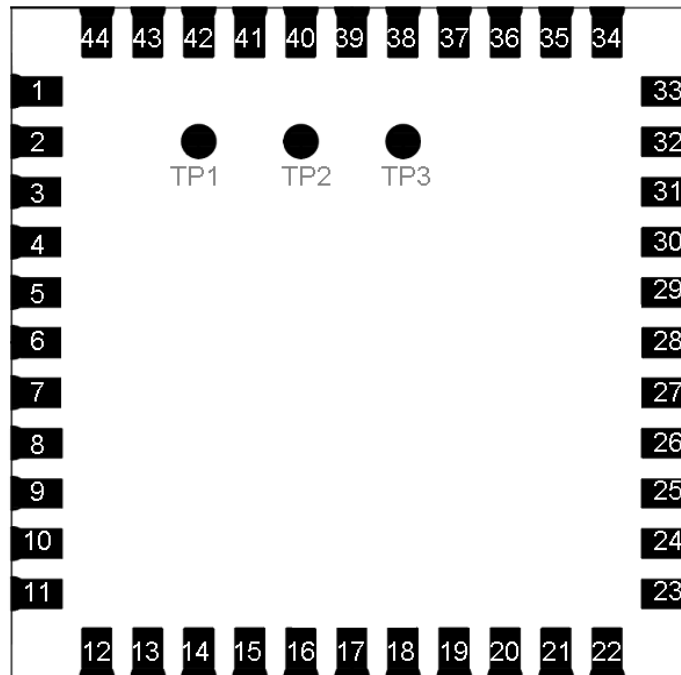
8.2 Pin Definition

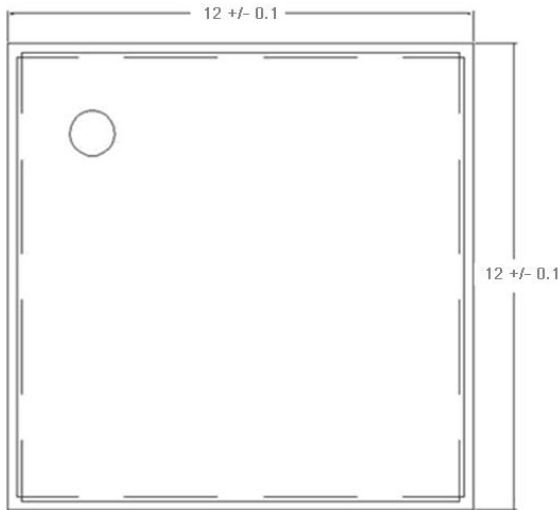| NO	Name	Type	Description
1	GND	—	Ground connections
2	WL_BT_ANT	I/O	RF I/O port
3	GND	—	Ground connections
4	FM_RX	I	FM radio RF input antenna port
5	NC	—	Floating (Don't connected to ground)
6	BT_WAKE	I	HOST wake-up Bluetooth device
7	BT_HOST_WAKE	O	Bluetooth device to wake-up HOST
8	NC	—	Floating (Don't connected to ground)
9	VBAT	P	Main power voltage source input
10	XTAL_IN	I	Crystal input
11	XTAL_OUT	O	Crystal output
12	WL_REG_ON	I	Internal regulators power enable/disable
13	WL_HOST_WAKE	O	WLAN to wake-up HOST

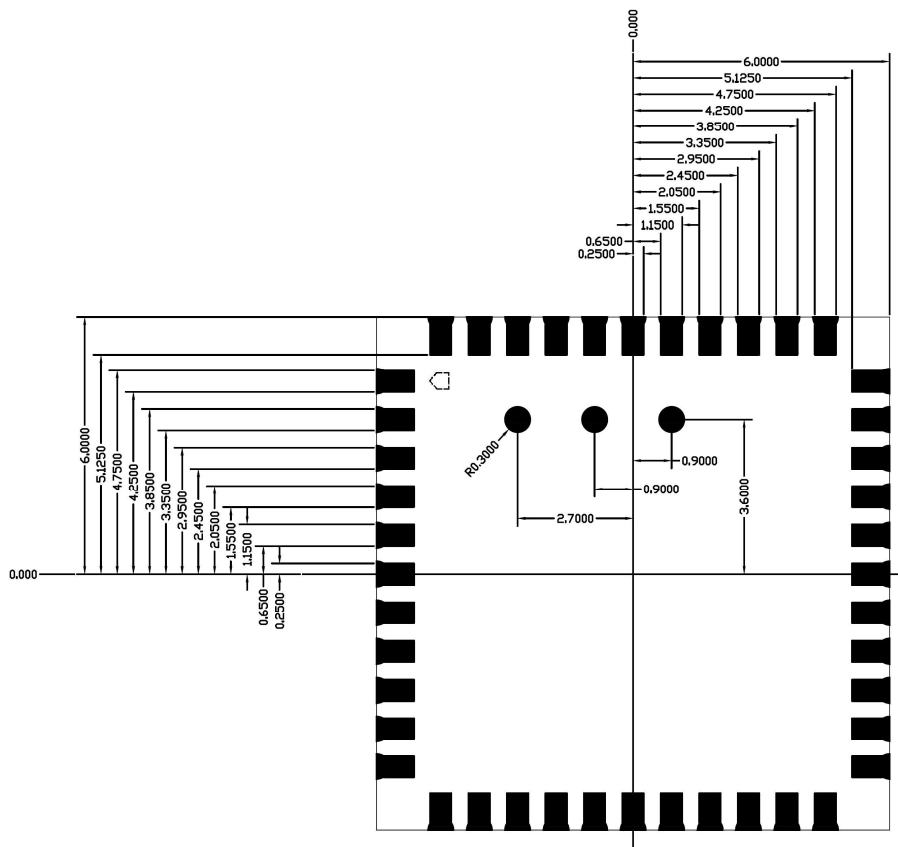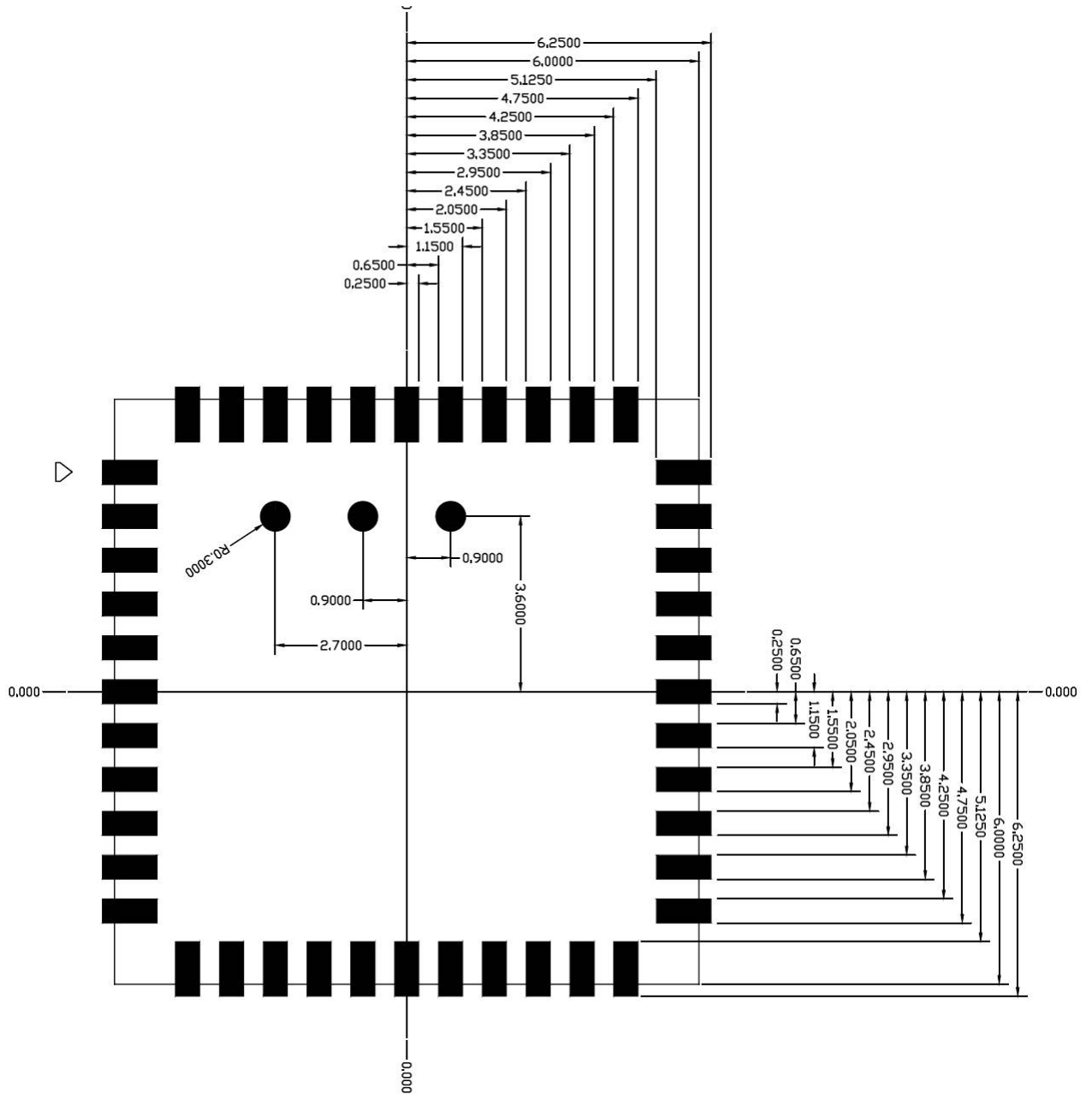| 14	SDIO_DATA_2	I/O	SDIO data line 2
15	SDIO_DATA_3	I/O	SDIO data line 3
16	SDIO_DATA_CMD	I/O	SDIO command line
17	SDIO_DATA_CLK	I/O	SDIO clock line
18	SDIO_DATA_0	I/O	SDIO data line 0
19	SDIO_DATA_1	I/O	SDIO data line 1
20	GND	—	Ground connections
21	VIN_LDO_OUT	P	Internal Buck voltage generation pin
22	VDDIO	P	I/O Voltage supply input
23	VIN_LDO	P	Internal Buck voltage generation pin
24	LPO	I	External Low Power Clock input (32.768KHz)
25	PCM_OUT	O	PCM Data output
26	PCM_CLK	I/O	PCM clock
27	PCM_IN	I	PCM data input
28	PCM_SYNC	I/O	PCM sync signal
29	NC	—	Floating (Don't connected to ground)
30	NC	—	Floating (Don't connected to ground)
31	GND	—	Ground connections
32	NC	—	Floating (Don't connected to ground)
33	GND	—	Ground connections
34	BT_RST_N	I	Low asserting reset for Bluetooth core
35	NC	—	Floating (Don't connected to ground)
36	GND	—	Ground connections
37	NC	—	Floating (Don't connected to ground)
38	NC	—	Floating (Don't connected to ground)
39	GPIO2	I/O	WiFi Co-existence pin with LTE
40	GPIO1	I/O	WiFi Co-existence pin with LTE
41	UART_RTS_N	O	Bluetooth/FM UART interface
42	UART_TXD	O	Bluetooth/FM UART interface
43	UART_RXD	I	Bluetooth/FM UART interface
44	UART_CTS_N	I	Bluetooth/FM UART interface
45	TP1	O	FM Analog AUDIO left output
46	TP2	O	FM Analog AUDIO right output
47	TP3 (NC)	—	Floating (Don't connected to ground)

9. Dimensions

9.1 Physical Dimensions

(Unit: mm)

< TOP VIEW >   < Side View >

12 +/- 0.1

12 +/- 0.1

1.5 +/- 0.1

< TOP VIEW >

0.000

6.0000
5.1250
4.7500
4.2500
3.8500
3.3500
2.9500
2.4500
2.0500
1.5500
1.1500
0.6500
0.2500

6.0000
5.1250
4.7500
4.2500
3.8500
3.3500
2.9500
2.4500
2.0500
1.5500
1.1500
0.6500
0.2500

0.000

R0.3000

2.7000

0.9000

0.9000

3.6000

9.2 Layout Recommendation

(Unit: mm)

< TOP VIEW >

10. External clock reference

External LPO signal characteristics

Parameter	Specification	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	± 30	ppm
Duty cycle	30 - 70	%
Module input Signal Level	400~3300	mV, p-p
Signal type	Square-wave	-
Input impedance	>100k	Ω
	<5	pF
Clock jitter (integrated over 300Hz – 15KHz)	<1	Hz

External Ref_CLK signal characteristics

No.	Item	Symb.	Min.	Type	Max.	Units	Remark
			Electrical Specification				
1	Nominal Frequency	F0		26.00000		MHz	
2	Mode of Vibration			Fundamental			
3	Frequency Tolerance	ΔF/F0	-10	-	10	ppm	at 25°C ±3°C
4	Operating Temperature Range	T_{OPR}	-30	-	85	°C	
5	Frequency Stability	TC	-10	-	10	ppm	
6	Storage Temperature	T_{STG}	-55	-	125	°C	
7	Load capacitance	CL	-	16		pF	
8	Equivalent Series Resistance	ESR	-	-	50	Ω	
9	Drive Level	DL	-	100	200	μW	
10	Insulation Resistance	IR	500	-	-	MΩ	At 100V$_{DC}$
11	Shunt Capacitance	C0	-	-	3	pF	
12	Aging Per Year	Fa	-2	-	2	ppm	First Year

10.1 SDIO Pin Description

The module supports SDIO version 2.0 for 4-bit modes (100 Mbps), and high speed 4-bit (50 MHz clocks – 200 Mbps). It has the ability to stop the SDIO clock and map the interrupt signal into a GPIO pin. This 'out-of-band' interrupt signal notifies the host when the WLAN device wants to turn on the SDIO interface. The ability to force the control of the gated clocks from within the WLAN chip is also provided.

❖ Function 0 Standard SDIO function (Max BlockSize / ByteCount = 32B)

❖ Function 1 Backplane Function to access the internal System On Chip (SOC) address space (Max BlockSize / ByteCount = 64B)

❖ Function 2 WLAN Function for efficient WLAN packet transfer through DMA (Max BlockSize/ByteCount=512B)

SDIO Pin Description

| SD 4-Bit Mode	
DATA0	Data Line 0
DATA1	Data Line 1 or Interrupt
DATA2	Data Line 2 or Read Wait
DATA3	Data Line 3
CLK	Clock
CMD	Command Line

11. Host Interface Timing Diagram

11.1 Power-up Sequence Timing Diagram

The module has signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN and internal regulator blocks. These signals are described below.

Additionally, diagrams are provided to indicate proper sequencing of the signals for carious operating states. The timing value indicated are minimum required values: longer delays are also acceptable.

※ WL_REG_ON: Used by the PMU to power up the WLAN section. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset.

※ BT_RST_N: Low asserting reset for Bluetooth and FM only. This pin has no effect on WLAN and does not control any PMU functions. This pin must be driven high or low (not left floating).
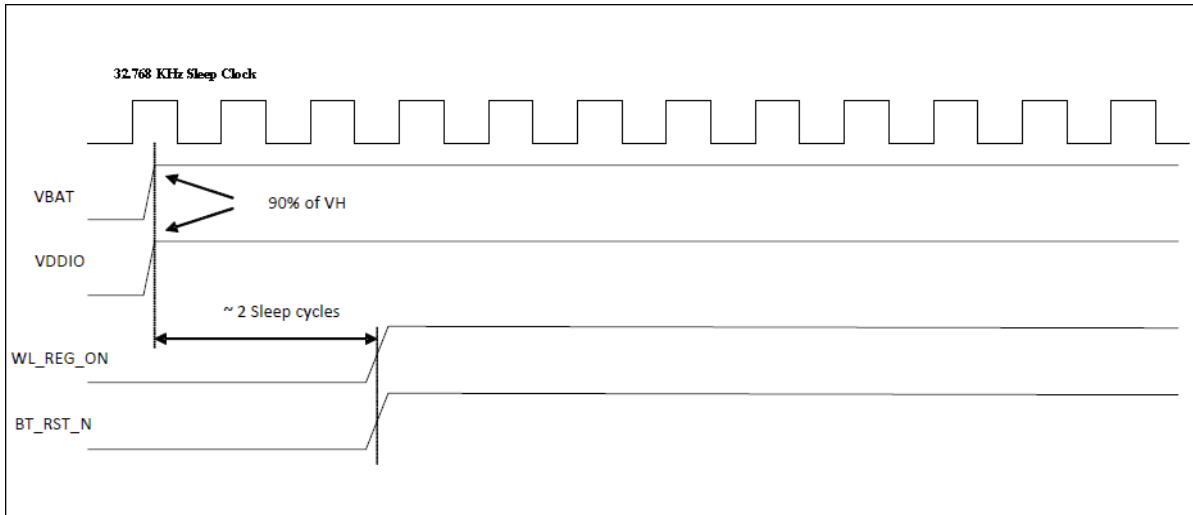
WLAN=ON, Bluetooth=ON
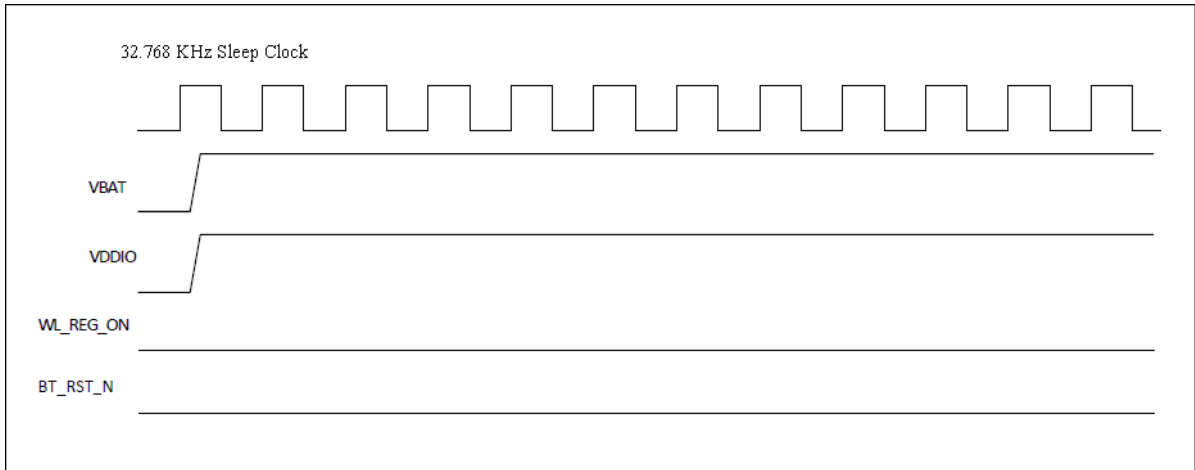
WLAN=OFF, Bluetooth=OFF
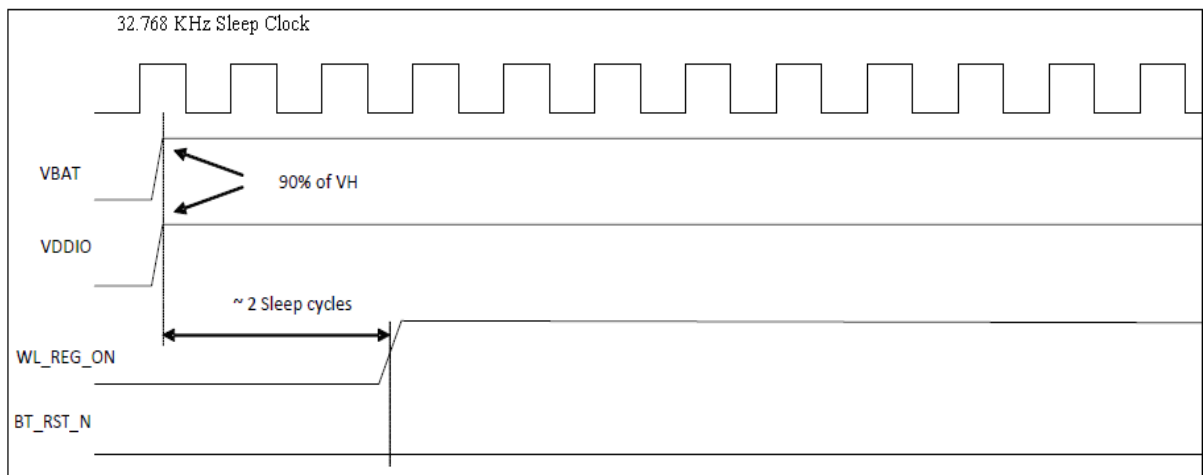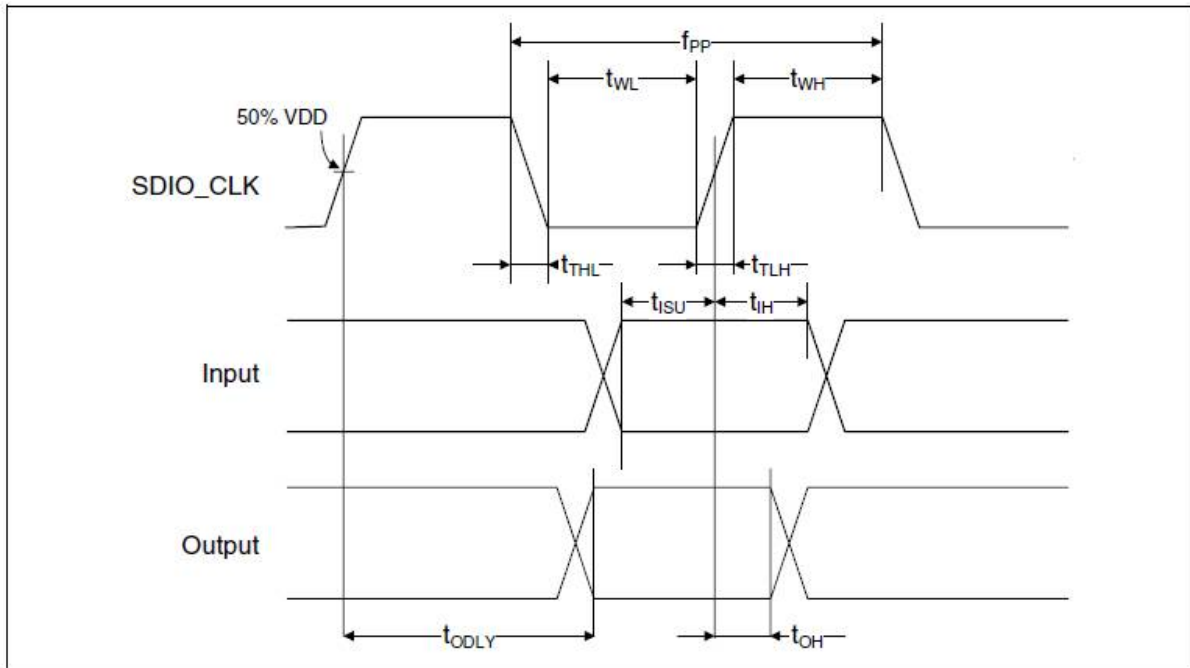

WLAN=ON, Bluetooth=OFF
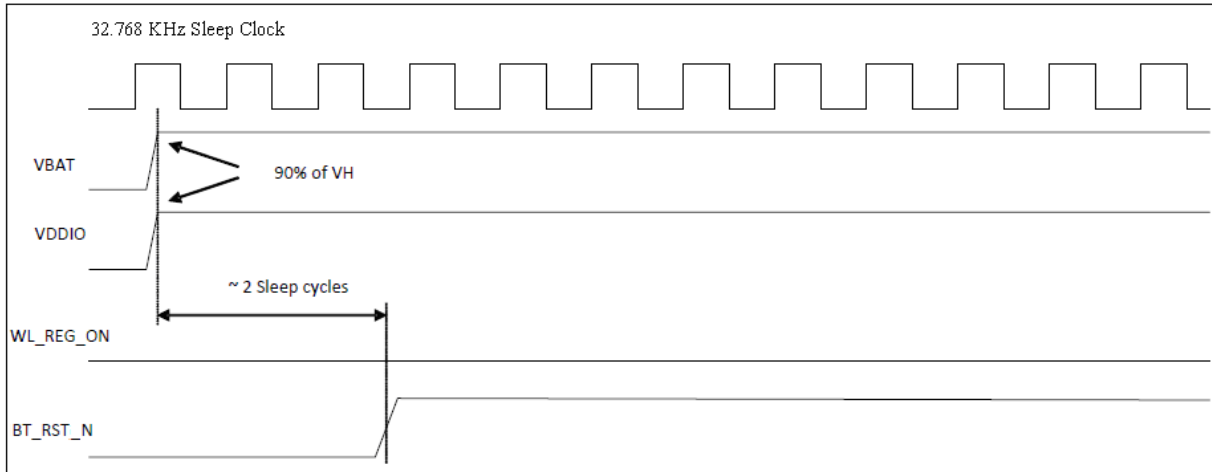
WLAN=OFF, Bluetooth=ON

11.2 SDIO Default Mode Timing Diagram
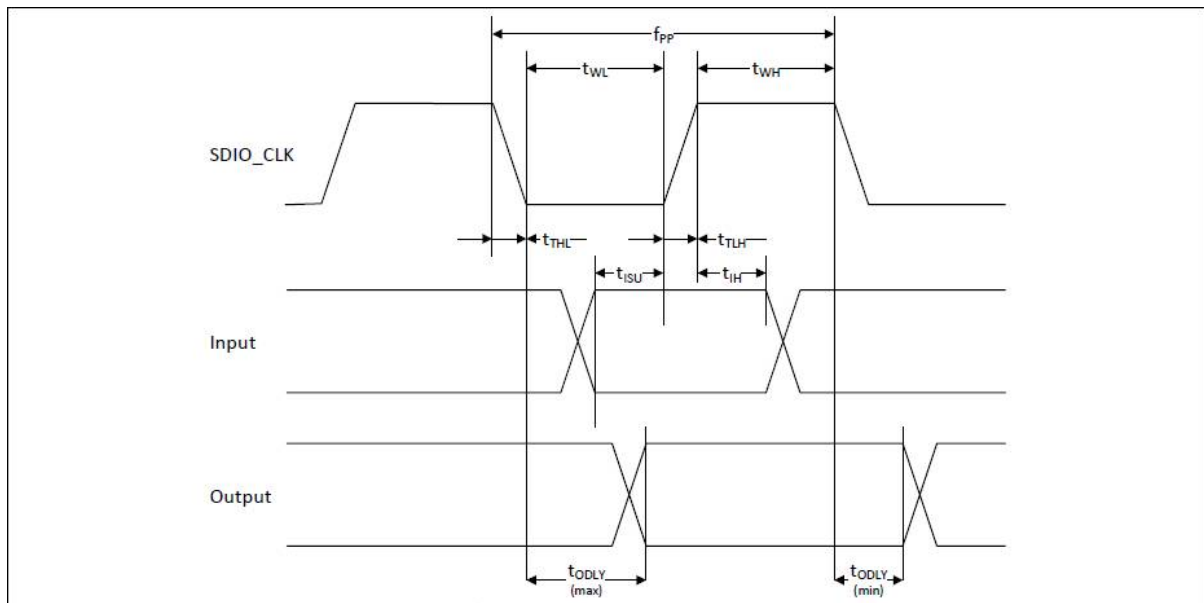
Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are refferred to minimum VIH and maximum VIL^b)					
Frequency-Data Transfer mode	fPP	0	-	25	MHz
Frequency-Identification mode	fOD	0	-	400	kHz
Clock low time	tWL	10	-	-	ns
Clock high time	tWH	10	-	-	ns
Clock rise time	tTLH	-	-	10	ns
Clock low time	tTHL	-	-	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISU	5	-	-	ns
Input hold time	tIH	5	-	-	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	tODLY	0	-	14	ns
Output delay time – Identification mode	tODLY	0	-	50	ns

a. Timing is based on CL ≤ 40pF load on CMD and Data.

b. min(Vih) = 0.7 x VDDIO and max(Vil) = 0.2 x VDDIO.

11.3 SDIO High Speed Mode Timing Diagram

| Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are refferred to minimum VIH and maximum VIL^b)					
Frequency-Data Transfer mode	fPP	0	-	50	MHz
Frequency-Identification mode	fOD	0	-	400	kHz
Clock low time	tWL	7	-	-	ns
Clock high time	tWH	7	-	-	ns
Clock rise time	tTLH	-	-	3	ns
Clock low time	tTHL	-	-	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISU	6	-	-	ns
Input hold time	tIH	2	-	-	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	tODLY	-	-	14	ns
Output hold time	tOH	2.5	-	-	ns
Total system capacitance (each line)	CL	-	-	40	pF

a. Timing is based on CL ≤ 40pF load on CMD and Data.

b. min(Vih) = 0.7 x VDDIO and max(Vil) = 0.2 x VDDIO.

12. Recommended Reflow Profile

Referred to IPC/JEDEC standard.

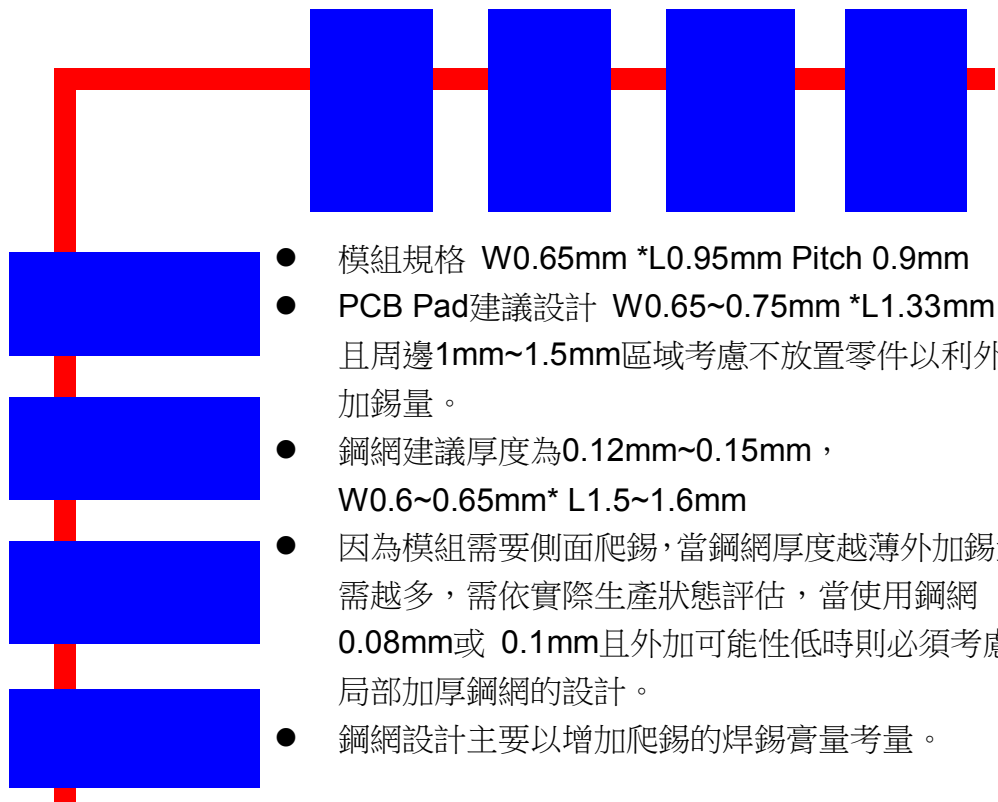Peak Temperature : <250°C

Number of Times : ≤2 times
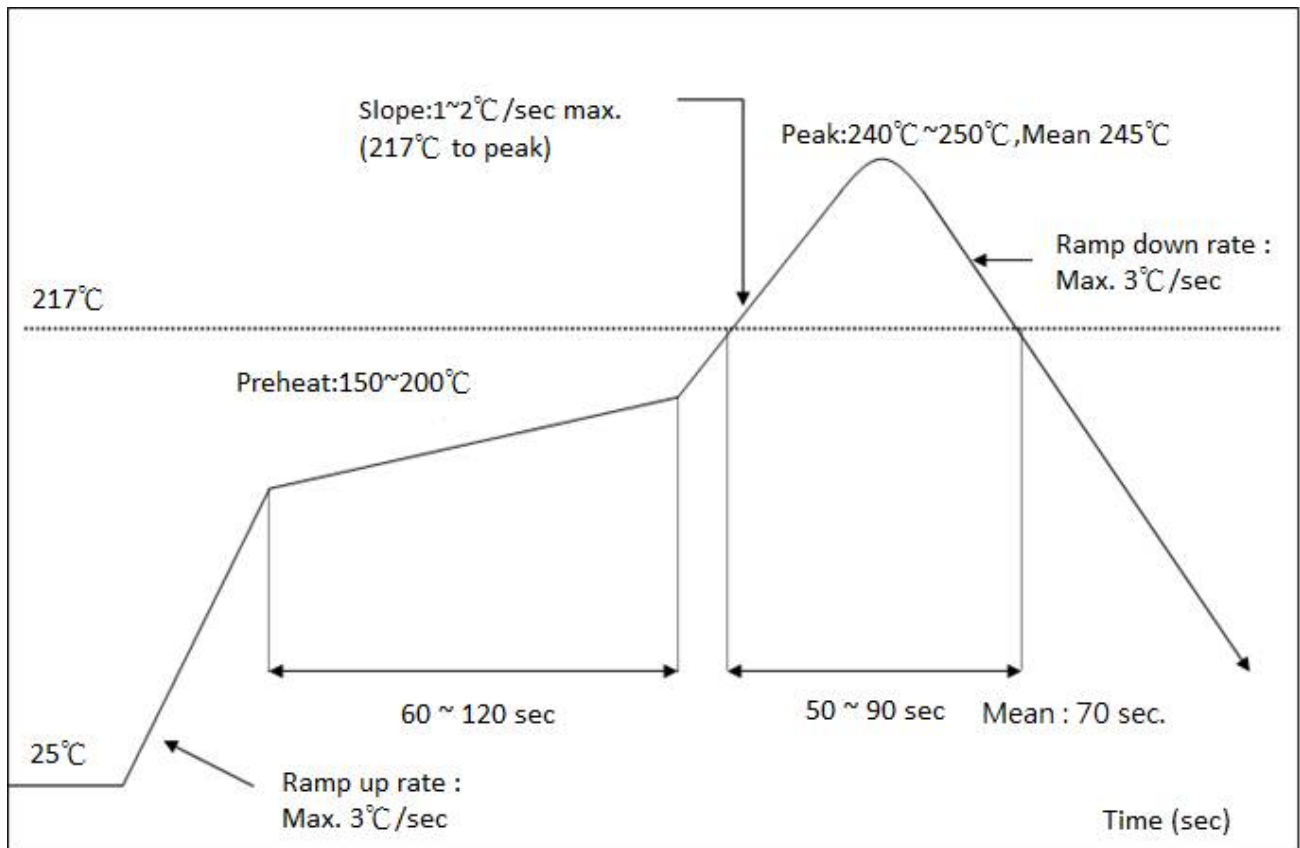
The notification of WiFi module before mounting:

The aperture of stencil should be larger than foot print of module, and the stencil thickness should be not less than 0.12mm.

Reflow 時需使用 N2, 含氧量建議 5000 ppm 以下,

It must use N2 for reflow and suggest the concentration of oxygen less than 5000 ppm .

Solder Paste definition

- 模組規格 W0.65mm *L0.95mm Pitch 0.9mm
- PCB Pad建議設計 W0.65~0.75mm *L1.33mm，
  且周邊1mm~1.5mm區域考慮不放置零件以利外
  加錫量。
- 鋼網建議厚度為0.12mm~0.15mm，
  W0.6~0.65mm* L1.5~1.6mm
- 因為模組需要側面爬錫,當鋼網厚度越薄外加錫量
  需越多，需依實際生產狀態評估，當使用鋼網
  0.08mm或 0.1mm且外加可能性低時則必須考慮
  局部加厚鋼網的設計。
- 鋼網設計主要以增加爬錫的焊錫膏量考量。

- Module Specifications : W:0.65mm * L:0.95mm pitch 0.9 mm
- The proposed design W:0.65~0.75 mm * L:1.33mm. Consider not place other parts in the peripheral area of 1 mm ~ 1.5 mm to facilitate additional amount of solder for PCB pad.
- We Suggest the thickness of Stencil between 0.12 mm ~0.15mm, the W between 0.6~0.65mm and the L between L1.5~1.6mm.
- If the thickness of the stencil is thinner, we suggest to adding more solder, to increase the wetting ability. Depends on different production situation, if the stencil thickness is 0.08~0.1mm, and the module nearby area is no more space for expending soldering area, we will suggest to increase the stencil thickness to increase the wetting ability.
- The major consideration parts of stencil design is to increase the solder paste wetting ability.
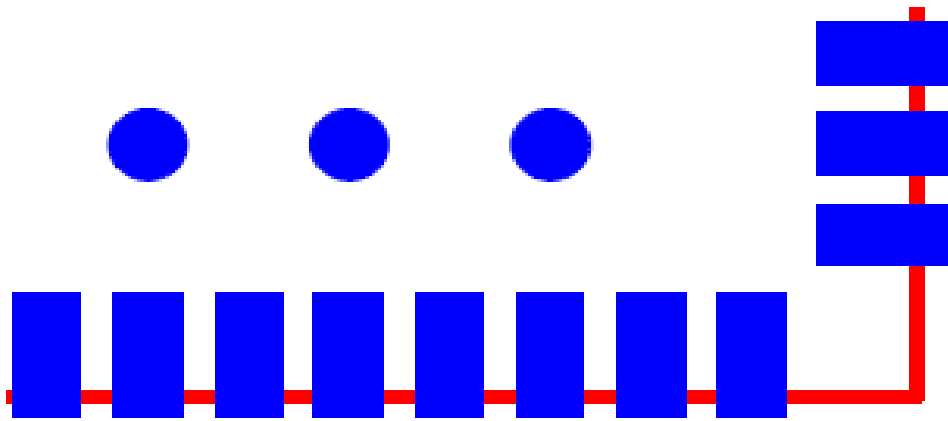
模組規格 L 0.7mm

PCB Pad 設計 L 0.8mm

鋼網開孔建議 L0.5mm~0.6mm

適當內縮可以避免撐高造成高度影響

- Module Specifications L 0.7mm
- The design for PCB Pad : L:0.8mm
- We recommend the apertures for stencil L:0.5mm~0.6mm
- In order to avoid highness impact caused solder paste thickness, the stencil open size can be appropriately retracted

13. Package Information

13.1 Label

Label A→ Anti-static and humidity notice
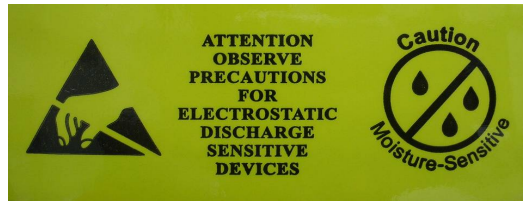
Label B→ MSL caution / Storage Condition

Label C→ Inner box label .

Label D→ Carton box label .

13.2 Dimension

AP6XXX ——→ Part Number
XXXXXXXX ——→ Lot Code
XXXX ——→ Date Code

W	24.00±0.30
A0	12.30±0.10
B0	12.30±0.10
K0	1.80±0.10
E	1.75±0.10
F	11.50±0.10
P0	4.00±0.10
P1	16.00±0.10
P2	2.00±0.10
D0	1.50 +0.10 −0.00
D1	⌀1.50MIN

1. 10 sprocket hole pitch cumulative tolerance ±0.20.
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481-D requirements.
5. Thickness : 0.30±0.05mm.
6. Packing length per 22" reel : 98.5 Meters.(1:3)
7. Component load per 13" reel : 1500 pcs.

ATTENTION
Electrostatic Sensitive Devices
Safe Handling Required

"A"

330.0 REF   100.0 REF

.2

Humidity indicator

Desiccant

B

A

C

C

50mm

338mm

355mm

D

360mm

285mm

375mm
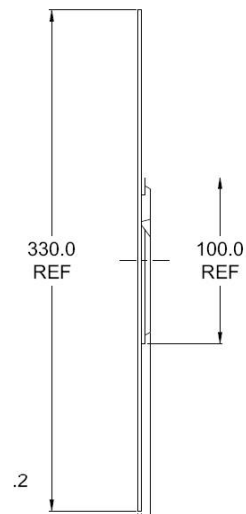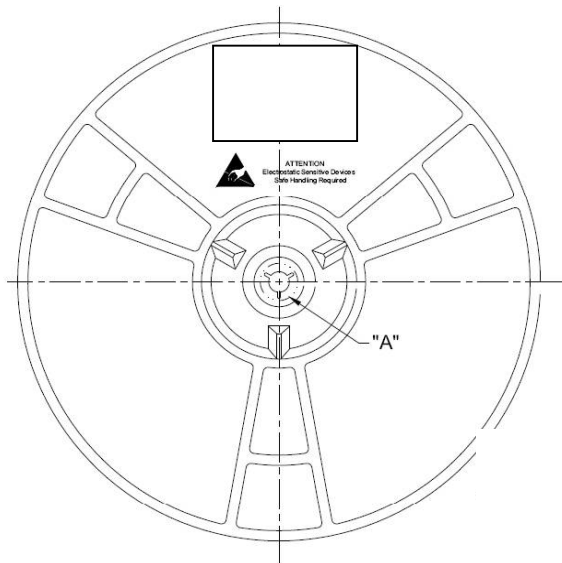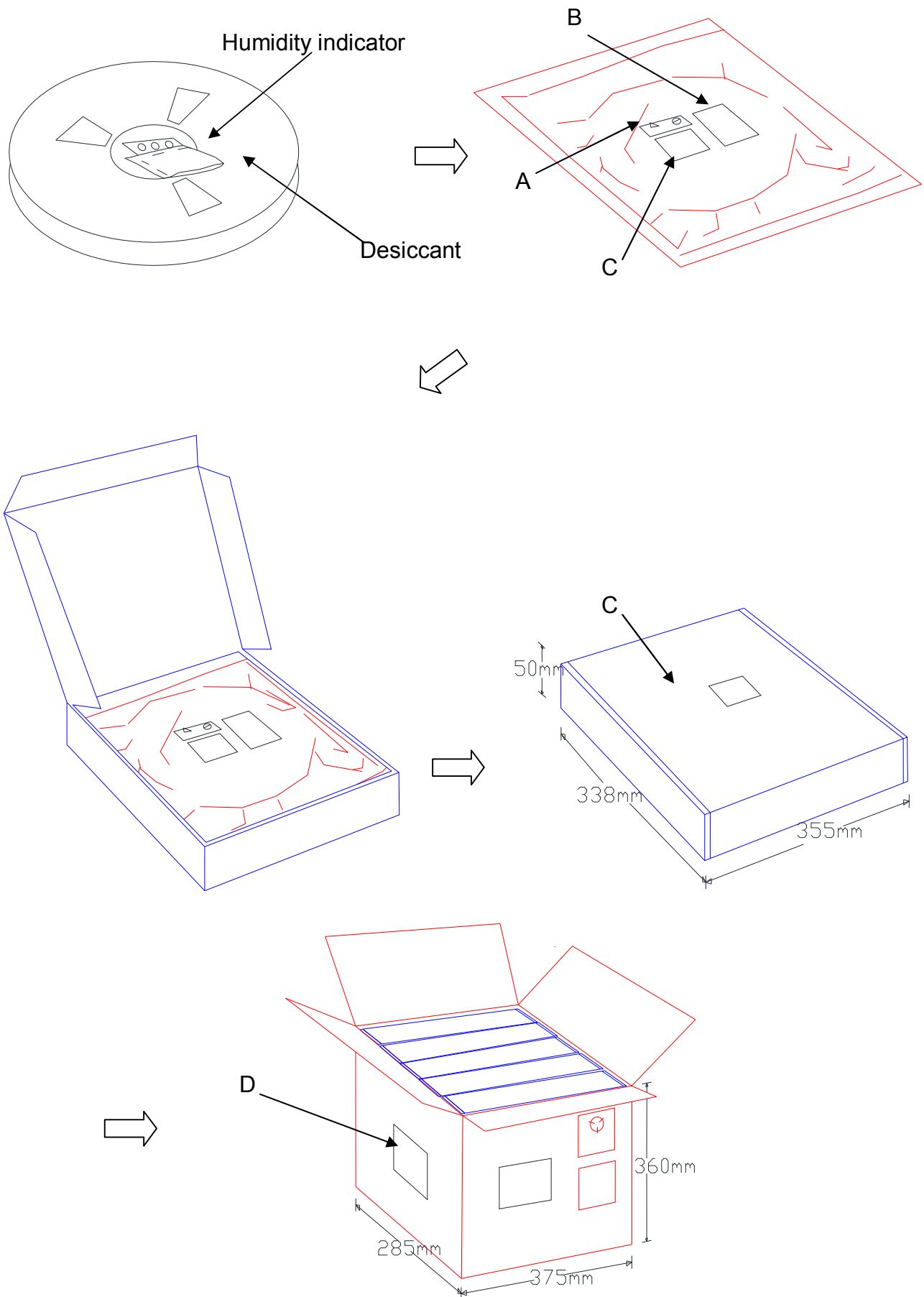
13.3 MSL Level / Storage Condition

LEVEL

4

If blank,see adjacent bar code label

⊘ **Caution**
This bag contains
MOISTURE-SENSITIVE DEVICES

1. Calculated shelf life in sealed bag:12months at<40℃ and <90% relative humidity(RH)

2. Peak package body temperature:_____**250**_____℃
   If blank,see adjacent bar code label

3. After bag is opened,devices that will be subjected to reflow solder or other high temperature process must be

   a) Mounted within:_____**72**_____hours of factory conditions
   If blank,see adjacent bar code label

   ≤30℃/60% RH,or

   b) Stored per J-STD-033

4. Devices require bake,before mounting,if:

   a) Humidity Indicator Card reads>10% for level 2a-5a devices or>60% for level 2 devices when read at 23±5℃

   b) 3a or 3b are not met.

5. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure.

Bag Seal Date:_____
If blank,see adjacent bar code label

Note:Level and body temperature defined by IPC/JEDEC J-STD-020