```
// SELECT bits 1:0
Modify DAP_SGTL_SURROUND->SELECT 0x0003;
// Ramp down the width to original value
for (int i = 0; i++; (7 - usOriginalVal)
{
 --usNextVal;
 Modify DAP_SGTL_SURROUND->WIDTH_CONTROL
usNextVal;
}
```

BASS ENHANCE ON/OFF

This programming example shows how to program the Bass Enhance on/off when end-user turns it on/off on their device.

The Bass level should be ramped down to the lowest Bass before Bass Enhance feature is turned on/off.

```
// Read current Bass level value
// BASS_LEVEL bits 6:0
usOriginalVal = Read DAP_BASS_ENHANCE_CTRL &&
0x007F;
usNextVal = usOriginalVal;
// Ramp Bass level to lowest bass (lowest bass = 0x007F)
usNumSteps = abs(0x007F - usOriginalVal);
for (int i = 0; i++; usNumSteps)
{
 ++usNextVal;
 Modify DAP_BASS_ENHANCE_CTRL->BASS_LEVEL
usNextVal;
}
// Enable (To disable, write 0x0000) Bass Enhance
// EN bit 0
Modify DAP_BASS_ENHANCE->EN 0x0001;
// Ramp Bass level back to original value
for (int i = 0; i++; usNumSteps)
{
 --usNextVal;
 Modify DAP_BASS_ENHANCE_CTRL->BASS_LEVEL
usNextVal;
}
```

AUTOMATIC VOLUME CONTROL (AVC) ON/OFF

This programming example shows how to program the AVC on/off when end-user turns it on/off on their device.

```
// Enable AVC (To disable, write 0x0000)
Modify DAP_AVC_CTRL->EN 0x0001
// bit 0
Register description
CHIP_ID        0x0000
```

Table 16. CHIP_ID 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PARTID								REVID							

BITS	FIELD	RW	RESET	DEFINITION
15:8	PARTID	RO	0xA0	SGTL5000 Part ID 0xA0 - 8 bit identifier for SGTL5000
7:0	REVID	RO	0x00	SGTL5000 Revision ID 0xHH - revision number for SGTL5000.

Table 17. CHIP_DIG_POWER 0x0002

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD									ADC_POWERUP	DAC_POWERUP	DAP_POWERUP	RSVD		I2S_OUT_POWERUP	I2S_IN_POWERUP

BITS	FIELD	RW	RESET	DEFINITION
15:7	RSVD	RO	0x0	Reserved
6	ADC_POWERUP	RW	0x0	Enable/disable the ADC block, both digital and analog 0x0 = Disable 0x1 = Enable

BITS	FIELD	RW	RESET	DEFINITION
5	DAC_POWERUP	RW	0x0	Enable/disable the DAC block, both analog and digital 0x0 = Disable 0x1 = Enable
4	DAP_POWERUP	RW	0x0	Enable/disable the DAP block 0x0 = Disable 0x1 = Enable
3:2	RSVD	RW	0x0	Reserved
1	I2S_OUT_POWERUP	RW	0x0	Enable/disable the I2S data output 0x0 = Disable 0x1 = Enable
0	I2S_IN_POWERUP	RW	0x0	Enable/disable the I2S data input 0x0 = Disable 0x1 = Enable

Table 18. CHIP_CLK_CTRL 0x0004

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										RATE_MODE		SYS_FS		MCLK_FREQ	

BITS	FIELD	RW	RESET	DEFINITION
15:6	RSVD	RO	0x0	Reserved
5:4	RATE_MODE	RW	0x0	Sets the sample rate mode. MCLK_FREQ is still specified relative to the rate in SYS_FS 0x0 = SYS_FS specifies the rate 0x1 = Rate is 1/2 of the SYS_FS rate 0x2 = Rate is 1/4 of the SYS_FS rate 0x3 = Rate is 1/6 of the SYS_FS rate
3:2	SYS_FS	RW	0x2	Sets the internal system sample rate 0x0 = 32 kHz 0x1 = 44.1 kHz 0x2 = 48 kHz 0x3 = 96 kHz
1:0	MCLK_FREQ	RW	0x0	Identifies incoming SYS_MCLK frequency and if the PLL should be used 0x0 = 256*Fs 0x1 = 384*Fs 0x2 = 512*Fs 0x3 = Use PLL The 0x3 (Use PLL) setting must be used if the SYS_MCLK is not a standard multiple of Fs (256, 384, or 512). This setting can also be used if SYS_MCLK is a standard multiple of Fs. Before this field is set to 0x3 (Use PLL), the PLL must be powered up by setting CHIP_ANA_POWER->PLL_POWERUP and CHIP_ANA_POWER->VCOAMP_POWERUP. Also, the PLL dividers must be calculated based on the external MCLK rate and CHIP_PLL_CTRL register must be set (see CHIP_PLL_CTRL register description details on how to calculate the divisors).

Table 19. CHIP_I2S_CTRL 0x0006

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD							SCLKFREQ	MS	SCLK_INV	DLEN		I2S_MODE		LRALIGN	LRPOL

BITS	FIELD	RW	RESET	DEFINITION
15:9	RSVD	RO	0x0	Reserved
8	SCLKFREQ	RW	0x0	Sets frequency of I2S_SCLK when in master mode (MS=1). When in slave mode (MS=0), this field must be set appropriately to match SCLK input rate. 0x0 = 64Fs 0x1 = 32Fs - Not supported for RJ mode (I2S_MODE = 1)
7	MS	RW	0x0	Configures master or slave of I2S_LRCLK and I2S_SCLK. 0x0 = Slave: I2S_LRCLK and I2S_SCLK are inputs 0x1 = Master: I2S_LRCLK and I2S_SCLK are outputs NOTE: If the PLL is used (CHIP_CLK_CTRL->MCLK_FREQ==0x3), the SGTL5000 must be a master of the I^2S port (MS==1)
6	SCLK_INV	RW	0x0	Sets the edge that data (input and output) is clocked in on for I2S_SCLK 0x0 = data is valid on rising edge of I2S_SCLK 0x1 = data is valid on falling edge of I2S_SCLK
5:4	DLEN	RW	0x1	I^2S data length 0x0 = 32 bits (only valid when SCLKFREQ=0), not valid for Right Justified Mode 0x1 = 24 bits (only valid when SCLKFREQ=0) 0x2 = 20 bits 0x3 = 16 bits
3:2	I2S_MODE	RW	0x0	Sets the mode for the I^2S port 0x0 = I^2S mode or Left Justified (Use LRALIGN to select) 0x1 = Right Justified Mode 0x2 = PCM Format A/B 0x3 = RESERVED
1	LRALIGN	RW	0x0	I2S_LRCLK Alignment to data word. Not used for Right Justified mode 0x0 = Data word starts 1 I2S_SCLK delay after I2S_LRCLK transition (I^2S format, PCM format A) 0x1 = Data word starts after I2S_LRCLK transition (left justified format, PCM format B)
0	LRPOL	RW	0x0	I2S_LRCLK Polarity when data is presented. 0x0 = I2S_LRCLK = 0 - Left, 1 - Right 1x0 = I2S_LRCLK = 0 - Right, 1 - Left The left subframe should be presented first regardless of the setting of LRPOL.

Table 20. CHIP_SSS_CTRL 0x000A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD	DAP_MIX_LRSWAP	DAP_LRSWAP	DAC_LRSWAP	RSVD	I2S_LRSWAP	DAP_MIX_SELECT		DAP_SELECT		DAC_SELECT		RSVD		I2S_SELECT	

BITS	FIELD	RW	RESET	DEFINITION
15	RSVD	RW	0x0	Reserved
14	DAP_MIX_LRSWAP	RW	0x0	DAP Mixer Input Swap 0x0 = Normal Operation 0x1 = Left and Right channels for the DAP MIXER Input are swapped.
13	DAP_LRSWAP	RW	0x0	DAP Input Swap 0x0 = Normal Operation 0x1 = Left and Right channels for the DAP Input are swapped
12	DAC_LRSWAP	RW	0x0	DAC Input Swap 0x0 = Normal Operation 0x1 = Left and Right channels for the DAC are swapped
11	RSVD	RW	0x0	Reserved
10	I2S_LRSWAP	RW	0x0	I2S_DOUT Swap 0x0 = Normal Operation 0x1 = Left and Right channels for the I2S_DOUT are swapped
9:8	DAP_MIX_SELECT	RW	0x0	Select data source for DAP mixer 0x0 = ADC 0x1 = I2S_IN 0x2 = Reserved 0x3 = Reserved
7:6	DAP_SELECT	RW	0x0	Select data source for DAP 0x0 = ADC 0x1 = I2S_IN 0x2 = Reserved 0x3 = Reserved
5:4	DAC_SELECT	RW	0x1	Select data source for DAC 0x0 = ADC 0x1 = I2S_IN 0x2 = Reserved 0x3 = DAP
3:2	RSVD	RW	0x0	Reserved
1:0	I2S_SELECT	WO	0x0	Select data source for I2S_DOUT 0x0 = ADC 0x1 = I2S_IN 0x2 = Reserved 0x3 = DAP

Table 21. CHIP_ADCDAC_CTRL 0x000E

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD		VOL_BUSY_DAC_RIGHT	VOL_BUSY_DAC_LEFT	RSVD		VOL_RAMP_EN	VOL_EXPO_RAMP	RSVD				DAC_MUTE_RIGHT	DAC_MUTE_LEFT	ADC_HPF_FREEZE	ADC_HPF_BYPASS

BITS	FIELD	RW	RESET	DEFINITION
15:14	RSVD	RO	0x0	Reserved
13	VOL_BUSY_DAC_RIGHT	RO	0x0	Volume Busy DAC Right 0x0 = Ready 0x1 = Busy - This indicates the channel has not reached its programmed volume/mute level
12	VOL_BUSY_DAC_LEFT	RO	0x0	Volume Busy DAC Left 0x0 = Ready 0x1 = Busy - This indicates the channel has not reached its programmed volume/mute level
11:10	RSVD	RO	0x0	Reserved
9	VOL_RAMP_EN	RW	0x1	Volume Ramp Enable 0x0 = Disables volume ramp. New volume settings take immediate effect without a ramp 0x1 = Enables volume ramp This field affects DAC_VOL. The volume ramp effects both volume settings and mute. When set to 1 a soft mute is enabled.
8	VOL_EXPO_RAMP	RW	0x0	Exponential Volume Ramp Enable 0x0 = Linear ramp over top 4 volume octaves 0x1 = Exponential ramp over full volume range This bit only takes effect if *VOL_RAMP_EN* is 1.
7:4	RSVD	RW	0x0	Reserved
3	DAC_MUTE_RIGHT	RW	0x1	DAC Right Mute 0x0 = Unmute 0x1 = Muted If *VOL_RAMP_EN* = 1, this is a soft mute.
2	DAC_MUTE_LEFT	RW	0x1	DAC Left Mute 0x0 = Unmute 0x1 = Muted If *VOL_RAMP_EN* = 1, this is a soft mute.
1	ADC_HPF_FREEZE	RW	0x0	ADC High Pass Filter Freeze 0x0 = Normal operation 0x1 = Freeze the ADC high-pass filter offset register. The offset continues to be subtracted from the ADC data stream.
0	ADC_HPF_BYPASS	RW	0x0	ADC High Pass Filter Bypass 0x0 = Normal operation 0x1 = Bypassed and offset not updated

Table 22. CHIP_DAC_VOL 0x0010

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAC_VOL_RIGHT								DAC_VOL_LEFT							

BITS	FIELD	RW	RESET	DEFINITION
15:8	DAC_VOL_RIGHT	RW	0x3C	DAC Right Channel Volume Set the Right channel DAC volume with 0.5017 dB steps from 0 to -90 dB 0x3B and less = Reserved 0x3C = 0 dB 0x3D = -0.5 dB 0xF0 = -90 dB 0xFC and greater = Muted If *VOL_RAMP_EN* = 1, there is an automatic ramp to the new volume setting.
7:0	DAC_VOL_LEFT	RW	0x3C	DAC Left Channel Volume Set the Left channel DAC volume with 0.5017 dB steps from 0 to -90 dB 0x3B and less = Reserved 0x3C = 0 dB 0x3D = -0.5 dB 0xF0 = -90 dB 0xFC and greater = Muted If *VOL_RAMP_EN* = 1, there is an automatic ramp to the new volume setting.

Table 23. CHIP_PAD_STRENGTH 0x0014

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD						I2S_LRCLK		I2S_SCLK		I2S_DOUT		CTRL_DATA		CTRL_CLK	

BITS	FIELD	RW	RESET	DEFINITION
15:14	RSVD	RW	0x0	Reserved
9:8	I2S_LRCLK	RW	0x1	I^2S LRCLK Pad Drive Strength Sets drive strength for output pads per the table below. VDDIO 1.8 V 2.5 V 3.3 V 0x0 = Disable 0x1 = 1.66 mA 2.87 mA 4.02 mA 0x2 = 3.33 mA 5.74 mA 8.03 mA 0x3 = 4.99 mA 8.61 mA 12.05 mA
7:6	I2S_SCLK	RW	0x1	I^2S SCLK Pad Drive Strength Sets drive strength for output pads per the table below. VDDIO 1.8 V 2.5 V 3.3 V 0x0 = Disable 0x1 = 1.66 mA 2.87 mA 4.02 mA 0x2 = 3.33 mA 5.74 mA 8.03 mA 0x3 = 4.99 mA 8.61 mA 12.05 mA

BITS	FIELD	RW	RESET	DEFINITION
5:4	I2S_DOUT	RW	0x1	I²S DOUT Pad Drive Strength Sets drive strength for output pads per the table below. VDDIO 1.8 V 2.5 V 3.3 V 0x0 = Disable 0x1 = 1.66 mA 2.87 mA 4.02 mA 0x2 = 3.33 mA 5.74 mA 8.03 mA 0x3 = 4.99 mA 8.61 mA 12.05 mA
3:2	CTRL_DATA	RW	0x3	I²C DATA Pad Drive Strength Sets drive strength for output pads per the table below. VDDIO 1.8 V 2.5 V 3.3 V 0x0 = Disable 0x1 = 1.66 mA 2.87 mA 4.02 mA 0x2 = 3.33 mA 5.74 mA 8.03 mA 0x3 = 4.99 mA 8.61 mA 12.05 mA
1:0	CTRL_CLK	RW	0x3	I²C CLK Pad Drive Strength Sets drive strength for output pads per the table below. VDDIO 1.8 V 2.5 V 3.3 V 0x0 = Disable 0x1 = 1.66 mA 2.87 mA 4.02 mA 0x2 = 3.33 mA 5.74 mA 8.03 mA 0x3 = 4.99 mA 8.61 mA 12.05 mA

Table 24. CHIP_ANA_ADC_CTRL 0x0020

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD							ADC_VOL_M6DB	ADC_VOL_RIGHT				ADC_VOL_LEFT			

BITS	FIELD	RW	RESET	DEFINITION
15:9	RSVD	RO	0x0	Reserved
8	ADC_VOL_M6DB	RW	0x0	ADC Volume Range Reduction This bit shifts both right and left analog ADC volume range down by 6.0 dB. 0x0 = No change in ADC range 0x1 = ADC range reduced by 6.0 dB

BITS	FIELD	RW	RESET	DEFINITION
7:4	ADC_VOL_RIGHT	RW	0x0	ADC Right Channel Volume Right channel analog ADC volume control in 1.5.0 dB steps. 0x0 = 0 dB 0x1 = +1.5 dB ... 0xF = +22.5 dB This range is -6.0 dB to +16.5 dB if *ADC_VOL_M6DB* is set to 1.
3:0	ADC_VOL_LEFT	RW	0x0	ADC Left Channel Volume Left channel analog ADC volume control in 1.5 dB steps. 0x0 = 0 dB 0x1 = +1.5 dB ... 0xF = +22.5 dB This range is -6.0 dB to +16.5 dB if *ADC_VOL_M6DB* is set to 1.

Table 25. CHIP_ANA_HP_CTRL 0x0022

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD	HP_VOL_RIGHT							RSVD	HP_VOL_LEFT						

BITS	FIELD	RW	RESET	DEFINITION
15	RSVD	RO	0x0	Reserved
14:8	HP_VOL_RIGHT	RW	0x18	Headphone Right Channel Volume Right channel headphone volume control with 0.5 dB steps. 0x00 = +12 dB 0x01 = +11.5 dB 0x18 = 0 dB ... 0x7F = -51.5 dB
7	RSVD	RO	0x0	Reserved
6:0	HP_VOL_LEFT	RW	0x18	Headphone Left Channel Volume Left channel headphone volume control with 0.5 dB steps. 0x00 = +12 dB 0x01 = +11.5 dB 0x18 = 0 dB ... 0x7F = -51.5 dB

Table 26 is an analog control register that includes mutes, input selects, and zero-cross-detectors for the ADC, headphone, and LINEOUT.

Table 26. 7.0.0.11. CHIP_ANA_CTRL 0x0024

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD							MUTE_LO	RSVD	SELECT_HP	EN_ZCD_HP	MUTE_HP	RSVD	SELECT_ADC	EN_ZCD_ADC	MUTE_ADC

BITS	FIELD	RW	RESET	DEFINITION
15:9	RSVD	RO	0x0	Reserved
8	MUTE_LO	RW	0x1	LINEOUT Mute 0x0 = Unmute 0x1 = Mute
7	RSVD	RO	0x0	Reserved
6	SELECT_HP	RW	0x0	Select the headphone input. 0x0 = DAC 0x1 = LINEIN
5	EN_ZCD_HP	RW	0x0	Enable the headphone zero cross detector (ZCD) 0x0 = HP ZCD disabled 0x1 = HP ZCD enabled
4	MUTE_HP	RW	0x1	Mute the headphone outputs 0x0 = Unmute 0x1 = Mute
3	RSVD	RO	0x0	Reserved
2	SELECT_ADC	RW	0x0	Select the ADC input. 0x0 = Microphone 0x1 = LINEIN
1	EN_ZCD_ADC	RW	0x0	Enable the ADC analog zero cross detector (ZCD) 0x0 = ADC ZCD disabled 0x1 = ADC ZCD enabled
0	MUTE_ADC	RW	0x1	Mute the ADC analog volume 0x0 = Unmute 0x1 = Mute

The Table 27, CHIP_LINREG_CTRL 0x0026 register controls the VDDD linear regulator and the charge pump.

Table 27. CHIP_LINREG_CTRL 0x0026

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD									VDDC_MAN_ASSN	VDDC_ASSN_OVRD	RSVD	D_PROGRAMMING			

BITS	FIELD	RW	RESET	DEFINITION
15:7	RSVD	RO	0x0	Reserved
6	VDDC_MAN_ASSN	RW	0x0	Determines chargepump source when VDDC_ASSN_OVRD is set. 0x0 = VDDA 0x1 = VDDIO
5	VDDC_ASSN_OVRD	RW	0x0	Charge pump Source Assignment Override 0x0 = Charge pump source is automatically assigned based on higher of VDDA and VDDIO 0x1 = the source of charge pump is manually assigned by VDDC_MAN_ASSN If VDDIO and VDDA are both the same and greater than 3.1 V, VDDC_ASSN_OVRD and VDDC_MAN_ASSN should be used to manually assign VDDIO as the source for charge pump.
4	RSVD	RW	0x0	Reserved
3:0	D_PROGRAMMING	RW	0x0	Sets the VDDD linear regulator output voltage in 50 mV steps. Must clear the LINREG_SIMPLE_POWERUP and STARTUP_POWERUP bits in the 0x0030 register after power-up, for this setting to produce the proper VDDD voltage. 0x0 = 1.60 0xF = 0.85

The Table 28. CHIP_REF_CTRL 0x0028 register controls the bandgap reference bias voltage and currents.

Table 28. CHIP_REF_CTRL 0x0028

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD							VAG_VAL					BIAS_CTRL			SMALL_POP

BITS	FIELD	RW	RESET	DEFINITION
15:9	RSVD	RO	0x0	Reserved
8:4	VAG_VAL	RW	0x0	Analog Ground Voltage Control These bits control the analog ground voltage in 25 mV steps. This should usually be set to VDDA/2 or lower for best performance (maximum output swing at minimum THD). This VAG reference is also used for the DAC and ADC voltage reference. So changing this voltage scales the output swing of the DAC and the output signal of the ADC. 0x00 = 0.800 V 0x1F = 1.575 V

BITS	FIELD	RW	RESET	DEFINITION
3:1	BIAS_CTRL	RW	0x0	Bias control These bits adjust the bias currents for all of the analog blocks. By lowering the bias current a lower quiescent power is achieved. It should be noted that this mode can affect performance by 3-4 dB. 0x0 = Nominal 0x1-0x3=+12.5% 0x4=-12.5% 0x5=-25% 0x6=-37.5% 0x7=-50%
0	SMALL_POP	RW	0x0	VAG Ramp Control Setting this bit slows down the VAG ramp from ~200 to ~400 ms to reduce the startup pop, but increases the turn on/off time. 0x0 = Normal VAG ramp 0x1 = Slow down VAG ramp

The Table 29, CHIP_MIC_CTRL 0x002A register controls the microphone gain and the internal microphone biasing circuitry.

Table 29. CHIP_MIC_CTRL 0x002A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD						BIAS_RESISTOR		RSVD	BIAS_VOLT			RSVD		GAIN	

BITS	FIELD	RW	RESET	DEFINITION
15:10	RSVD	RO	0x0	Reserved
9:8	BIAS_RESISTOR	RW	0x0	MIC Bias Output Impedance Adjustment Controls an adjustable output impedance for the microphone bias. If this is set to zero the micbias block is powered off and the output is highZ. 0x0 = Powered off 0x1 = 2.0 kΩ 0x2 = 4.0 kΩ 0x3 = 8.0 kΩ
7	RSVD	RO	0x0	Reserved
6:4	BIAS_VOLT	RW	0x0	MIC Bias Voltage Adjustment Controls an adjustable bias voltage for the microphone bias amp in 250 mV steps. This bias voltage setting should be no more than VDDA-200 mV for adequate power supply rejection. 0x0 = 1.25 V ... 0x7 = 3.00 V
3:2	RSVD	RO	0x0	Reserved
1:0	GAIN	RW	0x0	MIC Amplifier Gain Sets the microphone amplifier gain. At 0 dB setting the THD can be slightly higher than other paths- typically around ~65 dB. At other gain settings the THD are better. 0x0 = 0 dB 0x1 = +20 dB 0x2 = +30 dB 0x3 = +40 dB

Table 30. CHIP_LINE_OUT_CTRL 0x002C

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD				OUT_CURRENT				RSVD		LO_VAGCNTRL					

BITS	FIELD	RW	RESET	DEFINITION
15:12	RSVD	RO	0x0	Reserved
11:8	OUT_CURRENT	RW	0x0	Controls the output bias current for the LINEOUT amplifiers. The nominal recommended setting for a 10 kΩ load with 1.0 nF load cap is 0x3. There are only 5 valid settings. 0x0=0.18 mA, 0x1=0.27 mA, 0x3=0.36 mA, 0x7=0.45 mA, 0xF=0.54 mA
7:6	RSVD	RO	0x0	Reserved
5:0	LO_VAGCNTRL	RW	0x0	LINEOUT Amplifier Analog Ground Voltage Controls the analog ground voltage for the LINEOUT amplifiers in 25 mV steps. This should usually be set to VDDIO/2. 0x00 = 0.800 V ... 0x1F = 1.575 V ... 0x23 = 1.675 V 0x24-0x3F are invalid

Table 31. CHIP_LINE_OUT_VOL 0x002E

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD			LO_VOL_RIGHT					RSVD			LO_VOL_LEFT				

BITS	FIELD	RW	RESET	DEFINITION
15:13	RSVD	RO	0x0	Reserved
12:8	LO_VOL_RIGHT	RW	0x4	LINEOUT Right Channel Volume Controls the right channel LINEOUT volume in 0.5 dB steps. Higher codes have more attenuation. See programming information for Left channel.
7:5	RSVD	RO	0x0	Reserved
4:0	LO_VOL_LEFT	RW	0x4	LINEOUT Left Channel Output Level The LO_VOL_LEFT is used to normalize the output level of the left line output to full scale based on the values used to set LINE_OUT_CTRL -> LO_VAGCNTRL and CHIP_REF_CTRL -> VAG_VAL. In general this field should be set to: $40*\log((VAG\_VAL)/(LO\_VAGCNTRL)) + 15$ Table 32 shows suggested values based on typical VDDIO and VDDA voltages. After setting to the nominal voltage, this field can be used to adjust the output level in +/-0.5 dB increments by using values higher or lower than the nominal setting.

Table 32. LINEOUT Output Level Values

VDDA	VAG_VAL	VDDIO	LO_VAGCNTRL	LO_VOL_*
1.8 V	0.9	3.3 V	1.55	0x06
1.8 V	0.9	1.8 V	0.9	0x0F
3.3 V	1.55	1.8 V	0.9	0x19
3.3 V	1.55	3.3 V	1.55	0x0F

The Table 33, CHIP_ANA_POWER 0x0030 register contains all of the power down controls for the analog blocks. The only other power-down controls are BIAS_RESISTOR in the MIC_CTRL register and the EN_ZCD control bits in ANA_CTRL.

Table 33. CHIP_ANA_POWER 0x0030

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD	DAC_MONO	LINREG_SIMPLE_POWERUP	STARTUP_POWERUP	VDDC_CHRGPMP_POWERUP	PLL_POWERUP	LINREG_D_POWERUP	VCOAMP_POWERUP	VAG_POWERUP	ADC_MONO	REFTOP_POWERUP	HEADPHONE_POWERUP	DAC_POWERUP	CAPLESS_HEADPHONE_POWERUP	ADC_POWERUP	LINEOUT_POWERUP

BITS	FIELD	RW	RESET	DEFINITION
15	RSVD	RW	0x0	Reserved
14	DAC_MONO	RW	0x1	While DAC_POWERUP is set, this allows the DAC to be put into left only mono operation for power savings. 0x0 = Mono (left only) 0x1 = Stereo
13	LINREG_SIMPLE_POWERUP	RW	0x1	Power up the simple (low power) digital supply regulator. After reset, this bit can be cleared IF VDDD is driven externally OR the primary digital linreg is enabled with LINREG_D_POWERUP 0x0 = Power down 0x1 = Power up
12	STARTUP_POWERUP	RW	0x1	Power up the circuitry needed during the power up ramp and reset. After reset this bit can be cleared if VDDD is coming from an external source. 0x0 = Power down 0x1 = Power up
11	VDDC_CHRGPMP_POWERUP	RW	0x0	Power up the VDDC charge pump block. If neither VDDA or VDDIO is 3.0 V or larger this bit should be cleared before analog blocks are powered up. 0x0 = Power down 0x1 = Power up Note that for charge pump to function, either the PLL must be powered on and programmed correctly (refer to CHIP_CLK_CTRL->MCLK_FREQ description) or the internal oscillator (set CLK_TOP_CTRL->ENABLE_INT_OSC) must be enabled
10	PLL_POWERUP	RW	0x0	PLL Power Up 0x0 = Power down 0x1 = Power up When cleared, the PLL is turned off. This must be set before CHIP_CLK_CTRL -> MCLK_FREQ is programmed to 0x3. The CHIP_PLL_CTRL register must be configured correctly before setting this bit.
9	LINREG_D_POWERUP	RW	0x0	Power up the primary VDDD linear regulator. 0x0 = Power down 0x1 = Power up

BITS	FIELD	RW	RESET	DEFINITION
8	VCOAMP_POWERUP	RW	0x0	Power up the PLL VCO amplifier. 0x0 = Power down 0x1 = Power up
7	VAG_POWERUP	RW	0x0	Power up the VAG reference buffer. Setting this bit starts the power up ramp for the headphone and LINEOUT. The headphone (and/or LINEOUT) powerup should be set BEFORE clearing this bit. When this bit is cleared the power-down ramp is started. The headphone (and/or LINEOUT) powerup should stay set until the VAG is fully ramped down (200 to 400 ms after clearing this bit). 0x0 = Power down 0x1 = Power up
6	ADC_MONO	RW	0x1	While ADC_POWERUP is set, this allows the ADC to be put into left only mono operation for power savings. This mode is useful when only using the microphone input. 0x0 = Mono (left only) 0x1 = Stereo
5	REFTOP_POWERUP	RW	0x1	Power up the reference bias currents 0x0 = Power down 0x1 = Power up This bit can be cleared when the part is a sleep state to minimize analog power.
4	HEADPHONE_POWERUP	RW	0x0	Power up the headphone amplifiers 0x0 = Power down 0x1 = Power up
3	DAC_POWERUP	RW	0x0	Power up the DACs 0x0 = Power down 0x1 = Power up
2	CAPLESS_HEADPHONE_POWERUP	RW	0x0	Power up the capless headphone mode 0x0 = Power down 0x1 = Power up
1	ADC_POWERUP	RW	0x0	Power up the ADCs 0x0 = Power down 0x1 = Power up
0	LINEOUT_POWERUP	RW	0x0	Power up the LINEOUT amplifiers 0x0 = Power down 0x1 = Power up

The Table 34, CHIP_PLL_CTRL 0x0032 register may only be changed after reset, and before PLL_POWERUP is set.

Table 34. CHIP_PLL_CTRL 0x0032

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INT_DIVISOR					FRAC_DIVISOR										

BITS	FIELD	RW	RESET	DEFINITION
15:11	INT_DIVISOR	RW	0xA	This is the integer portion of the PLL divisor. To determine the value of this field, use the following calculation: INT_DIVISOR = FLOOR(PLL_OUTPUT_FREQ/INPUT_FREQ) PLL_OUTPUT_FREQ = 180.6336 MHz if System sample rate = 44.1 kHz else PLL_OUTPUT_FREQ = 196.608 MHz if System sample rate!= 44.1 kHz INPUT_FREQ = Frequency of the external MCLK provided if CHIP_CLK_TOP_CTRL->INPUT_FREQ_DIV2 = 0x0 else INPUT_FREQ = (Frequency of the external MCLK provided/2) If CHIP_CLK_TOP_CTRL->INPUT_FREQ_DIV2 = 0x1
10:0	FRAC_DIVISOR	RW	0x0	This is the fractional portion of the PLL divisor. To determine the value of this field, use the following calculation: FRAC_DIVISOR = ((PLL_OUTPUT_FREQ/INPUT_FREQ) - INT_DIVISOR)*2048 PLL_OUTPUT_FREQ = 180.6336 MHz if System sample rate = 44.1 kHz else PLL_OUTPUT_FREQ = 196.608 MHz if System sample rate!= 44.1 kHz INPUT_FREQ = Frequency of the external MCLK provided if CHIP_CLK_TOP_CTRL->INPUT_FREQ_DIV2 = 0x0 else INPUT_FREQ = (Frequency of the external MCLK provided/2) If CHIP_CLK_TOP_CTRL->INPUT_FREQ_DIV2 = 0x1

Table 35, CHIP_CLK_TOP_CTRL 0x0034 has the miscellaneous controls for the clock block.

Table 35. CHIP_CLK_TOP_CTRL 0x0034

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD				ENABLE_INT_OSC	RSVD							INPUT_FREQ_DIV2	RSVD		

BITS	FIELD	RW	RESET	DEFINITION
15:12	RESERVED	RO	0x0	Reserved
11	ENABLE_INT_OSC	RW	0x0	Setting this bit enables an internal oscillator to be used for the zero cross detectors, the short detect recovery, and the charge pump. This allows the I^2S clock to be shut off while still operating an analog signal path. This bit can be kept on when the I^2S clock is enabled, but the I^2S clock is more accurate so it is preferred to clear this bit when I^2S is present.
10:4	RSVD	RW	0x0	Reserved

BITS	FIELD	RW	RESET	DEFINITION
3	INPUT_FREQ_DIV2	RW	0x0	SYS_MCLK divider before PLL input 0x0 = pass through 0x1 = SYS_MCLK is divided by 2 before entering PLL This must be set when the input clock is above 17 MHz. This has no effect when the PLL is powered down.
2:0	RSVD	RW	0x0	Reserved

Status bits for analog blocks are found in Table 36, CHIP_ANA_STATUS 0x0036

Table 36. CHIP_ANA_STATUS 0x0036

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD						LRSHORT_STS	CSHORT_STS	RSVD			PLL_IS_LOCKED	RSVD			

BITS	FIELD	RW	RESET	DEFINITION
15:10	RSVD	RO	0x0	Reserved
9	LRSHORT_STS	RO	0x0	This bit is high whenever a short is detected on the left or right channel headphone drivers. 0x0 = Normal 0x1 = Short detected
8	CSHORT_STS	RO	0x0	This bit is high whenever a short is detected on the capless headphone common/ center channel driver. 0x0 = Normal 0x1 = Short detected
7:5	RSVD	RO	0x0	Reserved
4	PLL_IS_LOCKED	RO	0x0	This bit goes high after the PLL is locked. 0x0 = PLL is not locked 0x1 = PLL is locked
3:0	RSVD	RO	0x0	Reserved

Table 37, CHIP_ANA_TEST1 0x0038 and Table 38, CHIP_ANA_TEST2 0x003A register controls are intended only for debug.

Table 37. CHIP_ANA_TEST1 0x0038

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HP_IALL_ADJ		HP_I1_ADJ		HP_ANTIPOP			HP_CLASSAB	HP_HOLD_GND_CENTER	HP_HOLD_GND	VAG_DOUB_CURRENT	VAG_CLASSA	TM_ADCIN_TOHP	TM_HPCOMMON	TM_SELECT_MIC	TESTMODE

BITS	FIELD	RW	RESET	DEFINITION
15:14	HP_IALL_ADJ	RW	0x0	These bits control the overall bias current of the headphone amplifier (all stages including first and output stage). 0x0=nominal, 0x1=-50%, 0x2=+50%, 0x3=-40%
13:12	HP_I1_ADJ	RW	0x0	These bits control the bias current for the first stage of the headphone amplifier. 0x0=nominal, 0x1=-50%, 0x2=+100%, 0x3=+50%
11:9	HP_ANTIPOP	RW	0x0	These bits control the headphone output current in classA mode and also the pull-down strength while powering off. These bits normally are not needed.
8	HP_CLASSAB	RW	0x1	This defaults high. When this bit is high the headphone is in classAB mode. ClassA mode would normally not be used.
7	HP_HOLD_GND_CENTER	RW	0x1	This defaults high. When this bit is high and the capless headphone center channel is powered off, the output is tied to ground. This is the preferred mode of operation for best antipop performance.
6	HP_HOLD_GND	RW	0x1	This defaults high. When this bit is high and the headphone is powered off, the output is tied to ground. This is the preferred mode of operation for best antipop performance.
5	VAG_DOUB_CURRENT	RW	0x0	Double the VAG output current when in classA mode.
4	VAG_CLASSA	RW	0x0	Turn off the classAB output current for the VAG buffer. The classA current is limited so this may cause clipping in some modes.
3	TM_ADCIN_TOHP	RW	0x0	Put ADCmux output onto the headphone output pin. Must remove headphone load and any external headphone compensation for this mode.
2	TM_HPCOMMON	RW	0x0	Enable headphone common to be used in ADCmux for testing
1	TM_SELECT_MIC	RW	0x0	Enable the mic-adc-dac-HP path
0	TESTMODE	RW	0x0	Enable the analog test mode paths

Table 38. CHIP_ANA_TEST2 0x003A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD	LINEOUT_TO_VDDA	SPARE	MONOMODE_DAC	VCO_TUNE_AGAIN	LO_PASS_MASTERVAG	INVERT_DAC_SAMPLE_CLOCK	INVERT_DAC_DATA_TIMING	DAC_EXTEND_RTZ	DAC_DOUBLE_I	DAC_DIS_RTZ	DAC_CLASSA	INVERT_ADC_SAMPLE_CLOCK	INVERT_ADC_DATA_TIMING	ADC_LESSI	ADC_DITHEROFF

BITS	FIELD	RW	RESET	DEFINITION
15	RSVD	RO	0x0	Reserved
14	LINEOUT_TO_VDDA	RW	0x0	Changes the LINEOUT amplifier power supply from VDDIO to VDDA. Typically LINEOUT should be on the higher power supply. This bit is useful when VDDA is ~3.3 V and VDDIO is ~1.8 V.
13	SPARE	RW	0x0	Spare registers to analog.
12	MONOMODE_DAC	RW	0x0	Copy the left channel DAC data to the right channel. This allows both left and right to play from MONO dac data.
11	VCO_TUNE_AGAIN	RW	0x0	When toggled high then low forces the PLL VCO to retune the number of inverters in the ring oscillator loop.

BITS	FIELD	RW	RESET	DEFINITION
10	LO_PASS_MASTERVAG	RW	0x0	Tie the main analog VAG to the LINEOUT VAG. This can improve SNR for the LINEOUT when both are the same voltage.
9	INVERT_DAC_SAMPLE_CLOCK	RW	0x0	Change the clock edge used for the DAC output sampling.
8	INVERT_DAC_DATA_TIMING	RW	0x0	Change the clock edge used for the digital to analog DAC data crossing.
7	DAC_EXTEND_RTZ	RW	0x0	Extend the return-to-zero time for the DAC.
6	DAC_DOUBLE_I	RW	0x0	Double the output current of the DAC amplifier when it is in classA mode.
5	DAC_DIS_RTZ	RW	0x0	Turn off the return-to-zero in the DAC. In mode cases, this hurts the SNDR of the DAC.
4	DAC_CLASSA	RW	0x0	Turn off the classAB mode in the DAC amplifier. This mode should normally not be used. The output current is not high enough to support a full scale signal in this mode.
3	INVERT_ADC_SAMPLE_CLOCK	RW	0x0	Change the clock edge used for the ADC sampling.
2	INVERT_ADC_DATA_TIMING	RW	0x0	Change the clock edge used for the analog to digital ADC data crossing
1	ADC_LESSI	RW	0x0	Drops ADC bias currents by 20%
0	ADC_DITHEROFF	RW	0x0	Turns off the ADC dithering.

The Table 39, CHIP_SHORT_CTRL 0x003C register contains controls for the headphone short detectors.

Table 39. CHIP_SHORT_CTRL 0x003C

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD	LVLADJR			RSVD	LVLADJL			RSVD	LVLADJC			MODE_LR		MODE_CM	

BITS	FIELD	RW	RESET	DEFINITION
15	RSVD	RO	0x0	Reserved
14:12	LVLADJR	RW	0x0	These bits adjust the sensitivity of the right channel headphone short detector in 25 mA steps.This trip point can vary by ~30% over process so leave plenty of guard band to avoid false trips. This short detect trip point is also effected by the bias current adjustments made by CHIP_REF_CTRL -> BIAS_CTRL and by CHIP_ANA_TEST1 -> HP_IALL_ADJ. 0x3=25 mA 0x2=50 mA 0x1=75 mA 0x0=100 mA 0x4=125 mA 0x5=150 mA 0x6=175 mA 0x7=200 mA
11	RSVD	RO	0x0	Reserved

BITS	FIELD	RW	RESET	DEFINITION
10:8	LVLADJL	RW	0x0	These bits adjust the sensitivity of the left channel headphone short detector in 25 mA steps.This trip point can vary by ~30% over process so leave plenty of guard band to avoid false trips. This short detect trip point is also effected by the bias current adjustments made by CHIP_REF_CTRL -> BIAS_CTRL and by CHIP_ANA_TEST1 -> HP_IALL_ADJ. 0x3=25 mA 0x2=50 mA 0x1=75 mA 0x0=100 mA 0x4=125 mA 0x5=150 mA 0x6=175 mA 0x7=200 mA
7	RSVD	RO	0x0	Reserved
6:4	LVLADJC	RW	0x0	These bits adjust the sensitivity of the capless headphone center channel short detector in 50 mA steps. This trip point can vary by ~30% over process so leave plenty of guard band to avoid false trips. This short detect trip point is also effected by the bias current adjustments CHIP_REF_CTRL -> BIAS_CTRL and by CHIP_ANA_TEST1 -> HP_IALL_ADJ. 0x3=50 mA 0x2=100 mA 0x1=150 mA 0x0=200 mA 0x4=250 mA 0x5=300 mA 0x6=350 mA 0x7=400 mA
3:2	MODE_LR	RW	0x0	These bits control the behavior of the short detector for the capless headphone central channel driver. This mode should be set prior to powering up the headphone amplifier. When a short is detected the amplifier output switches to classA mode internally to avoid excessive currents. 0x0 = Disable short detector, reset short detect latch, software view non-latched short signal 0x1 = Enable short detector and reset the latch at timeout (every ~50 ms) 0x2 = This mode is not used/invalid 0x3 = Enable short detector with only manual reset (have to return to 0x0 to reset the latch)
1:0	MODE_CM	RW	0x0	These bits control the behavior of the short detector for the capless headphone central channel driver. This mode should be set prior to powering up the headphone amplifier. When a short is detected the amplifier output switches to classA mode interally to avoid excessive currents. 0x0 = Disable short detector, reset short detect latch, software view non-latched short signal 0x1 = Enable short detector and reset the latch at timeout (every ~50 ms) 0x2 = Enable short detector and auto reset when output voltage rises (preferred mode) 0x3 = Enable short detector with only manual reset (have to return to 0x0 to reset the latch)

Table 40. DAP_CONTROL 0x0100

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD											MIX_EN	RSVD			DAP_EN

BITS	FIELD	RW	RESET	DEFINITION
15:5	RSVD	RO	0x0	Reserved
4	MIX_EN	RW	0x0	Enable/Disable the DAP mixer path 0x0 = Disable 0x1 = Enable When enabled, DAP_EN must also be enabled to use the mixer.
3:1	RSVD	RO	0x0	Reserved
0	DAP_EN	RW	0x0	Enable/Disable digital audio processing (DAP) 0x0 = Disable. When disabled, no audio passes through. 0x1 = Enable. When enabled, audio can pass through DAP even if none of the DAP functions are enabled.

Table 41. DAP_PEQ 0x0102

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD													EN		

BITS	FIELD	RW	RESET	DEFINITION
15:3	RSVD	RO	0x0	Reserved
2:0	EN	RW	0x0	Set to Enable the PEQ filters 0x0 = Disabled 0x1 = 1 Filter Enabled 0x2 = 2 Filters Enabled ..... 0x7 = Cascaded 7 Filters DAP_AUDIO_EQ->EN bit must be set to 1 in order to enable the PEQ

Table 42. DAP_BASS_ENHANCE 0x0104

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD							BYPASS_HPF	RSVD	CUTOFF			RSVD			EN

BITS	FIELD	RW	RESET	DEFINITION
15:9	RSVD	RO	0x0	Reserved
8	BYPASS_HPF	RW	0x0	Bypass high pass filter 0x0 = Enable high pass filter 0x1 = Bypass high pass filter
7	RSVD	RO	0x0	Reserved

BITS	FIELD	RW	RESET	DEFINITION
6:4	CUTOFF	RW	0x4	Set cut-off frequency 0x0 = 80 Hz 0x1 = 100 Hz 0x2 = 125 Hz 0x3 = 150 Hz 0x4 = 175 Hz 0x5 = 200 Hz 0x6 = 225 Hz
3:1	RSVD	RO	0x0	Reserved
0	EN	RW	0x0	Enable/Disable Bass Enhance 0x0 = Disable 0x1 = Enable

Table 43. DAP_BASS_ENHANCE_CTRL 0x0106

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD		LR_LEVEL						RSVD	BASS_LEVEL						

BITS	FIELD	RW	RESET	DEFINITION
15:14	RSVD	RO	0x0	Reserved
13:8	LR_LEVEL	RW	0x5	Left/Right Mix Level Control 0x00= +6.0 dB for Main Channel ..... 0x3F= Least L/R Channel Level
7	RSVD	RO	0x0	
6:0	BASS_LEVEL	RW	0x1f	Bass Harmonic Level Control 0x00= Most Harmonic Boost ..... 0x7F=Least Harmonic Boost

Table 44. DAP_AUDIO_EQ 0x0108

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD														EN	

BITS	FIELD	RW	RESET	DEFINITION
15:2	RSVD	RO	0x0	Reserved
1:0	EN	RW	0x0	Selects between PEQ/GEQ/Tone Control and Enables it. 0x0 = Disabled. 0x1 = Enable PEQ. NOTE: DAP_PEQ->EN bit must also be set to the desired number of filters (bands) in order for the PEQ to be enabled. 0x2 = Enable Tone Control 0x3 = Enable 5 Band GEQ

Table 45. DAP_SGTL_SURROUND 0x010A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD									WIDTH_CONTROL			RSVD		SELECT	

BITS	FIELD	RW	RESET	DEFINITION
15:7	RSVD	RO	0x0	Reserved
6:4	WIDTH_CONTROL	RW	0x4	Freescale Surround Width Control - The width control changes the perceived width of the sound field. 0x0 = Least Width ..... 0x7 = Most Width
3:2	RSVD	RO	0x0	Reserved
1:0	SELECT	RW	0x0	Freescale Surround Selection 0x0 = Disabled 0x1 = Disabled 0x2 = Mono input Enable 0x3 = Stereo input Enable

Table 46. DAP_FILTER_COEF_ACCESS 0x010C

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD							WR	INDEX							

BITS	FIELD	RW	RESET	DEFINITION
15:9	RSVD	RO	0x0	Reserved
8	WR	WO	0x0	When set, the coefficients written in the ten coefficient data registers are loaded into the filter specified by INDEX
7:0	INDEX	RW	0x0	Specifies the index for each of the seven bands of the filter coefficient that needs to be written to. Each filter has 5 coefficients that need to be loaded into the 10 coefficient registers (MSB, LSB) before setting the index and WR bit. Steps to write coefficients: 1. Write the five 20-bit coefficient values to DAP_COEF_WR_XX_MSB and DAP_COEF_WR_XX_LSB registers (XX= B0,B1,B2,A1,A2) 2. Set INDEX of the coefficient from the table below. 3. Set the WR bit to load the coefficient. NOTE: Steps 2 and 3 can be performed with a single write to DAP_FILTER_COEF_ACCESS register. Coefficient address: Band 0 = 0x00 Band 1 = 0x01 Band 2 = 0x02 Band 3 = 0x03 Band 4 = 0x04 ... Band 7 = 0x06

Table 47. DAP_COEF_WR_B0_MSB 0x010E

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIT_19	BIT_18	BIT_17	BIT_16	BIT_15	BIT_14	BIT_13	BIT_12	BIT_11	BIT_10	BIT_9	BIT_8	BIT_7	BIT_6	BIT_5	BIT_4

BITS	FIELD	RW	RESET	DEFINITION
15	BIT_19	WO	0x0	Most significant 16-bits of the 20-bit filter coefficient that needs to be written
14	BIT_18	WO	0x0	
13	BIT_17	WO	0x0	
12	BIT_16	WO	0x0	
11	BIT_15	WO	0x0	
10	BIT_14	WO	0x0	
9	BIT_13	WO	0x0	
8	BIT_12	WO	0x0	
7	BIT_11	WO	0x0	
6	BIT_10	WO	0x0	
5	BIT_9	WO	0x0	
4	BIT_8	WO	0x0	
3	BIT_7	WO	0x0	
2	BIT_6	WO	0x0	
1	BIT_5	WO	0x0	
0	BIT_4	WO	0x0	

Table 48. DAP_COEF_WR_B0_LSB 0x0110

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD												BIT_3	BIT_2	BIT_1	BIT_0

BITS	FIELD	RW	RESET	DEFINITION
15:4	RSVD	RO	0x0	
3	BIT_3	WO	0x0	
2	BIT_2	WO	0x0	
1	BIT_1	WO	0x0	
0	BIT_0	WO	0x0	Least significant 4 bits of the 20-bit filter coefficient that needs to be written.

Table 49. DAP_AUDIO_EQ_BASS_BAND0 0x0116 115 Hz

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD									VOLUME						

BITS	FIELD	RW	RESET	DEFINITION
15:7	RSVD	RO	0x0	Reserved
6:0	VOLUME	RW	0x2F	Sets Tone Control Bass/GEQ Band0 0x5F = sets to 12 dB 0x2F = sets to 0 dB 0x00 = sets to -11.75 dB Each LSB is 0.25 dB

Table 50. DAP_AUDIO_EQ_BAND1 0x0118 330 Hz

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD									VOLUME						

BITS	FIELD	RW	RESET	DEFINITION
15:7	RSVD	RO	0x0	Reserved
6:0	VOLUME	RW	0x2F	Sets GEQ Band1 0x5F = sets to 12 dB 0x2F = sets to 0 dB 0x00 = sets to -11.75 dB Each LSB is 0.25 dB

Table 51. DAP_AUDIO_EQ_BAND2 0x011A 990 Hz

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD									VOLUME						

BITS	FIELD	RW	RESET	DEFINITION
15:7	RSVD	RO	0x0	Reserved
6:0	VOLUME	RW	0x2F	Sets GEQ Band2 0x5F = sets to 12 dB 0x2F = sets to 0 dB 0x00 = sets to -11.75 dB Each LSB is 0.25 dB

Table 52. DAP_AUDIO_EQ_BAND3 0x011C 3000 Hz

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD									VOLUME						

BITS	FIELD	RW	RESET	DEFINITION
15:7	RSVD	RO	0x0	Reserved
6:0	VOLUME	RW	0x2F	Sets GEQ Band3 0x5F = sets to 12 dB 0x2F = sets to 0 dB 0x00 = sets to -11.75 dB Each LSB is 0.25 dB

Table 53. DAP_AUDIO_EQ_TREBLE_BAND4 0x011E 9900 Hz

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD									VOLUME						

BITS	FIELD	RW	RESET	DEFINITION
15:7	RSVD	RO	0x0	Reserved
6:0	VOLUME	RW	0x2F	Sets Tone Control Treble/GEQ Band4 0x5F = sets to 12 dB 0x2F = sets to 0 dB 0x00 = sets to -11.75 dB Each LSB is 0.25 dB

Table 54, DAP_MAIN_CHAN 0x0120 sets the main channel volume level

Table 54. DAP_MAIN_CHAN 0x0120

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VOL															

BITS	FIELD	RW	RESET	DEFINITION
15:0	VOL	RW	0x8000	DAP Main Channel Volume 0xFFFF = 200% 0x8000 (default) = 100% 0x0000 = 0%

Table 55, DAP_MIX_CHAN 0x0122 sets the mix channel volume level

Table 55. DAP_MIX_CHAN 0x0122

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VOL															

BITS	FIELD	RW	RESET	DEFINITION
15:0	VOL	RW	0x0000	DAP Mix Channel Volume 0xFFFF = 200% 0x8000 = 100% 0x0000 (default) = 0%

Table 56. DAP_AVC_CTRL 0x0124

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD	RSVD	MAX_GAIN		RSVD		LBI_RESPONSE		RSVD		HARD_LIMIT_EN	RSVD				EN

BITS	FIELD	RW	RESET	DEFINITION
15	RSVD	RO	0x0	Reserved
14	RSVD	RW	0x1	Reserved.
13:12	MAX_GAIN	RW	0x1	Maximum gain that can be applied by the AVC in expander mode. 0x0 = 0 dB gain 0x1 = 6.0 dB of gain 0x2 = 12 dB of gain
11:10	RSVD	RO	0x0	Reserved
9:8	LBI_RESPONSE	RW	0x1	Integrator Response 0x0 = 0 mS LBI 0x1 = 25 mS LBI 0x2 = 50 mS LBI 0x3 = 100 mS LBI
7:6	RSVD	RO	0x0	Reserved
5	HARD_LIMIT_EN	RW	0x0	Enable Hard Limiter Mode 0x0 = Hard limit disabled. AVC Compressor/Expander is enabled. 0x1 = Hard limit enabled. The signal is limited to the programmed threshold. (Signal saturates at the threshold)
4:1	RSVD	RO	0x0	Reserved
0	EN	RW	0x0	Enable/disable AVC 0x0 = Disable 0x1 = Enable

Table 57. DAP_AVC_THRESHOLD 0x0126

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
THRESH															

BITS	FIELD	RW	RESET	DEFINITION
15:0	THRESH	RW	0x1473	AVC Threshold Value Threshold is programmable. Use the following formula to calculate hex value: Hex Value = ((10^(THRESHOLD_dB/20))*0.636)*2^15 Threshold can be set in the range of 0 dB to -96 dB Example Values: 0x1473 = Set Threshold to -12 dB 0x0A40 = Set Threshold to -18 dB

Table 58. DAP_AVC_ATTACK 0x0128

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD				RATE											

BITS	FIELD	RW	RESET	DEFINITION
15:12	RSVD	RO	0x0	Reserved
11:0	RATE	RW	0x28	AVC Attack Rate This is the rate at which the AVC applies attenuation to the signal to bring it to the threshold level. AVC Attack Rate is programmable. To use a custom rate, use the formula below to convert from dB/S to hex value: Hex Value = (1 - (10^(-(Rate_dBs/(20*SYS_FS)))) * 2^19 where, SYS_FS is the system sample rate configured in CHIP_CLK_CTRL register. Example values: 0x28 = 32 dB/s 0x10 = 8.0 dB/s 0x05 = 4.0 dB/s 0x03 = 2.0 dB/s

Table 59. DAP_AVC_DECAY 0x012A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD				RATE											

BITS	FIELD	RW	RESET	DEFINITION
15:12	RSVD	RO	0x0	Reserved
11:0	RATE	RW	0x50	AVC Decay Rate This is the rate at which the AVC releases the attenuation previously applied to the signal during attack. AVC Decay Rate is programmable. To use a custom rate, use the formula below to convert from dB/S to hex value: Hex Value = (1 - (10^(-(Rate_dBs/(20*SYS_FS)))) * 2^23 where, SYS_FS is the system sample rate configured in CHIP_CLK_CTRL register. Example values: 0x284 = 32 dB/s 0xA0 = 8.0 dB/s 0x50 = 4.0 dB/s 0x28 = 2.0 dB/s

Table 60. DAP_COEF_WR_B1_MSB 0x012C

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSB															

BITS	FIELD	RW	RESET	DEFINITION
15:0	MSB	RW	0x0	Most significant 16-bits of the 20-bit filter coefficient that needs to be written

Table 61. DAP_COEF_WR_B1_LSB 0x012E

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD												LSB			

BITS	FIELD	RW	RESET	DEFINITION
15:4	RSVD	RO	0x0	Reserved
3:0	LSB	RW	0x0	Least significant 4 bits of the 20-bit filter coefficient that needs to be written.

Table 62. DAP_COEF_WR_B2_MSB 0x0130

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSB															

BITS	FIELD	RW	RESET	DEFINITION
15:0	MSB	RW	0x0	Most significant 16-bits of the 20-bit filter coefficient that needs to be written

Table 63. DAP_COEF_WR_B2_LSB 0x0132

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD												LSB			

BITS	FIELD	RW	RESET	DEFINITION
15:4	RSVD	RO	0x0	Reserved
3:0	LSB	RW	0x0	Least significant 4 bits of the 20-bit filter coefficient that needs to be written.

Table 64. DAP_COEF_WR_A1_MSB 0x0134

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSB															

BITS	FIELD	RW	RESET	DEFINITION
15:0	MSB	RW	0x0	Most significant 16-bits of the 20-bit filter coefficient that needs to be written

Table 65. DAP_COEF_WR_A1_LSB 0x0136

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD												LSB			

BITS	FIELD	RW	RESET	DEFINITION
15:4	RSVD	RO	0x0	Reserved
3:0	LSB	RW	0x0	Least significant 4 bits of the 20-bit filter coefficient that needs to be written.

Table 66. DAP_COEF_WR_A2_MSB 0x0138

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSB															

BITS	FIELD	RW	RESET	DEFINITION
15:0	MSB	RW	0x0	Most significant 16-bits of the 20-bit filter coefficient that needs to be written

Table 67. DAP_COEF_WR_A2_LSB 0x013A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD												LSB			

BITS	FIELD	RW	RESET	DEFINITION
15:4	RSVD	RO	0x0	Reserved
3:0	LSB	RW	0x0	Least significant 4 bits of the 20-bit filter coefficient that needs to be written.