

PSoC® Creator™ Project Datasheet for alios_small

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1 Overview

PSoC 4200S family is one of the smaller members of the PSoC 4 family of devices and is upward compatible with larger members of PSoC 4.

- High-performance, 32-bit single cycle Cortex-M0 CPU core
- Capacitive touch sensing (CapSense®)
- Configurable Timer/Counter/PWM block
- Two current sourcing/sinking DACs (IDACs)
- Comparator with 1.2 V reference
- Configurable I2C block with master, slave, and multi-master operating modes
- Low-power operating modes including Sleep and Deep-Sleep

Figure 1 shows the major components of a typical <u>PSoC 4100S Plus</u> series member PSoC 4 device. For details on all the systems listed above, please refer to the <u>PSoC 4 Technical Reference Manual</u>.

Figure 1. PSoC 4100S Plus Device Series Block Diagram

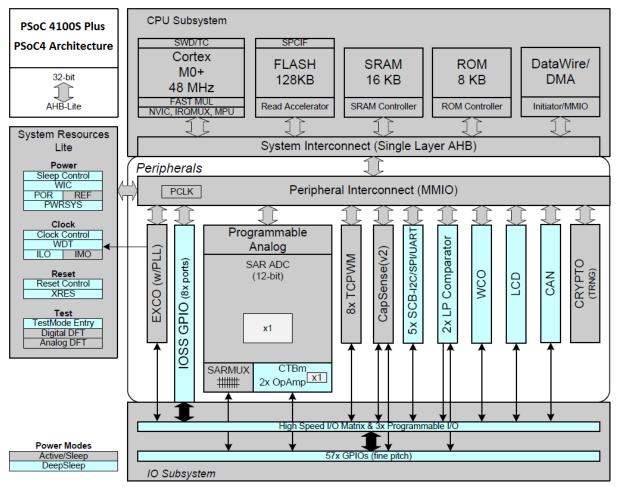




Table 1 lists the key characteristics of this device.

Table 1. Device Characteristics

Name	Value
Part Number	CY8C4147AZI-S445
Package Name	64-TQFP
Family	PSoC 4
Series	PSoC 4100S Plus
Max CPU speed (MHz)	48
Flash size (kB)	128
SRAM size (kB)	16
Vdd range (V)	1.71 to 5.5
Automotive qualified	No (Industrial Grade Only)
Temp range (Celsius)	-40 to 85

NOTE: The CPU speed noted above is the maximum available speed. The CPU is clocked by HFCLK, listed in the <u>System Clocks</u> section below.

Table 2 lists the device resources that this design uses:

Table 2. Device Resources

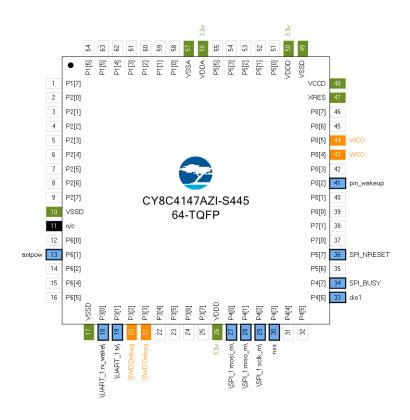
Resource Type	Used	Free	Max	% Used
Interrupts	4	24	28	14.29 %
IO	15	39	54	27.78 %
Segment LCD	0	1	1	0.00 %
CapSense	0	1	1	0.00 %
Die Temp	0	1	1	0.00 %
Serial Communication (SCB)	2	3	5	40.00 %
DMA Channels	0	8	8	0.00 %
Timer/Counter/PWM	0	8	8	0.00 %
Crypto	0	1	1	0.00 %
Smart IO Ports	0	3	3	0.00 %
Comparator/Opamp	0	2	2	0.00 %
Comparator	0	1	1	0.00 %
LP Comparator	0	2	2	0.00 %
SAR ADC	0	1	1	0.00 %
DAC				
7-bit IDAC	0	2	2	0.00 %



2 Pins

Figure 2 shows the pin layout of this device.

Figure 2. Device Pin Layout





2.1 Hardware Pins

Table 3 contains information about the pins on this device in device pin order. (No connection ["n/c"] pins have been omitted.)

Table 3. Device Pins

Pin	Port	Name	Туре	Drive Mode
1	P1[7]	GPIO [unused]	71	
2	P2[0]	GPIO [unused]		
3	P2[1]	GPIO [unused]		
4	P2[2]	GPIO [unused]		
5	P2[3]	GPIO [unused]		
6	P2[4]	GPIO [unused]	1	
7	P2[5]	GPIO [unused]		
8	P2[6]	GPIO [unused]	+	
9	P2[7]	GPIO [unused]	+	
10	VSSD	VSSD	Power	
12	P6[0]	GPIO [unused]	1 OWCI	
13	P6[1]	antpow	Software In/Out	Strong drive
14	P6[2]	GPIO [unused]		
15	P6[4]	GPIO [unused]		
16	P6[5]	GPIO [unused]	1	
17	VSSD	VSSD	Power	
18	P3[0]	\UART 1:rx wake\	Dgtl In	HiZ digital
19	P3[1]	\UART 1:tx\	Dgtl Out	Strong drive
20	P3[2]	Debug:SWD IO	Reserved	
21	P3[3]	Debug:SWD_CK	Reserved	
22	P3[4]	GPIO [unused]		
23	P3[5]	GPIO [unused]		
24	P3[6]	GPIO [unused]		
25	P3[7]	GPIO [unused]		
26	VDDD	VDDD	Power	
27	P4[0]	\SPI 1:mosi m\	Dgtl Out	Strong drive
28	P4[1]	\SPI 1:miso m\	Dgtl In	HiZ digital
29	P4[2]	\SPI 1:sclk m\	Dgtl Out	Strong drive
30	P4[3]	nss	Software	Strong drive
	1		In/Out	
31	P4[4]	GPIO [unused]		
32	P4[5]	GPIO [unused]		
33	P4[6]	dio1	Software	Res pull
			In/Out	down
34	P4[7]	SPI_BUSY	Software In/Out	HiZ digital
35	P5[6]	GPIO [unused]		
36	P5[7]	SPI_NRESET	Software In/Out	Strong drive
37	P7[0]	GPIO [unused]		
38	P7[1]	GPIO [unused]		
39	P0[0]	GPIO [unused]		
40	P0[1]	GPIO [unused]		
41	P0[2]	pin_wakeup	Software In/Out	Res pull down



Pin	Port	Name	Type	Drive Mode
42	P0[3]	GPIO [unused]		
43	P0[4]	XTAL 32kHz:Xi	Reserved	
44	P0[5]	XTAL 32kHz:Xo	Reserved	
45	P0[6]	GPIO [unused]		
46	P0[7]	GPIO [unused]		
47	XRES	XRES	Dedicated	
48	VCCD	VCCD	Power	
49	VSSD	VSSD	Power	
50	VDDD	VDDD	Power	
51	P5[0]	GPIO [unused]		
52	P5[1]	GPIO [unused]		
53	P5[2]	GPIO [unused]		
54	P5[3]	GPIO [unused]		
55	P5[5]	GPIO [unused]		
56	VDDA	VDDA	Power	
57	VSSA	VSSA	Power	
58	P1[0]	GPIO [unused]		
59	P1[1]	GPIO [unused]		
60	P1[2]	GPIO [unused]		
61	P1[3]	GPIO [unused]		
62	P1[4]	GPIO [unused]		
63	P1[5]	GPIO [unused]		
64	P1[6]	GPIO [unused]		

Abbreviations used in Table 3 have the following meanings:

- Dgtl In = Digital Input
- HiZ digital = High impedance digital
- Dgtl Out = Digital Output
- Res pull down = Resistive pull down



2.2 Hardware Ports

Table 4 contains information about the pins on this device in device port order. (No connection ["n/c"], power and dedicated pins have been omitted.)

Table 4. Device Ports

Port	Pin	Name	Туре	Drive Mode
P0[0]	39	GPIO [unused]		
P0[1]	40	GPIO [unused]		
P0[2]	41	pin_wakeup	Software In/Out	Res pull down
P0[3]	42	GPIO [unused]	III/Out	down
P0[4]	43	XTAL 32kHz:Xi	Reserved	
P0[5]	44	XTAL 32kHz:Xo	Reserved	
P0[6]	45	GPIO [unused]		
P0[7]	46	GPIO [unused]		
P1[0]	58	GPIO [unused]		
P1[1]	59	GPIO [unused]		
P1[2]	60	GPIO [unused]		
P1[3]	61	GPIO [unused]		
P1[4]	62	GPIO [unused]		
P1[5]	63	GPIO [unused]		
P1[6]	64	GPIO [unused]		
P1[7]	1	GPIO [unused]		
P2[0]	2	GPIO [unused]		
P2[1]	3	GPIO [unused]		
P2[2]	4	GPIO [unused]		
P2[3]	5	GPIO [unused]		
P2[4]	6	GPIO [unused]		
P2[5]	7	GPIO [unused]		
P2[6]	8	GPIO [unused]		
P2[7]	9	GPIO [unused]	Dettile	LII7 distitat
P3[0]	18	\UART_1:rx_wake\	Dgtl In	HiZ digital
P3[1]	19 20	\UART_1:tx\	Dgtl Out Reserved	Strong drive
P3[2]	21	Debug:SWD_IO Debug:SWD_CK	Reserved	
P3[3] P3[4]	22	GPIO [unused]	Reserved	
P3[5]	23	GPIO [unused]		
P3[6]	24	GPIO [unused]		
P3[7]	25	GPIO [unused]		
P4[0]	27	\SPI 1:mosi m\	Dgtl Out	Strong drive
P4[1]	28	\SPI 1:miso m\	Dgtl In	HiZ digital
P4[2]	29	\SPI 1:sclk m\	Dgtl Out	Strong drive
P4[3]	30	nss	Software	Strong drive
			In/Out	
P4[4]	31	GPIO [unused]		
P4[5]	32	GPIO [unused]		
P4[6]	33	dio1	Software In/Out	Res pull down
P4[7]	34	SPI_BUSY	Software In/Out	HiZ digital
P5[0]	51	GPIO [unused]		
P5[1]	52	GPIO [unused]		



Port	Pin	Name	Type	Drive Mode
P5[2]	53	GPIO [unused]		
P5[3]	54	GPIO [unused]		
P5[5]	55	GPIO [unused]		
P5[6]	35	GPIO [unused]		
P5[7]	36	SPI_NRESET	Software In/Out	Strong drive
P6[0]	12	GPIO [unused]		
P6[1]	13	antpow	Software In/Out	Strong drive
P6[2]	14	GPIO [unused]		
P6[4]	15	GPIO [unused]		
P6[5]	16	GPIO [unused]		
P7[0]	37	GPIO [unused]		
P7[1]	38	GPIO [unused]		

Abbreviations used in Table 4 have the following meanings:

- Res pull down = Resistive pull down
- Dgtl In = Digital Input
- HiZ digital = High impedance digital
- Dgtl Out = Digital Output



2.3 Software Pins

Table 5 contains information about the software pins on this device in alphabetical order. (Only software-accessible pins are shown.)

Table 5. Software Pins

Name	Port	Type
\SPI 1:miso m\	P4[1]	Dgtl In
\SPI 1:mosi m\	P4[0]	Dgtl Out
\SPI 1:sclk m\	P4[2]	Dgtl Out
\UART 1:rx wake\	P3[0]	Dgtl In
\UART 1:tx\	P3[1]	Dgtl Out
antpow	P6[1]	Software
		In/Out
Debug:SWD_CK	P3[3]	Reserved
Debug:SWD_IO	P3[2]	Reserved
dio1	P4[6]	Software
		In/Out
GPIO [unused]	P5[6]	
GPIO [unused]	P0[0]	
GPIO [unused]	P1[6]	
GPIO [unused]	P7[0]	
GPIO [unused]	P0[1]	
GPIO [unused]	P0[3]	
GPIO [unused]	P7[1]	
GPIO [unused]	P1[2]	
GPIO [unused]	P1[1]	
GPIO [unused]	P1[0]	
GPIO [unused]	P1[5]	
GPIO [unused]	P1[4]	
GPIO [unused]	P1[3]	
GPIO [unused]	P5[5]	
GPIO [unused]	P5[0]	
GPIO [unused]	P0[7]	
GPIO [unused]	P0[6]	
GPIO [unused]	P5[3]	
GPIO [unused]	P5[2]	
GPIO [unused]	P5[1]	
GPIO [unused]	P4[5]	
GPIO [unused]	P6[2]	
GPIO [unused]	P6[0]	
GPIO [unused]	P2[7]	
GPIO [unused]	P6[5]	
GPIO [unused]	P6[4]	
GPIO [unused]	P1[7]	
GPIO [unused]	P2[6]	
GPIO [unused]	P2[2]	
GPIO [unused]	P2[1]	
GPIO [unused]	P2[0]	
GPIO [unused]	P2[5]	
GPIO [unused]	P2[4]	
GPIO [unused]	P2[3]	
GPIO [unused]	P3[7]	



Name	Port	Туре
GPIO [unused]	P3[5]	
GPIO [unused]	P3[4]	
GPIO [unused]	P3[6]	
GPIO [unused]	P4[4]	
nss	P4[3]	Software In/Out
pin_wakeup	P0[2]	Software In/Out
SPI_BUSY	P4[7]	Software In/Out
SPI_NRESET	P5[7]	Software In/Out
XTAL 32kHz:Xi	P0[4]	Reserved
XTAL 32kHz:Xo	P0[5]	Reserved

Abbreviations used in Table 5 have the following meanings:

- Dgtl In = Digital Input
- Dgtl Out = Digital Output

For more information on reading, writing and configuring pins, please refer to:

- Pins chapter in the <u>System Reference Guide</u>
 CyPins API routines
- Programming Application Interface section in the cy_pins component datasheet



3 System Settings

3.1 System Configuration

Table 6. System Configuration Settings

Name	Value
Device Configuration Mode	Compressed
Unused Bonded IO	Disallowed
Heap Size (bytes)	0x1800
Stack Size (bytes)	0x0100
Include CMSIS Core Peripheral Library Files	True

3.2 System Debug Settings

Table 7. System Debug Settings

Name	Value
Debug Select	SWD (serial wire debug)
Chip Protection	Open

3.3 System Operating Conditions

Table 8. System Operating Conditions

Name	Value
VDDA (V)	3.3
VDDD (V)	3.3
Variable VDDA	True

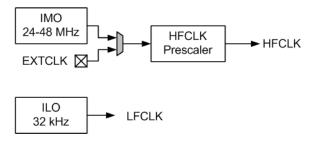


4 Clocks

The clock system includes these clock resources:

- Two internal clock sources:
 - o 24 to 48 MHz Internal Main Oscillator (IMO) ±2% at all frequencies with trim
 - o 32 kHz Internal Low Speed Oscillator (ILO)
- External clock (EXTCLK) generated using a signal from an I/O pin
- High-frequency clock (HFCLK) of up to 48 MHz selected from IMO or external clock
- Dedicated prescaler for HFCLK
- · Low-frequency clock (LFCLK sourced by ILO
 - o Dedicated prescaler for system clock (SYSCLK) of up to 48 MHz sourced by HFCLK
- 24 to 48 MHz Internal Main Oscillator (IMO) ±2%

Figure 3. System Clock Configuration





4.1 System Clocks

Table 9 lists the system clocks used in this design.

Table 9. System Clocks

Name	Domain	Source	Desired	Nominal	Accuracy	Start	Enabled
			Freq	Freq	(%)	at	
						Reset	
SysClk	NONE	HFClk	? MHz	24 MHz	±2	True	True
PLL0_Sel	NONE	IMO	24 MHz	24 MHz	±2	True	True
IMO	NONE		24 MHz	24 MHz	±2	True	True
HFCIk	NONE	IMO	24 MHz	24 MHz	±2	True	True
ILO	NONE		40 kHz	40 kHz	-50,+100	True	True
LFClk	NONE	ILO	? MHz	40 kHz	-50,+100	True	True
Timer_Sel	NONE	WCO	32.768	32.768	±0.015	True	True
			kHz	kHz			
WCO	NONE		32.768	32.768	±0.015	False	True
			kHz	kHz			
RTC_Sel	NONE		? MHz	? MHz	±0	True	True
Timer1	NONE	Timer_Sel	? MHz	? MHz	±0	False	False
Timer2	NONE	Timer_Sel	? MHz	? MHz	±0	False	False
ExtClk	NONE		16 MHz	? MHz	±0	False	False
Timer (WDT)	NONE	LFClk	? MHz	? MHz	±0	False	False
PLL0	NONE	PLL0_Sel	24 MHz	? MHz	±2	False	False
Timer0	NONE	Timer_Sel	? MHz	? MHz	±0.015	False	False
ECO	NONE		24 MHz	? MHz	±0	False	False

4.2 Local and Design Wide Clocks

Local clocks drive individual analog and digital blocks. Design wide clocks are a user-defined optimization, where two or more analog or digital blocks that share a common clock profile (frequency, etc) can be driven from the same clock divider output source.

Figure 4. Local and Design Wide Clock Configuration

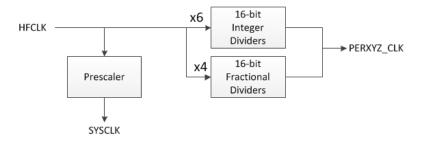


Table 10 lists the local clocks used in this design.

Table 10. Local Clocks

Name	Domain	Source	Desired Freq	Nominal Freq	Accuracy (%)	Start at Reset	Enabled
SPI_1_SCBCLK	FIXED FUNCT- ION	HFClk	48 MHz	24 MHz	±2	True	True



Name	Domain	Source	Desired Freq	Nominal Freq	Accuracy (%)	Start at Reset	Enabled
UART_1 SCBCLK	FIXED FUNCT- ION	HFClk	1.498 MHz	1.5 MHz	±2	True	True

For more information on clocking resources, please refer to:

- Clocking System chapter in the PSoC 4 Technical Reference Manual
- Clocking System Chapter in the FSOC 4 Technical
 Clocking chapter in the System Reference Guide
 CySysClkIno API routines
 CySysClkPIIO API routines
 CySysClkEco API routines
 CySysClkWite API routines

 - o CySysClkWrite API routines



5 Interrupts

5.1 Interrupts

This design contains the following interrupt components: (0 is the highest priority)

Table 11. Interrupts

Name	Intr Num	Vector	Priority
wakeup_irq	0	0	3
UART_1_RX_WAKEUP_IRQ	3	3	3
global_irq	4	4	2
UART 1 SCB IRQ	8	8	0

For more information on interrupts, please refer to:

- Interrupt Controller chapter in the PSoC 4 Technical Reference Manual
- Interrupts chapter in the <u>System Reference Guide</u>
 Cylnt API routines and related registers
- Datasheet for cy isr component



6 Flash Memory

PSoC 4 devices offer a host of Flash protection options and device security features that you can leverage to meet the security and protection requirements of an application. These requirements range from protecting configuration settings or Flash data to locking the entire device from external access.

Table 12 lists the Flash protection settings for your design.

Table 12. Flash Protection Settings

Start Address	End Address	Protection Level
0x0	0x1FFFF	U - Unprotected

Flash memory is organized as rows with each row of flash having 256 bytes. Each flash row can be assigned one of four protection levels:

- U Unprotected
- W Full Protection

For more information on Flash memory and protection, please refer to:

- Flash Protection chapter in the <u>PSoC 4 Technical Reference Manual</u>
- Flash and EEPROM chapter in the **System Reference Guide**
 - CySysFlash API routines

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7 Bootloader and Bootloadable

Figure 5 details the Flash memory map for the bootloader and/or bootloadable application(s) included in this design.

Figure 5. Bootloader Memory Map

Bootloadable application
Address 0

Metadata (64 bytes)

Bootloadable application

7.1 Bootloadable Application

Table 13. Bootloadable Settings

Name	Value
Application Version	0x0000
Application ID	0x0000
Application Custom ID	0x0
Application Image 1 Start Address	0x1600
Application Image 1 End Address	0x1FFFF
Manual Application Image Placement	False

7.2 Bootloader Application

Table 14. Bootloader Settings

· · · · · · · · · · · · · · · · · · ·					
Name	Value				
Checksum Type	BasicChecksum				
Supports Multiple Application Images	False				
Application Version	0x0000				
Bootloader Start Address	0x0				
Bootloader End Address	0x1595				

For more information on the bootloader and startup please refer to:

• Startup and Linking chapter in the System Reference Guide



• Datasheet for Bootloader and Bootloadable component

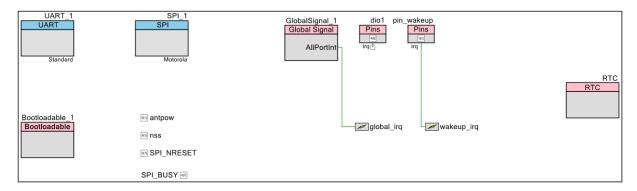


8 Design Contents

This design's schematic content consists of the following schematic sheet:

8.1 Schematic Sheet: Page 1

Figure 6. Schematic Sheet: Page 1



This schematic sheet contains the following component instances:

- Instance <u>Bootloadable_1</u> (type: Bootloadable_v1_60)
- Instance <u>RTC</u>(type: RTC_P4_v1_30)
- Instance <u>SPI_1</u> (type: SCB_P4_v4_0)
- Instance <u>UART_1</u> (type: SCB_P4_v4_0)



9 Components

9.1 Component type: Bootloadable [v1.60]

9.1.1 Instance Bootloadable_1

Description: Provides bootloadable application functionality.

Instance type: Bootloadable [v1.60]

Datasheet: online component datasheet for Bootloadable

Table 15. Component Parameters for Bootloadable 1

Parameter Name	Value	Description
appCustomID	0	Provides a 4 byte custom ID
		number to represent anything in the Bootloadable application.
appID	0	Provides a 2 byte number to represent the ID of the bootloadable application.
appVersion	0	Provides a 2 byte number to represent the version of the bootloadable application.
autoPlacement	true	Provides a method for PSoC Creator to place a Bootloadable application image at a specified location. If true, the image will be placed automatically. If false, the image will be placed at an address specified by the Placement Address option.
checksumExcludeSize	0	Provides a size in bytes of checksum exclude section
elfFilePath	.\bootloader.cydsn\C- ortexM0p\ARM_GCC 541\Debug\bootloader.elf	Provides a reference to the Bootloader application (.elf) that is associated with this Bootloadable application.
hexFilePath	.\bootloader.cydsn\C- ortexM0p\ARM_GCC 541\Debug\bootloader.hex	Provides a reference to the Bootloader application (.hex) that is associated with this Bootloadable application.
placementAddress	0	Allows specifying an address where the bootloadable application will be placed in the memory. Available only if the Automatic Application Image Placement option is true.
User Comments		Instance-specific comments.

9.2 Component type: RTC_P4 [v1.30]

9.2.1 Instance RTC

Description: PSoC 4 Real-time Clock Instance type: RTC_P4 [v1.30]

Datasheet: online component datasheet for RTC_P4

Table 16. Component Parameters for RTC

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Parameter Name	Value	Description
AlarmFunctionalityEn	true	This parameter defines the initial status of the Alarm functionality. This parameter can contain the following values: true-Alarm functionality is enabled, false-Alarm functionality is disabled.
DateFormat	MM/DD/YYYY	This parameter stores the date format. Can contain the following values: MM/DD/YYYY, DD/MM/YYYY, YYYY/MM/DD.
DaylightSavingsTimeEn	false	This parameter stores the default state of the DST functionality. The possible values: true – DST functionality is enabled, false – DST functionality is disabled.
DayOfMonthDstStart	22	This parameter stores the day of the month when the DST functionality should be started. The possible values are 131.
DayOfMonthDstStop	22	This parameter stores the day of the month when the DST functionality should be stopped. The possible values are 131.
DayOfWeekDstStart	Sunday	This parameter stores the day of the week when the DST functionality should be started. The possible values are MONDAYSUNDAY.
DayOfWeekDstStop	Sunday	This parameter stores the day of the week when the DST functionality should be stopped. The possible values are MONDAYSUNDAY.
DstDateType	Relative	This parameter stores the DST date type. Can contain the following values: Relative, Fixed.
HoursDstStart	00:00	This parameter stores the hour when the DST functionality should be started. The possible values are 00002300
HoursDstStop	00:00	This parameter stores the hour when the DST functionality should be stopped. The possible values are 00002300
InitialDay	1	This parameter stores the initial day. The possible values are 031
InitialHour	0	This parameter stores the initial hour. The possible values are 023
InitialMinute	0	This parameter stores the initial minute. The possible values are 059
InitialMonth	07/02/2021 0	This parameter stores the initial month. The possible values are 112



Parameter Name	Value	Description
InitialSecond	0	This parameter stores the initial second. The possible values are 059
InitialYear	1970	This parameter stores the initial year. The possible values are 1970MAX_UINT16
MonthDstStart	March	This parameter stores the month when the DST functionality should be started. The possible values are JANDEC.
MonthDstStop	October	This parameter stores the month when the DST functionality should be stopped. The possible values are JANDEC.
TimeFormat	24-Hour	This parameter stores the time format (24-Hours/12-Hours). The possible values: HOUR_12, HOUR_24.
UpdateManually	false	This parameter is used to map the RTC time update API automatically during RTC start to one of the WDTs selected and configured for RTC by the user in LFCLK interface.
User Comments		Instance-specific comments.
WeekOfMonthDstStart	Last	This parameter stores the week of the month when the DST functionality should be started. The possible values are FIRSTLAST.
WeekOfMonthDstStop	Last	This parameter stores the week of the month when the DST functionality should be stopped. The possible values are FIRSTLAST.

9.3 Component type: SCB_P4 [v4.0]

9.3.1 Instance SPI_1

Description: Serial Communication Block (SCB)

Instance type: SCB_P4 [v4.0]

Datasheet: online component datasheet for SCB_P4

Table 17. Component Parameters for SPI_1



Parameter Name	Value	Description
Ezl2cByteModeEnable	false	When the SCB mode is EZI2C,
LZIZODYtelWodeLilable	laise	this parameter specifies the
		number of bits per FIFO data
		element.
		The byte mode – false: a 16-bit
		FIFO data element. The FIFO
		depth is 8 entries.
		The byte mode – true: an 8-bit
		FIFO data element. The FIFO
		depth is 16 entries.
		Applicable only for devices
		other than PSoC 4000/PSoC
		4100/PSoC 4200.
C=10 oCloskCroseTorres	foloo	
Ezl2cClockFromTerm	false	When the SCB mode is EZI2C,
		this parameter provides a clock
		terminal to connect a clock
F 10 01 101 111	,	outside the component.
Ezl2cClockStretching	true	When the SCB mode is EZI2C,
		this parameter specifies
		whether the SCL is stretched
		while in EZI2C operation.
Ezl2cDataRate	100	When the SCB mode is EZI2C,
		this parameter defines EZI2C
		Data rate in kbps. The standard
		data rates are: 100, 400 and
		1000 kbps.
Ezl2cNumberOfAddresses	1	When the SCB mode is EZI2C,
		this parameter defines the
		number of I2C slave addresses
		that device respond to.
Ezl2cPrimarySlaveAddress	8	When the SCB mode is EZI2C,
		this parameter specifies EZI2C
		primary 7-bits slave address
		(MSB ignored).
Ezl2cSecondarySlaveAddress	9	When the SCB mode is EZI2C,
		this parameter specifies EZI2C
		secondary 7-bits slave address
		(MSB ignored).
		Only applicable when EZI2C
		clock stretching option is set.
Ezl2cSubAddressSize	8	When the SCB mode is EZI2C,
		this parameter specifies the
		maximum size of the slave
		buffer that is exposed to the
		master: 8bits – maximum buffer
		size is 256 bytes, 16 bits –
		maximum buffer size is 65535
		bytes.
Ezl2cWakeEnable	false	When the SCB mode is EZI2C,
	.5.75	this parameter enables wakeup
		from Deep Sleep on I2C
		address match event.
	1	2.2.2.222



Parameter Name	Value	Description
I2C Bus Voltage	3.3	When the SCB mode is I2C, this parameter specifies the voltage applied to the pull-up resistors on the I2C bus.
		Only applicable for devices other than PSoC 4000/PSoC 4100/PSoC 4200.
I2C Bus Voltage	3.3	When the SCB mode is EZI2C, this parameter specifies the voltage applied to the pull-up resistors on the I2C bus. Only applicable for devices other than PSoC 4000/PSoC 4100/PSoC 4200.
I2cAcceptAddress	false	When the SCB mode is I2C, this parameter specifies whether to accept the match slave address in RX FIFO or not. All slave matched addresses are ACKed. The user has to register the callback function to handle accepted addresses. This feature has to be used when more than one address support is required.
I2cAcceptGeneralCall	false	When the SCB mode is I2C, this parameter specifies whether to accept the general call address. The general call address is ACKed when accepted and NAKed otherwise. The user has to register the callback function to handle the general call address.
I2cByteModeEnable	false	When the SCB mode is I2C, this parameter specifies the number of bits per FIFO data element. The byte mode – false: a 16-bit FIFO data element. The FIFO depth is 8 entries. The byte mode – true: an 8-bit FIFO data element. The FIFO depth is 16 entries. Applicable only for devices other than PSoC 4000/PSoC 4100/PSoC 4200.
I2cClockFromTerm	false	When the SCB mode is I2C, this parameter provides a clock terminal to connect a clock outside the component.
I2cDataRate	100	When the SCB mode is I2C, this parameter specifies the data rate in kbps. The standard data rates are: 100, 400 and 1000 kbps.



		UTPRE EMBEDDED IN TO
Parameter Name	Value	Description
I2cExternIntrHandler	false	When the SCB mode is I2C, this parameter specifies whether the I2C interrupt handler is configured in SCB_I2CInit(). This parameter is intended to be used by the PM/SM bus component. The modification parameter default value causes I2C mode failures.
I2cManualOversampleControl	true	When the SCB mode is I2C, this parameter specifies the method of calculating the oversampling as manual or automatic.
I2cMode	Slave	When the SCB mode is I2C, this parameter defines the I2C operation mode as: Slave, Master, Multi-Master or Multi-Master-Slave.
I2cOvsFactor	16	When the SCB mode is I2C, this parameter defines the oversampling factor of SCBCLK.
I2cOvsFactorHigh	8	When the SCB mode is I2C, this parameter defines the high oversampling factor of SCBCLK. Only applicable for I2C Master modes.
I2cOvsFactorLow	8	When the SCB mode is I2C, this parameter defines the low oversampling factor of SCBCLK. Only applicable for I2C Master modes.
I2cSlaveAddress	8	When the SCB mode is I2C, this parameter specifies the I2C 7-bits slave address (MSB ignored).
I2cSlaveAddressMask	254	When the SCB mode is I2C, this parameter specifies the I2C Slave address mask. Bit value 0 – excludes bit from address comparison. Bit value 1 – the bit needs to match with the corresponding bit of the I2C slave address.
I2cWakeEnable	false	When the SCB mode is I2C, this parameter enables wakeup from Deep Sleep on an I2C address match event.
ScbMisoSdaTxEnable	true	This parameter defines the availability of the spi_miso_i2csda_uart_tx pin.
ScbMode	SPI	This parameter defines the mode of operation for the SCB component.
ScbMosiSclRxEnable	true	This parameter defines the availability of the spi_mosi_i2cscl_uart_rx pin.



Parameter Name	Value	Description
ScbRxWakeIrqEnable	false	This parameter defines the
·		availability of the spi_mosi_i2c
		scl_uart_rx_wake pin.
ScbSclkEnable	false	This parameter defines the
		availability of the sclk pin.
ScbSs0Enable	false	This parameter defines the
		availability of the ss0 pin.
ScbSs1Enable	false	This parameter defines the
		availability of the ss1 pin.
ScbSs2Enable	false	This parameter defines the
		availability of the ss2 pin.
ScbSs3Enable	false	This parameter defines the
		availability of the ss3 pin.
Show EZI2C Terminals	false	When the SCB mode is EZI2C,
		this parameter removes internal
		pins and expose signals to
		terminals. The exposed
		terminals must be connected to
		the pins.
Show I2C Terminals	false	When the SCB mode is I2C, this
		parameter removes internal pins
		and expose signals to terminals.
		The exposed terminals must be
		connected to the pins.
Show SPI Terminals	false	When the SCB mode is SPI,
		this parameter removes internal
		pins and expose signals to
		terminals. The exposed
		terminals must be connected to
		the pins or SmartIO component.
Show UART Terminals	false	When the SCB mode is UART,
		this parameter removes internal
		pins and expose signals to
		terminals. The exposed
		terminals must be connected to
		the pins or SmartIO component.
Slew Rate	Fast	When the SCB mode is EZI2C,
		this parameter specifies the
		slew rate settings of the I2C
		pins.
		For devices supporting GPIO Over-Voltage Tolerance
		(GPIO_OVT) pins, I2C FM+
		options should be used when
		I2C data rate is greater than
		400 kbps. This option also
		requires the I2C bus voltage to
		be defined.Refer to the Device
		Datasheet to determine which
		pins are GPIO OVT capable.
		pino are or ro_ovir capable.



Parameter Name	Value	Description EMBEDDED IN TO
Slew Rate	Fast	When the SCB mode is I2C, this
Ciew itale	1 431	parameter specifies the slew
		rate settings of the I2C pins.
		For devices supporting GPIO
		Over-Voltage Tolerance
		(GPIO_OVT) pins, I2C FM+
		options should be used when
		I2C data rate is greater than
		400 kbps. This option also
		requires the I2C bus voltage to
		be defined. Refer to the Device
		Datasheet to determine which
		pins are GPIO_OVT capable.
CmiDitData	0000	
SpiBitRate	8000	When the SCB mode is SPI,
		this parameter specifies the Bit
		rate in kbps (up to 8000 kbps);
		the actual rate may differ based
		on available clock frequency
		and component settings. This
		parameter has no effect if the
		Clock from terminal parameter
		is enabled.
SpiBitsOrder	MSB First	When the SCB mode is SPI,
		this parameter defines the bit
		order as: MSB first or LSB first.
SpiByteModeEnable	false	When the SCB mode is SPI,
		this parameter specifies the
		number of bits per FIFO data
		element.
		The byte mode – false: a 16-bit
		FIFO data element. The FIFO
		depth is 8 entries.
		The byte mode – true: an 8-bit
		FIFO data element. The FIFO
		depth is 16 entries.
		Applicable only for devices
		other than PSoC 4000/PSoC
		4100/PSoC 4200.
SpiClockFromTerm	false	When the SCB mode is SPI,
		this parameter provides a clock
		terminal to connect a clock
		outside the component.
SpiFreeRunningSclk	false	When the SCB mode is SPI,
		this parameter specifies the
		SCLK generation by the master
		as: gated or free running
		(continuous).
		Applicable only for devices
		other than PSoC 4000/PSoC
		4100/PSoC 4200.



Parameter Name	Value	Description
SpiInterruptMode	None	When the SCB mode is SPI,
		this parameter specifies the
		interrupt mode. None: Removes
		all interrupt support. Internal:
		Leaves the interrupt SCBIRQ
		inside the component - the
		interrupt terminal becomes
		invisible. External: Provides an
		interrupt terminal to connect an
		interrupt outside the component.
SpiIntrMasterSpiDone	false	When the SCB mode is SPI,
		this parameter enables the
		SCB.INTR_M. SPI_DONE
		interrupt source.
		SCB.INTR_M. SPI_DONE: all
		data are sent into TX FIFO and
		the TX FIFO and the shifter
		register are emptied.
		Only applicable for SPI Master
0 11 4 D E 11	6.1	mode.
SpilntrRxFull	false	When the SCB mode is SPI,
		this parameter enables the
		SCB.INTR_RX.FULL interrupt
		SOURCE.
		SCB.INTR_RX.FULL trigger condition: RX FIFO is full.
CnilntrDyNotEmpty	false	When the SCB mode is SPI,
SpiIntrRxNotEmpty	laise	this parameter enables the
		SCB.INTR RX.NOT EMPTY
		interrupt source.
		SCB.INTR RX.NOT EMPTY
		trigger condition: RX FIFO is not
		empty. There is at least one
		entry to get data from.
SpiIntrRxOverflow	false	When the SCB mode is SPI,
		this parameter enables the
		SCB.INTR RX.OVERFLOW
		interrupt source.
		SCB.INTR_RX.OVERFLOW
		trigger condition: attempt to
		write to a full RX FIFO.
SpiIntrRxTrigger	false	When the SCB mode is SPI,
		this parameter enables the
		SCB.INTR_RX.TRIGGER
		interrupt source.
		SCB.INTR_RX.TRIGGER
		trigger condition: remains active
		until RX FIFO has more entries
		than the value specified by
ChilateDul lade effect	falss	SpiRxTriggerLevel.
SpiIntrRxUnderflow	false	When the SCB mode is SPI,
		this parameter enables the
		SCB.INTR_RX.UNDERFLOW
		interrupt source. SCB.INTR RX.UNDERFLOW
		trigger condition: attempt to
		read from an empty RX FIFO.
		read from an empty tox r iFU.



		EMBEDDED IN TO
Parameter Name	Value	Description
SpiIntrSlaveBusError	false	When the SCB mode is SPI,
		this parameter enables the
		SCB.INTR_SLAVE.BUS
		ERROR interrupt source.
		SCB.INTR_SLAVE.BUS
		ERROR trigger condition: slave
		select line is deselected at an
		unexpected time in the SPI
		transfer.
		Only applicable for SPI Slave
		mode.
SpiIntrTxEmpty	false	When the SCB mode is SPI,
- F		this parameter enables the
		SCB.INTR_TX.EMPTY interrupt
		source.
		SCB.INTR TX.EMPTY trigger
		condition: TX FIFO is empty.
SpiIntrTxNotFull	false	When the SCB mode is SPI,
Opiniu i Aivou uli	iaise	this parameter enables the
		SCB.INTR_TX.NOT_FULL
		interrupt source.
		SCB.INTR TX.NOT FULL
		trigger condition: TX FIFO is not
		full. There is at least one entry
O. H. I. T. O fl	f.1.	to put data.
SpiIntrTxOverflow	false	When the SCB mode is SPI,
		this parameter enables the
		SCB.INTR_TX.OVERFLOW
		interrupt source.
		SCB.INTR_TX.OVERFLOW
		trigger condition: attempt to
On the fact of the same	6.1.	write to a full TX FIFO.
SpiIntrTxTrigger	false	When the SCB mode is SPI,
		this parameter enables the
		SCB.INTR_TX.TRIGGER
		interrupt source.
		SCB.INTR_TX.TRIGGER
		trigger condition: remains active
		until TX FIFO has fewer entries
		than the value specified by
		SpiTxTriggerLevel.
SpiIntrTxUnderflow	false	When the SCB mode is SPI,
		this parameter enables the
		SCB.INTR_TX.UNDERFLOW
		interrupt source.
		SCB.INTR_TX.UNDERFLOW
		trigger condition: attempt to
		read from an empty TX FIFO.
SpiLateMisoSampleEnable	false	When the SCB mode is SPI,
		this parameter enables late
		sampling of the MISO line by
		the master.
SpiMedianFilterEnable	false	When the SCB mode is SPI,
		this parameter applies a digital
		3 tap median filter to the SPI
		input line.
.		•



Parameter Name	Value	Description
SpiMode	Master	When the SCB mode is SPI,
•		this parameter selects SPI
		mode of operation as: Slave or
		Master.
SpiNumberOfRxDataBits	8	When the SCB mode is SPI,
		this parameter specifies the
		number of data bits inside the
		SPI byte/word for RX direction.
SpiNumberOfSelectLines	0	When the SCB mode is SPI,
		this parameter defines the
		number of slave select lines.
		The SPI Slave has only one slave select line. The SPI
		Master has up to 4 lines.
SpiNumberOfTxDataBits	8	When the SCB mode is SPI,
SpiriumberOrrxDatabits	0	this parameter define the
		number of data bits inside the
		SPI byte/word for TX direction.
SpiOvsFactor	8	When the SCB mode is SPI,
5510 (01 4010)		this parameter defines the
		oversampling factor of
		SCBCLK.
SpiRemoveMiso	false	When the SCB mode is SPI,
•		this parameter removes the
		MISO pin.
SpiRemoveMosi	false	When the SCB mode is SPI,
		this parameter removes the
		MOSI pin.
SpiRemoveSclk	false	When the SCB mode is SPI,
		this parameter removes the
		SCLK pin.
SpiRxBufferSize	8	When the SCB mode is SPI,
		this parameter defines the size
D. D. O. A. A. F. A. L.	f.1	of the RX buffer.
SpiRxOutputEnable	false	When the SCB mode is SPI,
		this parameter enables the RX
		trigger output terminal of the component. This terminal must
		be connected to the DMA input
		trigger or left unconnected. Only
		applicable for devices which
		have a DMA controller.
SpiRxTriggerLevel	7	When the SCB mode is SPI,
		this parameter defines the
		number of entries in the RX
		FIFO to control the SCB.INTR
		RX.TRIGGER interrupt event or
2 10 11 11	00111	RX DMA trigger output.
SpiSclkMode	CPHA = 0, CPOL	When the SCB mode is SPI,
	= 0	this parameter defines the serial
		clock phase (CPHA) and
SniSa0Dalarity	A office Lave	polarity (CPOL).
SpiSs0Polarity	Active Low	When the SCB mode is SPI, this parameter specifies active
		polarity of slave select 0.
		polarity of slave select o.
		Applicable only for devices
		other than PSoC 4000/PSoC
		00101 01011 000 4000/1 000



Parameter Name	Value	Doscription EMBEDDED IN TO
SpiSs1Polarity	Active Low	Description When the SCB mode is SPI,
	Active Low	this parameter specifies active
		polarity of slave select 1.
		Applicable only for devices
		other than PSoC 4000/PSoC 4100/PSoC 4200.
SpiSs2Polarity	Active Low	When the SCB mode is SPI, this parameter specifies active polarity of slave select 2.
		Applicable only for devices other than PSoC 4000/PSoC 4100/PSoC 4200.
SpiSs3Polarity	Active Low	When the SCB mode is SPI, this parameter specifies active polarity of slave select 3.
		Applicable only for devices other than PSoC 4000/PSoC 4100/PSoC 4200.
SpiSubMode	Motorola	When the SCB mode is SPI, this parameter defines the sub mode of the SPI as: Motorola, TI(Start Coincides), TI(Start Precedes), or National Semiconductor.
SpiTransferSeparation	Continuous	When the SCB mode is SPI, this parameter defines the type of SPI transfers separation as: continuous or separated.
SpiTxBufferSize	8	When the SCB mode is SPI, this parameter defines the size of the TX buffer.
SpiTxOutputEnable	false	When the SCB mode is SPI, this parameter enables the TX trigger output terminal of the component. This terminal must be connected to the DMA input trigger or left unconnected. Only applicable for devices which have a DMA controller.
SpiTxTriggerLevel	0	When the SCB mode is SPI, this parameter defines the number of entries in the TX FIFO to control the SCB.INTRTX.TRIGGER interrupt event or TX DMA trigger output.
SpiWakeEnable	false	When the SCB mode is SPI, this parameter enables wakeup from Deep Sleep on slave select event.



Parameter Name	Value	Description
UartByteModeEnable	false	When the SCB mode is UART,
		this parameter specifies the number of bits per FIFO data
		element.
		The byte mode – false: a 16-bit
		FIFO data element. The FIFO depth is 8 entries.
		The byte mode – true: an 8-bit
		FIFO data element. The FIFO depth is 16 entries.
		Applicable only for devices
		other than PSoC 4000/PSoC 4100/PSoC 4200.
UartClockFromTerm	false	When the SCB mode is UART,
		this parameter provides a clock terminal to connect a clock
UartCtsEnable	false	outside the component. When the SCB mode is UART,
CartotoEnable	Taioo	this parameter enables the cts input.
		Only applicable for devices other than PSoC 4000/PSoC 4100/PSoC 4200.
UartCtsPolarity	Active Low	When the SCB mode is UART,
		this parameter specifies active polarity of an input cts signal.
		Only applicable for devices other than PSoC 4000/PSoC 4100/PSoC 4200.
UartDataRate	115200	When the SCB mode is UART,
		this parameter specifies the Baud rate in bps (up to 1000
		kbps); the actual rate may differ
		based on available clock frequency and component
		settings. This parameter has no
		effect if the Clock from terminal
UartDirection	TX + RX	parameter is enabled. When the SCB mode is UART,
Cartollection	17 7 17	this parameter enables RX or
		TX direction or both
	false	simultaneously.
UartDropOnFrameErr	iaise	When the SCB mode is UART, this parameter defines whether
		the data is dropped from RX
Lloyt Drow On Donity (Fire	f-1	FIFO on a frame error event.
UartDropOnParityErr	false	When the SCB mode is UART, this parameter determines
		whether the data is dropped
		from RX FIFO on a parity error event.
		eveni.



Daramatar Nama	Value	EMBEDDED IN TO
Parameter Name UartInterruptMode	None	Description When the SCB mode is UART,
Cartificerruptiviode	None	this parameter specifies the
		interrupt mode. None: Removes
		all interrupt support. Internal:
		Leaves the interrupt SCBIRQ
		inside the component - the
		interrupt terminal becomes
		invisible. External: Provides an
		interrupt terminal to connect an
		interrupt outside component.
UartIntrRxBreakDetected	false	This parameter enables the RX
Cartinar (KB) Gaile Globale a		break detection interrupt source
		to trigger the interrupt output.
UartIntrRxFrameErr	false	When the SCB mode is UART,
Cartifier (XI TallioEll	laise	this parameter enables the
		SCB.INTR RX.FRAME -
		ERROR interrupt source.
		SCB.INTR_RX.FRAME
		ERROR trigger condition: frame
		error in received data frame.
UartIntrRxFull	false	When the SCB mode is UART,
Caramar ou an		this parameter enables the
		SCB.INTR_RX.FULL interrupt
		source.
		SCB.INTR_RX.FULL trigger
		condition: RX FIFO is full.
UartIntrRxNotEmpty	false	When the SCB mode is UART,
,	1	this parameter enables the
		SCB.INTR_RX.NOT_EMPTY
		interrupt source.
		SCB.INTR_RX.NOT_EMPTY
		trigger condition: RX FIFO is not
		empty. There is at least one
		entry to get data from.
UartIntrRxOverflow	false	When the SCB mode is UART,
		this parameter enables the
		SCB.INTR_RX.OVERFLOW
		interrupt source.
		SCB.INTR_RX.OVERFLOW
		trigger condition: attempt to
		write to a full RX FIFO.
UartIntrRxParityErr	false	When the SCB mode is UART,
		this parameter enables the
		SCB.INTR_RX.PARITY
		ERROR interrupt source.
		SCB.INTR_RX.PARITY
		ERROR trigger condition: parity
III. alla A.D. Talia		error in received data frame.
UartIntrRxTrigger	false	When the SCB mode is UART,
		this parameter enables the
		SCB.INTR_RX.TRIGGER
		interrupt source.
		SCB.INTR_RX.TRIGGER
		trigger condition: remains active until RX FIFO has more entries
		than the value specified by
		UartRxTriggerLevel.
		Garti Willigger Level.



Parameter Name	Value	Description
UartIntrRxUnderflow	false	When the SCB mode is UART,
		this parameter enables the
		SCB.INTR_RX.UNDERFLOW
		interrupt source.
		SCB.INTR_RX.UNDERFLOW
		trigger condition: attempt to read from an empty RX FIFO.
UartIntrTxEmpty	false	When the SCB mode is UART,
Curtina FAEIIIpty	laise	this parameter enables the
		SCB.INTR_TX.EMPTY interrupt
		source.
		SCB.INTR_TX.EMPTY trigger
LL . Al. A.T. Al. AF. II	f.1.	condition: TX FIFO is empty.
UartIntrTxNotFull	false	When the SCB mode is UART,
		this parameter enables the SCB.INTR TX.NOT FULL
		interrupt source.
		SCB.INTR_TX.NOT_FULL
		trigger condition: TX FIFO is not
		full. There is at least one entry
		to put data.
UartIntrTxOverflow	false	When the SCB mode is UART,
		this parameter enables the SCB.INTR TX.OVERFLOW
		interrupt source.
		SCB.INTR TX.OVERFLOW
		trigger condition: attempt to
		write to a full TX FIFO.
UartIntrTxTrigger	false	When the SCB mode is UART,
		this parameter enables the
		SCB.INTR_TX.TRIGGER interrupt source.
		SCB.INTR_TX.TRIGGER
		trigger condition: remains active
		until TX FIFO has fewer entries
		than the value specified by
		UartTxTriggerLevel.
UartIntrTxUartDone	false	When the SCB mode is UART,
		this parameter enables the SCB.INTR_TX.UART_DONE
		interrupt source.
		SCB.INTR_TX.UART_DONE
		trigger condition: all data are
		sent in to TX FIFO and the
		transmit FIFO and the shifter
LlortIntrTyl lortLootArb	foloo	register are emptied.
UartIntrTxUartLostArb	false	When the SCB mode is UART, this parameter enables the
		SCB.INTR_TX.UART_ARB
		LOST interrupt source.
		SCB.INTR_TX.UART_ARB
		LOST trigger condition: UART
		lost arbitration, the value driven
		on the TX line is not the same as the value observed on the
		RX line. This event is useful
		when the transmitter and the
		receiver share a TX/RX line.
		Only applicable for UART
	07/00/0004 07:00	SmartCard mode.



Dayamatay Name	Value	Docorintion EMBEDDED IN TO
Parameter Name UartIntrTxUartNack	Value false	Description When the SCB mode is UART,
Oartifiti i xOartivack	laise	this parameter enables the
		SCB.INTR_TX.UART_NACK
		interrupt source.
		SCB.INTR TX.UART NACK
		trigger condition: UART
		transmitter received a negative
		acknowledgement.
		Only applicable for UART
		SmartCard mode.
UartIntrTxUnderflow	false	When the SCB mode is UART,
		this parameter enables the
		SCB.INTR_TX.UNDERFLOW
		interrupt source. SCB.INTR TX.UNDERFLOW
		trigger condition: attempt to
		read from an empty TX FIFO.
UartIrdaLowPower	false	When the SCB mode is UART,
OartiidaLowi Owei	laise	this parameter enables the low
		power receiver option.
		Only applicable for UART IrDA
		mode.
UartIrdaPolarity	Non-Inverting	When the SCB mode is UART,
,		this parameter inverts the
		incoming RX line signal.
		Only applicable for UART IrDA
		mode.
UartMedianFilterEnable	false	When the SCB mode is UART,
		this parameter applies a digital
		3 tap median filter to the UART
Llowth Ma Capable	foloo	input line.
UartMpEnable	false	When the SCB mode is UART,
		this parameter enables the UART multi-processor mode.
		Only applicable for UART
		Standard mode.
UartMpRxAcceptAddress	false	When the SCB mode is UART,
Carampi da tecepa taareee	10.00	this parameter define whether to
		put the matched UART address
		into RX FIFO.
		Only applicable for UART multi-
		processor mode.
UartMpRxAddress	2	When the SCB mode is UART,
		this parameter defines the
		UART address.
		Only applicable for UART multi-
	055	processor mode.
UartMpRxAddressMask	255	When the SCB mode is UART,
		this parameter defines the address mask in multi-
		processor operation mode.
		Bit value 0 – excludes bit from
		address comparison.
		Bit value 1 – the bit needs to
		match with the corresponding
		bit of the UART address.
		Only applicable for UART multi-
		processor mode.



Parameter Name	Value	Description
UartNumberOfDataBits	8 bits	When the SCB mode is UART, this parameter defines the number of data bits inside the UART byte/word.
UartNumberOfStopBits	1 bit	When the SCB mode is UART, this parameter defines the number of Stop bits.
UartOvsFactor	12	When the SCB mode is UART, this parameter defines the oversampling factor of SCBCLK.
UartParityType	None	When the SCB mode is UART, this parameter applies UART parity check as Odd or Even or discards the parity entirely.
UartRtsEnable	false	When the SCB mode is UART, this parameter enables the rts output. Applicable only for devices other than PSoC 4000/PSoC
UartRtsPolarity	Active Low	4100/PSoC 4200. When the SCB mode is UART, this parameter specifies active polarity of the output rts signal. Applicable only for devices other than PSoC 4000/PSoC 4100/PSoC 4200.
UartRtsTriggerLevel	4	When the SCB mode is UART, this parameter specifies the number of entries in the RX FIFO to activate the rts output signal. When the receiver FIFO has fewer entries than the UartRtsTriggerLevel, an rts output signal is activated. Applicable only for devices other than PSoC 4000/PSoC 4100/PSoC 4200.
UartRxBreakWidth	11	This parameter specifies the break width in bits.
UartRxBufferSize	8	When the SCB mode is UART, this parameter defines the size of the RX buffer.
UartRxOutputEnable	false	When the SCB mode is UART, this parameter enables the RX trigger output terminal of the component. This terminal must be connected to the DMA input trigger or left unconnected. Only applicable for devices which have a DMA controller.



Davamatar Nama	Value	EMBEDDED IN TO
Parameter Name	Value	Description
UartRxTriggerLevel	/	When the SCB mode is UART,
		this parameter defines the
		number of entries in the RX
		FIFO to trigger control the
		SCB.INTR_RX.TRIGGER
		interrupt event or RX DMA
		trigger output.
UartSmCardRetryOnNack	false	When the SCB mode is UART,
		this parameter defines whether
		to send a message again when
		a NACK response is received.
		Only applicable for UART
		SmartCard mode.
UartSubMode	Standard	When the SCB mode is UART,
		this parameter defines the sub
		mode of UART as: Standard,
		SmartCard or IrDA.
UartTxBufferSize	8	When the SCB mode is UART,
GaittyBalloroi20		this parameter defines the size
		of the TX buffer.
UartTxOutputEnable	false	When the SCB mode is UART,
OartixOdiputEnable	laise	this parameter enables the TX
		trigger output terminal of the
		component. This terminal must
		be connected to the DMA input
		trigger or left unconnected. Only
		applicable for devices which
		have a DMA controller.
UartTxTriggerLevel	0	When the SCB mode is UART,
OarrixinggerLevel	0	
		this parameter defines the
		number of entries in the TX
		FIFO to control the SCB.INTR
		TX.TRIGGER interrupt event or
LL AVA/ - L E L L		TX DMA trigger output.
UartWakeEnable	false	When the SCB mode is UART,
		this parameter enables the
		wakeup from Deep Sleep on
		start bit event. The actual
		wakeup source is RX GPIO.
		The skip start UART feature
		allows it to continue receiving
		bytes.
User Comments	1	Instance-specific comments.

9.3.2 Instance UART_1

Description: Serial Communication Block (SCB)

Instance type: SCB_P4 [v4.0]

Datasheet: online component datasheet for SCB_P4

Table 18. Component Parameters for UART_1



Parameter Name	Value	Description
Ezl2cByteModeEnable	false	When the SCB mode is EZI2C,
		this parameter specifies the
		number of bits per FIFO data
		element.
		The byte mode – false: a 16-bit
		FIFO data element. The FIFO
		depth is 8 entries.
		The byte mode – true: an 8-bit
		FIFO data element. The FIFO
		depth is 16 entries.
		Applicable only for devices
		other than PSoC 4000/PSoC
		4100/PSoC 4200.
Ezl2cClockFromTerm	false	When the SCB mode is EZI2C,
		this parameter provides a clock
		terminal to connect a clock
		outside the component.
Ezl2cClockStretching	true	When the SCB mode is EZI2C,
		this parameter specifies
		whether the SCL is stretched
		while in EZI2C operation.
Ezl2cDataRate	100	When the SCB mode is EZI2C,
		this parameter defines EZI2C
		Data rate in kbps. The standard
		data rates are: 100, 400 and
		1000 kbps.
Ezl2cNumberOfAddresses	1	When the SCB mode is EZI2C,
		this parameter defines the
		number of I2C slave addresses
		that device respond to.
Ezl2cPrimarySlaveAddress	8	When the SCB mode is EZI2C,
•		this parameter specifies EZI2C
		primary 7-bits slave address
		(MSB ignored).
Ezl2cSecondarySlaveAddress	9	When the SCB mode is EZI2C,
,		this parameter specifies EZI2C
		secondary 7-bits slave address
		(MSB ignored).
		Only applicable when EZI2C
		clock stretching option is set.
Ezl2cSubAddressSize	8	When the SCB mode is EZI2C,
		this parameter specifies the
		maximum size of the slave
		buffer that is exposed to the
		master: 8bits – maximum buffer
		size is 256 bytes, 16 bits –
		maximum buffer size is 65535
		bytes.
Ezl2cWakeEnable	false	When the SCB mode is EZI2C,
		this parameter enables wakeup
		from Deep Sleep on I2C
		address match event.



Parameter Name	Value	Description
I2C Bus Voltage	3.3	When the SCB mode is I2C, this parameter specifies the voltage applied to the pull-up resistors on the I2C bus.
		Only applicable for devices other than PSoC 4000/PSoC 4100/PSoC 4200.
I2C Bus Voltage	3.3	When the SCB mode is EZI2C, this parameter specifies the voltage applied to the pull-up resistors on the I2C bus. Only applicable for devices other than PSoC 4000/PSoC 4100/PSoC 4200.
I2cAcceptAddress	false	When the SCB mode is I2C, this parameter specifies whether to accept the match slave address in RX FIFO or not. All slave matched addresses are ACKed. The user has to register the callback function to handle accepted addresses. This feature has to be used when more than one address support is required.
I2cAcceptGeneralCall	false	When the SCB mode is I2C, this parameter specifies whether to accept the general call address. The general call address is ACKed when accepted and NAKed otherwise. The user has to register the callback function to handle the general call address.
I2cByteModeEnable	false	When the SCB mode is I2C, this parameter specifies the number of bits per FIFO data element. The byte mode – false: a 16-bit FIFO data element. The FIFO depth is 8 entries. The byte mode – true: an 8-bit FIFO data element. The FIFO depth is 16 entries. Applicable only for devices other than PSoC 4000/PSoC 4100/PSoC 4200.
I2cClockFromTerm	false	When the SCB mode is I2C, this parameter provides a clock terminal to connect a clock outside the component.
I2cDataRate	100	When the SCB mode is I2C, this parameter specifies the data rate in kbps. The standard data rates are: 100, 400 and 1000 kbps.



Parameter Name	Value	Description
I2cExternIntrHandler	false	When the SCB mode is I2C, this parameter specifies whether the I2C interrupt handler is
		configured in SCB_I2CInit(). This parameter is intended to be used by the PM/SM bus component. The modification
10 M 10	4	parameter default value causes I2C mode failures.
I2cManualOversampleControl	true	When the SCB mode is I2C, this parameter specifies the method of calculating the oversampling as manual or automatic.
I2cMode	Slave	When the SCB mode is I2C, this parameter defines the I2C operation mode as: Slave, Master, Multi-Master or Multi-Master-Slave.
I2cOvsFactor	16	When the SCB mode is I2C, this parameter defines the oversampling factor of SCBCLK.
I2cOvsFactorHigh	8	When the SCB mode is I2C, this parameter defines the high oversampling factor of SCBCLK. Only applicable for I2C Master modes.
I2cOvsFactorLow	8	When the SCB mode is I2C, this parameter defines the low oversampling factor of SCBCLK. Only applicable for I2C Master modes.
I2cSlaveAddress	8	When the SCB mode is I2C, this parameter specifies the I2C 7-bits slave address (MSB ignored).
I2cSlaveAddressMask	254	When the SCB mode is I2C, this parameter specifies the I2C Slave address mask. Bit value 0 – excludes bit from address comparison. Bit value 1 – the bit needs to match with the corresponding bit of the I2C slave address.
I2cWakeEnable	false	When the SCB mode is I2C, this parameter enables wakeup from Deep Sleep on an I2C address match event.
ScbMisoSdaTxEnable	true	This parameter defines the availability of the spi_miso_i2csda_uart_tx pin.
ScbMode	UART	This parameter defines the mode of operation for the SCB component.
ScbMosiSclRxEnable	true	This parameter defines the availability of the spi_mosi_i2cscl_uart_rx pin.



Parameter Name	Value	Description Description
ScbRxWakeIrqEnable	false	This parameter defines the
· ·		availability of the spi_mosi_i2c
		scl_uart_rx_wake pin.
ScbSclkEnable	false	This parameter defines the
		availability of the sclk pin.
ScbSs0Enable	false	This parameter defines the
		availability of the ss0 pin.
ScbSs1Enable	false	This parameter defines the
		availability of the ss1 pin.
ScbSs2Enable	false	This parameter defines the
		availability of the ss2 pin.
ScbSs3Enable	false	This parameter defines the
		availability of the ss3 pin.
Show EZI2C Terminals	false	When the SCB mode is EZI2C,
		this parameter removes internal
		pins and expose signals to
		terminals. The exposed
		terminals must be connected to
Show I2C Terminals	false	the pins.
Show ize reminals	laise	When the SCB mode is I2C, this parameter removes internal pins
		and expose signals to terminals.
		The exposed terminals must be
		connected to the pins.
Show SPI Terminals	false	When the SCB mode is SPI,
		this parameter removes internal
		pins and expose signals to
		terminals. The exposed
		terminals must be connected to
		the pins or SmartIO component.
Show UART Terminals	false	When the SCB mode is UART,
		this parameter removes internal
		pins and expose signals to
		terminals. The exposed terminals must be connected to
		the pins or SmartIO component.
Slew Rate	Fast	When the SCB mode is EZI2C,
Siew Nate	rasi	this parameter specifies the
		slew rate settings of the I2C
		pins.
		For devices supporting GPIO
		Over-Voltage Tolerance
		(GPIO_OVT) pins, I2C FM+
		options should be used when
		I2C data rate is greater than
		400 kbps. This option also
		requires the I2C bus voltage to
		be defined.Refer to the Device
		Datasheet to determine which pins are GPIO OVT capable.
		pins are GriO_Ovi Capable.



Parameter Name	Value	Description
Slew Rate	Fast	When the SCB mode is I2C, this
Sion reads	1 401	parameter specifies the slew
		rate settings of the I2C pins.
		For devices supporting GPIO
		Over-Voltage Tolerance
		(GPIO_OVT) pins, I2C FM+
		options should be used when
		I2C data rate is greater than
		400 kbps. This option also
		requires the I2C bus voltage to
		be defined. Refer to the Device
		Datasheet to determine which
		pins are GPIO_OVT capable.
SpiBitRate	1000	When the SCB mode is SPI,
'		this parameter specifies the Bit
		rate in kbps (up to 8000 kbps);
		the actual rate may differ based
		on available clock frequency
		and component settings. This
		parameter has no effect if the
		Clock from terminal parameter
		is enabled.
SpiBitsOrder	MSB First	When the SCB mode is SPI,
·		this parameter defines the bit
		order as: MSB first or LSB first.
SpiByteModeEnable	false	When the SCB mode is SPI,
		this parameter specifies the
		number of bits per FIFO data
		element.
		The byte mode – false: a 16-bit
		FIFO data element. The FIFO
		depth is 8 entries.
		The byte mode – true: an 8-bit
		FIFO data element. The FIFO
		depth is 16 entries.
		Applicable only for devices
		other than PSoC 4000/PSoC
		4100/PSoC 4200.
SpiClockFromTerm	false	When the SCB mode is SPI,
		this parameter provides a clock
		terminal to connect a clock
		outside the component.
SpiFreeRunningSclk	false	When the SCB mode is SPI,
		this parameter specifies the
		SCLK generation by the master
		as: gated or free running
		(continuous).
		Applicable only for devices
		other than PSoC 4000/PSoC
		4100/PSoC 4200.



Parameter Name	Value	Description Description
SpilnterruptMode	None	When the SCB mode is SPI, this parameter specifies the interrupt mode. None: Removes all interrupt support. Internal: Leaves the interrupt SCBIRQ inside the component - the interrupt terminal becomes invisible. External: Provides an interrupt terminal to connect an interrupt outside the component.
SpiIntrMasterSpiDone	false	When the SCB mode is SPI, this parameter enables the SCB.INTR_M. SPI_DONE interrupt source. SCB.INTR_M. SPI_DONE: all data are sent into TX FIFO and the TX FIFO and the TX FIFO and the TX FIFO and solution of the TX FIFO and the Shifter register are emptied. Only applicable for SPI Master mode.
SpiIntrRxFull	false	When the SCB mode is SPI, this parameter enables the SCB.INTR_RX.FULL interrupt source. SCB.INTR_RX.FULL trigger condition: RX FIFO is full.
SpiIntrRxNotEmpty	false	When the SCB mode is SPI, this parameter enables the SCB.INTR_RX.NOT_EMPTY interrupt source. SCB.INTR_RX.NOT_EMPTY trigger condition: RX FIFO is not empty. There is at least one entry to get data from.
SpiIntrRxOverflow	false	When the SCB mode is SPI, this parameter enables the SCB.INTR_RX.OVERFLOW interrupt source. SCB.INTR_RX.OVERFLOW trigger condition: attempt to write to a full RX FIFO.
SpiIntrRxTrigger	false	When the SCB mode is SPI, this parameter enables the SCB.INTR_RX.TRIGGER interrupt source. SCB.INTR_RX.TRIGGER trigger condition: remains active until RX FIFO has more entries than the value specified by SpiRxTriggerLevel.
SpiIntrRxUnderflow	false	When the SCB mode is SPI, this parameter enables the SCB.INTR_RX.UNDERFLOW interrupt source. SCB.INTR_RX.UNDERFLOW trigger condition: attempt to read from an empty RX FIFO.



Parameter Name	Value	Description
SpiIntrSlaveBusError	false	When the SCB mode is SPI, this parameter enables the SCB.INTR_SLAVE.BUSERROR interrupt source. SCB.INTR_SLAVE.BUSERROR trigger condition: slave select line is deselected at an unexpected time in the SPI transfer. Only applicable for SPI Slave mode.
SpilntrTxEmpty	false	When the SCB mode is SPI, this parameter enables the SCB.INTR_TX.EMPTY interrupt source. SCB.INTR_TX.EMPTY trigger condition: TX FIFO is empty.
SpiIntrTxNotFull	false	When the SCB mode is SPI, this parameter enables the SCB.INTR_TX.NOT_FULL interrupt source. SCB.INTR_TX.NOT_FULL trigger condition: TX FIFO is not full. There is at least one entry to put data.
SpiIntrTxOverflow	false	When the SCB mode is SPI, this parameter enables the SCB.INTR_TX.OVERFLOW interrupt source. SCB.INTR_TX.OVERFLOW trigger condition: attempt to write to a full TX FIFO.
SpilntrTxTrigger	false	When the SCB mode is SPI, this parameter enables the SCB.INTR_TX.TRIGGER interrupt source. SCB.INTR_TX.TRIGGER trigger condition: remains active until TX FIFO has fewer entries than the value specified by SpiTxTriggerLevel.
SpilntrTxUnderflow	false	When the SCB mode is SPI, this parameter enables the SCB.INTR_TX.UNDERFLOW interrupt source. SCB.INTR_TX.UNDERFLOW trigger condition: attempt to read from an empty TX FIFO.
SpiLateMisoSampleEnable	false	When the SCB mode is SPI, this parameter enables late sampling of the MISO line by the master.
SpiMedianFilterEnable	false	When the SCB mode is SPI, this parameter applies a digital 3 tap median filter to the SPI input line.



SpiNumberOfRxDataBits Slave When the SCB mode is SPI, this parameter selects SPI mode of operation as: Slave or Master.		1	EMBEDDED IN TO
this parameter selects SPI mode of operation as: Slave or Master. SpiNumberOfRxDataBits 8 When the SCB mode is SPI, this parameter specifies the number of data bits inside the SPI byte/word for RX direction. SpiNumberOfSelectLines 1 When the SCB mode is SPI, this parameter defines the number of slave select lines. The SPI Slave has only one slave select line. The SPI Master has up to 4 lines. SpiNumberOfTxDataBits 8 When the SCB mode is SPI, this parameter define the number of data bits inside the SPI byte/word for TX direction. SpiOvsFactor 16 When the SCB mode is SPI, this parameter define the number of data bits inside the SPI byte/word for TX direction. SpiRemoveMiso false When the SCB mode is SPI, this parameter defines the oversampling factor of SCBCLK. SpiRemoveMosi false When the SCB mode is SPI, this parameter removes the MISO pin. SpiRemoveSclk false When the SCB mode is SPI, this parameter removes the MOSI pin. SpiRemoveSclk false When the SCB mode is SPI, this parameter removes the MOSI pin. SpiRxBufferSize 8 When the SCB mode is SPI, this parameter removes the SCLK pin. SpiRxBufferSize 8 When the SCB mode is SPI, this parameter removes the Nosi parameter removes the Scilk pin. SpiRxBufferSize 7 When the SCB mode is SPI, this parameter defines the size of the RX buffer. SpiRxTriggerLevel 7 When the SCB mode is SPI, this parameter defines the size of the RX buffer. SpiRxTriggerLevel 7 When the SCB mode is SPI, this parameter defines the size of the RX trigger output terminal of the component. This terminal must be connected to the DMA input trigger or left unconnected. Only applicable or devices which have a DMA controller. SpiRxTriggerLevel 7 When the SCB mode is SPI, this parameter defines the serial clock phase (CPHA) and polarity (CPOL). SpiSsOPolarity Active Low When the SCB mode is SPI, this parameter defines the serial clock phase (CPHA) and polarity (CPOL). Applicable only for devices other than PSoC 4000/PSoC	Parameter Name	Value	Description
SpiNumberOfRxDataBits 8	SpiMode	Slave	•
SpiNumberOfRxDataBits SpiNumberOfRxDataBits SpiNumberOfRxDataBits SpiNumberOfRxDataBits SpiNumberOfSelectLines SpiNumberOfSelectLines SpiNumberOfSelectLines SpiNumberOfSelectLines SpiNumberOfSelectLines SpiNumberOfSelectLines SpiNumberOfSelectLines SpiNumberOfSelectLines SpiNumberOfTxDataBits SpiNumberOfTxDataBit			1
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other than PSoC 4000/PSoC			
4100/PSoC 4200.			
			4100/PSoC 4200.



Parameter Name	Value	Description
SpiSs1Polarity	Active Low	When the SCB mode is SPI,
		this parameter specifies active
		polarity of slave select 1.
		Applicable only for devices
		other than PSoC 4000/PSoC
		4100/PSoC 4200.
SpiSs2Polarity	Active Low	When the SCB mode is SPI,
		this parameter specifies active
		polarity of slave select 2.
		Applicable only for devices
		other than PSoC 4000/PSoC
		4100/PSoC 4200.
SpiSs3Polarity	Active Low	When the SCB mode is SPI,
		this parameter specifies active
		polarity of slave select 3.
		Applicable only for devices
		other than PSoC 4000/PSoC
		4100/PSoC 4200.
SpiSubMode	Motorola	When the SCB mode is SPI,
		this parameter defines the sub
		mode of the SPI as: Motorola,
		TI(Start Coincides), TI(Start
		Precedes), or National
Ou 'Town for Our word' or	0	Semiconductor.
SpiTransferSeparation	Continuous	When the SCB mode is SPI,
		this parameter defines the type of SPI transfers separation as:
		continuous or separated.
SpiTxBufferSize	8	When the SCB mode is SPI,
Oprividancioize		this parameter defines the size
		of the TX buffer.
SpiTxOutputEnable	false	When the SCB mode is SPI,
	.555	this parameter enables the TX
		trigger output terminal of the
		component. This terminal must
		be connected to the DMA input
		trigger or left unconnected. Only
		applicable for devices which
		have a DMA controller.
SpiTxTriggerLevel	0	When the SCB mode is SPI,
		this parameter defines the
		number of entries in the TX
		FIFO to control the SCB.INTR TX.TRIGGER interrupt event or
		TX DMA trigger output.
SpiWakeEnable	false	When the SCB mode is SPI,
'		this parameter enables wakeup
		from Deep Sleep on slave
		select event.



Daramatar Nama	Value	Description EMBEDDED IN TO
Parameter Name	Value	Description
UartByteModeEnable	false	When the SCB mode is UART,
		this parameter specifies the
		number of bits per FIFO data element.
		The byte mode – false: a 16-bit
		FIFO data element. The FIFO
		depth is 8 entries.
		The byte mode – true: an 8-bit FIFO data element. The FIFO
		depth is 16 entries.
		Applicable only for devices
		other than PSoC 4000/PSoC
		4100/PSoC 4200.
LlautClaul/EngineTaura	foloo	
UartClockFromTerm	false	When the SCB mode is UART,
		this parameter provides a clock
		terminal to connect a clock
		outside the component.
UartCtsEnable	false	When the SCB mode is UART,
		this parameter enables the cts
		input.
		Outrandiashla fan dariasa
		Only applicable for devices
		other than PSoC 4000/PSoC
		4100/PSoC 4200.
UartCtsPolarity	Active Low	When the SCB mode is UART,
		this parameter specifies active
		polarity of an input cts signal.
		Only applicable for devices
		Only applicable for devices
		other than PSoC 4000/PSoC
II. (B. (B. (115000	4100/PSoC 4200.
UartDataRate	115200	When the SCB mode is UART,
		this parameter specifies the
		Baud rate in bps (up to 1000
		kbps); the actual rate may differ
		based on available clock
		frequency and component
		settings. This parameter has no
		effect if the Clock from terminal
LlowtDivo ation	TV : DV	parameter is enabled.
UartDirection	TX + RX	When the SCB mode is UART,
		this parameter enables RX or
		TX direction or both
11 15 0.5		simultaneously.
UartDropOnFrameErr	false	When the SCB mode is UART,
		this parameter defines whether
		the data is dropped from RX
		FIFO on a frame error event.
UartDropOnParityErr	false	When the SCB mode is UART,
		this parameter determines
		whether the data is dropped
		from RX FIFO on a parity error
		event.
		L



Parameter Name	Value	Description
UartInterruptMode	Internal	When the SCB mode is UART, this parameter specifies the interrupt mode. None: Removes all interrupt support. Internal:
		Leaves the interrupt SCBIRQ inside the component - the interrupt terminal becomes invisible. External: Provides an
		interrupt terminal to connect an interrupt outside component.
UartIntrRxBreakDetected	false	This parameter enables the RX break detection interrupt source to trigger the interrupt output.
UartIntrRxFrameErr	false	When the SCB mode is UART, this parameter enables the SCB.INTR_RX.FRAME ERROR interrupt source. SCB.INTR_RX.FRAME ERROR trigger condition: frame error in received data frame.
UartIntrRxFull	false	When the SCB mode is UART, this parameter enables the SCB.INTR_RX.FULL interrupt source. SCB.INTR_RX.FULL trigger condition: RX FIFO is full.
UartIntrRxNotEmpty	true	When the SCB mode is UART, this parameter enables the SCB.INTR_RX.NOT_EMPTY interrupt source. SCB.INTR_RX.NOT_EMPTY trigger condition: RX FIFO is not empty. There is at least one entry to get data from.
UartIntrRxOverflow	false	When the SCB mode is UART, this parameter enables the SCB.INTR_RX.OVERFLOW interrupt source. SCB.INTR_RX.OVERFLOW trigger condition: attempt to write to a full RX FIFO.
UartIntrRxParityErr	false	When the SCB mode is UART, this parameter enables the SCB.INTR_RX.PARITY ERROR interrupt source. SCB.INTR_RX.PARITY ERROR trigger condition: parity error in received data frame.
UartIntrRxTrigger	false	When the SCB mode is UART, this parameter enables the SCB.INTR_RX.TRIGGER interrupt source. SCB.INTR_RX.TRIGGER trigger condition: remains active until RX FIFO has more entries than the value specified by UartRxTriggerLevel.



		EMBEDDED IN T
Parameter Name	Value	Description
UartIntrRxUnderflow	false	When the SCB mode is UART,
		this parameter enables the
		SCB.INTR_RX.UNDERFLOW
		interrupt source.
		SCB.INTR_RX.UNDERFLOW
		trigger condition: attempt to
		read from an empty RX FIFO.
UartIntrTxEmpty	false	When the SCB mode is UART,
		this parameter enables the
		SCB.INTR_TX.EMPTY interrupt
		Source.
		SCB.INTR_TX.EMPTY trigger
LL ALVANTANI AFAU	£ . 1	condition: TX FIFO is empty.
UartIntrTxNotFull	false	When the SCB mode is UART,
		this parameter enables the
		SCB.INTR_TX.NOT_FULL
		interrupt source.
		SCB.INTR_TX.NOT_FULL trigger condition: TX FIFO is not
		full. There is at least one entry
		to put data.
UartIntrTxOverflow	false	When the SCB mode is UART,
Oartifiti (XOVerflow	laise	this parameter enables the
		SCB.INTR TX.OVERFLOW
		interrupt source.
		SCB.INTR_TX.OVERFLOW
		trigger condition: attempt to
		write to a full TX FIFO.
UartIntrTxTrigger	false	When the SCB mode is UART,
Carama (X1119go)	laico	this parameter enables the
		SCB.INTR TX.TRIGGER
		interrupt source.
		SCB.INTR TX.TRIGGER
		trigger condition: remains active
		until TX FIFO has fewer entries
		than the value specified by
		UartTxTriggerLevel.
UartIntrTxUartDone	true	When the SCB mode is UART,
		this parameter enables the
		SCB.INTR_TX.UART_DONE
		interrupt source.
		SCB.INTR_TX.UART_DONE
		trigger condition: all data are
		sent in to TX FIFO and the
		transmit FIFO and the shifter
		register are emptied.
UartIntrTxUartLostArb	false	When the SCB mode is UART,
		this parameter enables the
		SCB.INTR_TX.UART_ARB
		LOST interrupt source.
		SCB.INTR_TX.UART_ARB LOST trigger condition: UART
		lost arbitration, the value driven
		on the TX line is not the same
		as the value observed on the
		RX line. This event is useful
		when the transmitter and the
		receiver share a TX/RX line.
		Only applicable for UART
		SmartCard mode.
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Parameter Name	Value	Description
UartIntrTxUartNack	false	When the SCB mode is UART,
		this parameter enables the
		SCB.INTR_TX.UART_NACK
		interrupt source. SCB.INTR_TX.UART_NACK
		trigger condition: UART
		transmitter received a negative
		acknowledgement. o
		Only applicable for UART
		SmartCard mode.
UartIntrTxUnderflow	false	When the SCB mode is UART,
		this parameter enables the SCB.INTR TX.UNDERFLOW
		interrupt source.
		SCB.INTR TX.UNDERFLOW
		trigger condition: attempt to
		read from an empty TX FIFO.
UartIrdaLowPower	false	When the SCB mode is UART,
		this parameter enables the low
		power receiver option. Only applicable for UART IrDA
		mode.
UartIrdaPolarity	Non-Inverting	When the SCB mode is UART,
,		this parameter inverts the
		incoming RX line signal.
		Only applicable for UART IrDA
	falsa	mode.
UartMedianFilterEnable	false	When the SCB mode is UART, this parameter applies a digital
		3 tap median filter to the UART
		input line.
UartMpEnable	false	When the SCB mode is UART,
		this parameter enables the
		UART multi-processor mode. Only applicable for UART
		Standard mode.
UartMpRxAcceptAddress	false	When the SCB mode is UART,
Cartivipi (A tocopa taarocc	laico	this parameter define whether to
		put the matched UART address
		into RX FIFO.
		Only applicable for UART multi-
	2	processor mode.
UartMpRxAddress	2	When the SCB mode is UART, this parameter defines the
		UART address.
		Only applicable for UART multi-
		processor mode.
UartMpRxAddressMask	255	When the SCB mode is UART,
		this parameter defines the
		address mask in multi- processor operation mode.
		Bit value 0 – excludes bit from
		address comparison.
		Bit value 1 – the bit needs to
		match with the corresponding
		bit of the UART address.
		Only applicable for UART multi-
		processor mode.



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Parameter Name	Value	Description
UartNumberOfDataBits	8 bits	When the SCB mode is UART,
		this parameter defines the
		number of data bits inside the
	4.1.9	UART byte/word.
UartNumberOfStopBits	1 bit	When the SCB mode is UART,
		this parameter defines the
H-40F-4	40	number of Stop bits.
UartOvsFactor	13	When the SCB mode is UART,
		this parameter defines the
		oversampling factor of SCBCLK.
UartParityType	None	When the SCB mode is UART,
Oaltrailty i ype	None	this parameter applies UART
		parity check as Odd or Even or
		discards the parity entirely.
UartRtsEnable	false	When the SCB mode is UART,
CartitisEriable	laise	this parameter enables the rts
		output.
		output.
		Applicable only for devices
		other than PSoC 4000/PSoC
		4100/PSoC 4200.
UartRtsPolarity	Active Low	When the SCB mode is UART,
		this parameter specifies active
		polarity of the output rts signal.
		Applicable only for devices
		other than PSoC 4000/PSoC
		4100/PSoC 4200.
UartRtsTriggerLevel	4	When the SCB mode is UART,
		this parameter specifies the
		number of entries in the RX
		FIFO to activate the rts output
		signal. When the receiver FIFO
		has fewer entries than the
		UartRtsTriggerLevel, an rts output signal is activated.
		output signal is activated.
		Applicable only for devices
		other than PSoC 4000/PSoC
		4100/PSoC 4200.
UartRxBreakWidth	11	This parameter specifies the
		break width in bits.
UartRxBufferSize	8	When the SCB mode is UART,
		this parameter defines the size
		of the RX buffer.
UartRxOutputEnable	false	When the SCB mode is UART,
		this parameter enables the RX
		trigger output terminal of the
		component. This terminal must
		be connected to the DMA input
		trigger or left unconnected. Only
		applicable for devices which
		have a DMA controller.



Parameter Name	Value	Description
UartRxTriggerLevel	7	When the SCB mode is UART, this parameter defines the number of entries in the RX FIFO to trigger control the
		SCB.INTR_RX.TRIGGER interrupt event or RX DMA trigger output.
UartSmCardRetryOnNack	false	When the SCB mode is UART, this parameter defines whether to send a message again when a NACK response is received. Only applicable for UART SmartCard mode.
UartSubMode	Standard	When the SCB mode is UART, this parameter defines the sub mode of UART as: Standard, SmartCard or IrDA.
UartTxBufferSize	8	When the SCB mode is UART, this parameter defines the size of the TX buffer.
UartTxOutputEnable	false	When the SCB mode is UART, this parameter enables the TX trigger output terminal of the component. This terminal must be connected to the DMA input trigger or left unconnected. Only applicable for devices which have a DMA controller.
UartTxTriggerLevel	0	When the SCB mode is UART, this parameter defines the number of entries in the TX FIFO to control the SCB.INTRTX.TRIGGER interrupt event or TX DMA trigger output.
UartWakeEnable	true	When the SCB mode is UART, this parameter enables the wakeup from Deep Sleep on start bit event. The actual wakeup source is RX GPIO. The skip start UART feature allows it to continue receiving bytes.
User Comments		Instance-specific comments.



10 Other Resources

The following documents contain important information on Cypress software APIs that might be relevant to this design:

- Standard Types and Defines chapter in the <u>System Reference Guide</u>
 - Software base types
 - Hardware register types
 - Compiler defines
 - Cypress API return codes
 - Interrupt types and macros
- Registers
 - o The full PSoC 4 register map is covered in the PSoC 4 Registers Technical Reference
 - o Register Access chapter in the System Reference Guide

 - § CY_GET API routines§ CY_SET API routines
- System Functions chapter in the **System Reference Guide**
 - o General API routines
 - o CyDelay API routines
 - o CyVd Voltage Detect API routines
- Power Management
 - o Power Supply and Monitoring chapter in the PSoC 4 Technical Reference Manual
 - o Low Power Modes chapter in the PSoC 4 Technical Reference Manual
 - o Power Management chapter in the System Reference Guide
 - § CyPm API routines
- Watchdog Timer chapter in the **System Reference Guide**
 - CyWdť API routinės