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#### Title: TOP

ID: ASX00049

Version: V1.1

Date: 25/10/2023

Time: 9:44:26

Sheet 1 of 10

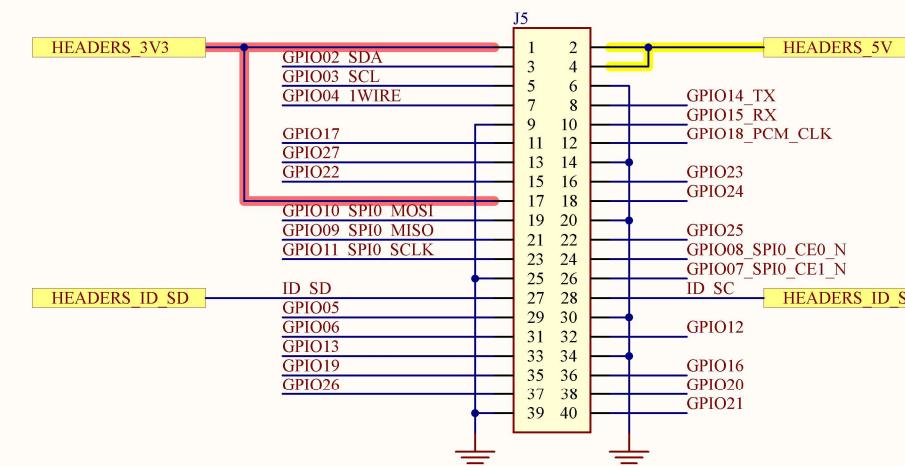
File: TOP.SchDoc

Author: Silvio Navaretti

RevAuthor: Silvio Navaretti



A



GPIO02_SDA	GPIO02_SDA
GPIO03_SCL	GPIO03_SCL
GPIO04_IWIRE	GPIO04_IWIRE
GPIO05	GPIO05
GPIO06	GPIO06
GPIO07_SPI0_CE1_N	GPIO07_SPI0_CE1_N
GPIO08_SPI0_CE0_N	GPIO08_SPI0_CE0_N
GPIO09_SPI0_MISO	GPIO09_SPI0_MISO
GPIO10_SPI0_MOSI	GPIO10_SPI0_MOSI
GPIO11_SPI0_SCLK	GPIO11_SPI0_SCLK
GPIO12	GPIO12
GPIO13	GPIO13
GPIO14_TX	GPIO14_TX
GPIO15_RX	GPIO15_RX
GPIO16	GPIO16
GPIO17	GPIO17
GPIO18_PCM_CLK	GPIO18_PCM_CLK
GPIO19	GPIO19
GPIO20	GPIO20
GPIO21	GPIO21
GPIO22	GPIO22
GPIO23	GPIO23
GPIO24	GPIO24
GPIO25	GPIO25
GPIO26	GPIO26
GPIO27	GPIO27

HEADERS\_GPIO

HEADERS\_GPIO

B

C

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## Title: RASP HEADERS

ID: ASX00049

Version: V1.1



Date: 25/10/2023 Time: 9:44:28

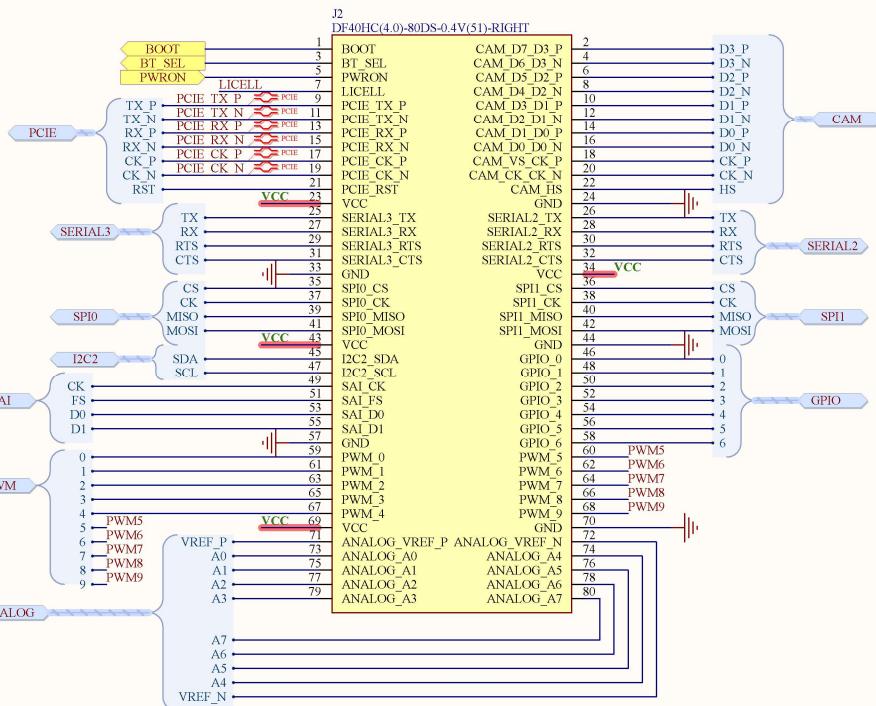
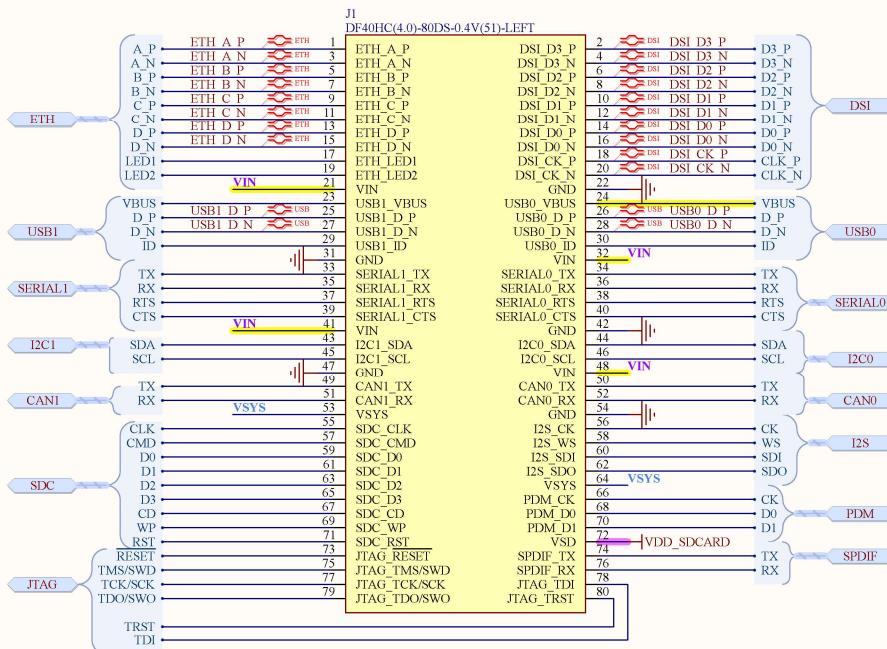
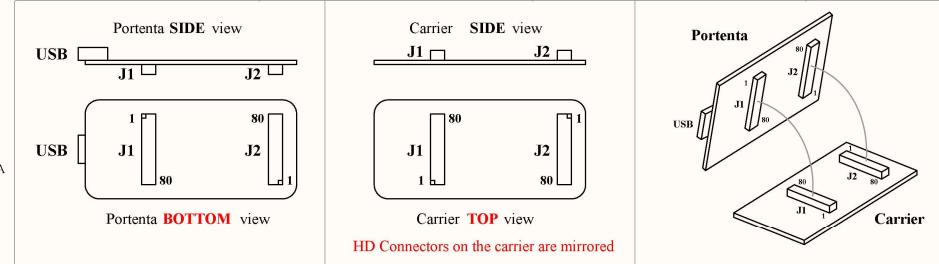
Sheet 2 of 10

File: Headers.SchDoc

Author: Silvio Navaretti

RevAuthor: Silvio Navaretti





#### SHARED PINS TABLE

NET	BUS 1	BUS 2
PB3	JTAG	SDC2
PH11	CAM	I2C4
PH12	CAM	I2C4
PI5	CAM	SA12A
PI6	CAM	SA12A
PI7	CAM	SA12A
PA4	CAM	ANALOG
PA6	CAM	ANALOG
PC2	ANALOG	ANALOG
PC3	ANALOG	ANALOG

#### POWER NETS TABLE

NET	TYPE	RANGES	DESCRIPTION
VIN	PORTENTA INPUT	4.1V to 6V.	Default 3.3V, PMIC (U10) programmable output.
VCC	PORTENTA OUTPUT	1.1V to 3.3V in steps, max 1A.	Default 3.3V, PMIC (U10) programmable output.
VSYS	PORTENTA RESERVED OUTPUT	RESERVED, DO NOT USE	Default 4.2V, PMIC (U10) programmable output which is also the input voltage of the buck inside the PMIC itself.
LICELL	PORTENTA INPUT	Coine cell max 3.6V, max 46uA.	Max 4uA with PMIC (U10) in coin cell mode, max 46uA with PMIC in standby/suspend mode.

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#### Title: HD Connectors female

ID: ASX0049

Version: V1.1



Date: 25/10/2023 Time: 9:44:29

Sheet 3 of 10

File: HDConn\_FIRMWARE.SchDoc

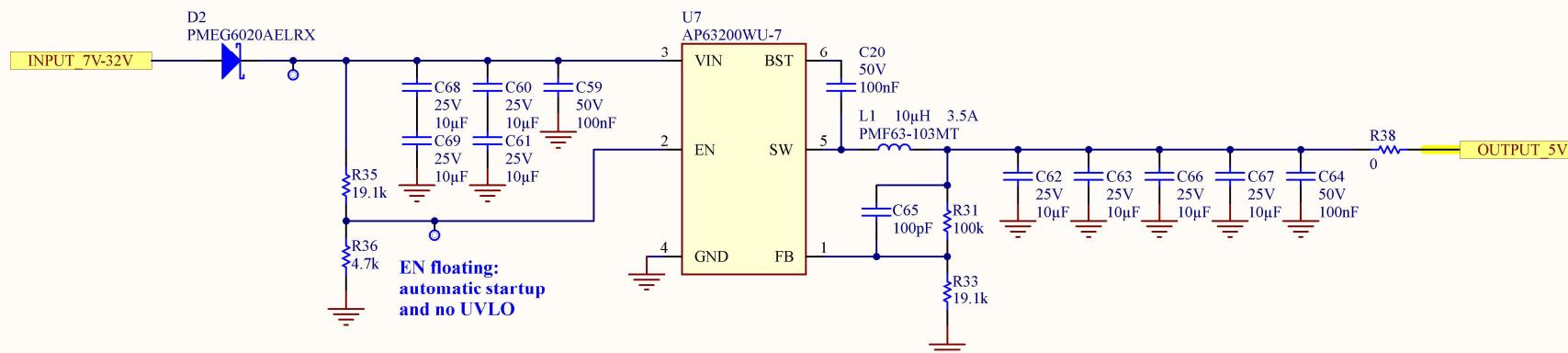
Author: Silvio Navaretti

RevAuthor:

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**5V STEP DOWN  
VIN MAX 32V  
MAX OUT CURRENT 1.5A  
REVERSE POLARITY PROTECTION**



B

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Title: POWER EXTERNAL

ID: ASX00049

Version: V1.1



Date: 25/10/2023 Time: 9:44:31

Sheet 4 of 10

File: DCDC\_CONVERTER.SchDoc

Author: Silvio Navaretti

RevAuthor: Silvio Navaretti

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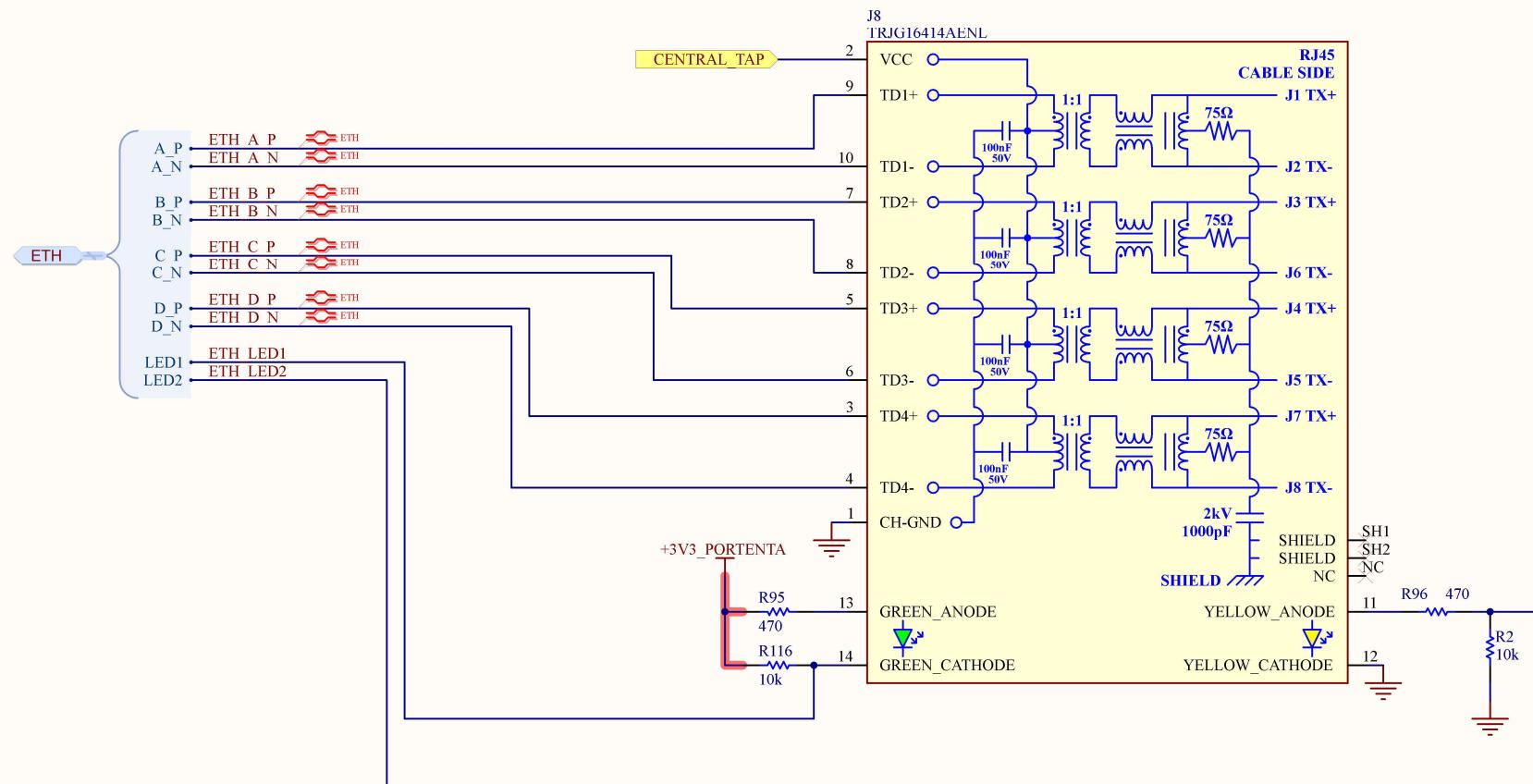
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### Title: ETHERNET

ID: ASX00049

Version: V1.1



Date: 25/10/2023 Time: 9:44:32

Sheet 5 of 10

File: ETH\_CONNECTOR.SchDoc

Author: Silvio Navaretti

RevAuthor: Silvio Navaretti

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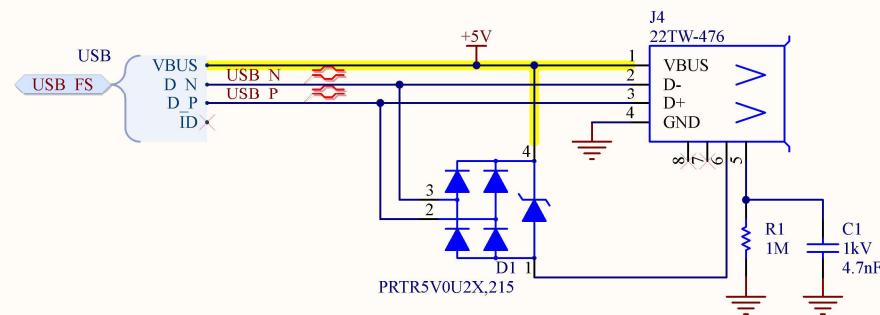
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Title: **USB**

ID: ASX00049

Version: V1.1



Date: 25/10/2023 Time: 9:44:34

Sheet 6 of 10

File: [USB.SchDoc](#) Author: Silvio Navaretti RevAuthor: Silvio Navaretti

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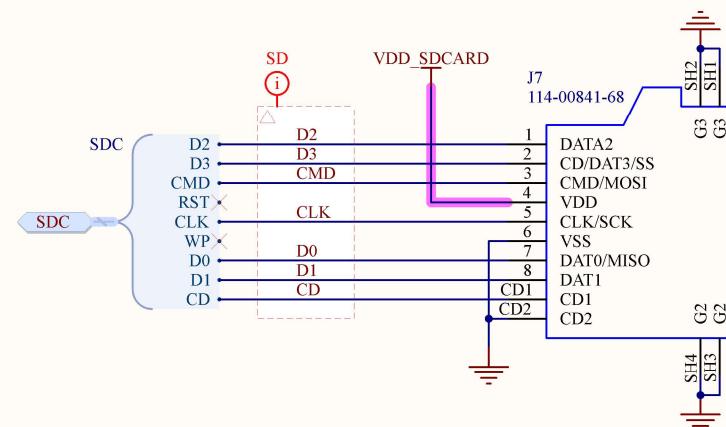
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#### Title: SD card

ID: ASX00049

Version: V1.1



Date: 25/10/2023

Time: 9:44:35

Sheet 7 of 10

File: SDcard.SchDoc

Author: Silvio Navaretti

RevAuthor: Silvio Navaretti

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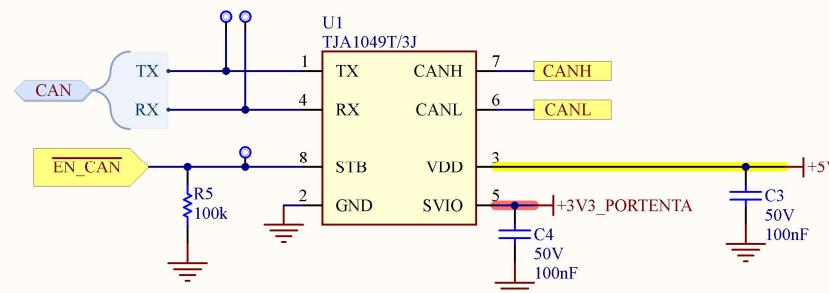
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### Title: CAN PHY

ID: ASX00049

Version: V1.1



Date: 25/10/2023 Time: 9:44:37

Sheet 8 of 10

File: CAN\_PHY.SchDoc

Author: Silvio Navaretti

RevAuthor: Silvio Navaretti

A

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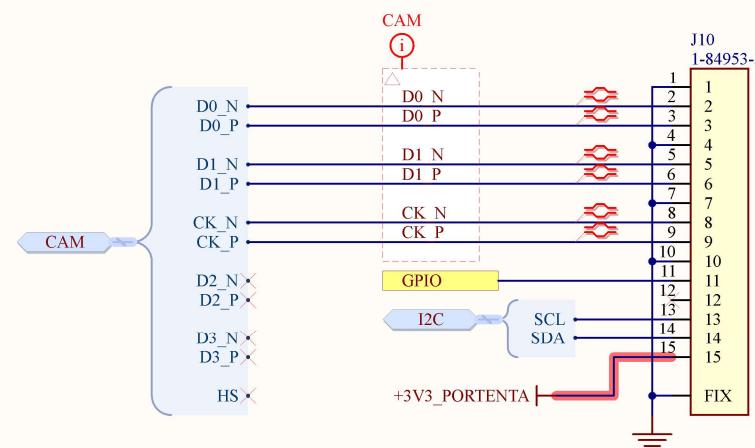
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Title: **CAMERA**

ID: ASX00049

Version: V1.1



Date: 25/10/2023 Time: 9:44:38

Sheet 9 of 10

File: CAMERA.SchDoc Author: Silvio Navaretti

RevAuthor: Silvio Navaretti

A

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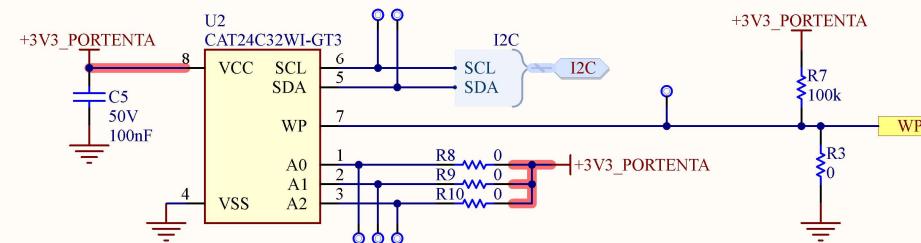
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CAT24C32WI-GT3 address bits

1	0	1	0	A2	A1	A0	R/W
---	---	---	---	----	----	----	-----

A2, A1, A0 can be pulled HIGH or LOW.  
They have an internal pulldown.

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Title: EEPROM

ID: ASX00049

Version: V1.1



Date: 25/10/2023 Time: 9:44:40

Sheet 10 of 10

File: EEPROM.SchDoc

Author: Silvio Navaretti

RevAuthor: Silvio Navaretti