HW/SW Co-Design, MEEC 2018/19

PROJECT SUGGESTION

Design proposals by the students are welcome, but must be formally accepted by the Professor.

 (CNN) Convolutional Neural Network image classification of handwritten digits. http://neuralnetworksanddeeplearning.com/chap6.html http://yann.lecun.com/exdb/mnist/

1st part: 5×5 image convolution of images from the MNIST data set (28×28 grayscale images of handwritten digits).

The elements of the convolution kernel will be integers.

2nd part: classification of images from the MNIST data set

Baseline trained network will be provided (at the Support Material web page).

The network weights will be single precision floating-point.

DATA INPUT/OUTPUT

The projects will be demonstrated by initializing the external memory with the appropriate input data and by calculating the data results.

The design performance will be evaluated by measuring the total processing time of the algorithm, starting from the first read of input data from the external memory and ending when all the resulting data is written (back to the external memory).

PROJECT SCHEDULE

The project will be implemented in two phases.

1st project: HW / SW co-processing architecture ~ 5 weeks (40%)

Embedded uniprocessor with (simpler) hardware accelerator (using GP).

Must demonstrate application functionality (simpler processing) and verification competences (HW IP simulation and Integrated Logic Analysis), and evaluate performance.

- Base application: compute the convolution as an integer matrix multiplication.
 - o Milestone 1: demonstrate working software-only application on the 2nd week.
 - Milestone 2: demonstrate HW/SW application using the axis_macc IP connected to the GP port.
- Simple optimization of the HW/SW application (software or/and hardware component).

2nd project: Multiprocessor system in a FPGA ~ 5 weeks (50%)

- Embedded (heterogeneous) multiprocessor(s) with hardware accelerator(s).
- Must demonstrate functionality and show parallelization/hardware acceleration.

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