F1C200s User Manual

Revision 1.2

Jul.22,2019

Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

Declaration

THIS DOCUMENTATION IS THE ORIGINAL WORK AND COPYRIGHTED PROPERTY OF ALLWINNER TECHNOLOGY (“ALLWINNER”). REPRODUCTION IN WHOLE OR IN PART MUST OBTAIN THE WRITTEN APPROVAL OF ALLWINNER AND GIVE CLEAR ACKNOWLEDGMENT TO THE COPYRIGHT OWNER.

THE INFORMATION FURNISHED BY ALLWINNER IS BELIEVED TO BE ACCURATE AND RELIABLE. ALLWINNER RESERVES THE RIGHT TO MAKE CHANGES IN CIRCUIT DESIGN AND/OR SPECIFICATIONS AT ANY TIME WITHOUT NOTICE. ALLWINNER DOES NOT ASSUME ANY RESPONSIBILITY AND LIABILITY FOR ITS USE. NOR FOR ANY INFRINGEMENTS OF PATENTS OR OTHER RIGHTS OF THE THIRD PARTIES WHICH MAY RESULT FROM ITS USE. NO LICENSE IS GRANTED BY IMPLICATION OR OTHERWISE UNDER ANY PATENT OR PATENT RIGHTS OF ALLWINNER. THIS DOCUMENTATION NEITHER STATES NOR IMPLIES WARRANTY OF ANY KIND, INCLUDING FITNESS FOR ANY PARTICULAR APPLICATION.

THIRD PARTY LICENSES MAY BE REQUIRED TO IMPLEMENT THE SOLUTION/PRODUCT. CUSTOMERS SHALL BE SOLELY RESPONSIBLE TO OBTAIN ALL APPROPRIATELY REQUIRED THIRD PARTY LICENSES. ALLWINNER SHALL NOT BE LIABLE FOR ANY LICENSE FEE OR ROYALTY DUE IN RESPECT OF ANY REQUIRED THIRD PARTY LICENSE. ALLWINNER SHALL HAVE NO WARRANTY, INDEMNITY OR OTHER OBLIGATIONS WITH RESPECT TO MATTERS COVERED UNDER ANY REQUIRED THIRD PARTY LICENSE.

 Copyright ©2019 Allwinner Technology Co., Ltd. All Rights Reserved

Revision History

Revision	Date	Description
1.0	Apr.18,2017	Initial Release Version.
1.1	Dec.25,2017	Update video decoding features in Section 2.5.
1.2	Jul.22,2019	Update EP numbers in Section 7.7.

 Copyright ©2019 Allwinner Technology Co., Ltd. All Rights Reserved

Table of Contents

Declaration 2

Revision History 3

Table of Contents 4

Chapter 1. About This Documentation 36

1.1. Documentation Overview 36

Chapter 2. Overview 37

2.1. Processor Features 38

2.1.1. CPU Architecture 38

2.2. Memory Subsystem 38

2.2.1. Boot ROM 38

2.2.2. SDRAM 38

2.2.3. SD/MMC Interface 38

2.3. System Peripheral 38

2.3.1. Timer 38

2.3.2. INTC 39

2.3.3. CCU 39

2.3.4. DMA 39

2.3.5. PWM 39

2.4. Display Subsystem 39

2.4.1. Display Engine 39

2.4.2. Display Output 39

 Copyright ©2019 Allwinner Technology Co., Ltd. All Rights Reserved

2.5. Video Engine 40
2.6. Image Subsystem 40
2.6.1. CSI 40
2.6.2. CVBS Input 40
2.7. Audio Subsystem 40
2.7.1. Audio Codec 40
2.8. Interfaces 40
2.8.1. USB 2.0 OTG 41
2.8.2. KEYADC 41
2.8.3. TP 41
2.8.4. Digital Audio Interface 41
2.8.5. UART 41
2.8.6. SPI 41
2.8.7. TWI 42
2.8.8. CIR 42
2.8.9. RSB™ 42
2.8.10. OWA 42
2.9. Package 42
2.10. System Block Diagram 43
Chapter 3. System 44
3.1. Memory Mapping 45
3.2. CCU 46
3.2.1. Overview 46
3.2.2. Feature 46

 Copyright ©2019 Allwinner Technology Co., Ltd. All Rights Reserved

3.2.3. Functionalities Description 46
3.2.3.1. System Bus 46
3.2.3.2. Bus clock tree 47
3.2.4. CCU Register List 47
3.2.5. CCU Register Description 48
3.2.5.1. PLL_CPU Control Register 48
3.2.5.2. PLL_AUDIO Control Register 49
3.2.5.3. PLL_VIDEO Control Register 50
3.2.5.4. PLL_VE Control Register 51
3.2.5.5. PLL_DDR Control Register 52
3.2.5.6. PLL_PERIPH Control Register 52
3.2.5.7. CPU Clock Source Register 53
3.2.5.8. AHB/APB/HCLKC Configuration Register 54
3.2.5.9. Bus Clock Gating Register 0 55
3.2.5.10. Bus Clock Gating Register 1 55
3.2.5.11. Bus Clock Gating Register 2 56
3.2.5.12. SDMMC0 Clock Register 58
3.2.5.13. SDMMC1 Clock Register 58
3.2.5.14. DAUDIO Clock Register 59
3.2.5.15. OWA Clock Register 59
3.2.5.16. CIR Clock Register 60
3.2.5.17. USBPHY Clock Register 60
3.2.5.18. DRAM Gating Register 60
3.2.5.19. BE Clock Register 61

 Copyright ©2019 Allwinner Technology Co., Ltd. All Rights Reserved

3.2.5.20. FE Clock Register 62
3.2.5.21. TCON Clock Register 62
3.2.5.22. De-interlacer Clock Register 62
3.2.5.23. TVE Clock Register 63
3.2.5.24. TVD Clock Register 64
3.2.5.25. CSI Clock Register 64
3.2.5.26. VE Clock Register 65
3.2.5.27. AUDIO CODEC Clock Register 65
3.2.5.28. AVS Clock Register 65
3.2.5.29. PLL Stable Time Register 0 65
3.2.5.30. PLL Stable Time Register 1 65
3.2.5.31. PLL_CPU Bias Register 66
3.2.5.32. PLL_AUDIO Bias Register 66
3.2.5.33. PLL_VIDEO Bias Register 66
3.2.5.34. PLL_VE Bias Register 67
3.2.5.35. PLL_DDR Bias Register 67
3.2.5.36. PLL_PERIPH Bias Register 67
3.2.5.37. PLL_CPU Tuning Register 68
3.2.5.38. PLL_DDR Tuning Register 68
3.2.5.39. PLL_AUDIO Pattern Control Register 69
3.2.5.40. PLL_VIDEO Pattern Control Register 69
3.2.5.41. PLL_DDR Pattern Control Register 70
3.2.5.42. Bus Software Reset Register 0 70
3.2.5.43. Bus Software Reset Register 1 71

 Copyright ©2019 Allwinner Technology Co., Ltd. All Rights Reserved

3.2.5.44. Bus Software Reset Register 2 72
3.2.6. Programming Guidelines 73
3.2.6.1. PLL 73
3.2.6.2. BUS 73
3.3. Timer 74
3.3.1. Overview 74
3.3.2. Feature 74
3.3.3. Functionalities Description 74
3.3.3.1. Typical Applications 74
3.3.3.2. Functional Block Diagram 75
3.3.4. Timer Register List 75
3.3.5. Timer Register Description 76
3.3.5.1. Timer IRQ Enable Register 76
3.3.5.2. Timer IRQ Status Register 76
3.3.5.3. Timer 0 Control Register 77
3.3.5.4. Timer 0 Interval Value Register 78
3.3.5.5. Timer 0 Current Value Register 78
3.3.5.6. Timer 1 Control Register 78
3.3.5.7. Timer 1 Interval Value Register 79
3.3.5.8. Timer 1 Current Value Register 79
3.3.5.9. Timer 2 Control Register 79
3.3.5.10. Timer 2 Interval Value Register 80
3.3.5.11. Timer 2 Current Value Register 80
3.3.5.12. AVS Counter Control Register 81

 Copyright ©2019 Allwinner Technology Co., Ltd. All Rights Reserved

3.3.5.13. AVS Counter 0 Register 81
3.3.5.14. AVS Counter 1 Register 81
3.3.5.15. AVS Counter Divisor Register 82
3.3.5.16. Watchdog IRQ Enable Register 82
3.3.5.17. Watchdog Status Register 82
3.3.5.18. Watchdog Control Register 83
3.3.5.19. Watchdog Configuration Register 83
3.3.5.20. Watchdog Mode Register 83
3.3.6. Programming Guidelines 84
3.3.6.1. Timer 84
3.3.6.2. Watchdog 84
3.4. PWM 85
3.4.1. Overview 85
3.4.2. Feature 85
3.4.3. Functionalities Description 85
3.4.3.1. Functional Block Diagram 85
3.4.4. Operation Principle 86
3.4.4.1. PWM output pins 86
3.4.5. PWM Register List 86
3.4.6. PWM Register Description 86
3.4.6.1. PWM Control Register 86
3.4.6.2. PWM Channel 0 Period Register 88
3.4.6.3. PWM Channel 1 Period Register 89
3.5. INTC 90

 Copyright ©2019 Allwinner Technology Co., Ltd. All Rights Reserved

3.5.1. Overview 90
3.5.2. Feature 90
3.5.3. Functionalities Description 90
3.5.3.1. Functional Block Diagram 90
3.5.4. Interrupt Source 91
3.5.5. INTC Register List 92
3.5.6. INTC Register Description 92
3.5.6.1. Interrupt Vector Register 92
3.5.6.2. Interrupt Base Address Register 93
3.5.6.3. NMI Interrupt Control Register 93
3.5.6.4. Interrupt IRQ Pending Register 0 93
3.5.6.5. Interrupt IRQ Pending Register 1 93
3.5.6.6. Interrupt Enable Register 0 93
3.5.6.7. Interrupt Enable Register 1 93
3.5.6.8. Interrupt Mask Register 0 94
3.5.6.9. Interrupt Mask Register 1 94
3.5.6.10. Interrupt Response Register 0 94
3.5.6.11. Interrupt Response Register 1 94
3.5.6.12. Interrupt Fast Forcing Register 0 94
3.5.6.13. Interrupt Fast Forcing Register 1 95
3.5.6.14. Interrupt Source Priority Register 0 95
3.5.6.15. Interrupt Source Priority Register 1 97
3.5.6.16. Interrupt Source Priority Register 2 100
3.5.6.17. Interrupt Source Priority Register 3 102

 Copyright ©2019 Allwinner Technology Co., Ltd. All Rights Reserved

3.6. DMA 106
3.6.1. Overview 106
3.6.2. Feature 106
3.6.3. Functionalities Description 106
3.6.4. Block diagram 107
3.6.5. Operation Principle 107
3.6.5.1. Address aligned and unaligned 107
3.6.5.2. Clock gating and reset 108
3.6.6. DMA Register List 108
3.6.7. DMA Register Description 108
3.6.7.1. DMA Interrupt Control Register 108
3.6.7.2. DMA Interrupt Status Register 109
3.6.7.3. DMA Priority Configure Register 109
3.6.7.4. Normal DMA Configure Register 110
3.6.7.5. Normal DMA Source Address Register 112
3.6.7.6. Normal DMA Destination Address Register 112
3.6.7.7. Normal DMA Byte Counter Register 112
3.6.7.8. Dedicated DMA Configure Register 112
3.6.7.9. Dedicated DMA Source Address Register 114
3.6.7.10. Dedicated DMA Destination Address Register 114
3.6.7.11. Dedicated DMA Byte Counter Register 115
3.6.7.12. Dedicated DMA Parameter Register 115
3.6.7.13. Dedicated DMA General Data Register 115
3.7. Port Controller 116

 Copyright ©2019 Allwinner Technology Co., Ltd. All Rights Reserved

3.7.1. Overview 116
3.7.2. Port Register List 116
3.7.3. Port Register Description 117
3.7.3.1. PA Configure Register 0 117
3.7.3.2. PA Configure Register 1 117
3.7.3.3. PA Configure Register 2 117
3.7.3.4. PA Configure Register 3 117
3.7.3.5. PA Data Register 118
3.7.3.6. PA Multi-Driving Register 0 118
3.7.3.7. PA Multi-Driving Register 1 118
3.7.3.8. PA Pull Register 0 118
3.7.3.9. PA Pull Register 1 118
3.7.3.10. PB Configure Register 0 118
3.7.3.11. PB Configure Register 1 119
3.7.3.12. PB Configure Register 2 119
3.7.3.13. PB Configure Register 3 119
3.7.3.14. PB Data Register 119
3.7.3.15. PB Multi-Driving Register 0 119
3.7.3.16. PB Multi-Driving Register 1 119
3.7.3.17. PB Pull Register 0 120
3.7.3.18. PB Pull Register 1 120
3.7.3.19. PC Configure Register 0 120
3.7.3.20. PC Configure Register 1 120
3.7.3.21. PC Configure Register 2 121

 Copyright ©2019 Allwinner Technology Co., Ltd. All Rights Reserved

3.7.3.22. PC Configure Register 3 121
3.7.3.23. PC Data Register 121
3.7.3.24. PC Multi-Driving Register 0 121
3.7.3.25. PC Multi-Driving Register 1 121
3.7.3.26. PC Pull Register 0 121
3.7.3.27. PC Pull Register 1 121
3.7.3.28. PD Configure Register 0 122
3.7.3.29. PD Configure Register 1 123
3.7.3.30. PD Configure Register 2 124
3.7.3.31. PD Configure Register 3 125
3.7.3.32. PD Data Register 125
3.7.3.33. PD Multi-Driving Register 0 125
3.7.3.34. PD Multi-Driving Register 1 125
3.7.3.35. PD Pull Register 0 125
3.7.3.36. PD Pull Register 1 126
3.7.3.37. PE Configure Register 0 126
3.7.3.38. PE Configure Register 1 127
3.7.3.39. PE Configure Register 2 128
3.7.3.40. PE Configure Register 3 128
3.7.3.41. PE Data Register 128
3.7.3.42. PE Multi-Driving Register 0 128
3.7.3.43. PE Multi-Driving Register 1 128
3.7.3.44. PE Pull Register 0 128
3.7.3.45. PE Pull Register 1 129

 Copyright ©2019 Allwinner Technology Co., Ltd. All Rights Reserved

3.7.3.46. PF Configure Register 0 129
3.7.3.47. PF Configure Register 1 130
3.7.3.48. PF Configure Register 2 130
3.7.3.49. PF Configure Register 3 130
3.7.3.50. PF Data Register 130
3.7.3.51. PF Multi-Driving Register 0 130
3.7.3.52. PF Multi-Driving Register 1 130
3.7.3.53. PF Pull Register 0 130
3.7.3.54. PD External Interrupt Configure Register 0 131
3.7.3.55. PD External Interrupt Configure Register 1 131
3.7.3.56. PD External Interrupt Configure Register 2 131
3.7.3.57. PD External Interrupt Configure Register 3 132
3.7.3.58. PD External Interrupt Control Register 132
3.7.3.59. PD External Interrupt Status Register 132
3.7.3.60. PD External Interrupt Debounce Register 132
3.7.3.61. PE External Interrupt Configure Register 0 133
3.7.3.62. PE External Interrupt Configure Register 1 133
3.7.3.63. PE External Interrupt Configure Register 2 134
3.7.3.64. PE External Interrupt Configure Register 3 134
3.7.3.65. PE External Interrupt Control Register 134
3.7.3.66. PE External Interrupt Status Register 134
3.7.3.67. PE External Interrupt Debounce Register 134
3.7.3.68. PF External Interrupt Configure Register 0 135
3.7.3.69. PF External Interrupt Configure Register 1 135

 Copyright ©2019 Allwinner Technology Co., Ltd. All Rights Reserved

3.7.3.70. PF External Interrupt Configure Register 2 135
3.7.3.71. PF External Interrupt Configure Register 3 136
3.7.3.72. PF External Interrupt Control Register 136
3.7.3.73. PF External Interrupt Status Register 136
3.7.3.74. PF External Interrupt Debounce Register 136
3.7.3.75. SDRAM Pad Multi-Driving Register 137
3.7.3.76. SDRAM Pad Pull Register 137
Chapter 4. ADC 139
4.1. KEYADC 140
4.1.1. Overview 140
4.1.2. Feature 140
4.1.3. Principle of operation 140
4.1.4. Block diagram 140
4.1.5. KEYADC Register List 141
4.1.6. KEYADC Register Description 141
4.1.6.1. KEYADC Control Register 141
4.1.6.2. KEYADC Interrupt Control Register 142
4.1.6.3. KEYADC Interrupt Status Register 142
4.1.6.4. KEYADC Data Register 143
4.2. TP 144
4.2.1. Overview 144
4.2.2. Feature 144
4.2.3. A/D conversion time 144
4.2.4. Work timing in different mode 144

 Copyright ©2019 Allwinner Technology Co., Ltd. All Rights Reserved

4.2.5. Operation Mode 146
4.2.5.1. Basic principle 146
4.2.5.2. Single-ended mode 146
4.2.5.3. Differential mode 147
4.2.5.4. Single touch detection 147
4.2.5.5. Dual touch detection 148
4.2.5.6. Touch pressure measurement 148
4.2.5.7. Pen down detection, with programmable sensitivity 149
4.2.5.8. Median and averaging filter 150
4.2.6. TP Register List 151
4.2.7. TP Register Description 151
4.2.7.1. TP Control Register 0 151
4.2.7.2. TP Control Register 1 152
4.2.7.3. TP Control Register 2 153
4.2.7.4. TP Control Register 3 154
4.2.7.5. TP Interrupt FIFO Control Register 154
4.2.7.6. TP Interrupt FIFO Status Register 155
4.2.7.7. TP Common Data Register 156
4.2.7.8. TP Data Register 156
4.3. Audio Codec 157
4.3.1. Overview 157
4.3.2. Feature 157
4.3.3. Block diagram 157
4.3.4. Signal Description 157

 Copyright ©2019 Allwinner Technology Co., Ltd. All Rights Reserved

4.3.5. Power Description 158
4.3.6. Function Description 158
4.3.6.1. ADC 158
4.3.6.2. Stereo ADC 158
4.3.6.3. Mixer 158
4.3.6.4. Headphone Mixer 158
4.3.6.5. ADC Record Mixer 158
4.3.6.6. Analog Audio Input Path 159
4.3.6.7. FM Input 159
4.3.7. Audio Codec Register List 160
4.3.8. Audio Codec Register Description 160
4.3.8.1. DAC Digital Part Control Register 160
4.3.8.2. DAC FIFO Control Register 162
4.3.8.3. DAC FIFO Status Register 164
4.3.8.4. DAC TX DATA Register 164
4.3.8.5. ADC FIFO Control Register 165
4.3.8.6. ADC FIFO Status Register 166
4.3.8.7. ADC RX DATA Register 167
4.3.8.8. DAC Analog & Output MIXER Control Register 167
4.3.8.9. ADC Analog and Input mixer Control Register 169
4.3.8.10. ADC&DAC performance tuning Register 170
4.3.8.11. Bias & DA16 Calibration Control Register 0 171
4.3.8.12. Bias & DA16 Calibration Control Register 1 172
4.3.8.13. DAC TX Counter Register 172

 Copyright ©2019 Allwinner Technology Co., Ltd. All Rights Reserved

4.3.8.14. ADC RX Counter Register 172
4.3.8.15. DAC Debug Register 172
4.3.8.16. ADC Debug Register 173
4.3.8.17. ADC DAP Control Register 173
4.3.8.18. ADC DAP Left Control Register 174
4.3.8.19. ADC DAP Right Control Register 175
4.3.8.20. ADC DAP Parameter Register 176
4.3.8.21. ADC DAP Left Average Coef Register 177
4.3.8.22. ADC DAP Left Decay & Attack Time Register 177
4.3.8.23. ADC DAP Right Average Coef Register 177
4.3.8.24. ADC DAP Right Decay & Attack Time Register 178
4.3.8.25. ADC DAP HPF Coef Register 178
4.3.8.26. ADC DAP Left Input Signal Low Average Coef Register 178
4.3.8.27. ADC DAP Right Input Signal Low Average Coef Register 178
4.3.8.28. ADC DAP Optimum Register 179
Chapter 5. Display 180
5.1. TCON 181
5.1.1. Overview 181
5.1.2. Feature 181
5.1.3. Block Diagram 181
5.1.3.1. LCD Timing Controller 181
5.1.4. TCON Register List 182
5.1.5. TCON Register Description 183
5.1.5.1. TCON Control Register 183

 Copyright ©2019 Allwinner Technology Co., Ltd. All Rights Reserved

5.1.5.2. TCON Interrupt Register 0 183
5.1.5.3. TCON Interrupt Register 1 184
5.1.5.4. TCON FRM Control Register 184
5.1.5.5. TCON FRM Seed0 Red Register 184
5.1.5.6. TCON FRM Seed0 Green Register 184
5.1.5.7. TCON FRM Seed0 Blue Register 185
5.1.5.8. TCON FRM Seed1 Red Register 185
5.1.5.9. TCON FRM Seed1 Green Register 185
5.1.5.10. TCON FRM Seed1 Blue Register 185
5.1.5.11. TCON FRM Table Register 0 185
5.1.5.12. TCON FRM Table Register 1 185
5.1.5.13. TCON FRM Table Register 2 186
5.1.5.14. TCON FRM Table Register 3 186
5.1.5.15. TCON0 Control Register 186
5.1.5.16. TCON Clock Control Register 187
5.1.5.17. TCON0 Basic Timing Register 0 187
5.1.5.18. TCON0 Basic Timing Register 1 187
5.1.5.19. TCON0 Basic Timing Register 2 188
5.1.5.20. TCON0 Basic Timing Register 3 188
5.1.5.21. TCON0 HV Timing Register 188
5.1.5.22. TCON0 CPU Interface Control Register 189
5.1.5.23. TCON0 CPU Write Register 190
5.1.5.24. TCON0 CPU Read Register 190
5.1.5.25. TCON0 CPU Read NX Register 190

 Copyright ©2019 Allwinner Technology Co., Ltd. All Rights Reserved

5.1.5.26. TCON0 IO Control Register 0 190
5.1.5.27. TCON0 IO Control Register 1 191
5.1.5.28. TCON1 Control Register 191
5.1.5.29. TCON1 Basic Timing Register 0 192
5.1.5.30. TCON1 Basic Timing Register 1 192
5.1.5.31. TCON1 Basic Timing Register 2 192
5.1.5.32. TCON1 Basic Timing Register 3 193
5.1.5.33. TCON1 Basic Timing Register 4 193
5.1.5.34. TCON1 Basic Timing Register 5 193
5.1.5.35. TCON1 IO Control Register 0 193
5.1.5.36. TCON1 IO Control Register 1 194
5.1.5.37. TCON Debug Information Register 194
5.2. Display Engine Front-End 196
5.2.1. Overview 196
5.2.2. Feature 196
5.2.3. Block Diagram 196
5.2.4. DEFE Register List 196
5.2.5. DEFE Register Description 198
5.2.5.1. DEFE Module Enable Register 198
5.2.5.2. DEFE Frame Process Control Register 198
5.2.5.3. DEFE CSC Bypass Register 199
5.2.5.4. DEFE Algorithm Selection Register 200
5.2.5.5. DEFE Line Interrupt Conrtol Register 200
5.2.5.6. DEFE Input Channel 0 Buffer Address Register 200

 Copyright ©2019 Allwinner Technology Co., Ltd. All Rights Reserved

5.2.5.7. DEFE Input Channel 1 Buffer Address Register 200
5.2.5.8. DEFE Input Channel 2 Buffer Address Register 201
5.2.5.9. DEFE Field Sequence Register 201
5.2.5.10. DEFE Channel 0 Tile Based Offset Register 201
5.2.5.11. DEFE Channel 1 Tile Based Offset Register 201
5.2.5.12. DEFE Channel 2 Tile Based Offset Register 202
5.2.5.13. DEFE Channel 0 Line Stride Register 202
5.2.5.14. DEFE Channel 1 Line Stride Register 202
5.2.5.15. DEFE Channel 2 Line Stride Register 202
5.2.5.16. DEFE Input Format Register 203
5.2.5.17. DEFE Write Back Address Register 204
5.2.5.18. DEFE Output Format Register 204
5.2.5.19. DEFE Interrupt Enable Register 205
5.2.5.20. DEFE Interrupt Status Register 206
5.2.5.21. DEFE Status Register.....206
5.2.5.22. DEFE CSC Coefficient 00 Register 207
5.2.5.23. DEFE CSC Coefficient 01 Register 207
5.2.5.24. DEFE CSC Coefficient 02 Register 207
5.2.5.25. DEFE CSC Coefficient 03 Register 207
5.2.5.26. DEFE CSC Coefficient 10 Register 208
5.2.5.27. DEFE CSC Coefficient 11 Register 208
5.2.5.28. DEFE CSC Coefficient 12 Register 208
5.2.5.29. DEFE CSC Coefficient 13 Register 208
5.2.5.30. DEFE CSC Coefficient 20 Register 208

 Copyright ©2019 Allwinner Technology Co., Ltd. All Rights Reserved

5.2.5.31. DEFE CSC Coefficient 21 Register 209
5.2.5.32. DEFE CSC Coefficient 22 Register 209
5.2.5.33. DEFE CSC Coefficient 23 Register 209
5.2.5.34. DEFE Input Size Register 209
5.2.5.35. DEFE Output Size Register 209
5.2.5.36. DEFE Horizontal Factor Register 210
5.2.5.37. DEFE Vertical Register 210
5.2.5.38. DEFE Channel 0 Horizontal Filter Coefficient Register 210
5.2.5.39. DEFE Channel 0 Vertical Filter Coefficient Register 210
5.2.5.40. DEFE Channel 1 Horizontal Filter Coefficient Register 211
5.2.5.41. DEFE Channel 1 Vertical Filter Coefficient Register 211
5.3. Display Engine Back-End 212
5.3.1. Overview 212
5.3.2. Feature 212
5.3.3. Block Diagram 212
5.3.4. DEBE Register List 213
5.3.5. DEBE Register Description 214
5.3.5.1. DEBE Mode Control Register 214
5.3.5.2. DEBE Color Control Register 215
5.3.5.3. DEBE Layer 0 Size Register 215
5.3.5.4. DEBE Layer 1 Size Register 215
5.3.5.5. DEBE Layer 2 Size Register 215
5.3.5.6. DEBE Layer 3 Size Register 216
5.3.5.7. DEBE Layer 0 Coordinate Control Register 216

 Copyright ©2019 Allwinner Technology Co., Ltd. All Rights Reserved

5.3.5.8. DEBE Layer 1 Coordinate Control Register 216
5.3.5.9. DEBE Layer 2 Coordinate Control Register 216
5.3.5.10. DEBE Layer 3 Coordinate Control Register 217
5.3.5.11. DEBE Layer 0 Frame Buffer Line Width Register 217
5.3.5.12. DEBE Layer 1 Frame Buffer Line Width Register 217
5.3.5.13. DEBE Layer 2 Frame Buffer Line Width Register 217
5.3.5.14. DEBE Layer 3 Frame Buffer Line Width Register 217
5.3.5.15. DEBE Layer 0 Frame Buffer Address Register 217
5.3.5.16. DEBE Layer 1 Frame Buffer Address Register 218
5.3.5.17. DEBE Layer 2 Frame Buffer Address Register 218
5.3.5.18. DEBE Layer 3 Frame Buffer Address Register 218
5.3.5.19. DEBE Register Buffer Control Register 218
5.3.5.20. DEBE Color Key Max Register 218
5.3.5.21. DEBE Color Key Min Register 219
5.3.5.22. DEBE Color Key Configuration Register 219
5.3.5.23. DEBE Layer 0 Attribute Control Register 0 219
5.3.5.24. DEBE Layer 1 Attribute Control Register 0 220
5.3.5.25. DEBE Layer 2 Attribute Control Register 0 221
5.3.5.26. DEBE Layer 3 Attribute Control Register 0 223
5.3.5.27. DEBE Layer 0 Attribute Control Register 1 224
5.3.5.28. DEBE Layer 1 Attribute Control Register 1 224
5.3.5.29. DEBE Layer 2 Attribute Control Register 1 225
5.3.5.30. DEBE Layer 3 Attribute Control Register 1 226
5.3.5.31. DEBE HWC Coordinate Control Register 230

 Copyright ©2019 Allwinner Technology Co., Ltd. All Rights Reserved

5.3.5.32. DEBE HWC Frame Buffer Format Register 230
5.3.5.33. DEBE Write Back Control Register 230
5.3.5.34. DEBE Write Back Address Register 231
5.3.5.35. DEBE Write Back Buffer Line Width Register 231
5.3.5.36. DEBE Input YUV Channel Control Register 231
5.3.5.37. DEBE YUV Channel 0 Frame Buffer Address Register 232
5.3.5.38. DEBE YUV Channel 1 Frame Buffer Address Register 232
5.3.5.39. DEBE YUV Channel 2 Frame Buffer Address Register 232
5.3.5.40. DEBE YUV Channel 0 Buffer Line Width Register 233
5.3.5.41. DEBE YUV Channel 1 Buffer Line Width Register 233
5.3.5.42. DEBE YUV Channel 2 Buffer Line Width Register 233
5.3.5.43. DEBE Coefficient 00 Register 233
5.3.5.44. DEBE Coefficient 01 Register 233
5.3.5.45. DEBE Coefficient 02 Register 234
5.3.5.46. DEBE Coefficient 03 Register 234
5.3.5.47. DEBE Coefficient 10 Register 234
5.3.5.48. DEBE Coefficient 11 Register 234
5.3.5.49. DEBE Coefficient 12 Register 235
5.3.5.50. DEBE Coefficient 13 Register 235
5.3.5.51. DEBE Coefficient 20 Register 235
5.3.5.52. DEBE Coefficient 21 Register 235
5.3.5.53. DEBE Coefficient 22 Register 235
5.3.5.54. DEBE Coefficient 23 Register 236
5.3.5.55. DEBE HWC Pattern Memory Block 236

 Copyright ©2019 Allwinner Technology Co., Ltd. All Rights Reserved

5.3.5.56. DEBE HWC Palette Table 236
5.3.5.57. Palette Mode 237
5.4. De-interlacer 239
5.4.1. Overview 239
5.4.2. Feature 239
5.4.3. De-interlacer Register List 239
5.4.4. De-interlacer Register Description 239
5.4.4.1. DI Control Register 239
5.4.4.2. DI Interrupt Control Register 240
5.4.4.3. DI Status Register 240
5.4.4.4. DI Size Setting Register 241
5.4.4.5. DI Format Setting Register 241
5.4.4.6. DI Input Line Stride 0 Setting Register 241
5.4.4.7. DI Input Line Stride 1 Setting Register 242
5.4.4.8. DI Output Line Stride 0 Setting Register 242
5.4.4.9. DI Output Line Stride 1 Setting Register 242
5.4.4.10. DI Flag Line Stride Setting Register 242
5.4.4.11. DI Current Frame Address 0 Register 242
5.4.4.12. DI Current Frame Address 1 Register 243
5.4.4.13. DI Pre-frame Address 0 Register 243
5.4.4.14. DI Pre-frame Address 1 Register 243
5.4.4.15. DI Output Frame Address 0 Register 243
5.4.4.16. DI Output Frame Address 1 Register 243
5.4.4.17. DI Flag Address Register 243

 Copyright ©2019 Allwinner Technology Co., Ltd. All Rights Reserved

5.4.4.18. DI Parameters Register 244
Chapter 6. Image Subsystem 245
6.1. CSI 245
6.1.1. Overview 245
6.1.2. Feature 245
6.1.3. Block Diagram 245
6.1.4. CSI Data Port 246
6.1.5. Timing 246
6.1.6. CSI Register List 247
6.1.7. CSI Register Description 247
6.1.7.1. CSI Enable Register 247
6.1.7.2. CSI Configuration Register 247
6.1.7.3. CSI Capture Control Register 249
6.1.7.4. CSI Scale Register 249
6.1.7.5. CSI FIFO 0 Output Buffer A Address Register 250
6.1.7.6. CSI FIFO 0 Output Buffer B Address Register 250
6.1.7.7. CSI FIFO 1 Output Buffer A Address Register 250
6.1.7.8. CSI FIFO 1 Output Buffer B Address Register 250
6.1.7.9. CSI FIFO 2 Output Buffer A Address Register 250
6.1.7.10. CSI FIFO 2 Output Buffer B Address Register 250
6.1.7.11. CSI Output Buffer Control Register 250
6.1.7.12. CSI Status Register 251
6.1.7.13. CSI Interrupt Enable Register 251
6.1.7.14. CSI Interrupt Status Register 252

 Copyright ©2019 Allwinner Technology Co., Ltd. All Rights Reserved

6.1.7.15. CSI Horizontal Size Register 253
6.1.7.16. CSI Vertical Size Register 253
6.1.7.17. CSI Buffer Length Register 253
Chapter 7. Interfaces 254
7.1. SD/MMC Interface 255
7.1.1. Overview 255
7.1.2. Feature 255
7.1.3. SD/MMC Timing 255
7.1.4. SD/MMC Pin List 255
7.1.5. SD/MMC DMA Controller Description 256
7.1.5.1. IDMAC Descriptor Structure 256
7.1.5.2. DES0 Definition 257
7.1.5.3. DES1 Definition 257
7.1.5.4. DES2 Definition 258
7.1.5.5. DES3 Definition 258
7.1.6. SD/MMC Register List 258
7.1.7. SD/MMC Register Description 259
7.1.7.1. SD Global Control Register 259
7.1.7.2. SD Clock Control Register 260
7.1.7.3. SD Timeout Register 260
7.1.7.4. SD Bus Width Register 260
7.1.7.5. SD Block Size Register 261
7.1.7.6. SD Byte Count Register 261
7.1.7.7. SD Command Register 261

 Copyright ©2019 Allwinner Technology Co., Ltd. All Rights Reserved

7.1.7.8. SD Command Argument Register 263
7.1.7.9. SD Response Register 0 263
7.1.7.10. SD Response Register 1 263
7.1.7.11. SD Response Register 2 263
7.1.7.12. SD Response Register 3 263
7.1.7.13. SD Interrupt Mask Register 264
7.1.7.14. SD Masked Interrupt Status Register 264
7.1.7.15. SD Raw Interrupt Status Register 265
7.1.7.16. SD Status Register 265
7.1.7.17. SD FIFO Water Level Register 267
7.1.7.18. SD Function Select Register 268
7.1.7.19. SD Transferred CIU Card Byte Count Register 268
7.1.7.20. SD Transferred Host to BIU-FIFO Byte Count Register 269
7.1.7.21. SD Debug Control Register 269
7.1.7.22. SD Auto Command 12 Argument Register 269
7.1.7.23. SD Hardware Reset Register 269
7.1.7.24. SD DMAC Control Register 269
7.1.7.25. SD Descriptor List Base Address Register 270
7.1.7.26. SD DMAC Status Register 271
7.1.7.27. SD DMAC Interrupt Enable Register 272
7.1.7.28. SD Current Host Descriptor Address Register 273
7.1.7.29. SD Current Buffer Descriptor Address Register 273
7.1.7.30. Card Threshold Control Register 273
7.1.7.31. EMMC4.5 DDR Start Bit Detection Control Register 274

 Copyright ©2019 Allwinner Technology Co., Ltd. All Rights Reserved

7.1.7.32. SD FIFO Register 274
7.2. TWI 275
7.2.1. Overview 275
7.2.2. Feature 275
7.2.3. Pin List 275
7.2.4. Timing Diagram 275
7.2.5. TWI Controller Operation 276
7.2.6. TWI Controller Register List 276
7.2.7. TWI Controller Register Description 277
7.2.7.1. TWI Slave Address Register 277
7.2.7.2. TWI Extend Address Register 277
7.2.7.3. TWI Data Register 277
7.2.7.4. TWI Control Register 277
7.2.7.5. TWI Status Register 279
7.2.7.6. TWI Clock Register 280
7.2.7.7. TWI Soft Reset Register 280
7.2.7.8. TWI Enhance Feature Register 280
7.2.7.9. TWI Line Control Register 280
7.3. SPI 282
7.3.1. Overview 282
7.3.2. Feature 282
7.3.3. SPI Timing Diagram 282
7.3.4. SPI Pin List 283
7.3.5. SPI Module Clock Source and Frequency 283

 Copyright ©2019 Allwinner Technology Co., Ltd. All Rights Reserved

7.3.6. SPI Register List 284
7.3.7. SPI Register Description 284
7.3.7.1. SPI Global Control Register 284
7.3.7.2. SPI Transfer Control Register 285
7.3.7.3. SPI Interrupt Control Register 287
7.3.7.4. SPI Interrupt Status Register 288
7.3.7.5. SPI FIFO Control Register 290
7.3.7.6. SPI FIFO Status Register 291
7.3.7.7. SPI Wait Clock Register 292
7.3.7.8. SPI Clock Control Register 292
7.3.7.9. SPI Master Burst Counter Register 293
7.3.7.10. SPI Master Transmit Counter Register 293
7.3.7.11. SPI Master Burst Control Counter Register 293
7.3.7.12. SPI TX Data Register 294
7.3.7.13. SPI RX Data Register 294
7.4. UART 295
7.4.1. Overview 295
7.4.2. Feature 295
7.4.3. UART Timing Diagram 295
7.4.4. UART Pin List 296
7.4.5. IrDA Inverted Signals 296
7.4.6. UART Register List 296
7.4.7. UART Register Description 297
7.4.7.1. UART Receiver Buffer Register 297

 Copyright ©2019 Allwinner Technology Co., Ltd. All Rights Reserved

7.4.7.2. UART Transmit Holding Register 297
7.4.7.3. UART Divisor Latch Low Register 298
7.4.7.4. UART Divisor Latch High Register 298
7.4.7.5. UART Interrupt Enable Register 298
7.4.7.6. UART Interrupt Identity Register 299
7.4.7.7. UART FIFO Control Register 300
7.4.7.8. UART Line Control Register 301
7.4.7.9. UART Modem Control Register 303
7.4.7.10. UART Line Status Register 304
7.4.7.11. UART Modem Status Register 306
7.4.7.12. UART Scratch Register 308
7.4.7.13. UART Status Register 308
7.4.7.14. UART Transmit FIFO Level Register 309
7.4.7.15. UART Receive FIFO Level Register 309
7.4.7.16. UART Halt TX Register 309
7.4.7.17. UART DBG DLL Register 310
7.4.7.18. UART DBG DLH Register 310
7.5. RSB 311
7.5.1. Overview 311
7.5.2. Feature 311
7.5.3. Terminology Definition 311
7.5.4. RSB Command Set 311
7.5.5. Software Operation Flow 312
7.5.6. RSB General Specification 314

 Copyright ©2019 Allwinner Technology Co., Ltd. All Rights Reserved

7.5.7. RSB Controller Register List 316
7.5.8. RSB Register Description 316
7.5.8.1. RSB Control Register 316
7.5.8.2. RSB Clock Control Register 317
7.5.8.3. RSB Interrupt Enable Register 317
7.5.8.4. RSB Status Register 317
7.5.8.5. RSB Address Register 318
7.5.8.6. RSB Data Buffer Register 318
7.5.8.7. RSB Line Control Register 318
7.5.8.8. RSB Device Mode Control Register 319
7.5.8.9. RSB Command Register 319
7.5.8.10. RSB Device Address Register 320
7.6. CIR Receiver 321
7.6.1. Overview 321
7.6.2. Feature 321
7.6.3. Timing 321
7.6.4. CIR Receiver Register List 322
7.6.5. CIR Receiver Register Description 322
7.6.5.1. CIR Control Register 322
7.6.5.2. CIR Receiver Configure Register 322
7.6.5.3. CIR Receiver FIFO Register 323
7.6.5.4. CIR Receiver Interrupt Control Register 323
7.6.5.5. CIR Receiver Status Register 323
7.6.5.6. CIR Configure Register 324

 Copyright ©2019 Allwinner Technology Co., Ltd. All Rights Reserved

7.7. USB-OTG 326
7.7.1. Overview 326
7.7.2. Feature 326
7.7.3. Functionalities Description 326
7.7.3.1. DMA Support 326
7.7.3.2. RAM Sharing 327
7.7.3.3. Power Save 328
7.7.3.4. Clock Source and Frequency 328
7.8. Digital Audio Interface 329
7.8.1. Overview 329
7.8.2. Feature 329
7.8.3. Signal Description 329
7.8.3.1. Digital Audio Interface Pin List 329
7.8.3.2. Digital Audio Interface MCLK and BCLK 329
7.8.3.3. Digital Audio Interface Clock Source and Frequency 330
7.8.4. Functionalities Description 330
7.8.4.1. Typical Applications 330
7.8.4.2. Functional Block Diagram 331
7.8.4.3. Operation Principle 331
7.8.5. Operation Modes 332
7.8.5.1. System setup and I2S/PCM initialization 332
7.8.5.2. The channel setup and DMA setup 332
7.8.5.3. Enable and disable the I2S/PCM 332
7.8.6. Digital Audio Interface Register List 333

 Copyright ©2019 Allwinner Technology Co., Ltd. All Rights Reserved

7.8.7. Digital Audio Interface Register Description 333
7.8.7.1. Digital Audio Control Register 333
7.8.7.2. Digital Audio Format Register 0 334
7.8.7.3. Digital Audio Format Register 1 335
7.8.7.4. Digital Audio TX FIFO Register 336
7.8.7.5. Digital Audio RX FIFO Register 336
7.8.7.6. Digital Audio FIFO Control Register 336
7.8.7.7. Digital Audio FIFO Status Register 337
7.8.7.8. Digital Audio DMA & Interrupt Control Register 338
7.8.7.9. Digital Audio Interrupt Status Register 339
7.8.7.10. Digital Audio Clock Divide Register 340
7.8.7.11. Digital Audio TX Counter Register 340
7.8.7.12. Digital Audio RX Counter Register 341
7.8.7.13. Digital Audio TX Channel Select Register 341
7.8.7.14. Digital Audio TX Channel Mapping Register 341
7.8.7.15. Digital Audio RX Channel Select Register 342
7.8.7.16. Digital Audio RX Channel Mapping Register 342
7.9. OWA Interface 344
7.9.1. Overview 344
7.9.2. Feature 344
7.9.3. Signal Description 344
7.9.3.1. OWA Interface Pin List 344
7.9.3.2. OWA Interface Clock Requirement 344
7.9.4. Functionalities Description 344

 Copyright ©2019 Allwinner Technology Co., Ltd. All Rights Reserved

7.9.4.1. Typical Applications 344
7.9.4.2. Functional Block Diagram 344
7.9.4.3. Operation Principle 345
7.9.5. Operation Modes 345
7.9.5.1. System setup and OWA initialization 346
7.9.5.2. The channel setup and DMA setup 346
7.9.5.3. Enable and disable the OWA 346
7.9.6. OWA Interface Register List 346
7.9.7. OWA Register Description 346
7.9.7.1. OWA General Control Register 346
7.9.7.2. OWA TX Configure Register 347
7.9.7.3. OWA TX FIFO Register 348
7.9.7.4. OWA FIFO Control Register 348
7.9.7.5. OWA FIFO Status Register 348
7.9.7.6. OWA Interrupt Control Register 349
7.9.7.7. OWA Interrupt Status Register 349
7.9.7.8. OWA TX Counter Register 350
7.9.7.9. OWA TX Channel Status Register 0 350
7.9.7.10. OWA TX Channel Status Register 1 351

 Copyright ©2019 Allwinner Technology Co., Ltd. All Rights Reserved

Chapter 1. About This Documentation

1.1. Documentation Overview

This documentation provides an overall description of the Allwinner F1C200s application processor, which will provide instructions to programmers from several sections, including system,ADC, display , image, and interfaces.

 Copyright ©2019 Allwinner Technology Co., Ltd. All Rights Reserved

Chapter 2. Overview

The F1C200s processor represents Allwinner's latest achievement in mobile applications processors. The processor targets the needs of video boombox markets.

The F1C200s is based on the ARM9 CPU architecture with a high degree of functional integration, and supports Full HD video playback, including H.264,H.263,MPEG1/2/4 decoder. Integrated audio codec and I2S/PCM interface provide end users with a good audio experience. TV-IN interface enables video input by connecting to video devices such as camera, and TV-OUT interface enables video output by connecting to TV devices.

To reduce the BOM costs, the F1C200s built-in DDR1 memory , and it is packed with general-purpose peripherals such as USB OTG, UART, SPI, TWI, TP, SD/MMC, CSI, etc. The F1C200s outperforms competitors in terms of its powerful performance, low power consumption, and flexible scalability.

Applications:

- Video Playback
- Audio Playback
- FM

Copyright ©2019 Allwinner Technology Co., Ltd. All Rights Reserved

2.1. Processor Features

2.1.1. CPU Architecture

The F1C200s platform is based on ARM9 CPU architecture.

- Five-stage pipeline architecture
- Support 16KByte D-Cache
- Support 32KByte I-Cache

2.2. Memory Subsystem

This section consists of:

- Boot ROM
- SDRAM
- SD/MMC Interface

2.2.1. Boot ROM

- On-Chip ROM boot loader
- Support system boot from SPI Nor/Nand Flash, and SD/TF card
- Support system code download through USB OTG

2.2.2. SDRAM

- SIP DDR1

2.2.3. SD/MMC Interface

- Support secure digital memory protocol commands (up to SD2.0)
- Support secure digital I/O protocol commands (up to SDIO2.0)
- Support multimedia card protocol commands (up to eMMC4.41)
- Support one SD (Verson1.0 to 2.0) or MMC (version 3.3 to eMMC4.41)
- Support hardware CRC generation and error detection
- Support host pull-up control
- Support SDIO interrupts in 1-bit and 4-bit modes
- Support SDIO suspend and resume operation
- Support SDIO read wait
- Support block size of 1 to 65535 bytes
- Support descriptor-based internal DMA controller
- Internal 128 bytes FIFO for data transfer
- Support 3.3V IO pad

2.3. System Peripheral

This section includes:

- Timer
- INTC
- CCU
- DMA
- PWM

2.3.1. Timer

- Three timers

Copyright ©2019 Allwinner Technology Co., Ltd. All Rights Reserved

- Support watchdog reset
- Support audio and video synchronize counter

2.3.2. INTC

- Support up to 64 interrupts
- Support 4-level priority
- Support interrupt mask
- Support interrupt fast forcing
- Support one external interrupt

2.3.3. CCU

- Support 6 PLLs
- Control of clock generation, division, distribution and gating
- Control of device software reset

2.3.4. DMA

- Support Normal DMA and Dedicated DMA
- Support two kinds of interrupt
- Support hardware continuous transfer mode

2.3.5. PWM

- Support two PWM outputs
- Support cycle mode and pulse mode
- Support 24MHz maximum output frequency

2.4. Display Subsystem

This section includes:

- Display Engine
- Display Output

2.4.1. Display Engine

- Support four layers overlay, each layer size up to 2048x2048 pixels
- Support Alpha blending/color key
- Support multi-format input formats
  - 1/2/4/8/16/32 bpp color
  - YUV444/YUV422/YUV420/YUV411
- Support hardware cursor
- Ultra-Scaling engine
  - 4-tap scale filter in horizontal and vertical direction
  - Input and output size up to 1280x720 pixels
  - Support write-back to memory function
- Support de-interlacing function for Standard-definition video

2.4.2. Display Output

- LCD RGB interface, TTL interface, up to 1280x720@60fps
- LCD Serial RGB interface, CCIR656 interface, up to 720x576@60fps
- LCD i8080 interface with 18/16/9/8 bit, up to 800x480@60fps
- LCD Dither function, supports RGB666/RGB565 interface
- TV CVBS output, supports NTSC/PAL, with auto plug detecting

Copyright ©2019 Allwinner Technology Co., Ltd. All Rights Reserved

2.5. Video Engine

- Support H.264 BP/MP/HP up to 1920x1080@30fps decoding
- Support MPEG1 and MPEG2 up to 1920x1080@30fps decoding
- Support MPEG4 SP/ASP GMC and H.263 including Sorenson Spark up to 1920x1080@30fps decoding
- Support MJPEG encode up to 1280x720@30fps
- Support JPEG encode size up to 8192 x 8192
- Support JPEG decode size up to 16384 x 16384

2.6. Image Subsystem

This section includes:

- CSI
- CVBS Input

2.6.1. CSI

- Support 8-bit CMOS-sensor interface
- Support YUV camera up to 5Mega pixel
- Support CCIR656 protocol for NTSC and PAL

2.6.2. CVBS Input

- Support NTSC/PAL
- Support 3D comb filter
- Support two TV CVBS channels:TVIN0,TVIN1

2.7. Audio Subsystem

2.7.1. Audio Codec

- Two audio digital-to-analog(DAC) channels
- Stereo capless headphone drivers:
  - Up to 100dB DR
  - Supports DAC Sample Rates from 8kHz to 192kHz
- Support analog/ digital volume control
- Analog low-power loop from FM/ line-in /microphone to headphone outputs
- Three audio inputs:
  - One microphone input
  - Stereo FM left/right input
  - One Line-in input
- One audio analog-to-digital(ADC) channel
  - 96dB SNR@A-weight
  - Supports ADC Sample Rates from 8KHz to 48KHz
  - Support AGC (Auto Gain Control)

2.8. Interfaces

This section includes:

- USB 2.0 OTG
- KEYADC
- TP
- Digital Audio Interface
- UART

 Copyright ©2019 Allwinner Technology Co., Ltd. All Rights Reserved

- SPI
- TWI
- CIR
- RSB™
- OWA

2.8.1. USB 2.0 OTG

- Support up to 6 User-Configurable Endpoints(TX Endpoint 1/2/3 and RX Endpoint 1/2/3) for Bulk, Isochronous, Control and Interrupt bi-directional transfer
- Support High-Bandwidth Isochronous & Interrupt transfers
- 64-Byte Endpoint 0 for Control Transfer (Endpoint0)
- Support industry-standard single port SRAM for USB Configurable Data FIFO. The size is 2048 byte with 32-bit word width. The RAM can be used by other modules when USB OTG disable
- Support point-to-point and point-to-multipoint transfer in Host mode
- Perform all transaction scheduling in hardware
- Power Optimization and Power Management capabilities

2.8.2. KEYADC

- 6-bit resolution
- Support hold key and general key
- Support single key and continuous key
- Sample rate up to 250Hz

2.8.3. TP

- 12-bit SAR type A/D converter
- 4-wire I/F
- Dual Touch Detect
- Touch-pressure measurement
- Sampling frequency: 2MHz
- Single-Ended conversion of touch screen inputs and ratio metric conversion of touch screen inputs
- TACQ up to 262ms
- Median and averaging filter to reduce noise
- Pen down detection, with programmable sensitivity
- Support X, Y change function

2.8.4. Digital Audio Interface

- I2S or PCM configured by software
- Master / Slave Mode operation configured by software
- I2S Audio data sample rate from 8kHz to 192kHz
- I2S Data format for standard I2S, Left Justified and Right Justified
- PCM supports linear sample (8-bit or 16-bit), 8-bit u-law and A-law commanded sample

2.8.5. UART

- Three UART controllers
- Compatible with industry-standard 16550 UARTs
- Support IRDA version 1.0 SIR protocol with maximum baud rate to 115200bps for all UARTs
- Support for word length from 5 to 8 bits,an optional parity bit, and 1,1.5 or 2 stop bits
- Programmable parity(even,odd and no parity)
- 32-Bytes Transmit and receive data FIFOs
- Support DMA controller interface
- Software/ Hardware Flow Control
- Interrupt support for FIFOs, Status Change

2.8.6. SPI

- Two SPI controllers
- Full-duplex synchronous serial interface
- Master/Slave configurable

Copyright ©2019 Allwinner Technology Co., Ltd. All Rights Reserved

- 8-bit wide by 64-entry FIFO for both transmit and receive data
- Polarity and phase of the chip select (SPI_SS) and SPI Clock (SPI_SCLK) are configurable

2.8.7. TWI

- Three TWI controllers
- Software-programmable for Slave or Master
- Support repeated START signal
- Multi-master systems supported
- Allow 10-bit addressing with TWI bus
- Performs arbitration and clock synchronization
- Own address and general call address detection
- Interrupt on address detection
- Support speeds up to 400Kbits/s (‘fast mode’)
- Allow operation from a wide range of input clock frequencies

2.8.8. CIR

- Full physical layer implementation
- Support CIR for remote control
- 64x8bits FIFO for data buffer
- Programmable FIFO thresholds

2.8.9. RSB™

- Support speed up to 20MHz with ultra low power
- Support push-pull bus
- Support host mode
- Support programmable output delay of CD signal
- Support parity check for address and data transmission
- Support multi-devices

2.8.10. OWA

- EC-60958 transmitter functionality
- Support S/PDIF Interface
- Support channel status insertion for the transmitter
- Support Parity generation on the transmitter
- One 32×24bits FIFO (TX) for audio data transfer
- Programmable FIFO thresholds
- Interrupt and DMA support

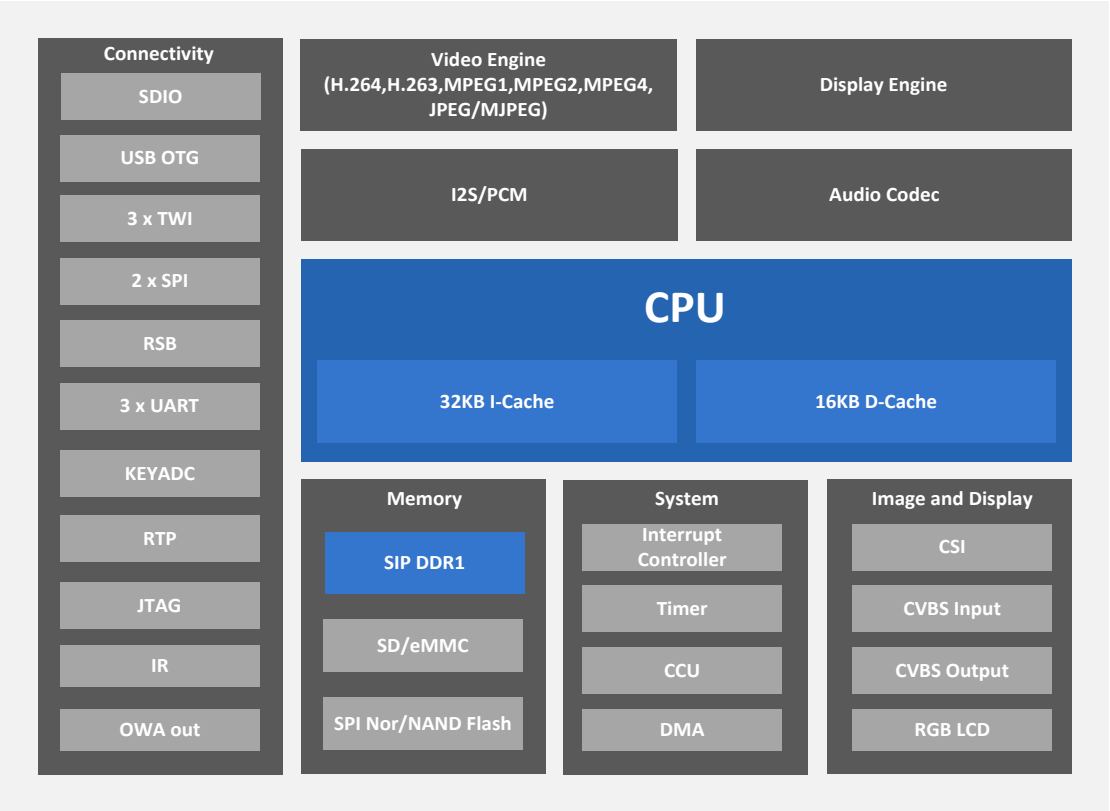
2.9. Package

- QFN88,10mm x 10mm

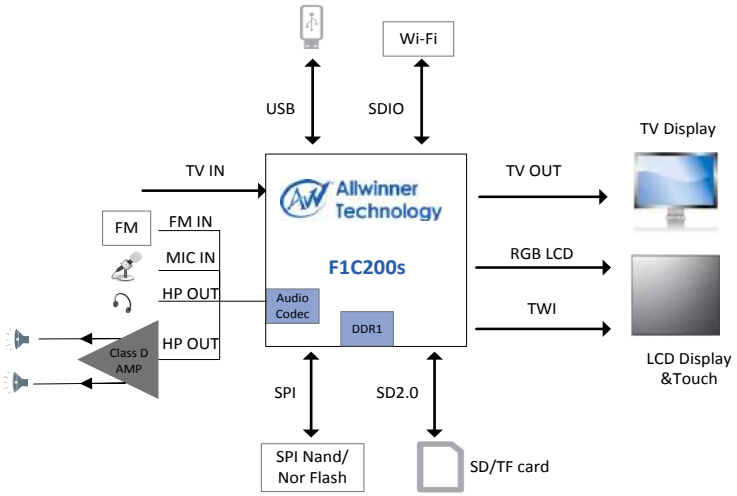
Copyright ©2019 Allwinner Technology Co., Ltd. All Rights Reserved

2.10. System Block Diagram

The block diagram of F1C200s processor is as follows:



The typical application diagram of F1C200s is as follows:



 Copyright ©2019 Allwinner Technology Co., Ltd. All Rights Reserved

Chapter 3. System

The chapter describes the F1C200s system from following sections:

- Memory Mapping
- CCU
- Timer
- PWM
- INTC
- DMA
- Port Controller

 Copyright ©2019 Allwinner Technology Co., Ltd. All Rights Reserved

3.1. Memory Mapping

Module	Address (It is for Cluster CPU)	Size (byte)
BROM	0x0000 0000---0x0000 7FFF	32K
SRAM A	0x0001 0000---0x0001 9FFF	40K
System Controller	0x01C0 0000---0x01C0 0FFF	4K
DRAMC	0x01C0 1000---0x01C0 1FFF	4K
DMA	0x01C0 2000---0x01C0 2FFF	4K
SPI0	0x01C0 5000---0x01C0 5FFF	4K
SPI1	0x01C0 6000---0x01C0 6FFF	4K
TVE	0x01C0 A000---0x01C0 AFFF	4K
TVD	0x01C0 B000---0x01C0 BFFF	4K
TCON	0x01C0 C000---0x01C0 CFFF	4K
VE	0x01C0 E000---0x01C0 EFFF	4K
SD/MMC 0	0x01C0 F000---0x01C0 FFFF	4K
SD/MMC 1	0x01C1 0000---0x01C1 0FFF	4K
USB-OTG	0x01C1 3000---0x01C1 3FFF	4K
CCU	0x01C2 0000---0x01C2 03FF	1K
INTC	0x01C2 0400---0x01C2 07FF	1K
PIO	0x01C2 0800---0x01C2 0BFF	1K
TIMER	0x01C2 0C00---0x01C2 0FFF	1K
PWM	0x01C2 1000---0x01C2 13FF	1K
OWA	0x01C2 1400---0x01C2 17FF	1K
RSB	0x01C2 1800---0x01C2 1BFF	1K
DAUDIO	0x01C2 2000---0x01C2 23FF	1K
CIR	0x01C2 2C00---0x01C2 2FFF	1K
KEYADC	0x01C2 3400---0x01C2 37FF	1K
Audio Codec	0x01C2 3C00---0x01C2 3FFF	1K
TP	0x01C2 4800---0x01C2 4BFF	1K
UART 0	0x01C2 5000---0x01C2 53FF	1K
UART 1	0x01C2 5400---0x01C2 57FF	1K
UART 2	0x01C2 5800---0x01C2 5BFF	1K
TWI 0	0x01C2 7000---0x01C2 73FF	1K
TWI 1	0x01C2 7400---0x01C2 77FF	1K
TWI 2	0x01C2 7800---0x01C2 7BFF	1K
CSI	0x01CB 0000---0x01CB 0FFF	4K
DEFE	0x01E0 0000---0x01E1 FFFF	128K
DEBE	0x01E6 0000---0x01E6 FFFF	64K
DE Interlace	0x01E7 0000---0x01E7 FFFF	64K
DDR1 Space	0x8000 0000---0xBFFF FFFF	1G

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.2. CCU

3.2.1. Overview

The CCU provides the registers to program the PLLs and the controls most of the clock generation, division, distribution, synchronization and gating. CCU input signal is the external clock for the reference frequency (24MHz). The outputs from CCU are mostly clocks to the other blocks in the system.

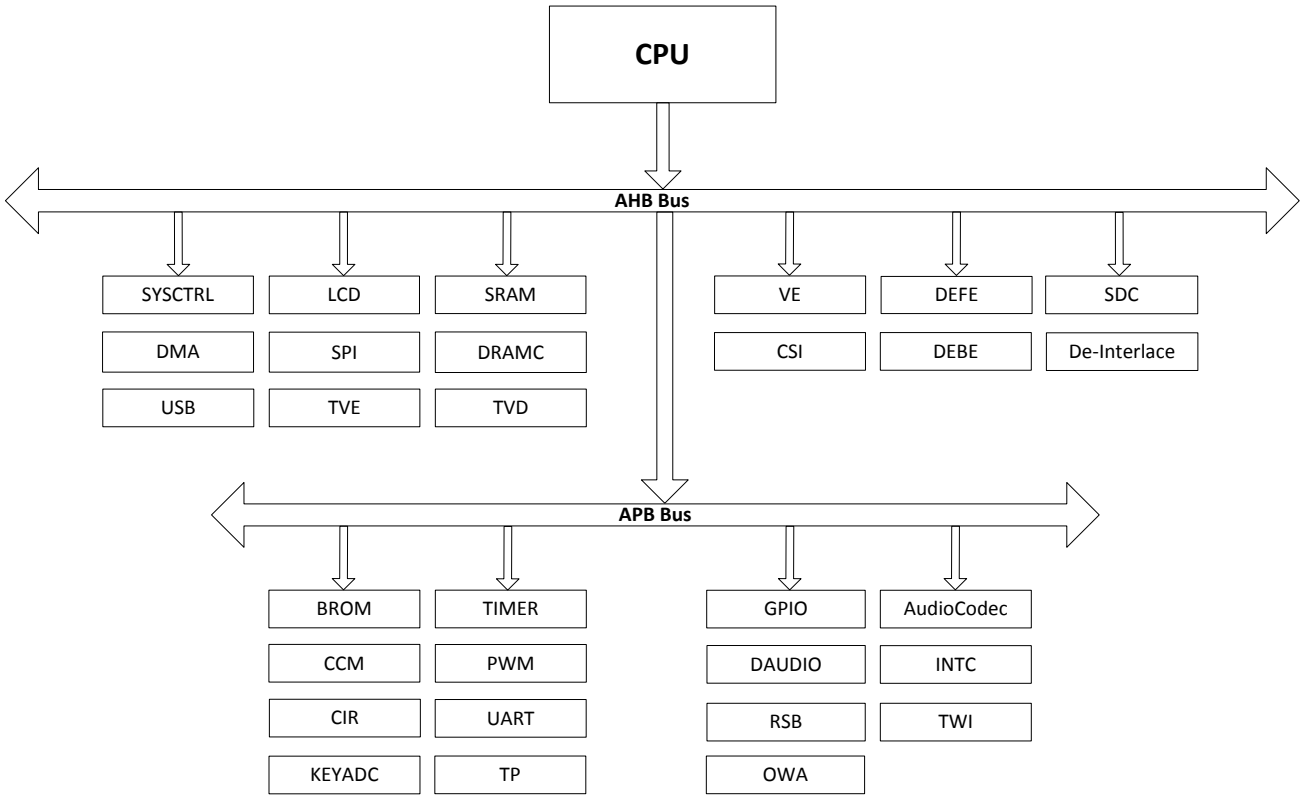
3.2.2. Feature

The CCU includes the following features:

- 6 PLLs, Main Oscillator and an on-chip RC Oscillator
- Bus Divisions
- Clock Output Control
- PLLs Bias Control
- PLLs Tunning Control
- PLLs Pattern Control
- Configuring Modules Clock
- Bus Clock Gating
- Bus Software Reset

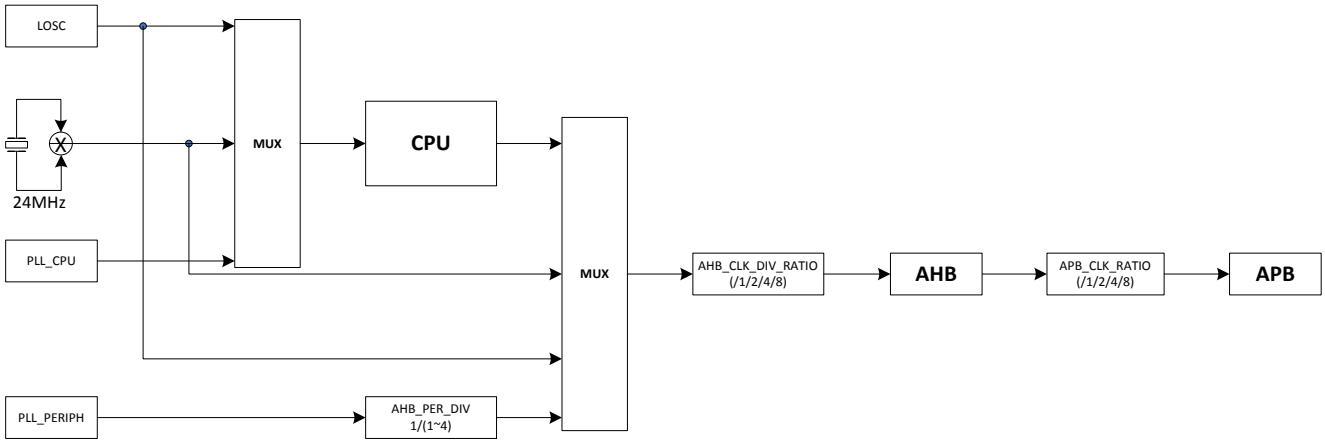
3.2.3. Functionalities Description

3.2.3.1. System Bus



 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.2.3.2. Bus clock tree



3.2.4. CCU Register List

Module Name	Base Address
CCU	0x01C20000

Register Name	Offset	Description
PLL_CPU_CTRL_REG	0x0000	PLL_CPU Control Register
PLL_AUDIO_CTRL_REG	0x0008	PLL_AUDIO Control Register
PLL_VIDEO_CTRL_REG	0x0010	PLL_VIDEO Control Register
PLL_VE_CTRL_REG	0x0018	PLL_VE Control Register
PLL_DDR_CTRL_REG	0x0020	PLL_DDR Control Register
PLL_PERIPH_CTRL_REG	0x0028	PLL_PERIPH Control Register
CPU_CLK_SRC_REG	0x0050	CPU Clock Source Register
AHB_APB_HCLKC_CFG_REG	0x0054	AHB/APB/HCLKC Configuration Register
BUS_CLK_GATING_REG0	0x0060	Bus Clock Gating Register 0
BUS_CLK_GATING_REG1	0x0064	Bus Clock Gating Register 1
BUS_CLK_GATING_REG2	0x0068	Bus Clock Gating Register 2
SDMMC0_CLK_REG	0x0088	SDMMC0 Clock Register
SDMMC1_CLK_REG	0x008C	SDMMC1 Clock Register
DAUDIO_CLK_REG	0x00B0	DAUDIO Clock Register
OWA_CLK_REG	0x00B4	OWA Clock Register
CIR_CLK_REG	0x00B8	CIR Clock Register
USBPHY_CLK_REG	0x00CC	USBPHY Clock Register
DRAM_GATING_REG	0x0100	DRAM GATING Register
BE_CLK_REG	0x0104	BE Clock Register
FE_CLK_REG	0x010C	FE Clock Register
TCON_CLK_REG	0x0118	TCON Clock Register
DI_CLK_REG	0x011C	De-interlacer Clock Register
TVE_CLK_REG	0x0120	TVE Clock Register

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

TVD_CLK_REG	0x0124	TVD Clock Register
CSI_CLK_REG	0x0134	CSI Clock Register
VE_CLK_REG	0x013C	VE Clock Register
AUDIO_CODEC_CLK_REG	0x0140	Audio Codec Clock Register
AVS_CLK_REG	0x0144	AVS Clock Register
PLL_STABLE_TIME_REG0	0x0200	PLL Stable Time Register 0
PLL_STABLE_TIME_REG1	0x0204	PLL Stable Time Register 1
PLL_CPU_BIAS_REG	0x0220	PLL_CPU Bias Register
PLL_AUDIO_BIAS_REG	0x0224	PLL_AUDIO Bias Register
PLL_VIDEO_BIAS_REG	0x0228	PLL_VIDEO Bias Register
PLL_VE_BIAS_REG	0x022C	PLL_VE Bias Register
PLL_DDR_BIAS_REG	0x0230	PLL_DDR Bias Register
PLL_PERIPH_BIAS_REG	0x0234	PLL_PERIPH Bias Register
PLL_CPU_TUN_REG	0x0250	PLL_CPU Tuning Register
PLL_DDR_TUN_REG	0x0260	PLL_DDR Tuning Register
PLL_AUDIO_PAT_CTRL_REG	0x0284	PLL_AUDIO Pattern Control Register
PLL_VIDEO_PAT_CTRL_REG	0x0288	PLL_VIDEO Pattern Control Register
PLL_DDR_PAT_CTRL_REG	0x0290	PLL_DDR Pattern Control Register
BUS_SOFT_RST_REG0	0x02C0	Bus Software Reset Register 0
BUS_SOFT_RST_REG1	0x02C4	Bus Software Reset Register 1
BUS_SOFT_RST_REG2	0x02D0	Bus Software Reset Register 2

3.2.5. CCU Register Description

3.2.5.1. PLL_CPU Control Register

Offset: 0x000			Register Name: PLL_CPU_CTRL_REG
Bit	R/W	Default/Hex	Description
31	R/W	0x0	PLL_ENABLE. 0: Disable 1: Enable The PLL output= (24MHz*N*K) / (M*P). The PLL output is for the CPU Clock. Note: The PLL output clock must be in the range of 200MHz~2.6GHz. Its default is 408MHz.
30:29	/	/	/
28	R	0x0	LOCK 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27:18	/	/	/
17:16	R/W	0x0	PLL_OUT_EXT_DIV_P PLL Output External Divider P 00: /1 01: /2 10: /4

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			11: /
15:13	/	/	/
12:8	R/W	0x10	PLL_FACTOR_N PLL Factor N. Factor=0, N=1 Factor=1, N=2 Factor=2, N=3 …… Factor=31,N=32
7:6	/	/	/
5:4	R/W	0x0	PLL_FACTOR_K. PLL Factor K.(K=Factor + 1) The range is from 1 to 4.
3:2	/	/	/
1:0	R/W	0x0	PLL_FACTOR_M. PLL Factor M. (M=Factor + 1) The range is from 1 to 4.

3.2.5.2. PLL_AUDIO Control Register

Offset: 0x008			Register Name: PLL_AUDIO_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_ENABLE. 0: Disable 1: Enable The PLL is for Audio. The PLL_AUDIO(8X) Output = 24MHz*N*2/M. The PLL output clock must be in the range of 20MHz~200MHz. Its default is 24.571MHz.
30:29	/	/	/
28	R	0x0	LOCK. 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27:25	/	/	/
24	R/W	0x0	PLL_SDM_EN. 0: Disable 1: Enable In this case, the PLL_FACTOR_N only low 4 bits are valid (N: The range is from 1 to 16).
23:15	/	/	/
14:8	R/W	0x55	PLL_FACTOR_N. PLL Factor N. Factor=0, N=1 Factor=1, N=2 …… Factor=127, N=128

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

7:5	/	/	/
4:0	R/W	0x14	PLL_PREDIV_M. PLL Pre-div Factor(M = Factor+1). The range is from 1 to 32

3.2.5.3. PLL_VIDEO Control Register

Offset: 0x010			Register Name: PLL_VIDEO_CTRL_REG
Bit	R/W	Default/Hex	Description
31	R/W	0x0	PLL_ENABLE. 0: Disable 1: Enable In the integer mode, the PLL output = (24MHz*N)/M. In the fractional mode, the PLL output is select by bit 25. Note: In the Clock Control Module, PLL(1X) Output=PLL while PLL(2X) Output=PLL * 2. The PLL output clock must be in the range of 30MHz~600MHz. Its default is 297MHz.
30	R/W	0x0	PLL_MODE. 0: Manual Mode 1: Auto Mode (Controlled by DE)
29	/	/	/
28	R	0x0	LOCK. 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27:26	/	/	/
25	R/W	0x1	FRAC_CLK_OUT. PLL clock output when PLL_MODE_SEL=0(PLL_PREDIV_M factor must be set to 0); No meaning when PLL_MODE_SEL =1. 0: PLLOUT=270MHz 1: PLLOUT=297MHz
24	R/W	0x1	PLL_MODE_SEL. 0: Fractional mode 1: Integer mode Note: When in Fractional mode, the pre-divider M should be set to 0.
23:21	/	/	/
20	R/W	0x0	PLL_SDM_EN. 0: Disable 1: Enable
19:15	/	/	/
14:8	R/W	0x62	PLL_FACTOR_N. PLL Factor N. Factor=0, N=1 Factor=1, N=2 Factor=2, N=3 ……

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Factor=127,N=128
7:4	/	/	/
3:0	R/W	0x7	PLL_PREDIV_M. PLL Pre-div Factor(M = Factor+1). The range is from 1 to 16.

3.2.5.4. PLL_VE Control Register

Offset: 0x018			Register Name: PLL_VE_CTRL_REG
Bit	R/W	Default/Hex	Description
31	R/W	0x0	PLL_ENABLE. 0: Disable 1: Enable In the integer mode, The PLL output = (24MHz*N)/M. In the fractional mode, the PLL output is select by bit 25. Note: The PLL output clock must be in the range of 30MHz~600MHz. Its default is 210MHz.
30:29	/	/	/
28	R	0x0	LOCK 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27:26	/	/	/
25	R/W	0x1	FRAC_CLK_OUT. PLL clock output when PLL_MODE_SEL=0(PLL_PREDIV_M factor must be set to 0); No meaning when PLL_MODE_SEL =1. 0: PLLOUT=270MHz 1: PLLOUT=297MHz
24	R/W	0x1	PLL_MODE_SEL. 0: Fractional mode 1: Integer mode Note: When in Fractional mode, the pre-divider M should be set to 0.
23:15	/	/	/
14:8	R/W	0x45	PLL_FACTOR_N. PLL Factor N. Factor=0, N=1 Factor=1, N=2 Factor=2, N=3 …… Factor=31, N=32 … Factor=127, N=128
7:4	/	/	/
3:0	R/W	0x7	PLL_PREDIV_M. PLL Pre-div Factor (M = Factor+1). The range is from 1 to 16.

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.2.5.5. PLL_DDR Control Register

Offset: 0x020			Register Name: PLL_DDR_CTRL_REG
Bit	R/W	Default/Hex	Description
31	R/W	0x0	PLL_ENABLE. 0: Disable 1: Enable This PLL is for DRAM. Set bit20 to validate the PLL after this bit is set to 1. The PLL Output = (24MHz*N*K)/M.
30:29	/	/	/
28	R	0x0	LOCK 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27:25	/	/	/
24	R/W	0x0	SDRAM_SIGMA_DELTA_EN. 0: Disable 1: Enable
23:21	/	/	/
20	R/W	0x0	PLL_DDR_CFG_UPDATE. PLL_DDR Configuration Update. When PLL_DDR has been changed, this bit should be set to 1 to validate the PLL, otherwise the change would be invalid. And this bit would be cleared automatically after the PLL change is valid. 0: No effect. 1: Validating the PLL_DDR.
19:13	/	/	/
12:8	R/W	0xC	PLL_FACTOR_N. PLL Factor N. Factor=0, N=1 Factor=1, N=2 Factor=2, N=3 …… Factor=31,N=32
7:6	/	/	/
5:4	R/W	0x1	PLL_FACTOR_K. PLL Factor K.(K=Factor + 1) The range is from 1 to 4.
3:2	/	/	/
1:0	R/W	0x1	PLL_FACTOR_M. PLL Factor M.(M = Factor + 1) The range is from 1 to 4.

3.2.5.6. PLL_PERIPH Control Register

Offset: 0x028			Register Name: PLL_PERIPH_CTRL_REG
Bit	R/W	Default/Hex	Description

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

31	R/W	0x0	PLL_ENABLE. 0: Disable 1: Enable The PLL Output = 24MHz*N*K. Note: The PLL Output should be fixed to 600MHz, it is not recommended to vary this value arbitrarily. The PLL output clock must be in the range of 200MHz~1.8GHz. Its default is 600MHz.
30:29	/	/	/
28	R	0x0	LOCK. 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27:19	/	/	/
18	R/W	0x1	PLL_24M_OUT_EN. PLL 24MHz Output Enable. 0: Disable 1: Enable When 25MHz crystal used, this PLL can output 24MHz.
17:16	R/W	0x0	PLL_24M_POST_DIV. PLL 24M Output Clock Post Divider (When 25MHz crystal used). 1/2/3/4.
15:13	/	/	/
12:8	R/W	0x18	PLL_FACTOR_N. PLL Factor N. Factor=0, N=1 Factor=1, N=2 Factor=2, N=3 …… Factor=31,N=32
7:6	/	/	/
5:4	R/W	0x0	PLL_FACTOR_K. PLL Factor K.(K=Factor + 1) The range is from 1 to 4.
3:2	/	/	/
1:0	R/W	0x1	PLL_FACTOR_M. PLL Factor M (M = Factor + 1) is only valid in plltest debug. The PLL_PERIPH back door clock output =24MHz*N*K/M. The range is from 1 to 4.

3.2.5.7. CPU Clock Source Register

Offset: 0x050			Register Name: CPU_CLK_SRC_REG
Bit	R/W	Default/Hex	Description
31:18	/	/	/
17:16	R/W	0x1	CPU_CLK_SRC_SEL. CPU Clock Source Select.

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			CPUCLK = CLK Source 00: LOSC 01: OSC24M 1X: PLL_CPU If the clock source is changed, at most to wait for 8 present running clock cycles.
15:0	/	/	/

3.2.5.8. AHB/APB/HCLKC Configuration Register

Offset: 0x054			Register Name: AHB_APB_HCLKC_CFG_REG
Bit	R/W	Default/Hex	Description
31:18	/	/	/
17:16	R/W	0x1	HCLKC_DIV HCLKC Clock Divide Ratio. The clock source is the CPUCLK 00: /1 01: /2 10: /3 11: /4
15:14	/	/	/
13:12	R/W	0x1	AHB_CLK_SRC_SEL. AHB_CLK = AHB_CLK_SRC_SEL/ AHB_CLK_DIV_RATIO 00: LOSC 01: OSC24M 10: CPUCLK 11: PLL_PERIPH/AHB_PRE_DIV
11:10	/	/	/
9:8	R/W	0x0	APB_CLK_RATIO. APB Clock Divide Ratio. APB clock source is AHB clock. APB_CLK = AHB_CLK/ APB_CLK_RATIO 0X: /2 10: /4 11: /8
7:6	R/W	0x0	AHB_PRE_DIV AHB Clock Pre-divide Ratio 00: /1 01: /2 10: /3 11: /4
5:4	R/W	0x1	AHB_CLK_DIV_RATIO. AHB Clock Divide Ratio. 00: /1 01: /2 10: /4

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			11: /8
3:0	/	/	/

3.2.5.9. Bus Clock Gating Register 0

Offset: 0x060			Register Name: BUS_CLK_GATING_REG0
Bit	R/W	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	USB_OTG_GATING. Gating Clock For USB-OTG 0: Mask 1: Pass
23:22	/	/	/
21	R/W	0x0	SPI1_GATING. Gating Clock For SPI1 0: Mask 1: Pass
20	R/W	0x0	SPI0_GATING. Gating Clock For SPI0 0: Mask 1: Pass
19:15	/	/	/
14	R/W	0x0	SDRAM_GATING. Gating Clock For SDRAM 0: Mask 1: Pass
13:10	/	/	/
9	R/W	0x0	SD1_GATING. Gating Clock For SD1 0: Mask 1: Pass
8	R/W	0x0	SD0_GATING. Gating Clock For SD0 0: Mask 1: Pass
7	/	/	/
6	R/W	0x0	DMA_GATING. Gating Clock For DMA 0: Mask 1: Pass
5:0	/	/	/

3.2.5.10. Bus Clock Gating Register 1

Offset: 0x064			Register Name: BUS_CLK_GATING_REG1
Bit	R/W	Default/Hex	Description
31:15	/	/	/

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

14	R/W	0x0	DEFE_GATING. Gating Clock For DEFE 0: Mask 1: Pass
13			
12	R/W	0x0	DEBE_GATING. Gating Clock For DEBE 0: Mask 1: Pass
11	/	/	/
10	R/W	0x0	TVE_GATING. Gating Clock For TVE 0: Mask 1: Pass
9	R/W	0x0	TVD_GATING. Gating Clock For TVD 0: Mask 1: Pass
8	R/W	0x0	CSI_GATING. Gating Clock For CSI 0: Mask 1: Pass
7:6	/	/	/
5	R/W	0x0	DEINTERLACE_GATING. Gating Clock For DE Interlacer 0: Mask 1: Pass
4	R/W	0x0	LCD_GATING. Gating Clock For LCD 0: Mask 1: Pass
3:1	/	/	/
0	R/W	0x0	VE_GATING. Gating Clock For VE 0: Mask 1: Pass

3.2.5.11. Bus Clock Gating Register 2

Offset: 0x068			Register Name: BUS_CLK_GATING_REG2
Bit	R/W	Default/Hex	Description
31:23	/	/	/
22	R/W	0x0	UART2_GATING. Gating Clock For UART2 0: Mask 1: Pass

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

21	R/W	0x0	UART1_GATING. Gating Clock For UART1 0: Mask 1: Pass
20	R/W	0x0	UART0_GATING. Gating Clock For UART0 0: Mask 1: Pass
19	/	/	/
18	R/W	0x0	TWI2_GATING. Gating Clock For TWI2 0: Mask 1: Pass
17	R/W	0x0	TWI1_GATING. Gating Clock For TWI1 0: Mask 1: Pass
16	R/W	0x0	TWI0_GATING. Gating Clock For TWI0 0: Mask 1: Pass
15:13	/	/	/
12	R/W	0x0	DAUDIO_GATING. Gating Clock For DAUDIO 0: Mask 1: Pass
11:4	/	/	/
3	R/W	0x0	RSB_GATING. Gating Clock For RSB 0: Mask 1: Pass
2	R/W	0x0	CIR_GATING. Gating Clock For CIR 0: Mask 1: Pass
1	R/W	0x0	OWA_GATING. Gating Clock For OWA 0: Mask 1: Pass
0	R/W	0x0	AUDIO_CODEC_GATING. Gating Clock For AUDIO_CODEC 0: Mask 1: Pass

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.2.5.12. SDMMC0 Clock Register

Offset: 0x088			Register Name: SDMMC0_CLK_REG
Bit	R/W	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/Divider N/Divider M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL_PERIPH 1X: /
23	/	/	/
22:20	R/W	0x0	SAMPLE_CLK_PHASE_CTR. Sample Clock Phase Control. The sample clock phase delay is based on the number of source clock that is from 0 to 7.
19:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock Pre-Divide Ratio (n) The select clock source is pre-divided by 2^n. The divider is 1/2/4/8.
15:11	/	/	/
10:8	R/W	0x0	OUTPUT_CLK_PHASE_CTR. Output Clock Phase Control. The output clock phase delay is based on the number of source clock that is from 0 to 7.
7:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock Divide Ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.2.5.13. SDMMC1 Clock Register

Offset: 0x08C			Register Name: SDMMC1_CLK_REG
Bit	R/W	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON SCLK= Clock Source/Divider N/Divider M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			01: PLL_PERIPH 1X: /
23	/	/	/
22:20	R/W	0x0	SAMPLE_CLK_PHASE_CTR. Sample Clock Phase Control. The sample clock phase delay is based on the number of source clock that is from 0 to 7.
19:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock Pre-Divide Ratio (n) The select clock source is pre-divided by 2^n. The divider is 1/2/4/8.
15:11	/	/	/
10:8	R/W	0x0	OUTPUT_CLK_PHASE_CTR. Output Clock Phase Control. The output clock phase delay is based on the number of source clock that is from 0 to 7.
7:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock Divide Ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.2.5.14. DAUDIO Clock Register

Offset: 0x0B0			Register Name: DAUDIO_CLK_REG
Bit	R/W	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON
30:18	/	/	/
17:16	R/W	0x0	CLK_SRC_SEL. 00: PLL_AUDIO (8X) 01: PLL_AUDIO(8X)/2 10: PLL_AUDIO(8X)/4 11: PLL_AUDIO(8X)/8
15:0	/	/	/.

3.2.5.15. OWA Clock Register

Offset: 0x0B4			Register Name: OWA_CLK_REG
Bit	R/W	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON
30:18	/	/	/
17:16	R/W	0x1	CLK_SRC_SEL.

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			00: PLL2 (8X) 01: PLL2(8X)/2 10: PLL2(8X)/4 11: PLL2(8X)/8
15:0	/	/	/

3.2.5.16. CIR Clock Register

Offset: 0x0B8			Register Name: CIR_CLK_REG
Bit	R/W	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 100MHz) 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/Divider N/Divider M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: LOSC 01: OSC24M 1X: /
23:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock Pre-divide ratio (n) The select clock source is pre-divided by 2^n. The divider is 1/2/4/8.
15:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.2.5.17. USBPHY Clock Register

Offset: 0x0CC			Register Name: USBPHY_CLK_REG
Bit	R/W	Default/Hex	Description
31:2	/	/	/
1	R/W	0x0	SCLK_GATING. USBPHY 24MHZ Clock Gating 0: Clock is OFF 1: Clock is ON
0	R/W	0x0	USBPHY_RST. USB PHY Reset Control 0: Assert 1: DEBE assert

3.2.5.18. DRAM Gating Register

Offset: 0x100			Register Name: DRAM_GATING_REG
Bit	R/W	Default/Hex	Description

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

31:27	/	/	/
26	R/W	0x0	BE_DCLK_GATING. Gating DRAM SCLK(1X) For BE 0: Mask 1: Pass
25	/	/	/
24	R/W	0x0	FE_DCLK_GATING. Gating DRAM SCLK(1X) For FE 0: Mask 1: Pass
23:4	/	/	/.
3	R/W	0x0	TVD_DCLK_GATING. Gating DRAM SCLK(1X) For TVD 0: Mask 1: Pass
2	R/W	0x0	DEINTERLACE_DCLK_GATING. Gating DRAM SCLK(1X) For DEINTERLACE 0: Mask 1: Pass
1	R/W	0x0	CSI_DCLK_GATING. Gating DRAM SCLK(1X) For CSI 0: Mask 1: Pass
0	R/W	0x0	VE_DCLK_GATING. Gating DRAM SCLK(1X) For VE 0: Mask 1: Pass

3.2.5.19. BE Clock Register

Offset: 0x104			Register Name: BE_CLK_REG
Bit	R/W	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK= Clock Source/Divider M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: PLL_VIDEO 001: / 010: PLL_PERIPH 011~111: /
23:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M.

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.2.5.20. FE Clock Register

Offset: 0x10C			Register Name: FE_CLK_REG
Bit	R/W	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK= Clock Source/Divider M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: PLL_VIDEO 001: / 010: PLL_PERIPH 011~111: /
23:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.2.5.21. TCON Clock Register

Offset: 0x118			Register Name: TCON_CLK_REG
Bit	R/W	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: PLL_VIDEO(1X) 001: / 010: PLL_VIDEO(2X) 011~111: /
23:0	/	/	/

3.2.5.22. De-interlacer Clock Register

Offset: 0x11C			Register Name: DI_CLK_REG
Bit	R/W	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0: Clock is OFF 1: Clock is ON SCLK = Clock Source/ Divider M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: PLL_VIDEO(1X) 001: / 010: PLL_VIDEO(2X) 011~111: /
23:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.2.5.23. TVE Clock Register

Offset: 0x120			Register Name: TVE_CLK_REG
Bit	R/W	Default/Hex	Description
31	R/W	0x0	SCLK2_GATING. Gating Special Clock 2 0: Clock is OFF 1: Clock is ON SCLK2= Clock Source/ Divider M
30:27	/	/	/
26:24	R/W	0x0	SCLK2_SRC_SEL. SClock2 Source Select 000: PLL_VIDEO(1X) 001: / 010: PLL_VIDEO(2X) 011~111: /
23:4	/	/	/
15	R/W	0x0	SCLK1_GATING. Gating Special Clock 1 0: Clock is OFF 1: Clock is ON SCLK = Clock Source
14:10	/	/	/
8	R/W	0x0	SCLK1_SRC_SEL. SClock1 Source Select 0: TVE_SCLK2 1: TVE_SCLK2 divide by 2
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.2.5.24. TVD Clock Register

Offset: 0x124			Register Name: TVD_CLK_REG
Bit	R/W	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/ Divider M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: PLL_VIDEO(1X) 001: OSC24M 010: PLL_VIDEO(2X) 011~111: /
23:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.2.5.25. CSI Clock Register

Offset: 0x134			Register Name: CSI_CLK_REG
Bit	R/W	Default/Hex	Description
31:16	/	/	/
15	R/W	0x0	CSI_MCLK_GATING. Gating Master Clock 0: Clock is OFF 1: Clock is ON SCLK =Master Clock Source/ CSI_MCLK_DIV_M.
14:11	/	/	/
10:8	R/W	0x0	MCLK_SRC_SEL. Master Clock Source Select 000: PLL_VIDEO(1X) 001: / 010:/ 011:/ 100: / 101: OSC24M 110~111:/
7:4	/	/	/
3:0	R/W	0x0	CSI_MCLK_DIV_M. CSI Master Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.2.5.26. VE Clock Register

Offset: 0x13C			Register Name: VE_CLK_REG
Bit	R/W	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. 0: Clock is OFF 1: Clock is ON SCLK = PLL_VE output.
30:0	/	/	/

3.2.5.27. AUDIO CODEC Clock Register

Offset: 0x140			Register Name: AUDIO_CODEC _CLK_REG
Bit	R/W	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = PLL_AUDIO output.
30:0	/	/	/

3.2.5.28. AVS Clock Register

Offset: 0x144			Register Name: AVS_CLK_REG
Bit	R/W	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = OSC24M.
30:0	/	/	/

3.2.5.29. PLL Stable Time Register 0

Offset: 0x200			Register Name: PLL_STABLE_TIME_REG0
Bit	R/W	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x00FF	PLL_LOCK_TIME PLL Lock Time (Unit: us). Note: When any PLL (except PLL_CPU) is enabled or changed, the corresponding PLL lock bit will be set after the PLL Lock Time.

3.2.5.30. PLL Stable Time Register 1

Offset: 0x204			Register Name: PLL_STABLE_TIME_REG1
Bit	R/W	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x00FF	PLL_CPU_LOCK_TIME PLL_CPU Lock Time (Unit: us). Note: When PLL_CPU is enabled or changed, the PLL_CPU lock bit will be set

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			after the PLL_CPU Lock Time.

3.2.5.31. PLL_CPU Bias Register

Offset: 0x220			Register Name: PLL_CPU_BIAS_REG
Bit	R/W	Default/Hex	Description
31	R/W	0x0	VCO_RST. VCO reset In.
30:28	/	/	/
27:24	R/W	0x8	PLL_VCO_BIAS_CTRL. PLL VCO Bias Control[3:0].
23:21	/	/	/
20:16	R/W	0x10	PLL_BIAS_CUR_CTRL. PLL Bias Current Control[4:0].
15:11	/	/	/
10:8	R/W	0x2	PLL_LOCK_CTRL. PLL Lock Time Control[2:0].
7:4	/	/	/
3:0	R/W	0x0	PLL_DAMP_FACT_CTRL. PLL Damping Factor Control[3:0].

3.2.5.32. PLL_AUDIO Bias Register

Offset: 0x224			Register Name: PLL_AUDIO_BIAS_REG
Bit	R/W	Default/Hex	Description
31:29	/	/	/
28:24	R/W	0x10	PLL_VCO_BIAS. PLL VCO Bias Current[4:0].
23:21	/	/	/
20:16	R/W	0x10	PLL_BIAS_CUR. PLL Bias Current[4:0].
15:0	/	/	/

3.2.5.33. PLL_VIDEO Bias Register

Offset: 0x228			Register Name: PLL_VIDEO_BIAS_REG
Bit	R/W	Default/Hex	Description
31:29	/	/	/
28:24	R/W	0x10	PLL_VCO_BIAS_CTRL. PLL VCO Bias Control[4:0].
23:21	/	/	/
20:16	R/W	0x10	PLL_BIAS_CTRL. PLL Bias Control[4:0].
15:3	/	/	/
2:0	R/W	0x0	PLL_DAMP_FACTOR_CTRL. PLL Damping Factor Control[2:0].

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.2.5.34. PLL_VE Bias Register

Offset: 0x22C			Register Name: PLL_VE_BIAS_REG
Bit	R/W	Default/Hex	Description
31:29	/	/	/
28:24	R/W	0x10	PLL_VCO_BIAS_CTRL. PLL VCO Bias Control[4:0].
23:21	/	/	/
20:16	R/W	0x10	PLL_BIAS_CTRL. PLL Bias Control[4:0].
15:3	/	/	/
2:0	R/W	0x0	PLL_DAMP_FACTOR_CTRL. PLL Damping Factor Control[2:0].

3.2.5.35. PLL_DDR Bias Register

Offset: 0x230			Register Name: PLL_DDR_BIAS_REG
Bit	R/W	Default/Hex	Description
31:28	R/W	0x8	PLL_VCO_BIAS. PLL VCO Bias[3:0].
27:26	/	/	/.
25	R/W	0x0	PLL_VCO_GAIN_CTRL_EN. PLL VCO Gain Control Enable. 0: Disable 1: Enable
24	R/W	0x1	PLL_BANDW_CTRL. PLL Band Width Control. 0: Narrow 1: Wide
23:21	/	/	/
20:16	R/W	0x10	PLL_BIAS_CUR_CTRL. PLL Bias Current Control.
15	/	/	/
14:12	R/W	0x4	PLL_VCO_GAIN_CTRL. PLL VCO Gain Control Bit[2:0].
11:4	/	/	/
3:0	R/W	0x0	PLL_DAMP_FACTOR_CTRL. PLL Damping Factor Control[3:0].

3.2.5.36. PLL_PERIPH Bias Register

Offset: 0x234			Register Name: PLL_PERH_BIAS_REG
Bit	R/W	Default/Hex	Description
31:29	/	/	/
28:24	R/W	0x10	PLL_VCO_BIAS. PLL VCO Bias[4:0].
23:21	/	/	/
20:16	R/W	0x10	PLL_BIAS_CUR_CTRL.

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			PLL Bias Current Control.
15:5	/	/	/
4	R/W	0x1	PLL_BANDW_CTRL. PLL Band Width Control. 0: Narrow 1: Wide.
3:2	/	/	/
1:0	R/W	0x0	PLL_DAMP_FACTOR_CTRL. PLL Damping Factor Control[1:0].

3.2.5.37. PLL_CPU Tuning Register

Offset: 0x250			Register Name: PLL_CPU_TUN_REG
Bit	R/W	Default/Hex	Description
31:28	/	/	/
27	R/W	0x1	PLL_BAND_WID_CTRL. PLL Band Width Control. 0: Narrow 1: Wide
26	R/W	0x0	VCO_GAIN_CTRL_EN. VCO Gain Control Enable. 0: Disable 1: Enable
25:23	R/W	0x4	VCO_GAIN_CTRL. VCO Gain Control Bits[2:0].
22:16	R/W	0x10	PLL_INIT_FREQ_CTRL. PLL Initial Frequency Control[6:0].
15	R/W	0x0	C_OD. C-Reg-Od For Verify.
14:8	R/W	0x10	C_B_IN. C-B-In[6:0] For Verify.
7	R/W	0x0	C_OD1. C-Reg-Od1 For Verify.
6:0	R	0x0	C_B_OUT. C-B-Out[6:0] For Verify.

3.2.5.38. PLL_DDR Tuning Register

Offset: 0x260			Register Name: PLL_DDR_TUN_REG
Bit	R/W	Default/Hex	Description
31:29	/	/	/
28	R/W	0x1	VREG1_OUT_EN. Vreg1 Out Enable. 0: Disable 1: Enable
27	/	/	/
26:24	R/W	0x4	PLL_LTIME_CTRL.

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			PLL Lock Time Control[2:0].
23	R/W	0x0	VCO_RST. VCO Reset In.
22:16	R/W	0x10	PLL_INIT_FREQ_CTRL. PLL Initial Frequency Control[6:0].
15	R/W	0x0	OD1. Reg-Od1 For Verify.
14:8	R/W	0x10	B_IN. B-In[6:0] For Verify.
7	R/W	0x0	OD. Reg-Od For Verify.
6:0	R	0x0	B_OUT. B-Out[6:0] For Verify.

3.2.5.39. PLL_AUDIO Pattern Control Register

Offset: 0x284			Register Name: PLL_AUDIO_PAT_CTRL_REG
Bit	R/W	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma-Delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 1X: Triangular
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	/	/	/
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

3.2.5.40. PLL_VIDEO Pattern Control Register

Offset: 0x288			Register Name: PLLVIDEO_PAT_CTRL_REG
Bit	R/W	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma-Delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1X: Triangular
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	/	/	/
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

3.2.5.41. PLL_DDR Pattern Control Register

Offset: 0x290			Register Name: PLLDDR_PAT_CTRL_REG
Bit	R/W	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma-Delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 1X: Triangular
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	/	/	/
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

3.2.5.42. Bus Software Reset Register 0

Offset: 0x02C0			**Register Name: BUS_SOFT_RST_REG0**
Bit	R/W	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	USBOTG_RST. USBOTG Reset. 0: Assert 1: De-assert
23:22			
21	R/W	0x0	SPI1_RST.

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			SPI1 Reset. 0: Assert 1: De-assert
20	R/W	0x0	SPI0_RST. SPI0 Reset. 0: Assert 1: De-assert
19:15	/	/	/
14	R/W	0x0	SDRAM_RST. SDRAM Reset. 0: Assert 1: De-assert
13:10	/	/	/
9	R/W	0x0	SD1_RST. SD/MMC 1 Reset. 0: Assert 1: De-assert
8	R/W	0x0	SD0_RST. SD/MMC 0 Reset. 0: Assert 1: De-assert
7	/	/	/
6	R/W	0x0	DMA_RST. DMA Reset. 0: Assert 1: De-assert
5:0	/	/	/

3.2.5.43. Bus Software Reset Register 1

Offset: 0x2C4			Register Name: BUS_SOFT_RST_REG1
Bit	R/W	Default/Hex	Description
31:15	/	/	/
14	R/W	0x0	DEFE_RST. DEFE Reset. 0: Assert 1: De-assert
13	/	/	/
12	R/W	0x0	DEBE_RST. DEBE Reset. 0: Assert 1: De-assert
11	/	/	/
10	R/W	0x0	TVE_RST. TVE Reset. 0: Assert

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: De-assert
9	R/W	0x0	TVD_RST. TVD Reset. 0: Assert 1: De-assert
8	R/W	0x0	CSI_RST. CSI Reset. 0: Assert 1: De-assert
7:6	/	/	
5	R/W	0x0	DEINTERLACE_RST. DEINTERLACE Reset. 0: Assert 1: De-assert
4	R/W	0x0	LCD_RST. LCD Reset. 0: Assert 1: De-assert
3:1	/	/	/
0	R/W	0x0	VE_RST. VE Reset. 0: Assert 1: De-assert

3.2.5.44. Bus Software Reset Register 2

Offset: 0x2D0			Register Name: BUS_SOFT_RST_REG2
Bit	R/W	Default/Hex	Description
31:23	/	/	/
22	R/W	0x0	UART2_RST. UART2 Reset. 0: Assert 1: De-assert
21	R/W	0x0	UART1_RST. UART1 Reset. 0: Assert 1: De-assert
20	R/W	0x0	UART0_RST. UART0 Reset. 0: Assert 1: De-assert
19	/	/	/
18	R/W	0x0	TWI2_RST. TWI2 Reset. 0: Assert 1: De-assert

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

17	R/W	0x0	TWI1_RST. TWI1 Reset. 0: Assert 1: De-assert
16	R/W	0x0	TWI0_RST. TWI0 Reset. 0: Assert 1: De-assert
15:13	/	/	/
12	R/W	0x0	DAUDIO_RST. DAUDIO Reset. 0: Assert 1: De-assert
11:4	/	/	/
3	R/W	0x0	RSB_RST. RSB Reset. 0: Assert 1: De-assert
2	R/W	0x0	CIR_RST. CIR Reset. 0: Assert 1: De-assert
1	R/W	0x0	OWA_RST. OWA Reset. 0: Assert 1: De-assert
0	R/W	0x0	AUDIO_CODEC_RST. AUDIO_CODEC Reset. 0: Assert 1: De-assert

3.2.6. Programming Guidelines

3.2.6.1. PLL

1) In practice, other PLLs doesn't support dynamic frequency scaling except for CPU
2) After the PLL_DDR frequency changes, the 20-bit of PLL_DDR Control Register should be written 1 to make it valid;

3.2.6.2. BUS

1) When setting the BUS clock, you should set the division factor first, and after the division factor becomes valid, switch the clock source. The clock source will be switched after at least three clock cycles;
2) The BUS clock should not be dynamically changed in most applications.

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.3. Timer

3.3.1. Overview

Timer 0/1/2 can take their inputs from LOSC or OSC24M. They provide the operating system's scheduler interrupt. It is designed to offer maximum accuracy and efficient management, even for systems with long or short response time. They provide 32-bit programmable down-counter and work in auto-reload mode or no-reload mode. When the current value in Current Value Register is counting down to zero, the timer will generate interrupt if set interrupt enable bit.

The watchdog is used to resume the controller operation when it had been disturbed by malfunctions such as noise and system errors. It features a down counter that allows a watchdog period of up to 16 seconds (512000 cycles). It can generate a general reset or interrupt request.

AVS counter is used to synchronize video and audio in the player.

3.3.2. Feature

The Timer module includes the following features:

- 3 timers for system scheduler counting using 24MHz or LOSC clock
- Each Timer could general individual interrupt
- 1 Watchdog for resetting whole system or interrupt
- 2 AVS counters used for synchronize video and audio in the player

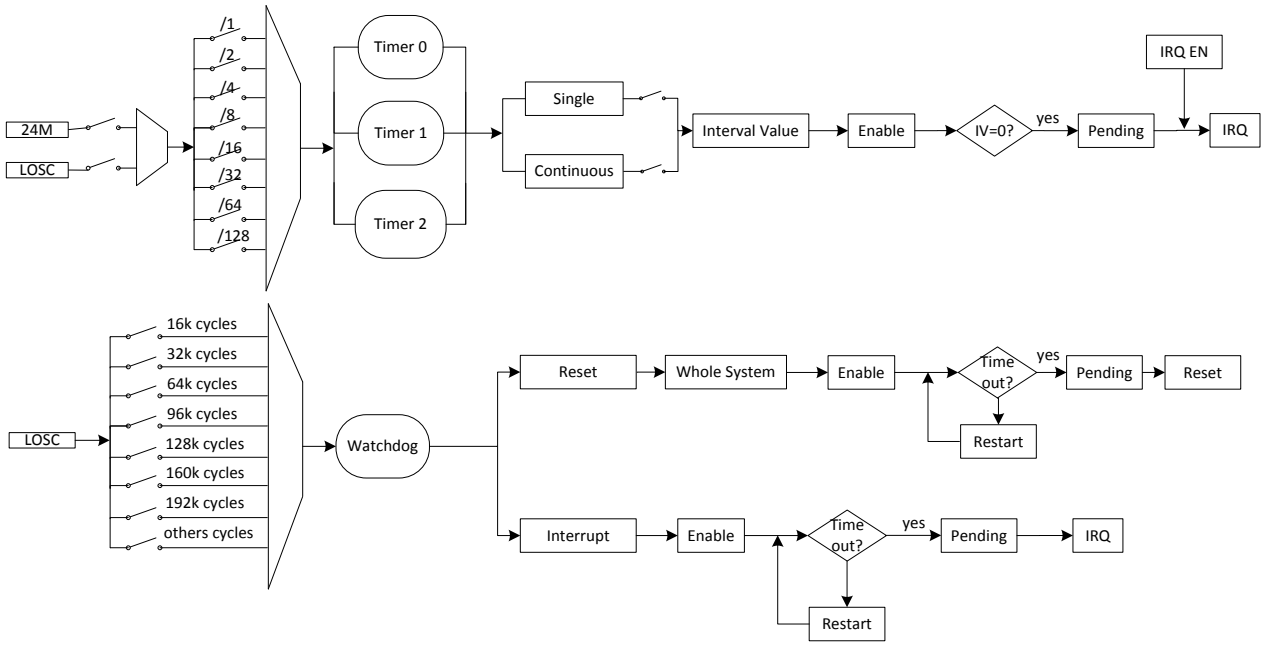
3.3.3. Functionalities Description

3.3.3.1. Typical Applications

- Timer provides scheduler interrupt and delay or calculates external devices' frequency
- The watchdog supports reset function for system operation' malfunction
- AVS is used to synchronize video and audio in the player

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.3.3.2. Functional Block Diagram



Timer function structure and work flow

Timer counter' clock input comes from one of the three clock sources that could be pre-scaled up to 128 division. In single mode, when current value is counted down to 0, enable bit would be cleared automatically and Timer stops working. But in continuous mode, Interval Value will be auto-reloaded into *Current Value Register* and then counter counts from the new interval value again when current value is counted down to 0. Every time current value is counted down to 0, a pending will be generated. Pending could be sent to INTC only if IRQ enable bit is set.

Generally watchdog could not count down to 0 because it would be restart inside Interval Value. Otherwise the malfunction makes the watchdog counts down to 0 and a pending will be generated, which causes a reset (*Watchdog Configuration Register* is configured to whole system) or an interrupt (*Watchdog Configuration Register* is configured to only interrupt).

AVS has two counters which are both up-counted. The counter' clock source comes from 24MHz/Divisor_N and Divisor_N is set in *AVS Counter Divisor Register.* AVS counter could be changed to pause or enable at any time.

3.3.4. Timer Register List

Module Name	Base Address
TIMER	0x01C20C00

Register Name	Offset	Description
TMR_IRQ_EN_REG	0x00	Timer IRQ Enable Register
TMR_IRQ_STA_REG	0x04	Timer Status Register
TMR0_CTRL_REG	0x10	Timer 0 Control Register
TMR0_INTV_VALUE_REG	0x14	Timer 0 Interval Value Register
TMR0_CUR_VALUE_REG	0x18	Timer 0 Current Value Register
TMR1_CTRL_REG	0x20	Timer 1 Control Register

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

TMR1_INTV_VALUE_REG	0x24	Timer 1 Interval Value Register
TMR1_CUR_VALUE_REG	0x28	Timer 1 Current Value Register
TMR2_CTRL_REG	0x30	Timer 2 Control Register
TMR2_INTV_VALUE_REG	0x34	Timer 2 Interval Value Register
TMR2_CUR_VALUE_REG	0x38	Timer 2 Current Value Register
AVS_CNT_CTL_REG	0x80	AVS Counter Control Register
AVS_CNT0_REG	0x84	AVS Counter 0 Register
AVS_CNT1_REG	0x88	AVS Counter 1 Register
AVS_CNT_DIV_REG	0x8C	AVS Counter Divisor Register
WDOG_IRQ_EN_REG	0xA0	Watchdog IRQ Enable Register
WDOG_IRQ_STA_REG	0xA4	Watchdog Status Register
WDOG_CTRL_REG	0xB0	Watchdog Control Register
WDOG_CFG_REG	0xB4	Watchdog Configuration Register
WDOG_MODE_REG	0xB8	Watchdog Mode Register

3.3.5. Timer Register Description

3.3.5.1. Timer IRQ Enable Register

Offset:0x0			Register Name: TMR_IRQ_EN_REG
Bit	R/W	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	TMR2_IRQ_EN. Timer 2 Interrupt Enable. 0: No effect, 1: Timer 2 Interval Value reached interrupt enable.
1	R/W	0x0	TMR1_IRQ_EN. Timer 1 Interrupt Enable. 0: No effect, 1: Timer 1 Interval Value reached interrupt enable.
0	R/W	0x0	TMR0_IRQ_EN. Timer 0 Interrupt Enable. 0: No effect, 1: Timer 0 Interval Value reached interrupt enable.

3.3.5.2. Timer IRQ Status Register

Offset:0x04			Register Name: TMR_IRQ_STA_REG
Bit	R/W	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	TMR2_IRQ_PEND. Timer 2 IRQ Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending, timer 2 interval value is reached.
1	R/W	0x0	TMR1_IRQ_PEND. Timer 1 IRQ Pending. Set 1 to the bit will clear it.

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0: No effect, 1: Pending, timer 1 interval value is reached.
0	R/W	0x0	TMR0_IRQ_PEND. Timer 0 IRQ Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending, timer 0 interval value is reached.

3.3.5.3. Timer 0 Control Register

Offset:0x10			Register Name: TMR0_CTRL_REG
Bit	R/W	Default/Hex	Description
31:8	/	/	/
7	R/W	0x0	TMR0_MODE. Timer 0 mode. 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
6:4	R/W	0x0	TMR0_CLK_PRES. Select the pre-scale of timer 0 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
3:2	R/W	0x1	TMR0_CLK_SRC. Timer 0 Clock Source. 00: LOSC 01: OSC24M 10: / 11: /
1	R/W	0x0	TMR0_RELOAD. Timer 0 Reload. 0: No effect 1: Reload timer 0 Interval value After the bit is set, it can not be written again before it's cleared automatically.
0	R/W	0x0	TMR0_EN. Timer 0 Enable. 0: Stop/Pause, 1: Start. If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to "0", the current value counter will pause. At least wait for 2 cycles, the start bit

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

3.3.5.4. Timer 0 Interval Value Register

Offset:0x14			Register Name: TMR0_INTV_VALUE_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0x0	TMR0_INTV_VALUE. Timer 0 Interval Value.

Note:

1) The value setting should consider the system clock and the timer clock source.

3.3.5.5. Timer 0 Current Value Register

Offset:0x18			Register Name: TMR0_CUR_VALUE_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0x0	TMR0_CUR_VALUE. Timer 0 Current Value.

Note:

1) Timer 0 current value is a 32-bit down-counter (from interval value to 0).

3.3.5.6. Timer 1 Control Register

Offset:0x20			Register Name: TMR1_CTRL_REG
Bit	R/W	Default/Hex	Description
31:8	/	/	/
7	R/W	0x0	TMR1_MODE. Timer 1 mode. 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
6:4	R/W	0x0	TMR1_CLK_PRES. Select the pre-scale of timer 1 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
3:2	R/W	0x1	TMR1_CLK_SRC. Timer 1 Clock Source. 00: LOSC

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			01: OSC24M. 10: / 11: /
1	R/W	0x0	TMR1_RELOAD. Timer 1 Reload. 0: No effect 1: Reload timer 1 Interval value After the bit is set, it can not be written again before it's cleared automatically.
0	R/W	0x0	TMR1_EN. Timer 1 Enable. 0: Stop/Pause, 1: Start. If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to "0", the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

3.3.5.7. Timer 1 Interval Value Register

Offset:0x24			Register Name: TMR1_INTV_VALUE_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0x0	TMR1_INTV_VALUE. Timer 1 Interval Value.

Note:

1) The value setting should consider the system clock and the timer clock source.

3.3.5.8. Timer 1 Current Value Register

Offset:0x28			Register Name: TMR1_CUR_VALUE_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0x0	TMR1_CUR_VALUE. Timer 1 Current Value.

3.3.5.9. Timer 2 Control Register

Offset:0x30			Register Name: TMR2_CTRL_REG
Bit	R/W	Default/Hex	Description
31:8	/	/	/
7	R/W	0x0	TMR2_MODE. Timer 2 mode. 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

6:4	R/W	0x0	TMR2_CLK_PRES. Select the pre-scale of timer 2 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
3:2	R/W	0x1	TMR2_CLK_SRC. Timer 2 Clock Source. 00: LOSC 01: OSC24M 10: / 11: /.
1	R/W	0x0	TMR2_RELOAD. Timer 2 Reload. 0: No effect 1: Reload timer 1 Interval value After the bit is set, it can not be written again before it's cleared automatically.
0	R/W	0x0	TMR2_EN. Timer 2 Enable. 0: Stop/Pause, 1: Start. If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to "0", the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

3.3.5.10. Timer 2 Interval Value Register

Offset:0x34			Register Name: TMR2_INTV_VALUE_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0x0	TMR2_INTV_VALUE. Timer 2 Interval Value.

Note:

1) The value setting should consider the system clock and the timer clock source.

3.3.5.11. Timer 2 Current Value Register

Offset:0x38			Register Name: TMR2_CUR_VALUE_REG
Bit	R/W	Default/Hex	Description

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

31:0	R/W	0x0	TMR2_CUR_VALUE. Timer 2 Current Value.

Note:

1) Timer 2 current value is a 32-bit down-counter (from interval value to 0).

3.3.5.12. AVS Counter Control Register

Offset:0x80			Register Name: AVS_CNT_CTL_REG
Bit	R/W	Default/Hex	Description
31:10	/	/	/
9	R/W	0x0	AVS_CNT1_PS. Audio/Video Sync Counter 1 Pause Control 0: Not pause 1: Pause Counter 1
8	R/W	0x0	AVS_CNT0_PS. Audio/Video Sync Counter 0 Pause Control 0: Not pause 1: Pause Counter 0
7:2	/	/	/
1	R/W	0x0	AVS_CNT1_EN. Audio/Video Sync Counter 1 Enable/ Disable. The counter source is OSC24M. 0: Disable 1: Enable
0	R/W	0x0	AVS_CNT0_EN. Audio/Video Sync Counter 1 Enable/ Disable. The counter source is OSC24M. 0: Disable 1: Enable

3.3.5.13. AVS Counter 0 Register

Offset:0x84			Register Name: AVS_CNT0_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0x0	AVS_CNT0. Counter 0 for Audio/ Video Sync Application The high 32 bits of the internal 33-bits counter register. The initial value of the internal 33-bits counter register can be set by software. The LSB bit of the 33-bits counter register should be zero when the initial value is updated. It will count from the initial value. The initial value can be updated at any time. It can also be paused by setting AVS_CNT0_PS to '1'. When it is paused, the counter won't increase.

3.3.5.14. AVS Counter 1 Register

Offset:0x88			Register Name: AVS_CNT1_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0x0	AVS_CNT1. Counter 1 for Audio/ Video Sync Application The high 32 bits of the internal 33-bits counter register. The initial value of the

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			internal 33-bits counter register can be set by software. The LSB bit of the 33-bits counter register should be zero when the initial value is updated. It will count from the initial value. The initial value can be updated at any time. It can also be paused by setting AVS_CNT1_PS to '1'. When it is paused, the counter won't increase.

3.3.5.15. AVS Counter Divisor Register

Offset:0x8C			Register Name: AVS_CNT_DIV_REG
Bit	R/W	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0x5DB	AVS_CNT1_D. Divisor N for AVS Counter 1 AVS CN1 CLK=24MHz/Divisor_N1. Divisor N1 = Bit [27:16] + 1. The number N is from 1 to 0x7ff. The zero value is reserved. The internal 33-bits counter engine will maintain another 12-bits counter. The 12-bits counter is used for counting the cycle number of one 24Mhz clock. When the 12-bits counter reaches (>= N) the divisor value, the internal 33-bits counter register will increase 1 and the 12-bits counter will reset to zero and restart again. *Note*: It can be configured by software at any time.
15:12	/	/	/
11:0	R/W	0x5DB	AVS_CNT0_D. Divisor N for AVS Counter 0 AVS CN0 CLK=24MHz/Divisor_N0. Divisor N0 = Bit [11:0] + 1 The number N is from 1 to 0x7ff. The zero value is reserved. The internal 33-bits counter engine will maintain another 12-bits counter. The 12-bits counter is used for counting the cycle number of one 24Mhz clock. When the 12-bits counter reaches (>= N) the divisor value, the internal 33-bits counter register will increase 1 and the 12-bits counter will reset to zero and restart again. *Note*: It can be configured by software at any time.

3.3.5.16. Watchdog IRQ Enable Register

Offset:0xA0			Register Name: WDOG_IRQ_EN_REG
Bit	R/W	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	WDOG_IRQ_EN. Watchdog Interrupt Enable. 0: No effect, 1: Watchdog interrupt enable.

3.3.5.17. Watchdog Status Register

Offset:0xA4			Register Name: WDOG_IRQ_STA_REG
Bit	R/W	Default/Hex	Description

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

31:1	/	/	/
0	R/W	0x0	WDOG_IRQ _PEND. Watchdog IRQ Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending, Watchdog interval value is reached.

3.3.5.18. Watchdog Control Register

Offset:0xB0			Register Name: WDOG_CTRL_REG
Bit	R/W	Default/Hex	Description
31:13	/	/	/
12:1	R/W	0x0	WDOG_KEY_FIELD. Watchdog Key Field. Should be written at value 0xA57. Writing any other value in this field aborts the write operation.
0	R/W	0x0	WDOG_RSTART. Watchdog Restart. 0: No effect, 1: Restart the Watchdog.

3.3.5.19. Watchdog Configuration Register

Offset:0xB4			Register Name: WDOG_CFG_REG
Bit	R/W	Default/Hex	Description
31:2	/	/	/
1:0	R/W	0x1	WDOG_CONFIG. 00: / 01: to whole system 10: only interrupt 11: /

3.3.5.20. Watchdog Mode Register

Offset:0xB8			Register Name: WDOG_MODE_REG
Bit	R/W	Default/Hex	Description
31:8	/	/	/
7:4	R/W	0x0	WDOG_INTV_VALUE. Watchdog Interval Value. Watchdog clock source is *LOSC*. If the clock source is turned off, Watchdog will not work. 0000: 16000 cycles (0.5s) 0001: 32000 cycles (1s) 0010: 64000 cycles (2s) 0011: 96000 cycles (3s) 0100: 128000 cycles (4s) 0101: 160000 cycles (5s) 0110: 192000 cycles (6s) 0111: 256000 cycles (8s) 1000: 320000 cycles (10s) 1001: 384000 cycles (12s)

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1010: 448000 cycles (14s) 1011: 512000 cycles (16s) others: /
3:1	/	/	/
0	R/W	0x0	WDOG_EN. Watchdog Enable. 0: No effect 1: Enable the Watchdog.

3.3.6. Programming Guidelines

3.3.6.1. Timer

Here takes Timer 0 for an example: 1ms delay, 24MHz clock source, Single mode, 2 prescale:

```
writel(0x2EE0,TMR_0_INTV);                  //Set interval value
writel(0x94, TMR_0_CTRL);                   //Select Single mode,24MHz clock source,2 pre-scale
writel(readl(TMR_0_CTRL)|(1<<1), TMR_0_CTRL);  //Set Reload bit
while((readl(TMR_0_CTRL)>>1)&1);            //Waiting Reload bit turns to 0
writel(readl(TMR_0_CTRL)|(1<<0), TMR_0_CTRL);  //Enable Timer0
```

3.3.6.2. Watchdog

Here is an example: 24M/750 as clock source, interval value is 1s, watchdog configuration to whole system, 500ms delay from watchdog enable to watchdog restart.

```
writel(0x1, WDOG_CONFIG);                   //To whole system
writel(0x10, WDOG_MODE);                    //Interval Value set 1s
writel(readl(WDOG_MODE)|(1<<0), WDOG_MODE);  //Enable Watchdog
delay_ms(500);                              //Delay 500ms
writel(readl(WDOG_CTRL)|(0xA57<<1)|(1<<0)，WDOG_CTRL); //Writel 0xA57 at Key Field and Restart Watchdog
……After 1s, Watchdog will general a pending, which would reset the system……
```

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.4. PWM

3.4.1. Overview

The output of the PWM is a toggling signal whose frequency and duty cycle can be modulated by its programmable registers. Each channel has a dedicated internal 16-bit up counter. If the counter reaches the value stored in the channel period register, it resets. At the beginning of a count period cycle, the PWMOUT is set to active state and count from 0x0000.

The PWM divider divides the clock (24MHz) by 1~4096 according to the pre-scalar bits in the PWM control register.

In PWM cycle mode, the output will be a square waveform; the frequency is set to the period register. In PWM pulse mode, the output will be a positive pulse or a negative pulse.

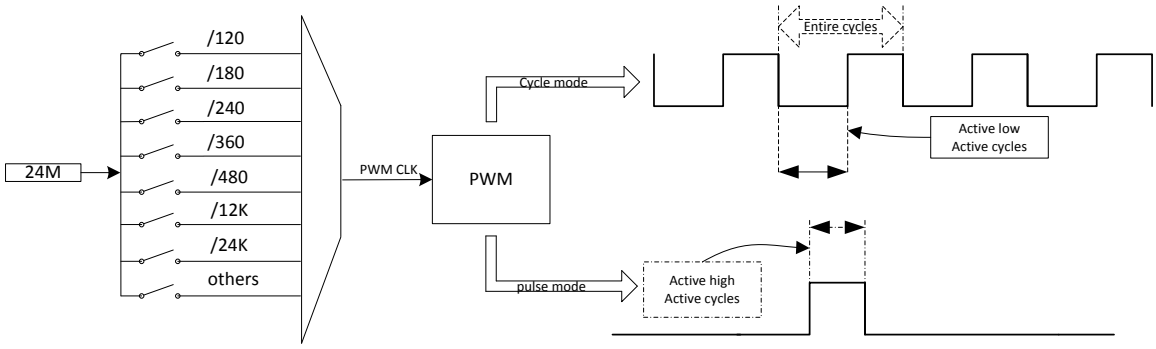
3.4.2. Feature

The PWM includes the following features:

- 2 PWM channels supported and 1 output pin for PWM1/2 channel each
- Support outputting 2 kinds of waveform: square waveform and pulse waveform
- Support 0% to 100% adjustable duty cycle
- Support 0Hz minimum output frequency and 24MHz maximum output frequency

3.4.3. Functionalities Description

3.4.3.1. Functional Block Diagram



PWM output waveform

When PWM is enabled, the PWM can output two signals from corresponding pins. PWM clock comes from the clock pre-scaled form 24MHz. In cycle mode, PWM outputs square waveform whose entire cycles length and active cycles length are decided by period register. And in pulse mode, PWM output a pulse waveform and the pulse length(active cycles length) is just decide by active cycles on period register. Entire cycles length and active cycles length could be counted out from the following formulas:

Entire cycles length = entire cycles / PWM CLK

Active cycles length = active cycles / PWM CLK

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.4.4. Operation Principle

3.4.4.1. PWM output pins

Before using PWM, it is necessary to configure PWM output at the corresponding pin. There are several pins which could be configured for PWM output for each PWM channel. Take configuring PWM1 output for an example, both PE6 pin and PF5 pin could be configured for PWM output.

3.4.5. PWM Register List

Module Name	Base Address
PWM	0x01C21000

Register Name	Offset	Description
PWM_CTRL_REG	0x00	PWM Control Register
PWM_CH0_PERIOD	0x04	PWM Channel 0 Period Register
PWM_CH1_PERIOD	0x08	PWM Channel 1 Period Register

3.4.6. PWM Register Description

3.4.6.1. PWM Control Register

Offset: 0x0			Register Name: PWM_CTRL_REG
Bit	R/W	Default/Hex	Description
31:30	/	/	/
29	RO	0x0	PWM1_RDY. PWM1 period register ready. 0: PWM1 period register is ready to write 1: PWM1 period register is busy
28	RO	0x0	PWM0_RDY. PWM0 period register ready. 0: PWM0 period register is ready to write 1: PWM0 period register is busy
27:25	/	/	/
24	R/W	0x0	PWM1_BYPASS. PWM CH1 bypass enable. If the bit is set to 1, PWM1's output is OSC24MHz. 0: Disable 1: Enable
23	R/W	0x0	PWM_CH1_PULSE_OUT_START. PWM Channel 1 pulse output start. 0: No effect 1: Output 1 pulse The pulse width should be according to the period 1 register [15:0], and the pulse state should be according to the active state. After the pulse is finished, the bit will be cleared automatically.

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

22	R/W	0x0	PWM_CH1_MODE. PWM Channel 1 mode. 0: Cycle mode 1: Pulse mode
21	R/W	0x0	PWM_CH1_CLK_GATING Gating the Special Clock for PWM1 (0: mask, 1: pass).
20	R/W	0x0	PWM_CH1_ACT_STATE. PWM Channel 1 Active State. 0: Low Level 1: High Level
19	R/W	0x0	PWM_CH1_EN. PWM Channel 1 Enable. 0: Disable 1: Enable
18:15	R/W	0x0	PWM_CH1_PRESCAL. PWM Channel 1 Pre-scalar. These bits should be setting before the PWM Channel 1 clock gate on. 0000: /120 0001: /180 0010: /240 0011: /360 0100: /480 0101: / 0110: / 0111: / 1000: /12k 1001: /24k 1010: /36k 1011: /48k 1100: /72k 1101: / 1110: / 1111: /1
14:10	/	/	/
9	R/W	0x0	PWM0_BYPASS. PWM CH0 bypass enable. If the bit is set to 1, PWM0's output is OSC24MHz. 0: Disable 1: Enable
8	R/W	0x0	PWM_CH0_PUL_START. PWM Channel 0 pulse output start. 0: No effect, 1: Output 1 pulse. The pulse width should be according to the period 0 register [15:0], and the pulse state should be according to the active state.

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			After the pulse is finished, the bit will be cleared automatically.
7	R/W	0x0	PWM_CHANNEL0_MODE. 0: Cycle mode, 1: Pulse mode.
6	R/W	0x0	SCLK_CH0_GATING. Gating the Special Clock for PWM0 (0: mask, 1: pass).
5	R/W	0x0	PWM_CH0_ACT_STA. PWM Channel 0 Active State. 0: Low Level 1: High Level
4	R/W	0x0	PWM_CH0_EN. PWM Channel 0 Enable. 0: Disable 1: Enable
3:0	R/W	0x0	PWM_CH0_PRESCAL. PWM Channel 0 Pre-scalar. These bits should be setting before the PWM Channel 0 clock gate on. 0000: /120 0001: /180 0010: /240 0011: /360 0100: /480 0101: / 0110: / 0111: / 1000: /12k 1001: /24k 1010: /36k 1011: /48k 1100: /72k 1101: / 1110: / 1111: /1

3.4.6.2. PWM Channel 0 Period Register

Offset: 0x04			Register Name: PWM_CH0_PERIOD
Bit	R/W	Default/Hex	Description
31:16	R/W	x	PWM_CH0_ENTIRE_CYS Number of the entire cycles in the PWM clock. 0 = 1 cycle 1 = 2 cycles …… N = N+1 cycles If the register need to be modified dynamically, the PCLK should be faster than the PWM CLK (PWM CLK = 24MHz/pre-scale).

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

15:0	R/W	x	PWM_CH0_ACT_CYS Number of the active cycles in the PWM clock. 0 = 0 cycle 1 = 1 cycles …… N = N cycles

Note:

- The active cycles should be no larger than the entire cycles.

3.4.6.3. PWM Channel 1 Period Register

Offset: 0x08			Register Name: PWM_CH1_PERIOD
Bit	R/W	Default/Hex	Description
31:16	R/W	x	PWM_CH1_ENTIRE_CYS Number of the entire cycles in the PWM clock. 0 = 1 cycle 1 = 2 cycles …… N = N+1 If the register need to be modified dynamically, the PCLK should be faster than the PWM CLK (PWM CLK = 24MHz/pre-scale).
15:0	R/W	x	PWM_CH1_ACT_CYS Number of the active cycles in the PWM clock. 0 = 0 cycle 1 = 1 cycles …… N = N cycles

Note:

- The active cycles should be no larger than the entire cycles.

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.5. INTC

3.5.1. Overview

Interrupt controller (INTC) handles all interrupt sources connected to it. It has a set of registers for managing interrupt sources and interrupt behavior. It provides a priority controller for serving higher interrupt even if a lower interrupt is serving. It also provides a fast forcing way for these interrupt sources which desire to have a fast interrupt request to CPU though they don't generate pending.

3.5.2. Feature

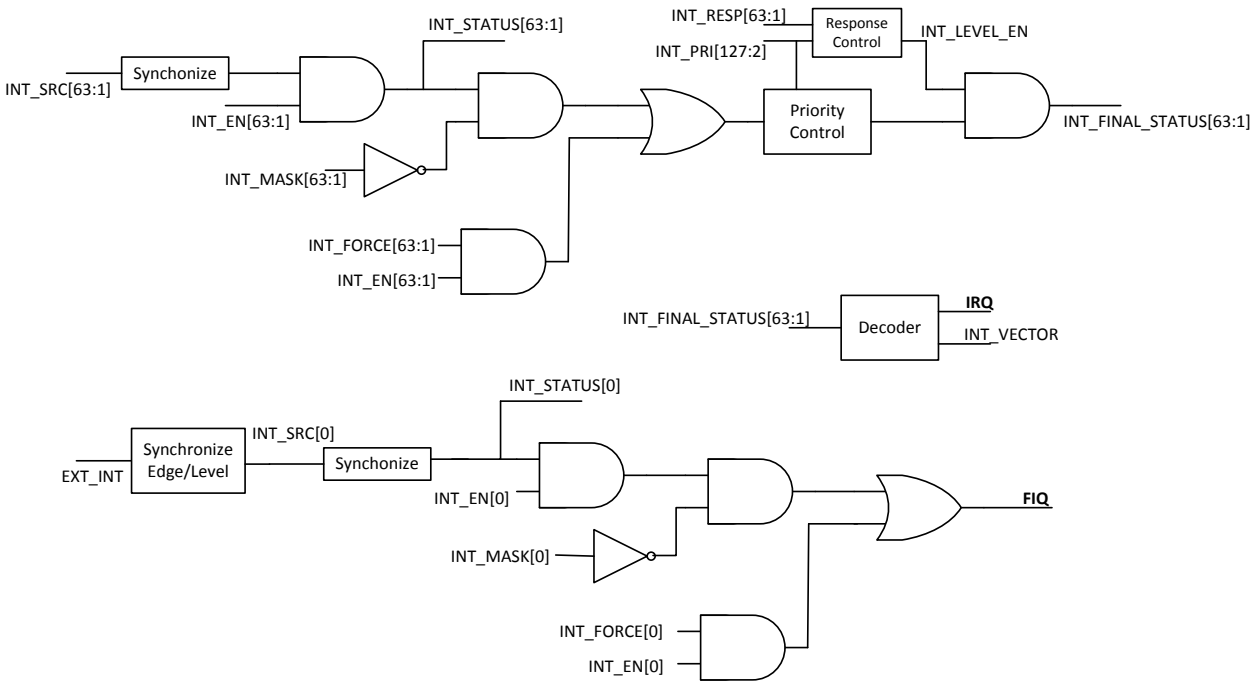
The INTC includes the following features:

- Controls the nIRQ Processor
- Sixty-four individually maskable interrupt sources
- One external NMI interrupt source
- 4-Level Priority Controller
- Thirteen External Sources of Edge-sensitive or Level-sensitive
- Fast Forcing

3.5.3. Functionalities Description

- Handling all interrupt sources for processor connected to INTC

3.5.3.1. Functional Block Diagram



It provides handling of up to sixty-three interrupt sources. The 4-level Priority Controller allows the user to define the priority for each interrupt source, thus permitting higher priority interrupts to be serviced even if a lower priority interrupt is being treated. The fast forcing feature redirects any internal or external source to provide a fast interrupt

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

rather than a normal interrupt.

For an interrupt pending, it becomes 1 when both interrupt source and relevant interrupt enable bit are high level, and if interrupt source or relevant interrupt enable is 0, the pending would become 0. Since NMI is a external interrupt, and it has four interrupt source type, so, after changing the type of interrupt source, its pending should be cleared by set 1 at the end of interrupt service progress.

3.5.4. Interrupt Source

Name	Number	Vector	Description
NMI	0	0x0000	NMI interrupt
UART0	1	0x0004	UART0 interrupt
UART1	2	0x0008	UART1 interrupt
UART2	3	0x000C	UART2 interrupt
/	4	0x0010	/
OWA	5	0x0014	OWA interrupt
CIR	6	0x0018	CIR interrupt
TWI0	7	0x001C	TWI0 interrupt
TWI1	8	0x0020	TWI1 interrupt
TWI2	9	0x0024	TWI2 interrupt
SPI0	10	0x0028	SPI0 interrupt
SPI1	11	0x002C	SPI1 interrupt
/	12	0x0030	/
Timer0	13	0x0034	Timer0 interrupt
Timer1	14	0x0038	Timer1 interrupt
Timer2	15	0x003C	Timer2 interrupt
Watchdog	16	0x0040	Watchdog interrupt
RSB	17	0x0044	RSB interrupt
DMA	18	0x0048	DMA interrupt
	19	0x004C	
Touch Panel	20	0x0050	Touch Panel interrupt
Audio Codec	21	0x0054	Audio Codec interrupt
KEYADC	22	0x0058	KEYADC interrupt
SDC0	23	0x005C	SDC0 interrupt
SDC1	24	0x0060	SDC1 interrupt
/	25	0x0064	/
USB-OTG	26	0x0068	USB-OTG interrupt
TVD	27	0x006C	TVD interrupt
TVE	28	0x0070	TVE interrupt
TCON	29	0x0074	LCD interrupt
DE_FE	30	0x0078	DE_FE interrupt
DE_BE	31	0x007C	DE_BE interrupt
CSI	32	0x0080	CSI interrupt
DE-interlacer	33	0x0084	DE-interlacer interrupt
VE	34	0x0088	VE interrupt

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

Name	Number	Vector	Description
DAUDIO	35	0x008C	DAUDIO interrupt
/	36	0x0090	
/	37	0x0094	/
PIOD	38	0x0098	PIOD interrupt
PIOE	39	0x009C	PIOE interrupt
PIOF	40	0x00A0	PIOF interrupt

3.5.5. INTC Register List

Module Name	Base Address
INTC	0x01C20400

Register Name	Offset	Description
INTC_VECTOR_REG	0x00	Interrupt Vector Register
INTC_BASE_ADDR_REG	0x04	Interrupt Base Address Register
NMI_INT_CTRL_REG	0x0C	NMI Interrupt Control Register
INTC_PEND_REG0	0x10	Interrupt Pending Register 0
INTC_PEND_REG1	0x14	Interrupt Pending Register 1
INTC_EN_REG0	0x20	Interrupt Enable Register 0
INTC_EN_REG1	0x24	Interrupt Enable Register 1
INTC_MASK_REG0	0x30	Interrupt Mask Register 0
INTC_MASK_REG1	0x34	Interrupt Mask Register 1
INTC_RESP_REG0	0x40	Interrupt Response Register 0
INTC_RESP_REG1	0x44	Interrupt Response Register 1
INTC_FF_REG0	0x50	Interrupt Fast Forcing Register 0
INTC_FF_REG1	0x54	Interrupt Fast Forcing Register 1
INTC_PRIO_REG0	0x60	Interrupt Source Priority Register 0
INTC_PRIO_REG1	0x64	Interrupt Source Priority Register 1
INTC_PRIO_REG2	0x68	Interrupt Source Priority Register 2
INTC_PRIO_REG3	0x6C	Interrupt Source Priority Register 3

3.5.6. INTC Register Description

3.5.6.1. Interrupt Vector Register

Offset:0x0			Register Name: INTC_VECTOR_REG
Bit	R/W	Default/Hex	Description
31:2	RO	0x0	INTC_VECTOR_ADDR. This register present the vector address for the interrupt currently active on the CPU IRQ input.
1:0	RO	0x0	Always return zero to this field.

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.5.6.2. Interrupt Base Address Register

Offset:0x4			Register Name: INTC_BASE_ADDR_REG
Bit	R/W	Default/Hex	Description
31:2	R/W	0x0	INTC_BASE_ADDR. This bit-field holds the upper 30 bits of the base address of the vector table.
1:0	RO	0x0	Always write zero to this bit-field.

3.5.6.3. NMI Interrupt Control Register

Offset:0x0C			Register Name: NMI_INT_CTRL_REG
Bit	R/W	Default/Hex	Description
31:2	/	/	/
1:0	R/W	0x0	NMI_SRC_TYPE. External NMI Interrupt Source Type. 00: Low level sensitive 01: Negative edge trigged 10: High level sensitive 11: Positive edge sensitive

3.5.6.4. Interrupt IRQ Pending Register 0

Offset:0x10			Register Name: INTC_PEND_REG0
Bit	R/W	Default/Hex	Description
31:0	R/W	0x0	INTC_PEND0. Interrupt Source [31:0] Pending/Clear Bit. 0: Corresponding interrupt is not pending. 1: Corresponding interrupt is pending

3.5.6.5. Interrupt IRQ Pending Register 1

Offset:0x14			Register Name: INTC_PEND_REG1
Bit	R/W	Default/Hex	Description
31:0	R/W	0x0	INTC_PEND1. Interrupt Source [63:32] Pending/Clear Bit. 0: Corresponding interrupt is not pending. 1: Corresponding interrupt is pending

3.5.6.6. Interrupt Enable Register 0

Offset:0x20			Register Name: INTC_EN_REG0
Bit	R/W	Default/Hex	Description
31:0	R/W	0x0	INTC_EN0. Interrupt Source [31:0] Enable Bits. 0: Corresponding interrupt is disabled. 1: Corresponding interrupt is enabled.

3.5.6.7. Interrupt Enable Register 1

Offset:0x24			Register Name: INTC_EN_REG1
Bit	R/W	Default/Hex	Description

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

31:0	R/W	0x0	INTC_EN1. Interrupt Source [63:32] Enable Bits. 0: Corresponding interrupt is disabled. 1: Corresponding interrupt is enabled.

3.5.6.8. Interrupt Mask Register 0

Offset:0x30			Register Name: INTC_MASK_REG0
Bit	R/W	Default/Hex	Description
31:0	R/W	0x0	INTC_MASK0. Interrupt Source [31:0] Mask Bits. 0: No effect. 1: interrupt is masked. If interrupt is enabled and the interrupt occurred, the interrupt pending bit will be set whether the corresponding interrupt mask bit is set.

3.5.6.9. Interrupt Mask Register 1

Offset:0x34			Register Name: INTC_MASK_REG1
Bit	R/W	Default/Hex	Description
31:0	R/W	0x0	INTC_MASK1. Interrupt Source [63:32] Mask Bits. 0: No effect. 1: interrupt is masked. If interrupt is enabled and the interrupt occurred, the interrupt pending bit will be set whether the corresponding interrupt mask bit is set.

3.5.6.10. Interrupt Response Register 0

Offset:0x40			Register Name: INTC_RESP_REG0
Bit	R/W	Default/Hex	Description
31:0	R/W	0x0	INTC_RESP0. Interrupt Response Bits. If the corresponding bit is set, the interrupt with the lower or the same priority level is masked.

3.5.6.11. Interrupt Response Register 1

Offset:0x44			Register Name: INTC_RESP_REG1
Bit	R/W	Default/Hex	Description
31:0	R/W	0x0	INTC_RESP1. Interrupt Response Bits. If the corresponding bit is set, the interrupt with the lower or the same priority level is masked.

3.5.6.12. Interrupt Fast Forcing Register 0

Offset:0x50			Register Name: INTC_FF_REG0
Bit	R/W	Default/Hex	Description
31:0	R/W	0x0	INTC_FF0.

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Enables the fast forcing feature on the corresponding interrupt source [31:0]. 0: No effect. 1: Forcing the corresponding interrupt. Setting this bit can be valid only when the corresponding interrupt enable bit is set.

3.5.6.13. Interrupt Fast Forcing Register 1

Offset:0x54			Register Name: INTC_FF_REG1
Bit	R/W	Default/Hex	Description
31:0	R/W	0x0	INTC_FF1. Enables the fast forcing feature on the corresponding interrupt source [63:32]. 0: No effect. 1: Forcing the corresponding interrupt. Setting this bit can be valid only when the corresponding interrupt enable bit is set.

3.5.6.14. Interrupt Source Priority Register 0

Offset:0x60			Register Name: INTC_PRIO_REG0
Bit	R/W	Default/Hex	Description
31:30	R/W	0x0	IRQ15_PRIO. IRQ 15 Priority. Set priority level for IRQ 15 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
29:28	R/W	0x0	IRQ14_PRIO. IRQ 14 Priority. Set priority level for IRQ 14 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
27:26	R/W	0x0	IRQ13_PRIO. IRQ 13 Priority. Set priority level for IRQ 13 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
25:24	R/W	0x0	IRQ12_PRIO. IRQ 12 Priority. Set priority level for IRQ 12 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
23:22	R/W	0x0	IRQ11_PRIO. IRQ 11 Priority. Set priority level for IRQ 11 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
21:20	R/W	0x0	IRQ10_PRIO. IRQ 10 Priority. Set priority level for IRQ 10 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
19:18	R/W	0x0	IRQ9_PRIO. IRQ 9 Priority. Set priority level for IRQ 9 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
17:16	R/W	0x0	IRQ8_PRIO. IRQ 8 Priority. Set priority level for IRQ 8 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
15:14	R/W	0x0	IRQ7_PRIO. IRQ 7 Priority. Set priority level for IRQ 7 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
13:12	R/W	0x0	IRQ6_PRIO. IRQ 6 Priority. Set priority level for IRQ 6 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
11:10	R/W	0x0	IRQ5_PRIO.

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			IRQ 5 Priority. Set priority level for IRQ 5 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
9:8	R/W	0x0	IRQ4_PRIO. IRQ 4 Priority. Set priority level for IRQ 4 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
7:6	R/W	0x0	IRQ3_PRIO. IRQ 3 Priority. Set priority level for IRQ 3 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
5:4	R/W	0x0	IRQ2_PRIO. IRQ 2 Priority. Set priority level for IRQ 2 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
3:2	R/W	0x0	IRQ1_PRIO. IRQ 1 Priority. Set priority level for IRQ 1 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
1:0	/	/	/

3.5.6.15. Interrupt Source Priority Register 1

Offset:0x64			Register Name: INTC_PRIO_REG1
Bit	R/W	Default/Hex	Description
31:30	R/W	0x0	IRQ31_PRIO. IRQ 31 Priority. Set priority level for IRQ 31 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Level3 = 0x3 level 3, highest priority
29:28	R/W	0x0	IRQ30_PRIO. IRQ 30 Priority. Set priority level for IRQ 30 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
27:26	R/W	0x0	IRQ29_PRIO. IRQ 29 Priority. Set priority level for IRQ 29 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
25:24	R/W	0x0	IRQ28_PRIO. IRQ 28 Priority. Set priority level for IRQ 28 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
23:22	R/W	0x0	IRQ27_PRIO. IRQ 27 Priority. Set priority level for IRQ 27 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
21:20	R/W	0x0	IRQ26_PRIO. IRQ 26 Priority. Set priority level for IRQ 26 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
19:18	R/W	0x0	IRQ25_PRIO. IRQ 25 Priority. Set priority level for IRQ 25 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
17:16	R/W	0x0	IRQ24_PRIO. IRQ 24 Priority.

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Set priority level for IRQ 24 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
15:14	R/W	0x0	IRQ23_PRIO. IRQ 23 Priority. Set priority level for IRQ 23 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
13:12	R/W	0x0	IRQ22_PRIO. IRQ 22 Priority. Set priority level for IRQ 22 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
11:10	R/W	0x0	IRQ21_PRIO. IRQ 21 Priority. Set priority level for IRQ 21 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
9:8	R/W	0x0	IRQ20_PRIO. IRQ 20 Priority. Set priority level for IRQ 20 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
7:6	R/W	0x0	IRQ19_PRIO. IRQ 19 Priority. Set priority level for IRQ 19 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
5:4	R/W	0x0	IRQ18_PRIO. IRQ 18 Priority. Set priority level for IRQ 18 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
3:2	R/W	0x0	IRQ17_PRIO. IRQ 17 Priority. Set priority level for IRQ 17 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
1:0	R/W	0x0	IRQ16_PRIO. IRQ 16 Priority. Set priority level for IRQ 16 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority

3.5.6.16. Interrupt Source Priority Register 2

Offset:0x68			Register Name: INTC_PRIO_REG2
Bit	R/W	Default/Hex	Description
31:30	R/W	0x0	IRQ47_PRIO. IRQ 47 Priority. Set priority level for IRQ 47 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
29:28	R/W	0x0	IRQ46_PRIO. IRQ 46 Priority. Set priority level for IRQ 46 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
27:26	R/W	0x0	IRQ45_PRIO. IRQ 45 Priority. Set priority level for IRQ 45 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
25:24	R/W	0x0	IRQ44_PRIO. IRQ 44 Priority. Set priority level for IRQ 44 Level0 = 0x0 level 0, lowest priority

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
23:22	R/W	0x0	IRQ43_PRIO. IRQ 43 Priority. Set priority level for IRQ 43 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
21:20	R/W	0x0	IRQ42_PRIO. IRQ 42 Priority. Set priority level for IRQ 42 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
19:18	R/W	0x0	IRQ41_PRIO. IRQ 41 Priority. Set priority level for IRQ 41 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
17:16	R/W	0x0	IRQ40_PRIO. IRQ 40 Priority. Set priority level for IRQ 40 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
15:14	R/W	0x0	IRQ39_PRIO. IRQ 39 Priority. Set priority level for IRQ 39 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
13:12	R/W	0x0	IRQ38_PRIO. IRQ 38 Priority. Set priority level for IRQ 38 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

11:10	R/W	0x0	IRQ37_PRIO. IRQ 37 Priority. Set priority level for IRQ 37 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
9:8	R/W	0x0	IRQ36_PRIO. IRQ 36 Priority. Set priority level for 36 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
7:6	R/W	0x0	IRQ35_PRIO. IRQ 35 Priority. Set priority level for IRQ 35 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
5:4	R/W	0x0	IRQ34_PRIO. IRQ 34 Priority. Set priority level for IRQ 34 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
3:2	R/W	0x0	IRQ33_PRIO. IRQ 33 Priority. Set priority level for IRQ 33 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
1:0	R/W	0x0	IRQ32_PRIO. IRQ 32 Priority. Set priority level for IRQ 32 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority

3.5.6.17. Interrupt Source Priority Register 3

Offset:0x6C	Register Name: INTC_PRIO_REG3

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	R/W	Default/Hex	Description
31:30	R/W	0x0	IRQ63_PRIO. IRQ 63 Priority. Set priority level for IRQ 63 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
29:28	R/W	0x0	IRQ62_PRIO. IRQ 62 Priority. Set priority level for IRQ 62 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
27:26	R/W	0x0	IRQ61_PRIO. IRQ 61 Priority. Set priority level for IRQ 61 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
25:24	R/W	0x0	IRQ60_PRIO. IRQ 60 Priority. Set priority level for IRQ 60 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
23:22	R/W	0x0	IRQ59_PRIO. IRQ 59 Priority. Set priority level for IRQ 59 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
21:20	R/W	0x0	IRQ58_PRIO. IRQ 58 Priority. Set priority level for IRQ 58 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
19:18	R/W	0x0	IRQ57_PRIO. IRQ 57 Priority.

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Set priority level for IRQ 57 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
17:16	R/W	0x0	IRQ56_PRIO. IRQ 56 Priority. Set priority level for IRQ 56 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
15:14	R/W	0x0	IRQ55_PRIO. IRQ 55 Priority. Set priority level for IRQ 55 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
13:12	R/W	0x0	IRQ54_PRIO. IRQ 54 Priority. Set priority level for IRQ 54 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
11:10	R/W	0x0	IRQ53_PRIO. IRQ 53 Priority. Set priority level for IRQ 53 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
9:8	R/W	0x0	IRQ52_PRIO. IRQ 52 Priority. Set priority level for IRQ 52 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
7:6	R/W	0x0	IRQ51_PRIO. IRQ 51 Priority. Set priority level for IRQ 51 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
5:4	R/W	0x0	IRQ50_PRIO. IRQ 50 Priority. Set priority level for IRQ 50 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
3:2	R/W	0x0	IRQ49_PRIO. IRQ 49 Priority. Set priority level for IRQ 49 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
1:0	R/W	0x0	IRQ48_PRIO. IRQ 48 Priority. Set priority level for IRQ 48 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.6. DMA

3.6.1. Overview

There are two kinds of system DMA in the Soc. One is Normal DMA (NDMA) with 4 channels; the other is Dedicated DMA (DDMA) with 4 channels.

Normal DMA master interface support single and INCR4 operation (may be early terminated), and will treat any response from AHB bus as OK response. Dedicated DMA master interface supports Single and INCR4 operation (may be early terminated), and will treat any response from DMA bus as OK response.

3.6.2. Feature

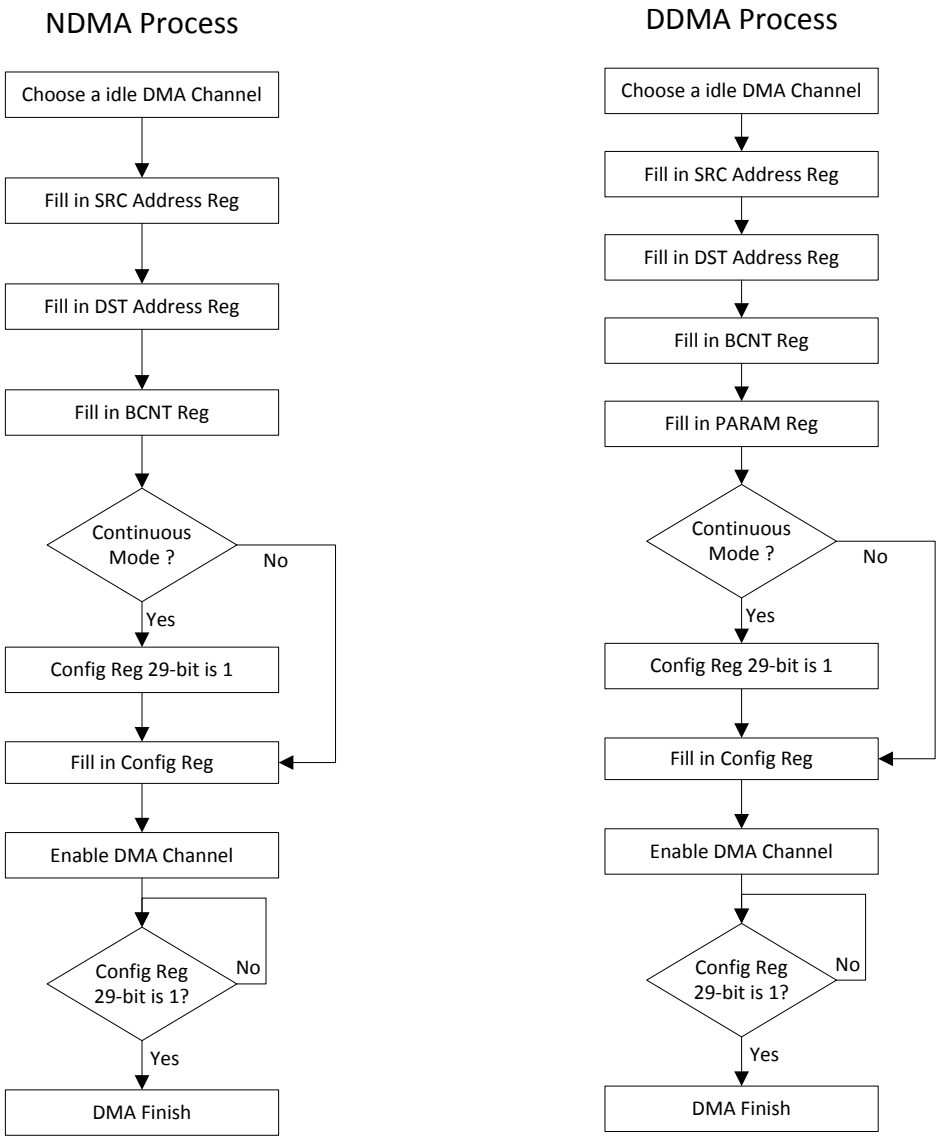
- 4 NDMA channels and 4DDMA channels for transaction
- Support multiple transfer DRQ types
- Support hardware continuous transfer mode
- Support two kinds of interrupt

3.6.3. Functionalities Description

- Transfer data from memory to memory
- Transfer data from memory to peripheral
- Transfer data from peripheral to memory
- Transfer data from peripheral to peripheral

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.6.4. Block diagram



3.6.5. Operation Principle

3.6.5.1. Address aligned and unaligned

DMA can support 8-bit/16-bit/32-bit data width. The data width of Source and Destination can be different, but the address should be aligned.

NDMA: SRC and DST are both work in INC mode (increase mode).

The address aligned includes source address word-aligned and destination address word-aligned.

DDMA: SRC and DST are both work in linear mode.

DMA Channel 0~3 are the Normal DMA，Channel 4~7 are the Dedicated DMA. NDMA and DDMA have some different working modes. Only some modes of the DDMA support the address not aligned:

	Mode	Address aligned
NDMA	Increase	Should
	IO	Should
DDMA	Linear	Not should

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

	IO	Should

Although the increase mode of NDMA should be address aligned, but its byte counter should not be multiple.
The DDMA forth channel has 8x64-bit FIFO; the other DDMA channels have 8x32-bit FIFO.

3.6.5.2. Clock gating and reset

By default the DMA clock gating is mask. When it is necessary to use DMA, its clock gating should be open in *AHB1 Module Clock Gating Register* and then de-assert the software reset in *AHB1 Module Software Reset Register* on CCU module. If it is no need to use DMA, both the gating bit and software reset bit should be wrote 0.

3.6.6. DMA Register List

Module Name	Base Address
DMA	0x01C02000

Register Name	Offset	Description
DMA_INT_CTRL_REG	0x00	DMA Interrupt Control Register
DMA_INT_STA_REG	0x04	DMA Interrupt Status Register
DMA_PTY_CFG_REG	0x08	DMA Priority Configure Register
NDMA_CFG_REG	0x100+n*0x20+0x0	Normal DMA Configure Register n (n=0~3)
NDMA_SRC_ADR_REG	0x100+n*0x20+0x4	Normal DMA Source Address Register n (n=0~3)
NDMA_DES_ADR_REG	0x100+n*0x20+0x8	Normal DMA Destination Address Register n (n=0~3)
NDMA_BYTE_CNT_REG	0x100+n*0x20+0xC	Normal DMA Byte Counter Register n (n=0~3)
DDMA_CFG_REG	0x300+n*0x20+0x0	Dedicated DMA Configure Register n (n=0~3)
DDMA_SRC_ADR_REG	0x300+n*0x20+0x4	Dedicated DMA Source Address Register n (n=0~3)
DDMA_DES_ADR_REG	0x300+n*0x20+0x8	Dedicated DMA Destination Address Register n (n=0~3)
DDMA_BYTE_CNT_REG	0x300+n*0x20+0xC	Dedicated DMA Byte Counter Register n (n=0~3)
DDMA_PAR_REG	0x300+n*0x20+0x18	Dedicated DMA Parameter Register n (n=0~3)
DDMA_GEN_DATA	0x300+n*0x20+0x1c	Dedicated DMA General DATA Register 3

3.6.7. DMA Register Description

3.6.7.1. DMA Interrupt Control Register

Offset: 0x00			Register Name: DMA_INT_CTRL_REG
Bit	R/W	Default/Hex	Description
31:24	/	/	Reserved.
[16 + 2*n + 1]	R/W	0x0	Dedicated DMA n Full Transfer Interrupt Enable (n=0~3) 0: Disable 1: Enable
[16 + 2*n + 0]	R/W	0x0	Dedicated DMA n Half Transfer Interrupt Enable (n=0~3) 0: Disable 1: Enable

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

15:8	/	/	Reserved.
[2*n + 1]	R/W	0x0	Normal DMA n Full Transfer Interrupt Enable (n=0~3) 0: Disable 1: Enable
[2*n + 0]	R/W	0x0	Normal DMA n Half Transfer Interrupt Enable (n=0~3) 0: Disable 1: Enable

3.6.7.2. DMA Interrupt Status Register

Offset: 0x04			Register Name: DMA_INT_STA_REG
Bit	R/W	Default/Hex	Description
31:24	/	/	Reserved.
[16+2*n+1]	R/W	0x0	Dedicated DMA n Full Transfer Interrupt Pending (n=0~3) 0: No interrupt 1: Interrupt pending Set 1 to clear it.
[16+2*n+0]	R/W	0x0	Dedicated DMA n Half Transfer Interrupt Pending (n=0~3) 0: No interrupt 1: Interrupt pending Set 1 to clear it.
15:8	/	/	Reserved.
[2*n+1]	R/W	0x0	Normal DMA n Full Transfer Interrupt Pending (n=0~3) 0: No interrupt 1: Interrupt pending Set 1 to clear it.
[2*n+0]	R/W	0x0	Normal DMA n Half Transfer Interrupt Pending (n=0~3) 0: No interrupt 1: Interrupt pending Set 1 to clear it.

3.6.7.3. DMA Priority Configure Register

Offset: 0x08			Register Name: DMA_PTY_CFG_REG
Bit	R/W	Default/Hex	Description
31:17	/	/	Reserved.
16	R/W	0x0	DMA Auto Clock Gating bit 0: DMA auto clock gating enable 1: DMA auto clock gating disable If DMA works in continuous mode, this bit should be set to 1.
15:10	/	/	Reserved.
9:7	R/W	0x3	NDMA Priority Counter. If NDMA grant the AHB Bus, it can continuously access AHB with burst or single operation for N+1 times without interrupt by other AHB masters.
6:4	R/W	0x1	AC320 Priority Counter. If AC320 grant the AHB Bus, it can continuously access AHB with burst or single operation for N+1 times without interrupt by other AHB masters.

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

3:2	/	/	Reserved.
1:0	R/W	0x0	NDMA/CPU Priority Configure Bit 00: CPU>NDMA 01: NDMA>CPU 10: Reserved 11: Reserved

Note:

1) For DDMA, the priority order is: 0>1>2>3;
2) For NDMA, the priority order is: 0>1>2>3;
3) The number is DMA index.

3.6.7.4. Normal DMA Configure Register

Offset: 0x100+n*0x20 + 0x0 (N=0~3)			Register Name: NDMA_CFG_REG
Bit	R/W	Default/Hex	Description
31	R/W	0x0	DMA Loading. If set to 1, DMA will start and load the DMA registers to the shadow registers. The bit will hold on until the DMA finished. It will be cleared automatically. Set 0 to the bit will reset the corresponding DMA channel.
30	RO	0x0	DMA Busy Status. 0: DMA idle, 1: DMA busy.
29	R/W	0x0	DMA Continuous Mode Enable. 0: Disable, 1: Enable.
28:26	R/W	0x0	DMA Wait State. 0: 1 1: 2 2: 4 3: 8 4: 16 5: 32 6: 64 7: 128
25:24	R/W	0x0	Normal DMA Destination Data Width. 00: 8-bit 01: 16-bit 10: 32-bit 11: /
23	R/W	0x0	DMA Destination Burst Length. 0: 1 1: 4
22:21	R/W	0x0	Normal DMA Destination Address Type. 00: Linear Mode 01: IO Mode 1x: /
20:16	R/W	0x0	Normal DMA Destination DRQ Type.

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0x00 : / 0x01 : OWA Tx 0x02 : / 0x03 : / 0x04 : SPI0 Tx 0x05 : SPI1 Tx 0x06 : / 0x07 : / 0x08 : UART0 Tx 0x09 : UART1 Tx 0x0A : UART2 Tx 0x0B : / 0x0C : Audio Codec DAC (headphone) 0x0D : / 0x0E : Daudio 0x0F : / 0x10 : SRAM Memory 0x11 : SDRAM Memory 0x12 : / 0x13 : / 0x14 : USB 0x15 : USB-EP1 0x16 : USB-EP2 0x17 : USB-EP3 Others : /
15	R/W	0x0	Normal DMA remain byte counter read enable If this bit is set, the remain byte counter can read out from NDMA_BYTE_CNT_REG register
14:10	/	/	Reserved.
9:8	R/W	0x0	Normal DMA Source Data Width. 00: 8-bit 01: 16-bit 10: 32-bit 11: /
7	R/W	0x0	DMA Source Burst Length. 0: 1 1: 4
6:5	R/W	0x0	Normal DMA Source Address Type. 00: Linear Mode 01: IO Mode 1x: /
4:0	R/W	0x0	Normal DMA Source DRQ Type. 0x00 : IR Rx 0x01 : / 0x02 : /

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0x03 : / 0x04 : SPI0 Rx 0x05 : SPI1 Rx 0x06 : / 0x07 : / 0x08 : UART0 Rx 0x09 : UART1 Rx 0x0A : UART2 Rx 0x0B : / 0x0C : Audio Codec 0x0D : TP ADC 0x0E : Daudio 0x0F : / 0x10 : SRAM memory 0x11 : SDRAM memory 0x12 : / 0x13 : / 0x14 : USB 0x15 : USB-EP1 0x16 : USB-EP2 0x17 : USB-EP3 Others : /

3.6.7.5. Normal DMA Source Address Register

Offset: 0x100+n*0x20+0x4 (N=0~3)			Register Name: NDMA_SRC_ADR_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0x0	Normal DMA Source Address.

3.6.7.6. Normal DMA Destination Address Register

Offset: 0x100+n*0x20+0x8 (N=0~3)			Register Name: NDMA_DES_ADR_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0x0	Normal DMA Destination Address.

3.6.7.7. Normal DMA Byte Counter Register

Offset: 0x100+n*0x20+0xC (N=0~3)			Register Name: NDMA_BYTE_CNT_REG
Bit	R/W	Default/Hex	Description
31:18	/	/	Reserved.
17:0	R/W	0x0	Normal DMA Byte Counter. If NDMA_CFG_REGn bit 15 is set, the remain byte counter can read out from this register

Note:

1) If ByteCounter=0, DMA will transfer no byte. The maximum value is 128k.

3.6.7.8. Dedicated DMA Configure Register

Offset: 0x300+n*0x20+0x0 (N=0~3)	Register Name: DDMA_CFG_REG

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	R/W	Default/Hex	Description
31	R/W	0x0	DMA Loading. If set to 1, DMA will start and load the DMA registers to the shadow registers. The bit will hold on until the DMA finished. It will be cleared automatically. Set 0 to the bit will stop the corresponding DMA channel and reset its state machine.
30	RO	0x0	DMA Busy Status. 0: DMA idle 1: DMA busy
29	R/W	0x0	DMA Continuous Mode Enable. 0: Disable 1: Enable
28	R/W	0x0	DMA Memory set mode enable 0: Disable 1: DMA will move data from Dedicate DMA General Data register to Destination device. This bit is only valid for DDMA3(n = 3) ,and if this bit is set, the configuration for the source（bit10-0） will be invalid.
27	/	/	/.
26	R/W	0x0	DMA Destination INCR8 enable 0: Single or INCR4 (determine by bit 23) 1: INCR8 This bit is only valid for DDMA3(n = 3)
25:24	R/W	0x0	DMA Destination Data Width. 00: 8-bit 01: 16-bit 10: 32-bit 11: /
23	R/W	0x0	DMA Destination Burst Length. 0: 1 1: 4
22:21	R/W	0x0	DMA Destination Address Mode 00: Linear Mode 01: IO Mode 1x: /
20:16	R/W	0x0	Dedicated DMA Destination DRQ Type 0x0: SRAM 0x1: SDRAM memory 0x2: LCD Controller (LCDC) 0x3: / 0x4: USB 0x5: / 0x6: / 0x7: /

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0x8: / 0x9: AHB Memory Others: /
15	R/W	0x0	DMA remain byte counter read enable If this bit is set, the remain byte counter can read out from *DDMA_BYTE_CNT_REG* register
14:11	/	/	Reserved.
10	R/W	0x0	DMA Source INCR8 enable 0: Single or INCR4 (determine by bit 7), 1: INCR8. This bit is only valid for DDMA3(n = 3)
9:8	R/W	0x0	DMA Source Data Width. 00: 8-bit 01: 16-bit 10: 32-bit 11: /
7	R/W	0x0	DMA Source Burst Length. 0: 1 1: 4
6:5	R/W	0x0	DMA Source Address Mode 00: Linear Mode 01: IO Mode 1x: /
4:0	R/W	0x0	Dedicated DMA Source DRQ Type 0x0: SRAM 0x1: SDRAM memory 0x2: / 0x3: / 0x4: USB 0x5: / 0x6: / 0x7: / 0x8: / 0x9: AHB Memory Others: /

3.6.7.9. Dedicated DMA Source Address Register

Offset: 0x300+n*0x20+0x4 (N=0~3)			Register Name: DDMA_SRC_ADR_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0x0	Dedicated DMA Source Start Address.

3.6.7.10. Dedicated DMA Destination Address Register

Offset: 0x300+n*0x20+0x8 (N=0~3)			Register Name: DDMA_DES_ADR_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0x0	Dedicated DMA Destination Start Address.

Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.6.7.11. Dedicated DMA Byte Counter Register

Offset: 0x300+n*0x20+0x0C (N=0~3)			Register Name: DDMA_BYTE_CNT_REG
Bit	R/W	Default/Hex	Description
31:25	/	/	Reserved.
24:0	R/W	0x0	Dedicated DMA Byte Counter. If DDMA_CFG_REGn bit 15 is set, the remain byte counter can read out from this register

Note:

1) If Byte Counter=0, DMA will transfer no byte. The maximum value is 0x1000000.

3.6.7.12. Dedicated DMA Parameter Register

Offset: 0x300+n*0x20+0x18 (N=0~3)			Register Name: DDMA_PAR_REG
Bit	R/W	Default/Hex	Description
31:24	R/W	0x0	Destination block counter.
23:16	R/W	0x0	Destination Comity Counter
15:8	R/W	0x0	Source block counter.
7:0	R/W	0x0	Source Comity Counter

Note:

1) If the counter=N, the value is N+1.

3.6.7.13. Dedicated DMA General Data Register

Offset: 0x300+3*0x20+0x1C			Register Name: DDMA_GEN_DATA
Bit	R/W	Default/Hex	Description
31:0	R/W	0x0	Dedicated DMA general data This register is only valid for DDMA3(n = 3)

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.7. Port Controller

3.7.1. Overview

The chip has 6 ports for multi-functional input/out pins. They are shown below:

- Port A(PA): 4 input/output port
- Port B(PB): 4 input/output port
- Port C(PC): 4 input/output port
- Port D(PD): 22 input/output port
- Port E(PE) : 13 input/output port
- Port F(PF) : 6 input/output port

For various system configurations, these ports can be easily configured by software. All these ports can be configured as GPIO if multiplexed functions are not used. The total 4 group external PIO interrupt sources are supported and interrupt mode can be configured by software.

3.7.2. Port Register List

Module Name	Base Address
PIO	0x01C20800

Register Name	Offset	Description
Pn_CFG0	n*0x24+0x00	Port n Configure Register 0 (n=0~5)
Pn_CFG1	n*0x24+0x04	Port n Configure Register 1 (n=0~5)
Pn_CFG2	n*0x24+0x08	Port n Configure Register 2 (n=0~5)
Pn_CFG3	n*0x24+0x0C	Port n Configure Register 3 (n=0~5)
Pn_DATA	n*0x24+0x10	Port n Data Register (n=0~5)
Pn_DRV0	n*0x24+0x14	Port n Multi-Driving Register 0 (n=0~5)
Pn_DRV1	n*0x24+0x18	Port n Multi-Driving Register 1 (n=0~5)
Pn_PUL0	n*0x24+0x1C	Port n Pull Register 0 (n=0~5)
Pn_PUL1	n*0x24+0x20	Port n Pull Register 1 (n=0~5)
PIO_INT_CFG0	0x200+n*0x20+0x0	PIO Interrupt Configure Register 0 (n=0~2)
PIO_INT_CFG1	0x200+n*0x20+0x4	PIO Interrupt Configure Register 1 (n=0~2)
PIO_INT_CFG2	0x200+n*0x20+0x8	PIO Interrupt Configure Register 2 (n=0~2)
PIO_INT_CFG3	0x200+n*0x20+0xC	PIO Interrupt Configure Register 3 (n=0~2)
PIO_INT_CTRL	0x200+n*0x20+0x10	PIO Interrupt Control Register (n=0~2)
PIO_INT_STA	0x200+n*0x20+0x14	PIO Interrupt Status Register (n=0~2)
PIO_INT_DEB	0x200+n*0x20+0x18	PIO Interrupt Debounce Register (n=0~2)
SDR_PAD_DRV	0x2C0	SDRAM Pad Multi-Driving Register
SDR_PAD_PUL	0x2C4	SDRAM Pad Pull Register

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.7.3. Port Register Description

3.7.3.1. PA Configure Register 0

Offset: 0x00			Register Name: PA_CFG0	
Bit	R/W	Default/Hex	Description	
31:15	/	/	Reserved	
14:12	R/W	7	PA3 Select 000: Input 010: TP_Y2 100: DA_OUT 110: SPI1_MISO	001: Output 011: IR_RX 101: UART1_TX 111: Disabled
11	/	/	Reserved	
10:8	R/W	7	PA2 Select 000: Input 010: TP_Y1 100: DA_IN 110: SPI1_CLK	001: Output 011: PWM0 101: UART1_RX 111: Disabled
7	/	/	Reserved	
6:4	R/W	7	PA1 Select 000: Input 010: TP_X2 100: DA_LRCK 110: SPI1_MOSI	001: Output 011: Reserved 101: UART1_CTS 111: Disabled
3	/	/	Reserved	
2:0	R/W	7	PA0 Select 000: Input 010: TP_X1 100: DA_BCLK 110: SPI1_CS	001: Output 011: Reserved 101: UART1_RTS 111: Disabled

3.7.3.2. PA Configure Register 1

Offset: 0x04			Register Name: PA_CFG1
Bit	R/W	Default/Hex	Description
31:0	/	/	Reserved

3.7.3.3. PA Configure Register 2

Offset: 0x08			Register Name: PA_CFG2
Bit	R/W	Default/Hex	Description
31:0	/	/	Reserved

3.7.3.4. PA Configure Register 3

Offset: 0x0C			Register Name: PA_CFG3
Bit	R/W	Default/Hex	Description

Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

31:0	/	/	Reserved

3.7.3.5. PA Data Register

Offset: 0x10			Register Name: PA_DAT
Bit	R/W	Default/Hex	Description
31:4	/	/	Reserved
3:0	R/W	0	If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

3.7.3.6. PA Multi-Driving Register 0

Offset: 0x14			Register Name: PA_DRV0
Bit	R/W	Default/Hex	Description
31:0	/	/	Reserved

3.7.3.7. PA Multi-Driving Register 1

Offset: 0x18			Register Name: PA_DRV1
Bit	R/W	Default/Hex	Description
31:0	/	/	Reserved

3.7.3.8. PA Pull Register 0

Offset: 0x1C			Register Name: PA_PULL0
Bit	R/W	Default/Hex	Description
31:0	/	/	Reserved

3.7.3.9. PA Pull Register 1

Offset: 0x20			Register Name: PA_PULL1
Bit	R/W	Default/Hex	Description
31:0	/	/	Reserved

3.7.3.10. PB Configure Register 0

Offset: 0x24			Register Name: PB_CFG0
Bit	R/W	Default/Hex	Description
31:15	/	/	Reserved
14:12	R/W	7	PB3 Select 000: Input 001: Output 010: DDR_REF_D 011: IR_RX 100: Reserved 101: Reserved 110: Reserved 111: Disabled
11	/	/	Reserved
10:8	R/W	2	Reserved
7	/	/	Reserved

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

6:4	R/W	2	Reserved
3	/	/	Reserved
2:0	R/W	2	Reserved

3.7.3.11. PB Configure Register 1

Offset: 0x28			Register Name: PB_CFG1
Bit	R/W	Default/Hex	Description
31:0	/	/	Reserved

3.7.3.12. PB Configure Register 2

Offset: 0x2C			Register Name: PB_CFG2
Bit	R/W	Default/Hex	Description
31:0	/	/	Reserved

3.7.3.13. PB Configure Register 3

Offset: 0x30			Register Name: PB_CFG3
Bit	R/W	Default/Hex	Description
31:0	/	0x7	Reserved

3.7.3.14. PB Data Register

Offset: 0x34			Register Name: PB_DAT
Bit	R/W	Default/Hex	Description
31:4	/	/	Reserved
3:0	R/W	0	If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

3.7.3.15. PB Multi-Driving Register 0

Offset: 0x38			Register Name: PB_DRV0
Bit	R/W	Default/Hex	Description
31:8	/	/	Reserved
[2i+1:2i] (i=0~3)	R/W	1	PB[n] Multi-Driving Select (n = 0~3) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

3.7.3.16. PB Multi-Driving Register 1

Offset: 0x3C			Register Name: PB_DRV1
Bit	R/W	Default/Hex	Description
31:0	/	/	Reserved

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.7.3.17. PB Pull Register 0

Offset: 0x40			Register Name: PB_PULL0
Bit	R/W	Default/Hex	Description
31:8	/	/	Reserved
[2i+1:2i] (i=0~3)	R/W	0x0	PB[n] Pull-up/down Select (n = 0~3) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

3.7.3.18. PB Pull Register 1

Offset: 0x44			Register Name: PB_PULL1
Bit	R/W	Default/Hex	Description
31:0	/	/	Reserved

3.7.3.19. PC Configure Register 0

Offset: 0x48			Register Name: PC_CFG0
Bit	R/W	Default/Hex	Description
31:15	/	/	Reserved
14:12	R/W	7	PC3 Select 000: Input 001: Output 010: SPI0_MOSI 011: UART0_TX 100: Reserved 101: Reserved 110: Reserved 111: Disabled
11	/	/	Reserved
10:8	R/W	7	PC2 Select 000: Input 001: Output 010: SPI0_MISO 011: SDC1_D0 100: Reserved 101: Reserved 110: Reserved 111: Disabled
7	/	/	Reserved
6:4	R/W	7	PC1 Select 000: Input 001: Output 010: SPI0_CS 011: SDC1_CMD 100: Reserved 101: Reserved 110: Reserved 111: Disabled
3	/	/	Reserved
2:0	R/W	7	PC0 Select 000: Reserved 001: Output 010: SPI0_CLK 011: SDC1_CLK 100: Reserved 101: Reserved 110: Reserved 111: Disabled

3.7.3.20. PC Configure Register 1

Offset: 0x4C			Register Name: PC_CFG1
Bit	R/W	Default/Hex	Description
31:0	/	/	Reserved

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.7.3.21. PC Configure Register 2

Offset: 0x50			Register Name: PC_CFG2
Bit	R/W	Default/Hex	Description
31:0	/	/	Reserved

3.7.3.22. PC Configure Register 3

Offset: 0x54			Register Name: PC_CFG3
Bit	R/W	Default/Hex	Description
31:0	/	/	Reserved

3.7.3.23. PC Data Register

Offset: 0x58			Register Name: PC_DATA
Bit	R/W	Default/Hex	Description
31:4	/	/	Reserved
3:0	R/W	0	If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

3.7.3.24. PC Multi-Driving Register 0

Offset: 0x5C			Register Name: PC_DRV0
Bit	R/W	Default/Hex	Description
31:8	/	/	Reserved
[2i+1:2i] (i=0~3)	R/W	1	PC[n] Multi-Driving Select (n = 0~3) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

3.7.3.25. PC Multi-Driving Register 1

Offset: 0x60			Register Name: PC_DRV1
Bit	R/W	Default/Hex	Description
31:0	/	/	Reserved

3.7.3.26. PC Pull Register 0

Offset: 0x64			Register Name: PC_PULL0
Bit	R/W	Default/Hex	Description
[2i+1:2i] (i=0~3)	R/W	0x0(PC1: 1)	PC[n] Pull-up/down Select (n = 0~3) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

3.7.3.27. PC Pull Register 1

Offset: 0x68			Register Name: PC_PULL1
Bit	R/W	Default/Hex	Description
31:0	/	/	Reserved

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.7.3.28. PD Configure Register 0

Offset: 0x6C			Register Name: PD_CFG0	
Bit	R/W	Default/Hex	Description	
31	/	/	Reserved	
30:28	R/W	7	PD7 Select 000: Input 010: LCD_D11 100: Reserved 110: EINTD7	 001: Output 011: DA_MCLK 101: Reserved 111: Disabled
27	/	/	Reserved	
26:24	R/W	7	PD6 Select 000: Input 010: LCD_D10 100: Reserved 110: EINTD6	 001: Output 011: TWI1_SDA 101: Reserved 111: Disabled
23	/	/	Reserved	
22:20	R/W	7	PD5 Select 000: Input 010: LCD_D7 100: Reserved 110: EINTD5	 001: Output 011: TWI1_SCK 101: Reserved 111: Disabled
19	/	/	Reserved	
18:16	R/W	7	PD4 Select 000: Input 010: LCD_D6 100: Reserved 110: EINTD4	 001: Output 011: UART1_TX 101: Reserved 111: Disabled
15	/	/	Reserved	
14:12	R/W	7	PD3 Select 000: Input 010: LCD_D5 100: Reserved 110: EINTD3	 001: Output 011: UART1_RX 101: Reserved 111: Disabled
11	/	/	Reserved	
10:8	R/W	7	PD2 Select 000: Input 010: LCD_D4 100: Reserved 110: EINTD2	 001: Output 011: UART1_CTS 101: Reserved 111: Disabled
7	/	/	Reserved	
6:4	R/W	7	PD1 Select 000: Input 010: LCD_D3 100: Reserved 110: EINTD1	 001: Output 011: UART1_RTS 101: Reserved 111: Disabled

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

3	/	/	Reserved	
2:0	R/W	7	PD0 Select 000: Input 010: LCD_D2 100: RSB_SDA 110: EINTD0	001: Output 011: TWI0_SDA 101: Reserved 111: Disabled

3.7.3.29. PD Configure Register 1

Offset: 0x70			Register Name: PD_CFG1	
Bit	R/W	Default/Hex	Description	
31	/	/	Reserved	
30:28	R/W	7	PD15 Select 000: Input 010: LCD_D21 100: TWI2_SCK 110: EINTD15	001: Output 011: UART2_RTS 101: Reserved 111: Disabled
27	/	/	Reserved	
26:24	R/W	7	PD14 Select 000: Input 010: LCD_D20 100: Reserved 110: EINTD14	001: Output 011: UART2_RX 101: Reserved 111: Disabled
23	/	/	Reserved	
22:20	R/W	7	PD13 Select 000: Input 010: LCD_D19 100: Reserved 110: EINTD13	001: Output 011: UART2_TX 101: Reserved 111: Disabled
19	/	/	Reserved	
18:16	R/W	7	PD12 Select 000: Input 010: LCD_D18 100: RSB_SCK 110: EINTD12	001: Output 011: TWI0_SCK 101: Reserved 111: Disabled
15	/	/	Reserved	
14:12	R/W	7	PD11 Select 000: Input 010: LCD_D15 100: Reserved 110: EINTD11	001: Output 011: DA_OUT 101: Reserved 111: Disabled
11	/	/	Reserved	
10:8	R/W	7	PD10 Select 000: Input 010: LCD_D14 100: Reserved	001: Output 011: DA_IN 101: Reserved

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			110: EINTD10	111: Disabled
7	/	/	Reserved	
6:4	R/W	7	PD9 Select 000: Input 010: LCD_D13 100: Reserved 110: EINTD9	001: Output 011: DA_LRCK 101: Reserved 111: Disabled
3	/	/	Reserved	
2:0	R/W	7	PD8 Select 000: Input 010: LCD_D12 100: Reserved 110: EINTD8	001: Output 011: DA_BCLK 101: Reserved 111: Disabled

3.7.3.30. PD Configure Register 2

Offset: 0x74			Register Name: PD_CFG2	
Bit	R/W	Default/Hex	Description	
31:23	/	/	Reserved	
22:20	R/W	7	PD21 Select 000: Input 010: LCD_VSYNC 100: Reserved 110: EINTD21	001: Output 011: SPI0_MISO 101: Reserved 111: Disabled
19	/	/	Reserved	
18:16	R/W	7	PD20 Select 000: Input 010: LCD_HSYNC 100: Reserved 110: EINTD20	001: Output 011: SPI0_CLK 101: Reserved 111: Disabled
15	/	/	Reserved	
14:12	R/W	7	PD19 Select 000: Input 010: LCD_DE 100: Reserved 110: EINTD19	001: Output 011: SPI0_MOSI 101: Reserved 111: Disabled
11	/	/	Reserved	
10:8	R/W	7	PD18 Select 000: Input 010: LCD_CLK 100: Reserved 110: EINTD18	001: Output 011: SPI0_CS 101: Reserved 111: Disabled
7	/	/	Reserved	
6:4	R/W	7	PD17 Select 000: Input 010: LCD_D23	001: Output 011: OWA_OUT

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			100: Reserved 110: EINTD17	101: Reserved 111: Disabled
3	/	/	Reserved	
2:0	R/W	7	PD16 Select 000: Input 010: LCD_D22 100: TWI2_SDA 110: EINTD16	001: Output 011: UART2_CTS 101: Reserved 111: Disabled

3.7.3.31. PD Configure Register 3

Offset: 0x78			Register Name: PD_CFG3
Bit	R/W	Default/Hex	Description
31:0	/	/	Reserved

3.7.3.32. PD Data Register

Offset: 0x7C			Register Name: PD_DAT
Bit	R/W	Default/Hex	Description
31:22	/	/	Reserved
21:0	R/W	0	If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

3.7.3.33. PD Multi-Driving Register 0

Offset: 0x80			Register Name: PD_DRV0
Bit	R/W	Default/Hex	Description
[2i+1:2i] (i=0~15)	R/W	1	PD[n] Multi-Driving Select (n = 0~15) 00: Level 0 10: Level 2	 01: Level 1 11: Level 3

3.7.3.34. PD Multi-Driving Register 1

Offset: 0x84			Register Name: PD_DRV1
Bit	R/W	Default/Hex	Description
31:12	/	/	Reserved
[2i+1:2i] (i=0~5)	R/W	1	PD[n] Multi-Driving Select (n = 16~21) 00: Level 0 10: Level 2	 01: Level 1 11: Level 3

3.7.3.35. PD Pull Register 0

Offset: 0x88			Register Name: PD_PULL0
Bit	R/W	Default/Hex	Description
[2i+1:2i] (i=0~15)	R/W	0x0	PD[n] Pull-up/down Select (n = 0~15) 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved

Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.7.3.36. PD Pull Register 1

Offset: 0x8C			Register Name: PD_PULL1
Bit	R/W	Default/Hex	Description
31:12	/	/	Reserved
[2i+1:2i] (i=0~5)	R/W	0x0	PD[n] Pull-up/down Select (n = 16~21) 00: Pull-up/down disable 01: Pull-up enable 10: Pull-down 11: Reserved

3.7.3.37. PE Configure Register 0

Offset: 0x90			Register Name: PE_CFG0
Bit	R/W	Default/Hex	Description
31	/	/	Reserved
30:28	R/W	7	PE7 Select 000: Input 001: Output 010: CSI_D4 011: UART2_TX 100: SPI1_CS 101: Reserved 110: EINTE7 111: Disabled
27	/	/	Reserved
26:24	R/W	7	PE6 Select 000: Input 001: Output 010:CSI_D3 011: PWM1 100: DA_OUT 101: OWA_OUT 110: EINTE6 111: Disabled
23	/	/	Reserved
22:20	R/W	7	PE5 Select 000: Input 001: Output 010: CSI_D2 011: LCD_D17 100: DA_IN 101: Reserved 110: EINTE5 111: Disabled
19	/	/	Reserved
18:16	R/W	7	PE4 Select 000: Input 001: Output 010: CSI_D1 011: LCD_D16 100: DA_LRCK 101: RSB_SDA 110: EINTE4 111: Disabled
15	/	/	Reserved
14:12	R/W	7	PE3 Select 000: Input 001: Output 010: CSI_D0 011: LCD_D9 100: DA_BCLK 101: RSB_SCK 110: EINTE3 111: Disabled
11	/	/	Reserved
10:8	R/W	7	PE2 Select 000: Input 001: Output 010: CSI_PCLK 011: LCD_D8

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			100: CLK_OUT	101: Reserved
			110: EINTE2	111: Disabled
7	/	/	Reserved	
			PE1 Select	
			000: Input	001: Output
			010: CSI_VSYNC	011: LCD_D1
			100: TWI2_SDA	101: UART0_TX
6:4	R/W	7	110: EINTE1	111: Disabled
3	/	/	Reserved	
			PE0 Select	
			000: Input	001: Output
			010: CSI_HSYNC	011: LCD_D0
			100: TWI2_SCK	101: UART0_RX
2:0	R/W	7	110: EINTE0	111: Disabled

3.7.3.38. PE Configure Register 1

Offset: 0x94			Register Name: PE_CFG1	
Bit	R/W	Default/Hex	Description	
31:19	/	/	Reserved	
			PE12 Select	
			000: Input	001: Output
			010: DA_MCLK	011: TWI0_SDA
			100: PWM0	101: Reserved
18:16	R/W	7	110: EINTE12	111: Disabled
15	/	/	Reserved	
			PE11 Select	
			000: Input	001: Output
			010: CLK_OUT	011: TWI0_SCK
			100: IR_RX	101: Reserved
14:12	R/W	7	110: EINTE11	111: Disabled
11	/	/	Reserved	
			PE10 Select	
			000: Input	001: Output
			010: CSI_D7	011: UART2_CTS
			100: SPI1_MISO	101: Reserved
10:8	R/W	7	110: EINTE10	111: Disabled
7	/	/	Reserved	
			PE9 Select	
			000: Input	001: Output
			010: CSI_D6	011: UART2_RTS
			100: SPI1_CLK	101: Reserved
6:4	R/W	7	110: EINTE9	111: Disabled
3	/	/	Reserved	
			PE8 Select	
2:0	R/W	7	000: Input	001: Output

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			010: CSI_D5 100: SPI1_MOSI 110: EINTE8	011: UART2_RX 101: Reserved 111: Disabled

3.7.3.39. PE Configure Register 2

Offset: 0x98			Register Name: PE_CFG2
Bit	R/W	Default/Hex	Description
31:0	/	/	Reserved

3.7.3.40. PE Configure Register 3

Offset: 0x9C			Register Name: PE_CFG3
Bit	R/W	Default/Hex	Description
31:0	/	/	Reserved

3.7.3.41. PE Data Register

Offset: 0xA0			Register Name: PE_DAT
Bit	R/W	Default/Hex	Description
31:13	/	/	Reserved
12:0	R/W	0	If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

3.7.3.42. PE Multi-Driving Register 0

Offset: 0xA4			Register Name: PE_DRV0
Bit	R/W	Default/Hex	Description
31:26	/	/	Reserved
[2i+1:2i] (i=0~12)	R/W	1	PD[n] Multi-Driving Select (n = 0~12) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

3.7.3.43. PE Multi-Driving Register 1

Offset: 0xA8			Register Name: PE_DRV1
Bit	R/W	Default/Hex	Description
31:0	/	/	Reserved

3.7.3.44. PE Pull Register 0

Offset: 0xAC			Register Name: PE_PULL0
Bit	R/W	Default/Hex	Description
31:26	/	/	Reserved
[2i+1:2i] (i=0~12)	R/W	0x0	PD[n] Pull-up/down Select (n = 0~12) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.7.3.45. PE Pull Register 1

Offset: 0xB0			Register Name: PE_PULL1
Bit	R/W	Default/Hex	Description
31:0	/	/	Reserved

3.7.3.46. PF Configure Register 0

Offset: 0xB4			Register Name: PF_CFG0	
Bit	R/W	Default/Hex	Description	
31:23	/	/	Reserved	
22:20	R/W	3	PF5 Select 000: Input 010: SDC0_D2 100: PWM1 110: EINTF5	 001: Output 011: DBG_CK 101: Reserved 111: Disabled
19	/	/	Reserved	
18:16	R/W	7	PF4 Select 000: Input 010: SDC0_D3 100: Reserved 110: EINTF4	 001: Output 011: UART0_TX 101: Reserved 111: Disabled
15	/	/	Reserved	
14:12	R/W	3	PF3 Select 000: Input 010: SDC0_CMD 100: Reserved 110: EINTF3	 001: Output 011: DBG_DO 101: Reserved 111: Disabled
11	/	/	Reserved	
10:8	R/W	7	PF2 Select 000: Input 010: SDC0_CLK 100: Reserved 110: EINTF2	 001: Output 011: UART0_TX 101: Reserved 111: Disabled
7	/	/	Reserved	
6:4	R/W	3	PF1 Select 000: Input 010: SDC0_D0 100: Reserved 110: EINTF1	 001: Output 011: DBG_DI 101: Reserved 111: Disabled
3	/	/	Reserved	
2:0	R/W	3	PF0 Select 000: Input 010: SDC0_D1 100: IR_RX 110: EINTF0	 001: Output 011: DBG_MS 101: Reserved 111: Disabled

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.7.3.47. PF Configure Register 1

Offset: 0xB8			Register Name: PF_CFG1
Bit	R/W	Default/Hex	Description
31:0	/	/	Reserved

3.7.3.48. PF Configure Register 2

Offset: 0xBC			Register Name: PF_CFG2
Bit	R/W	Default/Hex	Description
31:0	/	/	Reserved

3.7.3.49. PF Configure Register 3

Offset: 0xC0			Register Name: PF_CFG3
Bit	R/W	Default/Hex	Description
31:0	/	/	Reserved

3.7.3.50. PF Data Register

Offset: 0xC4			Register Name: PF_DAT
Bit	R/W	Default/Hex	Description
31:6	/	/	Reserved
5:0	R/W	0	If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

3.7.3.51. PF Multi-Driving Register 0

Offset: 0xC8			Register Name: PF_DRV0
Bit	R/W	Default/Hex	Description
31:12	/	/	Reserved
[2i+1:2i] (i=0~5)	R/W	1	PD[n] Multi-Driving Select (n = 0~5) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

3.7.3.52. PF Multi-Driving Register 1

Offset: 0xCC			Register Name: PF_DRV1
Bit	R/W	Default/Hex	Description
31:0	/	/	Reserved

3.7.3.53. PF Pull Register 0

Offset: 0xD0			Register Name: PF_PULL0
Bit	R/W	Default/Hex	Description
31:0	/	/	Reserved

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.7.3.54. PD External Interrupt Configure Register 0

Offset: 0x200			Register Name:PD_EINT_CFG0
Bit	R/W	Default/Hex	Description
[4i+3:4i] (i=0~7)	R/W	0	EINT_CFG External INTn Mode (n = 0~7) 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved

3.7.3.55. PD External Interrupt Configure Register 1

Offset: 0x204			Register Name: PD_EINT_CFG1
Bit	R/W	Default/Hex	Description
[4i+3:4i] (i=0~7)	R/W	0	EINT_CFG External INTn Mode (n = 8~15) 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved

3.7.3.56. PD External Interrupt Configure Register 2

Offset: 0x208			Register Name: PD_EINT_CFG2
Bit	R/W	Default/Hex	Description
31:24	/	/	Reserved
[4i+3:4i] (i=0~5)	R/W	0	EINT_CFG External INTn Mode (n = 16~21)

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved

3.7.3.57. PD External Interrupt Configure Register 3

Offset: 0x20C			Register Name: PD_EINT_CFG3
Bit	R/W	Default/Hex	Description
31:0	/	/	Reserved

3.7.3.58. PD External Interrupt Control Register

Offset: 0x210			Register Name: PD_EINT_CTRL
Bit	R/W	Default/Hex	Description
31:22	/	/	Reserved
[n] (n=0~21)	R/W	0	EINT_CTL External INTn Enable (n = 0~21) 0: Disable 1: Enable

3.7.3.59. PD External Interrupt Status Register

Offset: 0x214			Register Name: PD_EINT_STATUS
Bit	R/W	Default/Hex	Description
31:22	/	/	Reserved
[n] (n=0~21)	R/W	0	EINT_STATUS External INTn Pending Bit (n = 0~21) 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear

3.7.3.60. PD External Interrupt Debounce Register

Offset: 0x218			Register Name: PD_EINT_DEB
Bit	R/W	Default/Hex	Description

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

31:7	/	/	Reserved
6:4	R/W	0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32Khz 1: HOSC 24Mhz

3.7.3.61. PE External Interrupt Configure Register 0

Offset: 0x220			Register Name:PE_EINT_CFG0
Bit	R/W	Default/Hex	Description
[4i+3:4i] (i=0~7)	R/W	0	EINT_CFG External INTn Mode (n = 0~7) 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved

3.7.3.62. PE External Interrupt Configure Register 1

Offset: 0x224			Register Name: PE_EINT_CFG1
Bit	R/W	Default/Hex	Description
31:20	/	/	Reserved
[4i+3:4i] (i=0~4)	R/W	0	EINT_CFG External INTn Mode (n = 8~12) 0x0: Positive Edge 0x1: Negative Edge

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved

3.7.3.63. PE External Interrupt Configure Register 2

Offset: 0x228			Register Name: PE_EINT_CFG2
Bit	R/W	Default/Hex	Description
31:0	/	/	/

3.7.3.64. PE External Interrupt Configure Register 3

Offset: 0x22C			Register Name: PE_EINT_CFG3
Bit	R/W	Default/Hex	Description
31:0	/	/	/

3.7.3.65. PE External Interrupt Control Register

Offset: 0x230			Register Name: PE_EINT_CTRL
Bit	R/W	Default/Hex	Description
31:13	/	/	Reserved
[n] (n=0~12)	R/W	0	EINT_CTL External INTn Enable (n = 0~12) 0: Disable 1: Enable

3.7.3.66. PE External Interrupt Status Register

Offset: 0x234			Register Name: PE_EINT_STATUS
Bit	R/W	Default/Hex	Description
31:12	/	/	Reserved
[n] (n=0~12)	R/W	0	EINT_STATUS External INTn Pending Bit (n = 0~12) 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear

3.7.3.67. PE External Interrupt Debounce Register

Offset: 0x238	Register Name: PE_EINT_DEB

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	R/W	Default/Hex	Description
31:7	/	/	/
6:4	R/W	0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32Khz 1: HOSC 24Mhz

3.7.3.68. PF External Interrupt Configure Register 0

Offset: 0x240			Register Name:PF_EINT_CFG0
Bit	R/W	Default/Hex	Description
31:24	/	/	Reserved
[4i+3:4i] (i=0~5)	R/W	0	EINT_CFG External INTn Mode (n = 0~5) 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved

3.7.3.69. PF External Interrupt Configure Register 1

Offset: 0x244			Register Name: PF_EINT_CFG1
Bit	R/W	Default/Hex	Description
31:0	/	/	Reserved

3.7.3.70. PF External Interrupt Configure Register 2

Offset: 0x248			Register Name: PF_EINT_CFG2
Bit	R/W	Default/Hex	Description
31:0	/	/	/

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

3.7.3.71. PF External Interrupt Configure Register 3

Offset: 0x24C			Register Name: PF_EINT_CFG3
Bit	R/W	Default/Hex	Description
31:0	/	/	/

3.7.3.72. PF External Interrupt Control Register

Offset: 0x250			Register Name: PF_EINT_CTRL
Bit	R/W	Default/Hex	Description
31:6	/	/	/
[n] (n=0~5)	R/W	0	EINT_CTL External INTn Enable (n = 0~5) 0: Disable 1: Enable

3.7.3.73. PF External Interrupt Status Register

Offset: 0x254			Register Name: PF_EINT_STATUS
Bit	R/W	Default/Hex	Description
31:6	/	/	/
[n] (n=0~5)	R/W	0	EINT_STATUS External INTn Pending Bit (n = 0~5) 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear

3.7.3.74. PF External Interrupt Debounce Register

Offset: 0x258			Register Name: PF_EINT_DEB
Bit	R/W	Default/Hex	Description
31:7	/	/	/
6:4	R/W	0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0: LOSC 32Khz 1: HOSC 24Mhz

3.7.3.75. SDRAM Pad Multi-Driving Register

Offset: 0x2C0			Register Name: SDR_PAD_DRV
Bit	R/W	Default/Hex	Description
31:14	/	/	Reserved
13:12	R/W	0x1	ODT Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
11:10	R/W	0x1	RAS#, CAS#, SWE#, SCS#, CKE Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
9:8	R/W	0x1	DQS[3:0] Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
7:6	R/W	0x1	DQM[3:0] Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
5:4	R/W	0x1	DA[n], BA2,BA1, BA0 Multi-Driving Select (n=0~14) 00: Level 0 01: Level 1 10: Level 2 11: Level 3
3:2	R/W	0x1	CK, CK# Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
1:0	R/W	0x1	DQ[n] Multi-Driving Select (n = 0~31) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

3.7.3.76. SDRAM Pad Pull Register

Offset: 0x2C4	Register Name: SDR_PAD_PULL

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	R/W	Default/Hex	Description
31:24	/	/	Reserved
23	R/W	0x0	Internal Reference Enable 0: disable 1: enable
22:17	R/W	0x0	Reference Configuration Factor ((64 + Factor) / 192) * VDDQ
16	R/W	0x1	SDRAM Pad Type 0: LVCMOS 1: SSTL-2 Notes: SSTL2 pad type is only used for normal 2.5v DDR. For other dram, LVCMOS pad should be select.
15:10	/	/	Reserved
9:8	R/W	0x1	DQS[1:0] Pull-up Select 00: Pull-up disable 01: Pull-up 10: Reserved 11: Reserved
7:6	R/W	0x0	DQM[1:0] Pull-up Select 00: Pull-up disable 01: Pull-up 10: Reserved 11: Reserved
5:4	R/W	0x0	Reserved
3:2	R/W	0x0	CK, CK# Pull-up Select 00: Pull-up disable 01: Pull-up 10: Reserved 11: Reserved
1:0	R/W	0x1	DQ[n] Pull-up Select (n = 0~31) 00: Pull-up disable 01: Pull-up 10: Reserved 11: Reserved

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

Chapter 4. ADC

This section describes the F1C200s memory from two aspects:

- KEYADC
- TP
- Audio Codec

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

4.1. KEYADC

4.1.1. Overview

KEYADC is 6-bit resolution ADC for key application. The KEYADC can work up to 250Hz conversion rate.

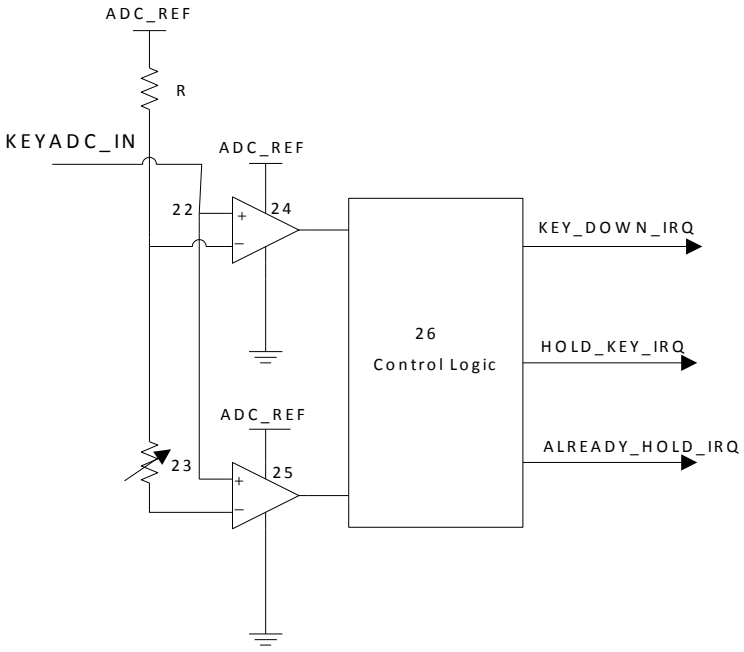
4.1.2. Feature

- Supports APB 32-bits bus width
- Interrupt Support
- Support Hold Key and General Key
- Support Single Key and continue key mode
- 6-bits Resolution
- Voltage input range between 0 to 2V
- Sample Rate up to 250Hz

4.1.3. Principle of operation

The KEYADC converted data can accessed by interrupt and polling method. If software can't access the last converted data instantly, the new converted data would update the old one at new sampling data.

4.1.4. Block diagram



 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

4.1.5. KEYADC Register List

Module Name	Base Address
KEYADC	0x01C23400

Register Name	Offset	Description
KEYADC_CTRL_REG	0x00	KEYADC Control Register
KEYADC_INTC_REG	0x04	KEYADC Interrupt Control Register
KEYADC_INTS_REG	0x08	KEYADC Interrupt Status Register
KEYADC_DATA_REG	0x0C	KEYADC Data Register

4.1.6. KEYADC Register Description

4.1.6.1. KEYADC Control Register

Offset: 0x00			Register Name: KEYADC_CTRL_REG
Bit	R/W	Default/Hex	Description
31:24	R/W	0x1	FIRST_CONCERT_DLY ADC First Convert Delay setting, ADC conversion is delayed by n samples
23:22	R/W	0x0	Reserved to 0
21:20	/	/	/
19:16	R/W	0x0	CONTINUE_TIME_SELECT. Continue Mode time select, one of 8*(N+1) sample as a valuable sample data
15:14	/	/	/
13:12	R/W	0x0	KEY_MODE_SELECT. Key Mode Select: 00: Normal Mode 01: Single Mode 10: Continue Mode
11:8	R/W	0x1	LEVELA_B_CNT. Level A to Level B time threshold select, judge ADC convert value in level A to level B in n+1 samples
7	R/W	0X0	KEY_ADC_HOLD_KEY_EN KEY_ADC Hold Key Enable 0: Disable 1: Enable
6	R/W	0x1	KEYADC_HOLD_EN. KEYADC Sample hold Enable 0: Disable 1: Enable
5: 4	R/W	0x2	LEVELB_VOL. Level B Corresponding Data Value setting (the real voltage value)

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			00: 0x3C (~1.9v) 01: 0x39 (~1.8v) 10: 0x36 (~1.7v) 11: 0x33 (~1.6v)
3: 2	R/W	0x2	KEYADC_SAMPLE_RATE. KEYADC Sample Rate 00: 250 Hz 01: 125 Hz 10: 62.5 Hz 11: 32.25 Hz
1	/	/	/
0	R/W	0x0	KEYADC_EN. KEYADC enable 0: Disable 1: Enable

4.1.6.2. KEYADC Interrupt Control Register

Offset: 0x04			Register Name: KEYADC_INTC_REG
Bit	R/W	Default/Hex	Description
31:5	/	/	/
4	R/W	0x0	ADC0_KEYUP_IRQ_EN. ADC 0 Key Up IRQ Enable 0: Disable 1: Enable
3	R/W	0x0	ADC0_ALRDY_HOLD_IRQ_EN. ADC 0 Already Hold IRQ Enable 0: Disable 1: Enable
2	R/W	0x0	ADC0_HOLD_IRQ_EN. ADC 0 Hold Key IRQ Enable 0: Disable 1: Enable
1	R/W	0x0	ADC0_KEYDOWN_EN ADC 0 Key Down Enable 0: Disable 1: Enable
0	R/W	0x0	ADC0_DATA_IRQ_EN. ADC 0 Data IRQ Enable 0: Disable 1: Enable

4.1.6.3. KEYADC Interrupt Status Register

Offset: 0x08			Register Name: KEYADC_INTS_REG
Bit	R/W	Default/Hex	Description
31:5	/	/	/

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

4	R/W	0x0	ADC0_KEYUP_PENDING. ADC 0 Key up pending Bit When general key pull up, it the corresponding interrupt is enabled. 0: No IRQ 1: IRQ Pending Notes: Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enable
3	R/W	0x0	ADC0_ALRDY_HOLD_PENDING. ADC 0 Already Hold Pending Bit When hold key pull down and pull the general key down, if the corresponding interrupt is enabled. 0: No IRQ 1: IRQ Pending Notes: Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enable
2	R/W	0x0	ADC0_HOLDKEY_PENDING. ADC 0 Hold Key pending Bit When Hold key pull down, the status bit is set and the interrupt line is set if the corresponding interrupt is enabled. 0: No IRQ 1: IRQ Pending Notes: Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enable.
1	R/W	0x0	ADC0_KEYDOWN_PENDING. ADC 0 Key Down IRQ Pending Bit When General key pull down, the status bit is set and the interrupt line is set if the corresponding interrupt is enabled. 0: No IRQ 1: IRQ Pending Notes: Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enable.
0	R/W	0x0	ADC0_DATA_PENDING. ADC 0 Data IRQ Pending Bit 0: No IRQ 1: IRQ Pending Notes: Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enable.

4.1.6.4. KEYADC Data Register

Offset: 0x0C			Register Name: KEYADC_DATA_REG
Bit	R/W	Default/Hex	Description
31:6	/	/	/
5:0	R	0x0	KEYADC_DATA. KEYADC Data

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

4.2. TP

4.2.1. Overview

The controller is a 4-wire resistive touch screen controller, includes 12-bit resolution A/D converter. Especially, it provides the ability of dual touch detection. The controller through the implementation of the two A/D conversion has been identified by the location of the screen of single touch, in addition to measurable increase in pressure on the touch screen.

4.2.2. Feature

- 12 bit SAR type A/D converter
- 4-wire I/F
- Dual Touch Detect
- Touch-pressure measurement (Support programmable threshold)
- Sampling frequency: 2MHz (max)
- Single-Ended Conversion of Touch Screen Inputs and Ratio Metric Conversion of Touch Screen Inputs
- TACQ up to 262ms
- Median and averaging filter to reduce noise
- Pen down detection, with programmable sensitivity
- Support X, Y change function

4.2.3. A/D conversion time

When the clock source is 24MHz and the prescalar value is 6, total 12-bit conversion time is as follows:

CLK_IN = 24MHz/6 = 4MHz

Conversion Time = 1 / (4MHz/13Cycles) = 3.25us

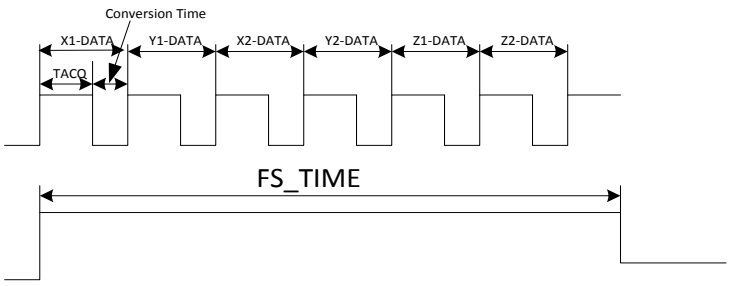
4.2.4. Work timing in different mode

FS_TIME (Frequency Scan Time) bases on TACQ and Touch Mode, they must meet the following in equation:

FS_TIME >= M*(TACQ + Conversion Time)

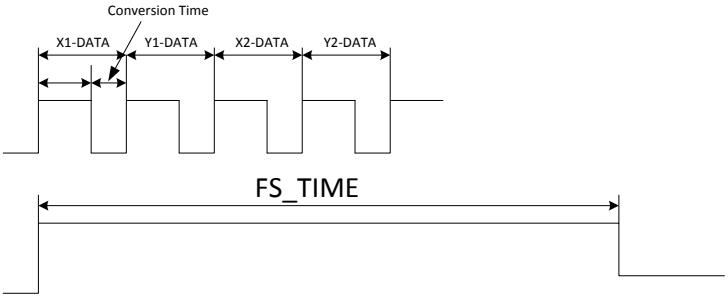
For example, if touch acquire time divider is 15, then TACQ = 4MHz /(16*(15+1)) = 64us.

When TP mode is dual and pressure measurement mode, then M=6, and the FS_TIME must be great or equal 6*(64 + 3.25) us.

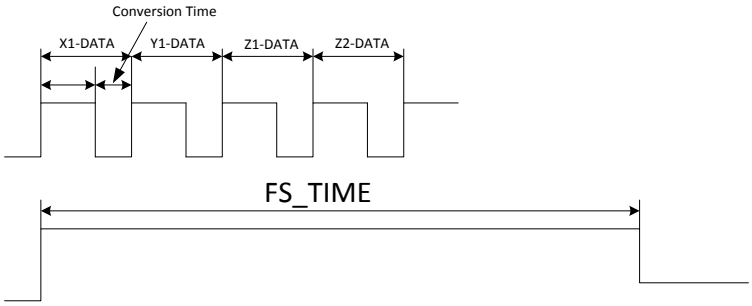


Dual Touch and Pressure Measurement

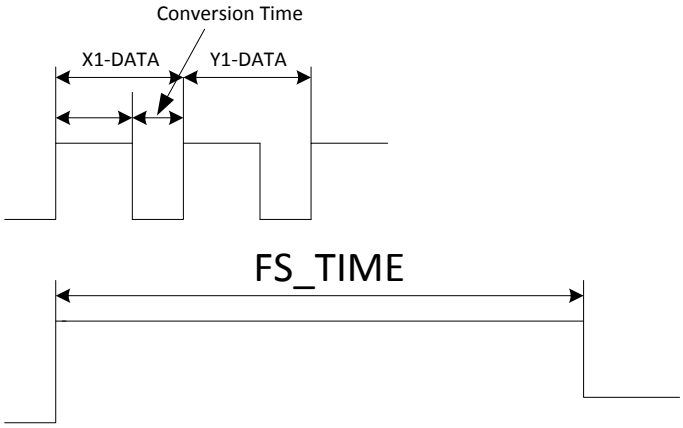
 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.



Dual Touch No Pressure Measurement

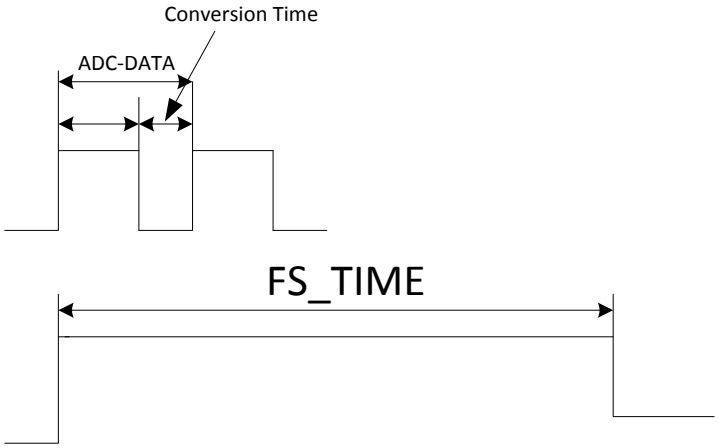


Single Touch and Pressure Measurement Mode



Single Touch No Pressure Measurement Mode

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.



General ADC Mode

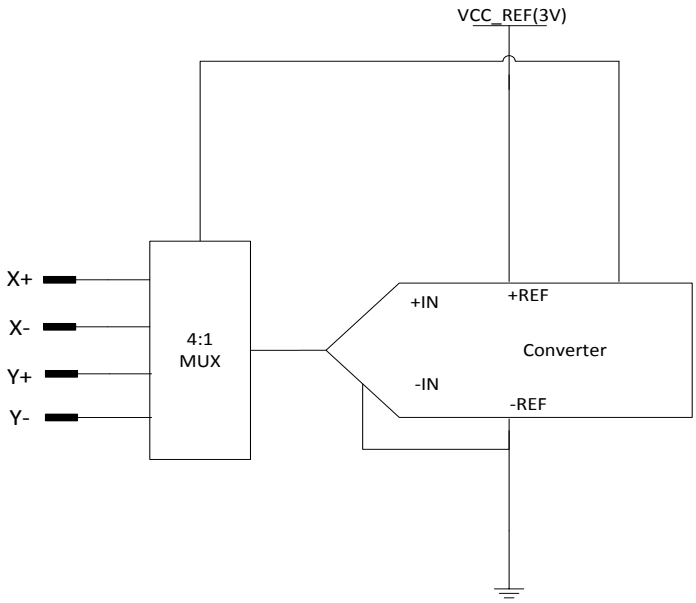
4.2.5. Operation Mode

4.2.5.1. Basic principle

The controller is a typical type of successive approximation ADC (SAR ADC), contains a sample/hold, analog-to-digital conversion, serial data output functions. The analog inputs (X+, X-, Y+, Y-) via control register enter the ADC, ADC can work in single-ended or differential mode. Selecting Aux ADC should work in single-ended mode; as a touch screen application, it works in a differential mode, which can effectively eliminate the impact on conversion accuracy caused by the parasitic resistance of the driver switch and external interference.

4.2.5.2. Single-ended mode

When the TP controller is in the measurement mode of AUX, the internal ADC is in single-ended mode, using the 3V reference source as the ADC reference voltage, application of the principle of single-ended mode shown in following figure.

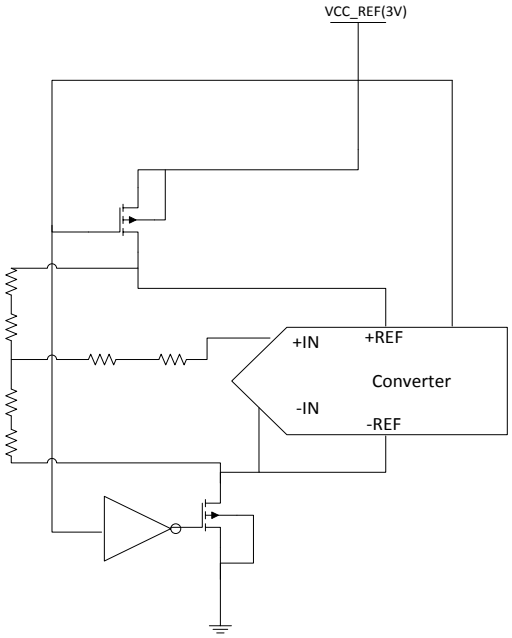


Simplified Diagram of Single-Ended Reference

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

4.2.5.3. Differential mode

When the TP the controller is in the measurement mode of X/Y/Z, the internal ADC is in differential mode, shown in the following Figure. The advantage of differential mode: +REF and –REF input directly to the Y+, Y-, which can eliminate measurement error because of the switch on-resistance. The disadvantage is that: both the sample or conversion process, the driver will need to be on. So relative to single-ended mode, the power consumption increased.

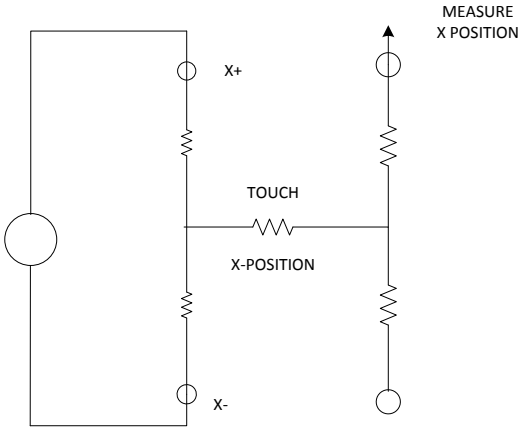


Simplified Diagram of Differential Reference

4.2.5.4. Single touch detection

The principle of operation is illustrated below, For an X coordinate measurement; the X+ pin is internally switched to VCC_REF and X- to GND. The X plate becomes a potential divider, and the voltage at the point of contact is proportional to its X co-ordinate. This voltage is measured on the Y+, which carry no current (hence there is no voltage drop in R_Y+ or R_Y-). Due to the ratio metric measurement method, the supply voltage does not affect measurement accuracy. The voltage references VREF+ and VREF- are taken from after the matrix switches, so that any voltage drop in these switches has no effect on the ADC measurement. Y coordinate measurements are similar to X coordinate measurements, with the X and Y plates interchanged. In Single Touch mode, only need to test X+, Y+ signal. But In Dual Touch mode, it need to test X+, X-,Y+,Y- signal.

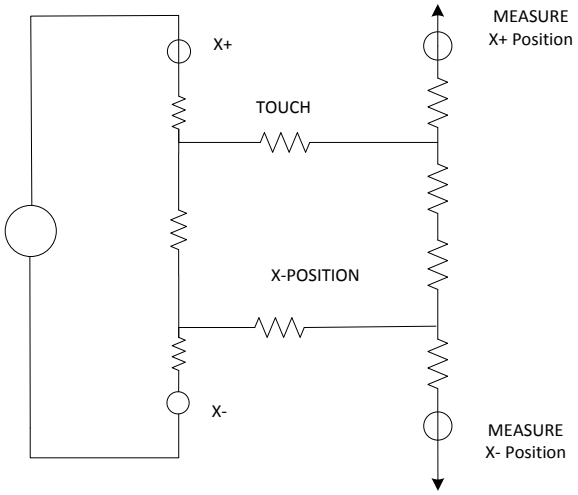
 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.



Single Touch X-Position Measurement

4.2.5.5. Dual touch detection

The principle of operation is illustrated below, For an X coordinate measurement; the X+ pin is internally switched to 3V and X- to GND. The X plate becomes a potential divider, and the voltage at the point of contact is proportional to its X coordinate. This voltage is measured on the Y+ and Y-, which carry no current (hence there is no voltage drop in R_Y+ or R_Y-). Due to the ratio metric measurement method, the supply voltage does not affect measurement accuracy. The voltage references VREF+ and VREF- are taken from after the matrix switches, so that any voltage drop in these switches has no effect on the ADC measurement. the controller will need to test X+,X-,Y+,Y- , and record Δ X=|X+ - X-|, Δ Y= | Y+ - Y-|. In practice, we can set a threshold. If Δ X or Δ Y greater than the threshold, we consider it as a dual touch, otherwise as a single touch.



Dual Touch X-Position Measurements

4.2.5.6. Touch pressure measurement

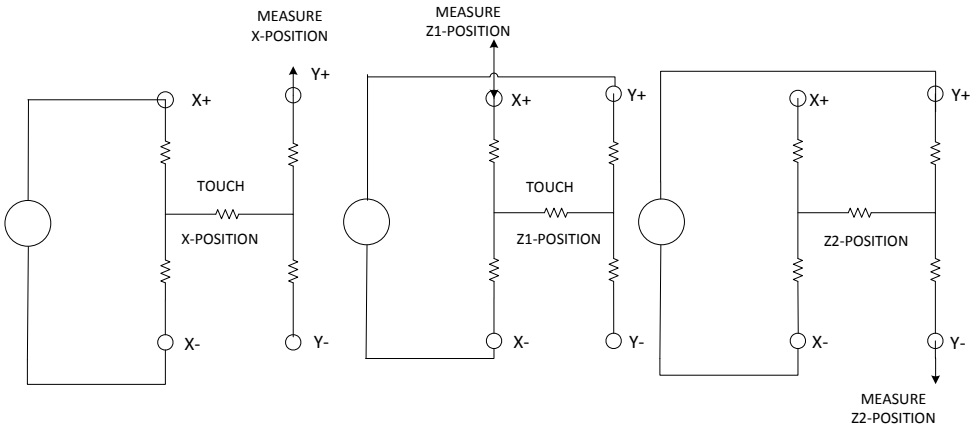
The pressure applied to the touch screen by a pen or finger to filter unavailable can also be measured by the controller using some simple calculations. The contact resistance between the X and Y plates is measured, which provides a good indication of the size of the depressed area and the applied pressure. The area of the touch spot t is proportional to the size of the object touching it. And the value of this resistance (R_{touch}) can be calculated using two different methods.

First Method:

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

The first method requires the user to know the total resistance of the X plate tablet (R_{XPLATE}). Three touch screen conversions are required: measurement of the X position, $X_{POSITION}$(Y+ input); measurement of the X+ input with the excitation voltage applied to Y+ and X− (Z1 measurement); and measurement of the Y− input with the excitation voltage applied to Y+ and X− (Z2 measurement). These three measurements are illustrated in following Figure. The controller have two special ADC channel settings to configure the X and Y switches for the Z1 and Z2 measurements and store the results in the Z1 and Z2 result registers. The touch resistance (R_{TOUCH}) can then be calculated using the following equation.

$$R_{TOUCH} = (R_{XPLATE}) \times (X_{POSITION}/4096) \times [(Z2/Z1) - 1]$$



Pressure Measurement

Second Method:

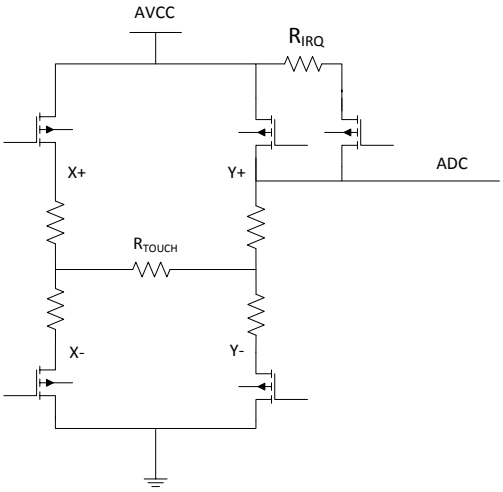
The second method requires the user to know the resistance of the X-plate and Y-plate tablets. Three touch screen conversions are required: a measurement of the X position ($X_{POSITION}$), the Y position ($Y_{POSITION}$), and the Z1 position. The following equation also calculates the touch resistance (R_{TOUCH}).

$$R_{TOUCH} = R_{XPLATE} \times (X_{POSITION}/4096) \times [(4096/Z1) - 1] - R_{YPLATE} \times [1 - (Y_{POSITION}/4096)]$$

4.2.5.7. Pen down detection, with programmable sensitivity

Pen down detection is used as an interrupt to the host. R_{IRQ} is an internal pull-up resistor with a programmable value of 6~96 kΩ (default 48kΩ). The pen down IRQ output is pulled high by an internal pull-up. In the pen down detection, the Y– driver is on and connected to GND, and the pen down IRQ output is connected to the X+ input. When the panel is touched, the X+ input is pulled to ground through the touch screen, and the pen down IRQ output goes low because of the current path through the panel to GND, initiating an interrupt to the processor. During the measurement cycle for X-, Y-, and Z-position, the X+ input is disconnected from the pen down IRQ pull-down transistor to eliminate any pull-up resistor leakage current from flowing through the touch screen, thus causing no errors.

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.



Example of pen touch Interrupt via pen down IRQ

4.2.5.8. Median and averaging filter

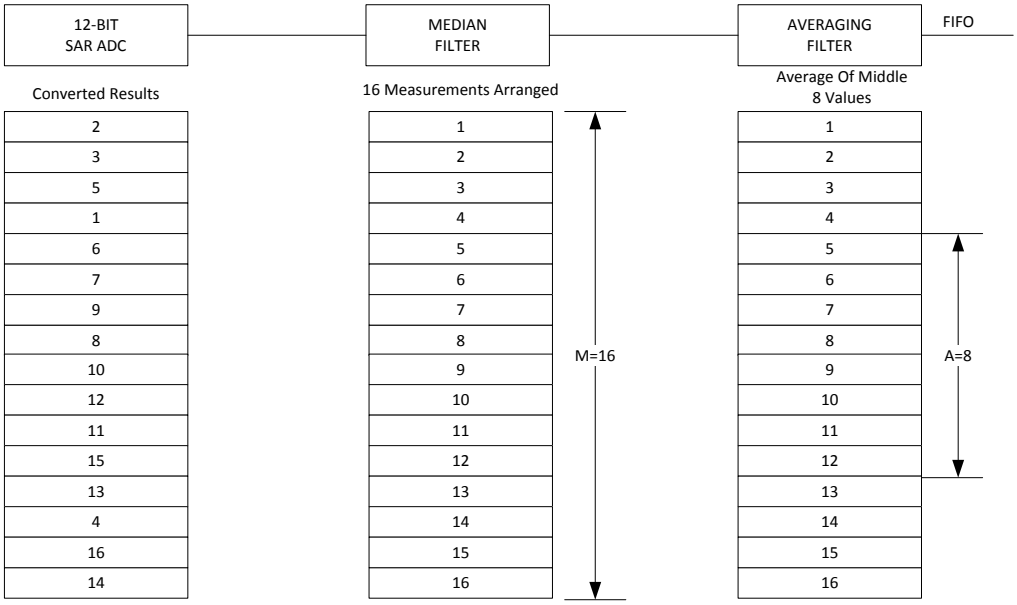
As explained in the Touch Screen Principles section, touch screens are composed of two resistive layers, normally placed over an LCD screen. Because these layers are in close proximity to the LCD screen, noise can be coupled from the screen onto these resistive layers, causing errors in the touch screen positional measurements. The controller contain a filtering block to process the data and discard the spurious noise before sending the information to the host. The purpose of this block is not only the suppression of noise; the on-chip filtering also greatly reduces the host processing loading. The processing function consists of two filters that are applied to the converted results: the median filter and the averaging filter. The median filter suppresses the isolated out-of-range noise and sets the number of measurements to be taken. These measurements are arranged in a temporary array, where the first value is the smallest measurement and the last value is the largest measurement. Then the averaging filter size determines the number of values to average. There are four choices which is configured by TP_CTRL3 register (bit 1 and bit 0) to filtrate the ADC sampling data. It is showed in following table.

Median and averaging Filter Size (TP_CTRL3)

bit1	bit0	Averaging Filter Size	Median Filter Size
0	0	2	4
0	1	3	5
1	0	4	8
1	1	8	16

Example： In this example, the TP_CTRL3 register bit 1 and bit 0 is configured as 2'b11. So the median filter has a window size of 16. This means that 16 measurements are taken and arranged in descending order in a temporary array. The averaging window size in this example is 8. The output is the average of the middle eight values of the 16 measurements taken with the median filter.

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.



Median and Averaging Filter Example

4.2.6. TP Register List

Module Name	Base Address
TP	0x01C24800

Register Name	Offset	Description
TP_CTRL_REG0	0x00	TP Control Register 0
TP_CTRL_REG1	0x04	TP Control Register 1
TP_CTRL_REG2	0x08	TP Control Register 2
TP_CTRL_REG3	0x0C	TP Control Register 3
TP_INT_FIFO_CTRL_REG	0x10	TP Interrupt FIFO Control Register
TP_INT_FIFO_STAT_REG	0x14	TP Interrupt FIFO Status Register
TP_COM_DATA_REG	0x1C	TP Common Data Register
TP_DATA_REG	0x24	TP Data Register

4.2.7. TP Register Description

4.2.7.1. TP Control Register 0

Offset: 0x00			Register Name: TP_CTRL_REG0
Bit	R/W	Default/Hex	Description
31:24	R/W	0xF	ADC_FIRST_DLY. ADC First Convert Delay Time(T_FCDT)setting Based on ADC First Convert Delay Mode select (Bit 23) T_FCDT = ADC_FIRST_DLY * ADC_FIRST_DLY_MODE
23	R/W	0x1	ADC_FIRST_DLY_MODE. ADC First Convert Delay Mode Select

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0: CLK_IN/16 1: CLK_IN/16*256
22	R/W	0x0	ADC_CLK_SELECT. ADC Clock Source Select: 0: OSC24M 1: Audio PLL
21:20	R/W	0x0	ADC_CLK_DIVIDER. ADC Clock Divider(CLK_IN) 00: CLK/2 01: CLK/3 10: CLK/6 11: CLK/1
19:16	R/W	0x0	FS_DIV. ADC Sample Frequency Divider 0000: CLK_IN/2(20-n) 0001: CLK_IN/2(20-n) 0010: CLK_IN/2(20-n) …. 1111: CLK_IN/32
15:0	R/W	0x0	TACQ. Touch panel ADC acquire time CLK_IN/(16*(N+1))

4.2.7.2. TP Control Register 1

Offset: 0x04			Register Name: TP_CTRL_REG1
Bit	R/W	Default/Hex	Description
31:20	/	/	/
19:12	R/W	0x0	STYLUS_UP_DEBOUNCE. Stylus Up De-bounce Time setting 0x00: 0 …. 0xff: 2N*(CLK_IN/16*256)
11:10	/	/	/
9	R/W	0x0	STYLUS_UP_DEBOUCE_EN. Stylus Up De-bounce Function Select 0: Disable 1: Enable
8	/	/	/
7	R/W	0x0	TOUCH_PAN_CALI_EN. Touch Panel Calibration 1: start Calibration, it is clear to 0 after calibration
6	R/W	0x0	TP_DUAL_EN. Touch Panel Double Point Enable 0: Disable 1: Enable

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

5	R/W	0x0	TP_EN. TP Function Enable 0: Disable 1: Enable
4	R/W	0x0	TP_MODE_SELECT. Touch Panel Mode and Auxiliary ADC Mode Select 0: TP 1: Auxiliary ADC
3	R/W	0x0	ADC_CHAN3_SELECT. Analog input channel 3 Select 0: Disable 1: Enable
2	R/W	0x0	ADC_CHAN2_SELECT. Analog input channel 2 Select 0: Disable 1: Enable
1	R/W	0x0	ADC_CHAN1_SELECT. Analog input channel 1 Select 0: Disable 1: Enable
0	R/W	0x1	ADC_CHAN0_SELECT. Analog input channel 0 Select 0: Disable 1: Enable

Note:

1) Channel 0~3 can be selected at the same time, but N channel selected, each channel has 1/N full speed of the ADC. When there is only one channel selected, it has the full conversion rate. CHAN0~3 correspond to TP_YN, TP_YP, TP_XN, TP_XP.

4.2.7.3. TP Control Register 2

Offset: 0x08			Register Name: TP_CTRL_REG2
Bit	R/W	Default/Hex	Description
31:28	R/W	0x8	TP_SENSITIVE_ADJUST. Internal Pull-up Resistor Control 0000 least sensitive 0011 …… 1111 most sensitive Notes: Used to adjust sensitivity of pen down detection
27:26	R/W	0x0	TP_FIFO_MODE_SELECT. TP FIFO Access Data Mode Select 00: FIFO store X1,Y1 data for single touch no pressure mode 01: FIFO store X1,Y1, Δ X, Δ Y data for dual touch no pressure mode 10: FIFO store X1,Y1, X2,Y2 data for dual touch no pressure mode 11: FIFO store X1,Y1, X2,Y2,Z1,Z2 data for dual touch and pressure mode

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Notes: The ADC output data in single touch mode can store in FIFO with TP_FIFO_MODE_SELECT configured as 01,10,11. But the data Δ X, Δ Y is theoretically equal to zero and X2,Y2 is equal to X1,Y1.
25	/	/	/
24	R/W	0x0	PRE_MEA_EN. TP Pressure Measurement Enable Control 0: Disable 1: Enable
23:0	R/W	0xFFF	PRE_MEA_THRE_CNT. TP Pressure Measurement threshold Control Notes: 0x000000: least sensitive 0xFFFFFF: most sensitive Notes: used to adjust sensitivity of touch

4.2.7.4. TP Control Register 3

Offset: 0x0C			Register Name: TP_CTRL_REG3
Bit	R/W	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	FILTER_EN. Filter Enable 0: Disable 1: Enable
1:0	R/W	0x1	FILTER_TYPE. Filter Type 00: 4/2 01: 5/3 10: 8/4 11: 16/8

4.2.7.5. TP Interrupt FIFO Control Register

Offset: 0x10			Register Name: TP_INT_FIFO_CTRL_REG
Bit	R/W	Default/Hex	Description
31:18	/	/	/
17	R/W	0x0	TP_OVERRUN_IRQ_EN. TP FIFO Over Run IRQ Enable 0: Disable 1: Enable
16	R/W	0x0	TP_DATA_IRQ_EN. TP FIFO Data Available IRQ Enable 0: Disable 1: Enable
15:14	/	/	/
13	R/W	0x0	TP_DATA_XY_CHANGE. TP FIFO X,Y Data interchange Function Select

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0: Disable 1: Enable
12:8	R/W	0xF	TP_FIFO_TRIG_LEVEL. TP FIFO Data Available Trigger Level Interrupt and DMA request trigger level for TP or Auxiliary ADC Trigger Level = TXTL + 1
7	R/W	0x0	TP_DATA_DRQ_EN. TP FIFO Data Available DRQ Enable 0: Disable 1: Enable
6:5	/	/	/
4	R/W	0x0	TP_FIFO_FLUSH. TP FIFO Flush Write '1' to flush TX FIFO, self clear to '0'
3:2	/	/	/
1	R/W	0x0	TP_UP_IRQ_EN. Touch Panel Last Touch (Stylus Up) IRQ Enable 0: Disable 1: Enable
0	R/W	0x0	TP_DOWN_IRQ_EN. Touch Panel First Touch (Stylus Down) IRQ Enable 0: Disable 1: Enable

4.2.7.6. TP Interrupt FIFO Status Register

Offset: 0x14			Register Name: TP_INT_FIFO_STAT_REG
Bit	R/W	Default/Hex	Description
31:18	/	/	/
17	R/W	0x0	FIFO_OVERRUN_PENDING. TP FIFO Over Run IRQ pending 0: No Pending IRQ 1: FIFO Overrun Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails
16	R/W	0x0	FIFO_DATA_PENDING. TP FIFO Data Available pending Bit 0: NO Pending IRQ 1: FIFO Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails
15:13	/	/	/
12:8	R	0x0	RXA_CNT. TP FIFO available Sample Word Counter
7:3	/	/	/
2	R	0x0	TP_IDLE_FLG. Touch Panel Idle Flag 0: idle

Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: not idle
1	R/W	0x0	TP_UP_PENDING. Touch Panel Last Touch (Stylus Up) IRQ Pending bit 0: No IRQ 1: IRQ Notes: Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enable.
0	R/W	0x0	TP_DOWN_PENDING. Touch Panel First Touch (Stylus Down) IRQ Pending bit 0: No IRQ 1: IRQ Notes: Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enable.

4.2.7.7. TP Common Data Register

Offset: 0x1C			Register Name: TP_COM_DATA_REG
Bit	R/W	Default/Hex	Description
31:12	/	/	/
11:0	R/W	0x0	TP_CDAT. TP Common Data Notes: used to adjust the tolerance of the internal ADC

4.2.7.8. TP Data Register

Offset: 0x24			Register Name: TP_DATA_REG
Bit	R/W	Default/Hex	Description
31:12	/	/	/
11:0	R	0x0	TP_DATA. Touch Panel X ,Y data or Auxiliary analogy input data converted by the internal ADC

Note：

In touch panel mode, the data stored in this register bases on TP_FIFO_MODE_SELECT. In Auxiliary ADC mode, the data stored in this register bases on ADC_CHAN_SELECT. If four channels are all enable, FIFO will access the input data in successive turn, first is ADC_CHAN0 data, then ADC_CHAN1, ADC_CHAN2, ADC_CHAN3 data. If there are only two or three channels selected, such as ADC_CHAN0 and ADC_CHAN3, firstly ADC_CHAN0 input data is accessed, then ADC_CHAN3 input data.

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

4.3. Audio Codec

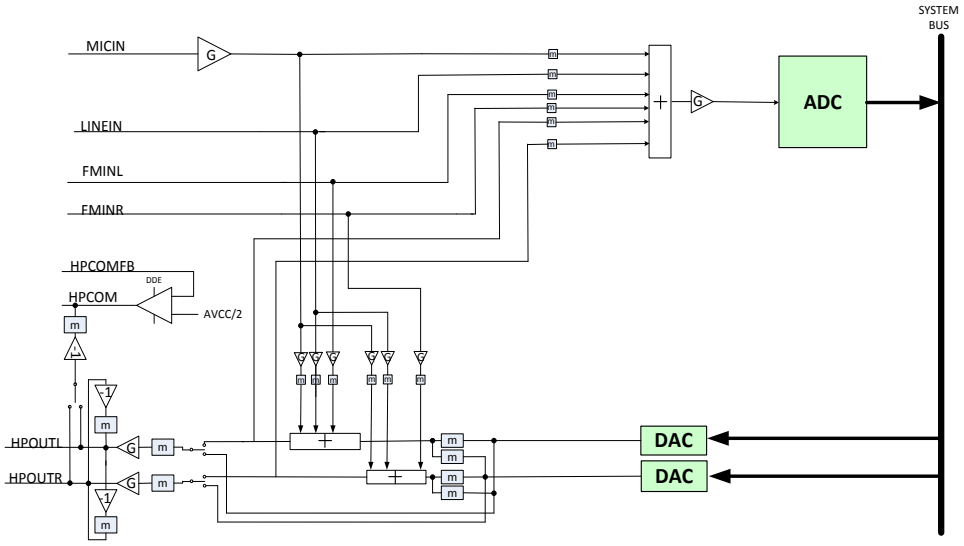
4.3.1. Overview

The embedded Audio Codec is a high-quality stereo audio codec designed for embed device. It provides a stereo DAC for playback, and a single ADC for recording.

4.3.2. Feature

- Two audio digital-to-analog (DAC) channels
- Stereo capless headphone drivers
  - Up to 100dB DR
  - Supports DAC Sample Rates from 8KHz to 192KHz
- Support analog/ digital volume control
- Analog low-power loop from line-in /microphone to lineout outputs
- Four audio inputs:
  - One microphone inputs
  - Stereo FM input
  - One line-in input
- One audio analog-to-digital(ADC) channel
  - 96dB SNR@A-weight
  - Supports ADC Sample Rates from 8KHz to 48KHz
  - Supports AGC
- Interrupt and DMA Support

4.3.3. Block diagram



The embedded Audio Codec

4.3.4. Signal Description

Signal Name	Type	Description

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

MICIN	I	Microphone input
FMINL	I	FM in left input
FMINR	I	FM in right input
LINEIN	I	Line in input
HPCOMFB	I	Headphone common reference feedback
HPCOM	O	Headphone common reference
HPOUTL	O	Headphone Left output
HPOUTR	O	Headphone Right output

4.3.5. Power Description

VRA1	O	Reference
VRA2	O	Reference
AVCC	I	Analog Power
HPVCC	O	Headphone Amplifier Power
AGND	GND	Analog Ground

4.3.6. Function Description

4.3.6.1. ADC

The ADC is used for recording sound. The sample rate of the ADC is independent of DAC sample rate. In order to save power，The volume control of the stereo ADC is set via register ADC_MIXER_CTRL Bit 18:16.

4.3.6.2. Stereo ADC

The stereo DAC can be configured to different sample rate by setting the register DAC_FIFOC Bit31:29. In order to save power, the left and right DAC can be powered down separately by setting register DAC_MIXER_CTRL Bit 31:30.

4.3.6.3. Mixer

The Codec supports two mixers for all function requirements:

1) Headphone mixer for dual channels
2) ADC record mixer for single channel

4.3.6.4. Headphone Mixer

The headphone mixer is used to drive stereo output, including HPOUTL/R, HPOUTL/R_N.

The following signals can be mixed into the headphone mixer:

1) FMINL/R
2) LINEIN
3) MICIN
4) Stereo DAC output

4.3.6.5. ADC Record Mixer

The ADC record mixer is used to mix analog signals as input to the ADC for recording.

1) FMINL/R
2) LINEIN

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

3) MICIN
4) Stereo DAC output

4.3.6.6. Analog Audio Input Path

The codec support four analog audio input paths:

1) FMINL
2) FMINR
3) LINEIN
4) MICIN

4.3.6.7. FM Input

FMINL and FMINR provide 2-channel stereo single-ended input that can be mixed into the Headphone mixer and ADC record mixer. The inputs are high impedance and low capacitance, thus ideally suited to receiving line level signals from external hi-fi or audio equipment or audio module FM.

Both line inputs include programmable volume level adjustments and ADC input mute. Passive RF and active Anti_Alias filters are also incorporated within the FM inputs. These prevent high frequencies aliasing into the audio band or otherwise degrading performance.

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

4.3.7. Audio Codec Register List

Module Name	Base Address
Audio Codec	0x01C23C00

Register Name	Offset	Description
AC_DAC_DPC_REG	0x00	DAC Digital Part Control Register
AC_DAC_FIFOC_REG	0x04	DAC FIFO Control Register
AC_DAC_FIFOS_REG	0x08	DAC FIFO Status Register
AC_DAC_TXDATA_REG	0x0c	DAC TX Data Register
AC_ADC_FIFOC_REG	0x10	ADC FIFO Control Register
AC_ADC_FIFOS_REG	0x14	ADC FIFO Status Register
AC_ADC_RXDATA_REG	0x18	ADC RX Data Register
DAC_MIXER_CTRL_REG	0x20	DAC&MIXER Control Register
ADC_MIXER_CTRL_REG	0x24	ADC Analog and Input mixer Control Register
ADDA_TUNE_REG	0x28	ADC&DAC performance tuning Register
BIAS_DA16_CAL_CTRL_REG0	0x2C	Bias&DA16 Calibration Control Register 0
BIAS_DA16_CAL_CTRL_REG1	0x34	Bias&DA16 Calibration Control Register 1
AC_DAC_CNT_REG	0x40	DAC TX FIFO Counter Register
AC_ADC_CNT_REG	0x44	ADC RX FIFO Counter Register
AC_DAC_DG_REG	0x48	DAC Debug Register
AC_ADC_DG_REG	0x4c	ADC Debug Register
AC_ADC_DAP_CTR_REG	0x70	ADC DAP Control Register
AC_ADC_DAP_LCTR_REG	0x74	ADC DAP Left Control Register
AC_ADC_DAP_RCTR_REG	0x78	ADC DAP Right Control Register
AC_ADC_DAP_PARA_REG	0x7C	ADC DAP Parameter Register
AC_ADC_DAP_LAC_REG	0x80	ADC DAP Left Average Coef Register
AC_ADC_DAP_LDAT_REG	0x84	ADC DAP Left Decay and Attack Time Register
AC_ADC_DAP_RAC_REG	0x88	ADC DAP Right Average Coef Register
AC_ADC_DAP_RDAT_REG	0x8C	ADC DAP Right Decay and Attack Time Register
ADC_DAP_HPFC_REG	0x90	ADC DAP HPF Coef Register
ADC_DAP_LINAC_REG	0x94	ADC DAP Left Input Signal Low Average Coef Register
ADC_DAP_RINAC_REG	0x98	ADC DAP Right Input Signal Low Average Coef Register
ADC_DAP_ORT_REG	0x9c	ADC DAP Optimum Register

4.3.8. Audio Codec Register Description

4.3.8.1. DAC Digital Part Control Register

Offset: 0x00			Register Name: AC_DAC_DPC_REG
Bit	R/W	Default/Hex	Description
31	R/W	0x0	EN_DA. DAC Digital Part Enable

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0: Disable 1: Enable
30:29	/	/	/
28:25	R/W	0x0	MODQU. Internal DAC Quantization Levels Levels=[7*(21+MODQU[3:0])]/128 Default levels=7*21/128=1.15
24	R/W	0x0	DWA. DWA Function Disable 0: Enable 1: Disable
23	/	/	/
22:21	R/W	0x0	HPVL_SOFT_MOD Headphone volume soft tuning mode 0X: Normal mode 10: Soft volume mode 11: DAC Soft disable or enable mode
20	R	0x0	DACA_CHND_ENA Internal status of DAC Analog channel enable control 0: Disable; 1: Enable
19	R/W	0x0	HPPA_MXRD_ENA Internal status of headphone PA mixer all-input mute control 0: Mute; 1: On
18	R/W	0x0	HPF_EN. High Pass Filter Enable 0: Disable 1: Enable
17:12	R/W	0x0	DVOL. Digital volume control: dvc, ATT=DVC[5:0]*(-1.16dB) 64 steps, -1.16dB/step
11:6	R/W	0x0	HPVL_STEP_CTRL Headphone volume soft tuning step control 0: 10us 1: 20us ... 7: 80us 8: 90us 9: 100us 10: 200us ... 16: 800us 17: 900us 18: 1ms 19: 2ms ...

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			25: 8ms 26: 9ms 27: 10ms 28: 20ms ... 34: 80ms 35: 90ms 36: 100ms 37: 200ms ... 43: 800ms 44: 900ms 45: 1s ... 52: 8s 53: 9s 54-63: 9s
5:0	R/W	0x10	HPVL_CTRL_OUT Internal status of headphone PA volume control Total 64 level, from -63dB to 0dB, 1dB/step, min when 000000(-63dB), max when 111111(0dB)

4.3.8.2. DAC FIFO Control Register

Offset: 0x04			Register Name: AC_DAC_FIFOC_REG
Bit	R/W	Default/Hex	Description
31:29	R/W	0x0	DAC_FS. Sample Rate of DAC 000: 48KHz 010: 24KHz 100: 12KHz 110: 192KHz 001: 32KHz 011: 16KHz 101: 8KHz 111: 96KHz 44.1KHz/22.05KHz/11.025KHz can be supported by Audio PLL Configure Bit
28	R/W	0	FIR_VER. FIR Version 0: 64-Tap FIR; 1: 32-Tap FIR
27	/	/	/
26	R/W	0x0	SEND_LASAT. Audio sample select when TX FIFO under run 0: Sending zero 1: Sending last audio sample
25:24	R/W	0x0	FIFO_MODE.

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			For 24-bits transmitted audio sample: 00/10: FIFO_I[23:0] = {TXDATA[31:8]} 01/11: Reserved For 16-bits transmitted audio sample: 00/10: FIFO_I[23:0] = {TXDATA[31:16], 8'b0} 01/11: FIFO_I[23:0] = {TXDATA[15:0], 8'b0}
23	/	/	/
22:21	R/W	0x0	DAC_DRQ_CLR_CNT. When TX FIFO available room less than or equal N, DRQ Request will be De-asserted. N is defined here: 00: IRQ/DRQ Deasserted when WLEVEL > TXTL 01: 4 10: 8 11: 16
20:15	/	/	/
14:8	R/W	0xF	TX_TRIG_LEVEL. TX FIFO Empty Trigger Level (TXTL[12:0]) Interrupt and DMA request trigger level for TX FIFO normal condition. IRQ/DRQ Generated when WLEVEL ≤ TXTL Notes: WLEVEL represents the number of valid samples in the TX FIFO Only TXTL[6:0] valid when TXMODE = 0
7	R/W	0x0	ADDA_LOOP_EN. ADDA loop Enable, adda 0: Disable 1: Enable
6	R/W	0x0	DAC_MONO_EN. DAC Mono Enable 0: Stereo, 64 levels FIFO 1: mono, 128 levels FIFO When enabled, L & R channel send same data
5	R/W	0x0	TX_SAMPLE_BITS. Transmitting Audio Sample Resolution 0: 16 bits 1: 24 bits
4	R/W	0x0	DAC_DRQ_EN. DAC FIFO Empty DRQ Enable 0: Disable 1: Enable
3	R/W	0x0	DAC_IRQ_EN. DAC FIFO Empty IRQ Enable 0: Disable 1: Enable
2	R/W	0x0	FIFO_UNDERRUN_IRQ_EN. DAC FIFO Under Run IRQ Enable 0: Disable

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: Enable
1	R/W	0x0	FIFO_OVERRUN_IRQ_EN. DAC FIFO Over Run IRQ Enable 0: Disable 1: Enable
0	R/W	0x0	FIFO_FLUSH. DAC FIFO Flush Write '1' to flush TX FIFO, self clear to '0'

4.3.8.3. DAC FIFO Status Register

Offset: 0x08			Register Name: AC_DAC_FIFOS_REG
Bit	R/W	Default/Hex	Description
31:24	/	/	/
23	R	0x1	TX_EMPTY. TX FIFO Empty 0: No room for new sample in TX FIFO 1: More than one room for new sample in TX FIFO (>= 1 word)
22:8	R	0x80	TXE_CNT. TX FIFO Empty Space Word Counter
7:4	/	/	/
3	R/W	0x1	TXE_INT. TX FIFO Empty Pending Interrupt 0: No Pending IRQ 1: FIFO Empty Pending Interrupt Write '1' to clear this interrupt or automatic clear if interrupt condition fails.
2	R/W	0x0	TXU_INT. TX FIFO Under run Pending Interrupt 0: No Pending Interrupt 1: FIFO Under run Pending Interrupt Write '1' to clear this interrupt
1	R/W	0x0	TXO_INT. TX FIFO Overrun Pending Interrupt 0: No Pending Interrupt 1: FIFO Overrun Pending Interrupt Write '1' to clear this interrupt
0	/	/	/

4.3.8.4. DAC TX DATA Register

Offset: 0x0C			Register Name: AC_DAC_TXDATA_REG
Bit	R/W	Default/Hex	Description
31:0	W	0x0	TX_DATA. Transmitting left, right channel sample data should be written this register one by one. The left channel sample data is first and then the right channel sample.

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

4.3.8.5. ADC FIFO Control Register

Offset: 0x10			Register Name: AC_ADC_FIFOC_REG
Bit	R/W	Default/Hex	Description
31:29	R/W	0x0	ADFS. Sample Rate of ADC 000: 48KHz 010: 24KHz 100: 12KHz 110: Reserved 001: 32KHz 011: 16KHz 101: 8KHz 111: Reserved 44.1KHz/22.05KHz/11.025KHz can be supported by Audio PLL Configure Bit
28	R/W	0x0	EN_AD. ADC Digital Part Enable, en_ad 0: Disable 1: Enable
27	/	/	/
26:25	/	/	/
24	R/W	0x0	RX_FIFO_MODE. RX FIFO Output Mode (Mode 0, 1) 0: Expanding ‘0’ at LSB of TX FIFO register 1: Expanding received sample sign bit at MSB of TX FIFO register For 24-bits received audio sample: Mode 0: RXDATA[31:0] = {FIFO_O[23:0], 8’h0} Mode 1: Reserved For 16-bits received audio sample: Mode 0: RXDATA[31:0] = {FIFO_O[23:8], 16’h0} Mode 1: RXDATA[31:0] = {16{FIFO_O[23]}, FIFO_O[23:8]}
23:19	/	/	/
18:17	R/W	0x0	ADCFDT. ADC FIFO Delay Time For writing Data after ADC digital part enable 00:5ms 01:10ms 10:20ms 11:30ms
16	R/W	0x0	ADCDFEN. ADC FIFO Delay Function For writing Data after ADC digital part enable 0: Disable 1: Enable
15:13	/	/	/
12:8	R/W	0xF	RX_FIFO_TRG_LEVEL. RX FIFO Trigger Level (RXTL[4:0]) Interrupt and DMA request trigger level for TX FIFO normal condition

Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			IRQ/DRQ Generated when WLEVEL ＞ RXTL[4:0] Notes: WLEVEL represents the number of valid samples in the RX FIFO
7	R/W	0x0	ADC_MONO_EN. ADC Mono Enable. 0: Stereo, 16 levels FIFO 1: mono, 32 levels FIFO When set to '1', Only left channel samples are recorded
6	R/W	0x0	RX_SAMPLE_BITS. Receiving Audio Sample Resolution 0: 16 bits 1: 24 bits
5	/	/	/
4	R/W	0x0	ADC_DRQ_EN. ADC FIFO Data Available DRQ Enable. 0: Disable 1: Enable
3	R/W	0x0	ADC_IRQ_EN. ADC FIFO Data Available IRQ Enable. 0: Disable 1: Enable
2	/	/	/
1	R/W	0x0	ADC_OVERRUN_IRQ_EN. ADC FIFO Over Run IRQ Enable 0: Disable 1: Enable
0	R/W	0x0	ADC_FIFO_FLUSH. ADC FIFO Flush. Write '1' to flush TX FIFO, self clear to '0'.

4.3.8.6. ADC FIFO Status Register

Offset: 0x14			Register Name: AC_ADC_FIFOS_REG
Bit	R/W	Default/Hex	Description
31:24	/	/	/
23	R	0x0	RXA. RX FIFO Available 0: No available data in RX FIFO 1: More than one sample in RX FIFO (>= 1 word)
22:14	/	/	/
13:8	R	0x0	RXA_CNT. RX FIFO Available Sample Word Counter
7:4	/	/	/
3	R/W	0x0	RXA_INT. RX FIFO Data Available Pending Interrupt 0: No Pending IRQ

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: Data Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails.
2	/	/	/
1	R/W	0x0	RXO_INT. RX FIFO Overrun Pending Interrupt 0: No Pending IRQ 1: FIFO Overrun Pending IRQ Write '1' to clear this interrupt
0	/	/	/

4.3.8.7. ADC RX DATA Register

Offset: 0x18			Register Name: AC_ADC_RXDATA_REG
Bit	R/W	Default/Hex	Description
31:0	R	0x0	RX_DATA. RX Sample Host can get one sample by reading this register. The left channel sample data is first and then the right channel sample.

4.3.8.8. DAC Analog & Output MIXER Control Register

Offset:20			Register Name: DAC_MIXER_CTRL_REG
Bit	R/W	Default/Hex	Description
31	R/W	0x0	DACAREN. Internal Analog Right channel DAC Enable 0:Disable; 1:Enable
30	R/W	0x0	DACALEN. Internal Analog Left channel DAC Enable 0:Disable; 1:Enable
29	R/W	0x0	RMIXEN. Right Analog Output Mixer Enable 0:Disable; 1:Enable
28	R/W	0x0	LMIXEN. Left Analog Output Mixer Enable 0:Disable; 1:Enable
27	R/W	0x0	RHPPAMUTE. All input source to Right Headphone PA mute, including Right Output mixer and Internal Right channel DAC: 0:Mute, 1: Not mute
26	R/W	0x0	LHPPAMUTE. All input source to Left Headphone PA mute, including Left Output mixer and Internal Left channel DAC: 0:Mute, 1: Not mute
25	R/W	0x0	RHPIS. Right Headphone Power Amplifier (PA) Input Source Select 0: Right channel DAC 1: Right Analog Mixer

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

24	R/W	0x0	LHPIS. Left Headphone Power Amplifier (PA) Input Source Select 0: Left channel DAC 1: Left Analog Mixer
23:22	R/W	0x0	HPCOM_FC. HPCOM function control 00: HPCOM off & output is floating 01: HPL inverting output 10: HPR inverting output 11: Direct driver for HPL & HPR
21	R/W	0x1	COMPTEN. HPCOM output protection enable when it is set as Direct driver for HPL/R 0: protection disable 1: protection enable
20:16	R/W	0x0	RMIXMUTE. Right Output Mixer Mute Control Mute, 1-Not mute Bit 4: MICIN Boost stage Bit 3: LINEIN Bit 2: FMINR Bit 1: Right channel DAC Bit 0: Left channel DAC
15	R/W	0x0	HPPAEN Right & Left Headphone Power Amplifier Enable 0-disable 1-enable
14:13	/	/	/
12:8	R/W	0x0	LMIXMUTE. Left Output Mixer Mute Control 0-Mute, 1-Not mute Bit 4: MICIN Boost stage Bit 3: LINEIN Bit 2: FMINL Bit 1: Left channel DAC Bit 0: Right channel DAC
7	R/W	0x0	LTRNMUTE. Left HPOUT Negative To Right HPOUT Mute 0: Mute 1: Not mute
6	R/W	0x0	RTLNMUTE. Right HPOUT Negative To Left HPOUT Mute 0: Mute 1: Not mute
5:0	R/W	0x0	HPVOL. Headphone Volume Control, (HPVOL): Total 64 level, from 0dB to -62dB,

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1dB/step, mute when 000000

4.3.8.9. ADC Analog and Input mixer Control Register

Offset: 0x24			Register Name: ADC_MIXER_CTRL_REG
Bit	R/W	Default/Hex	Description
31	R/W	0x0	ADCEN. ADC Analog Enable 0-Disable 1-Enable
30:27	/	/	/
26:24	R/W	0x3	MICG. MICIN BOOST stage to L or R output mixer Gain Control From -4.5dB to 6dB, 1.5dB/step, default is 0dB
23:21	R/W	0x0	LINEINVOL. LINEIN to L/R output mixer Gain Control From 0dB to 14dB, 2dB/step, default is 0dB
20:19	/	/	/
18:16	R/W	0x3	ADCG. ADC Input Gain Control From -4.5dB to 6dB, 1.5dB/step default is 0dB
15:14	R/W	0x1	COSSLOPECTRL. COS slop time control for Anti-pop 000: 131ms; 001: 262ms; 010: 393ms; 011: 524ms;
13:8	R/W	0x0	ADCMIXMUTE. ADC Mixer Mute Control: 0-Mute, 1-Not mute Bit 5: MICIN Boost stage Bit 4:FMINL Bit 3: FMINR Bit 2: LINEIN Bit 1: Left output mixer Bit 0: Right output mixer
7	R/W	0x0	PASPEEDSELECT. PA Speed Select; 0: Normal 1: Fast
6:4	R/W	0x0	FMINLVOL. FMINL/R to L/R output mixer Gain Control From 0dB to 14dB, 2dB/step, default is 0dB
3	R/W	0x0	MIC AMPEN. MIC Boost AMP Enable 0:Disable

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1:Enable
2:0	R/W	0x4	MICBOOST. MIC Boost AMP Gain Control 0dB when 000, 24dB to 42dB when 001 to 111, 3dB/step, default is 33dB

4.3.8.10. ADC&DAC performance tuning Register

Offset:0x28			Register Name: ADDA_TUNE_REG
Bit	R/W	Default/Hex	Description
31	R/W	0x0	ZERO_CROSS_EN. function enable for master volume change at zero cross over 0: disable 1: enable
30	R/W	0x0	ZERO_CROSS_TIME_SEL. Timeout control for master volume change at zero cross over 0: 32ms 1: 64ms
29:28	R/W	0x0	PTDBS HPCOM protect debounce time setting 00: 2-3ms; 01: 4-6ms; 10: 8-12ms; 11: 16-24ms at the same time, bit 17 is used to control the AVCCPORFLAG, write 1 to this bit, flag will be clear, and the calibration is done again
27	R/W	0x0	PA_SLOPE_SELECT PA slope select cosine or ramp 0: select cosine 1: select ramp
26:24	R/W	0x0	PA_ANTI_POP_CTRL. PA Anti-pop time Control 000:131ms 001:262ms 010:395ms 011:524ms 100:655ms 101:789ms 110:789ms 111:1048ms
23:22	R/W	0x0	OPMIC_BIAS_CUR OPMIC Bias Current Control
21:20	R/W	0x0	OPVR_BIAS_CUR. OPVR Bias Current Control
19:18	R/W	0x0	OPDAC_BIAS_CUR. OPDAC Bias Current Control
17:16	R/W	0x0	OPMIX_BIAS_CUR. OPMIX/OPLPF/OPDRV/OPCOM Bias Current Control
15:14	R/W	0x0	OPDRV_OPCOM_CUR. OPDRV/OPCOM output stage current setting

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

13:12	R/W	0x0	OPADC1_BIAS_CUR. OPADC1 Bias Current Select
11:10	R/W	0x0	OPADC2_BIAS_CUR. OPADC2 Bias Current Select
9:8	R/W	0x0	OPAAF_BIAS_CUR. OPAAF in ADC Bias Current Select
7:5	R/W	0x0	USB_BIAS_CUR. USB bias current tuning From 23uA to 30uA, Default is 25uA
4	R/W	0x0	DITHER ADC dither on/off control 0: dither off; 1: dither on
3:2	R/W	0x0	DITHER_CLK_SELECT ADC dither clock select 00: ADC FS * (8/9), about 43KHz when FS=48KHz 01: ADC FS * (16/15), about 51KHz when FS=48KHz 10: ADC FS * (4/3), about 64KHz when FS=48KHz 11: ADC FS * (16/9), about 85KHz when FS=48KHz
1:0	R/W	0x0	BIHE_CTRL, BIHE control 00: no BIHE 01: BIHE=7.5 HOSC 10: BIHE=11.5 HOSC 11: BIHE=15.5 HOSC

Note: This register must write 0x44555556 at the time of power on

4.3.8.11. Bias & DA16 Calibration Control Register 0

Offset:0x2C			Register Name: BIAS_DA16_CAL_CTRL0_REG
Bit	R/W	Default/Hex	Description
31:7	/	/	/
6	R/W	0x1	CURRENT_TEST_SELECT. Internal current sink test enable (from LINEIN pin) 0:Normal; 1: For Debug
5	/	/	/
4	R/W	0x1	BIAS and DA16 calibration clock select 0: 1KHz; 1: 500Hz
3	R/W	0x0	BIAS calibration mode select 0: average; 1: single
2	R/W	0x1	BIAS and DA16 calibration control Write 1 to this bit, the calibration will be doing again. Then this bit will be reset to zero automatically
1	R/W	0x1	BIASCALIVERIFY Bias Calibration Verify

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0: Calibration; 1: Register setting
0	R/W	0x0	DA16CALIVERIFY DA16 Calibration Verify 0: Calibration; 1: Register setting

Note: This register must write 0x00000004 at the time of power on

4.3.8.12. Bias & DA16 Calibration Control Register 1

Offset:0x34			Register Name: Bias_DA16_CAL_CTRL1_REG
Bit	R/W	Default/Hex	Description
31:29	/	/	/
28:23	R/W	0X0	BIASVERIFY Bias Register Setting Data, 6bit
22:0	/	/	/

Note: This register must write 0x10000000 at the time of power on

4.3.8.13. DAC TX Counter Register

Offset: 0x40			Register Name: AC_DAC_CNT_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0x0	TX_CNT. TX Sample Counter The audio sample number of sending into TXFIFO. When one sample is put into TXFIFO by DMA or by host IO, the TX sample counter register increases by one. The TX sample counter register can be set to any initial valve at any time. After been updated by the initial value, the counter register should count on base of this initial value. Notes: It is used for Audio/ Video Synchronization

4.3.8.14. ADC RX Counter Register

Offset: 0x44			Register Name: AC_ADC_CNT_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0x0	RX_CNT. RX Sample Counter The audio sample number of writing into RXFIFO. When one sample is written by Digital Audio Engine, the RX sample counter register increases by one. The RX sample counter register can be set to any initial valve at any time. After been updated by the initial value, the counter register should count on base of this initial value. Notes: It is used for Audio/ Video Synchronization

4.3.8.15. DAC Debug Register

Offset: 0x48			Register Name: AC_DAC_DG
Bit	R/W	Default/Hex	Description
31:12	/	/	/

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

11	R/W	0x0	DAC_MODU_SELECT. DAC Modulator Debug 0: DAC Modulator Normal Mode 1: DAC Modulator Debug Mode
10:9	R/W	0x0	DAC_PATTERN_SELECT. DAC Pattern Select 00: Normal (Audio Sample from TX FIFO) 01: -6 dB Sin wave 10: -60 dB Sin wave 11: silent wave
8	R/W	0x0	CODEC_CLK_SELECT. CODEC Clock Source Select: cksel 0: CODEC Clock from PLL 1: CODEC Clock from OSC (For Debug)
7	/	/	/
6	R/W	0x0	DA_SWP. DAC output channel swap enable, da_swp 0:Disable 1:Enable
5:0	/	/	/

4.3.8.16. ADC Debug Register

Offset: 0x4C			Register Name: AC_ADC_DG_REG
Bit	R/W	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	AD_SWP. ADC output channel swap enable (for digital filter) 0: disable 1: enable
23:0	/	/	/

4.3.8.17. ADC DAP Control Register

Offset: 0x70			Register Name: AC_ADC_DAP_CTR_REG
Bit	R/W	Default/Hex	Description
31	R/W	0X0	DAP_EN DAP for ADC enable 0 : bypass 1: enable
30	R/W	0x0	ADAP_ START. DAP for ADC start up 0 : disable 1: start up
29:22	/	/	/
21	R	0x0	ADAP_LSATU_FLAG. Left channel AGC saturation flag 0 : no saturation

Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: saturation
20	R	0x0	ADAP_LNOI_FLAG. Left channel AGC noise-threshold flag 0: 1:
19:12	R	0x0	ADAP_LCHAN_GAIN Left channel Gain applied by AGC (7.1format 2s component(-20dB – 40dB), 0.5dB/ step) 0x50 : 40dB 0x4F : 39.5dB ---------- 0x00 : 00dB 0xFF : -0.5dB
11:10	/	/	/
9	R	0x0	ADAP_RSATU_FLAG. Right AGC saturation flag 0 : no saturation 1: saturation
8	R	0x0	ADAP_RNOI_FLAG. Right channel AGC noise-threshold flag 0: 1:
7:0	R	0x0	ADAP_LCHAN_GAIN. Right Channel Gain applied by AGC (7.1format 2s component)(0.5dB step） 0x50 : 40dB 0x4F : 39.5dB ---------- 0x00 : 00dB 0xFF : -0.5dB

4.3.8.18. ADC DAP Left Control Register

Offset: 0x74			Register Name: AC_ADC_DAP_LCTR_REG
Bit	R/W	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0x1F (-86dB)	ADAP_LNOI_SET. Left channel noise threshold setting 0x00 : -24dB 0x01 : -26dB 0x02 : -28dB ---------- 0x1D: -82dB 0x1E: -84dB 0x1F: -86dB
15	/	/	/
14	R/W	0x1	AAGC_LCHAN_EN.

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Left AGC function enable 0:disable 1: enable
13	R/W	0x1	ADAP_LHPF_EN. Left HPF enable 0: disable 1: enable
12	R/W	0x1	ADAP_LNOI_DET. Left Noise detect enable 0: disable 1: enable
11:10	/	/	/
9:8	R/W	0x0	ADAP_LCHAN_HYS. Left Hysteresis setting 00 : 1dB 01 : 2dB 10 : 4dB 11 : disable
7:4	R/W	0x0	ADAP_LNOI_DEB. Left Noise debounce time 0000:0/fs 0001:4/fs 0010:8/fs ---------- 1111 :16*4096/fs $T=2^{(N+1)}$/fs ,except N=0
3:0	R/W	0x0	ADAP_LSIG_DEB. Left Signal debounce time 0000:0/fs 0001:4/fs 0010:8/fs ---------- 1111 :16*4096/fs $T=2^{(N+1)}$/fs ,except N=0

4.3.8.19. ADC DAP Right Control Register

Offset: 0x78			Register Name: AC_ADC_DAP_RCTR_REG
Bit	R/W	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x1F (-86dB)	ADAP_RNOI_SET. Right channel noise threshold setting 0x00 : -24dB 0x01 : -26dB 0x02 : -28dB ----------

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0x1D: -82dB 0x1E: -84dB 0x1F: -86dB
15	/	/	/
14	R/W	0x1	AAGC_RCHAN_EN. Right AGC enable 0:disable 1:enable
13	R/W	0x1	ADAP_RHPF_EN. Right HPF enable 0: disable 1: enable
12	R/W	0x1	ADAP_RNOI_DET. Right Noise detect enable 0: disable 1:enable
11:10	/	/	/
9:8	R/W	0x0	ADAP_RCHAN_HYS. Right Hysteresis setting 00 : 1dB 01 : 2dB 10 : 4dB 11 : disable;
7:4	R/W	0x0	ADAP_RNOI_DEB. Right Noise debounce time 0000:0/fs 0001:4/fs 0010:8/fs ---------- 1111：16*4096/fs $T=2^{(N+1)}$/fs ,except N=0
3:0	R/W	0x0	ADAP_RSIG_DEB. Right Signal debounce time 0000:0/fs 0001:4/fs 0010:8/fs ---------- 1111：16*4096/fs $T=2^{(N+1)}$/fs ,except N=0

4.3.8.20. ADC DAP Parameter Register

Offset: 0x7C			Register Name: AC_ADC_DAP_PARA_REG
Bit	R/W	Default/Hex	Description
31:30	/	/	/
29:24	R/W	0x2C	ADAP_LTARG_SET.

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Left channel target level setting (-1dB -- -30dB). (6.0format 2s component)
23:22	/	/	/
21:16	R/W	0x2C	ADAP_RTARG_SET. Right channel target level setting (-1dB -- -30dB). (6.0format 2s component)
15:8	R/W	0x28	ADAP_LGAIN_MAX. Left channel max gain setting (0-40dB). (7.1format 2s component)
7:0	R/W	0x28	ADAP_RGAIN_MAX. Right channel max gain setting (0-40dB). (7.1format 2s component)

4.3.8.21. ADC DAP Left Average Coef Register

Offset: 0x80			Register Name: AC_ADC_DAP_LAC_REG
Bit	R/W	Default/Hex	Description
31:27	/	/	/
26:0	R/W	0x0051EB8	ADAP_LAC. Average level coefficient setting(3.24format 2s component)

4.3.8.22. ADC DAP Left Decay & Attack Time Register

Offset: 0x84			Register Name: AC_ADC_DAP_LDAT_REG
Bit	R/W	Default/Hex	Description
31	/	/	/
30:16	R/W	0x0000	ADAP_LATT_SET Left attack time coefficient setting 0000 : 1x32/fs 0001 : 2x32/fs ---------- 7FFF : 2^{15} x32/fs T=(n+1)*32*fs When the gain decreases, the actual gain will decrease 0.5dB at every attack time.
15	/	/	/
14:0	R/W	0x001F (32x32fs)	ADAP_LDEC_SET Left decay time coefficient setting 0000 : 1x32/fs 0001 : 2x32/fs ---------- 7FFF : 2^{15} x32/fs T=(n+1)*32/fs When the gain increases, the actual gain will increase 0.5dB at every decay time.

4.3.8.23. ADC DAP Right Average Coef Register

Offset: 0x88			Register Name: AC_ADC_DAP_RAC_REG
Bit	R/W	Default/Hex	Description
31:27	/	/	/
26:0	R/W	0x0051EB8	ADAP_RAC.

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Average level coefficient setting(3.24fomat)

4.3.8.24. ADC DAP Right Decay & Attack Time Register

Offset: 0x8C			Register Name: AC_ADC_DAP_RDAT_REG
Bit	R/W	Default/Hex	Description
31	/	/	/
30:16	R/W	0x0000	ADAP_RATT_SET. Right attack time coefficient setting 0000 : 1x32/fs 0001 : 2x32/fs …… 7FFF : 2^{15} x32/fs T=(n+1)*32/fs When the gain decreases, the actual gain will decrease 0.5dB at every attack time.
15	/	/	/
14:0	R/W	0x001F	ADAP_RDEC_SET Right decay time coefficient setting 0000 : 1x32/fs 0001 : 2x32/fs …….. 7FFF : 2^{15}x32/fs T=(n+1)*32/fs When the gain increases, the actual gain will increase 0.5dB at every decay time.

4.3.8.25. ADC DAP HPF Coef Register

Offset: 0x90			Register Name: AC_ADC_DAP_HPFC_REG
Bit	R/W	Default/Hex	Description
31:27	/	/	/
26:0	R/W	0x0FFFAC1	ADAP_HPFC. HPF coefficient setting (3.24fomat)

4.3.8.26. ADC DAP Left Input Signal Low Average Coef Register

Offset: 0x94			Register Name: AC_ADC_DAP_LINAC_REG
Bit	R/W	Default/Hex	Description
31:27	/	/	/
26:0	R/W	0x0051EB8	ADAP_LINAC Left input signal average filter coefficient to check noise or not (the coefficients 3.24 format 2s complement) always the same as the left output signal average filter's

4.3.8.27. ADC DAP Right Input Signal Low Average Coef Register

Offset: 0x98			Register Name: AC_ADC_DAP_RNAC_REG
Bit	R/W	Default/Hex	Description

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

31:27	/	/	/
26:0	R/W	0x0051EB8	ADAP_RINAC Right input signal average filter coefficient to check noise or not (the coefficients 3.24 format 2s complement) always the same as the left output signal average filter's

4.3.8.28. ADC DAP Optimum Register

Offset: 0x9C			Register Name: AC_ADC_DAP_OPT_REG
Bit	R/W	Default/Hex	Description
31:11	/	/	/
10	R/W	0	Left energy default value setting(include the input and output) 0 : min 1 : max
9 :8	R/W	00	Left channel gain hysteresis setting. The different between target level and the signal level must larger than the hysteresis when the gain change. 00 : 0.4375db 01 : 0.9375db 10 : 1.9375db 11 : 3db
7:6	/	/	/
5	R/W	0	The input signal average filter coefficient setting 0 : is the reg94/reg98 1 : is the reg80/reg88;
4	R/W	0	AGC output when the channel in noise state 0 : output is zero 1 : output is the input data
3	/	/	/
2	R/W	0	Right energy default value setting(include the input and output) 0 : min; 1 : max
1 :0	R/W	00	Right channel gain hysteresis setting. The different between target level and the signal level must larger than the hysteresis when the gain changes. 00 : 0.4375db 01 : 0.9375db 10 : 1.9375db 11 : 3db

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

Chapter 5. Display

This chapter describes the F1C200s display system from following perspectives:

- TCON
- Display Engine Front-End
- Display Engine Back-End
- De-interlacer

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

5.1. TCON

5.1.1. Overview

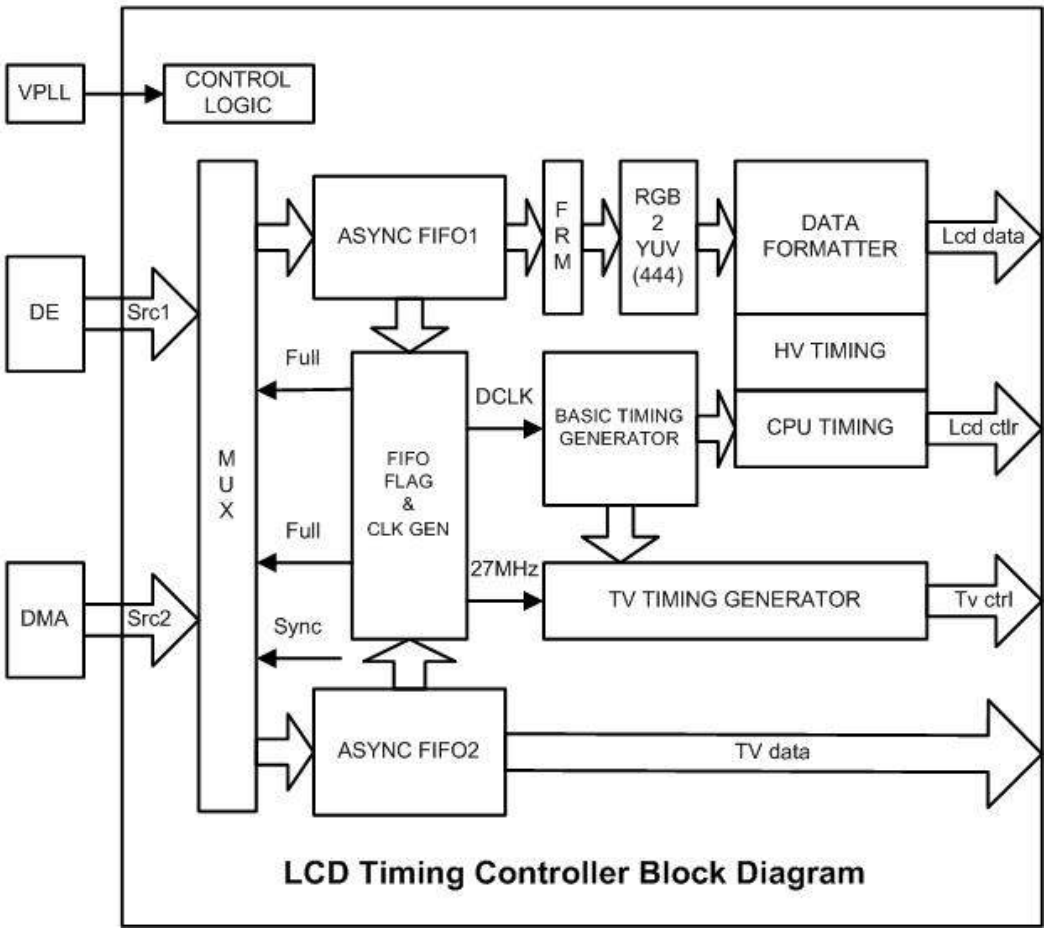
The TCON module is timing controller of display output interface. TCON0 control LCD timing, output LCD signal and data to IO. TCON1 control TV timing, output TV control signal and data to TVE module.

5.1.2. Feature

- Support RGB interface with DE/SYNC mode, up to 1280x720@60fps
- Support serial RGB/CCIR656 interface, up to 720x576@60fps
- Support i80 interface with 18/16/9/8 bit, up to 800x480@60fps
- Support pixel format: RGB888, RGB666 and RGB565
- LCD dither function, support RGB666/RGB565 interface

5.1.3. Block Diagram

5.1.3.1. LCD Timing Controller



LCD Timing Controller Block Diagram

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

5.1.4. TCON Register List

Module Name	Base Address
TCON	0x01C0C000

Register Name	Offset	Description
TCON_CTRL_REG	0x000	TCON Control Register
TCON_INT_REG0	0x004	TCON Interrupt Register 0
TCON_INT_REG1	0x008	TCON Interrupt Register 1
TCON_FRM_CTRL_REG	0x010	TCON FRM Control Register
TCON_FRM_SEED0_R_REG	0x014	TCON FRM Seed0 Red Register
TCON_FRM_SEED0_G_REG	0x018	TCON FRM Seed0 Green Register
TCON_FRM_SEED0_B_REG	0x01C	TCON FRM Seed0 Blue Register
TCON_FRM_SEED1_R_REG	0x020	TCON FRM Seed1 Red Register
TCON_FRM_SEED1_G_REG	0x024	TCON FRM Seed1 Green Register
TCON_FRM_SEED1_B_REG	0x028	TCON FRM Seed1 Blue Register
TCON_FRM_TBL_REG0	0x02C	TCON FRM Table Register 0
TCON_FRM_TBL_REG1	0x030	TCON FRM Table Register 1
TCON_FRM_TBL_REG2	0x034	TCON FRM Table Register 2
TCON_FRM_TBL_REG3	0x038	TCON FRM Table Register 3
TCON0_CTRL_REG	0x040	TCON0 Control Register
TCON_CLK_CTRL_REG	0x044	TCON Clock Control Register
TCON0_BASIC_TIMING_REG0	0x048	TCON0 Basic Timing Register 0
TCON0_BASIC_TIMING _REG1	0x04C	TCON0 Basic Timing Register 1
TCON0_BASIC_TIMING _REG2	0x050	TCON0 Basic Timing Register 2
TCON0_BASIC_TIMING _REG3	0x054	TCON0 Basic Timing Register 3
TCON0_HV_TIMING_REG	0x058	TCON0 HV Timing Register
TCON0_ CPU_IF_REG	0X060	TCON0 CPU Interface Control Register
TCON0_CPU_WR_REG	0x064	TCON0 CPU Mode Write Register
TCON0_CPU_RD_REG	0x068	TCON0 CPU Mode Read Register
TCON0_CPU_RD_NX_REG	0x06C	TCON0 CPU Mode Read NX Register
TCON0_IO_CTRL_REG0	0x088	TCON0 IO Control Register 0
TCON0_IO_CTRL_REG1	0x08C	TCON0 IO Control Register 1
TCON1_CTRL_REG	0x090	TCON1 Control Register
TCON1_BASIC_REG0	0x094	TCON1 Basic Timing Register 0
TCON1_BASIC_REG1	0x098	TCON1 Basic Timing Register 1
TCON1_BASIC_REG2	0x09C	TCON1 Basic Timing Register 2
TCON1_BASIC_REG3	0x0A0	TCON1 Basic Timing Register 3
TCON1_BASIC_REG4	0x0A4	TCON1 Basic Timing Register 4
TCON1_BASIC_REG5	0x0A8	TCON1 Basic Timing Register 5
TCON1_IO_CTRL_REG0	0x0F0	TCON1 IO Control Register 0
TCON1_IO_CTRL_REG1	0x0F4	TCON1 IO Control Register 1
TCON_DEBUG_INFO_REG	0x0FC	TCON Debug Information Register

Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

5.1.5. TCON Register Description

5.1.5.1. TCON Control Register

Offset: 0x000			Register Name: TCON_CTRL_REG
Bit	R/W	Default/Hex	Description
31	R/W	0	MODULE_EN: the whole module enable flag 0: disable 1: enable When it's disabled, the module will be reset to idle state.
30:1	/	/	/
0	R/W	0	IO_MAP_SEL: 0: TCON0 1: TCON1 Note: this bit determined which IO_INV/IO_TRI is valid. This function has deleted in this version.

5.1.5.2. TCON Interrupt Register 0

Offset: 0x004			Register Name: TCON_INT_REG0
Bit	R/W	Default/Hex	Description
31	R/W	0	VBIE_TCON0: TCON0 vertical blanking interrupt Enable 0: disable 1: enable
30	R/W	0	VBIE_TCON1: TCON1 vertical blanking interrupt Enable 0: disable 1: enable
29	R/W	0	LINE_TRG0IE: TCON0 line trigger interrupt enable 0: disable 1: enable
28	R/W	0	LINE_TRG1IE: TCON1 line trigger interrupt enable 0: disable 1: enable
27:16	/	/	/
15	R/W	0	VBI_TCON0: TCON0 vertical blanking interrupt Asserted during vertical no-display period every frame. Write 0 to clear it.
14	R/W	0	VBI_TCON1: TCON1 vertical blanking interrupt Asserted during vertical no-display period every frame. Write 0 to clear it.
13	R/W	0	LINE_TRG0: trigger when SY0 match the current TCON0 scan line Write 0 to clear it.
12	R/W	0	LINE_TRG1: trigger when SY1 match the current TCON1 scan line Write 0 to clear it.
11:0	/	/	/

Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

5.1.5.3. TCON Interrupt Register 1

Offset: 0x008			Register Name: TCON_INT_REG1
Bit	R/W	Default/Hex	Description
31:27	/	/	/
26:16	R/W	0	SY0: scan line for TCON0 line trigger(including inactive lines) Setting it for the specified line for trigger0. Note: SY0 is writable only when LINE_TRG0 disable.
15:11	/	/	/
10:0	R/W	0	SY1: scan line for TCON1 line trigger(including inactive lines) Setting it for the specified line for trigger 1. Note: SY1 is writable only when LINE_TRG1 disable.

5.1.5.4. TCON FRM Control Register

Offset: 0x010			Register Name: TCON_FRM_CTRL_REG
Bit	R/W	Default/Hex	Description
31	R/W	0	TCON0_FRM_EN 0:disable 1:enable
30:7	/	/	/
6	R/W	0	TCON0_FRM_MODE_r 0: 6bit frm output 1: 5bit frm output
5	R/W	0	TCON0_FRM_MODE_g 0: 6bit frm output 1: 5bit frm output
4	R/W	0	TCON0_FRM_MODE_b 0: 6bit frm output 1: 5bit frm output
1:0	R/W	0	FRM_TEST_MODE 00: FRM 01: half 5/6bit, half FRM 10: half 8bit, half FRM 11: half 8bit, half 5/6bit

5.1.5.5. TCON FRM Seed0 Red Register

Offset: 0x014			Register Name: TCON_FRM_SEED0_R_REG
Bit	R/W	Default/Hex	Description
31:25	/	/	/
24:0	R/W	0	SEED_R_VALUE0 Note: avoid set it to 0

5.1.5.6. TCON FRM Seed0 Green Register

Offset: 0x018			Register Name: TCON_FRM_SEED0_G_REG
Bit	R/W	Default/Hex	Description
31:25	/	/	/

Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

24:0	R/W	0	SEED_G_VALUE0 Note: avoid set it to 0

5.1.5.7. TCON FRM Seed0 Blue Register

Offset: 0x01C			Register Name: TCON_FRM_SEED0_B_REG
Bit	R/W	Default/Hex	Description
31:25	/	/	/
24:0	R/W	0	SEED_B_VALUE0 Note: avoid set it to 0

5.1.5.8. TCON FRM Seed1 Red Register

Offset: 0x020			Register Name: TCON_FRM_SEED1_R_REG
Bit	R/W	Default/Hex	Description
31:13	/	/	/
12:0	R/W	0	SEED_R_VALUE1 Note: avoid set it to 0

5.1.5.9. TCON FRM Seed1 Green Register

Offset: 0x024			Register Name: TCON_FRM_SEED1_G_REG
Bit	R/W	Default/Hex	Description
31:13	/	/	/
12:0	R/W	0	SEED_G_VALUE1 Note: avoid set it to 0

5.1.5.10. TCON FRM Seed1 Blue Register

Offset: 0x028			Register Name: TCON_FRM_SEED1_B_REG
Bit	R/W	Default/Hex	Description
31:13	/	/	/
12:0	R/W	0	SEED_B_VALUE1 Note: avoid set it to 0

5.1.5.11. TCON FRM Table Register 0

Offset: 0x02C			Register Name: TCON_FRM_TBL_REG0
Bit	R/W	Default/Hex	Description
31:0	R/W	0	FRM_TBL_VALUE0 Note: Recommend set as 0x01010000

5.1.5.12. TCON FRM Table Register 1

Offset: 0x030			Register Name: TCON_FRM_TBL_REG1
Bit	R/W	Default/Hex	Description
31:0	R/W	0	FRM_TBL_VALUE1 Note: Recommend set as 0x15151111

Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

5.1.5.13. TCON FRM Table Register 2

Offset: 0x034			Register Name: TCON_FRM_TBL_REG2
Bit	R/W	Default/Hex	Description
31:0	R/W	0	FRM_TBL_VALUE2 Note: Recommend set as 0x57575555

5.1.5.14. TCON FRM Table Register 3

Offset: 0x038			Register Name: TCON_FRM_TBL_REG3
Bit	R/W	Default/Hex	Description
31:0	R/W	0	FRM_TBL_VALUE3 Note: Recommend set as 0x7F7F7777

5.1.5.15. TCON0 Control Register

Offset: 0x040			Register Name: TCON0_CTRL_REG
Bit	R/W	Default/Hex	Description
31	R/W	0	TCON0_EN: TCON0 timing generator enable 0: disable 1: enable Note: It executes at the beginning of the first blank line of TCON0 timing.
30:27	/	/	/
26:24	R/W	0	I/F: panel interface type select 00: HV(Sync+DE) 01: 8080 I/F 1x: reserved
23	R/W	0	SWAP: TCON0 data manipulation 0: default 1: swap RED and BLUE data at FIFO1
22	R/W	0	WHITE_DATA: white data 0:all 0s 1:all 1s
21	R/W	0	FIFO1_RST Write 1 and then 0 at this bit will reset FIFO 1 Note: 1 holding time must more than 1 DCLK
20	R/W	0	Interlace_EN 0:disable 1:enable NOTE: this flag is valid only when TCON0_EN = 1
19:9	/	/	/
8:4	R/W	0	TCON0_STA_DLY STA delay NOTE: valid only when TCON0_EN = 1
3:2	/	/	/
1:0	R/W	0	TCON0_SRC_SEL: TCON0 data source select 00: DE CH1(FIFO1 enable) 01: reserved

Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			10: DMA 565 input(FIFO1 enable) 11: white data(FIFO1 disable) Note: 1) These bits are sampled only at the beginning of the first blank line of TCON0 timing. 2) Generally, when input source is changed, it would change at the beginning of the first blank line of TCON0 timing. 3) When FIFO1 and FIFO2 select the same source and FIFO2 is enabled, it executes at the beginning of the first blank line of TV timing. Also, TCON0 timing generator will reset to the beginning of the first blank line.

5.1.5.16. TCON Clock Control Register

Offset: 0x044			Register Name: TCON_CLK_CTRL_REG
Bit	R/W	Default/Hex	Description

31	R/W	0	LCLK_EN[3:0]: TCON0 clock enable
			4'h0, 4'h4,4'h6,4'ha7:dclk_en=0;dclk1_en=0;dclk2_en=0;dclkm2_en=0;
			4'h1: dclk_en = 1; dclk1_en = 0; dclk2_en = 0; dclkm2_en = 0;
			4'h2: dclk_en = 1; dclk1_en = 0; dclk2_en = 0; dclkm2_en = 1;
			4'h3: dclk_en = 1; dclk1_en = 1; dclk2_en = 0; dclkm2_en = 0;
			4'h5: dclk_en = 1; dclk1_en = 0; dclk2_en = 1; dclkm2_en = 0;
			4'h8,4'h9,4'ha,4'hb,4'hc,4'hd,4'he,4'hf:
			dclk_en = 1;
			dclk1_en = 1;
			dclk2_en = 1;
			dclkm2_en = 1;

30:8	/	/	/
7:0	R/W	0	DCLKDIV: dot clock divider Tdclk = Tsclk * DCLKDIV Note: 1.if dclk1&dclk2 used，5<DCLKDIV <96 2.if dclk only， DCLKDIV >=4 || DCLKDIV=2

5.1.5.17. TCON0 Basic Timing Register 0

Offset: 0x048			Register Name: TCON0_BASIC_TIMING_REG0
Bit	R/W	Default/Hex	Description
31:27	/	/	/
26:16	R/W	0	TCON0_X: screen width (in pixels) Panel width is X+1
15:11	/	/	/
10:0	R/W	0	TCON0_Y: screen height (in pixels) Panel height is Y+1

5.1.5.18. TCON0 Basic Timing Register 1

Offset: 0x04C			Register Name: TCON0_BASIC_TIMING_REG1
Bit	R/W	Default/Hex	Description

Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

31:28	/	/	/
27:16	R/W	0	HT: horizontal total time (in dclk) Thcycle = (HT+1) * Tdclk Note:1) parallel :HT >= (HBP +1) + (X+1) +2 2) serial 1: HT >= (HBP +1) + (X+1) *3+2 3) serial 2: HT >= (HBP +1) + (X+1) *3/2+2
15:10	/	/	/
9:0	R/W	0	HBP: horizontal back porch (in dclk) Thbp = (HBP +1) * Tdclk

5.1.5.19. TCON0 Basic Timing Register 2

Offset: 0x050			Register Name: TCON0_BASIC_TIMING_REG2
Bit	R/W	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0	VT: vertical front porch (in lines) TVT = (VT)/2 * Thsync Note: VT/2 >= (VBP+1) + (Y+1) +2
15:10	/	/	/
9:0	R/W	0	VBP: vertical back porch (in lines) Tvbp = (VBP +1) * Thsync

5.1.5.20. TCON0 Basic Timing Register 3

Offset: 0x054			Register Name: TCON0_BASIC_TIMING_REG3
Bit	R/W	Default/Hex	Description
31:22	/	/	/
25:16	R/W	0	HSPW: horizontal Sync Pulse Width (in dclk) Thspw = (HSPW+1) * Tdclk Note: HT> (HSPW+1)
15:10	/	/	/
5:0	R/W	0	VSPW: vertical Sync Pulse Width (in lines) Tvspw = (VSPW+1) * Thsync Note: VT/2 > (VSPW+1)

Note: Thsync: horizontal sync signal cycle time.

5.1.5.21. TCON0 HV Timing Register

Offset: 0x058			Register Name: TCON0_HV_TIMING_REG
Bit	R/W	Default/Hex	Description
31	R/W	0	HV_MOD: HV I/F mode select 0: 24bit parallel mode 1: 8bit serial mode
30	R/W	0	SERIAL_MOD: SERIAL I/F mode select 0: 8bit/3cycle RGB serial mode(RGB888) 1: 8bit/2cycle YUV serial mode(CCIR656)
29:28	/	/	/
27:26	R/W	0	RGB888_SM0: serial RGB888 mode Output sequence at odd lines of the panel

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			(line 1, 3, 5, 7…) 00: R→G→B 01: B→R→G 10: G→B→R 11: R→G→B
25:24	R/W	0	RGB888_SM1: serial RGB888 mode Output sequence at even lines of the panel (line 2, 4, 6, 8…) 00: R→G→B 01: B→R→G 10: G→B→R 11: R→G→B
23:22	R/W	0	YUV_SM: serial YUV mode Output sequence 2-pixel-pair of every scan line 00: YUYV 01: YVYU 10: UYVY 11: VYUY
21:20	R/W	0	YUV EAV/SAV F line delay 0:F toggle right after active video line 1:delay 2 line(CCIR NTSC) 2:delay 3 line(CCIR PAL) 3:reserved
19：0	/	/	/

5.1.5.22. TCON0 CPU Interface Control Register

Offset: 0x060			Register Name: TCON0_CPU_IF_CTRL_REG
Bit	R/W	Default/Hex	Description
31:29	R/W	0	CPU_MOD: CPU interface mode: 000: 18bit/256K mode 001: 16bit mode0 010: 16bit mode1 011: 16bit mode2 100: 16bit mode3 101: 9bit mode 110: 8bit 256K mode 111: 8bit 65K mode
28	R/W	0	AUTO: auto Transfer Mode: If it's 1, all the valid data during this frame are write to panel. Note: This bit is sampled by Vsync
27	R/W	0	FLUSH: direct transfer mode: If it's enabled, FIFO1 is regardless of the HV timing, pixels data keep being transferred unless the input FIFO was empty. Data output rate control by DCLK.
26	R/W	0	DA: pin A1 value in 8080 mode auto/flash states
25	R/W	0	CA: pin A1 value in 8080 mode WR/RD execute
24	R/W	0	VSYNC_CS_SEL

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0:CS 1:VSYNC
23	R	0	WR: 0:write operation is finishing 1:write operation is pending
22	R	0	RD: 0:read operation is finishing 1:read operation is pending
21:0	/	/	/

Note:

1. Write cycle = Tdclk
2. All bits except **CPU_MOD** can be real-time changed.
3. Software has to make sure **AUTO, FLUSH, WR** or **RD** won't happen at the same time, If they do, priority is **AUTO > FLUSH> WR> RD**.
4. Priority : CA >DA

5.1.5.23. TCON0 CPU Write Register

Offset: 0x064			Register Name: TCON0_CPU_WR_REG
Bit	R/W	Default/Hex	Description
31:24	/	/	/
23:0	W	/	Write data on 8080 bus

5.1.5.24. TCON0 CPU Read Register

Offset: 0x068			Register Name: TCON0_CPU_RD_REG
Bit	R/W	Default/Hex	Description
31:24	/	/	/
23:0	W	/	Read back data and launch a new read operation on 8080 bus.

5.1.5.25. TCON0 CPU Read NX Register

Offset: 0x068			Register Name: TCON0_CPU_RD_NX_REG
Bit	R/W	Default/Hex	Description
31:24	/	/	/
23:0	W	/	Read back data without a read operation on 8080 bus.

5.1.5.26. TCON0 IO Control Register 0

Offset: 0x088			Register Name: TCON0_IO_CTRL_REG0
Bit	R/W	Default/Hex	Description
31:28	R/W	0	DCLK_SEL[1:0] 00: used DCLK0(normal phase offset) 01: used DCLK1(1/3 phase offset) 10: used DCLK2(2/3 phase offset) 11: reserved
27	R/W	0	IO3_INV 0: not invert 1: invert

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

26	R/W	0	IO2 INV 0: not invert 1: invert
25	R/W	0	IO1_INV 0: not invert 1: invert
24	R/W	0	IO0_INV 0: not invert 1: invert
23:0	R/W	0	D[23:0]_INV:TCON0 output port D[23:0] polarity control, with independent bit control: 0s: normal polarity 1s: invert the specify output

Note: This register can be real-time changed, and work immediately.

5.1.5.27. TCON0 IO Control Register 1

Offset: 0x08C			Register Name: TCON0_IO_CTRL_REG1
Bit	R/W	Default/Hex	Description
31:28	/	/	/
27	R/W	1	IO3_OUTPUT_TRI_EN 1: disable 0: enable
26	R/W	1	IO2 OUTPUT_ TRI_EN 1: disable 0: enable
25	R/W	1	IO1_ OUTPUT_ TRI_EN 1: disable 0: enable
24	R/W	1	IO0_ OUTPUT_ TRI_EN 1: disable 0: enable
27:0	R/W	0xFFFFFF	D[23:0]_OUTPUT_ TRI_EN: TCON0 output port D[23:0] output enable, with independent bit control: 1s: disable 0s: enable

Note: This register can be real-time changed, and work immediately.

5.1.5.28. TCON1 Control Register

Offset: 0x090			Register Name: TCON1_CTRL_REG
Bit	R/W	Default/Hex	Description
31	R/W	0	TCON1_EN:TCON1 mode enable 0: disable 1: enable
30:21	/	/	/
20	R/W	0	Interlace_EN

Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0:disable 1:enable NOTE: this flag is valid only when TCON1_EN == 1
19:9	/	/	/
8:4	R/W	0	STA_DLY[4:0](for DE1 and DE2) STA delay NOTE: this flag is valid only when TCON1_EN == 1
3:2	/	/	/
1:0	R/W	0	TCON1_SRC_SEL: TCON1 data source select 00: DE CH1(FIFO2 enable) 01: reserved 1x: BLUE data(FIFO2 disable, RGB=0000FF)

5.1.5.29. TCON1 Basic Timing Register 0

Offset: 0x094			Register Name: TCON1_BASIC_TIMING_REG0
Bit	R/W	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0	TCON1_XI: TCON1 source width (in pixels) source width is X+1
15:12	/	/	/
11:0	R/W	0	TCON1_YI: TCON1 source height (in pixels) source height is Y+1

5.1.5.30. TCON1 Basic Timing Register 1

Offset: 0x098			Register Name: TCON1_BASIC_TIMING_REG1
Bit	R/W	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0	LS_XO: line scale output size width is LS_XO+1
15:12	/	/	/
11:0	R/W	0	LS_YO: line scale output size width is LS_YO+1 NOTE: this version LS_YO = TCON1_YI

5.1.5.31. TCON1 Basic Timing Register 2

Offset: 0x09C			Register Name: TCON1_BASIC_TIMING_REG2
Bit	R/W	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0	TCON1_XO: TCON1 output width (in pixels) width is TCON1_XO+1
15:12	/	/	/
11:0	R/W	0	TCON1_YO: TCON1 output height (in pixels) height is TCON1_YO+1

Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

5.1.5.32. TCON1 Basic Timing Register 3

Offset: 0x0A0			Register Name: TCON1_BASIC_TIMING_REG3
Bit	R/W	Default/Hex	Description
31:28	/	/	/
28:16	R/W	0	HT: horizontal total time Thcycle = (HT+1) * Thdclk
15:12	/	/	/
11:0	R/W	0	HBP: horizontal back porch Thbp = (HBP +1) * Thdclk

5.1.5.33. TCON1 Basic Timing Register 4

Offset: 0x0A4			Register Name: TCON1_BASIC_TIMING_REG4
Bit	R/W	Default/Hex	Description
31:28	/	/	/
28:16	R/W	0	VT: horizontal total time (in HD line) Tvt = VT/2 * Th
15:12	/	/	/
11:0	R/W	0	VBP: horizontal back porch (in HD line) Tvbp = (VBP +1) * Th

5.1.5.34. TCON1 Basic Timing Register 5

Offset: 0x0A8			Register Name: TCON1_BASIC_TIMING_REG5
Bit	R/W	Default/Hex	Description
31:26	/	/	/
25:16	R/W	0	HSPW: horizontal Sync Pulse Width (in dclk) Thspw = (HSPW+1) * Tdclk Note: HT> (HSPW+1)
15:10	/	/	/
9:0	R/W	0	VSPW: vertical Sync Pulse Width (in lines) Tvspw = (VSPW+1) * Th Note: VT/2 > (VSPW+1)

5.1.5.35. TCON1 IO Control Register 0

Offset: 0x0F0			Register Name: TCON1_IO_CTRL_REG0
Bit	R/W	Default/Hex	Description
31:28	/	/	/
27	R/W	0	IO3_INV 0: not invert 1: invert
26	R/W	0	IO2 INV 0: not invert 1: invert
25	R/W	0	IO1_INV 0: not invert 1: invert

Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

24	R/W	0	IO0_INV 0: not invert 1: invert
23:0	R/W	0	D[23:0]_INV:TCON1 output port D[23:0] polarity control, with independent bit control: 0s: normal polarity 1s: invert the specify output

Note: This register can be real-time changed, and work immediately.

5.1.5.36. TCON1 IO Control Register 1

Offset: 0x0F4			Register Name: TCON1_IO_CTRL_REG1
Bit	R/W	Default/Hex	Description
31:28	/	/	/
27	R/W	1	IO3_OUTPUT_TRI_EN 1: disable 0: enable
26	R/W	1	IO2 OUTPUT_ TRI_EN 1: disable 0: enable
25	R/W	1	IO1_ OUTPUT_ TRI_EN 1: disable 0: enable
24	R/W	1	IO0_ OUTPUT_ TRI_EN 1: disable 0: enable
27:0	R/W	0xFFFFFF	D[23:0]_OUTPUT_ TRI_EN: TCON1 output port D[23:0] output enable, with independent bit control: 1s: disable 0s: enable

Note: This register can be real-time changed, and work immediately.

5.1.5.37. TCON Debug Information Register

Offset: 0x0FC			Register Name: TCON_DEBUG_INFO_REG
Bit	R/W	Default/Hex	Description
31	R/W	/	TCON0_FIFO_UNDER_FLOW
30	R/W	/	TCON1_FIFO_UNDER_FLOW
29	R	1	TCON0_Field_POL 0: second field 1: first field
28	R	1	TCON1_Field_POL 0: second field 1: first field
27:26	/	/	/
25:16	R	/	TCON0_CURRENT_LINE
15:13	/	/	/

Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

12:0	R	/	TCON1_CURRENT_LINE

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

5.2. Display Engine Front-End

5.2.1. Overview

The display engine front-end (DEFE) provides image resizing function for display engine. It receives data from DRAM, performs the image resizing function, and outputs to DEBE module or DRAM.

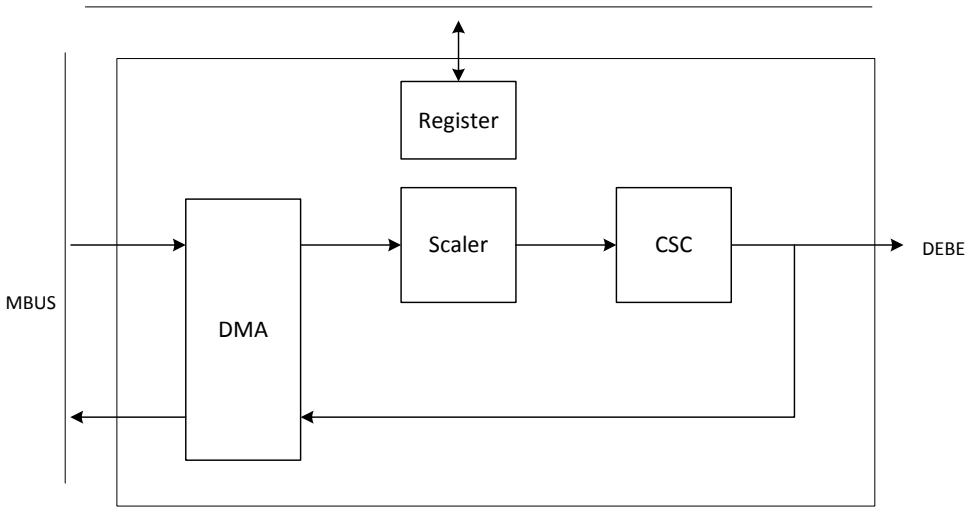
The DEFE can receive ARGB/YUV420/YUV422/YUV411 data format, and then converts to ARGB8888 for display, or write-back other format to DRAM. Horizontal and vertical direction scaling are implemented independently.

5.2.2. Feature

The DEFE includes the following features:

- Support YUV444/ YUV422/ YUV420/ YUV411/ ARGB8888 data format
- Support 1/16× to 32× resize ratio
- Support 32-phase 4-tap horizontal anti-alias filter, 32-phase 4-tap vertical anti-alias filter
- Support input size up to 2048×2048
- Support output size up 1280x1280
- Support direct display or write back to memory

5.2.3. Block Diagram



DEFE block diagram

5.2.4. DEFE Register List

Module Name	Base Address
DEFE	0x01E00000

Register Name	Offset	Description
DEFE_EN_REG	0x0000	DEFE Module Enable Register

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

DEFE_FRM_CTRL_REG	0x0004	DEFE Frame Process Control Register
DEFE_BYPASS_REG	0x0008	DEFE CSC Bypass Register
DEFE_AGTH_SEL_REG	0x000C	DEFE Algorithm Selection Register
DEFE_LINT_CTRL_REG	0x0010	DEFE Line Interrupt Control Register
DEFE_BUF_ADDR0_REG	0x0020	DEFE Input Channel 0 Buffer Address Register
DEFE_BUF_ADDR1_REG	0x0024	DEFE Input Channel 1 Buffer Address Register
DEFE_BUF_ADDR2_REG	0x0028	DEFE Input Channel 2 Buffer Address Register
DEFE_FIELD_CTRL_REG	0x002C	DEFE Field Sequence Register
DEFE_TB_OFF0_REG	0x0030	DEFE Channel 0 Tile Based Offset Register
DEFE_TB_OFF1_REG	0x0034	DEFE Channel 1 Tile Based Offset Register
DEFE_TB_OFF2_REG	0x0038	DEFE Channel 2 Tile Based Offset Register
DEFE_LINESTRD0_REG	0x0040	DEFE Channel 0 Line Stride Register
DEFE_LINESTRD1_REG	0x0044	DEFE Channel 1 Line Stride Register
DEFE_LINESTRD2_REG	0x0048	DEFE Channel 2 Line Stride Register
DEFE_INPUT_FMT_REG	0x004C	DEFE Input Format Register
DEFE_WB_ADDR_REG	0x0050	DEFE Write Back Address Register
DEFE_OUTPUT_FMT_REG	0x005C	DEFE Output Format Register
DEFE_INT_EN_REG	0x0060	DEFE Interrupt Enable Register
DEFE_INT_STATUS_REG	0x0064	DEFE Interrupt Status Register
DEFE_STATUS_REG	0x0068	DEFE Status Register
DEFE_CSC_COEF00_REG	0x0070	DEFE CSC Coefficient 00 Register
DEFE_CSC_COEF01_REG	0x0074	DEFE CSC Coefficient 01 Register
DEFE_CSC_COEF02_REG	0x0078	DEFE CSC Coefficient 02 Register
DEFE_CSC_COEF03_REG	0x007C	DEFE CSC Coefficient 03 Register
DEFE_CSC_COEF10_REG	0x0080	DEFE CSC Coefficient 10 Register
DEFE_CSC_COEF11_REG	0x0084	DEFE CSC Coefficient 11 Register
DEFE_CSC_COEF12_REG	0x0088	DEFE CSC Coefficient 12 Register
DEFE_CSC_COEF13_REG	0x008C	DEFE CSC Coefficient 13 Register
DEFE_CSC_COEF20_REG	0x0090	DEFE CSC Coefficient 20 Register
DEFE_CSC_COEF21_REG	0x0094	DEFE CSC Coefficient 21 Register
DEFE_CSC_COEF22_REG	0x0098	DEFE CSC Coefficient 22 Register
DEFE_CSC_COEF23_REG	0x009C	DEFE CSC Coefficient 23 Register
DEFE_INSIZE_REG	0x0100	DEFE Input Size Register
DEFE_OUTSIZE_REG	0x0104	DEFE Output Size Register
DEFE_HORZFACT_REG	0x0108	DEFE Horizontal Factor Register
DEFE_VERTFACT_REG	0x010C	DEFE Vertical factor Register
DEFE_CH0_HORZCOEF_REGN	0x0400+N*4	DEFE Channel 0 Horizontal Filter Coefficient Register N=0~31
DEFE_CH0_VERTCOEF_REGN	0x0500+N*4	DEFE Channel 0 Vertical Filter Coefficient Register N=0~31
DEFE_CH1_HORZCOEF_REGN	0x0600+N*4	DEFE Channel 1 Horizontal Filter Coefficient Register N=0~31
DEFE_CH1_VERTCOEF_REGN	0x0700+N*4	DEFE Channel 1 Vertical Filter Coefficient Register N=0~31

Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

Note: Registers 0x0008~0x010F except status registers are double buffered. When a new frame process starts and the buffered register configuration ready bit in frame process control register is set, the value of corresponding internal configuration register will be refreshed by this register, the programmer always can't read the value of corresponding internal register.

5.2.5. DEFE Register Description

5.2.5.1. DEFE Module Enable Register

Offset: 0x0000			Register Name: DEFE_EN_REG
Bit	R/W	Default/Hex	Description
31	R/W	0x1	BIST_EN Bist enable for cpu 0: Disable cpu accessing ram, mux ram to DEFE 1: Enable cpu accessing ram, mux ram to cpu Normally, set to 0 when using DEFE
30:1	/	/	/
0	R/W	0x0	EN DEFE enable 0: Disable 1: Enable When DEFE enable bit is disabled, the clock of DEFE module will be disabled If this bit is transition from 0 to 1, the frame process control register and the interrupt enable register will be initialed to default value, and the state machine of the module is reset

5.2.5.2. DEFE Frame Process Control Register

Offset: 0x0004			Register Name: DEFE_FRM_CTRL_REG
Bit	R/W	Default/Hex	Description
31:24	/	/	/
23	R/W	0x0	COEF_ACCESS_CTRL Fir coef ram access control 0: cpu don't access fir coef ram 1: cpu will access fir coef ram This bit will be set to 1 before cpu access fir coef ram
22:17	/	/	/
16	R/W	0x0	FRM_START Frame process start & reset control 0: reset 1: start If the bit is written to zero, the whole state machine and data paths of DEFE module will be reset. When the bit is written to 1, DEFE will start a new frame process.
15:12	/	/	/

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

11	R/W	0x0	OUT_CTRL DEFE output control 0: enable DEFE output to image 1: disable DEFE output to image If DEFE write back function is enable, DEFE output to image isn't recommended.
10:3	/	/	/
2	R/W	0x0	WB_EN Write back enable 0: Disable 1: Enable If output to image is enable, the writing back process will start when write back enable bit is set and a new frame processing begins. The bit will be self-cleared when writing-back frame process starts.
1	/	/	/
0	R/W	0x0	REG_RDY_EN Register ready enable 0: not ready 1: registers configuration ready As same as filter coefficients configuration, in order to ensure the display be correct, the correlative display configuration registers are buffered too, the programmer also can change the value of correlative registers in any time. When the registers setting is finished, the programmer should set the bit if the programmer need the new configuration in next scaling frame. When the new frame start, the bit will also be self-cleared.

5.2.5.3. DEFE CSC Bypass Register

Offset: 0x0008			Register Name: DEFE_BYPASS_REG
Bit	R/W	Default/Hex	Description
31:2	/	/	/
1	R/W	0x0	CSC_BYPASS_EN CSC by-pass enable 0: CSC enable 1: CSC will be by-passed Actually, in order ensure the module working be correct, This bit only can be set when input data format is the same as output data format (both YUV or both RGB)
0	R/W	0x0	DEFE_BYPASS_EN scale by-pass control 0: scale enable 1: scale will be by-passed Actually, in order ensure the module working be correct, This bit only can be set when the input size equals to the output size (including all components)

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

5.2.5.4. DEFE Algorithm Selection Register

Offset: 0xC			Register Name: DEFE_AGTH_SEL_REG
Bit	R/W	Default/Hex	Description
31:2	/	/	/
1:0	R/W	0x0	SCAL_AGTH Scaling algorithm selection 00: 4x4 01: 4x2 10: 4x1 11: reverved

5.2.5.5. DEFE Line Interrupt Conrtol Register

Offset: 0x0010			Register Name: DEFE_LINT_CTRL_REG
Bit	R/W	Default/Hex	Description
31:28	/	/	/
27:16	R	0x0	CURRENT_LINE
15	R/W	0x0	FIELD_SEL Field select 0: each field 1: end field(field counter in reg0x2c)
14:13	/	/	/
12:0	R/W	0x0	TRIG_LINE Trigger line number of line interrupt

5.2.5.6. DEFE Input Channel 0 Buffer Address Register

Offset: 0x0020			Register Name: DEFE_BUF_ADDR0_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0x0	BUF_ADDR DEFE frame buffer address In tile-based type: The address is the start address of the line in the first tile used to generating output frame. In non-tile-based type: The address is the start address of the first line.

5.2.5.7. DEFE Input Channel 1 Buffer Address Register

Offset: 0x0024			Register Name: DEFE_BUF_ADDR1_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0x0	BUF_ADDR DEFE frame buffer address In tile-based type: The address is the start address of the line in the first tile used to generating output frame. In non-tile-based type: The address is the start address of the first line.

Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

5.2.5.8. DEFE Input Channel 2 Buffer Address Register

Offset: 0x0028			Register Name: DEFE_BUF_ADDR2_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0x0	BUF_ADDR DEFE frame buffer address In tile-based type: The address is the start address of the line in the first tile used to generating output frame. In non-tile-based type: The address is the start address of the first line.

5.2.5.9. DEFE Field Sequence Register

Offset: 0x002C			Register Name: DEFE_FIELD_CTRL_REG
Bit	R/W	Default/Hex	Description
31:13	/	/	/
12	R/W	0x0	FIELD_LOOP_MOD Field loop mode 0：the last field； 1：the full frame
11	/	/	/
10:8	R/W	0x0	VALID_FIELD_CNT Valid field counter bit the valid value = this value + 1；
7:0	R/W	0x0	FIELD_CNT Field counter each bit specify a field to display，0：top field，1：bottom field

5.2.5.10. DEFE Channel 0 Tile Based Offset Register

Offset: 0x0030			Register Name: DEFE_TB_OFF0_REG
Bit	R/W	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x0	X_OFFSET1 The x offset of the bottom-right point in the end tile
15:13	/	/	/
12:8	R/W	0x0	Y_OFFSET0 The y offset of the top-left point in the first tile
7:5	/	/	/
4:0	R/W	0x0	X_OFFSET0 The x offset of the top-left point in the first tile

5.2.5.11. DEFE Channel 1 Tile Based Offset Register

Offset: 0x0034			Register Name: DEFE_TB_OFF1_REG
Bit	R/W	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x0	X_OFFSET1 The x offset of the bottom-right point in the end tile

Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

15:13	/	/	/
12:8	R/W	0x0	Y_OFFSET0 The y offset of the top-left point in the first tile
7:5	/	/	/
4:0	R/W	0x0	X_OFFSET0 The x offset of the top-left point in the first tile

5.2.5.12. DEFE Channel 2 Tile Based Offset Register

Offset: 0x0038			Register Name: DEFE_TB_OFF2_REG
Bit	R/W	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x0	X_OFFSET1 The x offset of the bottom-right point in the end tile
15:13	/	/	/
12:8	R/W	0x0	Y_OFFSET0 The y offset of the top-left point in the first tile
7:5	/	/	/
4:0	R/W	0x0	X_OFFSET0 The x offset of the top-left point in the first tile

5.2.5.13. DEFE Channel 0 Line Stride Register

Offset: 0x0040			Register Name: DEFE_LINESTRD0_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0x0	LINE_STRIDE **In tile-based type** The stride length is the distance from the start of the end line in one tile to the start of the first line in next tile(here next tile is in vertical direction) **In non-tile-base type** The stride length is the distance from the start of one line to the start of the next line.

5.2.5.14. DEFE Channel 1 Line Stride Register

Offset: 0x0044			Register Name: DEFE_LINESTRD1_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0x0	LINE_STRIDE **In tile-based type** The stride length is the distance from the start of the end line in one tile to the start of the first line in next tile(here next tile is in vertical direction) **In non-tile-based type** The stride length is the distance from the start of one line to the start of the next line.

5.2.5.15. DEFE Channel 2 Line Stride Register

Offset: 0x0048			Register Name: DEFE_LINESTRD2_REG
Bit	R/W	Default/Hex	Description

Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

31:0	R/W	0x0	LINE_STRIDE **In tile-based type** The stride length is the distance from the start of the end line in one tile to the start of the first line in next tile(here next tile is in vertical direction) **In non-tile-based type** The stride length is the distance from the start of one line to the start of the next line.

5.2.5.16. DEFE Input Format Register

Offset: 0x004C			Register Name: DEFE_INPUT_FMT_REG
Bit	R/W	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	BYTE_SEQ Input data byte sequence selection 0: P3P2P1P0(word) 1: P0P1P2P3(word)
15:13	/	/	/
12	R/W	0x0	SCAN_MOD Scanning Mode selection 0: non-interlace 1: interlace
11	/	/	/
10:8	R/W	0x0	DATA_MOD Input data mode selection 000: non-tile-based planar data 001: interleaved data 010: non-tile-based UV combined data 100: tile-based planar data 110: tile-based UV combined data other: reserved
7	/	/	/
6:4	R/W	0x0	DATA_FMT Input component data format **In non-tile-based planar data mode:** 000: YUV 4:4:4 001: YUV 4:2:2 010: YUV 4:2:0 011: YUV 4:1:1 100: CSI RGB data 101: RGB888 Other: Reserved **In interleaved data mode:** 000: YUV 4:4:4 001: YUV 4:2:2 101: ARGB8888

Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Other: reserved **In non-tile-based UV combined data mode:** 001: YUV 4:2:2 010: YUV 4:2:0 011: YUV 4:1:1 Other: reserve **In tile-based planar data mode:** 001: YUV 4:2:2 010: YUV 4:2:0 011: YUV 4:1:1 Other: Reserved **In tile-based UV combined data mode:** 001: YUV 4:2:2 010: YUV 4:2:0 011: YUV 4:1:1 Other: reserved
3:2	/	/	/
1:0	R/W	0x0	DATA_PS Pixel sequence **In interleaved YUV422 data mode:** 00: Y1V0Y0U0 01: V0Y1U0Y0 10: Y1U0Y0V0 11: U0Y1V0Y0 **In interleaved YUV444 data mode:** 00: VUYA 01: AYUV Other: reserved **In UV combined data mode: (UV component)** 00: V1U1V0U0 01: U1V1U0V0 Other: reserved **In interleaved ARGB8888 data mode:** 00: BGRA 01: ARGB Other: reserved

5.2.5.17. DEFE Write Back Address Register

Offset: 0x0050			Register Name: DEFE_WB_ADDR_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0x0	WB_ADDR Write-back address setting for scaled data.

5.2.5.18. DEFE Output Format Register

Offset: 0x005C	Register Name: DEFE_OUTPUT_FMT_REG

Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	R/W	Default/Hex	Description
31:18	/	/	/
17:16	R/W	0	WB_Ch_Sel Write back channel select(chsel) 0/1: Ch3 2: Ch4 3: Ch5 Other: reserved
15:9	/	/	/
8	R/W	0x0	BYTE_SEQ Output data byte sequence selection 0: P3P2P1P0(word) 1: P0P1P2P3(word) For ARGB, when this bit is 0, the byte sequence is BGRA, and when this bit is 1, the byte sequence is ARGB;
7:5	/	/	/
4	R/W	0x0	SCAN_MOD Output interlace enable 0: disable 1: enable When output interlace enable, scaler selects YUV initial phase according to LCD field signal
3	/	/	/
2:0	R/W	0x0	DATA_FMT Data format 000: planar RGB888 conversion data format 001: interleaved BGRA8888 conversion data format(A component always be pad 0xff) 010: interleaved ARGB8888 conversion data format(A component always be pad 0xff) 100: planar YUV 444 101: planar YUV 420(only support YUV input and not interleaved mode) 110: planar YUV 422(only support YUV input) 111: planar YUV 411(only support YUV input) Other: reserved

5.2.5.19. DEFE Interrupt Enable Register

Offset: 0x0060			Register Name: DEFE_INT_EN_REG
Bit	R/W	Default/Hex	Description
31:11	/	/	/
10	R/W	0x0	REG_LOAD_EN Register ready load interrupt enable
9	R/W	0x0	LINE_EN Line interrupt enable
8	/	/	/

Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

7	R/W	0x0	WB_EN Write-back end interrupt enable 0: Disable 1: Enable
6:0	/	/	/

5.2.5.20. DEFE Interrupt Status Register

Offset: 0x0064			Register Name: DEFE_INT_STATUS_REG
Bit	R/W	Default/Hex	Description
31:11	/	/	/
10	R/W	0x0	REG_LOAD_STATUS Register ready load interrupt status
9	R/W	0x0	LINE_STATUS Line interrupt status
8	/	/	/
7	R/W	0x0	WB_STATUS Write-back end interrupt status
6:0	/	/	/

5.2.5.21. DEFE Status Register

Offset: 0x0068			Register Name: DEFE_STATUS_REG
Bit	R/W	Default/Hex	Description
31:29	/	/	/
28:16	R	0x0	LINE_ON_SYNC Line number(when sync reached)
15:6	/	/	/
11	R	0x0	COEF_ACCESS_STATUS Fir coef access status 0: scaler module can access fir coef ram 1: cpu can access fir coef ram This bit must be 1 before cpu access fir coef ram. When this bit is 1, scaler module will fetch 0x00004000 from ram.
10:6	/	/	/
5	R	0x0	LCD_FIELD LCD field status 0: top field 1: bottom field
4	R	0x0	DRAM_STATUS Access dram status 0: idle 1: busy This flag indicates whether DEFE is accessing dram
3	/	/	/
2	R	0x0	CFG_PENDING Register configuration pending

Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0: no pending 1: configuration pending This bit indicates the registers for the next frame has been configured. This bit will be set when configuration ready bit is set and this bit will be cleared when a new frame process begin.
1	R	0x0	WB_STATUS Write-back process status 0: write-back end or write-back disable 1: write-back in process This flag indicates that a full frame has not been written back to memory. The bit will be set when write-back enable bit is set, and be cleared when write-back process end.
0	R	0x0	FRM_BUSY Frame busy. This flag indicates that the frame is being processed. The bit will be set when frame process reset & start is set, and be cleared when frame process reset or disabled.

5.2.5.22. DEFE CSC Coefficient 00 Register

Offset: 0x0070			Register Name: DEFE_CSC_COEF00_REG
Bit	R/W	Default/Hex	Description
31:13	/	/	/
12:0	R/W	0x0	COEF the Y/G coefficient the value equals to coefficient*2^{10}

5.2.5.23. DEFE CSC Coefficient 01 Register

Offset: 0x0074			Register Name: DEFE_CSC_COEF01_REG
Bit	R/W	Default/Hex	Description
31:13	/	/	/
12:0	R/W	0x0	COEF the Y/G coefficient the value equals to coefficient*2^{10}

5.2.5.24. DEFE CSC Coefficient 02 Register

Offset: 0x0078			Register Name: DEFE_CSC_COEF02_REG
Bit	R/W	Default/Hex	Description
31:13	/	/	/
12:0	R/W	0x0	COEF the Y/G coefficient the value equals to coefficient*2^{10}

5.2.5.25. DEFE CSC Coefficient 03 Register

Offset: 0x007C			Register Name: DEFE_CSC_COEF03_REG
Bit	R/W	Default/Hex	Description

Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

31:14	/	/	/
13:0	R/W	0x0	CONT the Y/G constant the value equals to coefficient*2^4

5.2.5.26. DEFE CSC Coefficient 10 Register

Offset: 0x0080			Register Name: DEFE_CSC_COEF10_REG
Bit	R/W	Default/Hex	Description
31:13	/	/	/
12:0	R/W	0x0	COEF the U/R coefficient the value equals to coefficient*2^{10}

5.2.5.27. DEFE CSC Coefficient 11 Register

Offset: 0x0084			Register Name: DEFE_CSC_COEF11_REG
Bit	R/W	Default/Hex	Description
31:13	/	/	/
12:0	R/W	0x0	COEF the U/R coefficient the value equals to coefficient*2^{10}

5.2.5.28. DEFE CSC Coefficient 12 Register

Offset: 0x0088			Register Name: DEFE_CSC_COEF12_REG
Bit	R/W	Default/Hex	Description
31:13	/	/	/
12:0	R/W	0x0	COEF the U/R coefficient the value equals to coefficient*2^{10}

5.2.5.29. DEFE CSC Coefficient 13 Register

Offset: 0x008C			Register Name: DEFE_CSC_COEF13_REG
Bit	R/W	Default/Hex	Description
31:14	/	/	/
13:00	R/W	0x0	CONT the U/R constant the value equals to coefficient*2^4

5.2.5.30. DEFE CSC Coefficient 20 Register

Offset: 0x0090			Register Name: DEFE_CSC_COEF20_REG
Bit	R/W	Default/Hex	Description
31:13	/	/	/
12:0	R/W	0x0	COEF the V/B coefficient the value equals to coefficient*2^{10}

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

5.2.5.31. DEFE CSC Coefficient 21 Register

Offset: 0x0094			Register Name: DEFE_CSC_COEF21_REG
Bit	R/W	Default/Hex	Description
31:13	/	/	/
12:0	R/W	0x0	COEF the V/B coefficient the value equals to coefficient*2^{10}

5.2.5.32. DEFE CSC Coefficient 22 Register

Offset: 0x0098			Register Name: DEFE_CSC_COEF22_REG
Bit	R/W	Default/Hex	Description
31:13	/	/	/
12:0	R/W	0x0	COEF the V/B coefficient the value equals to coefficient*2^{10}

5.2.5.33. DEFE CSC Coefficient 23 Register

Offset: 0x009C			Register Name: DEFE_CSC_COEF23_REG
Bit	R/W	Default/Hex	Description
31:14	/	/	/
13:00	R/W	0x0	CONT the V/B constant the value equals to coefficient*2^{4}

5.2.5.34. DEFE Input Size Register

Offset: 0x0100			Register Name: DEFE_INSIZE_REG
Bit	R/W	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0x0	IN_HEIGHT Input image Y/G component height Input image height = The value of these bits add 1
15:13	/	/	/
12:0	R/W	0x0	IN_WIDTH Input image Y/G component width The image width = The value of these bits add 1 The maximum width is 2048.

5.2.5.35. DEFE Output Size Register

Offset: 0x0104			Register Name: DEFE_OUTSIZE_REG
Bit	R/W	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0x0	OUT_HEIGHT Output layer Y/G component height The output layer height = The value of these bits add 1
15:13	/	/	/

Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

12:0	R/W	0x0	OUT_WIDTH Output layer Y/G component width The output layer width = The value of these bits add 1 The maximum width is 1280.

5.2.5.36. DEFE Horizontal Factor Register

Offset: 0x0108			Register Name: DEFE_HORZFACT_REG
Bit	R/W	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0x0	FACTOR_INT The integer part of the horizontal scaling ratio the horizontal scaling ratio = input width/output width
15:0	R/W	0x0	FACTOR_FRAC The fractional part of the horizontal scaling ratio the horizontal scaling ratio = input width/output width

5.2.5.37. DEFE Vertical Register

Offset: 0x010C			Register Name: DEFE_VERTFACT_REG
Bit	R/W	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0x0	FACTOR_INT The integer part of the vertical scaling ratio the vertical scaling ratio = input height/output height
15:0	R/W	0x0	FACTOR_FRAC The fractional part of the vertical scaling ratio the vertical scaling ratio = input height /output height

5.2.5.38. DEFE Channel 0 Horizontal Filter Coefficient Register

Offset: 0x0400+N*4 (N=0~31)			Register Name: DEFE_CH0_HORZCOEF0_REG
Bit	R/W	Default/Hex	Description
31:24	R/W	0x0	TAP3 Horizontal tap3 coefficient The value equals to coefficient*2^6
23:16	R/W	0x0	TAP2 Horizontal tap2 coefficient The value equals to coefficient*2^6
15:8	R/W	0x0	TAP1 Horizontal tap1 coefficient The value equals to coefficient*2^6
7:0	R/W	0x0	TAP0 Horizontal tap0 coefficient The value equals to coefficient*2^6

5.2.5.39. DEFE Channel 0 Vertical Filter Coefficient Register

Offset: 0x500+N*4 (N=0~31)	Register Name: DEFE_CH0_VERTCOEF_REG

Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	R/W	Default/Hex	Description
31:24	R/W	0x0	TAP3 Vertical tap3 coefficient The value equals to coefficient*2^6
23:16	R/W	0x0	TAP2 Vertical tap2 coefficient The value equals to coefficient*2^6
15:8	R/W	0x0	TAP1 Vertical tap1 coefficient The value equals to coefficient*2^6
7:0	R/W	0x0	TAP0 Vertical tap0 coefficient The value equals to coefficient*2^6

5.2.5.40. DEFE Channel 1 Horizontal Filter Coefficient Register

Offset: 0x600+N*4 (N=0~31)			Register Name: DEFE_CH1_HORZCOEF0_REG
Bit	R/W	Default/Hex	Description
31:24	R/W	0x0	TAP3 Horizontal tap3 coefficient The value equals to coefficient*2^6
23:16	R/W	0x0	TAP2 Horizontal tap2 coefficient The value equals to coefficient*2^6
15:8	R/W	0x0	TAP1 Horizontal tap1 coefficient The value equals to coefficient*2^6
7:0	R/W	0x0	TAP0 Horizontal tap0 coefficient The value equals to coefficient*2^6

5.2.5.41. DEFE Channel 1 Vertical Filter Coefficient Register

Offset: 0x700+N*4 (N=0~31)			Register Name: DEFE_CH1_VERTCOEF_REG
Bit	R/W	Default/Hex	Description
31:24	R/W	0x0	TAP3 Vertical tap3 coefficient The value equals to coefficient*2^6
23:16	R/W	0x0	TAP2 Vertical tap2 coefficient The value equals to coefficient*2^6
15:8	R/W	0x0	TAP1 Vertical tap1 coefficient The value equals to coefficient*2^6
7:0	R/W	0x0	TAP0 Vertical tap0 coefficient The value equals to coefficient*2^6

Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

5.3. Display Engine Back-End

5.3.1. Overview

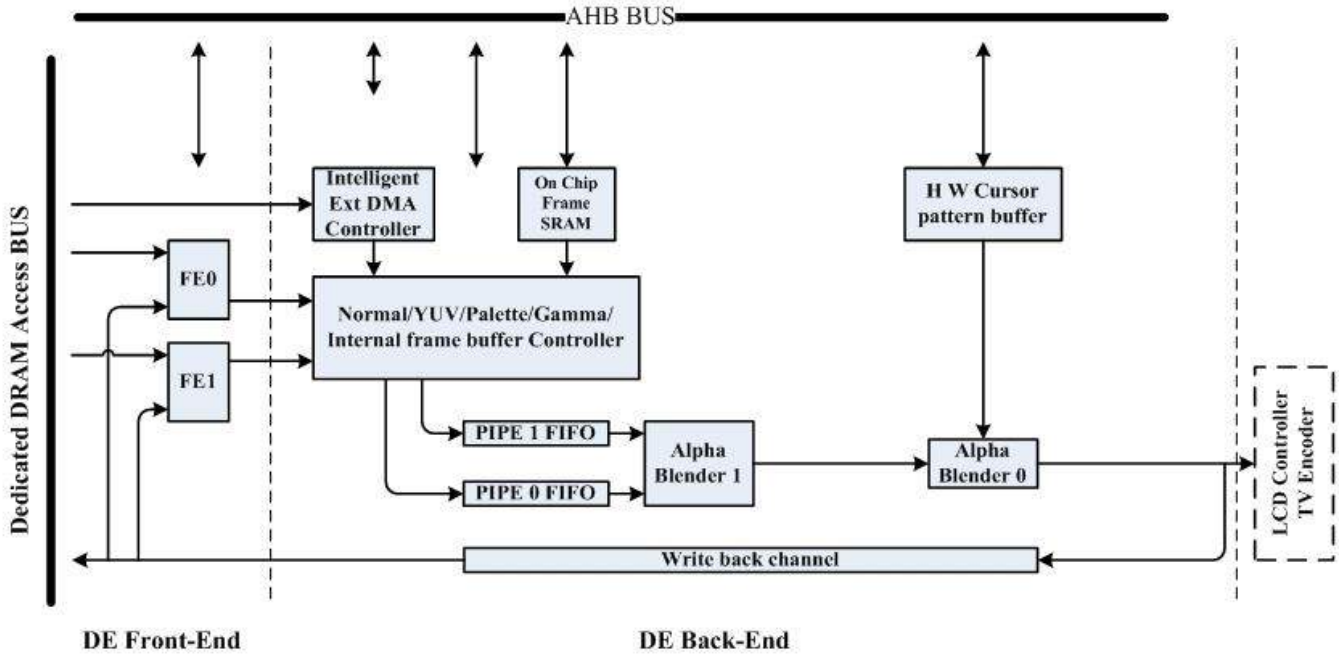
The display engine back-end (DEBE) has two pipes data path, and it can receive data from DEFE or data from SDRAM to do overlay, and then doing alpha blending in the Alpha Blender1 part. After blending, the data can do image enhancement in Color Correction or bypass to the flowing part LCD etc.

5.3.2. Feature

The DEBE includes the following features:

- Support four moveable and size-adjustable layers
- Support layer size up to 2048*2048 pixels
- Support alpha blending
- Support color key
- Support write back function
- Support multi-format input data
  - 1/2/4/8 bpp mono / palette
  - 16/24/32 bpp color support (external frame buffer)
  - YUV444/YUV422/YUV420/YUV411
- Support hardware cursor

5.3.3. Block Diagram



Display Engine Function Block

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

5.3.4. DEBE Register List

Module Name	Base Address
DEBE	0x01E60000

Register Name	Offset	Description
DEBE_MODE_CTRL_REG	0x800	DEBE Mode Control Register
DEBE_COLOR_CTRL_REG	0x804	DEBE Color Control Register
DEBE_LAY0_SIZE_REG	0x810	DEBE Layer 0 Size Register
DEBE_LAY1_SIZE_REG	0x814	DEBE Layer 1 Size Register
DEBE_LAY2_SIZE_REG	0x818	DEBE Layer 2 Size Register
DEBE_LAY3_SIZE_REG	0x81C	DEBE Layer 3 Size Register
DEBE_LAY0_CODNT_REG	0x820	DEBE layer 0 Coordinate Control Register
DEBE_LAY1_CODNT_REG	0x824	DEBE Layer 1 Coordinate Control Register
DEBE_LAY2_CODNT_REG	0x828	DEBE Layer 2 Coordinate Control Register
DEBE_LAY3_CODNT_REG	0x82C	DEBE Layer 3 Coordinate Control Register
DEBE_LAY0_LINEWIDTH_REG	0x840	DEBE Layer 0 Frame Buffer Line Width Register
DEBE_LAY1_LINEWIDTH_REG	0x844	DEBE Layer 1 Frame Buffer Line Width Register
DEBE_LAY2_LINEWIDTH_REG	0x848	DEBE Layer 2 Frame Buffer Line Width Register
DEBE_LAY3_LINEWIDTH_REG	0x84C	DEBE Layer 3 Frame Buffer Line Width Register
DEBE_LAY0_FB_ADDR_REG	0x850	DEBE Layer 0 Frame Buffer Address Register
DEBE_LAY1_FB_ADDR_REG	0x854	DEBE Layer 1 Frame Buffer Address Register
DEBE_LAY2_FB_ADDR_REG	0x858	DEBE Layer 2 Frame Buffer Address Register
DEBE_LAY3_FB_ADDR_REG	0x85C	DEBE Layer 3 Frame Buffer Address Register
DEBE_REGBUFF_CTRL_REG	0x870	DEBE Register Buffer Control Register
DEBE_CK_MAX_REG	0x880	DEBE Color Key Max Register
DEBE_CK_MIN_REG	0x884	DEBE Color Key Min register
DEBE_CK_CFG_REG	0x888	DEBE Color Key Configuration Register
DEBE_ LAY0_ATT_CTRL_REG0	0x890	DEBE Layer 0 Attribute Control Register 0
DEBE_ LAY1_ATT_CTRL_REG0	0x894	DEBE Layer 1 Attribute Control register 1
DEBE_ LAY2_ATT_CTRL_REG0	0x898	DEBE Layer2 Attribute Control Register 0
DEBE_ LAY3_ATT_CTRL_REG0	0x89C	DEBE Layer3 Attribute Control Register 0
DEBE_ LAY0_ATT_CTRL_REG1	0x8A0	DEBE Layer0 Attribute Control Register 1
DEBE_ LAY1_ATT_CTRL_REG1	0x8A4	DEBE Layer 1 Attribute Control Register 1
DEBE_ LAY2_ATT_CTRL_REG1	0x8A8	DEBE Layer 2 Attribute Control Register 1
DEBE_ LAY3_ATT_CTRL_REG1	0x8AC	DEBE Layer 3 Attribute Control Register 1
DEBE_HWC_CTRL_REG	0x8D8	DEBE HWC Coordinate Control Register
DEBE_HWCFB_CTRL_REG	0x8E0	DEBE HWC Frame Buffer Format Register
DEBE_WB_CTRL_REG	0x8F0	DEBE Write Back Control Register
DEBE_WB_ADDR_REG	0x8F4	DEBE Write Back Address Register
DEBE_WB_ LW _REG	0x8F8	DEBE Write Back Buffer Line Width Register
DEBE_IYUV_CH_CTRL_REG	0x920	DEBE Input YUV Channel Control Register
DEBE_CH0_YUV_FB_ADDR_REG	0x930	DEBE YUV Channel 0 Frame Buffer Address Register
DEBE_CH1_YUV_FB_ADDR_REG	0x934	DEBE YUV Channel 1 Frame Buffer Address Register

Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

DEBE_CH2_YUV_FB_ADDR_REG	0x938	DEBE YUV Channel 2 Frame Buffer Address Register
DEBE_CH0_YUV_BLW_REG	0x940	DEBE YUV Channel 0 Buffer Line Width Register
DEBE_CH1_YUV_ BLW _REG	0x944	DEBE YUV Channel 1 Buffer Line Width Register
DEBE_CH2_YUV_ BLW _REG	0x948	DEBE YUV Channel 2 Buffer Line Width Register
DEBE_COEF00_REG	0x950	DEBE Coefficient 00 Register
DEBE_ COEF01_REG	0x954	DEBE Coefficient 01 Register
DEBE_ COEF02_REG	0x958	DEBE Coefficient 02 Register
DEBE_ COEF03_REG	0x95C	DEBE Coefficient 03 Register
DEBE_ COEF10_REG	0x960	DEBE Coefficient 10 Register
DEBE_ COEF11_REG	0x964	DEBE Coefficient 11 Register
DEBE_ COEF12_REG	0x968	DEBE Coefficient 12 Register
DEBE_ COEF13_REG	0x96C	DEBE Coefficient 13 Register
DEBE_ COEF20_REG	0x970	DEBE Coefficient 20 Register
DEBE_ COEF21_REG	0x974	DEBE Coefficient 21 Register
DEBE_ COEF22_REG	0x978	DEBE Coefficient 22 Register
DEBE_ COEF23_REG	0x97C	DEBE Coefficient 23 Register

5.3.5. DEBE Register Description

5.3.5.1. DEBE Mode Control Register

Offset: 0x800			Register Name: DEBE_MODE_CTRL_REG
Bit	R/W	Default/Hex	Description
31:17	/	/	/
16	R/W	0	Hardware cursor enabled/disabled control 0: Disabled 1: Enabled Hardware cursor has the highest priority, in the alpha blender0, the alpha value of cursor will be selected
15:12	/	/	/
11	R/W	0	Layer3 Enable/Disable 0: Disabled 1: Enabled
10	R/W	0	Layer2 Enable/Disable 0: Disabled 1: Enabled
9	R/W	0	Layer1 Enable/Disable 0: Disabled 1: Enabled
8	R/W	0	Layer0 Enable/Disable 0: Disabled 1: Enabled
7:6	/	/	/
5	R/W	0	Output CSC enable 0: disable

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: enable
4	R/W	0	De-flick enable 0: disable 1: enable
3:2	/	/	/
1	R/W	0	Normal output channel Start & Reset control 0: reset 1: start
0	R/W	0	DE back-end enable/disable 0: disable 1: enable

5.3.5.2. DEBE Color Control Register

Offset : 0x804			Register Name: DEBE_BACKCOLOR_REG
Bit	R/W	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0	Red Red screen background color value
15:08	R/W	0	Green Green screen background color value
07:00	R/W	0	Blue Blue screen background color value

5.3.5.3. DEBE Layer 0 Size Register

Offset: 0x810			Register Name: DEBE_LAY0_SIZE_REG
Bit	R/W	Default/Hex	Description
31:27	/	/	/
26:16	R/W	0	Layer Height The Layer Height = The value of these bits add 1
15:11	/	/	/
10:0	R/W	0	Layer Width The Layer Width = The value of these bits add 1

5.3.5.4. DEBE Layer 1 Size Register

Offset: 0x814			Register Name: DEBE_LAY1_SIZE_REG
Bit	R/W	Default/Hex	Description
31:27	/	/	/
26:16	R/W	0	Layer Height The Layer Height = The value of these bits add 1
15:11	/	/	/
10:0	R/W	0	Layer Width The Layer Width = The value of these bits add 1

5.3.5.5. DEBE Layer 2 Size Register

Offset: 0x818	Register Name: DEBE_LAY2_SIZE_REG

Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	R/W	Default/Hex	Description
31:27	/	/	/
26:16	R/W	0	Layer Height The Layer Height = The value of these bits add 1
15:11	/	/	/
10:0	R/W	0	Layer Width The Layer Width = The value of these bits add 1

5.3.5.6. DEBE Layer 3 Size Register

Offset: 0x81C			Register Name: DEBE_LAY3_SIZE_REG
Bit	R/W	Default/Hex	Description
31:27	/	/	/
26:16	R/W	0	Layer Height The Layer Height = The value of these bits add 1
15:11	/	/	/
10:0	R/W	0	Layer Width The Layer Width = The value of these bits add 1

5.3.5.7. DEBE Layer 0 Coordinate Control Register

Offset: 0x820			Register Name: DEBE_LAY0_CODNT_REG
Bit	R/W	Default/Hex	Description
31:16	R/W	0	Y coordinate Y is the left-top y coordinate of layer on screen in pixels The Y represent the two's complement
15:0	R/W	0	X coordinate X is left-top x coordinate of the layer on screen in pixels The X represent the two's complement

5.3.5.8. DEBE Layer 1 Coordinate Control Register

Offset: 0x824			Register Name: DEBE_LAY1_CODNT_REG
Bit	R/W	Default/Hex	Description
31:16	R/W	0	Y coordinate Y is the left-top y coordinate of layer on screen in pixels The Y represent the two's complement
15:0	R/W	0	X coordinate X is left-top x coordinate of the layer on screen in pixels The X represent the two's complement

5.3.5.9. DEBE Layer 2 Coordinate Control Register

Offset: 0x828			Register Name: DEBE_LAY2_CODNT_REG
Bit	R/W	Default/Hex	Description
31:16	R/W	0	Y coordinate Y is the left-top y coordinate of layer on screen in pixels The Y represent the two's complement
15:0	R/W	0	X coordinate

Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			X is left-top x coordinate of the layer on screen in pixels The X represent the two's complement

5.3.5.10. DEBE Layer 3 Coordinate Control Register

Offset: 0x82C			Register Name: DEBE_LAY3_CODNT_REG
Bit	R/W	Default/Hex	Description
31:16	R/W	0	Y coordinate Y is the left-top y coordinate of layer on screen in pixels The Y represent the two's complement
15:0	R/W	0	X coordinate X is left-top x coordinate of the layer on screen in pixels The X represent the two's complement

5.3.5.11. DEBE Layer 0 Frame Buffer Line Width Register

Offset: 0x840			Register Name: DEBE_LAY0_LINEWIDTH_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0	Layer frame buffer line width in bits.

Note: If the layer is selected by video channel or YUV channel, the setting of this register will be ignored.

5.3.5.12. DEBE Layer 1 Frame Buffer Line Width Register

Offset: 0x844			Register Name: DEBE_LAY1_LINEWIDTH_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0	Layer frame buffer line width in bits.

Note: If the layer is selected by video channel or YUV channel, the setting of this register will be ignored.

5.3.5.13. DEBE Layer 2 Frame Buffer Line Width Register

Offset: 0x848			Register Name: DEBE_LAY2_LINEWIDTH_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0	Layer frame buffer line width in bits.

Note: If the layer is selected by video channel or YUV channel, the setting of this register will be ignored.

5.3.5.14. DEBE Layer 3 Frame Buffer Line Width Register

Offset: 0x84C			Register Name: DEBE_LAY3_LINEWIDTH_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0	Layer frame buffer line width in bits.

Note: If the layer is selected by video channel or YUV channel, the setting of this register will be ignored.

5.3.5.15. DEBE Layer 0 Frame Buffer Address Register

Offset : 0x850			Register Name: DEBE_LAY0_FB_ADDR_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0	Buffer Address Layer Frame Buffer Address in bit

Note: If the layer is selected by video channel or YUV channel, the setting of this register will be ignored.

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

5.3.5.16. DEBE Layer 1 Frame Buffer Address Register

Offset : 0x854			Register Name: DEBE_LAY1_FB_ADDR_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0	Buffer Address Layer Frame Buffer Address in bit

Note: If the layer is selected by video channel or YUV channel, the setting of this register will be ignored.

5.3.5.17. DEBE Layer 2 Frame Buffer Address Register

Offset : 0x858			Register Name: DEBE_LAY2_FB_ADDR_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0	Buffer Address Layer Frame Buffer Address in bit

Note: If the layer is selected by video channel or YUV channel, the setting of this register will be ignored.

5.3.5.18. DEBE Layer 3 Frame Buffer Address Register

Offset : 0x85C			Register Name: DEBE_LAY3_FB_ADDR_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0	Buffer Address Layer Frame Buffer Address in bit

Note: If the layer is selected by video channel or YUV channel, the setting of this register will be ignored.

5.3.5.19. DEBE Register Buffer Control Register

Offset: 0x870			Register Name: DEBE_REGBUFF_CTRL_REG
Bit	R/W	Default/Hex	Description
31:2	/	/	/
1	R/W	0	Module registers loading auto mode disable control 0: registers auto loading mode 1: disable registers auto loading mode, the registers will be loaded by write 1 to bit0 of this register
0	R/W	0	Register load control When the Module registers loading auto mode disable control bit is set, the registers will be loaded by write 1 to the bit, and the bit will self clean when the registers is loading done

5.3.5.20. DEBE Color Key Max Register

Offset: 0x880			Register Name: DEBE_CK_MAX_REG
Bit	R/W	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0xFF	Red Red color key max
15:8	R/W	0xFF	Green Green color key max
7:0	R/W	0xFF	Blue Blue color key max

Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

5.3.5.21. DEBE Color Key Min Register

Offset: 0x884			Register Name: DEBE_CK_MIN_REG
Bit	R/W	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0	Red Red color key min
15:8	R/W	0	Green Green color key min
7:0	R/W	0	Blue Blue color key min

5.3.5.22. DEBE Color Key Configuration Register

Offset: 0x888			Register Name: DEBE_CK_CFG_REG
Bit	R/W	Default/Hex	Description
31:6	/	/	/
5:4	R/W	0	Red Match Rule 00: always match 01: always match 10: match if (Color Min=<Color<=Color Max) 11: match if (Color>Color Max or Color<Color Min)
3:2	R/W	0	Green Match Rule 00: always match 01: always match 10: match if (Color Min=<Color<=Color Max) 11: match if (Color>Color Max or Color<Color Min)
1:0	R/W	0	Blue Match Rule 00: always match 01: always match 10: match if (Color Min=<Color<=Color Max) 11: match if (Color>Color Max or Color<Color Min)

5.3.5.23. DEBE Layer 0 Attribute Control Register 0

Offset: 0x890			Register Name: DEBE_LAY0_ATT_CTRL_RGE0
Bit	R/W	Default/Hex	Description
31:24	R/W	0	Alpha value Alpha value is used for this layer
23:22	R/W	0	Layer working mode selection 00: normal mode (Non-Index mode) 01: palette mode (Index mode) Other: reserved Except the normal mode, if the palette working mode is selected, the on chip palette table SRAM will be enabled.
21:20	/	/	/
19:18	R/W	0	Color key Mode 00: disabled color key

Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			01: The layer color key match another channel pixel data in Alpha Blender1. 1x: Reserved Only 2 channels pixel data can get to Alpha Blender1 at the same screen coordinate.
17:16	/	/	/
15	R/W	0	Pipe Select 0: select Pipe 0 1: select Pipe 1
14:12	/	/	/
11:10	R/W	0	Priority The rule is: 11>10>01>00 • When more than 2 layers are enabled, the priority value of each layer must be different, soft designer must keep the condition. • If more than 1 layer selects the same pipe, in the overlapping area, only the pixel of highest priority layer can pass the pipe to blender1. • If both 2 pipes are selected by layers, in the overlapping area, the alpha value will use the alpha value of higher priority layer in the blender1.
9:3	/	/	/
2	R/W	0	YUV channel selection 0: disable 1: enable Setting 2 or more layers YUV channel mode is illegal, programmer should confirm it.
1	R/W	0	Layer video channel selection 0: disable 1: enable Normally, one layer cannot be set both video channel and YUV channel mode, if both 2 mode is set, the layer will work in video channel mode, YUV channel mode will be ignored, and programmer should confirm it. Setting 2 or more layers video channel mode is illegal, programmer should confirm it.
0	R/W	0	Alpha Enable 0: Disabled the alpha value of this register 1: Enabled the alpha value of this register for the layer

5.3.5.24. DEBE Layer 1 Attribute Control Register 0

Offset: 0x894			Register Name: DEBE_LAY1_ATT_CTRL_RGE0
Bit	R/W	Default/Hex	Description
31:24	R/W	0	Alpha value Alpha value is used for this layer
23:22	R/W	0	Layer working mode selection 00: normal mode (Non-Index mode) 01: palette mode (Index mode) Other: reserved

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Except the normal mode, if the palette working mode is selected, the on chip palette table SRAM will be enabled.
21:20	/	/	/
19:18	R/W	0	Color key Mode 00: disabled color key 01: The layer color key match another channel pixel data in Alpha Blender1. 1x: Reserved Only 2 channels pixel data can get to Alpha Blender1 at the same screen coordinate.
17:16	/	/	/
15	R/W	0	Pipe Select 0: select Pipe 0 1: select Pipe 1
14:12	/	/	/
11:10	R/W	0	Priority The rule is: 11>10>01>00 • When more than 2 layers are enabled, the priority value of each layer must be different, soft designer must keep the condition. • If more than 1 layer selects the same pipe, in the overlapping area, only the pixel of highest priority layer can pass the pipe to blender1. • If both 2 pipes are selected by layers, in the overlapping area, the alpha value will use the alpha value of higher priority layer in the blender1.
9:3	/	/	/
2	R/W	0	YUV channel selection 0: disable 1: enable Setting 2 or more layers YUV channel mode is illegal, programmer should confirm it.
1	R/W	0	Layer video channel selection 0: disable 1: enable Normally, one layer cannot be set both video channel and YUV channel mode, if both 2 mode is set, the layer will work in video channel mode, YUV channel mode will be ignored, and programmer should confirm it. Setting 2 or more layers video channel mode is illegal, programmer should confirm it.
0	R/W	0	Alpha Enable 0: Disabled the alpha value of this register 1: Enabled the alpha value of this register for the layer

5.3.5.25. DEBE Layer 2 Attribute Control Register 0

Offset: 0x898			Register Name: DEBE_LAY2_ATT_CTRL_RGE0
Bit	R/W	Default/Hex	Description
31:24	R/W	0	Alpha value

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Alpha value is used for this layer
23:22	R/W	0	Layer working mode selection 00: normal mode (Non-Index mode) 01: palette mode (Index mode) Other: reserved Except the normal mode, if the palette working mode is selected, the on chip palette table SRAM will be enabled.
21:20	/	/	/
19:18	R/W	0	Color key Mode 00: disabled color key 01: The layer color key match another channel pixel data in Alpha Blender1. 1x: Reserved Only 2 channels pixel data can get to Alpha Blender1 at the same screen coordinate.
17:16	/	/	/
15	R/W	0	Pipe Select 0: select Pipe 0 1: select Pipe 1
14:12	/	/	/
11:10	R/W	0	Priority The rule is: 11>10>01>00 • When more than 2 layers are enabled, the priority value of each layer must be different, soft designer must keep the condition. • If more than 1 layer selects the same pipe, in the overlapping area, only the pixel of highest priority layer can pass the pipe to blender1. • If both 2 pipes are selected by layers, in the overlapping area, the alpha value will use the alpha value of higher priority layer in the blender1.
9:3	/	/	/
2	R/W	0	YUV channel selection 0: disable 1: enable Setting 2 or more layers YUV channel mode is illegal, programmer should confirm it.
1	R/W	0	Layer video channel selection 0: disable 1: enable Normally, one layer cannot be set both video channel and YUV channel mode, if both 2 mode is set, the layer will work in video channel mode, YUV channel mode will be ignored, and programmer should confirm it. Setting 2 or more layers video channel mode is illegal, programmer should confirm it.
0	R/W	0	Alpha Enable 0: Disabled the alpha value of this register 1: Enabled the alpha value of this register for the layer

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

5.3.5.26. DEBE Layer 3 Attribute Control Register 0

Offset: 0x89C			Register Name: DEBE_LAY3_ATT_CTRL_RGE0
Bit	R/W	Default/Hex	Description
31:24	R/W	0	Alpha value Alpha value is used for this layer
23:22	R/W	0	Layer working mode selection 00: normal mode (Non-Index mode) 01: palette mode (Index mode) Other: reserved Except the normal mode, if the palette working mode is selected, the on chip palette table SRAM will be enabled.
21:20	/	/	/
19:18	R/W	0	Color key Mode 00: disabled color key 01: The layer color key match another channel pixel data in Alpha Blender1. 1x: Reserved Only 2 channels pixel data can get to Alpha Blender1 at the same screen coordinate.
17:16	/	/	/
15	R/W	0	Pipe Select 0: select Pipe 0 1: select Pipe 1
14:12	/	/	/
11:10	R/W	0	Priority The rule is: 11>10>01>00 • When more than 2 layers are enabled, the priority value of each layer must be different, soft designer must keep the condition. • If more than 1 layer selects the same pipe, in the overlapping area, only the pixel of highest priority layer can pass the pipe to blender1. • If both 2 pipes are selected by layers, in the overlapping area, the alpha value will use the alpha value of higher priority layer in the blender1.
9:3	/	/	/
2	R/W	0	YUV channel selection 0: disable 1: enable Setting 2 or more layers YUV channel mode is illegal, programmer should confirm it.
1	R/W	0	Layer video channel selection 0: disable 1: enable Normally, one layer cannot be set both video channel and YUV channel mode, if both 2 mode is set, the layer will work in video channel mode, YUV channel mode will be ignored, and programmer should confirm it. Setting 2 or more layers video channel mode is illegal, programmer should

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			confirm it.
0	R/W	0	Alpha Enable 0: Disabled the alpha value of this register 1: Enabled the alpha value of this register for the layer

5.3.5.27. DEBE Layer 0 Attribute Control Register 1

Offset : 0x8A0			Register Name: DEBE_LAY0_ATT_CTRL_RGE1
Bit	R/W	Default/Hex	Description
31:12	/	/	/
11:8	R/W	0	Frame buffer format Normal mode data format 0000: mono 1-bpp 0001: mono 2-bpp 0010: mono 4-bpp 0011: mono 8-bpp 0100: color 16-bpp (R:6/G:5/B:5) 0101: color 16-bpp (R:5/G:6/B:5) 0110: color 16-bpp (R:5/G:5/B:6) 0111: color 16-bpp (Alpha:1/R:5/G:5/B:5) 1000: color 16-bpp (R:5/G:5/B:5/Alpha:1) 1001: color 32-bpp (Padding:8/R:8/G:8/B:8) 1010: color 32-bpp (Alpha:8/R:8/G:8/B:8) 1011: color 24-bpp (R/G/B/R) 1100-0x1111: Reserved Palette Mode data format In palette mode, the data of external frame buffer is regarded as pattern. 0000: 1-bpp 0001: 2-bpp 0010: 4-bpp 0011: 8-bpp other: Reserved Note: If the layer is selected by video channel or YUV channel, the setting of the bits will be ignored.
7:3	/	/	/
2	R/W	0	B R channel swap 0: RGB. Follow the bit[11:8]----RGB 1: BGR. Swap the B R channel in the data format.
01:0	R/W	0	PS Pixels Sequence See the follow table “Pixels Sequence” Note: If the layer is selected by video channel or YUV channel, the setting of the bits will be ignored.

5.3.5.28. DEBE Layer 1 Attribute Control Register 1

Offset : 0x8A4	Register Name: DEBE_LAY1_ATT_CTRL_RGE1

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	R/W	Default/Hex	Description
31:12	/	/	/
11:8	R/W	0	Frame buffer format Normal mode data format 0000: mono 1-bpp 0001: mono 2-bpp 0010: mono 4-bpp 0011: mono 8-bpp 0100: color 16-bpp (R:6/G:5/B:5) 0101: color 16-bpp (R:5/G:6/B:5) 0110: color 16-bpp (R:5/G:5/B:6) 0111: color 16-bpp (Alpha:1/R:5/G:5/B:5) 1000: color 16-bpp (R:5/G:5/B:5/Alpha:1) 1001: color 32-bpp (Padding:8/R:8/G:8/B:8) 1010: color 32-bpp (Alpha:8/R:8/G:8/B:8) 1011: color 24-bpp (R/G/B/R) 1100-0x1111: Reserved Palette Mode data format In palette mode, the data of external frame buffer is regarded as pattern. 0000: 1-bpp 0001: 2-bpp 0010: 4-bpp 0011: 8-bpp other: Reserved Note: If the layer is selected by video channel or YUV channel, the setting of the bits will be ignored.
7:3	/	/	/
2	R/W	0	B R channel swap 0: RGB. Follow the bit[11:8]----RGB 1: BGR. Swap the B R channel in the data format.
01:0	R/W	0	PS Pixels Sequence See the follow table “Pixels Sequence” Note: If the layer is selected by video channel or YUV channel, the setting of the bits will be ignored.

5.3.5.29. DEBE Layer 2 Attribute Control Register 1

Offset : 0x8A8			Register Name: DEBE_LAY2_ATT_CTRL_RGE1
Bit	R/W	Default/Hex	Description
31:12	/	/	/
11:8	R/W	0	Frame buffer format Normal mode data format 0000: mono 1-bpp 0001: mono 2-bpp 0010: mono 4-bpp

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0011: mono 8-bpp 0100: color 16-bpp (R:6/G:5/B:5) 0101: color 16-bpp (R:5/G:6/B:5) 0110: color 16-bpp (R:5/G:5/B:6) 0111: color 16-bpp (Alpha:1/R:5/G:5/B:5) 1000: color 16-bpp (R:5/G:5/B:5/Alpha:1) 1001: color 32-bpp (Padding:8/R:8/G:8/B:8) 1010: color 32-bpp (Alpha:8/R:8/G:8/B:8) 1011: color 24-bpp (R/G/B/R) 1100-0x1111: Reserved Palette Mode data format In palette mode, the data of external frame buffer is regarded as pattern. 0000: 1-bpp 0001: 2-bpp 0010: 4-bpp 0011: 8-bpp other: Reserved Note: If the layer is selected by video channel or YUV channel, the setting of the bits will be ignored.
7:3	/	/	/
2	R/W	0	B R channel swap 0: RGB. Follow the bit[11:8]----RGB 1: BGR. Swap the B R channel in the data format.
01:0	R/W	0	PS Pixels Sequence See the follow table “Pixels Sequence” Note: If the layer is selected by video channel or YUV channel, the setting of the bits will be ignored.

5.3.5.30. DEBE Layer 3 Attribute Control Register 1

Offset : 0x8AC			Register Name: DEBE_LAY3_ATT_CTRL_RGE1
Bit	R/W	Default/Hex	Description
31:12	/	/	/
11:8	R/W	0	Frame buffer format Normal mode data format 0000: mono 1-bpp 0001: mono 2-bpp 0010: mono 4-bpp 0011: mono 8-bpp 0100: color 16-bpp (R:6/G:5/B:5) 0101: color 16-bpp (R:5/G:6/B:5) 0110: color 16-bpp (R:5/G:5/B:6) 0111: color 16-bpp (Alpha:1/R:5/G:5/B:5) 1000: color 16-bpp (R:5/G:5/B:5/Alpha:1) 1001: color 32-bpp (Padding:8/R:8/G:8/B:8)

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1010: color 32-bpp (Alpha:8/R:8/G:8/B:8) 1011: color 24-bpp (R/G/B/R) 1100-0x1111: Reserved Palette Mode data format In palette mode, the data of external frame buffer is regarded as pattern. 0000: 1-bpp 0001: 2-bpp 0010: 4-bpp 0011: 8-bpp other: Reserved Note: If the layer is selected by video channel or YUV channel, the setting of the bits will be ignored.
7:3	/	/	/
2	R/W	0	B R channel swap 0: RGB. Follow the bit[11:8]----RGB 1: BGR. Swap the B R channel in the data format.
01:0	R/W	0	PS Pixels Sequence See the follow table “Pixels Sequence” Note: If the layer is selected by video channel or YUV channel, the setting of the bits will be ignored.

Pixels sequence table

DE-layer attribute control register1 [11:8] = FBF (frame buffer format)

DE-layer attribute control register1 [1:0] = PS (pixels sequence

Mono or palette 1-bpp mode: FBF = 0000

PS=00

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P31	P30	P29	P28	P27	P26	P25	P24	P23	P22	P21	P20	P19	P18	P17	P16
P15	P14	P13	P12	P11	P10	P09	P08	P07	P06	P05	P04	P03	P02	P01	P00
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=01

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P24	P25	P26	P27	P28	P29	P30	P31	P16	P17	P18	P19	P20	P21	P22	P23
P08	P09	P10	P11	P12	P13	P14	P15	P00	P01	P02	P03	P04	P05	P06	P07
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=10

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P07	P06	P05	P04	P03	P02	P01	P00	P15	P14	P13	P12	P11	P10	P09	P08
P23	P22	P21	P20	P19	P18	P17	P16	P31	P30	P29	P28	P27	P26	P25	P24
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=11

Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P00	P01	P02	P03	P04	P05	P06	P07	P08	P09	P10	P11	P12	P13	P14	P15
P16	P17	P18	P19	P20	P21	P22	P23	P24	P25	P26	P27	P28	P29	P30	P31
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

Mono or palette 2-bpp mode: FBF = 0001

PS=00

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P15		P14		P13		P12		P11		P10		P09		P08	
P07		P06		P05		P04		P03		P02		P01		P00	
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=01

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P12		P13		P14		P15		P08		P09		P10		P11	
P04		P05		P06		P07		P00		P01		P02		P03	
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=10

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P03		P02		P01		P00		P07		P06		P05		P04	
P11		P10		P09		P08		P15		P14		P13		P12	
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=11

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P00		P01		P02		P03		P04		P05		P06		P07	
P08		P09		P10		P11		P12		P13		P14		P15	
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

Mono 4-bpp or palette 4-bpp mode: FBF = 0010

PS=00

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P07				P06				P05				P04			
P03				P02				P01				P00			
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=01

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P06				P07				P04				P05			
P02				P03				P00				P01			
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=10

Bit

Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P01				P00				P03				P02			
P05				P04				P07				P06			
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=11

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P00				P01				P02				P03			
P04				P05				P06				P07			
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

Mono 8-bpp mode or palette 8-bpp mode: FBF = 0011

PS=00/11

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P3								P2							
P1								P0							
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=01/10

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P0								P1							
P2								P3							
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

Color 16-bpp mode: FBF = 0100 or 0101 or 0110 or 0111 or 1000

PS=00

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P1															
P0															
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=01

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P0															
P1															
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=10/11

Invalid

Color 24-bpp or 32-bpp mode: FBF = 1001 or 1010

PS=00/01

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P0															
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

The bytes sequence is **ARGB**

Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

PS=10/11

Bit															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P0															
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

The bytes sequence is **BGRA**

5.3.5.31. DEBE HWC Coordinate Control Register

Offset: 0x8D8			Register Name: DEBE_HWC_CTRL_REG
Bit	R/W	Default/Hex	Description
31:27	R/W	0	Y coordinate offset The hardware cursor is 32*32 2-bpp pattern, this value represent the start position of the cursor in Y coordinate
26:16	R/W	0	Hardware cursor Y coordinate
15:11	R/W	0	X coordinate offset The hardware cursor is 32*32 2-bpp pattern, this value represent the start position of the cursor in X coordinate
10:0	R/W	0	Hardware cursor X coordinate

5.3.5.32. DEBE HWC Frame Buffer Format Register

Offset: 0x8E0			Register Name: DEBE_HWC_FB_CTRL_REG
Bit	R/W	Default/Hex	Description
31:6	/	/	/
5:4	R/W	0	Y size control 00: 32pixels per line 01: 64pixels per line Other: reserved
3:2	R/W	0	X size control 00: 32pixels per row 01: 64pixels per row Other: reserved
1:0	R/W	0	Pixels format control 00: 1bpp 01: 2bpp 10: 4bpp 11: reserved

5.3.5.33. DEBE Write Back Control Register

Offset: 0x8F0			Register Name: DEBE_WB_CTRL_REG
Bit	R/W	Default/Hex	Description
31:13	/	/	/
12	R/W	0	Write back data format setting 0: ARGB (little endian syatem) 1: BGRA (little endian syatem)
11:10	/	/	/

Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

9	R/W	0	Error flag 0: 1: write back error
8	R/W	0	Write-back process status 0: write-back end or write-back disable 1: write-back in process This flag indicates that a full frame has not been written back to memory. The bit will be set when write-back enable bit is set, and be cleared when write-back process end.
7:2	/	/	/
1	R/W	0	Write back only control 0: disable the write back only control, the normal channel data of back end will transfer to LCD/TV controller too. 1: enable the write back only function, the all output data will bypass the LCD/TV controller.
0	R/W	0	Write back enable 0: Disable 1: Enable • If normal channel of back-end is selected by LCD/TV controller (write back only function is disabled), the writing back process will start when write back enable bit is set and a new frame processing begins. • The bit will be cleared when the new writing-back frame start to process.

5.3.5.34. DEBE Write Back Address Register

Offset: 0x8F4			Register Name: DEBE_WB_ADDR_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0	The start address of write back data in bits

5.3.5.35. DEBE Write Back Buffer Line Width Register

Offset: 0x8F8			Register Name: DEBE_WB_LINEWIDTH_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0	Write back image buffer line width in bits

5.3.5.36. DEBE Input YUV Channel Control Register

Offset: 0x920			Register Name: DEBE_IYUV_CTRL_REG
Bit	R/W	Default/Hex	Description
31:15	/	/	/
14:12	R/W	0	**Input data format** 000: planar YUV 411 001: planar YUV 422 010: planar YUV 444 011: interleaved YUV 422 100: interleaved YUV 444 Other: illegal

Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

11:10	/	/	/
9:8	R/W	0	**Pixel sequence** **In planar data format mode:** 00: Y3Y2Y1Y0 01: Y0Y1Y2Y3 (the other 2 components are same) Other: illegal **In interleaved YUV 422 data format mode:** 00: UYVY 01: YUYV 10: VYUY 11: YVYU **In interleaved YUV 444 data format mode:** 00: AYUV 01: VUYA Other: illegal
7:5	/	/	/
4	R/W	0	0: linner 1:
3:1	/	/	/
0	R/W	0	YUV channel enable control 0: disable 1: enable

Source data input data ports:

Input buffer channel	**Planar YUV**	**Interleaved YUV**
Channel0	Y	YUV
Channel1	U	-
Channel2	V	-

5.3.5.37. DEBE YUV Channel 0 Frame Buffer Address Register

Offset: 0x930			Register Name: DEBE_CH0_YUV_ADDR_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0	Buffer Address Frame buffer address in bits

5.3.5.38. DEBE YUV Channel 1 Frame Buffer Address Register

Offset: 0x934			Register Name: DEBE_CH1_YUV_ADDR_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0	Buffer Address Frame buffer address in bits

5.3.5.39. DEBE YUV Channel 2 Frame Buffer Address Register

Offset: 0x938			Register Name: DEBE_CH2_YUV_ADDR_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0	Buffer Address

Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Frame buffer address in bits

5.3.5.40. DEBE YUV Channel 0 Buffer Line Width Register

Offset: 0x940			Register Name: DEBE_CH0_YUV_BLW_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0	Line width The width is the distance from the start of one line to the start of the next line. Description in bits

5.3.5.41. DEBE YUV Channel 1 Buffer Line Width Register

Offset: 0x944			Register Name: DEBE_CH1_YUV_BLW_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0	Line width The width is the distance from the start of one line to the start of the next line. Description in bits

5.3.5.42. DEBE YUV Channel 2 Buffer Line Width Register

Offset: 0x948			Register Name: DEBE_CH2_YUV_BLW_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0	Line width The width is the distance from the start of one line to the start of the next line. Description in bits

YUV to RGB conversion algorithm formula:

G = (GY component coefficient * Y) + (GU component coefficient * U) + (GV component coefficient * V) + G constant
R = (RY component coefficient * Y) + (RU component coefficient * U) + (RV component coefficient * V) + R constant
B = (BY component coefficient * Y) + (BU component coefficient * U) + (BV component coefficient * V) + B constant

5.3.5.43. DEBE Coefficient 00 Register

Offset: 0x950			Register Name: DEBE_COEF00_REG
Bit	R/W	Default/Hex	Description
31:29	/	/	/
28:16	R/W	UDF	the Y/G coefficient for de-flicker the value equals to coefficient*2^{10}
15:13	/	/	/
12:0	R/W	UDF	the Y/G coefficient the value equals to coefficient*2^{10}

5.3.5.44. DEBE Coefficient 01 Register

Offset: 0x954			Register Name: DEBE_COEF01_REG
Bit	R/W	Default/Hex	Description
31:29	/	/	/

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

28:16	R/W	UDF	the U/G coefficient for de-flicker the value equals to coefficient*2^{10}
15:13	/	/	/
12:0	R/W	UDF	the U/G coefficient the value equals to coefficient*2^{10}

5.3.5.45. DEBE Coefficient 02 Register

Offset: 0x958			Register Name: DEBE_COEF02_REG
Bit	R/W	Default/Hex	Description
31:29	/	/	/
28:16	R/W	UDF	the V/G coefficient for de-flicker the value equals to coefficient*2^{10}
15:13	/	/	/
12:0	R/W	UDF	the V/G coefficient the value equals to coefficient*2^{10}

5.3.5.46. DEBE Coefficient 03 Register

Offset: 0x95C			Register Name: DEBE_COEF03_REG
Bit	R/W	Default/Hex	Description
31:29	/	/	/
28:16	R/W	UDF	the Y/G constant for de-flicker the value equals to coefficient*2^{4}
15:13	/	/	/
12:0	R/W	UDF	the Y/G constant the value equals to coefficient*2^{4}

5.3.5.47. DEBE Coefficient 10 Register

Offset: 0x960			Register Name: DEBE_COEF10_REG
Bit	R/W	Default/Hex	Description
31:29	/	/	/
28:16	R/W	UDF	The Y/R coefficient for de-flicker the value equals to coefficient*2^{10}
15:13	/	/	/
12:0	R/W	UDF	the Y/R coefficient the value equals to coefficient*2^{10}

5.3.5.48. DEBE Coefficient 11 Register

Offset: 0x964			Register Name: DEBE_COEF11_REG
Bit	R/W	Default/Hex	Description
31:29	/	/	/
28:16	R/W	UDF	the U/R coefficient for de-flicker the value equals to coefficient*2^{10}
15:13	/	/	/
12:0	R/W	UDF	the U/R coefficient

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			the value equals to coefficient*2^{10}

5.3.5.49. DEBE Coefficient 12 Register

Offset: 0x968			Register Name: DEBE_COEF12_REG
Bit	R/W	Default/Hex	Description
31:29	/	/	/
28:16	R/W	UDF	the V/R coefficient for de-flicker the value equals to coefficient*2^{10}
15:13	/	/	/
12:0	R/W	UDF	the V/R coefficient the value equals to coefficient*2^{10}

5.3.5.50. DEBE Coefficient 13 Register

Offset: 0x96C			Register Name: DEBE_COEF13_REG
Bit	R/W	Default/Hex	Description
31:29	/	/	/
28:16	R/W	UDF	the Y/R constant for de-flicker the value equals to coefficient*2^{4}
15:13	/	/	/
12:0	R/W	UDF	the U/R constant the value equals to coefficient*2^{4}

5.3.5.51. DEBE Coefficient 20 Register

Offset: 0x970			Register Name: DEBE_COEF20_REG
Bit	R/W	Default/Hex	Description
31:29	/	/	/
28:16	R/W	UDF	The Y/B coefficient for de-flicker the value equals to coefficient*2^{10}
15:13	/	/	/
12:0	R/W	UDF	the Y/B coefficient the value equals to coefficient*2^{10}

5.3.5.52. DEBE Coefficient 21 Register

Offset: 0x974			Register Name: DEBE_COEF21_REG
Bit	R/W	Default/Hex	Description
31:29	/	/	/
28:16	R/W	UDF	the U/B coefficient for de-flicker the value equals to coefficient*2^{10}
15:13	/	/	/
12:0	R/W	UDF	the U/B coefficient the value equals to coefficient*2^{10}

5.3.5.53. DEBE Coefficient 22 Register

Offset: 0x978	Register Name: DEBE_COEF22_REG

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	R/W	Default/Hex	Description
31:29	/	/	/
28:16	R/W	UDF	the V/B coefficient for de-flicker the value equals to coefficient*2^{10}
15:13	/	/	/
12:0	R/W	UDF	the V/B coefficient the value equals to coefficient*2^{10}

5.3.5.54. DEBE Coefficient 23 Register

Offset: 0x97C			Register Name: DEBE_COEF23_REG
Bit	R/W	Default/Hex	Description
31:29	/	/	/
28:16	R/W	UDF	the Y/B constant for de-flicker the value equals to coefficient*2^{4}
15:13	/	/	/
12:0	R/W	UDF	the Y/B constant the value equals to coefficient*2^{4}

5.3.5.55. DEBE HWC Pattern Memory Block

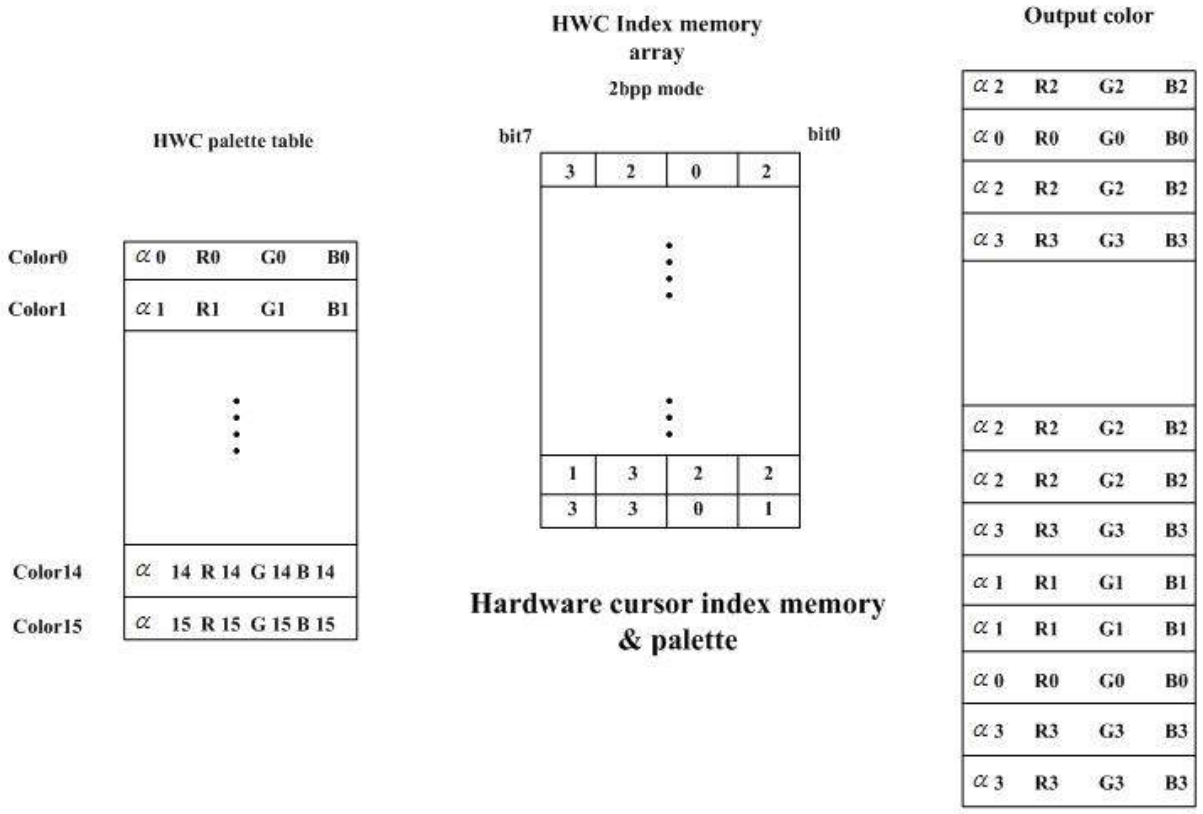
Offset: 0x1400-0x15FF			DEBE_HWC_ PAT_MEM_BLK
Bit	R/W	Default/Hex	Description
31:0	R/W	UDF	Hardware cursor pixel pattern Specify the color displayed for each of the hardware cursor pixels.

5.3.5.56. DEBE HWC Palette Table

Offset: 0x1600-0x163F			DEBE_HWC_ PALETTE_TABLE
Bit	R/W	Default/Hex	Description
31:24	R/W	0	Alpha value
23:16	R/W	0	Red value
15:8	R/W	0	Green value
7:0	R/W	0	Blue value

The follow figure (only with 2bpp mode) shows the RAM array used for hardware cursor palette lookup and the corresponding colors output.

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.



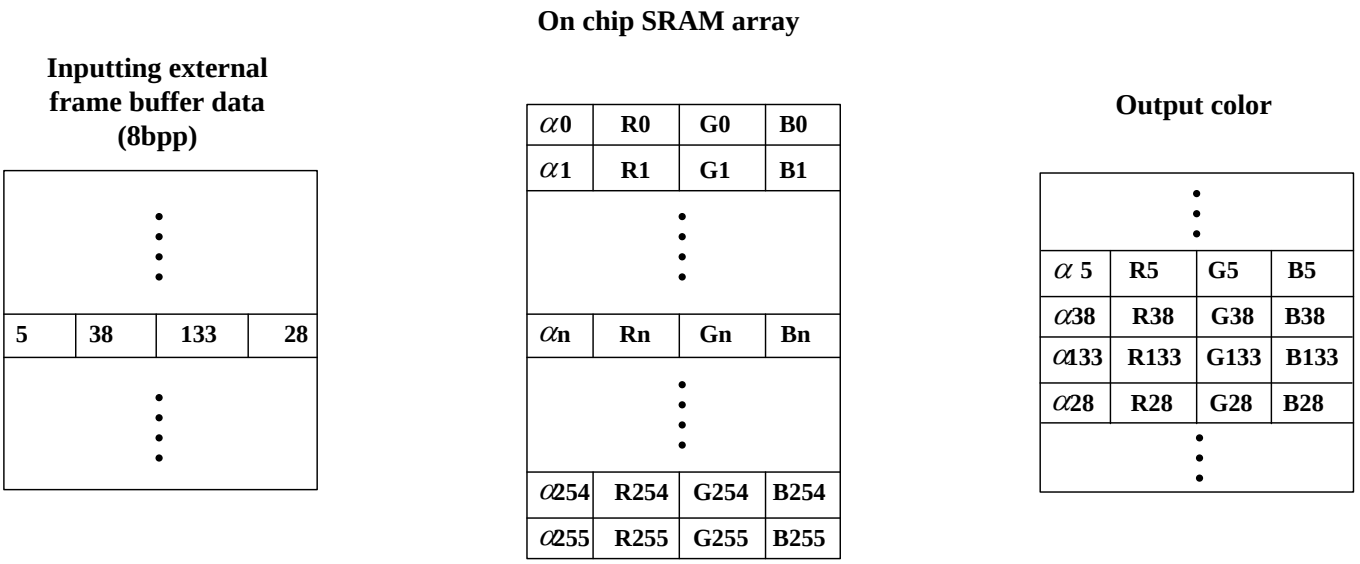
5.3.5.57. Palette Mode

Offset: 0x1000-0x13FF			DEBE_SRAM_BLK
Bit	R/W	Default/Hex	Description
31:24	R/W	UDF	Alpha value
23:16	R/W	UDF	Red value
15:8	R/W	UDF	Green value
7:0	R/W	UDF	Blue value

In this mode, RAM array is used for palette lookup table; each pixel in the layer frame buffer is treated as an index into the RAM array to select the actual color.

The follow figure shows the RAM array used for palette lookup and the corresponding colors output.

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.



On chip SRAM for palette lookup

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

5.4. De-interlacer

5.4.1. Overview

The De-interlacer converts the interlaced input video frame to a progressive one. The frame base on top field will be processed.

5.4.2. Feature

The De-interlacer includes the following features:

- Support planar UV combined YUV420 and tile-based UV combined YUV420 input format
- Support planar UV combined YUV420 output format
- Support input size up to 720×576

5.4.3. De-interlacer Register List

Module Name	Base Address
DI	0x01E70000

Register Name	Offset	Description
DI_CTRL_REG	0x000	DI Control Register
DI_INT_CTRL_REG	0x004	DI Interrupt Control Register
DI_STATUS_REG	0x008	DI Status Register
DI_SIZE_SET_REG	0x010	DI Size Setting Register
DI_FORMAT_SET _REG	0x014	DI Format Setting Register
DI_INPUT_LS0_SET _REG	0x020	DI input Line Stride 0 Setting Register
DI_INPUT_LS1_SET _REG	0x024	DI Input Line Stride 1 Setting Register
DI_OUTPUT_LS0_SET _REG	0x028	DI Output Line Stride 0 Setting Register
DI_OUTPUT_LS1_SET _REG	0x02C	DI Output Line Stride 1 Setting Register
DI_FLAG_LS_SET _REG	0x030	DI Flag Line Stride Setting Register
DI_CUR_FRAME_ADDR0_REG	0x040	DI Current Frame Address 0 Register
DI_CUR_FRAME_ADDR1_REG	0x044	DI Current Frame Address 1 Register
DI_PREFRAME_ADDR0_REG	0x050	DI Pre-frame Address 0 Register
DI_PREFRAME_ADDR1_REG	0x054	DI Pre-frame Address 1 Register
DI_OUTPUT_FRAME_ADDR0_REG	0x060	DI Output Frame Address 0 Register
DI_OUTPUT_FRAME_ADDR1_REG	0x064	DI Output Frame Address 1 Register
DI_FLAG_ADDR_REG	0x070	DI Motion Flag Address Register
DI_PARA_REG	0x080	DI Parameters Register

5.4.4. De-interlacer Register Description

5.4.4.1. DI Control Register

Offset: 0x000			Register Name: DI_CTRL_REG
Bit	R/W	Default/Hex	Description

Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

31	R/W	0x0	RESET Module reset 0: Do nothing or reset finished. 1: Reset module. Module will reset when write 1 to this bit. The **START** bit and **DI_INT_CTRL_REG** will be initialed to default value, and the state machine of the module will reset. This bit would self clear when reset finished.
30:1	/	/	/
0	R/W	0x0	START Start de-interlacing function 0: Start finish 1: Start one frame de-interlacing Write 1 will start one frame de-interlacing process. The bit would self clear when one frame de-interlacing process starts.

5.4.4.2. DI Interrupt Control Register

Offset: 0x004			Register Name: DI_INT_CTRL_REG
Bit	R/W	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	FINISH_INT_EN De-interlacing finish interrupt enable 0: Disable 1: Enable

5.4.4.3. DI Status Register

Offset: 0x008			Register Name: DI_STATUS_REG
Bit	R/W	Default/Hex	Description
31	R	0x0	CUR_CHL De-interlacing current channel. 0: luma channel 1: chroma channel
30:26	/	/	/
25:16	R	0x0	CUR_LINE De-interlacing line counter. Note: Start from zero. Counter for current processing line.
15:9	/	/	/
8	R	0x0	BUSY De-interlacing process status. The bit will become 1 when a frame de-interlacing process running and will clear when process stop.
7:1	/	/	/
0	R/W	0x0	FINISH_FLAG De-interlacing finish flag. 0: Unfinished 1: Finished

Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			The bit will become 1 when a frame de-interlacing process finish. Write 1 to clear it.

5.4.4.4. DI Size Setting Register

Offset: 0x10			**Register Name: DI_SIZE_SET_REG**
Bit	R/W	Default/Hex	Description
31:26	/	/	/
25:16	R/W	0x0	HEIGHT De-interlacing height. The actual height is the register value + 1. Note: The actual height must be 2 lines aligned.
15:10	/	/	/
9:0	R/W	0x0	WIDTH De-interlacing width. The actual width is the register value + 1. Note: The actual width must be 2 pixels aligned.

5.4.4.5. DI Format Setting Register

Offset: 0x014			Register Name: DI_FORMAT_SET_REG
Bit	R/W	Default/Hex	Description
31:5	/	/	/
4	R/W	0x0	PS_REVERSION Pixel sequence reversion enable 0: Disable. 1: Enable.
3:1	/	/	/
0	R/W	0x0	IN_FORMAT Input format 0: Non-tile-based UV combined. 1: Tile-based UV combined. (32 x 32)

5.4.4.6. DI Input Line Stride 0 Setting Register

Offset: 0x020			Register Name: DI_INPUT_LS0_REG
Bit	R/W	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0	LS Input line stride of first plane in WORD. In tile-based type The stride length is the distance from the start of the end line in one tile to the start of the first line in vertical direction next tile. In non-tile-based type The stride length is the distance from the start of one line to the start of the next line.

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

5.4.4.7. DI Input Line Stride 1 Setting Register

Offset: 0x024			Register Name: DI_INPUT_LS1_SET_REG
Bit	R/W	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0	LS Input line stride of second plane in WORD. In tile-based type The stride length is the distance from the start of the end line in one tile to the start of the first line in vertical direction next tile. In non-tile-based type The stride length is the distance from the start of one line to the start of the next line.

5.4.4.8. DI Output Line Stride 0 Setting Register

Offset: 0x028			Register Name: DI_OUTPUT_LS0_SET_REG
Bit	R/W	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0	LS Output line stride of first plane in WORD. The stride length is the distance from the start of one line to the start of the next line.

5.4.4.9. DI Output Line Stride 1 Setting Register

Offset: 0x02C			Register Name: DI_OUTPUT_LS1_SET_REG
Bit	R/W	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0	LS Output line stride of second plane in WORD. The stride length is the distance from the start of one line to the start of the next line.

5.4.4.10. DI Flag Line Stride Setting Register

Offset: 0x030			Register Name: DI_FLAG_LS_SET_REG
Bit	R/W	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0	LS Flag line stride in WORD. The stride length is the distance from the start of one line to the start of the next line.

5.4.4.11. DI Current Frame Address 0 Register

Offset: 0x040			Register Name: DI_CUR_FRAME_ADDR0_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0x0	ADDR Start address of first plane in BYTE.

Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Note: When input format is tile-based type, frame start address must be a tile start address.

5.4.4.12. DI Current Frame Address 1 Register

Offset: 0x044			Register Name: DI_CUR_FRAME_ADDR1_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0x0	ADDR Start address of second plane in BYTE. Note: When input format is tile-based type, frame start address must be a tile start address.

5.4.4.13. DI Pre-frame Address 0 Register

Offset: 0x050			Register Name: DI_PREFRAME_ADDR0_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0x0	ADDR Start address of first plane in BYTE. Note: When input format is tile-based type, frame start address must be a tile start address.

5.4.4.14. DI Pre-frame Address 1 Register

Offset: 0x054			Register Name: DI_PREFRAME_ADDR1_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0x0	ADDR Start address of second plane in BYTE. Note: When input format is tile-based type, frame start address must be a tile start address.

5.4.4.15. DI Output Frame Address 0 Register

Offset: 0x060			Register Name: DI_OUTPUT_FRAME_ADDR0_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0x0	ADDR Start address of first plane in BYTE. Note: Must word-aligned.

5.4.4.16. DI Output Frame Address 1 Register

Offset: 0x064			Register Name: DI_OUTPUT_FRAME_ADDR1_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0x0	ADDR Start address of second plane in BYTE. Note: Must word-aligned.

5.4.4.17. DI Flag Address Register

Offset: 0x070			Register Name: DI_FLAG_ADDR_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0x0	ADDR

Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Start address in BYTE.

5.4.4.18. DI Parameters Register

Offset: 0x080			Register Name: DI_PARA_REG
Bit	R/W	Default/Hex	Description
31:24	R/W	0x5	CHROMA_DIFF_TH
23:16	R/W	0xa	SPATIAL_TH2
15:8	R/W	0x6	AVG_LUMA_SHIFTER
7:0	R/W	0x9	MIN_LUMA_TH

Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

Chapter 6. Image Subsystem

This chapter describes the F1C200s image subsystem:

- CSI

6.1. CSI

6.1.1. Overview

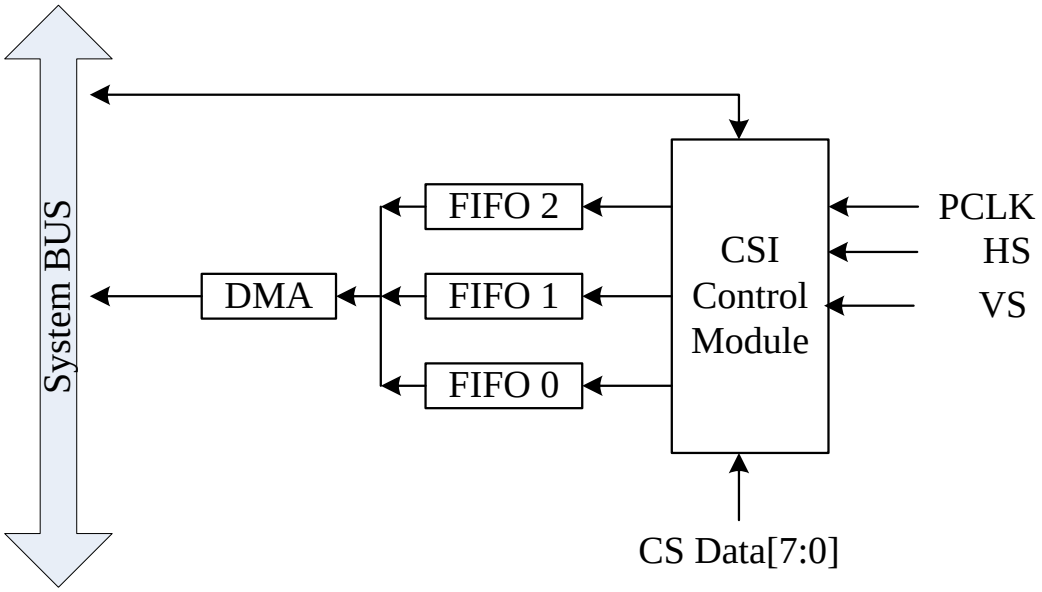
The CSI is a parallel CMOS sensor interface that can receive data input from CMOS Sensor or the NTSC/PAL image system.

6.1.2. Feature

The CSI module includes the following features:

- 8 bits input data
- Support CCIR656 protocol for NTSC and PAL
- 3 parallel data paths for image stream parsing
- Support Received data double buffer
- Parsing bayer data into planar R, G, B output to memory
- Parsing interlaced data into planar or MB Y, Cb, Cr output to memory
- Pass raw data direct to memory
- All data transmit timing can be adjusted by software
- Luminance statistical value

6.1.3. Block Diagram

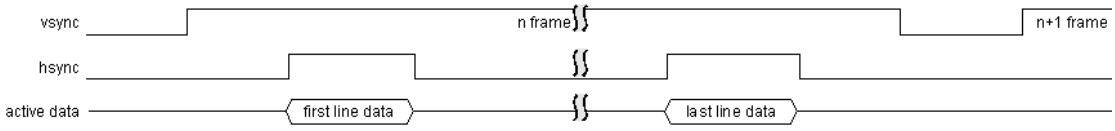


 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

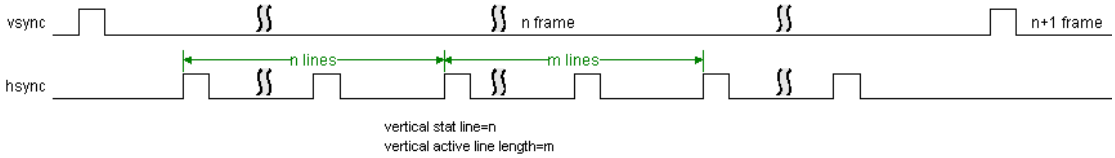
6.1.4. CSI Data Port

FIFO	Bayer	YCbCr (YUV)	Interlaced	Pass-through
FIFO0	Red pixel data	Y pixel data	All field 1 pixel data	All pixel data
FIFO1	Green pixel data	Cb (U) pixel data	All field 2 pixel data	-
FIFO2	Blue pixel data	Cr (V) pixel data	-	-

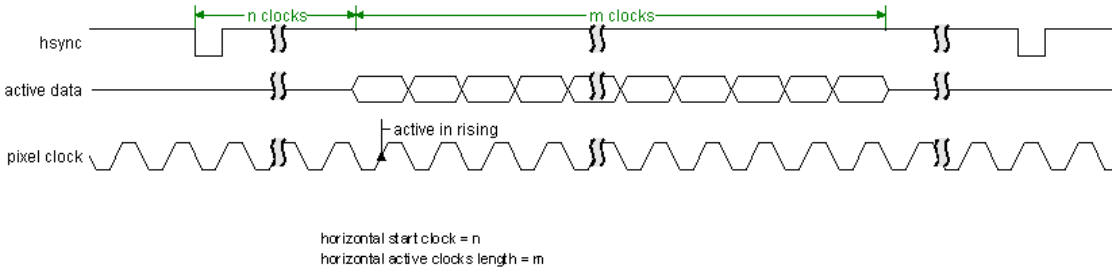
6.1.5. Timing



Vref= positive, Href= positive



Vertical size setting



Horizontal size setting and pixel clock timing (Href= positive)

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

6.1.6. CSI Register List

Module Name	Base Address
CSI	0x01CB0000

Register Name	Offset	Description
CSI_EN_REG	0x000	CSI Enable Register
CSI_CFG_REG	0x004	CSI Configuration Register
CSI_CAP_REG	0x008	CSI Capture Control Register
CSI_SCALE_REG	0x00C	CSI Scale Register
CSI_FIFO0_BUFA_REG	0x010	CSI FIFO 0 Output Buffer A Address Register
CSI_ FIFO0_BUFB_REG	0x014	CSI FIFO 0 Output Buffer B Address Register
CSI_ FIFO1_BUFA_REG	0x018	CSI FIFO 1 Output Buffer A Address Register
CSI_ FIFO1_BUFB_REG	0x01C	CSI FIFO 1 Output Buffer B Address Register
CSI_ FIFO2_BUFA_REG	0x020	CSI FIFO 2 Output Buffer A Address Register
CSI_ FIFO2_BUFB_REG	0x024	CSI FIFO 2 Output Buffer B Address Register
CSI_BUF_CTL_REG	0x028	CSI Output Buffer Control Register
CSI_BUF_STA_REG	0x02C	CSI Status Register
CSI_INT_EN_REG	0x030	CSI Interrupt Enable Register
CSI_INT_STA_REG	0x034	CSI Interrupt Status Register
CSI_HSIZE_REG	0x040	CSI Horizontal Size Register
CSI_VSIZE_REG	0x044	CSI Vertical Size Register
CSI_BUF_LEN_REG	0x048	CSI Line Buffer Length Register

6.1.7. CSI Register Description

6.1.7.1. CSI Enable Register

Offset: 0x000			Register Name: CSI_EN_REG
Bit	R/W	Default/Hex	Description
31:1	/	/	/
0	R/W	0	CSI_EN Enable 0: Reset and disable the CSI module 1: Enable the CSI module

6.1.7.2. CSI Configuration Register

Offset: 0x004			Register Name: CSI_CFG_REG
Bit	R/W	Default/Hex	Description
31:23	/	/	/
22:20	R/W	3	INPUT_FMT Input data format 000: RAW stream

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			001: reserved 010: CCIR656 (one channel) 011: YUV422 others: reserved
19:16	R/W	0	OUTPUT_FMT Output data format When the input format is set RAW stream 0000: pass-throug When the input format is set CCIR656 interface 0000: field planar YCbCr 422 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: frame planar YCbCr 422 0100: field planar YCbCr 422 UV combined 0101: field planar YCbCr 420 UV combined 0110: frame planar YCbCr 420 UV combined 0111: frame planar YCbCr 422 UV combined 1111: interlaced interleaved YCbCr422. In this mode, capturing interlaced input and output the interlaced fields from individual ports. Field 1 data will be written to FIFO0 output buffer and field 2 data will be wrote to FIFO1 output buffer. 1000: field MB YCbCr 422 1001: field MB YCbCr 420 1010: frame MB YCbCr 420 1011: frame MB YCbCr 422 When the input format is set YUV422 0000: planar YUV 422 0001: planar YUV 420 0100: planar YUV 422 UV combined 0101: planar YUV 420 UV combined 1000: MB YUV 422 1001: MB YUV 420
15:12	/	/	/
11:10	R/W	0	FIELD_SEL Field selection. Applies to CCIR656 interface only. 00: start capturing with field 1. 01: start capturing with field 2. 10: start capturing with either field. 11: reserved
9:8	R/W	2	INPUT_SEQ Input data sequence, only valid for ~~Bayer mode and~~ YUV422 mode. 00: YUYV 01: YVYU 10: UYVY 11: VYUY

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

7:3	/	/	/
2	R/W	1	VREF_POL Vref polarity 0: negative 1: positive This register is not apply to CCIR656 interface.
1	R/W	0	HERF_POL Href polarity 0: negative 1: positive This register is not applied to CCIR656 interface.
0	R/W	1	CLK_POL Data clock type 0: active in falling edge 1: active in rising edge

6.1.7.3. CSI Capture Control Register

Offset: 0x008			Register Name: CSI_CAP_REG
Bit	R/W	Default/Hex	Description
31:2	/	/	/
1	R/W	0	VCAP_ON Video capture control: Capture the video image data stream. 0: Disable video capture If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is wrote to output FIFO. 1: Enable video capture The CSI starts capturing image data at the start of the next frame.
0	W	0	SCAP_ON Still capture control: Capture a single still image frame. 0: Disable still capture. 1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self clearing and always reads as a 0.

6.1.7.4. CSI Scale Register

Offset: 0x00C			Register Name: CSI_SCALE_REG
Bit	R/W	Default/Hex	Description
31:28	/	/	/
27:24	R/W	0xF	VER_MASK Vertical (line) mask. Every 4-line is a mask group. Bit 24 mask the first line, bit 25 mask the second line, and so on. Mask bit = 0 means discarding this line data.
23:16	/	/	/

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

15:0	R/W	0xFFFF	HOR_MASK Horizontal (data stream) mask. Every 16-byte is a mask group. Bit 0 mask the first byte; bit 1 mask the second byte, and so on. Mask bit = 0 means discarding this byte from the data stream.

6.1.7.5. CSI FIFO 0 Output Buffer A Address Register

Offset: 0x010			Register Name: CSI_FIFO0_BUFA_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0	FIFO0_BUFA FIFO 0 output buffer-A address

6.1.7.6. CSI FIFO 0 Output Buffer B Address Register

Offset: 0x014			Register Name: CSI_FIFO0_BUFB_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0	FIFO0_BUFB FIFO 0 output buffer-B address

6.1.7.7. CSI FIFO 1 Output Buffer A Address Register

Offset: 0x018			Register Name: CSI_FIFO1_BUFA_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0	FIFO1_BUFA FIFO 1 output buffer-A address

6.1.7.8. CSI FIFO 1 Output Buffer B Address Register

Offset: 0x01C			Register Name: CSI_FIFO1_BUFB_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0	FIFO1_BUFB FIFO 1 output buffer-B address

6.1.7.9. CSI FIFO 2 Output Buffer A Address Register

Offset: 0x020			Register Name: CSI_FIFO2_BUFA_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0	FIFO2_BUFA FIFO 2 output buffer-A address

6.1.7.10. CSI FIFO 2 Output Buffer B Address Register

Offset: 0x024			Register Name: CSI_FIFO2_BUFB_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0	FIFO2_BUFB FIFO 2 output buffer-B address

6.1.7.11. CSI Output Buffer Control Register

Offset: 0x028			Register Name: CSI_BUF_CTRL_REG
Bit	R/W	Default/Hex	Description
31:3	/	/	/

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

2	R/W	0	DBN Buffer selected at next storing for CSI 0: Next buffer selection is buffer-A 1: Next buffer selection is buffer-B
1	R	0	DBS output buffer selected status 0: Selected output buffer-A 1: Selected output buffer-B
0	R/W	0	DBE Double buffer mode enable 0: disable 1: enable If the double buffer mode is disabled, the buffer-A will be always selected by CSI module.

6.1.7.12. CSI Status Register

Offset: 0x02C			Register Name: CSI_BUF_STA_REG
Bit	R/W	Default/Hex	Description
31:8	R	0	LUM_STATIS luminance statistical value When frame done interrupt flag come, value is ready and will last until next frame done. For raw data, value = (G>>1+R+G)>>8 For yuv422, value = Y>>8
7:2	/	/	/
1	R	0	VCAP_STA Video capture in progress Indicates the CSI is capturing video image data (multiple frames). The bit is set at the start of the first frame after enabling video capture. When software disables video capture, it clears itself after the last pixel of the current frame is captured.
0	R	0	SCAP_STA Still capture in progress Indicates the CSI is capturing still image data (single frame). The bit is set at the start of the first frame after enabling still frame capture. It clears itself after the last pixel of the first frame is captured. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means filed end.

6.1.7.13. CSI Interrupt Enable Register

Offset: 0x030			Register Name: CSI_INT_EN_REG
Bit	R/W	Default/Hex	Description
31:08	/	/	/
7	R/W	0	VS_INT_EN

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			vsync flag The bit is set when vsync come. And at this time load the buffer address for the coming frame. So after this irq come, change the buffer address could only effect next frame
6	R/W	0	HB_OF_INT_EN Hblank FIFO overflow The bit is set when 3 FIFOs still overflow after the hblank.
5	/	/	/
4	R/W	0	FIFO2_OF_INT_EN FIFO 2 overflow The bit is set when the FIFO 2 become overflow.
3	R/W	0	FIFO1_OF_INT_EN FIFO 1 overflow The bit is set when the FIFO 1 become overflow.
2	R/W	0	FIFO0_OF_INT_EN FIFO 0 overflow The bit is set when the FIFO 0 become overflow.
1	R/W	0	FD_INT_EN Frame done Indicates the CSI has finished capturing an image frame. Applies to video capture mode. The bit is set after each completed frame capturing data is written to buffer as long as video capture remains enabled.
0	R/W	0	CD_INT_EN Capture done Indicates the CSI has completed capturing the image data. For still capture, the bit is set when one frame data has been wrote to buffer. For video capture, the bit is set when the last frame has been written to buffer after video capture has been disabled. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means field end.

6.1.7.14. CSI Interrupt Status Register

Offset: 0x034			Register Name: CSI_INT_STA_REG
Bit	R/W	Default/Hex	Description
31:8	/	/	/
7	R/W	0	VS_PD vsync flag
6	R/W	0	HB_OF_PD Hblank FIFO overflow
5	/	/	/
4	R/W	0	FIFO2_OF_PD FIFO 2 overflow
3	R/W	0	FIFO1_OF_PD

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			FIFO 1 overflow
2	R/W	0	FIFO0_OF_PD FIFO 0 overflow
1	R/W	0	FD_PD Frame done
0	R/W	0	CD_PD Capture done

6.1.7.15. CSI Horizontal Size Register

Offset: 0x040			Register Name: CSI_HSIZE_REG
Bit	R/W	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0x500	HOR_LEN Horizontal pixel clock length. Valid pixel clocks of a line.
15:13	/	/	/
12:0	R/W	0	HOR_START Horizontal pixel clock start. Pixel data is valid from this clock.

6.1.7.16. CSI Vertical Size Register

Offset: 0x044			Register Name: CSI_VSIZE_REG
Bit	R/W	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0x1E0	VER_LEN Vertical line length. Valid line number of a frame.
15:13	/	/	/
12:0	R/W	0	VER_START Vertical line start. Data is valid from this line.

6.1.7.17. CSI Buffer Length Register

Offset: 0x048			Register Name: CSI_BUF_LEN_REG
Bit	R/W	Default/Hex	Description
31:13	/	/	/
12:0	R/W	0x280	BUF_LEN Buffer length of a line. Unit is byte. It is the max of the 3 FIFOs.

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

Chapter 7. Interfaces

This chapter describes the F1C200s interfaces, including:

- SD/MMC Interface
- TWI
- SPI
- UART
- RSB
- CIR Receiver
- USB-OTG
- Digital Audio Interface
- OWA Interface

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

7.1. SD/MMC Interface

7.1.1. Overview

The SD/MMC controller can be configured either as a Secure Digital Multimedia Card controller, which simultaneously supports Secure Digital memory (SD Memory), UHS-1 Card, Secure Digital I/O (SDIO), Multimedia Cards (MMC), eMMC Card.

7.1.2. Feature

The SD/MMC controller includes the following features:

- Support secure digital memory protocol commands (up to SD2.0)
- Support secure digital I/O protocol commands (up to SDIO2.0)
- Support multimedia card protocol commands (up to eMMC4.41)
- Support one SD (Verson1.0 to 2.0) or MMC (version 3.3 to eMMC4.41)
- Support hardware CRC generation and error detection
- Support host pull-up control
- Support SDIO interrupts in 1-bit and 4-bit modes
- Support SDIO suspend and resume operation
- Support SDIO read wait
- Support block size of 1 to 65535 bytes
- Support descriptor-based internal DMA controller
- Internal 128 bytes FIFO for data transfer
- Support 3.3V IO pad

7.1.3. SD/MMC Timing

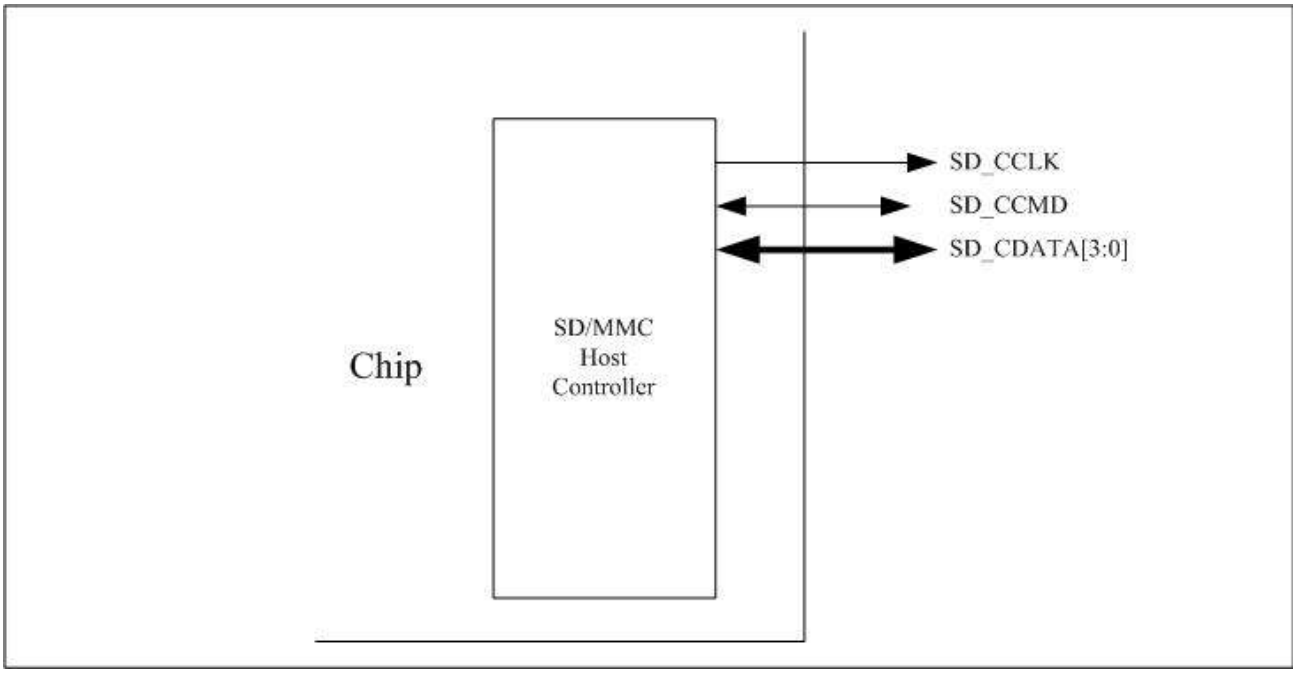
Please refer to relative specifications:

- Physical Layer Specification Ver2.00 Final
- SDIO Specification Ver2.00
- Multimedia Cards (MMC – version 4.2)
- JEDEC Standard – JESD84-44, EMBEDDED MULTI-MEDIA CARD (eMMC), ELECTRICAL STANDARD

7.1.4. SD/MMC Pin List

Port Name	Width	Direction	Description
SD_CCLK	1	OUT	Clock output for SD/SDIO/MMC card
SD_CCMD	1	IN/OUT	CMD line
SD_CDATA	4	IN/OUT	Data line

Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.



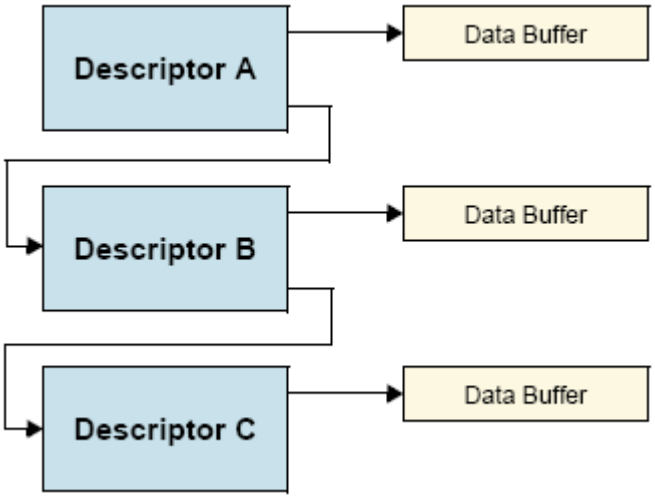
SD/MMC Pin Diagram

7.1.5. SD/MMC DMA Controller Description

SD2.0 controller has an internal DMA controller (IDMAC) to transfer data between host memory and SDMMC port. With a descriptor, IDMAC can efficiently move data from source to destination by automatically loading next DMA transfer arguments, which need less CPU intervention. Before transfer data in IDMAC, host driver should construct a descriptor list, configure arguments of every DMA transfer, then launch the descriptor and start the DMA. IDMAC has an interrupt controller, when enabled, it can interrupt the HOST CPU in situations such as data transmission completed or some errors happened.

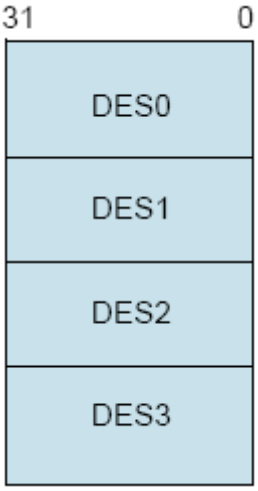
7.1.5.1. IDMAC Descriptor Structure

The IDMAC uses a descriptor with a chain structure, and each descriptor points to a unique buffer and the next descriptor.



 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

This figure illustrates the internal formats of a descriptor. The descriptor addresses must be aligned to the bus width used for 32-bit buses. Each descriptor contains 16 bytes of control and status information.



DES0 is a notation used to denote the [31:0] bits, DES1 to denote [63:32] bits, DES2 to denote [95:64]bits, and DES3 to denote [127:96]bits in a descriptor.

7.1.5.2. DES0 Definition

Bits	Name	Descriptor
31	HOLD	DES_OWN_FLAG When set, this bit indicates that the descriptor is owned by the IDMAC. When this bit is reset, it indicates that the descriptor is owned by the host. This bit is cleared when transfer is over.
30	ERROR	ERR_FLAG When some error happened in transfer, this bit will be set.
29:5	/	/
4	Chain Flag	CHAIM_MOD When set, this bit indicates that the second address in descriptor is the next descriptor address. Must be set 1.
3	First DES Flag	FIRST_FLAG When set, this bit indicates that this descriptor contains the first buffer of data. Must be set to 1 in first DES.
2	Last DES Flag	LAST_FLAG When set, this bit indicates that the buffers pointed to by this descriptor are the last data buffer
1	Disable Interrupt on completion	CUR_TXRX_OVER_INT_DIS When set, this bit will prevent the setting of the TX/RX interrupt bit of the IDMAC status register for data that ends in the buffer pointed to by this descriptor
0	/	/

7.1.5.3. DES1 Definition

Bits	Name	Descriptor

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

31:13	/	/
12:0	Buffer size	BUFF_SIZE These bits indicate the data buffer byte size, which must be a multiple of 4 bytes. If this filed is 0, the DMA ignores this buffer and proceeds to the next descriptor.

7.1.5.4. DES2 Definition

Bits	Name	Descriptor
31:0	Buffer address pointer	BUFF_ADDR these bits indicate the physical address of data buffer. The IDMAC ignores DES2[1:0], corresponding to the bus width of 32.

7.1.5.5. DES3 Definition

Bits	Name	Descriptor
31:0	Next descriptor address	NEXT_DESP_ADDR These bits indicate the pointer to the physical memory where the next descriptor is present.

7.1.6. SD/MMC Register List

Module Name	Base Address
SDC0	0x01C0F000
SDC1	0x01C10000

Register Name	Offset	Description
SD_GCTL_REG	0x000	SD Control Register
SD_CKCR_REG	0x004	SD Clock Control Register
SD_TMOR_REG	0x008	SD Time Out Register
SD_BWDR_REG	0x00C	SD Bus Width Register
SD_BKSR_REG	0x010	SD Block size Register
SD_BYCR_REG	0x014	SD Byte Count Register
SD_CMDR_REG	0x018	SD Command Register
SD_CAGR_REG	0x01C	SD Command Argument Register
SD_RESP0_REG	0x020	SD Response Register 0
SD_RESP1_REG	0x024	SD Response Register 1
SD_RESP2_REG	0x028	SD Response Register 2
SD_RESP3_REG	0x02C	SD Response Register 3
SD_IMKR_REG	0x030	SD Interrupt Mask Register
SD_MISR_REG	0x034	SD Masked Interrupt Status Register
SD_RISR_REG	0x038	SD Raw Interrupt Status Register
SD_STAR_REG	0x03C	SD Status Register
SD_FWLR_REG	0x040	SD FIFO Water Level Register
SD_FUNS_REG	0x044	SD FIFO Function Select Register
SD_CBCR_REG	0x048	SD Transferred CIU Card Byte Count Register

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

SD_BBCR_REG	0x04C	SD Transferred Host To BIU-FIFO Byte Count Register
SD_DBGC_REG	0x050	SD Current Debug Control Address Register
SD_A12A_REG	0x058	SD Auto Command 12 Argument Register
SD_HWRST_REG	0x078	SD Hardware Reset Register
SD_DMAC_REG	0x080	SD BUS Mode Control Register
SD_DLBA_REG	0x084	SD Descriptor List Base Address Register
SD_IDST_REG	0x088	SD DMAC Status Register
SD_IDIE_REG	0x08C	SD DMAC Interrupt Enable Register
SD_CHDA_REG	0x090	SD Current Host Descriptor Address Register
SD_CBDA_REG	0x094	SD Current Buffer Descriptor Address Register
CARD_THLDC_REG	0x100	Card Threshold Control Register
EMMC_DSBD_REG	0x10C	EMMC4.5 DDR Start Bit Detection Control Register
SD_FIFO_REG	0x200	SD FIFO Register

7.1.7. SD/MMC Register Description

7.1.7.1. SD Global Control Register

Offset: 0x000			Register Name: SD_CTRL_REG
Bit	R/W	Default/Hex	Description
31	R/W	0	FIFO_AC_MOD FIFO Access Mode 1-AHB bus 0-DMA bus
30:11	/	/	/
10	R/W	0	DDR_MOD_SEL DDR Mode Select 0 – SDR mode 1 – DDR mode
9	/	/	/
8	R/W	1	CD_DBC_ENB Card Detect (Data[3] status) de-bounce Enable 0 - disable de-bounce 1 – enable de-bounce
7:6	/	/	/
5	R/W	0	DMA_ENB DMA Global Enable 0 – Disable DMA to transfer data, using AHB bus 1 – Enable DMA to transfer data
4	R/W	0	INT_ENB Global Interrupt Enable 0 – Disable interrupts 1 – Enable interrupts
3	/	/	/
2	R/W	0	DMA_RST

Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			DMA Reset
1	R/W	0	FIFO_RST FIFO Reset 0 – No change 1 – Reset FIFO *This bit is auto-cleared after completion of reset operation.*
0	R/W	0	SOFT_RST Software Reset 0 – No change 1 – Reset SD/MMC controller *This bit is auto-cleared after completion of reset operation.*

7.1.7.2. SD Clock Control Register

Offset: 0x004			Register Name: SD_CLKDIV_REG
Bit	R/W	Default/Hex	Description
31:18	/	/	/
17	R/W	0	CCLK_CTRL Card Clock Output Control 0 – Card clock always on 1 – Turn off card clock when FSM in IDLE state
16	R/W	0	CCLK_ENB Card Clock Enable 0 – Card Clock off 1 – Card Clock on
15:8	/	/	/
7:0	R/W	0	CCLK_DIV Card clock divider n – Source clock is divided by 2*n.(n=0~255)

7.1.7.3. SD Timeout Register

Offset: 0x008			Register Name: SD_TMOUT_REG
Bit	R/W	Default/Hex	Description
31:8	R/W	0xffffff	DTO_LMT Data Timeout Limit
7:0	R/W	0x40	RTO_LMT Response Timeout Limit

7.1.7.4. SD Bus Width Register

Offset: 0x00C			Register Name: SD_CTYPE_REG
Bit	R/W	Default/Hex	Description
31:2	/	/	/
1:0	R/W	0	CARD_WID Card width 2’b00 – 1-bit width 2’b01 – 4-bit width

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			2'b1x – 8-bit width

7.1.7.5. SD Block Size Register

Offset: 0x010			Register Name: SD_BLKSIZ_REG
Bit	R/W	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x200	BLK_SZ Block size

7.1.7.6. SD Byte Count Register

Offset: 0x014			Register Name: SD_BYTCNT_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0x200	BYTE_CNT Byte counter Number of bytes to be transferred; should be integer multiple of Block Size for block transfers.

7.1.7.7. SD Command Register

Offset: 0x018			Register Name: SD_CMD_REG
Bit	R/W	Default/Hex	Description
31	R/W	0	CMD_LOAD Start Command. This bit is auto cleared when current command is sent. If there is no any response error happened, a command complete interrupt bit (CMD_OVER) will be set in interrupt register. You should not write any other command before this bit is cleared, or a command busy interrupt bit (CMD_BUSY) will be set in interrupt register.
30	/	/	/
29	R/W	0	Use Hold Register 0 - CMD and DATA sent to card bypassing HOLD Register 1 - CMD and DATA sent to card through the HOLD Register
28	R/W	0	VOL_SW Voltage Switch 0 – normal command 1 – Voltage switch command, set for CMD11 only
27	R/W	0	BOOT_ABT Boot Abort Setting this bit will terminate the boot operation.
26	R/W	0	EXP_BOOT_ACK Expect Boot Acknowledge. When Software sets this bit along in mandatory boot operation, controller expects a boot acknowledge start pattern of 0-1-0 from the selected card.
25:24	R/W	0	BOOT_MOD Boot Mode 2'b00 – normal command

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			2'b01 - Mandatory Boot operation 2'b10 - Alternate Boot operation 2'b11 - reserved
23	R/W	0	/
22	R/W	0	/
21	R/W	0	PRG_CLK Change Clock 0 – Normal command 1 – Change Card Clock; when this bit is set, controller will change clock domain and clock output. No command will be sent.
20:16	-	-	/
15	R/W	0	SEND_INIT_SEQ Send Initialization 0 – normal command sending 1 – Send initialization sequence before sending this command.
14	R/W	0	STOP_ABT_CMD Stop Abort Command 0 – normal command sending 1 – send Stop or abort command to stop current data transfer in progress.(CMD12, CMD52 for writing "I/O Abort" in SDIO CCCR)
13	R/W	0	WAIT_PRE_OVER Wait Data Transfer Over 0 – Send command at once, do not care of data transferring 1 – Wait for data transfer completion before sending current command
12	R/W	0	STOP_CMD_FLAG Send Stop CMD Automatically (CMD12) 0 – Do not send stop command at end of data transfer 1 – Send stop command automatically at end of data transfer
11	R/W	0	TRANS_MODE Transfer Mode 0 – Block data transfer command 1 – Stream data transfer command
10	R/W	0	TRANS_DIR Transfer Direction 0 – Read operation 1 – Write operation
9	R/W	0	DATA_TRANS Data Transfer 0 – without data transfer 1 – with data transfer
8	R/W	0	CHK_RESP_CRC Check Response CRC 0 – Do not check response CRC 1 – Check response CRC
7	R/W	0	LONG_RESP

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Response Type 0 –Short Response (48 bits) 1 –Long Response (136 bits)
6	R/W	0	RESP_RCV Response Receive 0 – Command without Response 1 – Command with Response
5:0	R/W	0	CMD_IDX CMD Index Command index value

7.1.7.8. SD Command Argument Register

Offset: 0x01C			Register Name: SD_CMDARG_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0	CMD_ARG Command argument

7.1.7.9. SD Response Register 0

Offset: 0x020			Register Name: SD_RESP_REG0
Bit	R/W	Default/Hex	Description
31:0	R	0	CMD_RESP0 response 0 Bit[31:0] of response

7.1.7.10. SD Response Register 1

Offset: 0x024			Register Name: SD_RESP_REG1
Bit	R/W	Default/Hex	Description
31:0	R	0	CMD_RESP1 response 1 Bit[63:31] of response

7.1.7.11. SD Response Register 2

Offset: 0x028			Register Name: SD_RESP_REG2
Bit	R/W	Default/Hex	Description
31:0	R	0	CMD_RESP2 response 2 Bit[95:64] of response

7.1.7.12. SD Response Register 3

Offset: 0x02C			Register Name: SD_RESP_REG3
Bit	R/W	Default/Hex	Description
31:0	R	0	CMD_RESP3 response 3 Bit[127:96] of response

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

7.1.7.13. SD Interrupt Mask Register

Offset: 0x030			Register Name: SD_INTMASK_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0	INT_MASK 0 – interrupt masked 1 – interrupt enabled Bit field defined as following: bit 31– card removed bit 30 – card inserted bit 17~29 - reserved bit 16 – SDIO interrupt bit 15 – Data End-bit error bit 14 – Auto Stop Command done bit 13 – Data Start Error bit 12 – Command Busy and illegal write bit 11 – FIFO under run/overflow bit 10 – Data starvation timeout /V1.8 Switch Done bit 9 – Data timeout/Boot data start bit 8 – Response timeout/Boot ACK received bit 7 – Data CRC error bit 6 – Response CRC error bit 5 – Data Receive Request bit 4 –Data Transmit Request bit 3 – Data Transfer Complete bit 2 – Command Complete bit 1 – Response Error (no response or response CRC error) bit 0 – Reserved

7.1.7.14. SD Masked Interrupt Status Register

Offset: 0x034			Register Name: SD_MINTSTS_REG
Bit	R/W	Default/Hex	Description
31:0	R	0	MSKD_ISTA Interrupt status. Enabled only if corresponding bit in mask register is set. Bit field defined as following: bit 31 – card removed bit 30 – card inserted bit 17~29 - reserved bit 16 – SDIO interrupt bit 15 – Data End-bit error bit 14 – Auto command done bit 13 – Data Start Error bit 12 – Command Busy and illegal write bit 11 – FIFO under run/overflow bit 10 – Data starvation timeout (HTO)/V1.8 Switch Done bit 9 – Data timeout/Boot data start

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			bit 8 – Response timeout/Boot ACK received bit 7 – Data CRC error bit 6 – Response CRC error bit 5 – Data Receive Request bit 4 –Data Transmit Request bit 3 – Data Transfer Complete bit 2 – Command Complete bit 1 – Response Error (no response or response CRC error) bit 0 – Reserved

7.1.7.15. SD Raw Interrupt Status Register

Offset: 0x038			Register Name: SD_RINTSTS_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0	RAW_ISTA Raw Interrupt Status. *This is write-1-to-clear bits.* Bit field defined as following: bit 31 – card removed bit 30 – card inserted bit 17~29 - reserved bit 16 – SDIO interrupt bit 15 – Data End-bit error bit 14 – Auto command done bit 13 – Data Start Error bit 12 – Command Busy and illegal write bit 11 – FIFO under run/overflow bit 10 – Data starvation timeout (HTO)/V1.8 Switch Done bit 9 – Data timeout/Boot data start bit 8 – Response timeout/Boot ACK received bit 7 – Data CRC error bit 6 – Response CRC error bit 5 – Data Receive Request bit 4 –Data Transmit Request bit 3 – Data Transfer Complete bit 2 – Command Complete bit 1 – Response Error (no response or response CRC error) bit 0 – Reserved

7.1.7.16. SD Status Register

Offset: 0x3C			Register Name: SD_STATUS_REG
Bit	R/W	Default/Hex	Description
31	R	0	DMA_REQ dma_req DMA request signal state
30:22	/	/	/

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

21:17	R	0	FIFO_LEVEL FIFO Level Number of filled locations in FIFO
16:11	R	0	RESP_IDX Response Index Index of previous response, including any auto-stop sent by controller
10	R	0	FSM_BUSY Data FSM Busy Data transmit or receive state-machine is busy
9	R	0	CARD_BUSY Card data busy Inverted version of DATA[0] 0 – card data not busy 1 – card data busy
8	R	0	CARD_PRESENT Data[3] status level of DATA[3]; checks whether card is present 0 – card not present 1 – card present
7:4	R	0	FSM_STA Command FSM states: 0 – Idle 1 – Send init sequence 2 – Tx cmd start bit 3 – Tx cmd tx bit 4 – Tx cmd index + arg 5 – Tx cmd crc7 6 – Tx cmd end bit 7 – Rx resp start bit 8 – Rx resp IRQ response 9 – Rx resp tx bit 10 – Rx resp cmd idx 11 – Rx resp data 12 – Rx resp crc7 13 – Rx resp end bit 14 – Cmd path wait NCC 15 – Wait; CMD-to-response turnaround
3	R	0	FIFO_FULL FIFO full 1 – FIFO full 0 – FIFO not full
2	R	1	FIFO_EMPTY FIFO Empty 1 - FIFO Empty 0 - FIFO not Empty

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

1	R	1	FIFO_TX_LEVEL FIFO TX Water Level flag 0 – FIFO didn't reach transmit trigger level 1 - FIFO reached transmit trigger level
0	R	0	FIFO_RX_LEVEL FIFO TX Water Level flag 0 – FIFO didn't reach receive trigger level 1 - FIFO reached receive trigger level

7.1.7.17. SD FIFO Water Level Register

Offset: 0x040			Register Name: SD_FIFOTH_REG
Bit	R/W	Default/Hex	Description
31	/	/	/
30:28	R/W	0	BSIZE_OF_TRANS Burst size of multiple transaction 000 – 1 transfers 001 – 4 010 – 8 011 – 16 100 – 32 101 – 64 110 – 128 111 – 256 Should be programmed same as DMA controller multiple transaction size. The units for transfers are the DWORD. A single transfer would be signaled based on this value. Value should be sub-multiple of (RX_TL + 1) and (FIFO_DEPTH - TX_TL) Recommended: MSize = 8, TX_TL = 16, RX_TL = 15
27:21	R	0	/
20:16	R/W	0xF	RX_TL Rx Trigger Level 0x0~0x1e – RX Trigger Level is 0~30 0x1f – reserved FIFO threshold when FIFO request host to receive data from FIFO. When FIFO data level is greater than this value, DMA is request is raised if DMA enabled, or RX interrupt bit is set if interrupt enabled. At the end of packet, if the last transfer is less than this level, the value is ignored and relative request will be raised as usual. Recommended: 15 (means greater than 15)
15:5	R	0	/
4:0	R/W	0	TX_TL TX Trigger Level 0x1~0x1f – TX Trigger Level is 1~31 0x0 – no trigger

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			FIFO threshold when FIFO requests host to transmit data to FIFO. When FIFO data level is less than or equal to this value, DMA TX request is raised if DMA enabled, or TX request interrupt bit is set if interrupt enabled. At the end of packet, if the last transfer is less than this level, the value is ignored and relative request will be raised as usual. Recommended: 16 (means less than or equal to 16)

7.1.7.18. SD Function Select Register

Offset: 0x044			Register Name: SD_CTRL_REG
Bit	R/W	Default/Hex	Description
31:16	R/W	0	CEATA_EN CEATA Support ON/OFF 0xceaa – CEATA support on. All hidden CEATA relative bits are accessible normally and these 16 bits return value of 0x1 when be read. Other value – CEATA support off. All hidden CEATA relative bits cannot be access and these 16 bits return value of 0 when be read.
15:11	/	/	/
10	R/W	0	/
9	R/W	0	/
8	R/W	0	/
7:3	/	/	/
2	R/W	0	ABT_RDATA Abort Read Data 0 – Ignored 1 –After suspend command is issued during read-transfer, software polls card to find when suspend happened. Once suspend occurs, software sets bit to reset data state-machine, which is waiting for next block of data. Used in SDIO card suspends sequence. *This bit is auto-cleared once controller reset to idle state.*
1	R/W	0	READ_WAIT Read Wait 0 – Clear SDIO read wait 1 – Assert SDIO read wait
0	R/W	0	HOST_SEND_MMC_IRQRESQ Host Send MMC IRQ Response 0 – Ignored 1 – Send auto IRQ response When host is waiting MMC card interrupt response, setting this bit will make controller cancel wait state and return to idle state, at which time, controller will receive IRQ response sent by itself. *This bit is auto-cleared after response is sent.*

7.1.7.19. SD Transferred CIU Card Byte Count Register

Offset: 0x048			Register Name: SD_TCBCNT_REG
Bit	R/W	Default/Hex	Description

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

31:0	R	0	TRANS_BYTE_CNT_TO_CARD Number of bytes transferred by CIU unit to card. The register should be accessed in full to avoid read-coherency problems and read only after data transfer completes.

7.1.7.20. SD Transferred Host to BIU-FIFO Byte Count Register

Offset: 0x04C			Register Name: SD_TBBCNT_REG
Bit	R/W	Default/Hex	Description
31:0	R	0	TRANS_BYTE_CNT_ON_BUS Number of bytes transferred by Host/DMA memory and BIU FIFO. The register should be accessed in full to avoid read-coherency problems and read only after data transfer completes.

7.1.7.21. SD Debug Control Register

Offset: 0x050			Register Name: SD_FIFO_REG
Bit	R/W	Default/Hex	Description
31:12	-	-	/
11:0	R/W	0	DBG_ON 0xdeb – Debug on. ALL hidden register bits will be accessible and these 12 bits return 0x1 when be read. Other values – Debug off. All hidden register bits will not be accessed and these 12 bits return 0 when be read.

7.1.7.22. SD Auto Command 12 Argument Register

Offset: 0x058			Register Name: SD_A12A_REG
Bit	R/W	Default/Hex	Description
31:16	/	/	/
0:15	R/W	0xffff	SD_A12A. SD_A12A set the argument of command 12 automatically send by controller

7.1.7.23. SD Hardware Reset Register

Offset: 0x078			Register Name: SD_FIFO_REG
Bit	R/W	Default/Hex	Description
31:1	/	/	/
0	R/W	1	HW_RESET. 1 – Active mode 0 – Reset These bits cause the cards to enter pre-idle state, which requires them to be re-initialized.

7.1.7.24. SD DMAC Control Register

Offset: 0x080			Register Name: SD_BUS_MODE_REG
Bit	R/W	Default/Hex	Description
31	W	0	DES_LOAD_CTRL

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			When DMAC fetches a descriptor, if the valid bit of a descriptor is not set, DMAC FSM will go to the suspend state. Setting this bit will make DMAC re-fetch descriptor again and do the transfer normally.
10:8	R	0	PRG_BURST_LEN Programmable Burst Length. These bits indicate the maximum number of beats to be performed in one IDMAC transaction. The IDMAC will always attempt to burst as specified in PBL each time it starts a Burst transfer on the host bus. The permissible values are 1, 4, 8, 16, 32, 64, 128 and 256. This value is the mirror of MSIZE of FIFOTH register. In order to change this value, write the required value to FIFOTH register. This is an encode value as follows. 000 – 1 transfers 001 – 4 transfers 010 – 8 transfers 011 – 16 transfers 100 – 32 transfers 101 – 64 transfers 110 – 128 transfers 111 – 256 transfers Transfer unit is either 16, 32, or 64 bits, based on HDATA_WIDTH. PBL is a read-only value.
7	R/W	0	IDMAC_ENB IDMAC Enable. When set, the IDMAC is enabled. DE is read/write.
6:2	R/W	0	DES_SKIP_LEN Descriptor Skip Length. Specifies the number of Word to skip between two unchained descriptors. This is applicable only for dual buffer structure. Default value is set to 4 DWORD.
1	R/W	0	FIX_BUST_CTRL Fixed Burst. Controls whether the AHB Master interface performs fixed burst transfers or not. When set, the AHB will use only SINGLE, INCR4, INCR8 during start of normal burst transfers. When reset, the AHB will use SINGLE and INCR burst transfer operations.
0	R/W	0	IDMAC_RST DMA Reset. When set, the DMA Controller resets all its internal registers. SWR is read/write. It is automatically cleared after 1 clock cycle.

7.1.7.25. SD Descriptor List Base Address Register

Offset: 0x084			Register Name: SD_DLBA_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0	DES_BASE_ADDR

Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Start of Descriptor List. Contains the base address of the First Descriptor. The LSB bits [1:0] are ignored and taken as all-zero by the IDMAC internally. Hence these LSB bits are read-only.

7.1.7.26. SD DMAC Status Register

Offset: 0x088			Register Name: SD_DLBA_REG
Bit	R/W	Default/Hex	Description
31:17	/	/	/
16:13	R	0	DMAC_FSM_STA DMAC FSM present state. 0 – DMA_IDLE 1 – DMA_SUSPEND 2 – DESC_RD 3 – DESC_CHK 4 – DMA_RD_REQ_WAIT 5 – DMA_WR_REQ_WAIT 6 – DMA_RD 7 – DMA_WR 8 – DESC_CLOSE This bit is read-only.
12:10	R	0	DMAC_ERR_STA Error Bits. Indicates the type of error that caused a Bus Error. Valid only with Fatal Bus Error bit (IDSTS[2]) set. This field does not generate an interrupt. 3'b001 – Host Abort received during transmission 3'b010 – Host Abort received during reception Others: Reserved EB is read-only.
9	R/W	0	ABN_INT_SUM Abnormal Interrupt Summary. Logical OR of the following: IDSTS[2] – Fatal Bus Interrupt IDSTS[4] – DU bit Interrupt IDSTS[5] – Card Error Summary Interrupt Only unmasked bits affect this bit. This is a sticky bit and must be cleared each time a corresponding bit that causes AIS to be set is cleared. Writing a 1 clears this bit.
8	R/W	0	NOR_INT_SUM Normal Interrupt Summary. Logical OR of the following: IDSTS[0] – Transmit Interrupt IDSTS[1] – Receive Interrupt Only unmasked bits affect this bit. This is a sticky bit and must be cleared each time a corresponding bit that causes NIS to be set is cleared. Writing a 1 clears this bit.

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

7:6	/	/	/
5	R/W	0	ERR_FLAG_SUM Card Error Summary. Indicates the status of the transaction to/from the card; also present in RINTSTS. Indicates the logical OR of the following bits: EBE – End Bit Error RTO – Response Timeout/Boot Ack Timeout RCRC – Response CRC SBE – Start Bit Error DRTO – Data Read Timeout/BDS timeout DCRC – Data CRC for Receive RE – Response Error Writing a 1 clears this bit.
4	R/W	0	DES_UNAVL_INT Descriptor Unavailable Interrupt. This bit is set when the descriptor is unavailable due to OWN bit = 0 (DES0[31] =0). Writing a 1 clears this bit.
3	/	/	/
2	R/W	0	FATAL_BERR_INT Fatal Bus Error Interrupt. Indicates that a Bus Error occurred (IDSTS[12:10]). When this bit is set, the DMA disables all its bus accesses. Writing a 1 clears this bit.
1	R/W	0	RX_INT Receive Interrupt. Indicates the completion of data reception for a descriptor. Writing a 1 clears this bit.
0	R/W	0	TX_INT Transmit Interrupt. Indicates that data transmission is finished for a descriptor. Writing a ‘1’ clears this bit.

7.1.7.27. SD DMAC Interrupt Enable Register

Offset: 0x08C			Register Name: SD_IDIE_REG
Bit	R/W	Default/Hex	Description
31:10	/	/	/
9	R/W	0	ABN_INT_ENB Abnormal Interrupt Summary Enable. When set, an abnormal interrupt is enabled. This bit enables the following bits: IDINTEN[2] – Fatal Bus Error Interrupt IDINTEN[4] – DU Interrupt IDINTEN[5] – Card Error Summary Interrupt
8	R/W	0	NOR_INT_ENB Normal Interrupt Summary Enable. When set, a normal interrupt is enabled. When reset, a normal interrupt is

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			disabled. This bit enables the following bits: IDINTEN[0] – Transmit Interrupt IDINTEN[1] – Receive Interrupt
7:6	/	/	/
5	R/W	0	ERR_SUM_INT_ENB Card Error summary Interrupt Enable. When set, it enables the Card Interrupt summary.
4	R/W	0	DES_UNAVL_INT_ENB Descriptor Unavailable Interrupt. When set along with Abnormal Interrupt Summary Enable, the DU interrupt is enabled.
3	/	/	/
2	R/W	0	FERR_INT_ENB Fatal Bus Error Enable. When set with Abnormal Interrupt Summary Enable, the Fatal Bus Error Interrupt is enabled. When reset, Fatal Bus Error Enable Interrupt is disabled.
1	R/W	0	RX_INT_ENB Receive Interrupt Enable. When set with Normal Interrupt Summary Enable, Receive Interrupt is enabled. When reset, Receive Interrupt is disabled.
0	R/W	0	TX_INT_ENB Transmit Interrupt Enable. When set with Normal Interrupt Summary Enable, Transmit Interrupt is enabled. When reset, Transmit Interrupt is disabled.

7.1.7.28. SD Current Host Descriptor Address Register

Offset: 0x090			Register Name: SD_CHDA_REG
Bit	R/W	Default/Hex	Description
31:0	R	0	CUR_DES_ADDR Host Descriptor Address Pointer. Cleared on reset. Pointer updated by IDMAC during operation. This register points to the start address of the current descriptor read by the IDMAC.

7.1.7.29. SD Current Buffer Descriptor Address Register

Offset: 0x094			Register Name: SD_CBDA_REG
Bit	R/W	Default/Hex	Description
31:0	R	0	CUR_BUFF_ADDR Host Buffer Address Pointer. Cleared on Reset. Pointer updated by IDMAC during operation. This register points to the current Data Buffer Address being accessed by the IDMAC.

7.1.7.30. Card Threshold Control Register

Offset: 0x100			Register Name: SD_THLD_CTLR_REG
Bit	R/W	Default/Hex	Description

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

31:28	/	/	/
27:16	R/W	0	CARD_RD_THLD Card Read Threshold Size
15:1	/	/	/
0	R/W	0	CARD_RD_THLD_ENB Card Read Threshold Enable 0: Card Read Threshold Disable 1: Card Read Threshold Enable Host controller initiates Read Transfer only if CARD_RD_THLD amount of space is available in receive FIFO

7.1.7.31. EMMC4.5 DDR Start Bit Detection Control Register

Offset: 0x10C			Register Name: EMMC_DDR_SBIT_DET_REG
Bit	R/W	Default/Hex	Description
31:1	/	/	/
0	R/W	0	HALF_START_BIT Control for start bit detection mechanism inside mstorage based on duration of start bit. For eMMC 4.5, start bit can be: 0: Full cycle 1: Less than one full cycle Set HALF_START_BIT=1 for eMMC 4.5 and above; set to 0 for SD applications.

7.1.7.32. SD FIFO Register

Offset: 0x200			Register Name: SD_FIFO_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0	TX/RX_FIFO Data FIFO

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

7.2. TWI

7.2.1. Overview

This TWI Controller is designed to be used as an interface between CPU host and the serial TWI bus. It can supports all the standard TWI transfer, including Slave and Master. The communication to the TWI bus is carried out on a byte-wise basis using interrupt or polled handshaking. This TWI Controller can be operated in standard mode (100K bps) or fast-mode, supporting data rate up to 400K bps. Multiple Masters and 10-bit addressing Mode are supported for this specified application. General Call Addressing is also supported in Slave mode.

7.2.2. Feature

The TWI Controller includes the following features:

- Software-programmable for Slave or Master
- Support Repeated START signal
- Multi-master systems supported
- Allow 10-bit addressing with TWI bus
- Performs arbitration and clock synchronization
- Own address and General Call address detection
- Interrupt on address detection
- Support speeds up to 400Kbits/s (‘fast mode’)
- Allow operation from a wide range of input clock frequencies

7.2.3. Pin List

Port Name	Width	Direction	Description
TWI_SCL	1	IN/OUT	TWI Clock line
TWI_SDA	1	IN/OUT	TWI Serial Data line

7.2.4. Timing Diagram

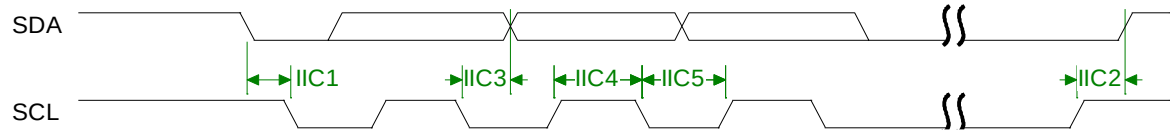
Data transferred are always in a unit of 8-bit (byte), followed by an acknowledge bit. The number of bytes that can be transmitted per transfer is unrestricted. Data is transferred in serial with the MSB first. Between each byte of data transfer, a receiver device will hold the clock line SCL low to force the transmitter into a wait state while waiting the response from microprocessor.

Data transfer with acknowledge is obligatory. The clock line is driven by the master all the time, including the acknowledge-related clock cycle, except for the SCL holding between each byte. After sending each byte, the transmitter releases the SDA line to allow the receiver to pull down the SDA line and send an acknowledge signal (or leave it high to send a "not acknowledge") to the transmitter.

When a slave receiver doesn't acknowledge the slave address (unable to receive because of no resource available), the data line must be left high by the slave so that the master can then generate a STOP condition to abort the transfer. Slave receiver can also indicate not to want to send more data during a transfer by leave the acknowledge signal high. And the master should generate the STOP condition to abort the transfer.

Below diagram provides an illustration the relation of SDA signal line and SCL signal line on the TWI serial bus.

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.



TWI Timing Diagram

7.2.5. TWI Controller Operation

There are four operation modes on the TWI bus which dictates the communications method. They are Master Transmit, Master Receive, Slave Transmit and Slave Receive. In general, CPU host controls TWI by writing commands and data to its registers. The TWI interrupts the CPU host for the attention each time a byte transfer is done or a START/STOP conditions is detected. The CPU host can also poll the status register for current status if the interrupt mechanism is not disabled by the CPU host.

When the CPU host wants to start a bus transfer, it initiates a bus START to enter the master mode by setting IM_STA bit in the 2WIRE_CNTR register to high (before it must be low). The TWI will assert INT line and INT_FLAG to indicate a completion for the START condition and each consequent byte transfer. At each interrupt, the micro-processor needs to check the 2WIRE_STAT register for current status. A transfer has to be concluded with STOP condition by setting M_STP bit high.

In Slave Mode, the TWI also constantly samples the bus and look for its own slave address during addressing cycles. Once a match is found, it is addressed and interrupts the CPU host with the corresponding status. Upon request, the CPU host should read the status, read/write 2WIRE_DATA data register, and set the 2WIRE_CNTR control register. After each byte transfer, a slave device always halt the operation of remote master by holding the next low pulse on SCL line until the microprocessor responds to the status of previous byte transfer or START condition.

7.2.6. TWI Controller Register List

Module Name	Base Address
TWI0	0x01C27000
TWI1	0x01C27400
TWI2	0x01C27800

Register Name	Offset	Description
TWI_ADDR_REG	0x00	TWI Slave Address
TWI_XADDR_REG	0x04	TWI Extended Slave Address Register
TWI_DATA_REG	0x08	TWI Data Byte Register
TWI_CNTR_REG	0x0C	TWI Control Register
TWI_STAT_REG	0x10	TWI Status Register
TWI_CCR_REG	0x14	TWI Clock Control Register
TWI_SRST_REG	0x18	TWI Software Reset Register
TWI_EFR_REG	0x1C	TWI Enhance Feature Register
TWI_LCR_REG	0x20	TWI Line Control Register

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

7.2.7. TWI Controller Register Description

7.2.7.1. TWI Slave Address Register

Offset: 0x00			Register Name: TWI_ADDR_REG
Bit	R/W	Default/Hex	Description
31:8	/	/	/
7:1	R/W	0	SLA Slave address 7-bit addressing: SLA6, SLA5, SLA4, SLA3, SLA2, SLA1, SLA0 10-bit addressing: 1, 1, 1, 1, 0, SLAX[9:8]
0	R/W	0	GCE General call address enable 0: Disable 1: Enable

Note:

For 7-bit addressing:

SLA6 – SLA0 is the 7-bit address of the TWI when in slave mode. When the TWI receives this address after a START condition, it will generate an interrupt and enter slave mode. (SLA6 corresponds to the first bit received from the TWI bus.) If GCE is set to '1', the TWI will also recognize the general call address (00h).

For 10-bit addressing:

When the address received starts with 11110b, the TWI recognizes this as the first part of a 10-bit address and if the next two bits match ADDR[2:1] (i.e. SLAX9 and SLAX8 of the device's extended address), it sends an ACK. (The device does not generate an interrupt at this point.) If the next byte of the address matches the XADDR register (SLAX7 – SLAX0), the TWI generates an interrupt and goes into slave mode.

7.2.7.2. TWI Extend Address Register

Offset: 0x04			Register Name: TWI_XADDR_REG
Bit	R/W	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0	SLAX Extend Slave Address SLAX[7:0]

7.2.7.3. TWI Data Register

Offset: 0x08			Register Name: TWI_DATA_REG
Bit	R/W	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0	TWI_DATA Data byte for transmitting or received

7.2.7.4. TWI Control Register

Offset: 0x0C			Register Name: TWI_CNTR_REG
Bit	R/W	Default/Hex	Description

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

31:8	/	/	/
7	R/W	0	INT_EN Interrupt Enable 1'b0: The interrupt line always low 1'b1: The interrupt line will go high when INT_FLAG is set.
6	R/W	0	BUS_EN TWI Bus Enable 1'b0: The TWI bus inputs ISDA/ISCL are ignored and the TWI Controller will not respond to any address on the bus 1'b1: The TWI will respond to calls to its slave address – and to the general call address if the GCE bit in the ADDR register is set. Notes: In master operation mode, this bit should be set to '1'
5	R/W	0	M_STA Master Mode Start When M_STA is set to '1', TWI Controller enters master mode and will transmit a START condition on the bus when the bus is free. If the M_STA bit is set to '1' when the TWI Controller is already in master mode and one or more bytes have been transmitted, then a repeated START condition will be sent. If the M_STA bit is set to '1' when the TWI is being accessed in slave mode, the TWI will complete the data transfer in slave mode then enter master mode when the bus has been released. The M_STA bit is cleared automatically after a START condition has been sent: writing a '0' to this bit has no effect.
4	R/W	0	M_STP Master Mode Stop If M_STP is set to '1' in master mode, a STOP condition is transmitted on the TWI bus. If the M_STP bit is set to '1' in slave mode, the TWI will behave as if a STOP condition has been received, but no STOP condition will be transmitted on the TWI bus. If both M_STA and M_STP bits are set, the TWI will first transmit the STOP condition (if in master mode) then transmit the START condition. The M_STP bit is cleared automatically: writing a '0' to this bit has no effect.
3	R/W	0	INT_FLAG Interrupt Flag INT_FLAG is automatically set to '1' when any of 28 (out of the possible 29) states is entered (see 'STAT Register' below). The only state that does not set INT_FLAG is state F8h. If the INT_EN bit is set, the interrupt line goes high when IFLG is set to '1'. If the TWI is operating in slave mode, data transfer is suspended when INT_FLAG is set and the low period of the TWI bus clock line (SCL) is stretched until '0' is written to INT_FLAG. The TWI clock line is then released and the interrupt line goes low.
2	R/W	0	A_ACK Assert Acknowledge When A_ACK is set to '1', an Acknowledge (low level on SDA) will be sent during the acknowledge clock pulse on the TWI bus if: 1) Either the whole of a matching 7-bit slave address or the first or the second byte of a matching 10-bit slave address has been received.

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			2) The general call address has been received and the GCE bit in the ADDR register is set to '1'. 3) A data byte has been received in master or slave mode. When A_ACK is '0', a Not Acknowledge (high level on SDA) will be sent when a data byte is received in master or slave mode. If A_ACK is cleared to '0' in slave transmitter mode, the byte in the DATA register is assumed to be the 'last byte'. After this byte has been transmitted, the TWI will enter state C8h then return to the idle state (status code F8h) when INT_FLAG is cleared. The TWI will not respond as a slave unless A_ACK is set.
1:0	R/W	0	/

7.2.7.5. TWI Status Register

Offset: 0x10			Register Name: TWI_STAT_REG
Bit	R/W	Default/Hex	Description
31:8	/	/	/
7:0	R	0xF8	STA Status Information Byte **Code Status** 0x00: Bus error 0x08: START condition transmitted 0x10: Repeated START condition transmitted 0x18: Address + Write bit transmitted, ACK received 0x20: Address + Write bit transmitted, ACK not received 0x28: Data byte transmitted in master mode, ACK received 0x30: Data byte transmitted in master mode, ACK not received 0x38: Arbitration lost in address or data byte 0x40: Address + Read bit transmitted, ACK received 0x48: Address + Read bit transmitted, ACK not received 0x50: Data byte received in master mode, ACK transmitted 0x58: Data byte received in master mode, not ACK transmitted 0x60: Slave address + Write bit received, ACK transmitted 0x68: Arbitration lost in address as master, slave address + Write bit received, ACK transmitted 0x70: General Call address received, ACK transmitted 0x78: Arbitration lost in address as master, General Call address received, ACK transmitted 0x80: Data byte received after slave address received, ACK transmitted 0x88: Data byte received after slave address received, not ACK transmitted 0x90: Data byte received after General Call received, ACK transmitted 0x98: Data byte received after General Call received, not ACK transmitted 0xA0: STOP or repeated START condition received in slave mode 0xA8: Slave address + Read bit received, ACK transmitted 0xB0: Arbitration lost in address as master, slave address + Read bit received, ACK transmitted 0xB8: Data byte transmitted in slave mode, ACK received 0xC0: Data byte transmitted in slave mode, ACK not received 0xC8: Last byte transmitted in slave mode, ACK received 0xD0: Second Address byte + Write bit transmitted, ACK received 0xD8: Second Address byte + Write bit transmitted, ACK not received 0xF8: No relevant status information, INT_FLAG=0 Others: Reserved

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

7.2.7.6. TWI Clock Register

Offset: 0x14			Register Name: TWI_CCR_REG
Bit	R/W	Default/Hex	Description
31:7	/	/	/
6:3	R/W	0	CLK_M
2:0	R/W	0	CLK_N The TWI bus is sampled by the TWI at the frequency defined by F0: Fsamp = F 0 = Fin / 2^CLK_N The TWI OSCL output frequency, in master mode, is F1 / 10: F1 = F0 / (CLK_M + 1) Foscl = F1 / 10 = Fin / (2^CLK_N * (CLK_M + 1)*10) For Example： Fin = 48Mhz (APB clock input) For 400kHz full speed 2Wire, CLK_N = 2, CLK_M=2 F0 = 48M/2^2=12Mhz, F1= F0/(10*(2+1)) = 0.4Mhz For 100Khz standard speed 2Wire, CLK_N=2, CLK_M=11 F0=48M/2^2=12Mhz, F1=F0/(10*(11+1)) = 0.1Mhz

7.2.7.7. TWI Soft Reset Register

Offset: 0x18			Register Name: TWI_SRST_REG
Bit	R/W	Default/Hex	Description
31:1	/	/	/
0	R/W	0	SOFT_RST Soft Reset Write ‘1’ to this bit to reset the TWI and clear to ‘0’ when completing Soft Reset operation.

7.2.7.8. TWI Enhance Feature Register

Offset: 0x1C			Register Name: TWI_EFR_REG
Bit	R/W	Default/Hex	Description
31:2	/	/	/
1:0	R/W	0	DBN Data Byte number follow Read Command Control 0— No Data Byte to be wrote after read command 1— Only 1 byte data to be wrote after read command 2— 2 bytes data can be wrote after read command 3— 3 bytes data can be wrote after read command

7.2.7.9. TWI Line Control Register

Offset: 0x20			Register Name: TWI_LCR_REG
Bit	R/W	Default/Hex	Description
31:6	/	/	/
5	R	1	SCL_STATE Current state of TWI_SCL 0 – low

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1 - high
4	R	1	SDA_STATE Current state of TWI_SDA 0 – low 1 - high
3	R/W	1	SCL_CTL TWI_SCL line state control bit When line control mode is enabled (bit[2] set), value of this bit decide the output level of TWI_SCL 0 – output low level 1 – output high level
2	R/W	0	SCL_CTL_EN TWI_SCL line state control enable When this bit is set, the state of TWI_SCL is control by the value of bit[3]. 0-disable TWI_SCL line control mode 1-enable TWI_SCL line control mode
1	R/W	1	SDA_CTL TWI_SDA line state control bit When line control mode is enabled (bit[0] set), value of this bit decide the output level of TWI_SDA 0 – output low level 1 – output high level
0	R/W	0	SDA_CTL_EN TWI_SDA line state control enable When this bit is set, the state of TWI_SDA is control by the value of bit[1]. 0-disable TWI_SDA line control mode 1-enable TWI_SDA line control mode

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

7.3. SPI

7.3.1. Overview

The SPI is the Serial Peripheral Interface which allows rapid data communication with less software interrupts. The SPI module contains one 64x8 receiver buffer (RXFIFO) and one 64x8 transmit buffer (TXFIFO). It can work at two modes: Master mode and Slave mode.

7.3.2. Feature

The SPI includes the following features:

- Full-duplex synchronous serial interface
- Master/Slave configurable
- Four chip selects to support multiple peripherals for SPI0,SPI1 has one chip select
- 8-bit wide by 64-entry FIFO for both transmit and receive data
- Polarity and phase of the Chip Select (SPI_SS) and SPI Clock (SPI_SCLK) are configurable

7.3.3. SPI Timing Diagram

The serial peripheral interface master uses the SPI_SCLK signal to transfer data in and out of the shift register. Data is clocked using any one of four programmable clock phase and polarity combinations.

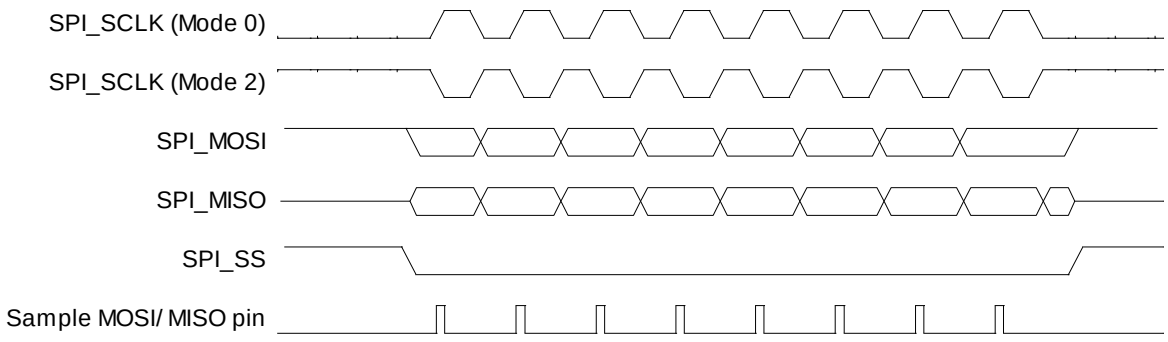
During Phase 0, Polarity 0 and Phase 1, Polarity 1 operations, output data changes on the falling clock edge and input data is shifted in on the rising edge.

During Phase 1, Polarity 0 and Phase 0, Polarity 1 operations, output data changes on the rising edges of the clock and is shifted in on falling edges.

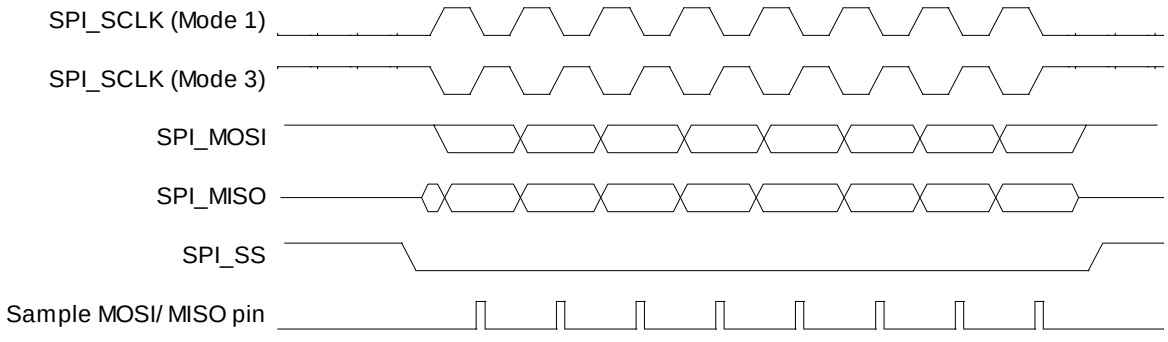
The POL defines the signal polarity when SPI_SCLK is in idle state. The SPI_SCLK is high level when POL is '1' and it is low level when POL is '0'. The PHA decides whether the leading edge of SPI_SCLK is used for setup or sample data. The leading edge is used for setup data when PHA is '1' and for sample data when PHA is '0'. The four kinds of modes are listed below:

SPI Mode	POL	PHA	Leading Edge	Trailing Edge
0	0	0	Rising, Sample	Falling, Setup
1	0	1	Rising, Setup	Falling, Sample
2	1	0	Falling, Sample	Rising, Setup
3	1	1	Failing, Setup	Rising, Sample

Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.



SPI Phase 0 Timing Diagram



SPI Phase 1 Timing Diagram

7.3.4. SPI Pin List

The direction of SPI pin is different in two work modes: Master Mode and Slave Mode.

Port Name	Width	Direction(M)	Direction(S)	Description
SPI_SCLK	1	OUT	IN	SPI Clock
SPI_MOSI	1	OUT	IN	SPI Master Output Slave Input Data Signal
SPI_MISO	1	IN	OUT	SPI Master Input Slave Output Data Signal
SPI_SS[3:0]	4	OUT	IN	SPI Chip Select Signal

7.3.5. SPI Module Clock Source and Frequency

The SPI module uses two clock sources: AHB_CLK and SPI_CLK. The SPI_SCLK can in the range from 3Khz to 100 MHZ and AHB_CLK >= 2xSPI_SCLK.

Clock Name	Description	Requirement
AHB_CLK	AHB bus clock, as the clock source of SPI module	AHB_CLK >= 2xSPI_SCLK
SPI_CLK	SPI serial input clock	

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

7.3.6. SPI Register List

Module Name	Base Address
SPI0	0x01C05000
SPI1	0x01C06000

Register Name	Offset	Description
SPI_GCR_REG	0x04	SPI Global Control Register
SPI_TCR_REG	0x08	SPI Transfer Control Register
SPI_IER_REG	0x10	SPI Interrupt Control Register
SPI_ISR_REG	0x14	SPI Interrupt Status Register
SPI_FCR_REG	0x18	SPI FIFO Control Register
SPI_FSR_REG	0x1C	SPI FIFO Status Register
SPI_WCR_REG	0x20	SPI Wait Clock Counter Register
SPI_CCR_REG	0x24	SPI Clock Rate Control Register
SPI_MBC_REG	0x30	SPI Burst Counter Register
SPI_MTC_REG	0x34	SPI Transmit Counter Register
SPI_BCC_REG	0x38	SPI Burst Control Register
SPI_TXD_REG	0x200	SPI TX Data Register
SPI_RXD_REG	0x300	SPI RX Data Register

7.3.7. SPI Register Description

7.3.7.1. SPI Global Control Register

Offset: 0x04			Register Name: SPI_CTL_REG
Bit	R/W	Default/Hex	Description
31	R/W	0	SRST Soft reset Write ‘1’ to this bit will clear the SPI controller, and auto clear to ‘0’ when reset operation completes Write ‘0’ has no effect.
30:8	/	/	/
7	R/W	1	TP_EN Transmit Pause Enable In master mode, it is used to control transmit state machine to stop smart burst sending when RX FIFO is full. 1 – stop transmit data when RXFIFO full 0 – normal operation, ignore RXFIFO status Note: Can’t be written when XCH=1
6:2	/	/	/
1	R/W	0	MODE SPI Function Mode Select

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0: Slave Mode 1: Master Mode Note: Can't be written when XCH=1
0	R/W	0	EN SPI Module Enable Control 0: Disable 1: Enable

7.3.7.2. SPI Transfer Control Register

Offset: 0x08			Register Name: SPI_INTCTL_REG
Bit	R/W	Default/Hex	Description
31	R/W	0x0	XCH Exchange Burst In master mode it is used to start SPI burst 0: Idle 1: Initiates exchange. Write "1" to this bit will start the SPI burst, and will auto clear after finishing the bursts transfer specified by BC. Write "1" to SRST will also clear this bit. Write '0' to this bit has no effect. Note： Can't be written when XCH=1.
30:14	/	/	/
13	R/W	0x0	SDM Master Sample Data Mode 0 - Delay Sample Mode 1 - Normal Sample Mode In Normal Sample Mode, SPI master samples the data at the correct edge for each SPI mode; In Delay Sample Mode, SPI master samples data at the edge that is half cycle delayed by the correct edge defined in respective SPI mode.
12	R/W	0x0	FBS First Transmit Bit Select 0: MSB first 1: LSB first Note： Can't be written when XCH=1.
11	R/W	0x0	SDC Master Sample Data Control Set this bit to '1' to make the internal read sample point with a delay of half cycle of SPI_CLK. It is used in high speed read operation to reduce the error caused by the time delay of SPI_CLK propagating between master and slave. 0 – normal operation, do not delay internal read sample point 1 – delay internal read sample point Note： Can't be written when XCH=1.
10	R/W	0x0	RPSM Rapids mode select

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Select Rapids mode for high speed write. 0: normal write mode 1: rapids write mode Note：Can't be written when XCH=1.
9	R/W	0x0	DDB Dummy Burst Type 0: The bit value of dummy SPI burst is zero 1: The bit value of dummy SPI burst is one Note：Can't be written when XCH=1.
8	R/W	0x0	DHB Discard Hash Burst In master mode it controls whether discarding unused SPI bursts 0: Receiving all SPI bursts in BC period 1: Discard unused SPI bursts, only fetching the SPI bursts during dummy burst period. The bursts number is specified by TC. Note：Can't be written when XCH=1.
7	R/W	0x1	SS_LEVEL When control SS signal manually (SPI_CTRL_REG.SS_CTRL==1), set this bit to '1' or '0' to control the level of SS signal. 0: set SS to low 1: set SS to high Note：Can't be written when XCH=1.
6	R/W	0x0	SS_OWNER SS Output Owner Select Usually, controller sends SS signal automatically with data together. When this bit is set to 1, software must manually write SPI_CTL_REG.SS_LEVEL to 1 or 0 to control the level of SS signal. 0: SPI controller 1: Software Note：Can't be written when XCH=1.
5:4	R/W	0x0	SS_SEL SPI Chip Select Select one of four external SPI Master/Slave Devices 00: SPI_SS0 will be asserted 01: SPI_SS1 will be asserted 10: SPI_SS2 will be asserted 11: SPI_SS3 will be asserted Note：Can't be written when XCH=1.
3	R/W	0x0	SSCTL In master mode, this bit selects the output wave form for the SPI_SSx signal. Only valid when SS_OWNER = 0. 0: SPI_SSx remains asserted between SPI bursts 1: Negate SPI_SSx between SPI bursts Note：Can't be written when XCH=1.
2	R/W	0x1	SPOL

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			SPI Chip Select Signal Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle) Note：Can't be written when XCH=1.
1	R/W	0x1	CPOL SPI Clock Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle) Note：Can't be written when XCH=1.
0	R/W	0x1	CPHA SPI Clock/Data Phase Control 0: Phase 0 (Leading edge for sample data) 1: Phase 1 (Leading edge for setup data) Note：Can't be written when XCH=1.

7.3.7.3. SPI Interrupt Control Register

Offset: 0x10			Register Name: SPI_IER_REG
Bit	R/W	Default/Hex	Description
31:14	R	0x0	Reserved.
13	R/W	0x0	SS_INT_EN SSI Interrupt Enable Chip Select Signal (SSx) from valid state to invalid state 0: Disable 1: Enable
12	R/W	0x0	TC_INT_EN Transfer Completed Interrupt Enable 0: Disable 1: Enable
11	R/W	0x0	TF_UDR_INT_EN TXFIFO under run Interrupt Enable 0: Disable 1: Enable
10	R/W	0x0	TF_OVF_INT_EN TX FIFO Overflow Interrupt Enable 0: Disable 1: Enable
9	R/W	0x0	RF_UDR_INT_EN RXFIFO under run Interrupt Enable 0: Disable 1: Enable
8	R/W	0x0	RF_OVF_INT_EN RX FIFO Overflow Interrupt Enable 0: Disable 1: Enable
7	R	0x0	Reserved.

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

6	R/W	0x0	TF_FUL_INT_EN TX FIFO Full Interrupt Enable 0: Disable 1: Enable
5	R/W	0x0	TX_EMP_INT_EN TX FIFO Empty Interrupt Enable 0: Disable 1: Enable
4	R/W	0x0	TX_ERQ_INT_EN TX FIFO Empty Request Interrupt Enable 0: Disable 1: Enable
3	R	0x0	Reserved
2	R/W	0x0	RF_FUL_INT_EN RX FIFO Full Interrupt Enable 0: Disable 1: Enable
1	R/W	0x0	RX_EMP_INT_EN RX FIFO Empty Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	RF_RDY_INT_EN RX FIFO Ready Request Interrupt Enable 0: Disable 1: Enable

7.3.7.4. SPI Interrupt Status Register

Offset: 0x14			Register Name: SPI_INT_STA_REG
Bit	R/W	Default/Hex	Description
31:14	/	0	/
13	R/W	0	SSI SS Invalid Interrupt When SSI is 1, it indicates that SS has changed from valid state to invalid state. Writing 1 to this bit clears it.
12	R/W	0	TC Transfer Completed In master mode, it indicates that all bursts specified by BC has been exchanged. In other condition, When set, this bit indicates that all the data in TXFIFO has been loaded in the Shift register, and the Shift register has shifted out all the bits. Writing 1 to this bit clears it. 0: Busy 1: Transfer Completed
11	R/W	0	TF_UDF TXFIFO Underrun

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			This bit is set when if the TXFIFO is underrun. Writing 1 to this bit clears it. 0: TXFIFO is not underrun 1: TXFIFO is underrun
10	R/W	0	TF_OVF TXFIFO Overflow This bit is set when if the TXFIFO is overflow. Writing 1 to this bit clears it. 0: TXFIFO is not overflow 1: TXFIFO is overflowed
9	R/W	0	RX_UDF RXFIFO Underrun When set, this bit indicates that RXFIFO has underrun. Writing 1 to this bit clears it.
8	R/W	0	RX_OVF RXFIFO Overflow When set, this bit indicates that RXFIFO has overflowed. Writing 1 to this bit clears it. 0: RXFIFO is available. 1: RXFIFO has overflowed.
7	/	/	/
6	R/W	0	TX_FULL TXFIFO Full This bit is set when if the TXFIFO is full . Writing 1 to this bit clears it. 0: TXFIFO is not Full 1: TXFIFO is Full
5	R/W	1	TX_EMP TXFIFO Empty This bit is set if the TXFIFO is empty. Writing 1 to this bit clears it. 0: TXFIFO contains one or more words. 1: TXFIFO is empty
4	R/W	0	TX_READY TXFIFO Ready 0: TX_WL > TX_TRIG_LEVEL 1: TX_WL <= TX_TRIG_LEVEL This bit is set any time if TX_WL <= TX_TRIG_LEVEL. Writing “1” to this bit clears it. Where TX_WL is the water level of RXFIFO
3	/	/	reserved
2	R/W	0	RX_FULL RXFIFO Full This bit is set when the RXFIFO is full. Writing 1 to this bit clears it. 0: Not Full 1: Full
1	R/W	1	RX_EMP RXFIFO Empty This bit is set when the RXFIFO is empty. Writing 1 to this bit clears it. 0: Not empty

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: empty
0	R/W	0	RX_RDY RXFIFO Ready 0: RX_WL < RX_TRIG_LEVEL 1: RX_WL >= RX_TRIG_LEVEL This bit is set any time if RX_WL >= RX_TRIG_LEVEL. Writing “1” to this bit clears it. Where RX_WL is the water level of RXFIFO.

7.3.7.5. SPI FIFO Control Register

Offset: 0x18			Register Name: SPI_DMACTL_REG
Bit	R/W	Default/Hex	Description
31	R/W	0	TX_FIFO_RST TX FIFO Reset Write ‘1’ to this bit will reset the control portion of the TX FIFO and auto clear to ‘0’ when completing reset operation, write to ‘0’ has no effect.
30	R/W	0	TF_TEST_ENB TX Test Mode Enable 0: disable 1: enable Note: In normal mode, TX FIFO can only be read by SPI controller, write ‘1’ to this bit will switch TX FIFO read and write function to AHB bus. This bit is used to test the TX FIFO, don’t set in normal operation and don’t set RF_TEST and TF_TEST at the same time.
29:28	/	/	/
27:26	R/W	0x0	TX_FIFO_ACCESS_SIZE 00: TX FIFO access in byte 01: TX FIFO access in word (4bytes) 10: Reserved 11: TX FIFO access size controlled by bus
25	/	/	/
24	R/W	0x0	TF_ DRQ_EN TX FIFO DMA Request Enable 0: Disable 1: Enable
23:16	R/W	0x40	TX_TRIG_LEVEL TX FIFO Empty Request Trigger Level
15	R/W	0x0	RF_RST RXFIFO Reset Write ‘1’ to this bit will reset the control portion of the receiver FIFO, and auto clear to ‘0’ when completing reset operation, write ‘0’ to this bit has no effect.
14	R/W	0x0	RF_TEST RX Test Mode Enable 0: Disable 1: Enable

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Note: In normal mode, RX FIFO can only be written by SPI controller, write '1' to this bit will switch RX FIFO read and write function to AHB bus. This bit is used to test the RX FIFO, don't set in normal operation and don't set RF_TEST and TF_TEST at the same time.
13:12	R	0x0	Reserved
11:10	R/W	0x0	RX_FIFO_ACCESS_SIZE 00: RX FIFO access in byte 01: RX FIFO access in word (4bytes) 10: Reserved 11: RX FIFO access size controlled by bus
9	R/W	0x0	RX_DMA_MODE SPI RX DMA Mode Control 0: Normal DMA mode 1: Dedicate DMA mode
8	R/W	0x0	RF_ DRQ_EN RX FIFO DMA Request Enable 0: Disable 1: Enable
7:0	R/W	0x1	RX_TRIG_LEVEL RX FIFO Ready Request Trigger Level

7.3.7.6. SPI FIFO Status Register

Offset: 0x1C			Register Name: SPI_FSR_REG
Bit	R/W	Default/Hex	Description
31	R	0x0	TB_WR TX FIFO Write Buffer Write Enable
30:28	R	0x0	TB_CNT TX FIFO Write Buffer Counter These bits indicate the number of words in TX FIFO Write Buffer
27:24	R	0x0	Reserved
23:16	R	0x0	TF_CNT TX FIFO Counter These bits indicate the number of words in TX FIFO 0: 0 byte in TX FIFO 1: 1 byte in TX FIFO … 64: 64 bytes in TX FIFO Other: /
15	R	0x0	RB_WR RX FIFO Read Buffer Write Enable
14:12	R	0x0	RB_CNT RX FIFO Read Buffer Counter These bits indicate the number of words in RX FIFO Read Buffer
11:8	R	0x0	Reserved
7:0	R	0x0	RF_CNT

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			RX FIFO Counter These bits indicate the number of words in RX FIFO 0: 0 byte in RX FIFO 1: 1 byte in RX FIFO … 64: 64 bytes in RX FIFO Others: /

7.3.7.7. SPI Wait Clock Register

Offset: 0x20			Register Name: SPI_WAIT_REG
Bit	R/W	Default/Hex	Description
31:20	/	/	/
19:16	R/W	0x0	SWC Dual mode direction switch wait clock counter (for master mode only). 0: No wait states inserted n: n SPI_SCLK wait states inserted Note: These bits control the number of wait states to be inserted before start dual data transfer in dual SPI mode. The SPI module counts SPI_SCLK by SWC for delaying next word data transfer. Note：Can't be written when XCH=1.
15:0	R/W	0	WCC Wait Clock Counter (In Master mode) These bits control the number of wait states to be inserted in data transfers. The SPI module counts SPI_SCLK by WCC for delaying next word data transfer. 0: No wait states inserted N: N SPI_SCLK wait states inserted

7.3.7.8. SPI Clock Control Register

Offset: 0x24			Register Name: SPI_CCTL_REG
Bit	R/W	Default/Hex	Description
31:13	/	/	/
12	R/W	0	DRS Divide Rate Select (Master Mode Only) 0: Select Clock Divide Rate 1 1: Select Clock Divide Rate 2
11:8	R/W	0	CDR1 Clock Divide Rate 1 (Master Mode Only) This field selects the baud rate of the SPI_SCLK based on a division of the AHB_CLK. These bits allow SPI to synchronize with different external SPI devices. The max frequency is one quarter of AHB_CLK. The divide ratio is determined according to the following table using the equation: 2^(n+1). The SPI_SCLK is determined according to the following equation: SPI_CLK = AHB_CLK / 2^(n+1).
7:0	R/W	0x2	CDR2

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Clock Divide Rate 2 (Master Mode Only) The SPI_SCLK is determined according to the following equation: SPI_CLK = AHB_CLK / (2*(n + 1)).

7.3.7.9. SPI Master Burst Counter Register

Offset: 0x30			Register Name: SPI_BC_REG
Bit	R/W	Default/Hex	Description
31:24	/	/	/
23:0	R/W	0	MBC Master Burst Counter In master mode, this field specifies the total burst number. 0: 0 burst 1: 1 burst … N: N bursts

7.3.7.10. SPI Master Transmit Counter Register

Offset: 0x34			**Register Name: SPI_TC_REG**
Bit	R/W	Default/Hex	Description
31:24	/	/	/
23:0	R/W	0	MWTC Master Write Transmit Counter In master mode, this field specifies the burst number that should be sent to TXFIFO before automatically sending dummy burst. For saving bus bandwidth, the dummy burst (all zero bits or all one bits) is sent by SPI Controller automatically. 0: 0 burst 1: 1 burst … N: N bursts

7.3.7.11. SPI Master Burst Control Counter Register

Offset: 0x38			Register Name: SPI_BCC_REG
Bit	R/W	Default/Hex	Description
31:29	R	0x0	Reserved
28	R/W	0x0	DRM Master Dual Mode RX Enable 0: RX use single-bit mode 1: RX use dual mode Note：Can’t be written when XCH=1.
27:24	R/W	0x0	DBC Master Dummy Burst Counter In master mode, this field specifies the burst number that should be sent before receive in dual SPI mode. The data is don’t care by the device. 0: 0 burst

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: 1 burst … N: N bursts Note：Can't be written when XCH=1.
23:0	R/W	0x0	STC Master Single Mode Transmit Counter In master mode, this field specifies the burst number that should be sent in single mode before automatically sending dummy burst. This is the first transmit counter in all bursts. 0: 0 burst 1: 1 burst … N: N bursts Note：Can't be written when XCH=1.

7.3.7.12. SPI TX Data Register

Offset: 0x200			Register Name: SPI_TXD_REG
Bit	R/W	Default/Hex	Description
31:0	W/R	0x0	TDATA Transmit Data This register can be accessed in byte, half-word or word unit by AHB. In byte accessing method, if there are rooms in RXFIFO, one burst data is written to RXFIFO and the depth is increased by 1. In half-word accessing method, two SPI burst data are written and the TXFIFO depth is increase by 2. In word accessing method, four SPI burst data are written and the TXFIFO depth is increased by 4. Note: This address is writing-only if TF_TEST is '0', and if TF_TEST is set to '1', this address is readable and writable to test the TX FIFO through the AHB bus.

7.3.7.13. SPI RX Data Register

Offset: 0x300			Register Name: SPI_RXD_REG
Bit	R/W	Default/Hex	Description
31:0	R	0	RDATA Receive Data This register can be accessed in byte, half-word or word unit by AHB. In byte accessing method, if there are data in RXFIFO, the top word is returned and the RXFIFO depth is decreased by 1. In half-word accessing method, two SPI bursts are returned and the RXFIFO depth is decrease by 2. In word accessing method, the four SPI bursts are returned and the RXFIFO depth is decreased by 4. Note: This address is read-only if RF_TEST is '0', and if RF_TEST is set to '1', this address is readable and writable to test the RX FIFO through the AHB bus.

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

7.4. UART

7.4.1. Overview

The UART is used for serial communication with a peripheral, modem (data carrier equipment, DCE) or data set. Data is written from a master (CPU) over the APB bus to the UART and it is converted to serial form and transmitted to the destination device. Serial data is also received by the UART and stored for the master (CPU) to read back.

The UART contains registers to control the character length, baud rate, parity generation/checking, and interrupt generation. Although there is only one interrupt output signal from the UART, there are several prioritized interrupt types that can be responsible for its assertion. Each of the interrupt types can be separately enabled/disabled with the control registers.

The UART has 16450 and 16550 modes of operation, which are compatible with a range of standard software drivers. In 16550 mode, transmit and receive operations are both buffered by FIFOs. In 16450 mode, these FIFOs are disabled.

The UART supports data lengths from five to eight bits, an optional parity bit and 1, 1 ½ or 2 stop bits, and is fully programmable by an AMBA APB CPU interface. A 16-bit programmable baud rate generator and an 8-bit scratch register are included, together with separate transmit and receive FIFOs. Eight modem control lines and a diagnostic loop-back mode are provided.

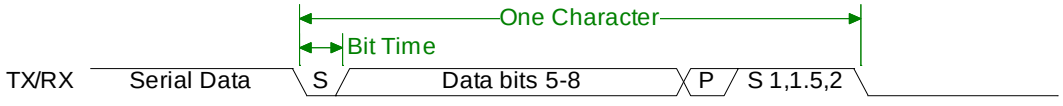
Interrupts can be generated for a range of TX Buffer/FIFO, RX Buffer/FIFO, Modem Status and Line Status conditions.

7.4.2. Feature

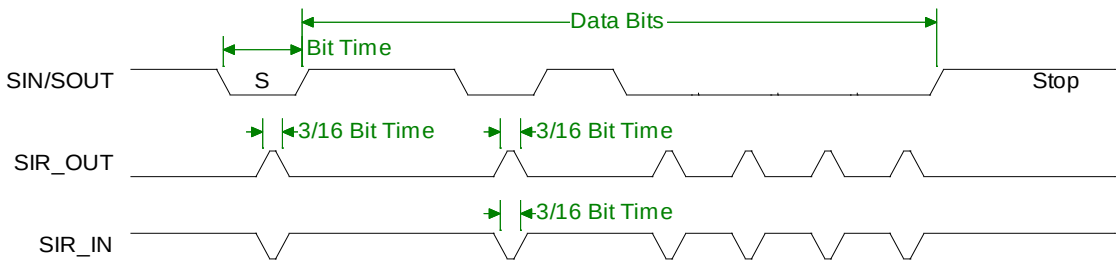
The UART includes the following features:

- Compatible with industry-standard 16550 UARTs
- 64-Bytes Transmit and receive data FIFOs
- DMA controller interface
- Software/ Hardware Flow Control
- Programmable Transmit Holding Register Empty interrupt
- Interrupt support for FIFOs, Status Change

7.4.3. UART Timing Diagram



UART Serial Data Format



Serial IrDA Data Format

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

7.4.4. UART Pin List

Port Name	Width	Direction	Description
UART0_TX	1	OUT	UART Serial Bit output
UART0_RX	1	IN	UART Serial Bit input
UART1_TX	1	OUT	UART Serial Bit output
UART1_RX	1	IN	UART Serial Bit input
UART1_RTS	1	OUT	UART Request To Send This active low output signal informs Modem that the UART is ready to send data
UART1_CTS	1	IN	UART Clear To End This active low signal is an input showing when Modem is ready to accept data
UART2_TX	1	OUT	UART Serial Bit output
UART2_RX	1	IN	UART Serial Bit input
UART2_RTS	1	OUT	UART Request To Send This active low output signal informs Modem that the UART is ready to send data
UART2_CTS	1	IN	UART Clear To End This active low signal is an input showing when Modem is ready to accept data

7.4.5. IrDA Inverted Signals

When the UART is working in IrDA mode (MCR[6]='1'), if HALT[4] is set to '1', the signal is inverted before transferring to pin SOUT and if HALT[5] is set to '1', the signal is inverted after receiving from pin SIN.

7.4.6. UART Register List

There are 3 UART controllers. UART1 has full modem control signals, including RTS, CTS, DTR, DSR, DCD and RING signal.

Module Name	Base Address
UART0	0x01C25000
UART1	0x01C25400
UART2	0x01C25800

Register Name	Offset	Description
UART_RBR_REG	0x00	UART Receive Buffer Register
UART_THR_REG	0x00	UART Transmit Holding Register
UART_DLL_REG	0x00	UART Divisor Latch Low Register
UART_DLH_REG	0x04	UART Divisor Latch High Register
UART_IER_REG	0x04	UART Interrupt Enable Register
UART_IIR_REG	0x08	UART Interrupt Identity Register
UART_FCR_REG	0x08	UART FIFO Control Register
UART_LCR_REG	0x0C	UART Line Control Register

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

UART_MCR_REG	0x10	UART Modem Control Register
UART_LSR_REG	0x14	UART Line Status Register
UART_MSR_REG	0x18	UART Modem Status Register
UART_SCH_REG	0x1C	UART Scratch Register
UART_USR_REG	0x7C	UART Status Register
UART_TFL_REG	0x80	UART Transmit FIFO Level Register
UART_RFL_REG	0x84	UART Receive FIFO Level Register
UART_HSK_REG	0x88	UART DMA Handshake Config Register
UART_HALT_REG	0xA4	UART Halt TX Register
UART_DBG_DLL_REG	0xB0	UART Debug DLL Register
UART_DBG_DLH_REG	0xB4	UART Debug DLH Register

7.4.7. UART Register Description

7.4.7.1. UART Receiver Buffer Register

Offset: 0x00			Register Name: UART_RBR_REG
Bit	R/W	Default/Hex	Description
31:8	/	/	/
7:0	R	0	RBR Receiver Buffer Register Data byte received on the serial input port (sin) in UART mode, or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line Status Register (LCR) is set. If in FIFO mode and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO is preserved, but any incoming data are lost and an overrun error occurs.

7.4.7.2. UART Transmit Holding Register

Offset: 0x00			Register Name: UART_THR_REG
Bit	R/W	Default/Hex	Description
31:8	/	/	/
7:0	W	0	THR Transmit Holding Register Data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If in FIFO mode and FIFOs are enabled (FCR[0] = 1) and THRE is set, 16 number of characters of data may be written to the THR before the FIFO is full. Any attempt to write data when the FIFO is full results in the write data being lost.

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

7.4.7.3. UART Divisor Latch Low Register

Offset: 0x00			Register Name: UART_DLL_REG
Bit	R/W	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0	DLL Divisor Latch Low Lower 8 bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may only be accessed when the DLAB bit (LCR[7]) is set and the UART is not busy (USR[0] is zero). The output baud rate is equal to the serial clock (sclk) frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor). Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur. Also, once the DLL is set, at least 8 clock cycles of the slowest UART clock should be allowed to pass before transmitting or receiving data.

7.4.7.4. UART Divisor Latch High Register

Offset: 0x04			Register Name: UART_DLH_REG
Bit	R/W	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0	DLH Divisor Latch High Upper 8 bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may only be accessed when the DLAB bit (LCR[7]) is set and the UART is not busy (USR[0] is zero). The output baud rate is equal to the serial clock (sclk) frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor). Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur. Also, once the DLH is set, at least 8 clock cycles of the slowest UART clock should be allowed to pass before transmitting or receiving data.

7.4.7.5. UART Interrupt Enable Register

Offset: 0x04			Register Name: UART_IER_REG
Bit	R/W	Default/Hex	Description
31:8	/	/	/
7	R/W		PTIME Programmable THRE Interrupt Mode Enable This is used to enable/disable the generation of THRE Interrupt. 0: Disable 1: Enable
6:4	/	/	/
3	R/W	0	EDSSI

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Enable Modem Status Interrupt This is used to enable/disable the generation of Modem Status Interrupt. This is the fourth highest priority interrupt. 0: Disable 1: Enable
2	R/W	0	ELSI Enable Receiver Line Status Interrupt This is used to enable/disable the generation of Receiver Line Status Interrupt. This is the highest priority interrupt. 0: Disable 1: Enable
1	R/W	0	ETBEI Enable Transmit Holding Register Empty Interrupt This is used to enable/disable the generation of Transmitter Holding Register Empty Interrupt. This is the third highest priority interrupt. 0: Disable 1: Enable
0	R/W	0	ERBFI Enable Received Data Available Interrupt This is used to enable/disable the generation of Received Data Available Interrupt and the Character Timeout Interrupt (if in FIFO mode and FIFOs enabled). These are the second highest priority interrupts. 0: Disable 1: Enable

7.4.7.6. UART Interrupt Identity Register

Offset: 0x08			Register Name: UART_IIR_REG
Bit	R/W	Default/Hex	Description
31:8	/	/	/
7:6	R	0	FEFLAG FIFOs Enable Flag This is used to indicate whether the FIFOs are enabled or disabled. 00: Disable 11: Enable
5:4	/	/	/
3:0	R	0x1	IID Interrupt ID This indicates the highest priority pending interrupt which can be one of the following types: 0000: modem status 0001: no interrupt pending 0010: THR empty 0100: received data available 0110: receiver line status 0111: busy detect

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1100: character timeout Bit 3 indicates an interrupt can only occur when the FIFOs are enabled and used to distinguish a Character Timeout condition interrupt.

Interrupt ID	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset
0001	-	None	None	-
0110	Highest	Receiver line status	Overrun/parity/ framing errors or break interrupt	Reading the line status register
0100	Second	Received data available	Receiver data available (non-FIFO mode or FIFOs disabled) or RCVR FIFO trigger level reached (FIFO mode and FIFOs enabled)	Reading the receiver buffer register (non-FIFO mode or FIFOs disabled) or the FIFO drops below the trigger level (FIFO mode and FIFOs enabled)
1100	Second	Character timeout indication	No characters in or out of the RCVR FIFO during the last 4 character times and there is at least 1character in it during This time	Reading the receiver buffer register
0010	Third	Transmit holding register empty	Transmitter holding register empty (Program THRE Mode disabled) or XMIT FIFO at or below threshold (Program THRE Mode enabled)	Reading the IIR register (if source of interrupt); or, writing into THR (FIFOs or THRE Mode not selected or disabled) or XMIT FIFO above threshold (FIFOs and THRE Mode selected and enabled).
0000	Fourth	Modem status	Clear to send or data set ready or ring indicator or data carrier detect. Note that if auto flow control mode is enabled, a change in CTS (that is, DCTS set) does not cause an interrupt.	Reading the Modem status Register
0111	Fifth	Busy detect indication	UART_16550_COMPATIBLE = NO and master has tried to write to the Line Control Register while the UART is busy (USR[0] is set to one).	Reading the UART status register

7.4.7.7. UART FIFO Control Register

Offset: 0x08	Register Name: UART_FCR_REG

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	R/W	Default/Hex	Description
31:8	/	/	/
7:6	W	0	RT RCVR Trigger This is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt is generated. In auto flow control mode it is used to determine when the rts_n signal is de-asserted. It also determines when the dma_rx_req_n signal is asserted in certain modes of operation. 00: 1 character in the FIFO 01: FIFO ¼ full 10: FIFO ½ full 11: FIFO-2 less than full
5:4	W	0	TFT TX Empty Trigger Writes have no effect when THRE_MODE_USER = Disabled. This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. It also determines when the dma_tx_req_n signal is asserted when in certain modes of operation. 00: FIFO empty 01: 2 characters in the FIFO 10: FIFO ¼ full 11: FIFO ½ full
3	W	0	DMAM DMA Mode 0: Mode 0 1: Mode 1
2	W	0	XFIFOR XMIT FIFO Reset This resets the control portion of the transmit FIFO and treats the FIFO as empty. This also De-asserts the DMA TX request. It is 'self-clearing'. It is not necessary to clear this bit.
1	W	0	RFIFOR RCVR FIFO Reset This resets the control portion of the receive FIFO and treats the FIFO as empty. This also De-asserts the DMA RX request. It is 'self-clearing'. It is not necessary to clear this bit.
0	W	0	FIFOE Enable FIFOs This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. Whenever the value of this bit is changed both the XMIT and RCVR controller portion of FIFOs is reset.

7.4.7.8. UART Line Control Register

Offset: 0x0C	Register Name: UART_LCR_REG

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	R/W	Default/Hex	Description
31:8	/	/	/
7	R/W	0	DLAB Divisor Latch Access Bit It is writeable only when UART is not busy (USR[0] is zero) and always readable. This bit is used to enable reading and writing of the Divisor Latch register (DLL and DLH) to set the baud rate of the UART. This bit must be cleared after initial baud rate setup in order to access other registers. 0: Select RX Buffer Register (RBR) / TX Holding Register(THR) and Interrupt Enable Register (IER) 1: Select Divisor Latch LS Register (DLL) and Divisor Latch MS Register (DLM)
6	R/W	0	BC Break Control Bit This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. If SIR_MODE = Enabled and active (MCR[6] set to one) the sir_out_n line is continuously pulsed. When in Loopback Mode, the break condition is internally looped back to the receiver and the sir_out_n line is forced low.
5:4	R/W	0	EPS Even Parity Select It is writeable only when UART is not busy (USR[0] is zero) and always writable readable. This is used to select between even and odd parity, when parity is enabled (PEN set to one). Setting the LCR[5] is uset to reverse the LCR[4]. 00: Odd Parity 01: Even Parity 1X: Reverse LCR[4]
3	R/W	0	PEN Parity Enable It is writeable only when UART is not busy (USR[0] is zero) and always readable. This bit is used to enable and disable parity generation and detection in transmitted and received serial character respectively. 0: parity disabled 1: parity enabled
2	R/W	0	STOP Number of stop bits It is writeable only when UART is not busy (USR[0] is zero) and always readable. This is used to select the number of stop bits per character that the peripheral transmits and receives. If set to zero, one stop bit is transmitted in the serial data. If set to one and the data bits are set to 5 (LCR[1:0] set to zero) one and a half stop bits is transmitted. Otherwise, two stop bits are transmitted. Note that regardless of the number of stop

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			bits selected, the receiver checks only the first stop bit. 0: 1 stop bit 1: 1.5 stop bits when DLS (LCR[1:0]) is zero, else 2 stop bit
1:0	R/W	0	DLS Data Length Select It is writeable only when UART is not busy (USR[0] is zero) and always readable. This is used to select the number of data bits per character that the peripheral transmits and receives. The number of bit that may be selected areas follows: 00: 5 bits 01: 6 bits 10: 7 bits 11: 8 bits

7.4.7.9. UART Modem Control Register

Offset: 0x10			Register Name: UART_MCR_REG
Bit	R/W	Default/Hex	Description
31:7	/	/	/
6	R/W	0	SIRE SIR Mode Enable 0: IrDA SIR Mode disabled 1: IrDA SIR Mode enabled
5	R/W	0	AFCE Auto Flow Control Enable When FIFOs are enabled and the Auto Flow Control Enable (AFCE) bit is set, Auto Flow Control features are enabled. 0: Auto Flow Control Mode disabled 1: Auto Flow Control Mode enabled
4	R/W	0	LOOP Loop Back Mode 0: Normal Mode 1: Loop Back Mode This is used to put the UART into a diagnostic mode for test purposes. If operating in UART mode (SIR_MODE != Enabled or not active, MCR[6] set to zero), data on the sout line is held high, while serial data output is looped back to the sin line, internally. In this mode all the interrupts are fully functional. Also, in loopback mode, the modem control inputs (dsr_n, cts_n, ri_n, dcd_n) are disconnected and the modem control outputs (dtr_n, rts_n, out1_n, out2_n) are looped back to the inputs, internally. If operating in infrared mode (SIR_MODE == Enabled AND active, MCR[6] set to one), data on the sir_out_n line is held low, while serial data output is inverted and looped back to the sir_in line.
3:2	/	/	/
1	R/W	0	RTS Request to Send

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] set to zero), the rts_n signal is set low by programming MCR[1] (RTS) to a high.In Auto Flow Control, AFCE_MODE == Enabled and active (MCR[5] set to one) and FIFOs enable (FCR[0] set to one), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). The rts_n signal is De-asserted when MCR[1] is set low. 0: rts_n De-asserted (logic 1) 1: rts_n asserted (logic 0) Note that in Loopback mode (MCR[4] set to one), the rts_n output is held inactive high while the value of this location is internally looped back to an input.
0	R/W	0	DTR Data Terminal Ready This is used to directly control the Data Terminal Ready (dtr_n) output. The value written to this location is inverted and driven out on dtr_n. 0：dtr_n De-asserted (logic 1) 1：dtr_n asserted (logic 0) The Data Terminal Ready output is used to inform the modem or data set that the UART is ready to establish communications. Note that in Loopback mode (MCR[4] set to one), the dtr_n output is held inactive high while the value of this location is internally looped back to an input.

7.4.7.10. UART Line Status Register

Offset: 0x14			Register Name: UART_LSR_REG
Bit	R/W	Default/Hex	Description
31:8	/	/	/
7	R	0	FIFOERR RX Data Error in FIFO When FIFOs are disabled, this bit is always 0. When FIFOs are enabled, this bit is set to 1 when there is at least one PE, FE, or BI in the RX FIFO. It is cleared by a read from the LSR register provided there are no subsequent errors in the FIFO.
6	R	1	TEMT Transmitter Empty If the FIFOs are disabled, this bit is set to "1" whenever the TX Holding Register and the TX Shift Register are empty. If the FIFOs are enabled, this bit is set whenever the TX FIFO and the TX Shift Register are empty. In both cases, this bit is cleared when a byte is written to the TX data channel.
5	R	1	THRE

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			TX Holding Register Empty If the FIFOs are disabled, this bit is set to "1" whenever the TX Holding Register is empty and ready to accept new data and it is cleared when the CPU writes to the TX Holding Register. If the FIFOs are enabled, this bit is set to "1" whenever the TX FIFO is empty and it is cleared when at least one byte is written to the TX FIFO.
4	R	0	BI Break Interrupt This is used to indicate the detection of a break sequence on the serial input data. If in UART mode (SIR_MODE == Disabled), it is set whenever the serial input, sin, is held in a logic '0' state for longer than the sum of *start time* + *data bits* + *parity* + *stop bits*. If in infrared mode (SIR_MODE == Enabled), it is set whenever the serial input, sir_in, is continuously pulsed to logic '0' for longer than the sum of *start time* + *data bits* + *parity* + *stop bits*. A break condition on serial input causes one and only one character, consisting of all zeros, to be received by the UART. In the FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading the LSR clears the BI bit. In the non-FIFO mode, the BI indication occurs immediately and persists until the LSR is read.
3	R	0	FE Framing Error This is used to indicate the occurrence of a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. In the FIFO mode, since the framing error is associated with a character received, it is revealed when the character with the framing error is at the top of the FIFO. When a framing error occurs, the UART tries to resynchronize. It does this by assuming that the error was due to the start bit of the next character and then continues receiving the other bit i.e. data, and/or parity and stop. It should be noted that the Framing Error (FE) bit (LSR[3]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). 0: no framing error 1:framing error Reading the LSR clears the FE bit.
2	R	0	PE Parity Error This is used to indicate the occurrence of a parity error in the receiver if the Parity Enable (PEN) bit (LCR[3]) is set. In the FIFO mode, since the parity error is associated with a character received, it is revealed when the

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			character with the parity error arrives at the top of the FIFO. It should be noted that the Parity Error (PE) bit (LSR[2]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). 0: no parity error 1: parity error Reading the LSR clears the PE bit.
1	R	0	OE Overrun Error This occurs if a new data character was received before the previous data was read. In the non-FIFO mode, the OE bit is set when a new character arrives in the receiver before the previous character was read from the RBR. When this happens, the data in the RBR is overwritten. In the FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost. 0: no overrun error 1: overrun error Reading the LSR clears the OE bit.
0	R	0	DR Data Ready This is used to indicate that the receiver contains at least one character in the RBR or the receiver FIFO. 0: no data ready 1: data ready This bit is cleared when the RBR is read in non-FIFO mode, or when the receiver FIFO is empty, in FIFO mode.

7.4.7.11. UART Modem Status Register

Offset: 0x18			Register Name: UART_MSR_REG
Bit	R/W	Default/Hex	Description
31:8	/	/	/
7	R	0	DCD Line State of Data Carrier Detect This is used to indicate the current state of the modem control line dcd_n. This bit is the complement of dcd_n. When the Data Carrier Detect input (dcd_n) is asserted it is an indication that the carrier has been detected by the modem or data set. 0: dcd_n input is De-asserted (logic 1) 1: dcd_n input is asserted (logic 0)
6	R	0	RI Line State of Ring Indicator This is used to indicate the current state of the modem control line ri_n. This bit is the complement of ri_n. When the Ring Indicator input (ri_n) is asserted it is an indication that a telephone ringing signal has been received by the modem or data set.

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0: ri_n input is De-asserted (logic 1) 1: ri_n input is asserted (logic 0)
5	R	0	DSR Line State of Data Set Ready This is used to indicate the current state of the modem control line dsr_n. This bit is the complement of dsr_n. When the Data Set Ready input (dsr_n) is asserted it is an indication that the modem or data set is ready to establish communications with UART. 0: dsr_n input is De-asserted (logic 1) 1: dsr_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), DSR is the same as MCR[0] (DTR).
4	R	0	CTS Line State of Clear To Send This is used to indicate the current state of the modem control line cts_n. This bit is the complement of cts_n. When the Clear to Send input (cts_n) is asserted it is an indication that the modem or data set is ready to exchange data with UART. 0: cts_n input is De-asserted (logic 1) 1: cts_n input is asserted (logic 0) In Loopback Mode (MCR[4] = 1), CTS is the same as MCR[1] (RTS).
3	R	0	DDCD Delta Data Carrier Detect This is used to indicate that the modem control line dcd_n has changed since the last time the MSR was read. 0: no change on dcd_n since last read of MSR 1: change on dcd_n since last read of MSR Reading the MSR clears the DDCD bit. Note: Ff the DDCD bit is not set and the dcd_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDCD bit is set when the reset is removed if the dcd_n signal remains asserted.
2	R	0	TERI Trailing Edge Ring Indicator This is used to indicate that a change on the input ri_n (from an active-low to an inactive-high state) has occurred since the last time the MSR was read. 0: no change on ri_n since last read of MSR 1: change on ri_n since last read of MSR Reading the MSR clears the TERI bit.
1	R	0	DDSR Delta Data Set Ready This is used to indicate that the modem control line dsr_n has changed since the last time the MSR was read. 0: no change on dsr_n since last read of MSR 1: change on dsr_n since last read of MSR Reading the MSR clears the DDSR bit. In Loopback Mode (MCR[4] = 1),

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			DDSR reflects changes on MCR[0] (DTR). Note: If the DDSR bit is not set and the dsr_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDSR bit is set when the reset is removed if the dsr_n signal remains asserted.
0	R	0	DCTS Delta Clear to Send This is used to indicate that the modem control line cts_n has changed since the last time the MSR was read. 0: no change on ctsdsr_n since last read of MSR 1: change on ctsdsr_n since last read of MSR Reading the MSR clears the DCTS bit. In Loopback Mode (MCR[4] = 1), DCTS reflects changes on MCR[1] (RTS). Note: If the DCTS bit is not set and the cts_n signal is asserted (low) and a reset occurs (software or otherwise), then the DCTS bit is set when the reset isremoved if the cts_n signal remains asserted.

7.4.7.12. UART Scratch Register

Offset: 0x1C			Register Name: UART_SCH_REG
Bit	R/W	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0	SCRATCH_REG Scratch Register This register is for programmers to use as a temporary storage space. It has no defined purpose in the UART.

7.4.7.13. UART Status Register

Offset: 0x7C			Register Name: UART_USR_REG
Bit	R/W	Default/Hex	Description
31:5	/	/	/
4	R	0	RFF Receive FIFO Full This is used to indicate that the receive FIFO is completely full. 0: Receive FIFO not full 1: Receive FIFO Full This bit is cleared when the RX FIFO is no longer full.
3	R	0	RFNE Receive FIFO Not Empty This is used to indicate that the receive FIFO contains one or more entries. 0: Receive FIFO is empty 1: Receive FIFO is not empty This bit is cleared when the RX FIFO is empty.
2	R	1	TFE Transmit FIFO Empty This is used to indicate that the transmit FIFO is completely empty. 0: Transmit FIFO is not empty

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: Transmit FIFO is empty This bit is cleared when the TX FIFO is no longer empty.
1	R	1	TFNF Transmit FIFO Not Full This is used to indicate that the transmit FIFO in not full. 0: Transmit FIFO is full 1: Transmit FIFO is not full This bit is cleared when the TX FIFO is full.
0	R	0	BUSY UART Busy Bit 0: Idle or inactive 1: Busy

7.4.7.14. UART Transmit FIFO Level Register

Offset: 0x80			Register Name: UART_TFL_REG
Bit	R/W	Default/Hex	Description
31:7	/	/	/
6:0	R	0	TFL Transmit FIFO Level This is indicates the number of data entries in the transmit FIFO.

7.4.7.15. UART Receive FIFO Level Register

Offset: 0x84			Register Name: UART_RFL_REG
Bit	R/W	Default/Hex	Description
31:7	/	/	/
6:0	R	0	RFL Receive FIFO Level This is indicates the number of data entries in the receive FIFO.

7.4.7.16. UART Halt TX Register

Offset: 0xA4			Register Name: UART_HALT_REG
Bit	R/W	Default/Hex	Description
31:6	/	/	/
5	R/W	0	SIR_RX_INVERT SIR Receiver Pulse Polarity Invert 0: Not invert receiver signal 1: Invert receiver signal
4	R/W	0	SIR_TX_INVERT SIR Transmit Pulse Polarity Invert 0: Not invert transmit pulse 1: Invert transmit pulse
3	/	/	/
2	R/W	0	CHANGE_UPDATE After the user using HALT[1] to change the baudrate or LCR configuration, write 1 to update the configuration and waiting this bit self clear to 0 to

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			finish update process. Write 0 to this bit has no effect. 1: Update trigger, Self clear to 0 when finish update.
1	R/W	0	CHCFG_AT_BUSY This is an enable bit for the user to change LCR register configuration (except for the DLAB bit) and baudrate register (DLH and DLL) when the UART is busy (USB[0] is 1). 1: Enable change when busy
0	R/W	0	HALT_TX Halt TX This register is use to halt transmissions for testing, so that the transmit FIFO can be filled by the master when FIFOs are implemented and enabled. 0 : Halt TX disabled 1 : Halt TX enabled Note: If FIFOs are not enabled, the setting of the halt TX register has no effect on operation.

7.4.7.17. UART DBG DLL Register

Offset: 0xB0			Register Name: UART_DBG_DLL_REG
Bit	R/W	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0	DEBUG DLL

7.4.7.18. UART DBG DLH Register

Offset: 0xB4			Register Name: UART_DBG_DLH_REG
Bit	R/W	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0	DEBUG DLH

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

7.5. RSB

7.5.1. Overview

The reduced serial bus(RSB) Host Controller is designed to communicate with RSB Device using two push-pull wires. It supports a simplified two wire protocol (RSB) on a push-pull bus. The transfer speed can be up to 20MHz and the performance will be improved much.

7.5.2. Feature

The RSB includes the following features:

- Support industry-standard AMBA Peripheral Bus (APB) and it is fully compliant with the AMBA Specification, Revision 2.0.
- Support speed up to 20MHz with ultra low power
- Support Push-Pull bus
- Support Host mode
- Support programmable output delay of CD signal
- Support parity check for address and data transmission
- Support multi-devices

7.5.3. Terminology Definition

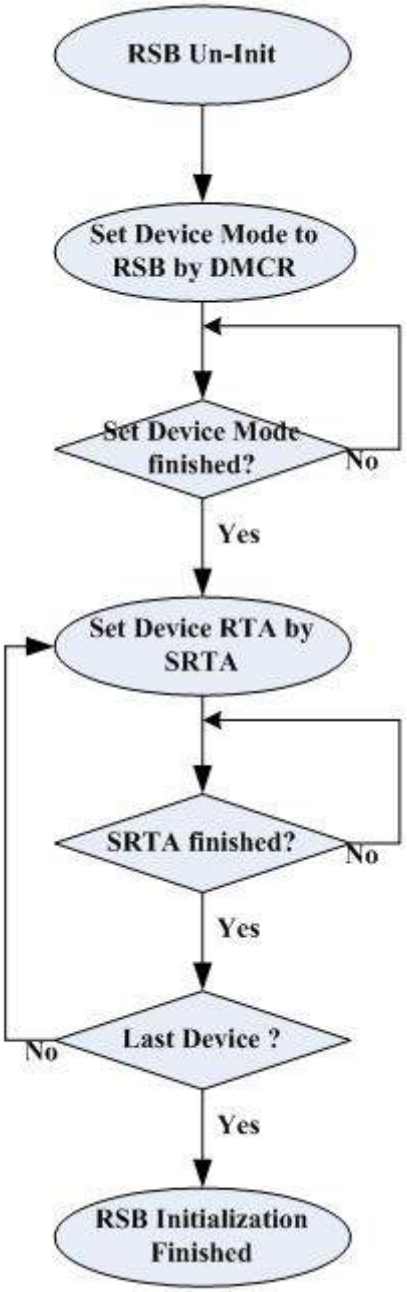
TERM	Description
CK	A line that is used to transmit clock from Host to Device
CD	A line that is used to transmit Command and Data between Host and Device
DA	Device Address is a 16bits address that is the ID of each type device.
RTA	Run-Time Address is an 8bits address that is used to address device during Read or Write transmission. The valid RTA is 0x17 0x2D 0x3A 0x4E 0x59 0x63 0x74 0x8B 0x9C 0xA6 0xB1 0xC5 0xD2 0xE8 and 0xFF.
HD	Host to Device Handshake is used to change the ownership of CD from Host to Device.
DH	Device to Host Handshake is used to change the ownership of CD from Device to Host.
SB	Start Bit: a HIGH to LOW transition on the CD while CK is high.

7.5.4. RSB Command Set

Command	Value	Description
SRTA	0xE8	Set Run-Time-Address
RD8	0x8B	Read one byte from Device
RD16	0x9C	Read two bytes from Device
RD32	0xA6	Read four bytes from Device
WR8	0x4E	Write one byte to Device
WR16	0x59	Write two bytes to Device
WR32	0x63	Write four bytes to Device

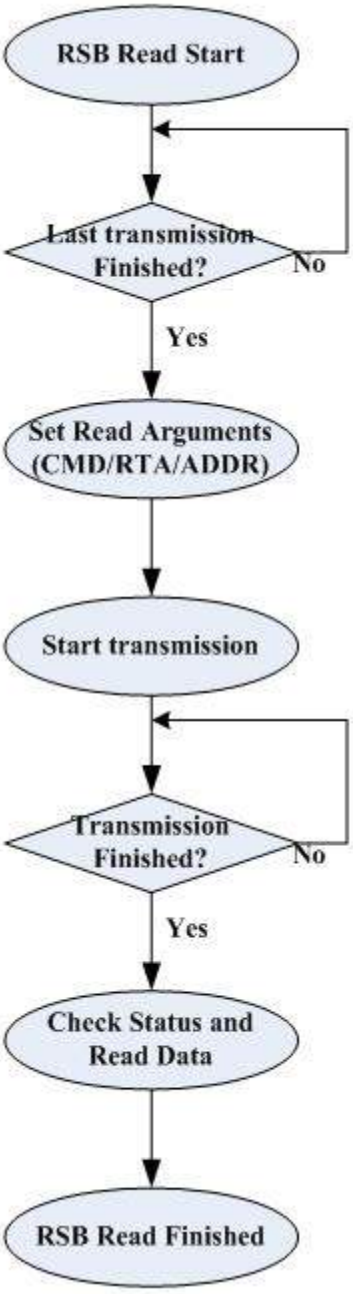
 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

7.5.5. Software Operation Flow



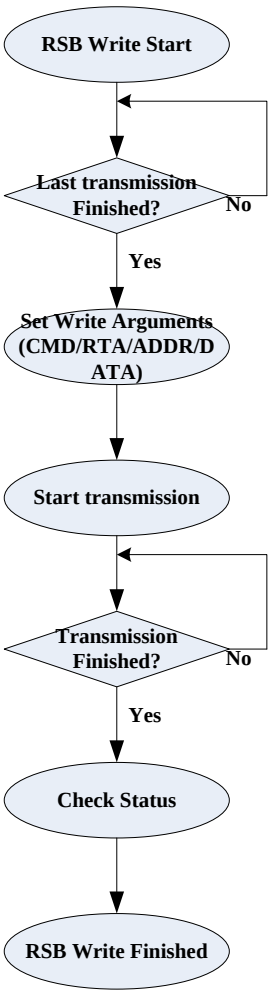
RSB System Initialization

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.



RSB Read from Device

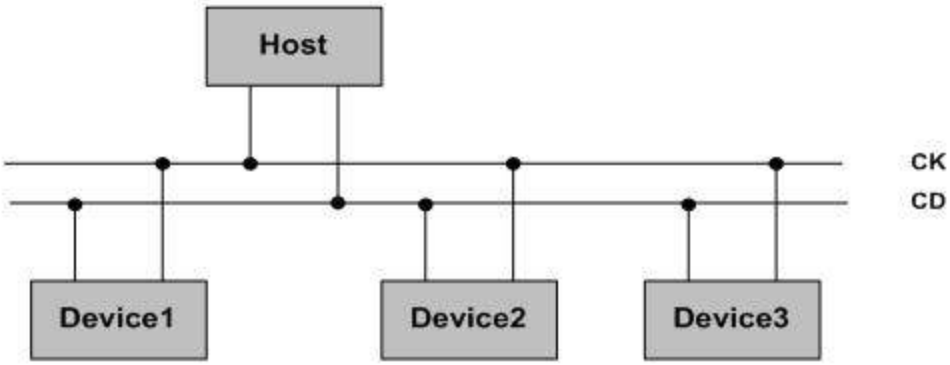
 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.



RSB Write to Device

7.5.6. RSB General Specification

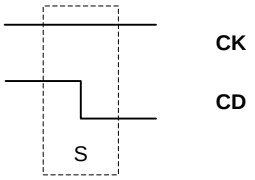
RSB uses push-pull bus，and supports multi-devices. It uses CK as clock and uses CD to transmit command and data. The Bus Topology is showed below:



RSB Bus Topology

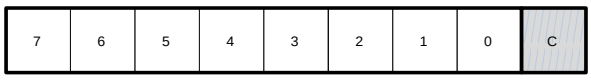
The start bit marks the beginning of a transaction. The Start bit is defined as a HIGH to LOW transition on the CD while CK is high.

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.



Start signal

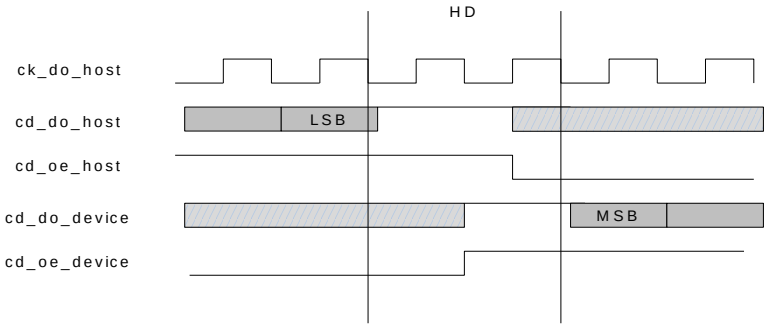
RSB protocol uses parity bit to check the correction of address and data.



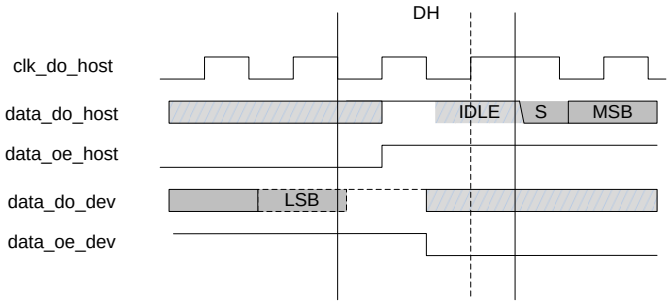
Parity bit

ACK bit is the acknowledgement from device to host, The ACK is low active. When device finds the parity bit is error, it will not send ACK to host, so host can know that an error happens in the transaction.

Both Host and Device can drive the CD, so there are two handshakes, HD (host to device) and DH (device to host), for Host and device to convert the direction of data transmission.



HD Handshake



DH Handshake

To improve transaction efficiency and to be flexible in device address assignment, RSB use Device Address (DA) and Run-Time Address (RTA). RTA is assigned dynamically by host. Host software shall ensure that different device has different RTA in the same system. Device's default RTA is 0 and 0 is the reserved address. If RTA is 0 when setting RTA, the setting is invalid.

There are three command types in RSB:

1) Set run-time address (RTA): It is used to set run time address (RTA) for different devices in the same system. There are 15 devices in a system at most. The RTA can be selected from the RTA code set and a device's RTA can be modified many times by using set run-time address command.

SRTA Timing

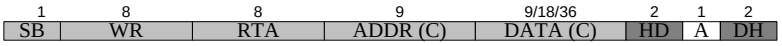
2) Read command: It is used to read data from device. It has byte, half word and word operation. When the device

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

receives the command, they shall check if the command's RTA matches their own RTA.

Read Timing

3) Write command: It is used to write data to the devices. It has byte, half word and word operation. When the device receives the command, they shall check if the command's RTA matches their own RTA.



Write Timing

7.5.7. RSB Controller Register List

Module Name	Base Address
RSB	0x08003400

Register Name	Offset	Description
RSB_CTRL_REG	0x0000	RSB Control Register
RSB_CCR_REG	0x0004	RSB Clock Control Register
RSB_INTE_REG	0x0008	RSB Interrupt Enable Register
RSB_STAT_REG	0x000C	RSB Status Register
RSB_AR_REG	0x0010	RSB Address Register
RSB_DATA_REG	0x001C	RSB Data Buffer Register
RSB_LCR_REG	0x0024	RSB Line Control register
RSB_DMCR_REG	0x0028	RSB Device Mode Control register
RSB_CMD_REG	0x002C	RSB Command Register
RSB_DAR_REG	0x0030	RSB Device address Register

7.5.8. RSB Register Description

7.5.8.1. RSB Control Register

Offset: 0x00			Register Name: RSB_CTRL_REG
Bit	R/W	Default/Hex	Description
7	R/W	0	START_TRANS Write ‘1’ to this bit will start a new transmission with the configuration of other registers. It is cleared to ‘0’ automatically when the transaction completes or an error happens in the transmission.
6	R/W	0	ABORT_TRANS Write ‘1’ to this bit will abort the current transmission. It is cleared to ‘0’ automatically when the transmission has been aborted.
5:2	/	/	/
1	R/W	0	GLOBAL_INT_ENB Global interrupt enable bit 1 – enable interrupt

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0 – disable interrupt
0	R/W	0	Soft Reset Write '1' to this bit will reset the controller into default state. All of the status of controller will be cleared. And this bit will be cleared to '0' automatically when reset operation completes.

7.5.8.2. RSB Clock Control Register

Offset: 0x04			Register Name: RSB_CCR_REG
Bit	R/W	Default/Hex	Description
31:11	/	/	/
10:8	R/W	0	CD_ODLY CD output delay Delay time of n source clock cycles before output CD signal.
7:0	R/W	0	CK_DIV $F_{ck} = F_{source} / 2*(divider+1)$

7.5.8.3. RSB Interrupt Enable Register

Offset: 0x08			Register Name: RSB_INTE_REG
Bit	R/W	Default/Hex	Description
31:3	/	/	/
2	R/W	0	LOAD_BSY_ENB Loading Busy Interrupt Enable 1 – enable 0 – disable
1	R/W	0	TRANS_ERR_ENB Transfer Error Interrupt Enable 1 – enable 0 – disable
0	R/W	0	TRANS_OVER_ENB Transfer complete Interrupt Enable 1 – enable 0 – disable

7.5.8.4. RSB Status Register

Offset: 0x0C			Register Name: RSB_INTS_REG
Bit	R/W	Default/Hex	Description
31:17	/	/	/
16	R	0	TRANS_ERR_ACK. If a negative ACK is received from Device, then this bit is set to '1' by hardware. This bit is cleared when a new transmission is started.
15:12	/	/	/
11:8	R	0	TRANS_ERR_DATA If the parity check of 1st byte is negative, then bit8 is set to '1' by hardware. If the parity check of 2nd byte is negative, then bit9 is set to '1' by hardware; and so on. These bits are cleared when a new transmission is started.

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

7:3	/	/	/
2	R/W	0	LOAD_BSY Loading Busy Flag If software writes any control registers during transmission, this bit will be set to '1'. If LOAD_BSY_ENB=1, an interrupt will be generated. Software can clear this flag by writing '1' to this bit.
1	R/W	0	TRANS_ERR Transfer Error Flag If an error happened during transmission, This bit will be set to '1'. If TRANS_ERR_ENB=1, an interrupt will be generated. Software can clear this flag by writing '1' to this bit.
0	R/W	0	TRANS_OVER Transfer Over Flag If the transmission has transferred over, this bit is set to '1'. If TRANS_OVER_ENB=1, an interrupt will be generated. Software can clear this flag by writing '1' to this bit.

7.5.8.5. RSB Address Register

Offset: 0x10			Register Name: RSB_AR_REG
Bit	R/W	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0	ADDR The ADDR is send to device during Read and Write command.

7.5.8.6. RSB Data Buffer Register

Offset: 0x1C			Register Name: RSB_DATA_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0	RSB DATA If the command is configured as read, Software can read this register to get the data from device; If the command is configured as write, Software can write this register to send the data to device. If the command is rd8 or wr8, then the low byte is active; If the command is rd16 or wr16, then the low two byte is active; If the command is rd32 or wr32, then the whole word is active

7.5.8.7. RSB Line Control Register

Offset: 0x24			Register Name: RSB_LCR_REG
Bit	R/W	Default/Hex	Description
31:6	/	/	/
5	R	1	CK_STATE Current state of CK pin 0 – low 1 - high
4	R	1	CD_STATE

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Current state of CD pin 0 – low 1 – high
3	R/W	1	CK_CTL CK line state control bit When line control mode is enabled (bit[2] set), value of this bit decide the output level of CK 0 – output low level 1 – output high level
2	R/W	0	CK_CTL_EN CK line state control enable When this bit is set, the state of CK is control by the value of bit[3]. 0-disable CK line control mode 1-enable CK line control mode
1	R/W	1	CD_CTL CD line state control bit When line control mode is enabled (bit[0] set), value of this bit decide the output level of CD 0 – output low level 1 – output high level
0	R/W	0	CD_CTL_EN CD line state control enable When this bit is set, the state of CD is control by the value of bit [1]. 0-disable CD line control mode 1-enable CD line control mode

7.5.8.8. RSB Device Mode Control Register

Offset: 0x28			Register Name: RSB_DMCR_REG
Bit	R/W	Default/Hex	Description
31	R/W	0	DEVICE_MODE_START When set to '1', host will send DEVICE_MODE to device to switch the device's bus mode from NTWI to RSB. This bit will be self-cleared when DEVICE_MODE is sent onto the RSB bus.
30:24	/	/	/
23:0	R/W	0x3e3e00	DEVICE_MODE Data The data send to device during DEVICE_MODE

7.5.8.9. RSB Command Register

Offset: 0x2C			Register Name: RSB_CMD_REG
Bit	R/W	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0	CMD_IDX command index

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

7.5.8.10. RSB Device Address Register

Offset: 0x30			Register Name: RSB_DAR_REG
Bit	R/W	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0	RTA Run-Time Address
15:0	R/W	0	DA Device Address

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

7.6. CIR Receiver

7.6.1. Overview

CIR receiver is implemented in hardware to save CPU resource. It samples the input signals on the programble frequency and records these samples into RX FIFO when one CIR signal is found on the air. The CIR receiver uses Run-Length Code (RLC) to encode pulse width, and the encoded data is buffered in a 64 levels and 8-bit width RX FIFO: the MSB bit is used to record the polarity of the receiving CIR signal (The high level is represented as 1 and the low level is represented as 0), and the rest 7 bits are used for the length of RLC. The maximum length is 128. If the duration of one level (high or low) is more than 128, another byte is used. Since there are always some noises in the air, a threshold can be set to filter the noises to reduce system loading and improve system stability.

7.6.2. Feature

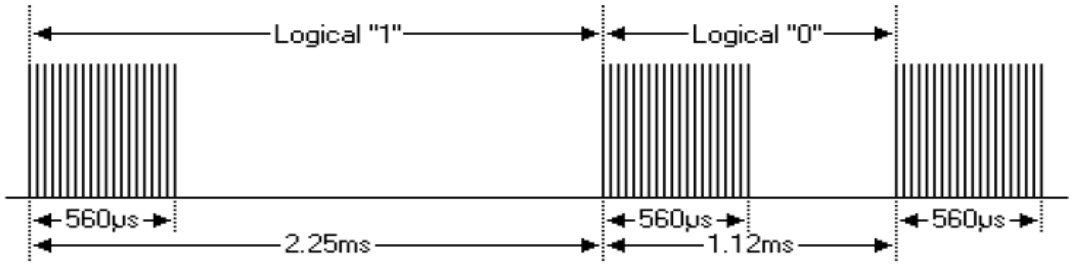
The CIR includes the following features:

- Support APB 16-bits bus width
- Full physical layer implementation
- Support CIR for remote control
- 64x8bits FIFO for data buffer
- Programmable FIFO threshold

7.6.3. Timing

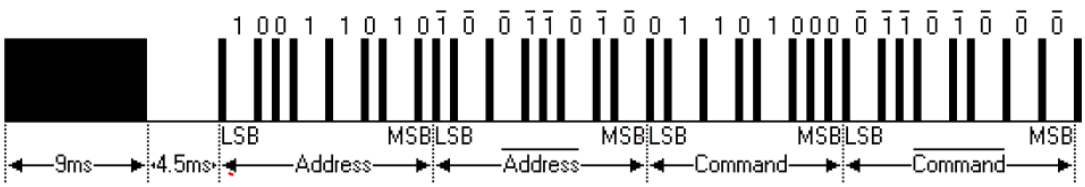
CIR contains many protocols which designed by different manufacturers. Here to NEC protocol as an example: A message is started by a 9ms AGC burst, which was used to set the gain of the earlier IR receivers. This AGC burst is then followed by a 4.5ms space, which is then followed by the address and command.

Bit definition: the logical “1” takes 2.25ms to transmit, while a logical “0” is only 1.12ms.



Bit Definition

Timing for a message:



 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

7.6.4. CIR Receiver Register List

Module Name	Base Address
CIR	0x01C22C00

Register Name	Offset	Description
CIR_CTRL_REG	0x00	CIR Control Register
CIR_RXCTL_REG	0x10	CIR Receiver Configure Register
CIR_RXFIFO_REG	0x20	CIR Receiver FIFO Register
CIR_RXINT_REG	0x2C	CIR Receiver Interrupt Control Register
CIR_RXSTA_REG	0x30	CIR Receiver Status Register
CIR_CONFIG_REG	0x34	CIR Configure Register

7.6.5. CIR Receiver Register Description

7.6.5.1. CIR Control Register

Offset: 0x00			Register Name: CIR_CTRL_REG
Bit	R/W	Default/Hex	Description
31:9	/	/	/
8	R/W	0	CGPO General Program Output (GPO) Control in CIR mode for TX Pin 0: Low level 1: High level
7:6	/	/	/
5:4	R/W	0	CIR ENABLE 00~10: Reserved 11: CIR mode enable
3:2	/	/	/.
1	R/W	0	RXEN Receiver Block Enable 0: Disable 1: Enable
0	R/W	0	GEN Global Enable A disable on this bit overrides any other block or channel enables and flushes all FIFOs. 0: Disable 1: Enable

7.6.5.2. CIR Receiver Configure Register

Offset: 0x10			Register Name: CIR_RXCTL_REG
Bit	R/W	Default/Hex	Description
31:3	/	/	/
2	R/W	1	RPPI

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Receiver Pulse Polarity Invert 0: Not invert receiver signal 1: Invert receiver signal
1:0	/	/	/

7.6.5.3. CIR Receiver FIFO Register

Offset: 0x20			Register Name: CIR_RXFIFO_REG
Bit	R/W	Default/Hex	Description
31:8	/	/	/
7:0	R	0	Receiver Byte FIFO

7.6.5.4. CIR Receiver Interrupt Control Register

Offset: 0x2C			Register Name: CIR_RXINT_REG
Bit	R/W	Default/Hex	Description
31:14	/	/	/
13:8	R/W	0	RAL RX FIFO Available Received Byte Level for interrupt and DMA request TRIGGER_LEVEL = RAL + 1
5	R/W	0	DRQ_EN RX FIFO DMA Enable 0: Disable 1: Enable When set to '1', the Receiver FIFO DRQ is asserted if reaching RAL. The DRQ is De-asserted when condition fails.
4	R/W	0	RAI_EN RX FIFO Available Interrupt Enable 0: Disable 1: Enable When set to '1', the Receiver FIFO IRQ is asserted if reaching RAL. The IRQ is De-asserted when condition fails.
3:2	/	/	/
1	R/W	0	RPEI_EN Receiver Packet End Interrupt Enable 0: Disable 1: Enable
0	R/W	0	ROI_EN Receiver FIFO Overrun Interrupt Enable 0: Disable 1: Enable

7.6.5.5. CIR Receiver Status Register

Offset: 0x30			Register Name: CIR_RXSTA_REG
Bit	R/W	Default/Hex	Description
31:15	/	/	/
14:8	R	0	RAC

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			RX FIFO Available Counter 0: No available data in RX FIFO 1: 1 byte available data in RX FIFO 2: 2 byte available data in RX FIFO … 64: 64 byte available data in RX FIFO
7	R	0	STAT Status of CIR 0:Idle 1:busy
4	R/W	0	RA RX FIFO Available 0: RX FIFO not available according its level 1: RX FIFO available according its level This bit is cleared by writing a ‘1’.
3:2	/	/	/
1	R/W	0	RPE Receiver Packet End Flag 0: STO was not detected. In CIR mode, one CIR symbol is receiving or not detected. 1: STO field or packet abort symbol (7’b0000,000 and 8’b0000,0000 for MIR and FIR) is detected. In CIR mode, one CIR symbol is received. This bit is cleared by writing a ‘1’.
0	R/W	0	ROI Receiver FIFO Overrun 0: Receiver FIFO not overrun 1: Receiver FIFO overrun This bit is cleared by writing a ‘1’.

7.6.5.6. CIR Configure Register

Offset: 0x34			Register Name: CIR_CONFIG_REG
Bit	R/W	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	SCS2 Bit2 of Sample Clock Select for CIR This bit is defined by SCS bits below.
23	R/W	0x0	ATHC Active Threshold Control for CIR 0x0 –ATHR in Unit of (Sample Clock) 0x1 –ATHR in Unit of (128*Sample Clocks)
22:16	R/W	0x0	ATHR Active Threshold for CIR These bits control the duration of CIR from Idle to Active State. The duration can be calculated by ((ATHR + 1)*(ATHC? Sample Clock: 128*Sample Clock)).

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

<table>
<tr><td>15:8</td><td>R/W</td><td>0x18</td><td>ITHR
Idle Threshold for CIR
The Receiver uses it to decide whether the CIR command has been received. If there is no CIR signal on the air, the receiver is staying in IDLE status. One active pulse will bring the receiver from IDLE status to Receiving status. After the CIR is end, the inputting signal will keep the specified level (high or low level) for a long time. The receiver can use this idle signal duration to decide that it has received the CIR command. The corresponding flag is asserted. If the corresponding interrupt is enableD, the interrupt line is asserted to CPU.
When the duration of signal keeps one status (high or low level) for the specified duration ((ITHR + 1)*128 sample_clk), this means that the previous CIR command has been finished.</td></tr>
<tr><td>7:2</td><td>R/W</td><td>0xa</td><td>NTHR
Noise Threshold for CIR
When the duration of signal pulse (high or low level) is less than NTHR, the pulse is taken as noise and should be discarded by hardware.
0: all samples are recorded into RX FIFO
1: If the signal is only one sample duration, it is taken as noise and discarded.
2: If the signal is less than (<=) two sample duration, it is taken as noise and discarded.
…
61: if the signal is less than (<=) sixty-one sample duration, it is taken as noise and discarded.</td></tr>
<tr><td>1:0</td><td>R/W</td><td>0</td><td>SCS
Sample Clock Select for CIR
<table>
<tr><td>SCS2</td><td>SCS[1]</td><td>SCS[0]</td><td>Sample Clock</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>ir_clk/64</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>ir_clk/128</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>ir_clk/256</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>ir_clk/512</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>ir_clk</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Reserved</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Reserved</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Reserved</td></tr>
</table>
</td></tr>
</table>

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

7.7. USB-OTG

7.7.1. Overview

The USB OTG is dual-role USB controller supporting Host and device functions. It can also be configured as a Host-only or Device-only controller, full compliant with the USB 2.0 Specification. The USB OTG can support high-speed (HS, 480-Mbps), full-speed (FS, 12-Mbps), and low-speed (LS, 1.5-Mbps) transfers in Host mode, support high-speed (HS, 480-Mbps) and full-speed (FS, 12-Mbps) in Device mode.

7.7.2. Feature

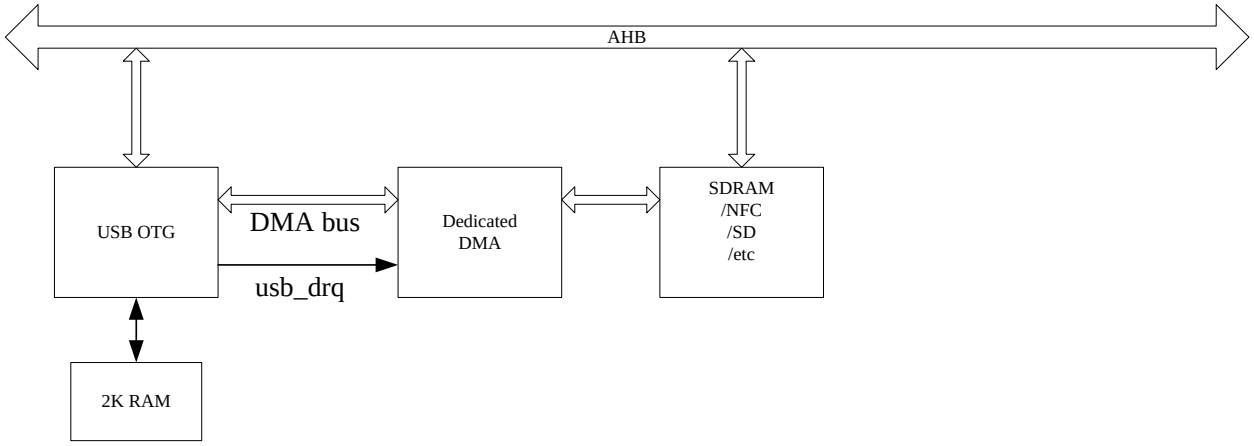
The USB-OTG includes the following features:

- 64-Byte Endpoint 0 for Control Transfer
- Support up to 6 User-Configurable Endpoints(TX Endpoint 1/2/3 and RX Endpoint 1/2/3) for Bulk, Isochronous, Control and Interrupt bi-directional transfers
- Support High-Bandwidth Isochronous & Interrupt transfers
- Support point-to-point and point-to-multipoint transfer in both Host and Peripheral mode

7.7.3. Functionalities Description

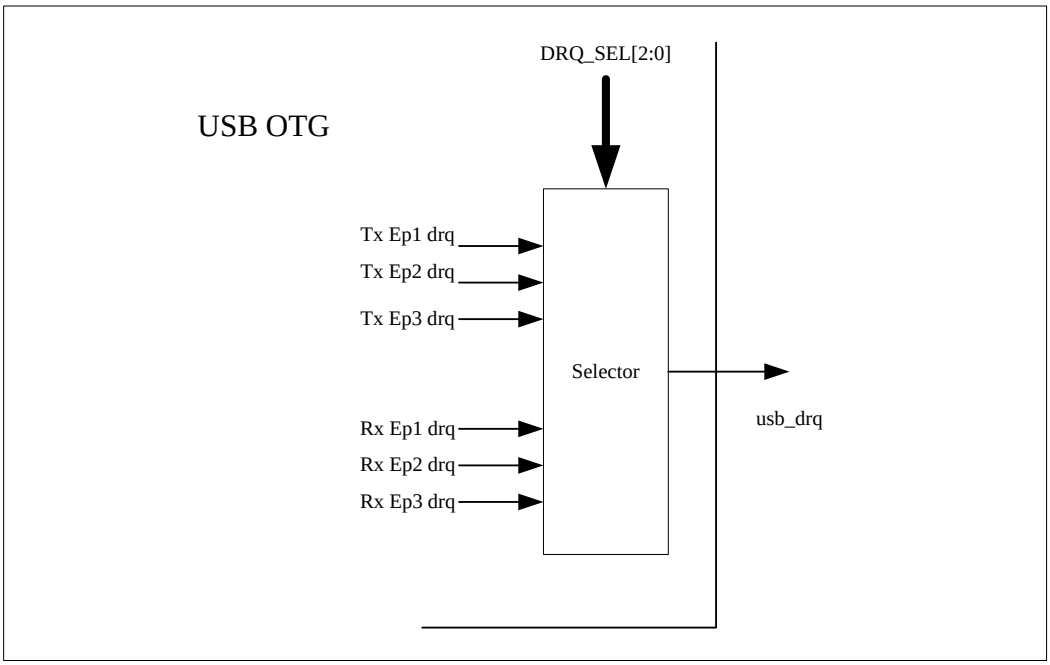
7.7.3.1. DMA Support

The USB-OTG supports DMA access or IO method to the FIFO for TX Endpoints 1-3 and RX Endpoints 1-3. For saving AHB bus bandwidth, one dedicated DMA operation is recommended. The method can be selected by CPU host. When BUS_SEL is '0' in the register of USB_EFR, Endpoints' FIFO is accessed by CPU host through IO method on ABH bus. When BUS_SEL is '1' in the register of USB_EFR, Endpoints' FIFO is accessed by dedicated DMA engine. Any operation of FIFO ports by CPU host is unpredictable. But CPU host can access other registers by AHB bus.



USB-OTG DMA Block Diagram

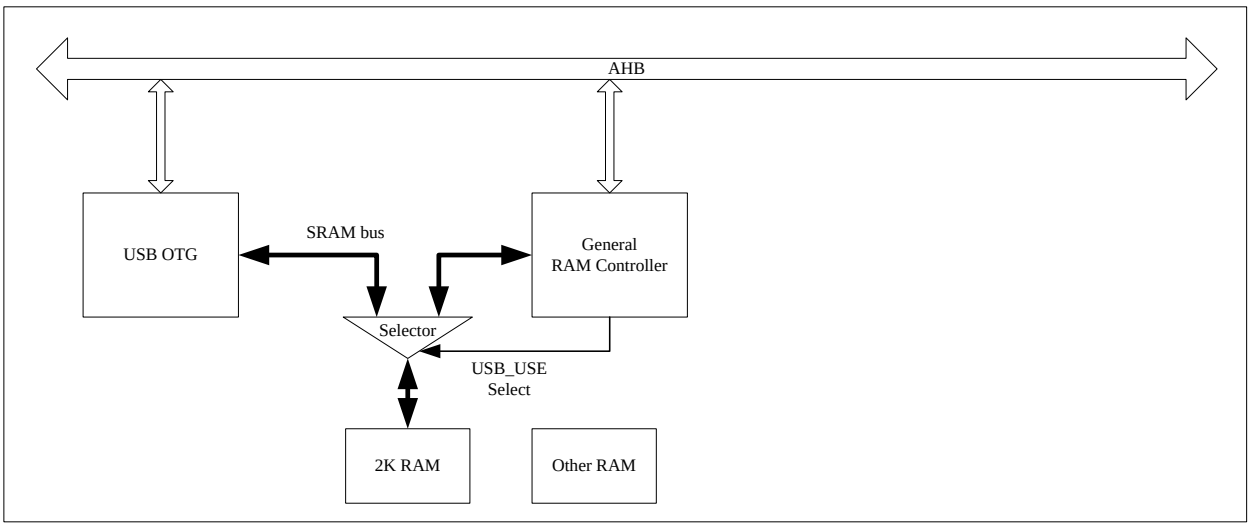
 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.



USB-OTG DMA Request Line Select

Since there is only one usb_req signal connected to dedicated DMA engine, but separate DMA request line for each TX endpoint and each RX endpoint in internal of USB. A total of six DMA request lines are implemented. The lines of DMA_REQ[0], DMA_REQ[1], DMA_REQ[2] are associated with TX EP1, EP2, EP3. The lines of DMA_REQ[4], DMA_REQ[5], DMA_REQ[6] are associated with Rx EP1, EP2, EP3. CPU host can select the source of usb_req signal for DMA request.

7.7.3.2. RAM Sharing



USB-OTG RAM Sharing Diagram

For saving memory area, 2K byte Single Port RAM is shared with other engines. When USB-OTG function is disabled, the RAM can be used by other engines. The single 2K bytes RAM with 32-bit width are requested by USB-OTG. General RAM controller can decide whether USB-OTG can use this RAM. In default state, the RAM is used by other engine. And when USB_USE bit is set to '1' in General RAM controller, the RAM is used by USB-OTG. The General RAM controller is in

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

charge of the 2K bytes RAM address space allocation.

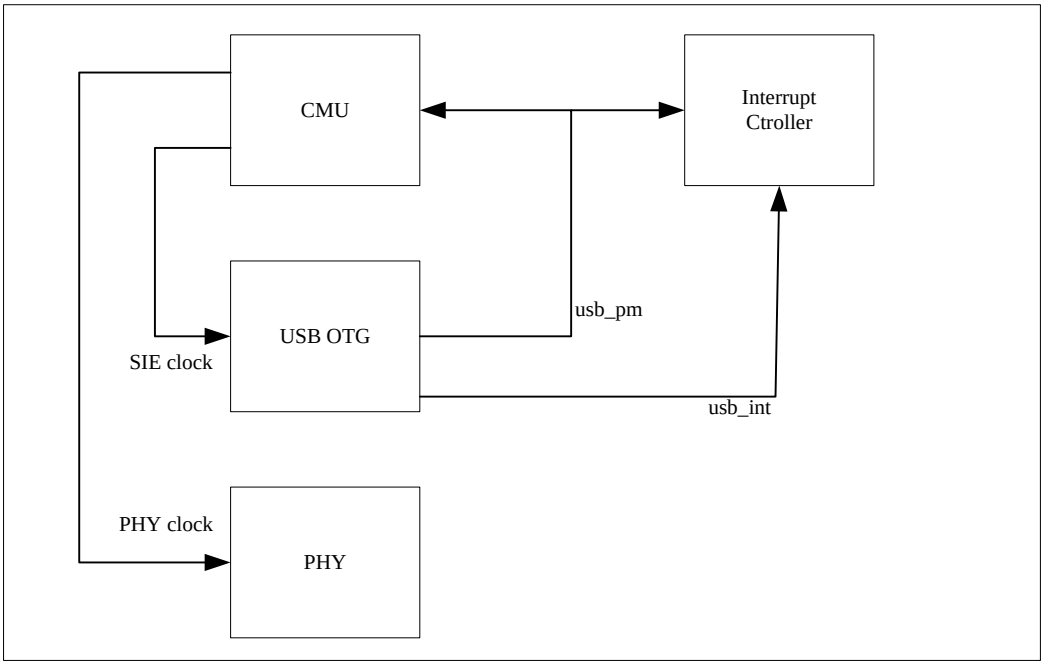
7.7.3.3. Power Save

For power saving, after system is powered and USB SIE and its PHY are reset, the clocks to SIE and PHY are gating in default state. The signal POWERDWN which is output by SIE is used for active its clock. It is de-asserted (asynchronously) under the following conditions:

When no session is in progress: AVALID going high; D+/D- going high

When in Host Suspend mode: VBUSVALID going low; K state on the bus

When in Peripheral Suspend mode: AVALID going low; K state on the bus



USB-OTG Interrupt, Wakeup Diagram

This signal is outputted to System interrupt controller and System Clock Management Unit.

7.7.3.4. Clock Source and Frequency

There are two clocks for USB-OTG SIE module. One is from AHB bus and one is from UTMI Transceiver which is called USB-OTG PHY.

Name	Description
USB_CLK	System clock (provided by AHB bus clock). This clock needs to be >30MHz and up to 180MHz
USB_XCLK	Transceiver Macrocell clock. 60MHz

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

7.8. Digital Audio Interface

7.8.1. Overview

The Digital Audio Interface can be configured as I2S interface or PCM interface by software. When configured as I2S interface, it can support the industry standard format for I2S, left-justified, or right-justified. PCM is a standard method used to digital audio for transmission over digital communication channels. It supports linear 13 or 16-bits linear or 8-bit u-law or A-law commanded sample formats at 8K samples/s and can receive and transmit on any selection of four of the first four slots following PCM_SYNC.

7.8.2. Feature

The Digital Audio includes the following features:

- Supports industry-standard AMBA Peripheral Bus (APB) and it is fully compliant with the AMBA Specification, Revision 2.0
- Supports APB 32-bits bus width
- I2S or PCM configured by software
- Full-duplex synchronous serial interface
- Master / Slave Mode operation configured by software
- Audio data resolutions of 16, 20, 24
- I2S Audio data sample rate from 8kHz to 192kHz
- I2S Data format for standard I2S, Left Justified and Right Justified
- I2S support 2 channel output and 2 channel input
- PCM supports linear sample (8-bits or 16-bits), 8-bits u-law and A-law companded sample
- One 128x24-bits FIFO for data transmit, one 64x24-bits FIFO for data receive
- Programmable FIFO thresholds
- Interrupt and DMA Support
- Two 32-bits Counters for AV sync application
- Loopback mode for test

7.8.3. Signal Description

7.8.3.1. Digital Audio Interface Pin List

Signal Name	Direction(M)	Description	Pin
DA_LRCK	I/O	Digital Audio Sample Rate Clock/Sync	PB1/PD9/PE4/PA1
DA_BCLK	I/O	Digital Audio Serial Clock	PB0/PD8/PE3/PA0
DA_SDO0	O	Digital Audio Serial Data Output	PB3/PD11/PE6/PA3
DA_SDI	I	Digital Audio Serial Data Output	PB2/PD10/PE5/PA2
DA_MCLK	O	Digital Audio MCLK Output	PD7

7.8.3.2. Digital Audio Interface MCLK and BCLK

The Digital Audio Interface can support sampling rates from 128fs to 768fs, where fs is the audio sampling frequency typically 32kHz, 44.1kHz, 48kHz or 96kHz. For different sampling frequency, the tables list the coefficient value of

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

MCLKDIV and BCLKDIV.

Sampling Rate (kHz)	128fs	192fs	256fs	384fs	512fs	768fs
8	24	16	12	8	6	4
16	12	8	6	4	X	2
32	6	4	X	2	X	1
64	X	2	X	1	X	X
128	X	1	X	X	X	X
12	16	X	8	X	4	X
24	8	X	4	X	2	X
48	4	X	2	X	1	X
96	2	X	1	X	X	X
192	1	X	X	X	X	X

MCLKDIV value for 24.576MHz Audio Serial Frequency

Sampling Rate (kHz)	128fs	192fs	256fs	384fs	512fs	768fs
11.025	16	X	8	X	4	X
22.05	8	X	4	X	2	X
44.1	4	X	2	X	1	X
88.2	2	X	1	X	X	X
176.4	1	X	X	X	X	X

MCLKDIV value for 22.5792 MHz Audio Serial Frequency

Word Select Size	128fs	192fs	256fs	384fs	512fs	768fs
16	4	6	8	12	16	X
24	X	4	X	8	X	16
32	2	X	4	6	8	12

BCLKDIV value for Different Word Select Size

7.8.3.3. Digital Audio Interface Clock Source and Frequency

There are two clocks for Digital Audio Interface. One is from APB bus and one is from Audio PLL.

Name	Description
Audio_PLL	24.576Mhz or 22.528Mhz generated by Audio PLL
APB_CLK	APB bus system clock. In I2S mode, it is requested >= 0.25 BCLK. In PCM mode, it is requested >= 0.5 BCLK.

7.8.4. Functionalities Description

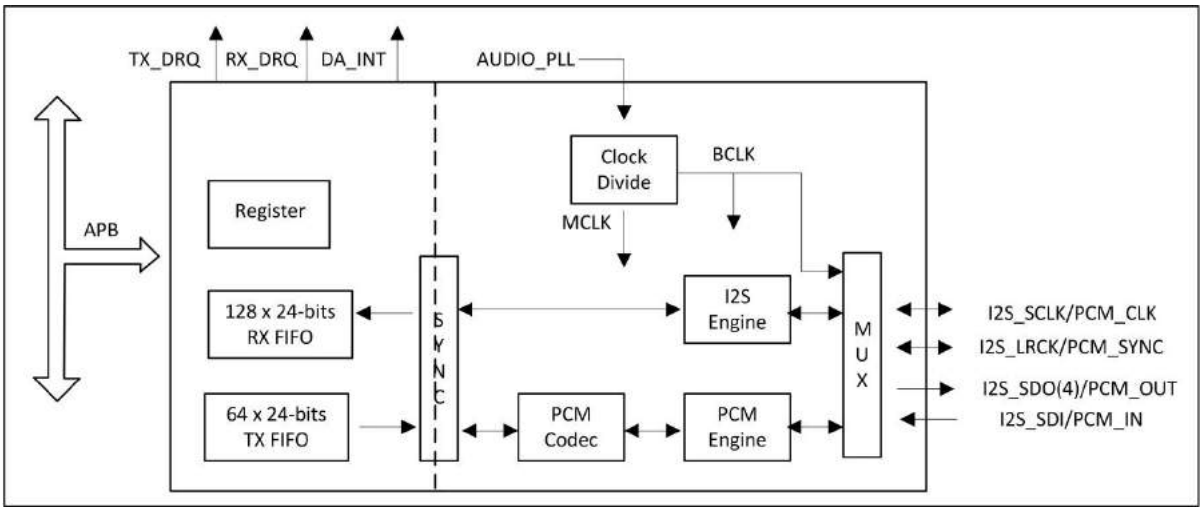
7.8.4.1. Typical Applications

The I2S and PRCM provide a serial bus interface for stereo and multichannel audio data. This interface is most commonly used by consumer audio market, including compact disc, digital audio tape, digital sound processors, and digital TV-sound.

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

7.8.4.2. Functional Block Diagram

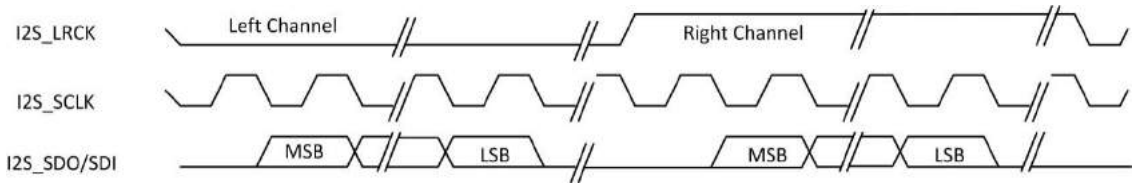
The digital audio interface block diagram is shown below:



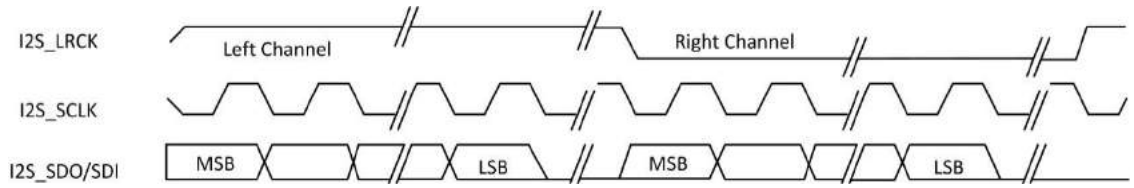
Digital Audio Interface System Block Diagram

7.8.4.3. Operation Principle

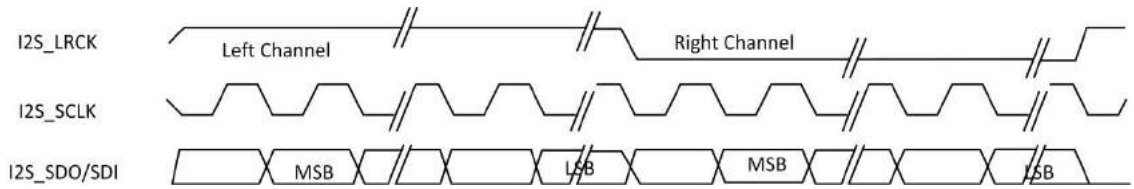
Digital Audio Interface Timing Diagram:



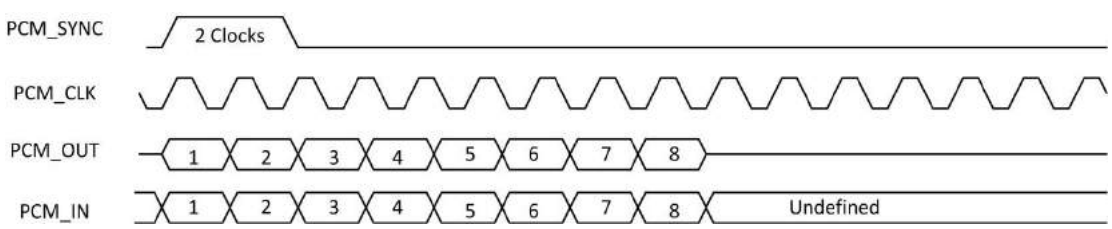
Standard I2S Timing Diagram



I2S Left-justified Timing Diagram

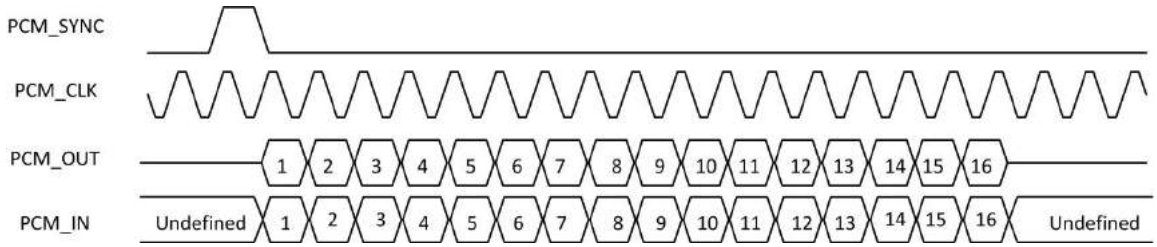


I2S Right-justified Timing Diagram



PCM Long Frame SYNC Timing Diagram (8-bits Companded Sample Example)

Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.



PCM Short Frame SYNC Timing Diagram

7.8.5. Operation Modes

The software operation of the I2S/PCM is divided into five steps: system setup, I2S/PCM initialization, the channel setup, DMA setup and Enable/Disable module. These five setups are described in detail in the following sections.

7.8.5.1. System setup and I2S/PCM initialization

The first step in the System setup is properly programming the GPIO. Since the I2S/PCM port is a multiplex pin, you can find the function in the pin multiplex specification. The clock source for the I2S/PCM should be followed. At first you must reset the audio PLL through the PLL_ENABLE bit of PLL_AUDIO_CTRL_REG in the CCU. The second step, you must setup the frequency of the audio pll in the PLL_AUDIO_CTRL_REG. After that, you must open the I2S/PCM gating through the DAUDIO_CLK_REG when you checkout that the LOCK bit of PLL_AUDIO_CTRL_REG become 1. At last, you must reset the I2S/PCM in the APB0_RST_REG and open the IIS/PCM bus gating in the BUS_GATING_REG2.

After the system setup, the register of I2S/PCM can be setup. At first, you should initialization the I2S/PCM. You should close the globe enable bit(DA_CTL[0]) , TX enable bit(DA_CTL[2]) and RX enable bit(DA_CTL[1]) by writing 0 to it. After that, you must clear the TX/RX FIFO by writing 0 to register DA_FCTL[25:24]. At last, you can clear the TX/RX FIFO counter by writing 0 to DA_TXCNT/DA_RXCNT.

7.8.5.2. The channel setup and DMA setup

Before the usage and control of I2S/PCM, you should setup the I2S/PCM of mater and slave. The configuration can be referred to the protocol of I2S/PCM. Then, you can set the translation mode, the sample precision, the wide of slot, the frame mode and the trigger level. The register set can be found in the spec.

The I2S/PCM supports three methods to transfer the data. The most common way is DMA, the set of DMA can be found in the DMA spec. In this module, you need to enable the DRQ.

7.8.5.3. Enable and disable the I2S/PCM

To enable the function, you can enable TX/RX by writing the DA_CTL[2:1]. After that, you must enable I2S/PCM by writing the Globe Enable bit to 1 in the DA_CTL. The disable process is to write the Globe Enable to 0.

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

7.8.6. Digital Audio Interface Register List

Module Name	Base Address
DA	0x01C22000

Register Name	Offset	Description
DA_CTRL_REG	0x00	Digital Audio Control Register
DA_FAT_REG0	0x04	Digital Audio Format Register 0
DA_FAT_REG1	0x08	Digital Audio Format Register 1
DA_TXFIFO_REG	0x0C	Digital Audio TX FIFO Register
DA_RXFIFO_REG	0x10	Digital Audio RX FIFO Register
DA_FCTL_REG	0x14	Digital Audio FIFO Control Register
DA_FSTA_REG	0x18	Digital Audio FIFO Status Register
DA_INT_REG	0x1C	Digital Audio Interrupt Control Register
DA_ISTA_REG	0x20	Digital Audio Interrupt Status Register
DA_CLKD_REG	0x24	Digital Audio Clock Divide Register
DA_TXCNT_REG	0x28	Digital Audio RX Sample Counter Register
DA_RXCNT_REG	0x2C	Digital Audio TX Sample Counter Register
DA_TXCHSEL_REG	0x30	Digital Audio TX Channel Select register
DA_TXCHMAP_REG	0x34	Digital Audio TX Channel Mapping Register
DA_RXCHSEL_REG	0x38	Digital Audio RX Channel Select register
DA_RXCHMAP_REG	0x3C	Digital Audio RX Channel Mapping Register

7.8.7. Digital Audio Interface Register Description

7.8.7.1. Digital Audio Control Register

Offset: 0x00			Register Name: DA_CTRL_REG
Bit	R/W	Default/Hex	Description
31:9	/	/	/
8	R/W	0	SDO0_EN 0: Disable 1: Enable
7	/	/	/
6	R/W	0	ASS Audio sample select when TX FIFO under run 0: Sending zero 1: Sending last audio sample
5	R/W	0	MS Master Slave Select 0: Master 1: Slave
4	R/W	0	PCM

Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0: I2S Interface 1: PCM Interface
3	R/W	0	LOOP Loop back test 0: Normal mode 1: Loop back test When set '1', connecting the SDO with the SDI in Master mode.
2	R/W	0	TXEN Transmitter Block Enable 0: Disable 1: Enable
1	R/W	0	RXEN Receiver Block Enable 0: Disable 1: Enable
0	R/W	0	GEN Globe Enable A disable on this bit overrides any other block or channel enables and flushes all FIFOs. 0: Disable 1: Enable

7.8.7.2. Digital Audio Format Register 0

Offset: 0x04			Register Name: DA_FAT_REG0
Bit	R/W	Default/Hex	Description
31:8	/	/	/
7	R/W	0	LRCP Left/ Right Clock Parity 0: Normal 1: Inverted In DSP/ PCM mode(only for short frame) 0: MSB is available on 2nd BCLK rising edge after LRC rising edge 1: MSB is available on 1st BCLK rising edge after LRC rising edge
6	R/W	0	BCP BCLK Parity 0: Normal 1: Inverted
5:4	R/W	0	SR Sample Resolution 00: 16-bits 01: 20-bits 10: 24-bits 11: Reserved
3:2	R/W	0x3	WSS Word Select Size

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			00: 16 BCLK 01: 20 BCLK 10: 24 BCLK 11: 32 BCLK
1:0	R/W	0	FMT Serial Data Format 00: Standard I2S Format 01: Left Justified Format 10: Right Justified Format 11: Reserved

7.8.7.3. Digital Audio Format Register 1

Offset: 0x08			Register Name: DA_FAT_REG1
Bit	R/W	Default/Hex	Description
31:15	/	/	/
14:12	R/W	0x4	PCM_SYNC_PERIOD PCM SYNC Period Clock Number 000: 16 BCLK period 001: 32 BCLK period 010: 64 BCLK period 011: 128 BCLK period 100: 256 BCLK period Others : Reserved
11	R/W	0	PCM_SYNC_OUT PCM Sync Out 0: Enable PCM_SYNC output in Master mode 1: Suppress PCM_SYNC whilst keeping PCM_CLK running. Some Codec utilize this to enter a low power state.
10	R/W	0	PCM Out Mute Write 1 force PCM_OUT to 0
9	R/W	0	MLS MSB / LSB First Select 0: MSB First 1: LSB First
8	R/W	0	SEXT Sign Extend (only for 16 bits slot) 0: Zeros or audio gain padding at LSB position 1: Sign extension at MSB position When writing the bit is 0, the unused bits are audio gain for 13-bit linear sample and zeros padding for 8-bit companding sample. When writing the bit is 1, the unused bits are both sign extension.
7:6	R/W	0	SI Slot Index 00: the 1st slot 01: the 2nd slot

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			10: the 3rd slot 11: the 4th slot
5	R/W	1	SW Slot Width 0: 8 clocks width 1: 16 clocks width Notes: For A-law or u-law PCM sample, if this bit is set to 1, eight zero bits are following with PCM sample.
4	R/W	0	SSYNC Short Sync Select 0: Long Frame Sync 1: Short Frame Sync It should be set '1' for 8 clocks width slot.
3:2	R/W	0	RX_PDM PCM Data Mode 00: 16-bits Linear PCM 01: 8-bits Linear PCM 10: 8-bits u-law 11: 8-bits A-law
1:0	R/W	0	TX_PDM PCM Data Mode 00: 16-bits Linear PCM 01: 8-bits Linear PCM 10: 8-bits u-law 11: 8-bits A-law

7.8.7.4. Digital Audio TX FIFO Register

Offset: 0x0C			Register Name: DA_TXFIFO_REG
Bit	R/W	Default/Hex	Description
31:0	W	0	TX_DATA TX Sample Transmitting left, right channel sample data should be written this register one by one. The left channel sample data is first and then the right channel sample.

7.8.7.5. Digital Audio RX FIFO Register

Offset: 0x10			Register Name: DA_RXFIFO_REG
Bit	R/W	Default/Hex	Description
31:0	R	0	RX_DATA RX Sample Host can get one sample by reading this register. The left channel sample data is first and then the right channel sample.

7.8.7.6. Digital Audio FIFO Control Register

Offset: 0x14	Register Name: DA_FCTL_REG

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

Bit	R/W	Default/Hex	Description
31	R/W	0	FIFOSRC TX FIFO source select 0: APB bus 1: Analog Audio CODEC
30:26	/	/	/
25	R/W	0	FTX Write ‘1’ to flush TX FIFO, self clear to ‘0’.
24	R/W	0	FRX Write ‘1’ to flush RX FIFO, self clear to ‘0’.
23:19	/	/	/
18:12	R/W	0x40	TXTL TX FIFO Empty Trigger Level Interrupt and DMA request trigger level for TXFIFO normal condition Trigger Level = TXTL
11:10	/	/	/
9:4	R/W	0xF	RXTL RX FIFO Trigger Level Interrupt and DMA request trigger level for RXFIFO normal condition Trigger Level = RXTL + 1
3	/	/	/
2	R/W	0	TXIM TX FIFO Input Mode (Mode 0, 1) 0: Valid data at the MSB of TXFIFO register 1: Valid data at the LSB of TXFIFO register Example for 20-bits transmitted audio sample: Mode 0: FIFO_I[23:0] = {4’h0, TXFIFO[31:12]} Mode 1: FIFO_I[23:0] = {4’h0, TXFIFO[19:0]}
1:0	R/W	0	RXOM RX FIFO Output Mode (Mode 0, 1, 2, 3) 00: Expanding ‘0’ at LSB of DA_RXFIFO register. 01: Expanding received sample sign bit at MSB of DA_RXFIFO register. 10: Truncating received samples at high half-word of DA_RXFIFO register and low half-word of DA_RXFIFO register is filled by ‘0’. 11: Truncating received samples at low half-word of DA_RXFIFO register and high half-word of DA_RXFIFO register is expanded by its sign bit. Example for 20-bits received audio sample: Mode 0: RXFIFO[31:0] = {FIFO_O[19:0], 12’h0} Mode 1: RXFIFO[31:0] = {12{FIFO_O[19]}, FIFO_O[19:0]} Mode 2: RXFIFO[31:0] = {FIFO_O[19:4], 16’h0} Mode 3: RXFIFO[31:0] = {16{FIFO_O[19], FIFO_O[19:4]}

7.8.7.7. Digital Audio FIFO Status Register

Offset: 0x18			Register Name: DA_FSTA_REG
Bit	R/W	Default/Hex	Description

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

31:29	/	/	/
28	R	1	TXE TX FIFO Empty 0: No room for new sample in TX FIFO 1: More than one room for new sample in TX FIFO (>= 1 word)
27:24	/	/	/
23:16	R	0x80	TXE_CNT TX FIFO Empty Space Word Counter
15:9	/	/	/
8	R	0	RXA RX FIFO Available 0: No available data in RX FIFO 1: More than one sample in RX FIFO (>= 1 word)
7	/	/	/
6:0	R	0	RXA_CNT RX FIFO Available Sample Word Counter

7.8.7.8. Digital Audio DMA & Interrupt Control Register

Offset: 0x1C			Register Name: DA_INT_REG
Bit	R/W	Default/Hex	Description
31:8	/	/	/
7	R/W	0	TX_DRQ TX FIFO Empty DRQ Enable 0: Disable 1: Enable
6	R/W	0	TXUI_EN TX FIFO Under run Interrupt Enable 0: Disable 1: Enable
5	R/W	0	TXOI_EN TX FIFO Overrun Interrupt Enable 0: Disable 1: Enable When set to ‘1’, an interrupt happens when writing new audio data if TX FIFO is full.
4	R/W	0	TXEI_EN TX FIFO Empty Interrupt Enable 0: Disable 1: Enable
3	R/W	0	RX_DRQ RX FIFO Data Available DRQ Enable 0: Disable 1: Enable When set to ‘1’, RXFIFO DMA Request line is asserted if Data is available in RX FIFO.

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

2	R/W	0	RXUI_EN RX FIFO Under run Interrupt Enable 0: Disable 1: Enable
1	R/W	0	RXOI_EN RX FIFO Overrun Interrupt Enable 0: Disable 1: Enable
0	R/W	0	RXAI_EN RX FIFO Data Available Interrupt Enable 0: Disable 1: Enable

7.8.7.9. Digital Audio Interrupt Status Register

Offset: 0x20			Register Name: DA_ISTA_REG
Bit	R/W	Default/Hex	Description
31:7	/	/	/
6	R/W	0	TXU_INT TX FIFO Under run Pending Interrupt 0: No Pending Interrupt 1: FIFO Under run Pending Interrupt
5	R/W	0	TXO_INT TX FIFO Overrun Pending Interrupt 0: No Pending Interrupt 1: FIFO Overrun Pending Interrupt Write '1' to clear this interrupt
4	R/W	1	TXE_INT TX FIFO Empty Pending Interrupt 0: No Pending IRQ 1: FIFO Empty Pending Interrupt Write '1' to clear this interrupt or automatic clear if interrupt condition fails.
3:2	/	/	/
2	R/W	0	RXU_INT RX FIFO Under run Pending Interrupt 0: No Pending Interrupt 1:FIFO Under run Pending Interrupt Write 1 to clear this interrupt
1	R/W	0	RXO_INT RX FIFO Overrun Pending Interrupt 0: No Pending IRQ 1: FIFO Overrun Pending IRQ Write '1' to clear this interrupt
0	R/W	0	RXA_INT RX FIFO Data Available Pending Interrupt 0: No Pending IRQ

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			1: Data Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails.

7.8.7.10. Digital Audio Clock Divide Register

Offset: 0x24			Register Name: DA_CLKD_REG
Bit	R/W	Default/Hex	Description
31:8	/	/	/
7	R/W	0	MCLKO_EN 0: Disable MCLK Output 1: Enable MCLK Output Notes: Whether in Slave or Master mode, when this bit is set to 1, MCLK should be output.
6:4	R/W	0	BCLKDIV BCLK Divide Ratio from MCLK 000: Divide by 2 (BCLK = MCLK/2) 001: Divide by 4 010: Divide by 6 011: Divide by 8 100: Divide by 12 101: Divide by 16 110: Divide by 32 111: Divide by 64
3:0	R/W	0	MCLKDIV MCLK Divide Ratio from Audio PLL Output 0000: Divide by 1 0001: Divide by 2 0010: Divide by 4 0011: Divide by 6 0100: Divide by 8 0101: Divide by 12 0110: Divide by 16 0111: Divide by 24 1000: Divide by 32 1001: Divide by 48 1010: Divide by 64 Others : Reserved

7.8.7.11. Digital Audio TX Counter Register

Offset: 0x28			Register Name: DA_TXCNT
Bit	R/W	Default/Hex	Description
31:0	R/W	0	TX_CNT TX Sample Counter The audio sample number of sending into TXFIFO. When one sample is put into TXFIFO by DMA or by host IO, the TX sample counter register increases by one. The TX sample counter register can be set to any initial valve at any

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			time. After been updated by the initial value, the counter register should count on base of this initial value.

7.8.7.12. Digital Audio RX Counter Register

Offset: 0x2C			Register Name: DA_RXCNT_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0	RX_CNT RX Sample Counter The audio sample number of writing into RXFIFO. When one sample is written by Digital Audio Engine, the RX sample counter register increases by one. The RX sample counter register can be set to any initial valve at any time. After been updated by the initial value, the counter register should count on base of this initial value.

7.8.7.13. Digital Audio TX Channel Select Register

Offset: 0x30			Register Name: DA_TXCHSEL_REG
Bit	R/W	Default/Hex	Description
31:3	/	/	/
2:0	R/W	1	TX_CHSEL TX Channel Select 0: 1-ch 1: 2-ch 2: 3-ch 3: 4-ch

7.8.7.14. Digital Audio TX Channel Mapping Register

Offset: 0x34			Register Name: DA_TXCHMAP_REG
Bit	R/W	Default/Hex	Description
31:15	/	/	/
14:12	R/W	3	TX_CH3_MAP TX Channel3 Mapping 000: 1st sample 001: 2nd sample 010: 3rd sample 011: 4th sample 100: 5th sample 101: 6th sample 110: 7th sample 111: 8th sample
11	/	/	/
10:8	R/W	2	TX_CH2_MAP TX Channel2 Mapping 000: 1st sample 001: 2nd sample 010: 3rd sample

Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			011: 4th sample 100: 5th sample 101: 6th sample 110: 7th sample 111: 8th sample
7	/	/	/
6:4	R/W	1	TX_CH1_MAP TX Channel1 Mapping 000: 1st sample 001: 2nd sample 010: 3rd sample 011: 4th sample 100: 5th sample 101: 6th sample 110: 7th sample 111: 8th sample
3	/	/	/
2:0	R/W	0	TX_CH0_MAP TX Channel0 Mapping 000: 1st sample 001: 2nd sample 010: 3rd sample 011: 4th sample 100: 5th sample 101: 6th sample 110: 7th sample 111: 8th sample

7.8.7.15. Digital Audio RX Channel Select Register

Offset: 0x38			Register Name: DA_RXCHSEL_REG
Bit	R/W	Default/Hex	Description
31:3	/	/	/
2:0	R/W	1	RX_CHSEL RX Channel Select 0: 1-ch 1: 2-ch 2: 3-ch 3: 4-ch Others: Reserved

7.8.7.16. Digital Audio RX Channel Mapping Register

Offset: 0x3C			Register Name: DA_RXCHMAP_REG
Bit	R/W	Default/Hex	Description
31:15	/	/	/
14:12	R/W	3	RX_CH3_MAP

Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			RX Channel3 Mapping 000: 1st sample 001: 2nd sample 010: 3rd sample 011: 4th sample Others: Reserved
11	/	/	/
10:8	R/W	2	RX_CH2_MAP RX Channel2 Mapping 000: 1st sample 001: 2nd sample 010: 3rd sample 011: 4th sample Others: Reserved
7	/	/	/
6:4	R/W	1	RX_CH1_MAP RX Channel1 Mapping 000: 1st sample 001: 2nd sample 010: 3rd sample 011: 4th sample Others: Reserved
3	/	/	/
2:0	R/W	0	RX_CH0_MAP RX Channel0 Mapping 000: 1st sample 001: 2nd sample 010: 3rd sample 011: 4th sample Others: Reserved

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

7.9. OWA Interface

7.9.1. Overview

The OWA interface is one wire audio interface.

7.9.2. Feature

The OWA includes the following features:

- IEC-60958 transmitter functionality
- Support S/PDIF Interface
- Support channel status insertion for the transmitter
- Hardware Parity generation on the transmitter
- One 32×24bits FIFO (TX) for audio data transfer
- Programmable FIFO thresholds
- Interrupt and DMA support

7.9.3. Signal Description

7.9.3.1. OWA Interface Pin List

Signal Name	Direction(M)	Description	Pin
OWA_DOUT	O	OWA output	PE6/PD17

7.9.3.2. OWA Interface Clock Requirement

Clock Name	Description	Requirement
apb_clk	APB bus clock	>13 MHz
s_clk	OWA serial access clock	4x24.576 MHz or 4x22.5792 MHz from CCU

7.9.4. Functionalities Description

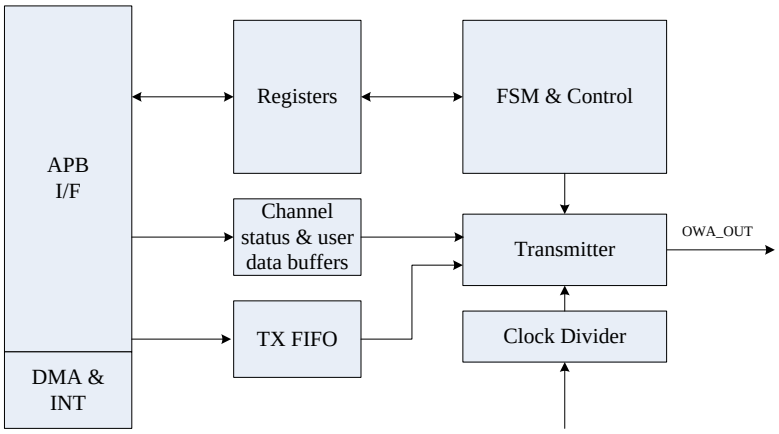
7.9.4.1. Typical Applications

The OWA provides a serial bus interface for audio data between system. This interface is widely used for consumer audio connect.

7.9.4.2. Functional Block Diagram

The OWA interface block diagram is shown below:

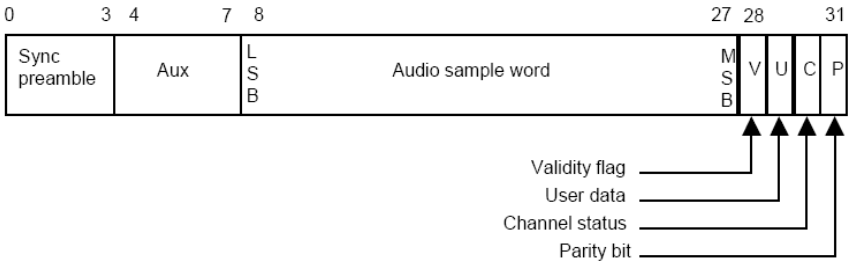
 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.



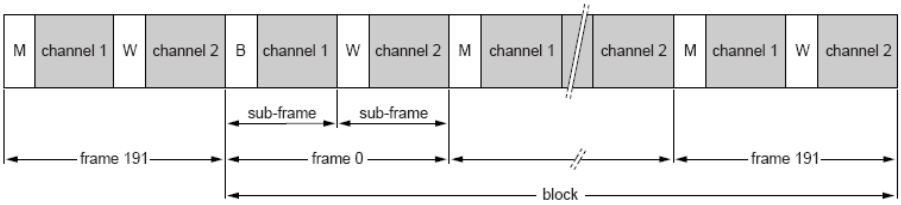
OWA Interface Block Diagram

7.9.4.3. Operation Principle

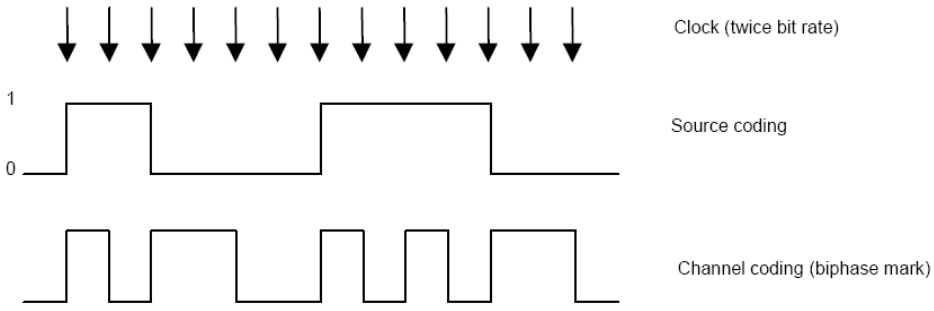
OWA Frame format:



Sub-frame format



Frame/block format



Biphase-Mark Encoding

7.9.5. Operation Modes

The software operation of the OWA is divided into five steps: system setup, OWA initialization, the channel setup, DMA setup and Enable/Disable module. These five steps are described in detail in the following sections.

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

7.9.5.1. System setup and OWA initialization

The first step In the OWA initialization is properly programming the GPIO. Since the OWA port is a multiplex pin. You can find the function in the pin multiplex specification. The clock source for the OWA should be followed. At first you must reset the audio PLL through the PLL_ENABLE bit of PLL_AUDIO_CTRL_REG in the CCU. The second step, you must setup the frequency of the audio pll in the PLL_AUDIO_CTRL_REG. After that, you must open the OWA gating through the OWA_CLK_REG when you checkout that the LOCK bit of PLL_AUDIO_CTRL_REG becomes to 1. At last, you must reset APB0_RST_REG of the OWA and open the OWA bus gating in the APB0_GATING_REG.

After the system setup, the register of OWA can be setup. At first, you should reset the OWA by writing 1 to OWA_CTL[0] and clear the TX FIFO by writing 1 to register OWA_FCTL[17]. After that you should enable the globe enable bit by writing 1 to OWA_CTL[1] and clear the interrupt and TX counter through the OWA_ISTA and SP_TXCNT.

7.9.5.2. The channel setup and DMA setup

The OWA support three methods to transfer the data. The most common way is DMA, the set of DMA can be found in the DMA spec. In this module, you just to enable the DRQ.

7.9.5.3. Enable and disable the OWA

To enable the function, you can enable TX by writing the OWA_TX_CFIG[31]. After that, you must enable OWA by writing the Globe Enable bit to 1 in the OWA_CTL. Write the Globe Enable to 0 to disable process.

7.9.6. OWA Interface Register List

Module Name	Base Address
OWA	0x01C21400

Register Name	Offset	Description
OWA_GEN_CTRL_REG	0x00	OWA General Control Register
OWA_TX_CFG_REG	0x04	OWA TX Configuration Register
OWA_TX_FIFO_REG	0x0C	OWA TX FIFO Register
OWA_FCTL_REG	0x14	OWA FIFO Control Register
OWA_FSTA_REG	0x18	OWA FIFO Status Register
OWA_INT_REG	0x1C	OWA Interrupt Control Register
OWA_ISTA_REG	0x0C	OWA Interrupt Status Register
OWA_TX_CNT_REG	0x24	OWA TX Counter Register
OWA_TX_CHSTA_REG0	0x2C	OWA TX Channel Status Register 0
OWA_TX_CHSTA_REG1	0x30	OWA TX Channel Status Register 1

7.9.7. OWA Register Description

7.9.7.1. OWA General Control Register

Offset: 0x00			Register Name: OWA_CTRL_REG
Bit	R/W	Default/Hex	Description
31:10	/	/	/

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

9:4	R/W	0x08	MCLK_DIV_RATIO Mclk divide Ratio Note: only support 2n divide ratio(n=1~31)
3	/	/	/
2	R/W	0	MCLK_OUT_EN Mclk Output Enable 0: Disable 1: Enable
1	R/W	0	GEN Globe Enable A disable on this bit overrides any other block or channel enables. 0: Disable 1: Enable
0	R/W	0	RST Reset 0: Normal 1: Reset *Self clear to 0*

7.9.7.2. OWA TX Configure Register

Offset: 0x04			Register Name: OWA_TX_CFG_REG
Bit	R/W	Default/Hex	Description
31	R/W	0	TX_SINGLE_MODE Tx single channel mode 0: Disable 1: Eanble
30:18	/	/	/
17	R/W	0	ASS Audio sample select with TX FIFO under run when 0: sending 0 1: sending the last audio *Note: This bit is only valid in PCM mode*
16	R/W	0	TX_AUDIO TX data type 0: Linear PCM (Valid bit of both sub-frame set to 0) 1: Non-audio(Valid bit of both sub-frame set to 1)
15:9	/	/	/
8:4	R/W	0xF	TX_RATIO TX clock divide Ratio *Note: clock divide ratio = TX TATIO +1*
3:2	R/W	0	TX_SF TX Sample format: 00: 16bit 01: 20bit

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			10: 24bit 11: Reserved
1	R/W	0	TX_CHM CHSTMODE 0: Channel status A&B set to 0 1: Channel status A&B generated form TX_CHSTA
0	R/W	0	TXEN 0: disabled 1: enabled

7.9.7.3. OWA TX FIFO Register

Offset: 0x0C			Register Name: OWA_TXFIFO_REG
Bit	R/W	Default/Hex	Description
31:0	W	0	TX_DATA Transmitting A, B channel data should be written this register one by one. The A channel data is first and then the B channel data.

7.9.7.4. OWA FIFO Control Register

Offset: 0x14			Register Name: OWA_FCTL_REG
Bit	R/W	Default/Hex	Description
31	R/W	0	FIFOSRC TX FIFO source select 0 : APB bus 1: Analog Audio CODEC
30:18	/	/	/
17	R/W	0	FTX Write “1” to flush TX FIFO, self clear to “0”
16:13	/	/	/
12:8	R/W	0x10	TXTL TX FIFO empty Trigger Level Interrupt and DMA request trigger level for TX FIFO normal condition Trigger Level = TXTL
7:3	R/W	0x0F	Reserved
2	R/W	0	TXIM TX FIFO Input Mode(Mode0, 1) 0: Valid data at the MSB of OWA_TXFIFO register 1: Valid data at the LSB of OWA_TXFIFO register Example for 20-bits transmitted audio sample: Mode 0: FIFO_I[23:0] = {TXFIFO[31:12], 4’h0} Mode 1: FIFO_I[23:0] = {TXFIFO[19:0], 4’h0}
1:0	R/W	0	Reserved

7.9.7.5. OWA FIFO Status Register

Offset: 0x18			Register Name: OWA_FSTA_REG
Bit	R/W	Default/Hex	Description

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

31:15	/	/	/
14	R	1	TXE TX FIFO Empty (indicate FIFO is not full) 0: No room for new sample in TX FIFO 1: More than one room for new sample in TX FIFO (>=1 word)
13:8	R	0x20	TXE_CNT TX FIFO Empty Space Word counter
7:0	/	/	/

7.9.7.6. OWA Interrupt Control Register

Offset: 0x1C			Register Name: OWA_INT_REG
Bit	R/W	Default/Hex	Description
31:8	/	/	/
7	R/W	0	TX_DRQ TX FIFO Empty DRQ Enable 0: Disable 1: Enable
6	R/W	0	TXUI_EN TX FIFO Under run Interrupt Enable 0: Disable 1: Enable
5	R/W	0	TXOI_EN TX FIFO Overrun Interrupt Enable 0: Disable 1: Enable
4	R/W	0	TXEI_EN TX FIFO Empty Interrupt Enable 0: Disable 1: Enable
3:0	/	/	/

7.9.7.7. OWA Interrupt Status Register

Offset: 0x20			Register Name: OWA_ISTA_REG
Bit	R/W	Default/Hex	Description
31:7	/	/	/
6	R/W	0	TXU_INT TX FIFO Under run Pending Interrupt 0: No pending IRQ 1: FIFO Under run Pending Interrupt *Write "1" to clear this interrupt*
5	R/W	0	TXO_INT TX FIFO Overrun Pending Interrupt 0: No Pending IRQ 1: FIFO Overrun Pending Interrupt *Write "1" to clear this interrupt*

Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

4	R/W	1	TXE_INT TX FIFO Empty Pending Interrupt 0: No Pending IRQ 1: FIFO Empty Pending Interrupt *Write "1" to clear this interrupt or automatically clear if interrupt condition fails.*
3:0	/	/	/

7.9.7.8. OWA TX Counter Register

Offset: 0x24			Register Name: OWA_TX_CNT_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0	TX_CNT TX Sample counter The audio sample number of writing into TX FIFO. When one sample is written by DMA or by host IO, the TX sample counter register increases by one. The TX Counter register can be set to any initial value at any time. After been updated by the initial value, the counter register should count on base of this value.

7.9.7.9. OWA TX Channel Status Register 0

Offset: 0x2C			Register Name: OWA_TX_CHSTA_REG0
Bit	R/W	Default/Hex	Description
31: 30	/	/	/
29:28	R/W		CA Clock Accuracy 00: Level 2 01: Level 1 10: Level 3 11: not matched
27:24	R/W		FREQ Sampling frequency 0000: 44.1kHz 1000: Reserved 0001: not indicated 1001: 768kHz 0010: 48kHz 1010: 96kHz 0011: 32kHz 1011: Reserved 0100: 22.05kHz 1100:176.4kHz 0101: Reserved 1101: Reserved 0110: 24kHz 1110: 192kHz 0111: Reserved 1111: Reserved
23:20	R/W	0	CN Channel Number
19:16	R/W	0	SN Source Number
15:8	R/W	0	CC Category code

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			Indicates the kind of equipment that generates the digital audio interface signal.
7:6	R/W	0	MODE Mode 00: Default Mode 01~11: Reserved
5:3	R/W	0	EMP Emphasis Additional format information For bit 1 = “0”, Linear PCM audio mode: 000: 2 audio channels without pre-emphasis 001: 2 audio channels with 50 μs / 15 μs pre-emphasis 010: Reserved (for 2 audio channels with pre-emphasis) 011: Reserved (for 2 audio channels with pre-emphasis) 100~111: Reserved For bit 1 = “1”, other than Linear PCM applications: 000: Default state 001~111: Reserved
2	R/W	0	CP Copyright 0: copyright is asserted 1: no copyright is asserted
1	R/W	0	TYPE Audio Data Type 0: Linear PCM Samples 1: For none-linear PCM audio such as AC3, DTS, MPEG audio
0	R/W	0	PRO Application type 0: Consumer Application 1: Professional Application Note: This bit must be fixed to “0”

7.9.7.10. OWA TX Channel Status Register 1

Offset: 0x30			Register Name: OWA_TX_CHSTA_REG1
Bit	R/W	Default/Hex	Description
31:10	/	/	/
9:8	R/W	0	CGMS_A 00: Copying is permitted without restriction 01: One generation of copies may be made 10: Condition not be used 11: No copying is permitted
7:4	R/W	0	ORIG_FREQ Original sampling frequency 0000: not indicated 0001: 192kHz

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.

			0010: 12kHz 0011: 176.4kHz 0100: Reserved 0101: 96kHz 0110: 8kHz 0111: 88.2kHz 1000: 16kHz 1001: 24kHz 1010: 11.025kHz 1011: 22.05kHz 1100: 32kHz 1101: 48kHz 1110: Reserved 1111: 44.1kHz
3:1	R/W	0	WL Sample word length For bit 0 = “0”: 000: not indicated 001: 16 bits 010: 18 bits 100: 19 bits 101: 20 bits 110: 17 bits 111: Reserved For bit 0 = “1”: 000: not indicated 001: 20 bits 010: 22 bits 100: 23 bits 101: 24 bits 110: 21 bits 111: Reserved
0	R/W	0	MWL Max Word length 0: Maximum audio sample word length is 20 bits 1: Maximum audio sample word length is 24 bits

 Copyright©2019 Allwinner Technology Co.,Ltd. All Rights Reserved.