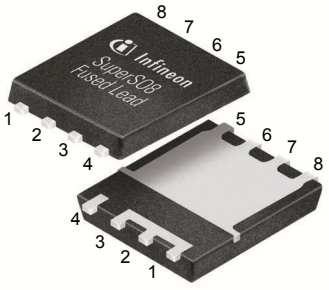
# MOSFET

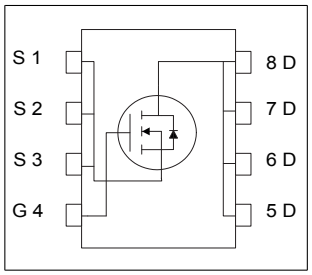
## OptiMOS™ Power-Transistor, 60 V

TDSON-8 FL (enlarged source interconnection)




### Features

- Optimized for synchronous rectification
- 175 °C rated
- 100% avalanche tested
- Superior thermal resistance
- N-channel
- Qualified according to JEDEC[1] for target applications
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21
- Higher solder joint reliability due to enlarged source interconnection




### Table 1 Key Performance Parameters

| Parameter | Value | Unit |
|---|---|---|
| $V_{DS}$ | 60 | V |
| $R_{DS(on),max}$ | 1.95 | mΩ |
| $I_D$ | 100 | A |
| $Q_{OSS}$ | 63 | nC |
| $Q_G$(0V..10V) | 58 | nC |

| Type / Ordering Code | Package | Marking | Related Links |
|---|---|---|---|
| BSC019N06NS | TDSON-8 FL | 019N06NS | - |

[1] J-STD20 and JESD22

## Table of Contents

# 1 Maximum ratings

at $T_A$=25 °C, unless otherwise specified

## Table 2 Maximum ratings

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Continuous drain current | $I_D$ | -<br>-<br>- | -<br>-<br>- | 100<br>100<br>28 | A | $V_{GS}$=10 V, $T_A$=25 °C<br>$V_{GS}$=10 V, $T_A$=100 °C<br>$V_{GS}$=10 V, $T_A$=25 °C, $R_{thJA}$=50 K/W[1)] |
| Pulsed drain current[2)] | $I_{D,pulse}$ | - | - | 400 | A | $T_A$=25 °C |
| Avalanche energy, single pulse[3)] | $E_{AS}$ | - | - | 220 | mJ | $I_D$=50 A, $R_{GS}$=25 Ω |
| Gate source voltage | $V_{GS}$ | -20 | - | 20 | V | - |
| Power dissipation | $P_{tot}$ | -<br>- | -<br>- | 136<br>3.0 | W | $T_A$=25 °C<br>$T_A$=25 °C, $R_{thJA}$=50 K/W |
| Operating and storage temperature | $T_j$, $T_{stg}$ | -55 | - | 175 | °C | - |

# 2 Thermal characteristics

## Table 3 Thermal characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Thermal resistance, junction - case, bottom | $R_{thJC}$ | - | 0.7 | 1.1 | K/W | - |
| Thermal resistance, junction - case, top | $R_{thJC}$ | - | - | 20 | K/W | - |
| Device on PCB, 6 cm$^2$ cooling area[1)] | $R_{thJA}$ | - | - | 50 | K/W | - |

[1)] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm$^2$ (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.
[2)] See Diagram 3 for more detailed information
[3)] See Diagram 13 for more detailed information

# 3 Electrical characteristics

## Table 4 Static characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | 60 | - | - | V | $V_{GS}$=0 V, $I_D$=1 mA |
| Gate threshold voltage | $V_{GS(th)}$ | 2.1 | 2.8 | 3.3 | V | $V_{DS}$=$V_{GS}$, $I_D$=74 µA |
| Zero gate voltage drain current | $I_{DSS}$ | -<br>- | 0.5<br>10 | 1<br>100 | µA | $V_{DS}$=60 V, $V_{GS}$=0 V, $T_j$=25 °C<br>$V_{DS}$=60 V, $V_{GS}$=0 V, $T_j$=125 °C |
| Gate-source leakage current | $I_{GSS}$ | - | 10 | 100 | nA | $V_{GS}$=20 V, $V_{DS}$=0 V |
| Drain-source on-state resistance | $R_{DS(on)}$ | -<br>- | 1.7<br>2.4 | 1.95<br>3.2 | mΩ | $V_{GS}$=10 V, $I_D$=50 A<br>$V_{GS}$=6 V, $I_D$=12.5 A |
| Gate resistance[1)] | $R_G$ | - | 1.7 | 2.6 | Ω | - |
| Transconductance | $g_{fs}$ | 60 | 120 | - | S | \|$V_{DS}$\|>2\|$I_D$\|$R_{DS(on)max}$, $I_D$=50 A |

## Table 5 Dynamic characteristics[1)]

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input capacitance | $C_{iss}$ | - | 4200 | 5250 | pF | $V_{GS}$=0 V, $V_{DS}$=30 V, $f$=1 MHz |
| Output capacitance | $C_{oss}$ | - | 960 | 1200 | pF | $V_{GS}$=0 V, $V_{DS}$=30 V, $f$=1 MHz |
| Reverse transfer capacitance | $C_{rss}$ | - | 41 | 82 | pF | $V_{GS}$=0 V, $V_{DS}$=30 V, $f$=1 MHz |
| Turn-on delay time | $t_{d(on)}$ | - | 12 | - | ns | $V_{DD}$=30 V, $V_{GS}$=10 V, $I_D$=30 A, $R_{G,ext}$=1.6 Ω |
| Rise time | $t_r$ | - | 7 | - | ns | $V_{DD}$=30 V, $V_{GS}$=10 V, $I_D$=30 A, $R_{G,ext}$=1.6 Ω |
| Turn-off delay time | $t_{d(off)}$ | - | 26 | - | ns | $V_{DD}$=30 V, $V_{GS}$=10 V, $I_D$=30 A, $R_{G,ext}$=1.6 Ω |
| Fall time | $t_f$ | - | 8 | - | ns | $V_{DD}$=30 V, $V_{GS}$=10 V, $I_D$=30 A, $R_{G,ext}$=1.6 Ω |

## Table 6 Gate charge characteristics[2)]

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Gate to source charge | $Q_{gs}$ | - | 19 | - | nC | $V_{DD}$=30 V, $I_D$=50 A, $V_{GS}$=0 to 10 V |
| Gate charge at threshold | $Q_{g(th)}$ | - | 12 | - | nC | $V_{DD}$=30 V, $I_D$=50 A, $V_{GS}$=0 to 10 V |
| Gate to drain charge[1)] | $Q_{gd}$ | - | 11 | 16 | nC | $V_{DD}$=30 V, $I_D$=50 A, $V_{GS}$=0 to 10 V |
| Switching charge | $Q_{sw}$ | - | 18 | - | nC | $V_{DD}$=30 V, $I_D$=50 A, $V_{GS}$=0 to 10 V |
| Gate charge total[1)] | $Q_g$ | - | 58 | 77 | nC | $V_{DD}$=30 V, $I_D$=50 A, $V_{GS}$=0 to 10 V |
| Gate plateau voltage | $V_{plateau}$ | - | 4.4 | - | V | $V_{DD}$=30 V, $I_D$=50 A, $V_{GS}$=0 to 10 V |
| Gate charge total, sync. FET | $Q_{g(sync)}$ | - | 51 | - | nC | $V_{DS}$=0.1 V, $V_{GS}$=0 to 10 V |
| Output charge[1)] | $Q_{oss}$ | - | 63 | 79 | nC | $V_{DD}$=30 V, $V_{GS}$=0 V |

[1)] Defined by design. Not subject to production test
[2)] See ″Gate charge waveforms″ for parameter definition

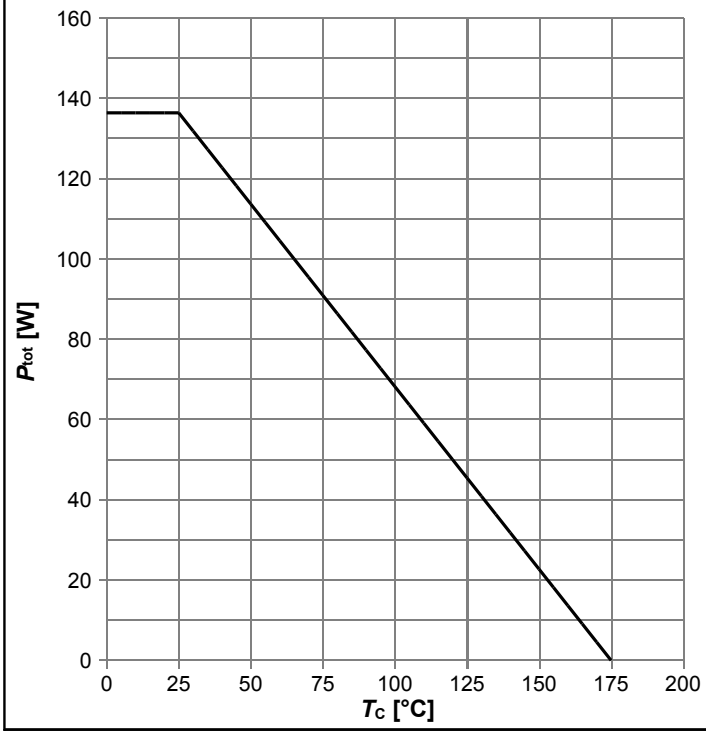
## Table 7 Reverse diode

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Diode continuous forward current | $I_S$ | - | - | 100 | A | $T_C$=25 °C |
| Diode pulse current | $I_{S,pulse}$ | - | - | 400 | A | $T_C$=25 °C |
| Diode forward voltage | $V_{SD}$ | - | 0.9 | 1.2 | V | $V_{GS}$=0 V, $I_F$=50 A, $T_j$=25 °C |
| Reverse recovery time[1)] | $t_{rr}$ | - | 42 | 67 | ns | $V_R$=30 V, $I_F$=50A, d$i_F$/d$t$=100 A/µs |
| Reverse recovery charge | $Q_{rr}$ | - | 43 | - | nC | $V_R$=30 V, $I_F$=50A, d$i_F$/d$t$=100 A/µs |

[1)] Defined by design. Not subject to production test

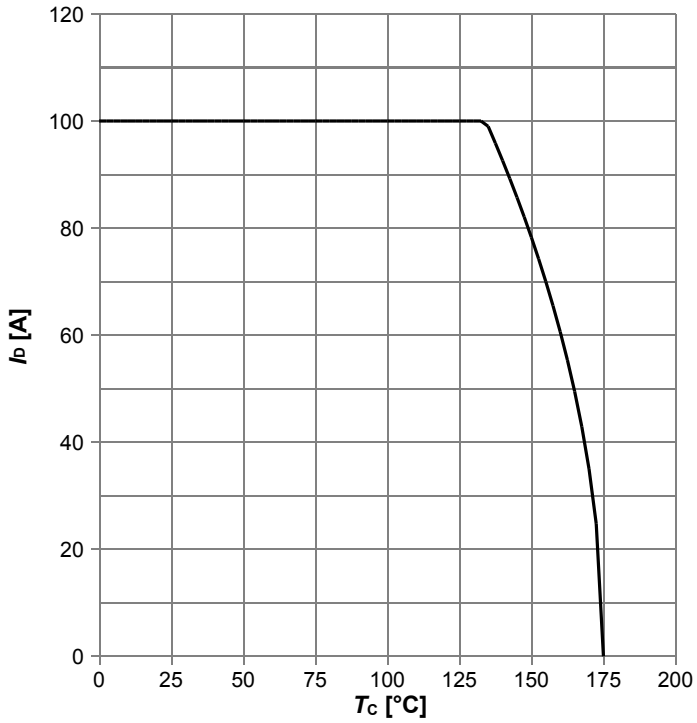
# 4 Electrical characteristics diagrams

**Diagram 1: Power dissipation**



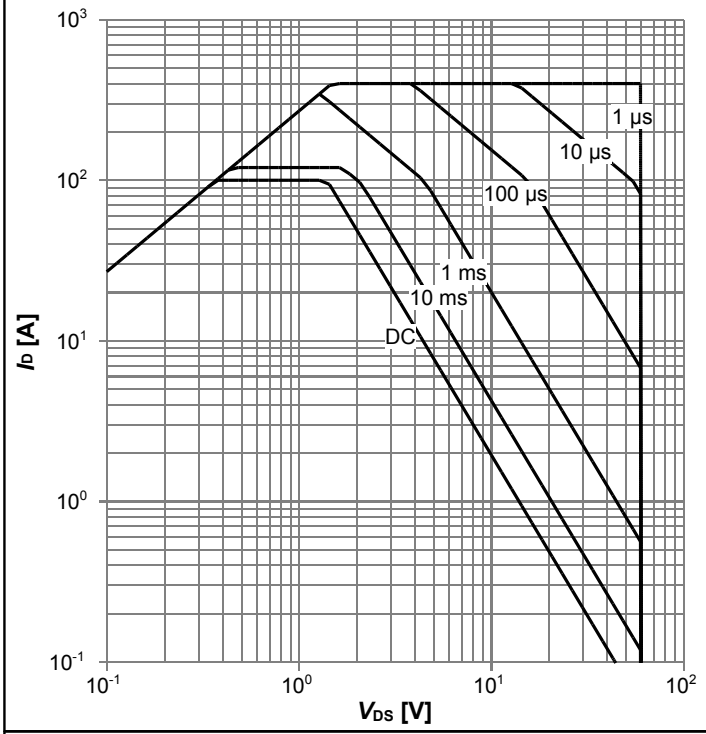

$P_{tot}=f(T_C)$

**Diagram 2: Drain current**



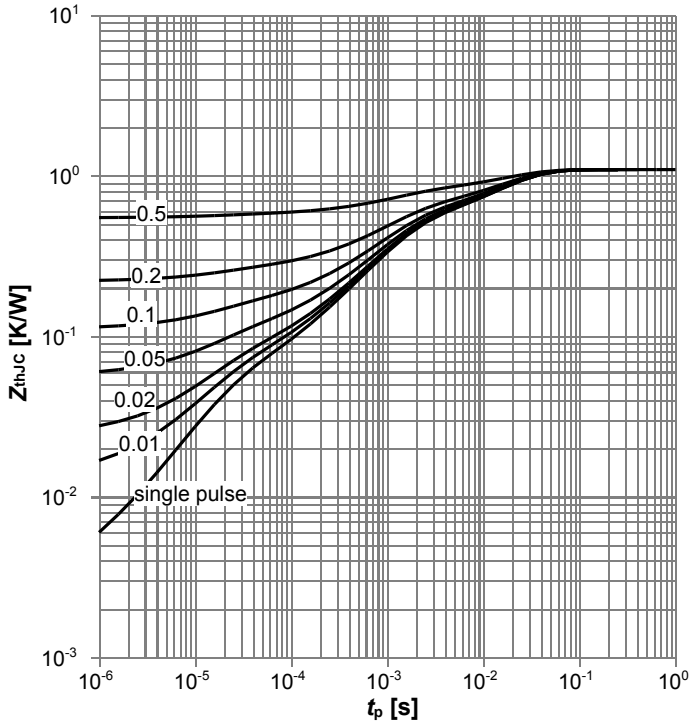

$I_D=f(T_C)$; $V_{GS}\geq 10$ V

**Diagram 3: Safe operating area**



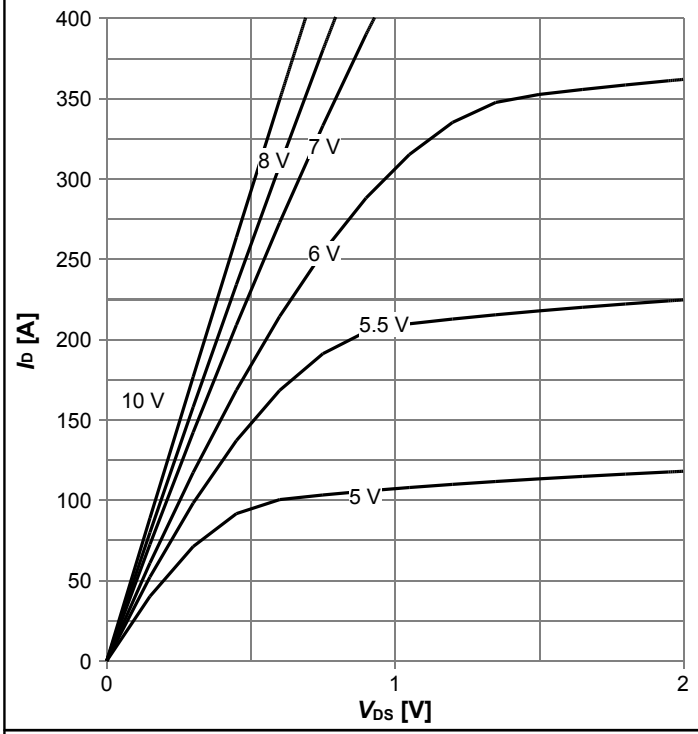

$I_D=f(V_{DS})$; $T_C=25$ °C; D=0; parameter: $t_p$

**Diagram 4: Max. transient thermal impedance**



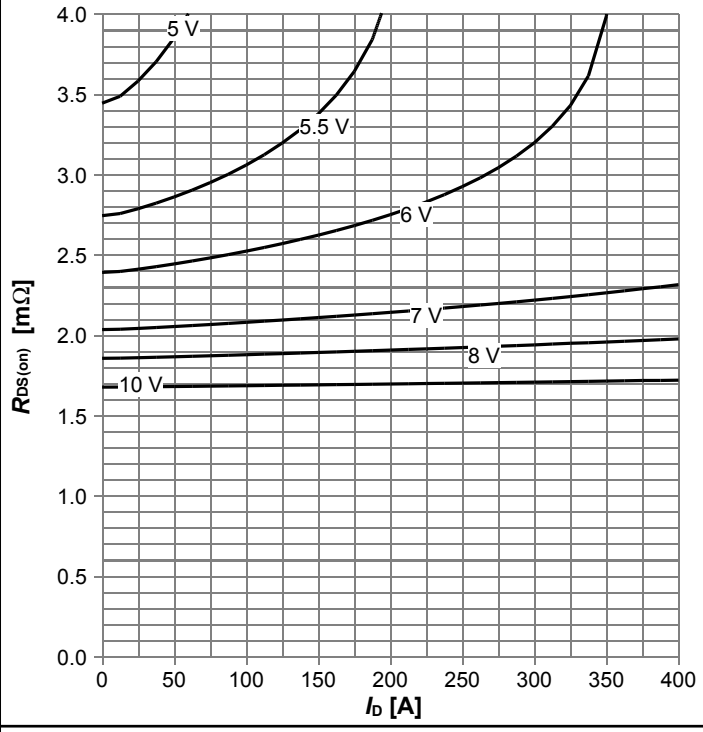

$Z_{thJC}=f(t_p)$; parameter: $D=t_p/T$

**Diagram 5: Typ. output characteristics**



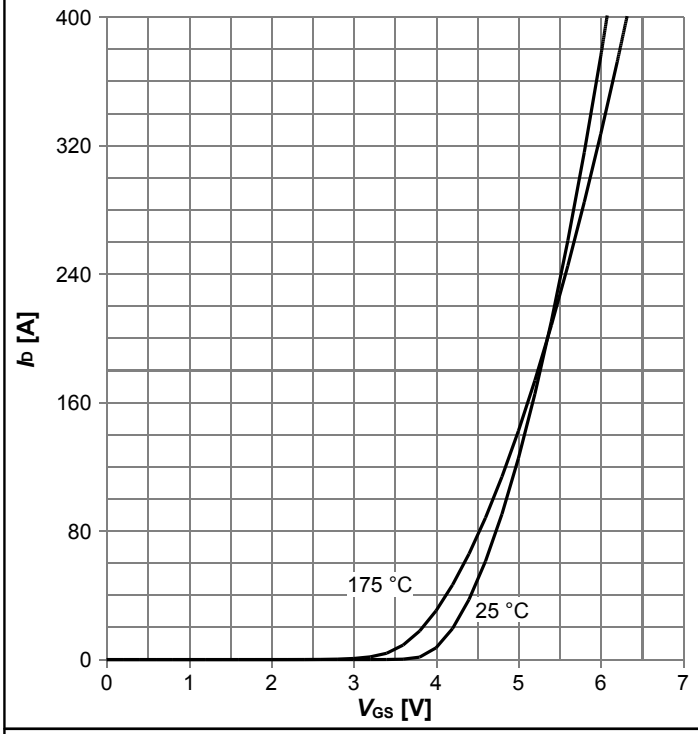

$I_D=f(V_{DS})$; $T_j=25$ °C; parameter: $V_{GS}$

**Diagram 6: Typ. drain-source on resistance**



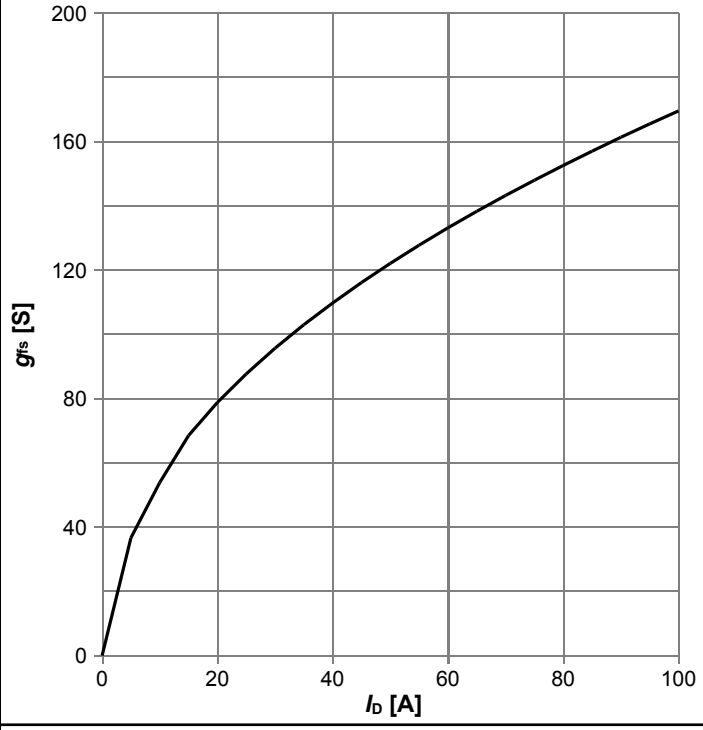

$R_{DS(on)}=f(I_D)$; $T_j=25$ °C; parameter: $V_{GS}$

**Diagram 7: Typ. transfer characteristics**



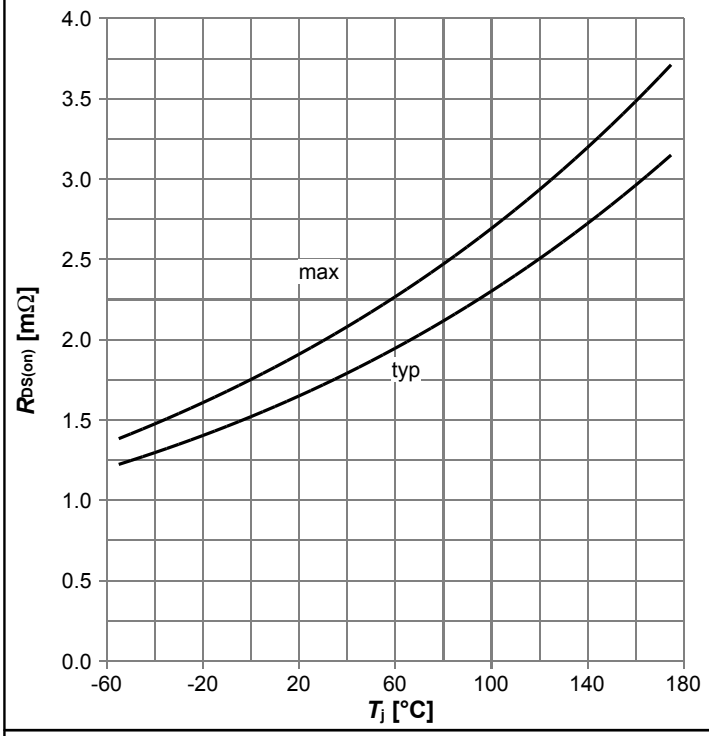

$I_D=f(V_{GS})$; $|V_{DS}|>2|I_D|R_{DS(on)max}$; parameter: $T_j$

**Diagram 8: Typ. forward transconductance**



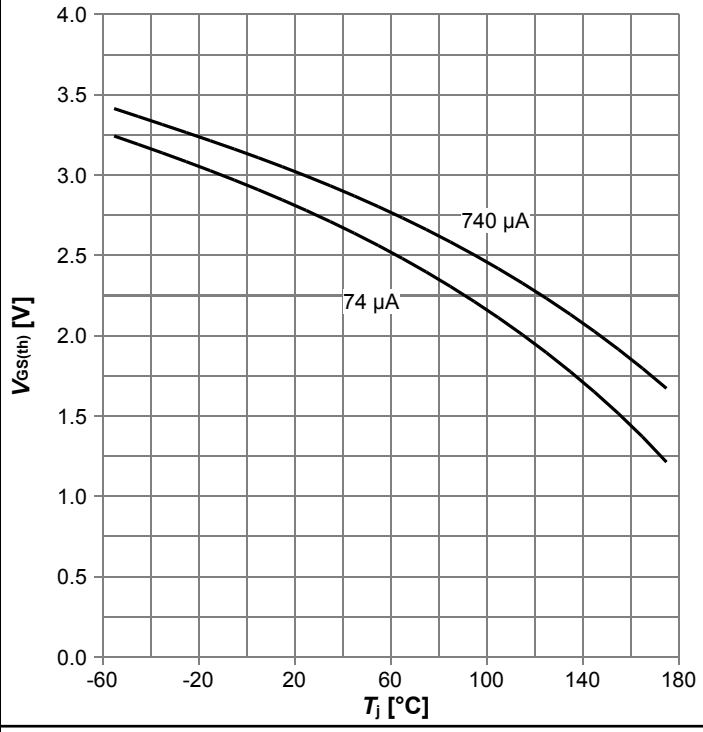

$g_{fs}=f(I_D)$; $T_j=25$ °C

**Diagram 9: Drain-source on-state resistance**



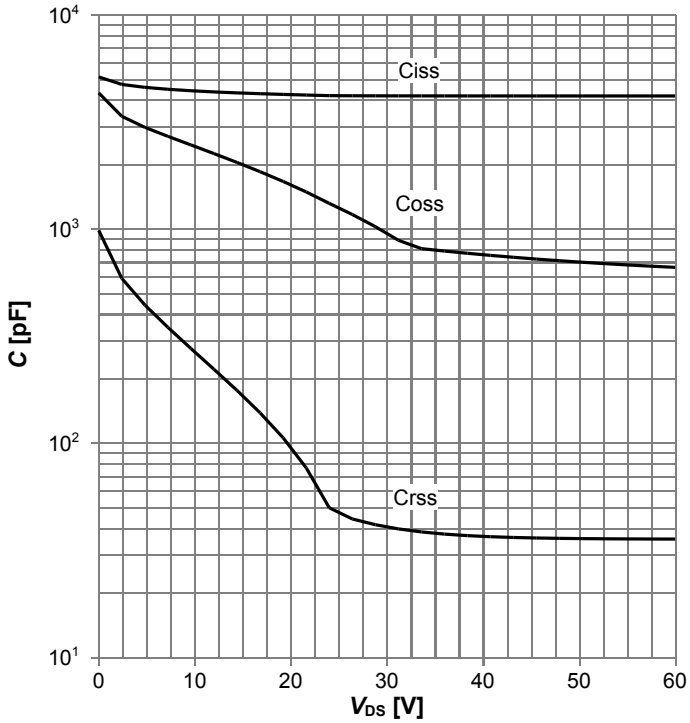

$R_{DS(on)}$=f($T_j$); $I_D$=50 A; $V_{GS}$=10 V

**Diagram 10: Typ. gate threshold voltage**



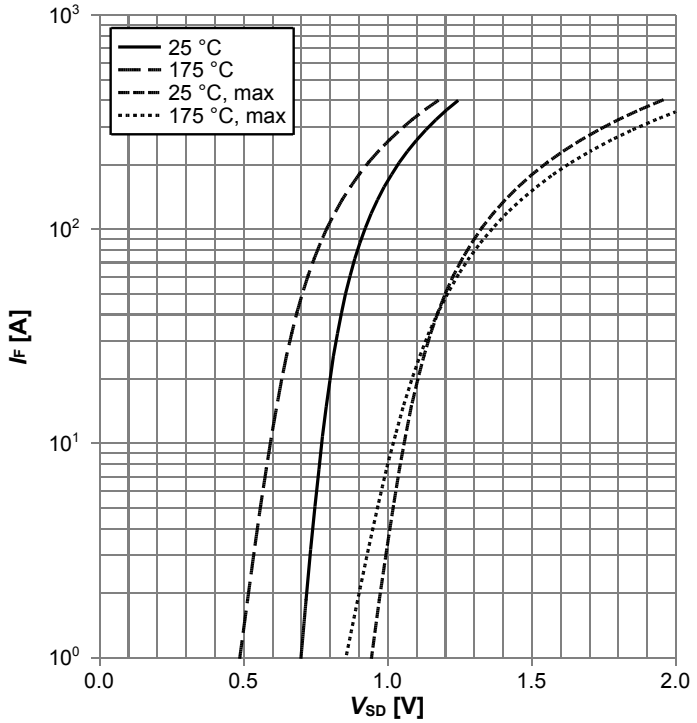

$V_{GS(th)}$=f($T_j$); $V_{GS}$=$V_{DS}$

**Diagram 11: Typ. capacitances**



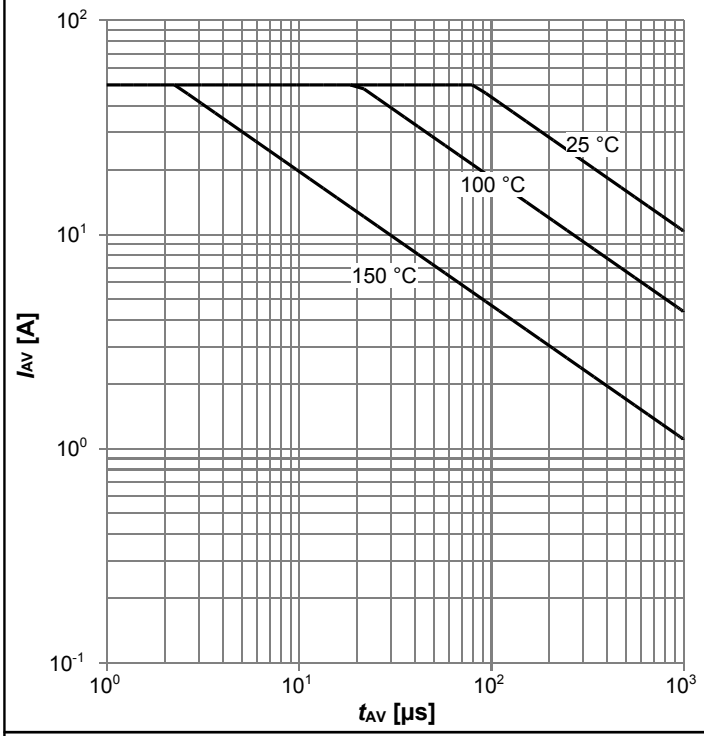

$C$=f($V_{DS}$); $V_{GS}$=0 V; $f$=1 MHz

**Diagram 12: Forward characteristics of reverse diode**



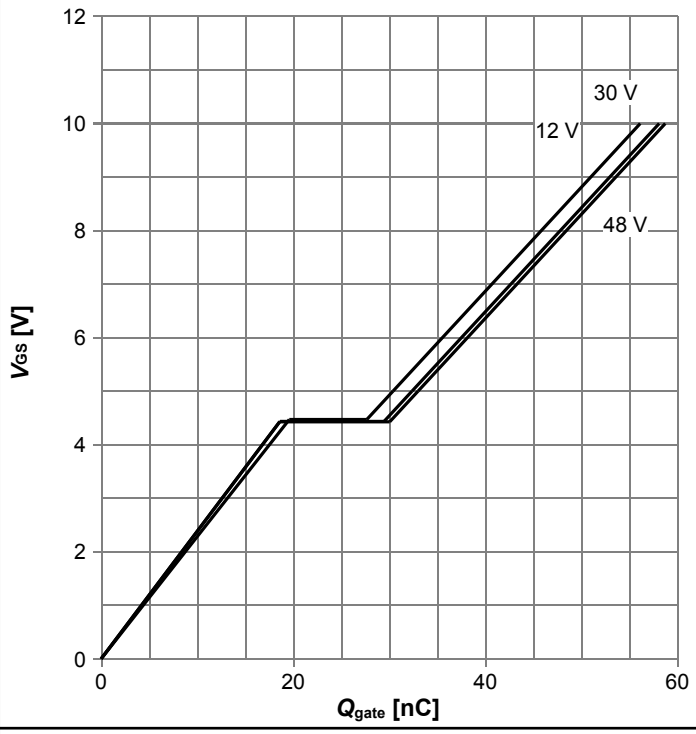

$I_F$=f($V_{SD}$); parameter: $T_j$

**Diagram 13: Avalanche characteristics**



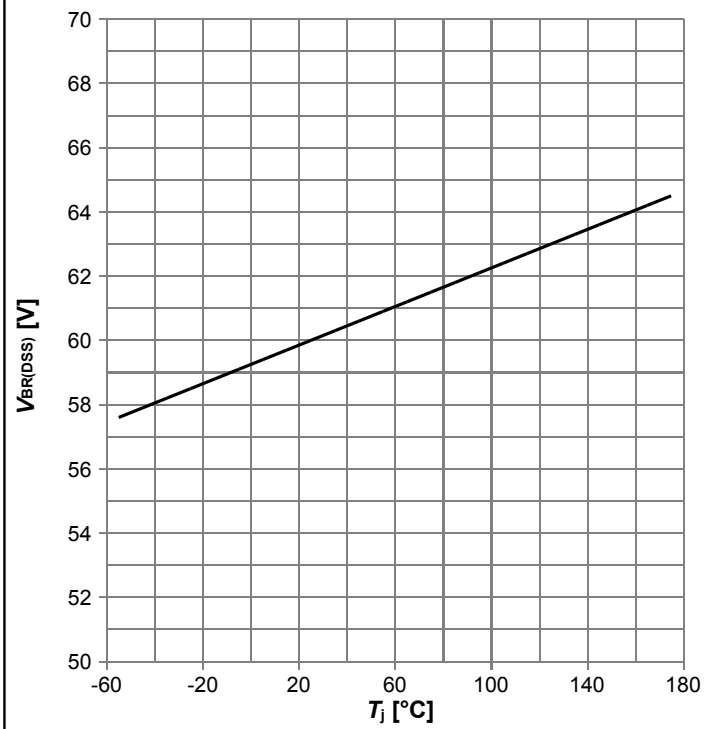

$I_{AS}$=f($t_{AV}$); $R_{GS}$=25 Ω; parameter: $T_{j(start)}$

**Diagram 14: Typ. gate charge**



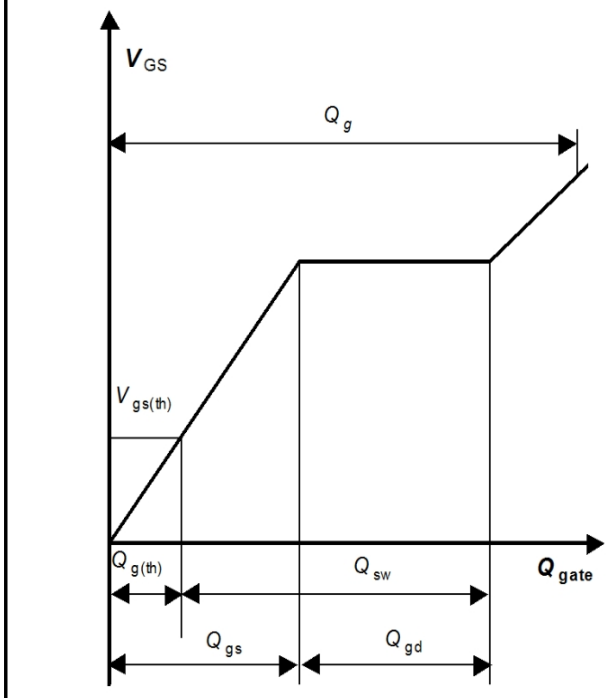

$V_{GS}$=f($Q_{gate}$); $I_D$=50 A pulsed; parameter: $V_{DD}$

**Diagram 15: Drain-source breakdown voltage**

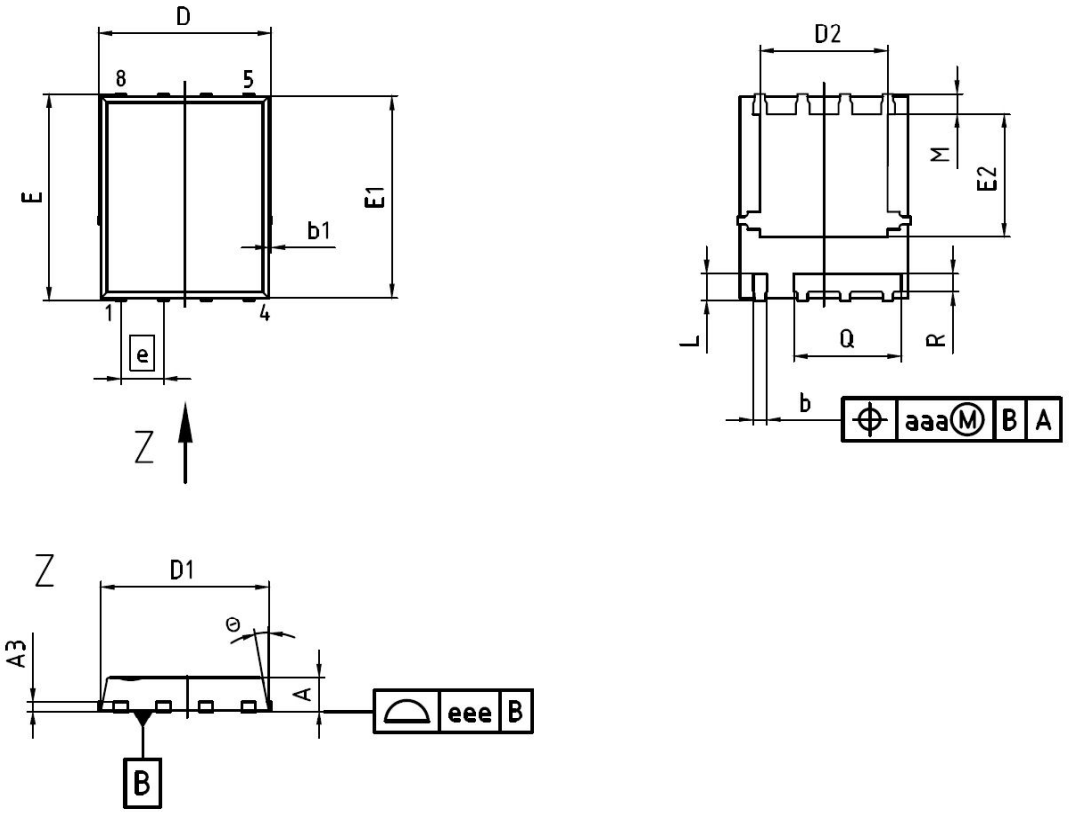



$V_{BR(DSS)}$=f($T_j$); $I_D$=1 mA

Gate charge waveforms



## 5 Package Outlines




| DIM | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 0.90 | 1.10 | 0.035 | 0.043 |
| A3 | 0.25 (REF) | | 0.011 (REF) | |
| b | 0.34 | 0.54 | 0.013 | 0.021 |
| b1 | 0.02 | 0.22 | 0.001 | 0.009 |
| D | 5.15 (BSC) | | 0.203 (BSC) | |
| D1 | 5.00 (BSC) | | 0.197 (BSC) | |
| D2 | 3.70 | 4.40 | 0.146 | 0.173 |
| E | 6.15 (BSC) | | 0.242 (BSC) | |
| E1 | 6.00 (BSC) | | 0.236 (BSC) | |
| E2 | 3.40 | 3.80 | 0.134 | 0.150 |
| e | 1.27 (BSC) | | 0.050 (BSC) | |
| N | 8 | | 8 | |
| L | 0.74 | 0.84 | 0.029 | 0.033 |
| M | 0.45 | 0.66 | 0.018 | 0.026 |
| Θ | 8.5° | 12° | 8.5° | 12° |
| Q | 3.15 | 3.25 | 0.124 | 0.128 |
| R | 0.48 | 0.58 | 0.019 | 0.023 |
| aaa | 0.25 | | 0.010 | |
| eee | 0.08 | | 0.003 | |

DOCUMENT NO.
Z8B00162237

SCALE
0
2.5
0 2.5
5mm

EUROPEAN PROJECTION

ISSUE DATE
02-08-2011

REVISION
01

**Figure 1 Outline TDSON-8 FL, dimensions in mm/inches**

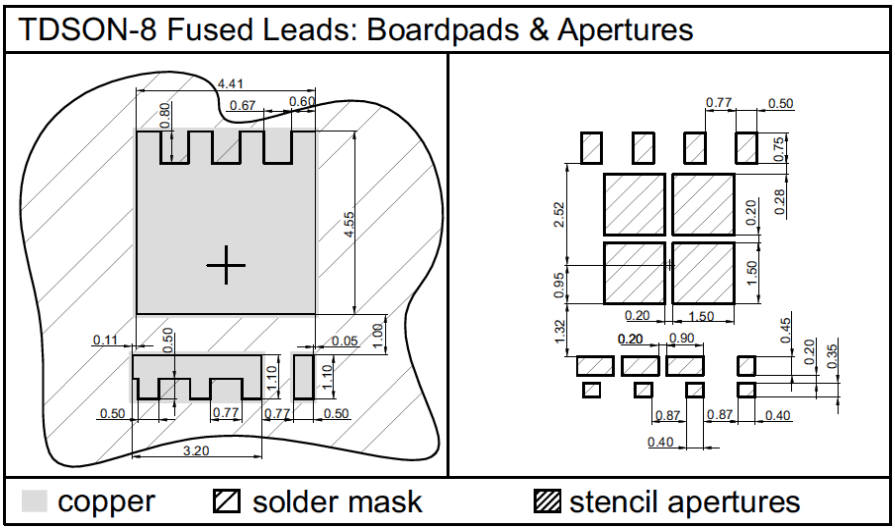



**Figure 2 Outline Footprint (TDSON-8 FL)**

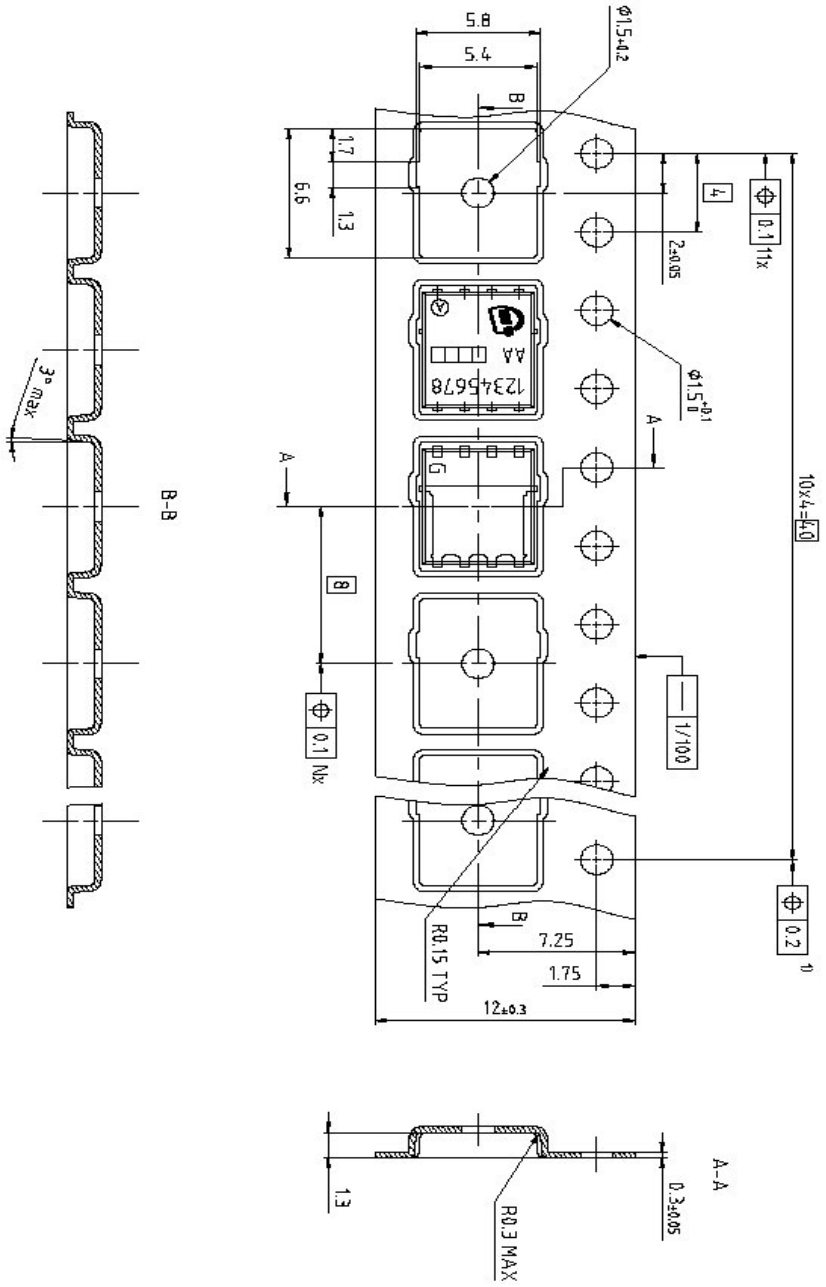



**Figure 3 Outline Tape (TDSON-8 FL )**

## Revision History

BSC019N06NS

**Revision: 2017-03-20, Rev. 2.1**

| Previous Revision | | |
|---|---|---|
| Revision | Date | Subjects (major changes since last revision) |
| 2.0 | 2016-01-11 | Release of final version |
| 2.1 | 2017-03-20 | Rev. 2.0 |



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