CAD for Electronics LAB MANUAL

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List of Experiments:

Part A

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2. (a)Transient Analysis of NMOS inverter using step input.
   (b) Transient Analysis of NMOS inverter using pulse input.
   (c) DC Analysis (VTC) of NMOS inverter.
3. (a) Analysis of CMOS inverter using step input.
   (b) Transient Analysis of CMOS inverter using step input with parameters.
   (c) Transient Analysis of CMOS inverter using pulse input.
   (d) Transient Analysis of CMOS inverter using pulse input with parameters.
   (e) DC Analysis (VTC) of CMOS inverter with and without parameters.
4. Transient & DC Analysis of NAND Gate using CMOS inverter.
5. Transient Analysis of NOR Gate inverter and implementation of XOR gate using NOR gate.
6. To design and perform transient analysis of D latch using CMOS inverter.
7. To design and perform the transient analysis of SR latch circuit using CMOS inverter.
8. To design and perform the transient analysis of CMOS transmission gate.
9. Analysis of frequency response of Common Source amplifiers.
10. Analysis of frequency response of Source Follower amplifiers

Part B:

HDL (using VHDL program module & verilog Module)

VHDL PROGRAMS

1. Design and Simulation of Full Adder using VHDL program module
2. Design and Simulation of 4x1 MUX using VHDL program module
3. Design and Simulation of BCD to Excess-3 code using VHDL program module
4. Design and Simulation of 3 to 8 decoder using VHDL program module
5. Design and Simulation of JK Flip-flop using VHDL program module **6.** Design and Simulation of CMOS Inverter using verilog Module

EXPERIMENT NO-1

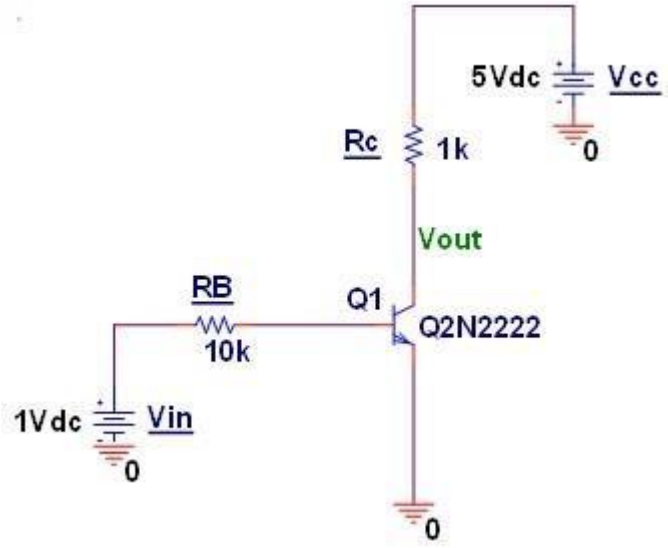
OBJECTIVE: (a) Transient Analysis of BJT inverter using step input.

(b) DC Analysis (VTC) of BJT inverter with and without parameters.

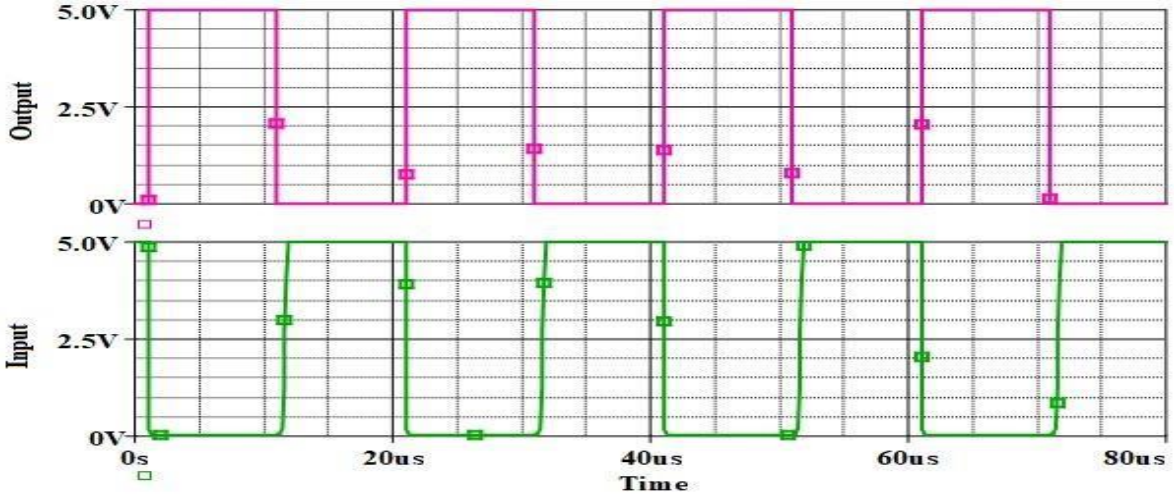
SOFTWARE : ORCAD Capture CIS

Theory: - The inverter is truly the nucleus of all digital designs. The inverter circuit using Bipolar Junction Transistor (BJT) is shown in Fig.1. When the input voltage is low, the transistor does not conduct, there is no current through R_C, and the collector voltage (output) is pulled up to V_{CC}. When the input voltage is increased, the transistor beings to conduct, the voltage drop across R_C start increasing, and the output voltage falls. Finally, when the input voltage is high enough to drive the transistor into saturation, there is a fixed small drop (V_{CE} = 0.1 to 0.2 V) across the transistor, and the output voltage saturates to this low value.

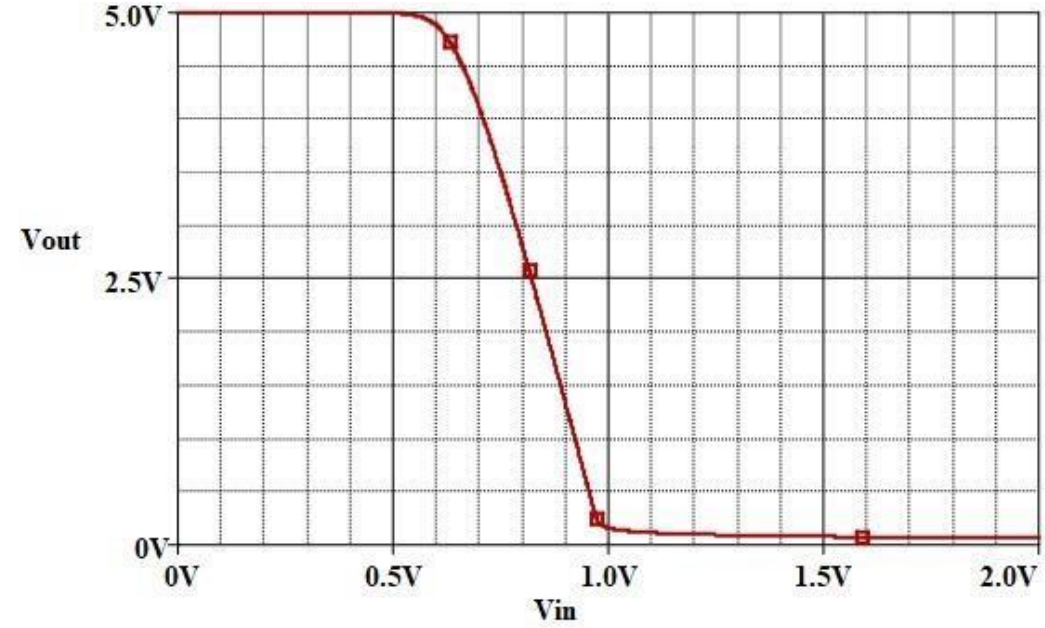
Schematic on ORCAD Capture CIS:- The schematic of BJT inverter is drawn on Capture CIS as shown in Fig.3.

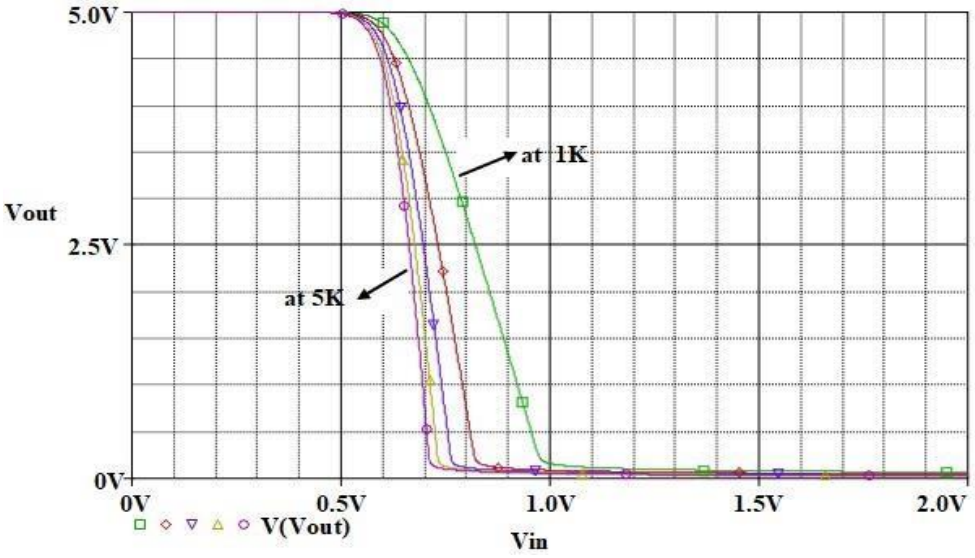


(a) Transient Analysis of BJT inverter using step input.



(b) DC analysis of BJT inverter: -





Result: The Transient and DC analysis of BJT inverter in PSPICE has been done and the waveform were plotted successfully.

EXPERIMENT NO-2

OBJECTIVE: (a)Transient Analysis of NMOS inverter using step input.

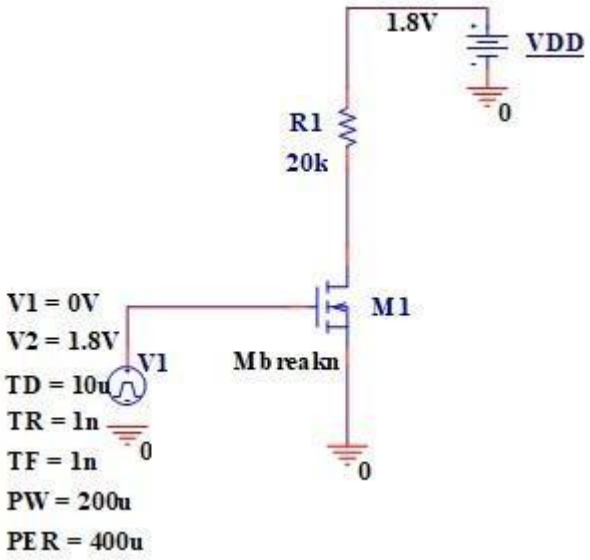
(b) Transient Analysis of NMOS inverter using pulse input.

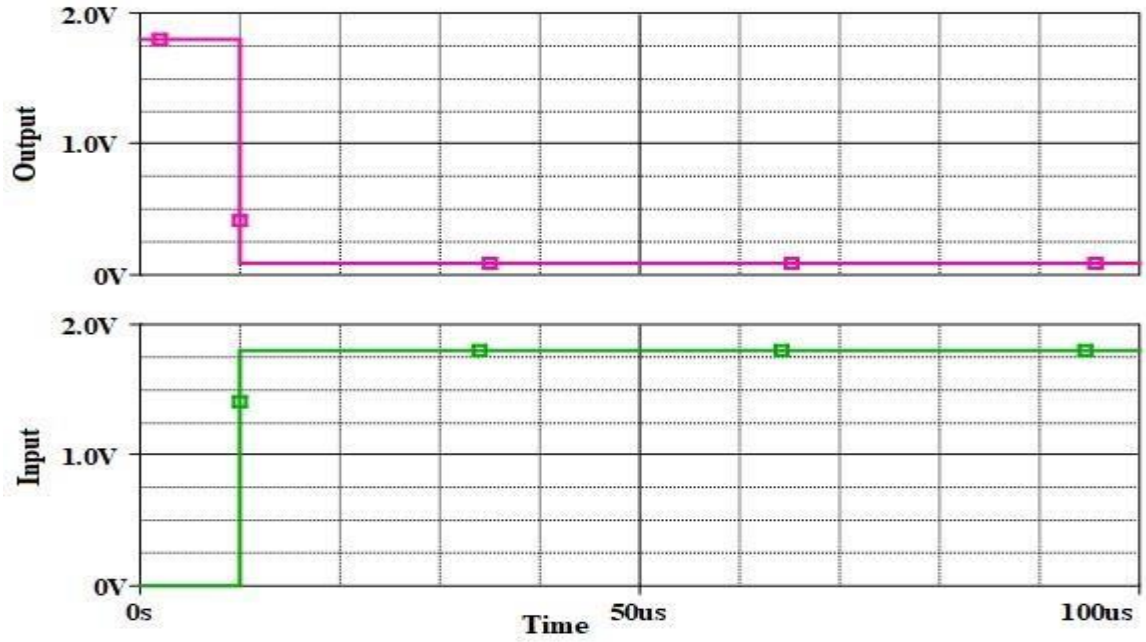
(c) DC Analysis (VTC) of NMOS inverter.

SOFTWARE / TOOL REQUIRED: ORCAD Capture CIS

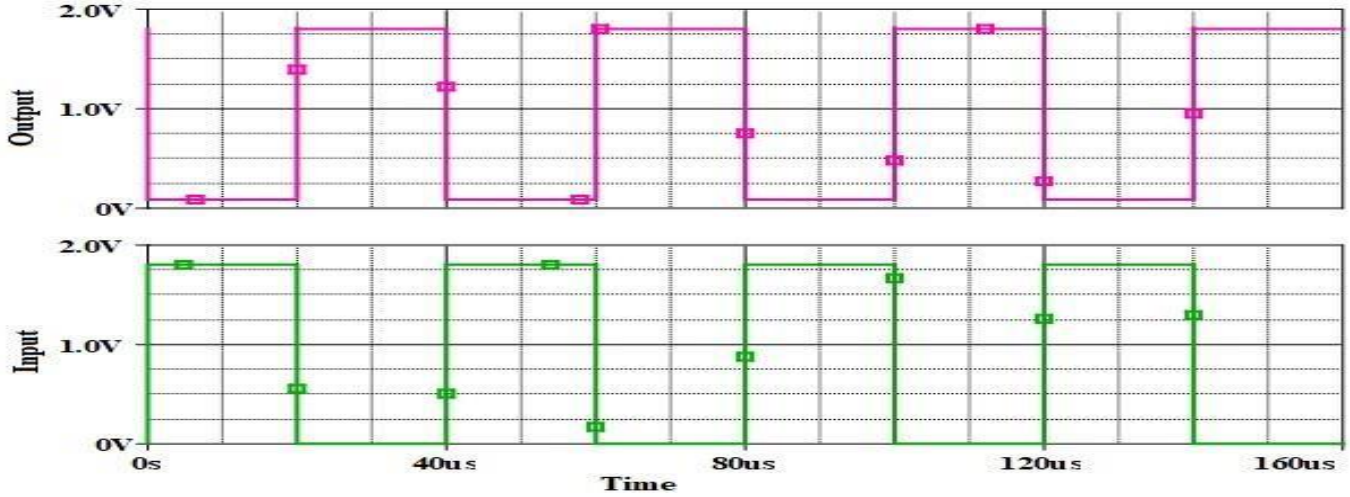
Theory: The basic structure of a resistive load inverter is shown in the Fig.1. Here, enhancement type NMOS acts as the driver transistor. The load consists of a simple linear resistor R_L. The power supply of the circuit is V_{DD} and the drain current I_D is equal to the load current I_R. When the input of the driver transistor is less than threshold voltage V_{Th} (i.e.$V_{in} < V_{Th}$), driver transistor is in the cut – off region and does not conduct any current. So, the voltage drop across the load resistor is ZERO and output voltage is equal to the V_{DD}. Now, when the input voltage increases further, driver transistor will start conducting the non-zero current and NMOS goes in saturation region.

(a) Transient Analysis of NMOS inverter using step input.

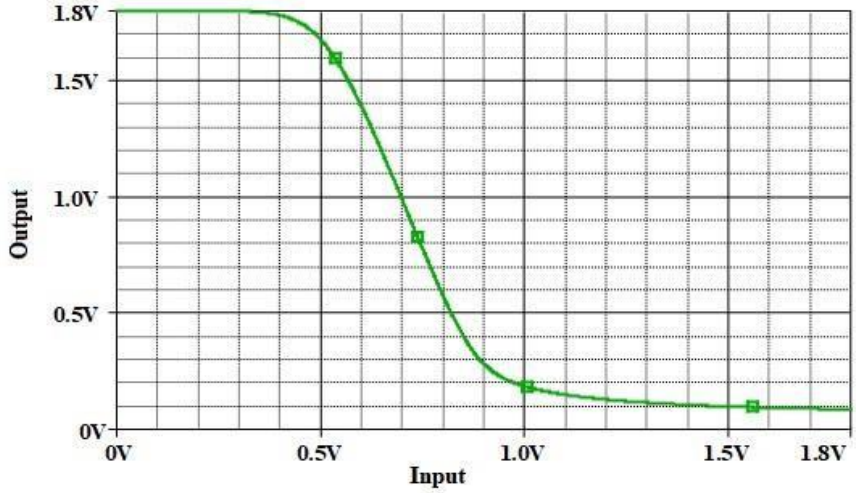




(b) Transient Analysis of NMOS inverter using pulse input.



(c) DC Analysis (VTC) of NMOS inverter:



Result: The Transient and DC analysis of NMOS inverter in PSPICE has been done and the waveform were plotted successfully.

EXPERIMENT NO-3

OBJECTIVE: (a) Analysis of CMOS inverter using step input.

(b) Transient Analysis of CMOS inverter using step input with parameters.

(c) Transient Analysis of CMOS inverter using pulse input.

(d) Transient Analysis of CMOS inverter using pulse input with parameters.

(e) DC Analysis (VTC) of CMOS inverter with and without parameters.

SOFTWARE / TOOL REQUIRED: ORCAD PSPICE A/D, 180nm TSMC technology parameter.

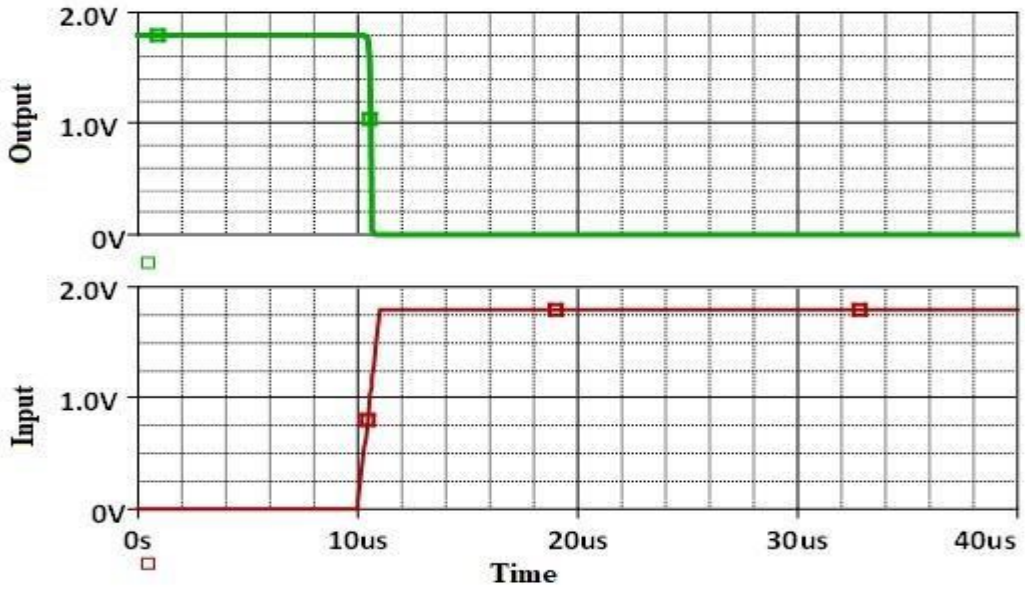
Theory: The term CMOS stands for complementary metal oxide semiconductor. The basic structure of a Complementary Metal oxide semiconductor inverter consists of an n-MOS transistor and p-MOS transistor as a load and the gates of the two transistors are shorted at the input and the drains of the two transistors are also shorted where the output is obtained

PSPICE Code and Simulation Result:

(a) PSPICE code for Analysis of CMOS inverter using step input.

```
Mn No Ni 0 0 NMOS W=0.18u L=0.18u
Mp No Ni Ndd Ndd PMOS W=4.5u L=0.18u
Vdd Ndd 0 1.8V
Vi Ni 0 PWL(10u 0 11us 1.8V 1ms 1.8V)        ; Step input of rise time 1us and starting from
10us
.tran 1u 40u                                  ; step size=1u and time spam= 0 to 40us
.probe
.end
```

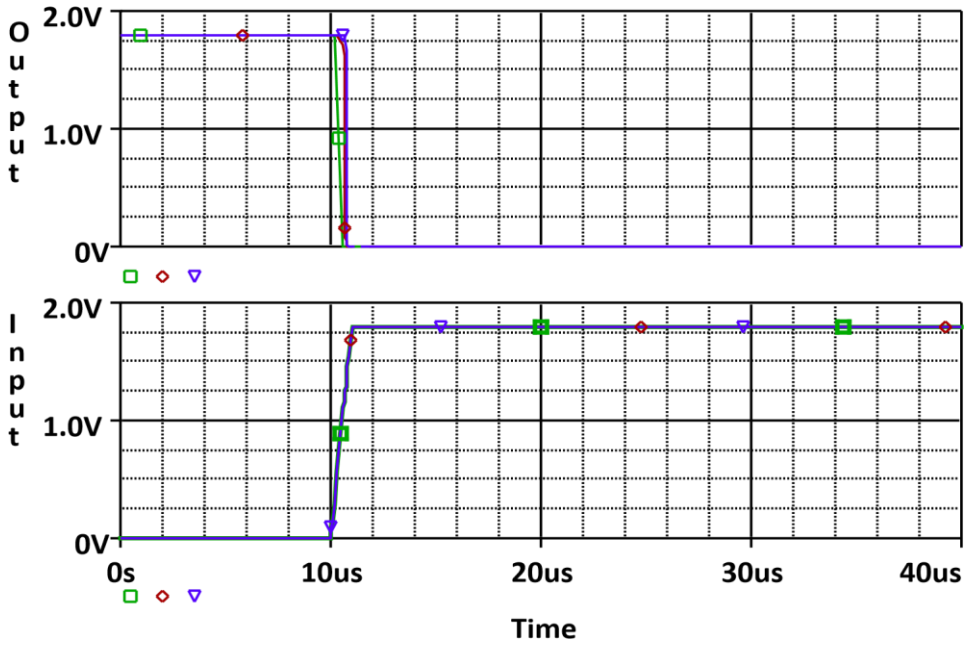
Simulation Result:



(b) PSPICE code for Transient Analysis of CMOS inverter using step input with parameters.

```
Mn No Ni 0 0 NMOS W=0.18u L=0.18u
Mp No Ni Ndd Ndd PMOS W={var} L=0.18u
Vdd Ndd 0 1.8V
Vi Ni 0 PWL(10u 0 11us 1.8V 1ms 1.8V)        ; Step input of rise time 1us and starting from 10u
.param var = 0.45u
.step param var list 0.18u 18u 180u   ; Variation of Channel length of PMOS transistor .tran 1u
40u
.probe .end
```

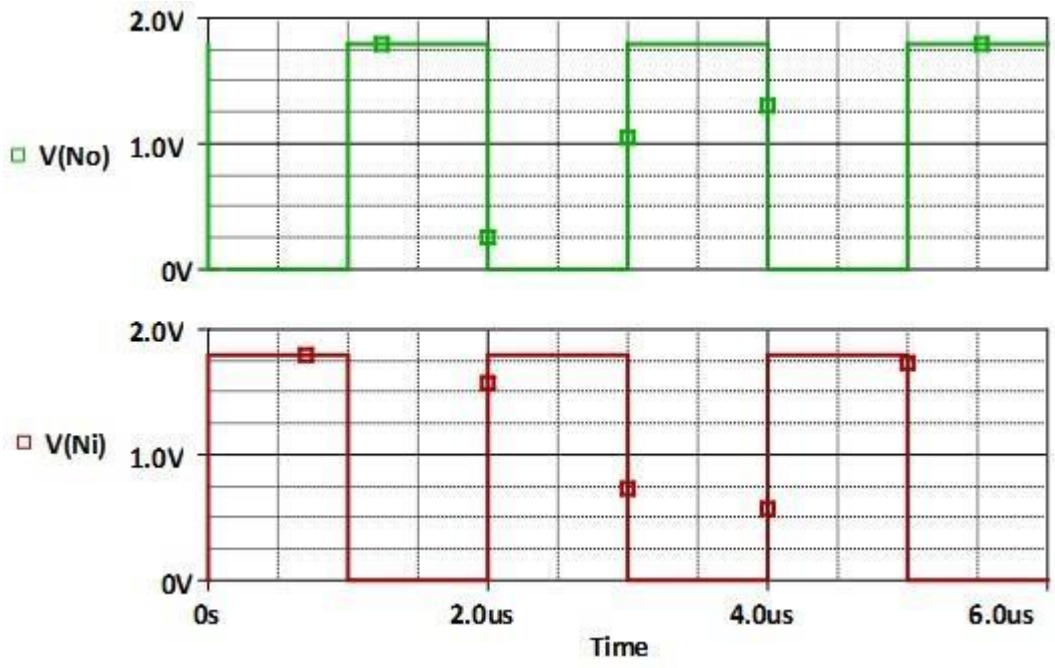
Simulation Result:



(c) PSPICE code for Transient Analysis of CMOS inverter using pulse input.

```
Mn No Ni 0 0 NMOS W=0.18u L=0.18u
Mp No Ni Ndd Ndd PMOS W=0.36u L=0.18u
Vdd Ndd 0 1.8V
Vi Ni 0 Pulse(0 1.8V 0 1n 1n 1u 2u)
.tran 1u 6u
.probe
.end
```

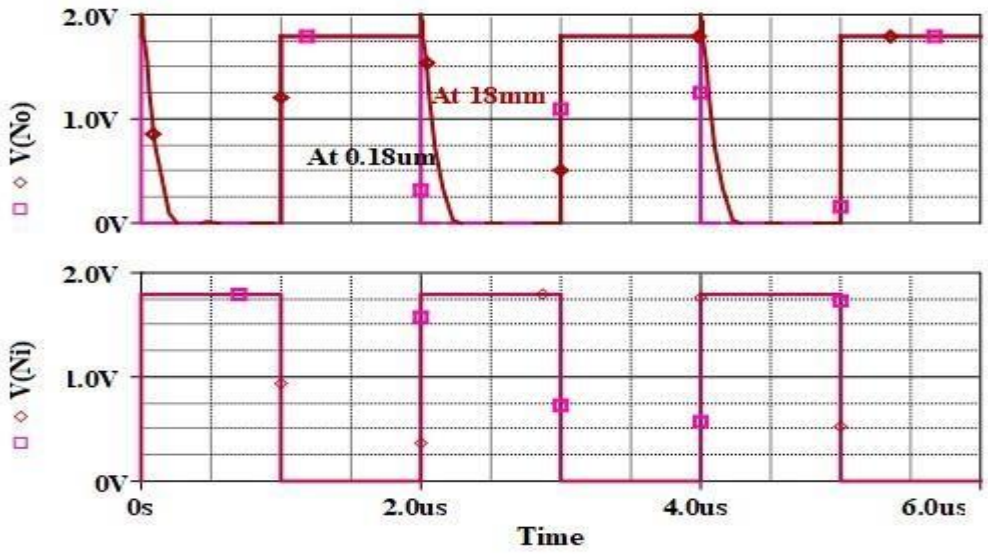
Simulation Result:



(d) PSPICE code for Transient Analysis of CMOS inverter using pulse input with parameters.

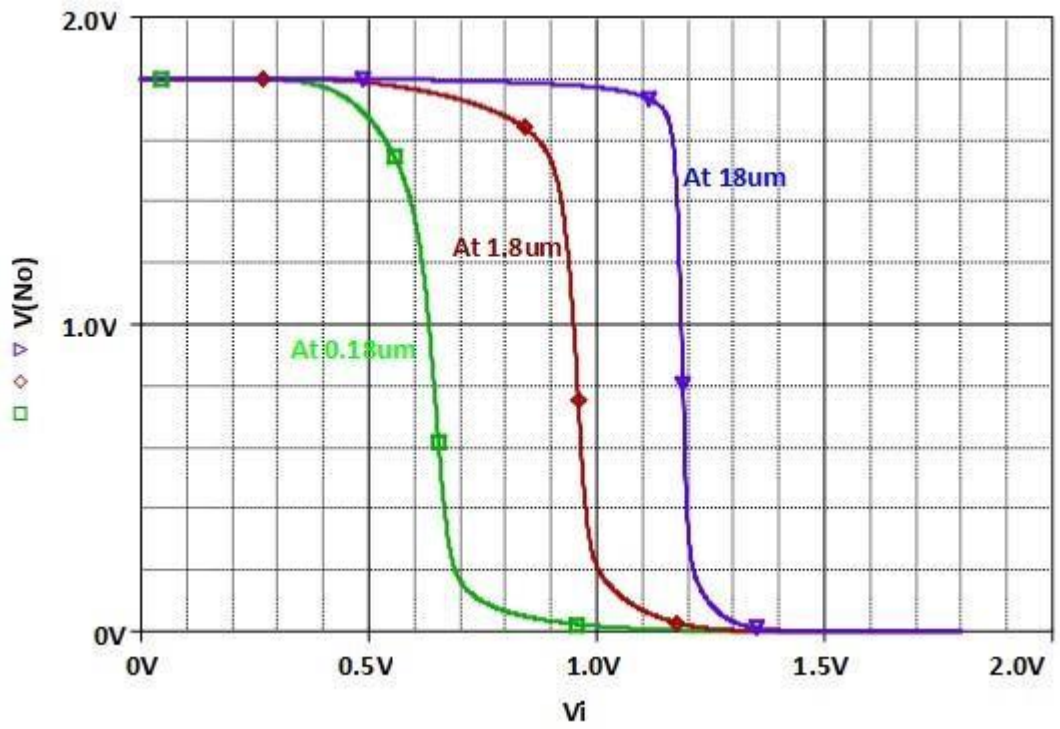
```
Mn No Ni 0 0 NMOS W=0.18u L=0.18u
Mp No Ni Ndd Ndd PMOS W={var} L=0.18u
Vdd Ndd 0 1.8V
Vi Ni 0 Pulse(0 1.8V 0 1n 1n 1u 2u)
.param var = 0.45u
.step param var list 0.18u 18m  ; Variation of Channel length of PMOS transistor .tran 1u 6u
.probe
.end
```

Simulation Result:



(d.1) PSPICE code for DC Analysis (VTC) of CMOS inverter with parameters:

```
Mn No Ni 0 0 NMOS W=0.18u L=0.18u
Mp No Ni Ndd Ndd PMOS W={var} L=0.18u
Vdd Ndd 0 1.8V
Vi Ni 0 1.8V
.param var = 0.45u
.step param var list 0.18u 1.8u 18u
.dc Vi 0 1.8v 1m
.probe
.end
```



Result: DC analysis and transient analysis of CMOS inverter is carried out and the simulation results are verified through PSPICE simulation using 180nm TSMC technology parameter.

EXPERIMENT NO-4

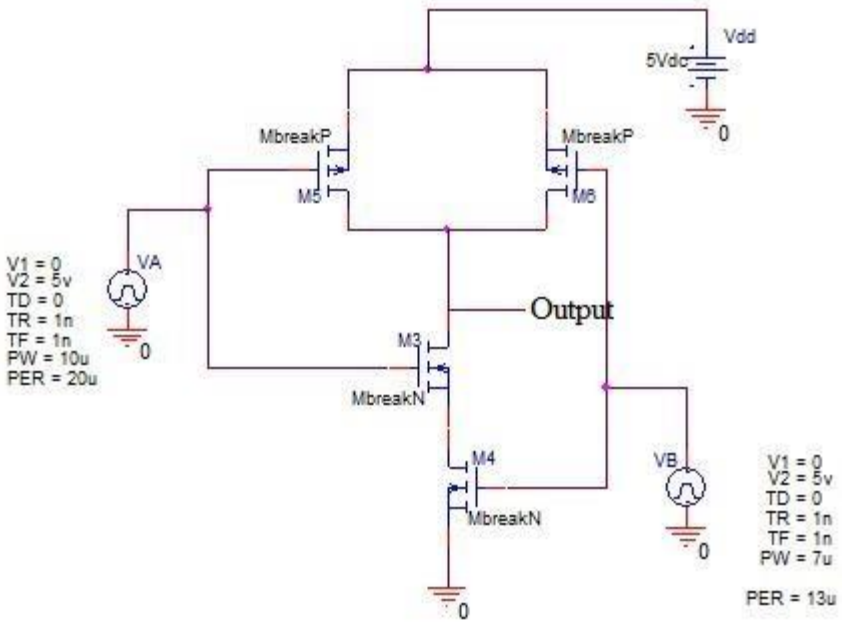
OBJECTIVE: Transient & DC Analysis of NAND Gate using CMOS inverter.

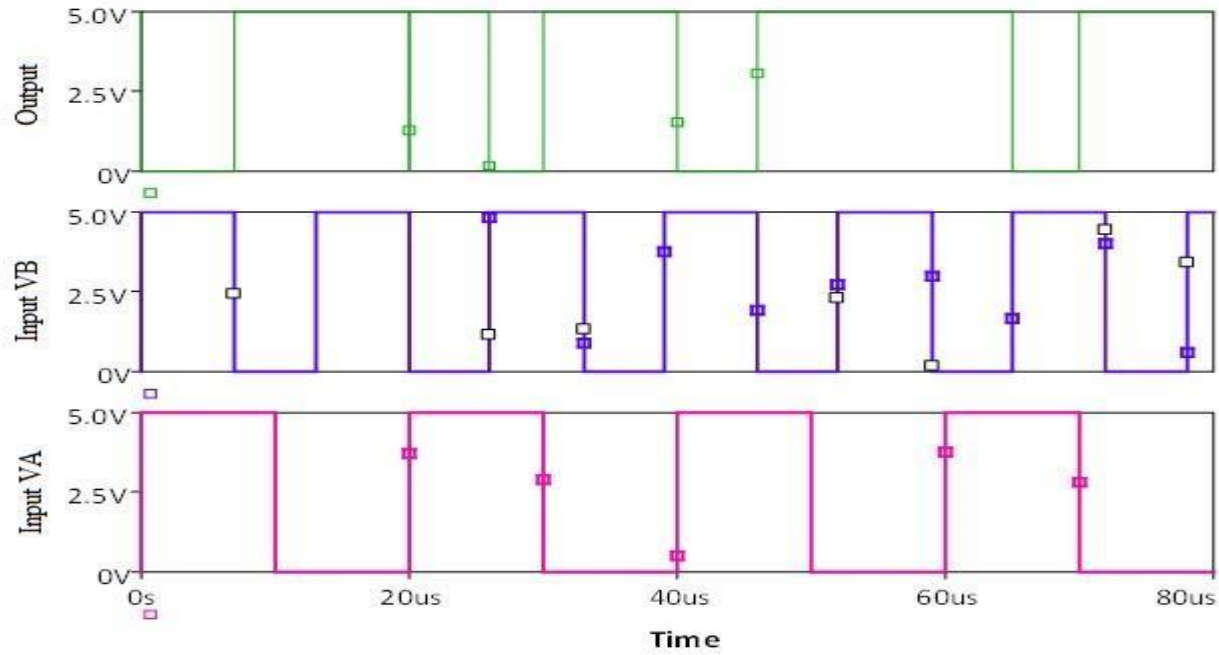
SOFTWARE REQUIRED: ORCAD Capture CIS, 180nm TSMC technology parameter.

THEORY:

NAND Gate: The NAND gate is a digital logic gate with 'n' inputs one output, that performs the operation of the AND gate followed by the operation of the NOT gate. If the input of the NAND gate high, then the output of the gate will be low

Schematic on ORCAD PSPICE:





Result: The output of 2 input NAND Gate is verified through PSPICE simulation.

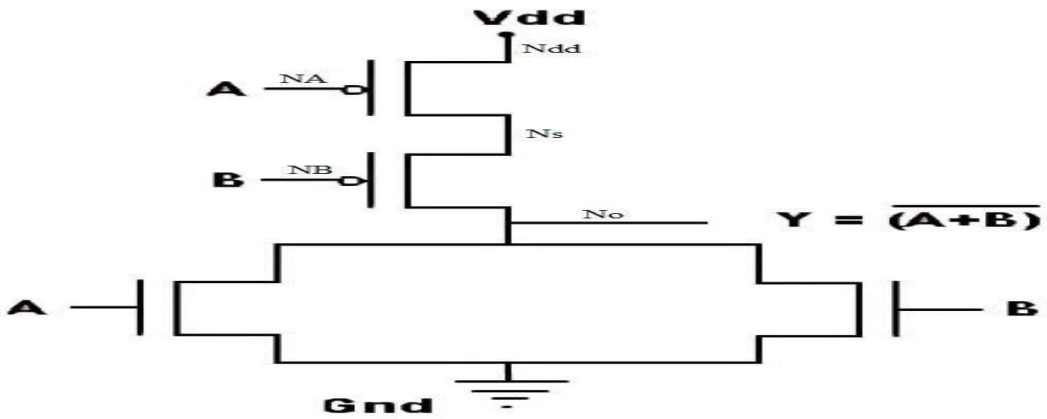
EXPERIMENT NO-5

OBJECTIVE: Transient Analysis of NOR Gate and implementation of XOR gate using NOR gate.

SOFTWARE REQUIRED: ORCAD PSPICE A/D, 180nm TSMC technology parameter.

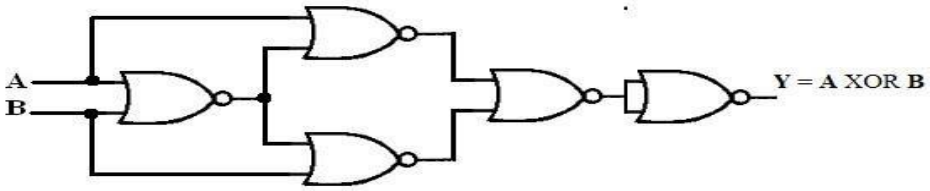
THEORY:

NOR Gate: The NOR gate is a digital logic gate with n inputs and one output, that performs the operation of the OR gate followed by the NOT gate. NOR gate is designed by combining the OR and NOT gate. When any one of the inputs of the NOR gate is true, then the output of the NOR gate will be false. The symbol and truth table of the NOR gate with the truth table is shown below.



XOR Gate: The Exclusive-OR gate is a digital logic gate with two inputs and one output. The short form of this gate is Ex-OR. If any one of the inputs of this gate is high, then the output of the EX-OR gate will be high. The symbol and truth table of the EX-OR are shown below.

Implementation of XOR Gate using NOR Gate



PSPICE Code and Simulation Result

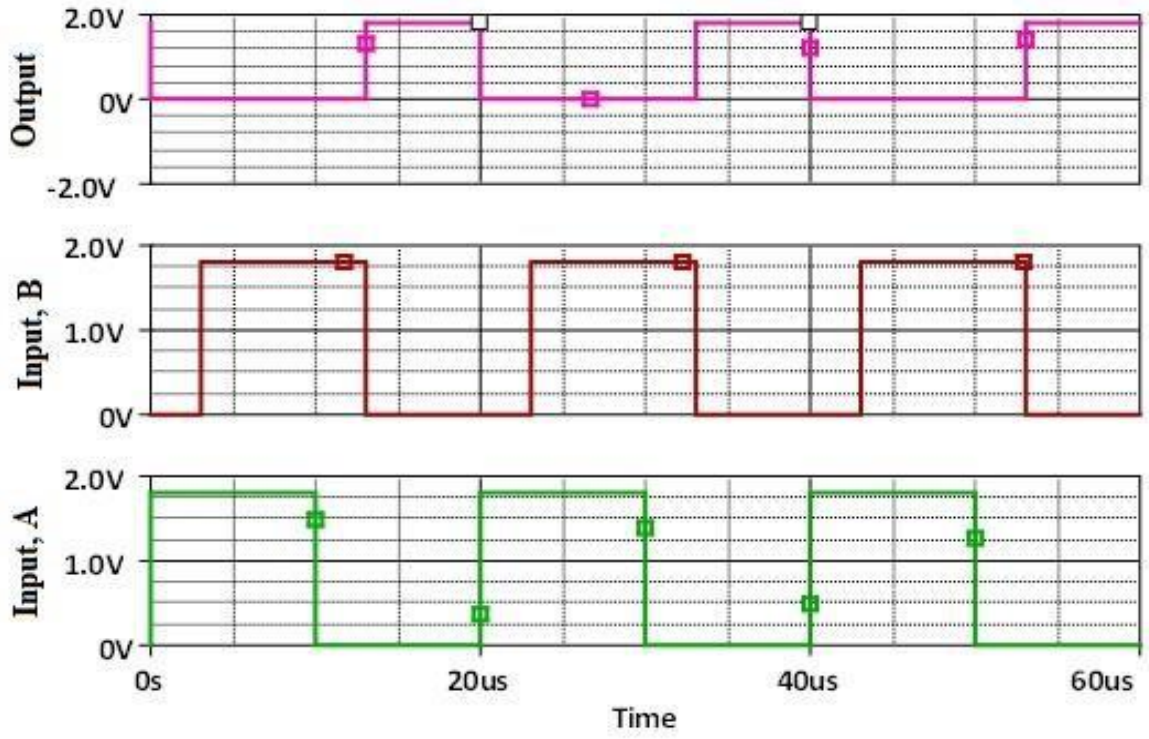
(a) PSPICE Code for NOR Gate: PSPICE code for the circuit of Fig.1 is written below.

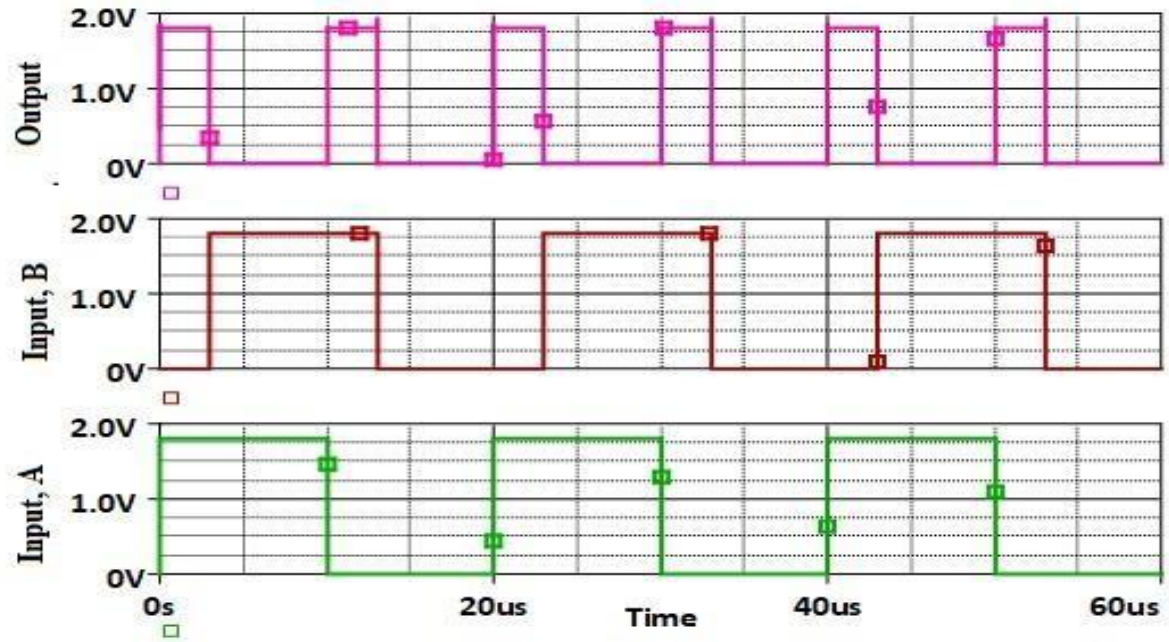
```
Mn1 No NA 0 0 NMOS W=0.18u L =0.18u
Mn2 No Nb 0 0 NMOS W=0.18u L =0.18u
Mn3 No Nb Ns Ns PMOS W=0.9u L =0.18u
Mn4 Ns NA Ndd Ndd PMOS W=0.9u L =0.18u
Vdd Ndd 0 1.8V
C No 0 1p
VA Na 0 pulse(0 1.8V 0 1n 1n 10u 20u)
```

```
VB Nb 0 pulse(0 1.8v 3u 1n 1n 10u 20u)
.tran 1u 60u
.probe
.end
```

(b)PSPICE code for XOR Gate using NOR gate: PSPICE code for the XOR gate using NOR gate as shown in circuit of Fig.2 is written below.

```
.subckt NOR NA Nb No
Mn1 No NA 0 0 NMOS W=0.18u L =0.18u
Mn2 No Nb 0 0 NMOS W=0.18u L =0.18u
Mn3 No Nb Ns Ns PMOS W=0.9u L =0.18u
Mn4 Ns NA Ndd Ndd PMOS W=0.9u L =0.18u
Vdd Ndd 0 1.8V
.ends
X1 NAi NBi No1 NOR
X2 NAi No1 No2 NOR
X3 NBi No1 No3 NOR
X4 No2 No3 No4 NOR
X5 NO4 NO4 Nout NOR
VA NAi 0 pulse(0 1.8V 0 1n 1n 10u 20u)
VB NBi 0 pulse(0 1.8v 3u 1n 1n 10u 20u)
.tran 1u 60u
.probe
.end
```





Result: The transient response of NOR gate and XOR gate is verified through PSPICE simulation using 180nm TSMC technology parameter.

EXPERIMENT NO-6

OBJECTIVE: To design and perform transient analysis of D latch using CMOS inverter.

SOFTWARE REQUIRED: ORCAD PSPICE A/D, 180nm TSMC technology parameter.

THEORY: A simple implementation of D latch is shown in Fig.1. The circuit consists of two inverters connected in a positive feedback loop. The loop is closed when the clock is low (Φ =0 and Φbar =1). The input D is connected to the flip flop through a switch that closes when the clock is high.

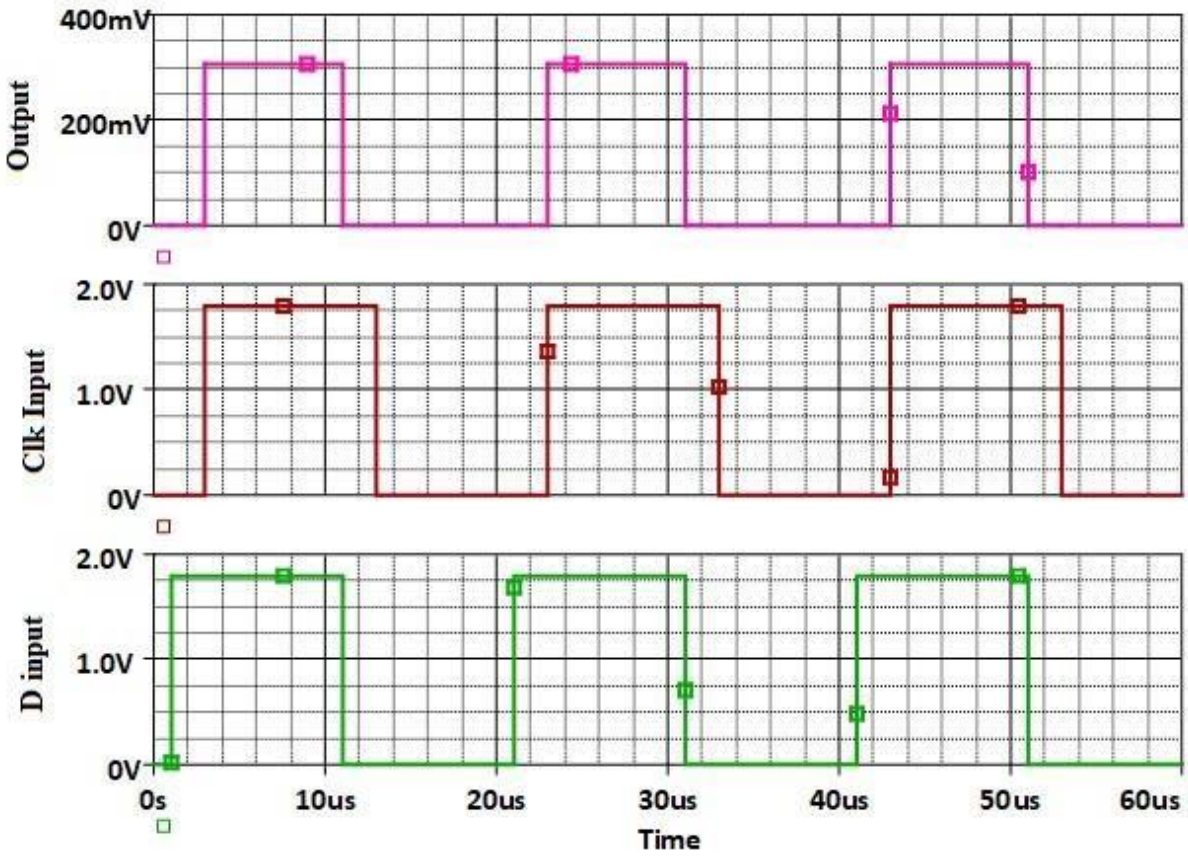
PSPICE Code and Simulation Result

PSPICE Code

```
.subckt INV Ni No
Mn No Ni 0 0 NMOS W=0.18u L=0.18u
Mp No Ni Ndd Ndd PMOS W=4.5u L=0.18u
Vdd Ndd 0 1.8V
.ends
X1 N1 No1 INV
X2 No1 No2 INV
Mn1 Ni Nclk N1 N1 NMOS W=0.9u L=0.18u
Mn2 No2 Nclkb N1 N1 NMOS W=0.9u L=0.18u
Vi Ni 0 pulse(0 1.8V 1u 1n 1n 10u 20u)
Vclk Nclk 0 pulse(0 1.8V 3u 1n 1n 10u 20u)
Vclkb Nclkb 0 pulse(1.8v 0V 3u 1n 1n 10u 20u)
.tran 1u 60u
```

.probe
.end

Simulation Result:



Result: The transient analysis of D latch using CMOS inverter is performed through PSPICE simulation.

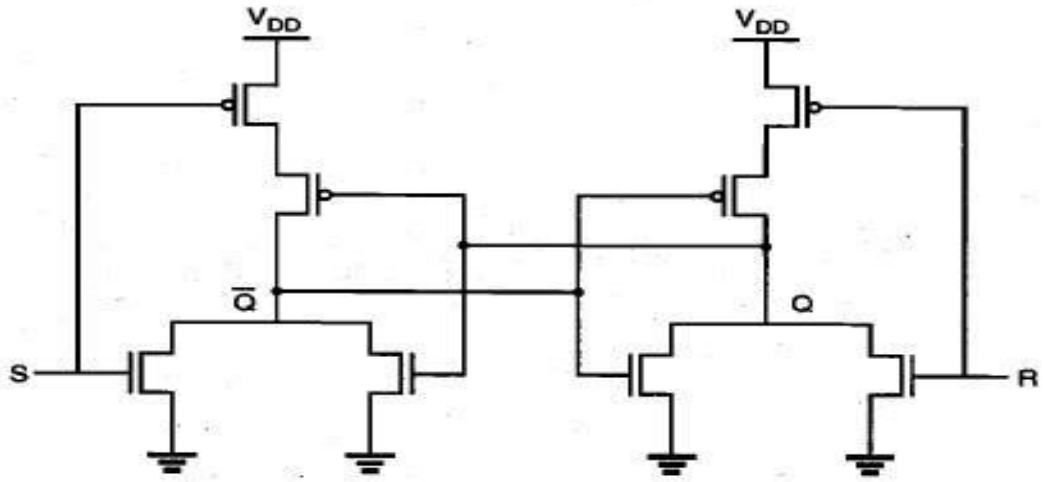
EXPERIMENT NO-7

OBJECTIVE: To design and perform the transient analysis of SR latch circuit using CMOS inverter.

SOFTWARE REQUIRED: ORCAD PSPICE A/D, 180nm TSMC technology parameter.

THEORY: Latch is bistable multivibrator circuit. Fig.1 shows the circuit structure of the simple CMOS SR latch, which has two triggering inputs, S (set) and R (reset).

If the set input (S) is equal to logic **"1"** and the reset input is equal to logic **"0."** then the output Q will be forced to logic **"1"**. While Q' is forced to logic **"0"**. This means the SR latch will be set, irrespective of its previous state. Similarly, if S is equal to "0" and R is equal to **"1"** then the output Q will be forced to **"0"** while Q' is forced to **"1"**. This means the latch is reset, regardless of its previously held state

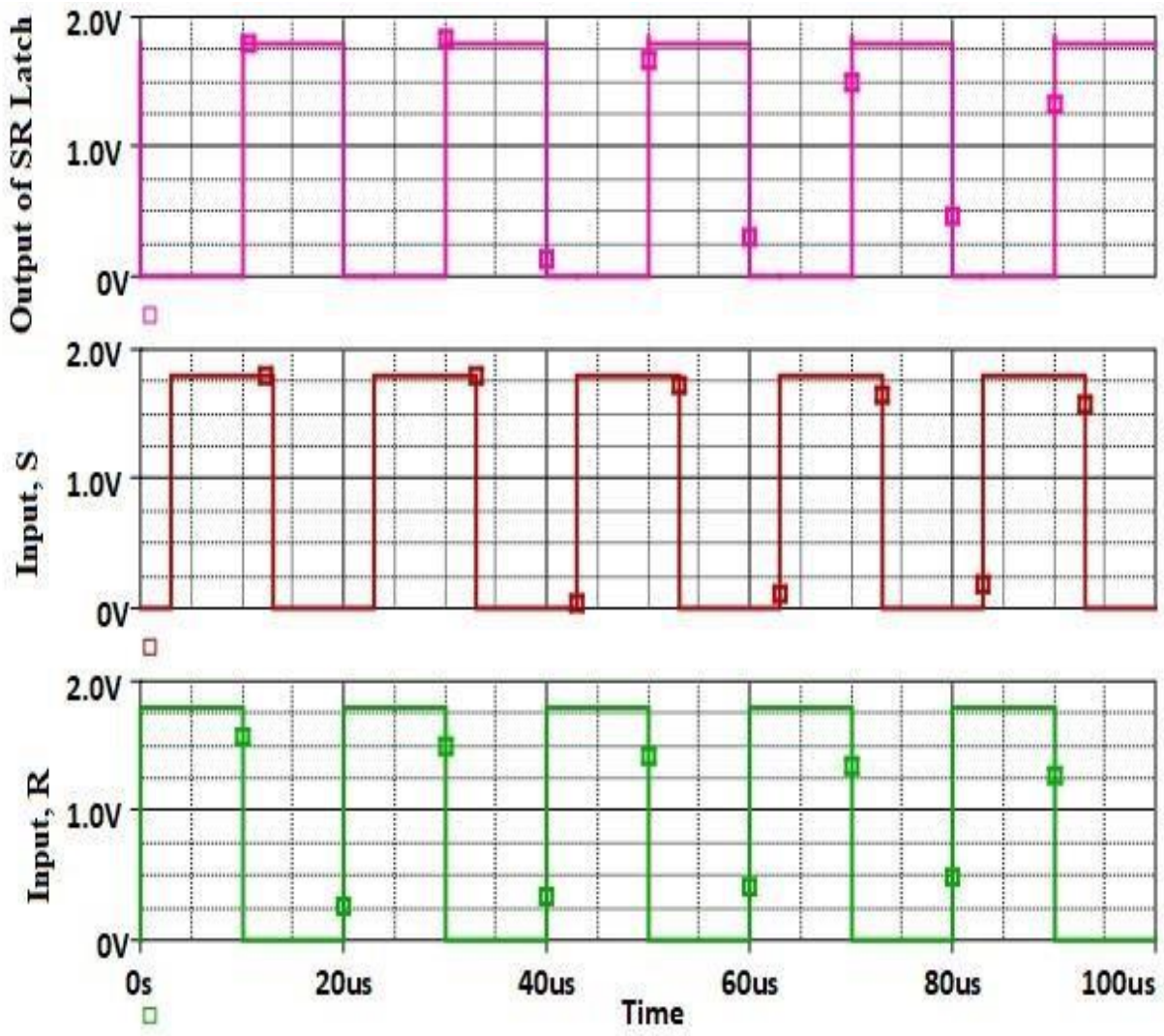


PSPICE Code and Simulation Result

PSPICE Code: PSPICE code for the SR latch shown in Fig.2 is written below.

```
.subckt NOR NA Nb No
Mn1 No NA 0 0 NMOS W=0.18u L =0.18u
Mn2 No Nb 0 0 NMOS W=0.18u L =0.18u
Mn3 No Nb Ns Ns PMOS W=0.9u L =0.18u
Mn4 Ns NA Ndd Ndd PMOS W=0.9u L =0.18u
Vdd Ndd 0 1.8V
.ends
X1 NRi Nqbar Nq NOR
X2 NSi Nq Nqbar NOR
VR NRi 0 pulse(0 1.8V 0 1n 1n 10u 20u)
VS NSi 0 pulse(0 1.8v 3u 1n 1n 10u 20u)
.tran 1u 100u
.probe
.end
```

Simulation Result: The simulated result of SR lath is shown in Fig.3.



Result: The transient analysis of SR latch is performed through PSPICE simulation.

EXPERIMENT NO-8

OBJECTIVE: Analysis of frequency response of Common Source amplifiers.

SOFTWARE REQUIRED: ORCAD PSPICE A/D, 180nm TSMC technology parameter.

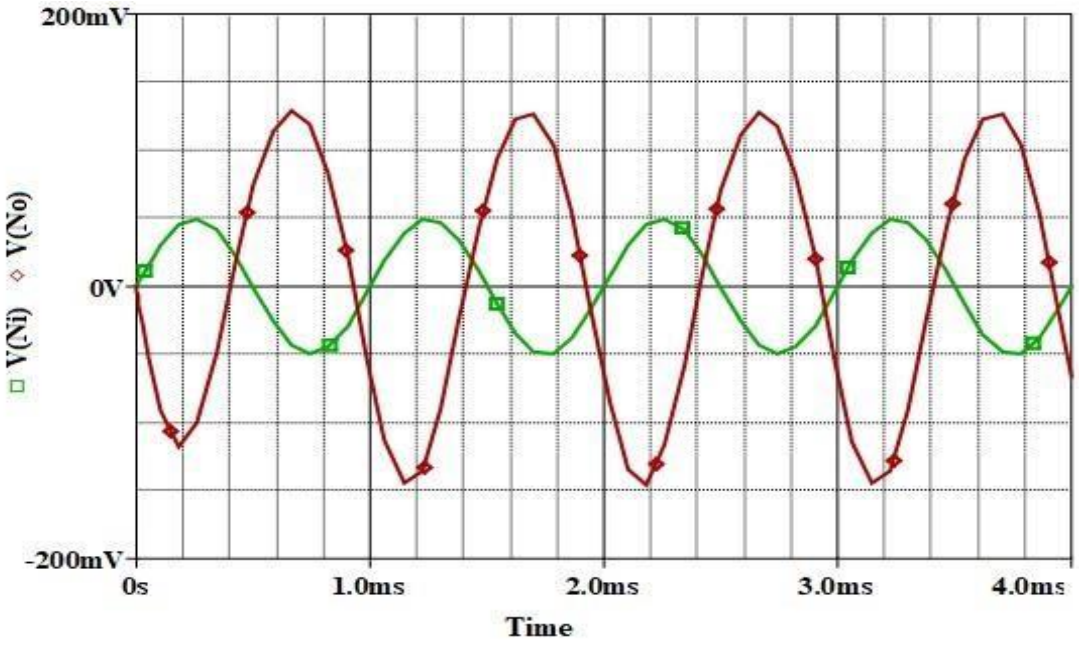
THEORY: The common source amplifier circuit is shown in Fig.1. In CS amplifier, the input is applied between gate and source while output is taken between drain and source. In this circuit the MOSFET converts variations in the gate-source voltage into a small signal drain current which passes through a resistive load and generates the amplified voltage across the load resistor.

PSPICE Code and Simulation Result:

(a) PSPICE code for transient analysis-

```
Mn Nd Ng Ns Ns NMOS W=18u L =0.18u
Rd Ndd Nd 1k
Rs Ns 0 1k  R1
Ng Ndd 100k
R2 Ng 0 100k
vdd Ndd 0 1.8V C1
Ng Ni 1u
C3 Ns 0 1u
C2 Nd No 1u
RL No 0 10k
Vi Ni 0 sin(0 50mv 1k)
.tran 1u 4m
.probe
.end
```

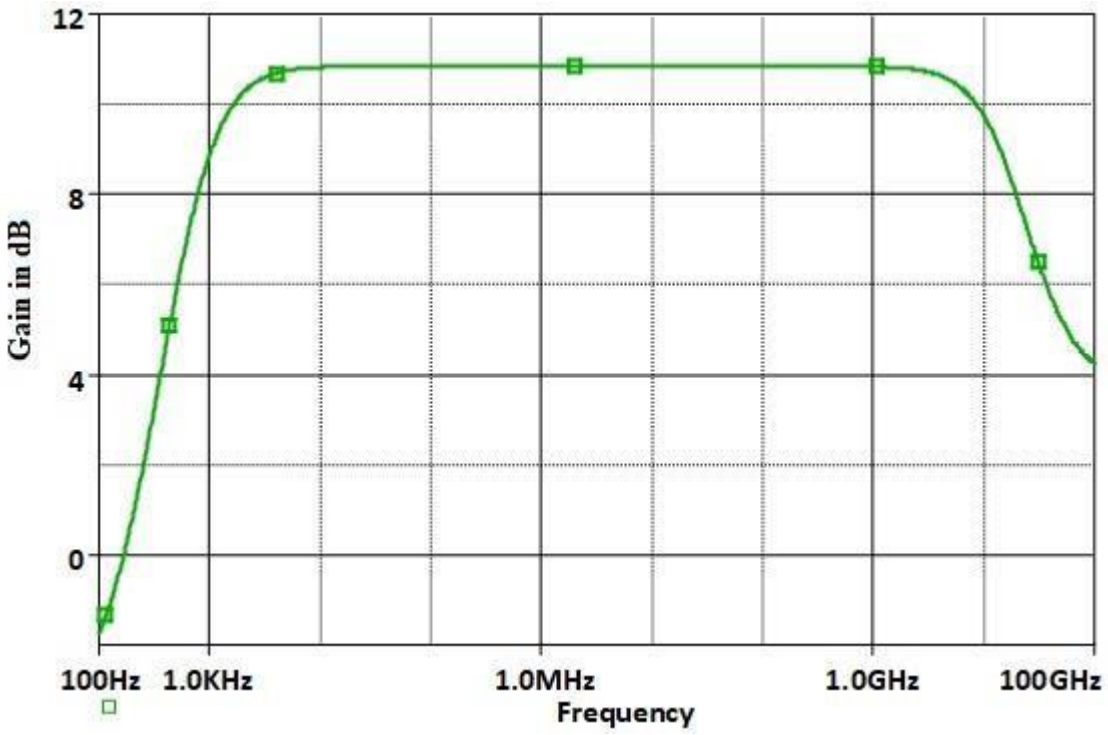
Simulation Result: The simulated transient response of CS amplifier is shown in Fig.2, which shows that input and output are out of phase.



(b) PSPICE code for frequency response:

```
Mn Nd Ng Ns Ns NMOS W=18u L =0.18u
Rd Ndd Nd 1k
Rs Ns 0 1k
R1 Ng Ndd 100k
R2 Ng 0 100k
vdd Ndd 0 1.8V
C1 Ng Ni 1u
C3 Ns 0 1u
C2 Nd No 1u
RL No 0 10k
Vi Ni 0 AC 50mv
.AC DEC 100 100HZ 100GHZ
.probe
.end
```

Simulation Result: The frequency response of CS amplifier is shown in Fig.3



Result: Transient and frequency response of CS MOSFET amplifier is carried out through PSPICE simulation using 180nm TSMC technology parameter.

EXPERIMENT NO-9

OBJECTIVE: Analysis of frequency response of Source Follower amplifiers

SOFTWARE REQUIRED: ORCAD PSPICE A/D, 180nm TSMC technology parameter.

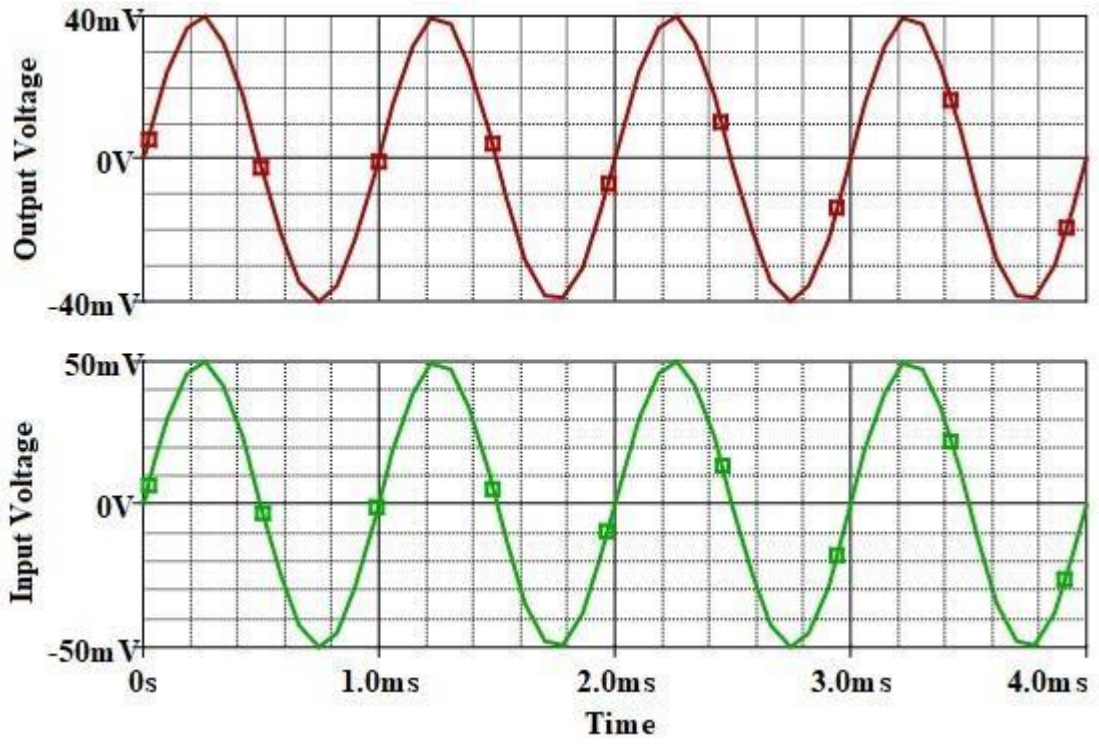
THEORY: In the common drain amplifier, the input signal is applied between gate and drain and the output voltage is developed across a resistor in the source to drain circuit. The drain is the terminal common to the input and the output sides. Since the gain to CD amplifier is approximately one, therefore it is also known as source follower

PSPICE Code and Simulation Result:

(a) PSPICE code for transient analysis-

```
Mn Nd Ng Ns Ns NMOS W=18u L =0.18u
Rd Nd Ndd 1k
Rs Ns 0 10k
R1 Ng Ndd 10meg
R2 Ng 0 10meg
Vdd Ndd 0 1.8V
C1 Ng Ni 1u
C2 Ns No 1u
RL No 0 10k
Vi Ni 0 sin(0 50mv 1k)
.tran 1u 4m
.probe
.end
```

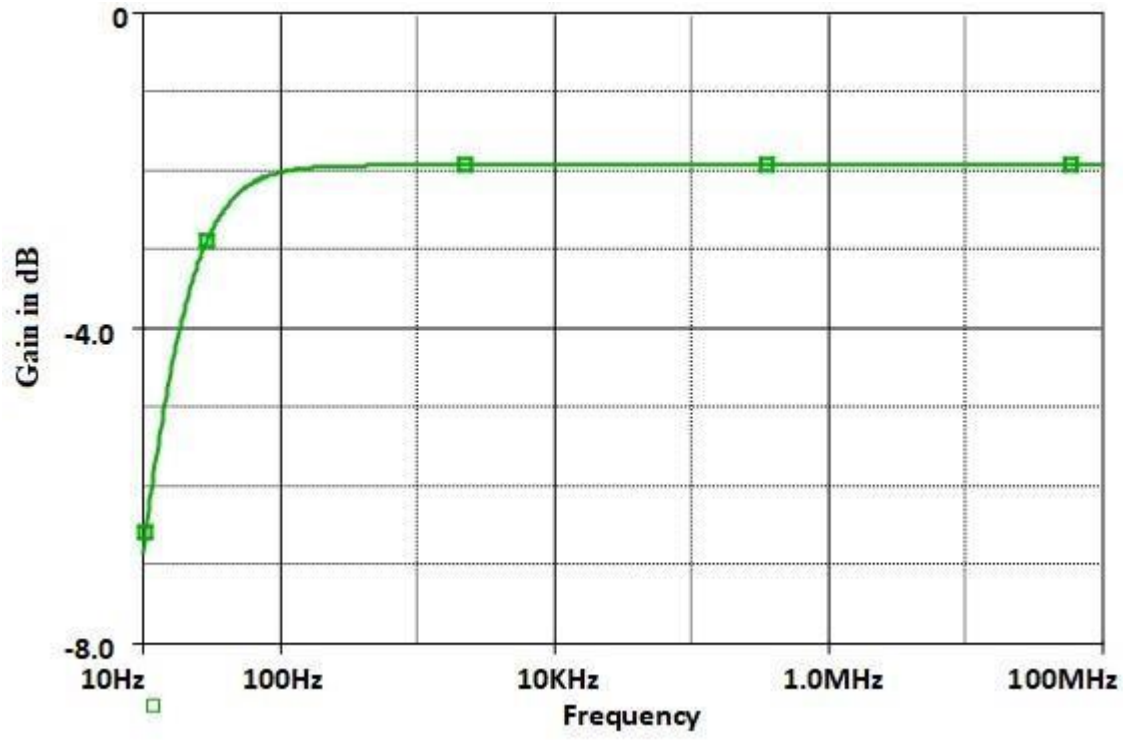
Simulation Result:



(b)PSPICE code for frequency response:

```
Mn Nd Ng Ns Ns NMOS W=18u L =0.18u
Rd Nd Ndd 1k
Rs Ns 0 10k
R1 Ng Ndd 10meg
R2 Ng 0 10meg
vdd Ndd 0 1.8V C1
Ng Ni 1u
C2 Ns No 1u
RL No 0 10k
Vi Ni 0 AC 50mv
.AC DEC 100 10HZ 100meGHZ

.probe
.end
```

Simulation Result: The frequency response of CD amplifier is shown in Fig.3



Result: Transient and frequency response of CD MOSFET amplifier is carried out through PSPICE simulation using 180nm TSMC technology parameter.

Experiment-10

OBJECTIVE: Design and Simulation of Full Adder using VHDL program module

SOFTWARE REQUIRED: Xilinx ISE

THEORY: A **full adder** is a logical circuit that performs an addition operation on three one-bit binary numbers. There are three inputs named as A and B and C_i and two outputs sum (S) and carryout (C_o) in a Full Adder.

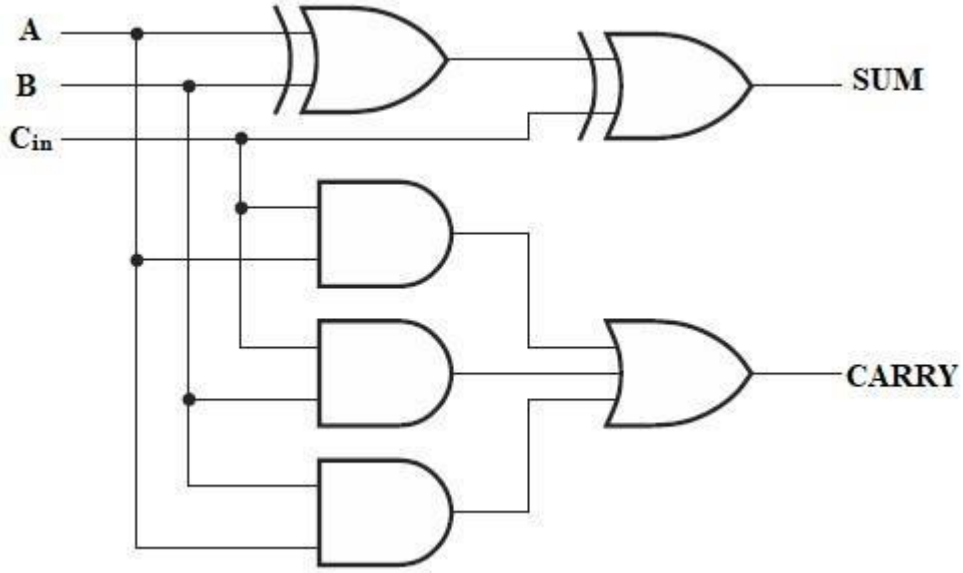
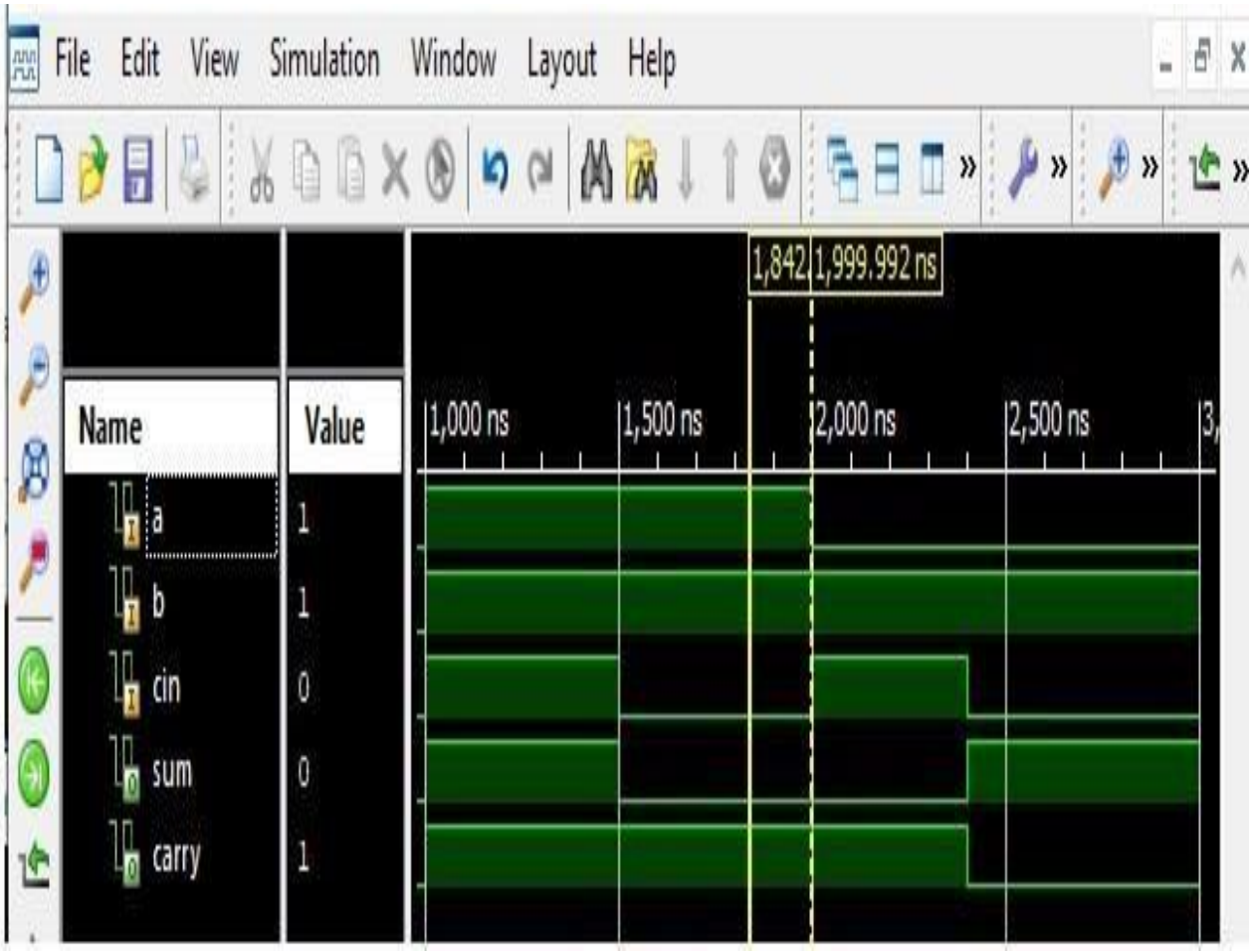


Fig. Gate level circuit diagram of Full Adder

VHDL Code:

```
library IEEE;  use
IEEE.STD_LOGIC_1164.ALL;

entity FA is
Port(A, B, Cin : in BIT;
SUM, CARRY: out BIT);  end
FA;

architecture Behavioral of FA is begin
SUM <= A xor B xor Cin ;
CARRY <= (A and B) or ((A or B) and Cin ); end
Behavioral;
```

Output waveform:



RESULT: Design and Simulation of Full Adder using VHDL program has been done and the waveform were plotted successfully.

EXPERIMENT NO -11

OBJECTIVE: Design and Simulation of 4x1 MUX using VHDL program module.

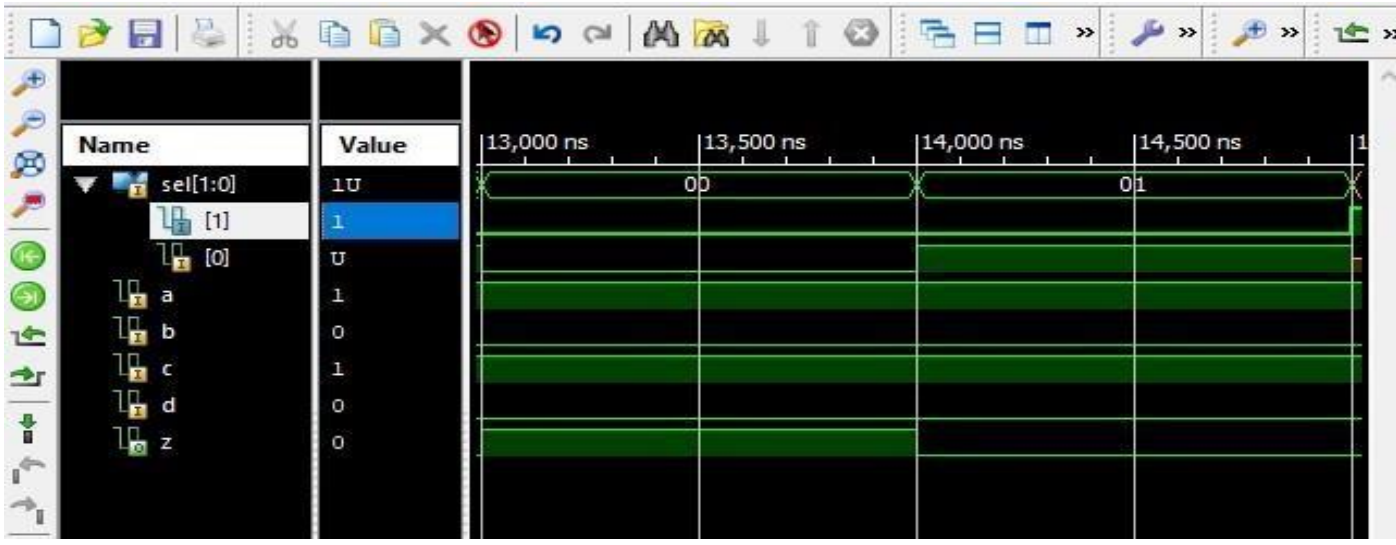
SOFTWARE REQUIRED: Xilinx ISE

THEORY: Multiplexer (MUX) select one input from the multiple inputs and forwarded to output line through selection line. It consists of 2^n inputs and 1 output. The input data lines are controlled by n selection lines.

VHDL Code:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity MUX is
port (Sel : in std_logic_vector(1 downto 0);  A,
B, C, D : in std_logic; Z
: out std_logic );
end MUX;

architecture Behavioral of MUX is begin
process (Sel, A, B, C, D)
begin if (Sel = "00") then Z<=
A;  elsif (Sel = "01") then Z<=
B;
elsif (Sel = "10") then Z<= C;
else Z<= D;
end if ; end
process ;
end Behavioral;
```

Output waveform:



RESULT: Design and Simulation of 4:1 Multiplexer using VHDL program on Xilinx ISE software has been done and the waveform were plotted successfully.

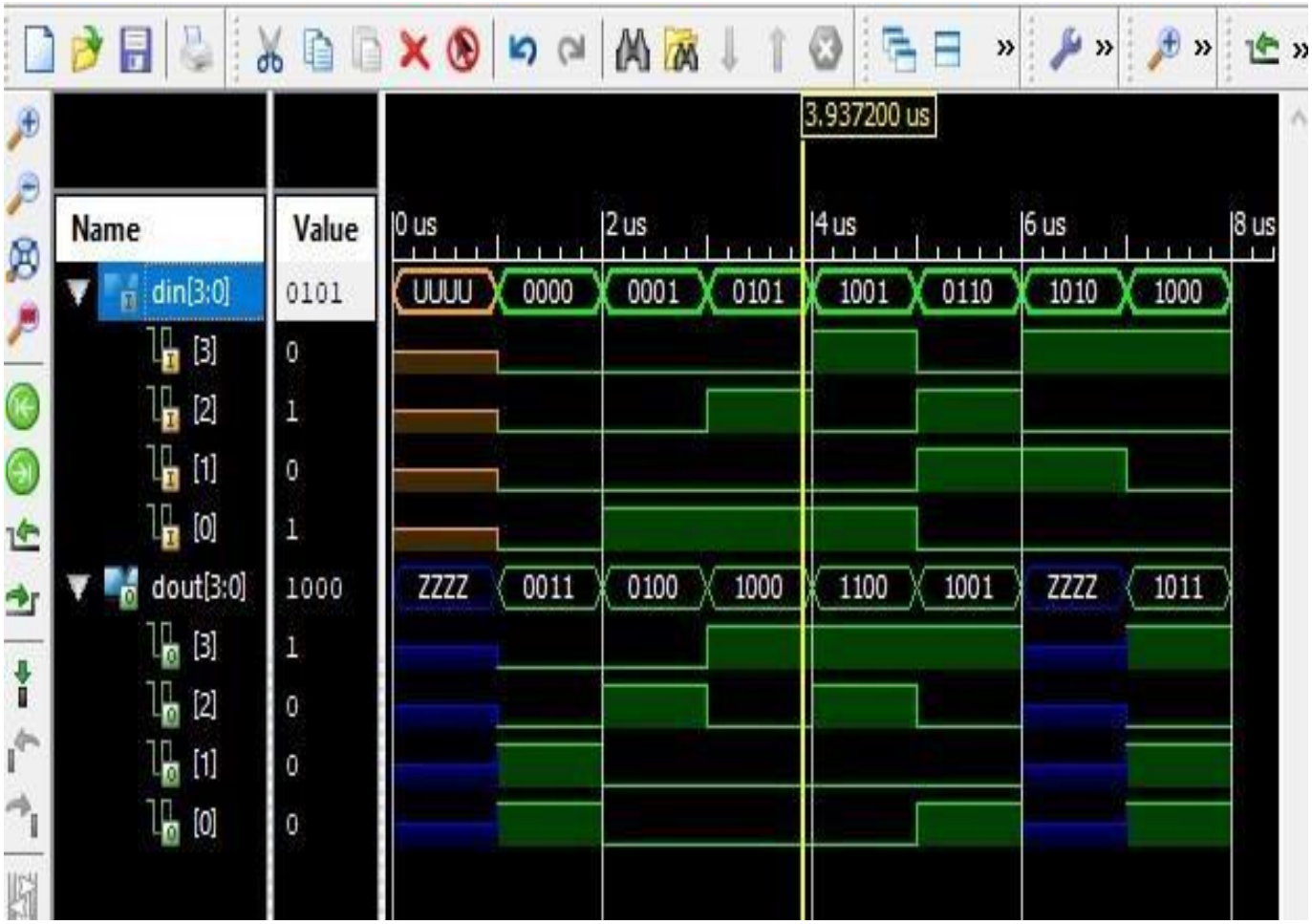
EXPERIMENT-12

OBJECTIVE: Design and Simulation of BCD to Excess-3 code using VHDL program module.
SOFTWARE REQUIRED: Xilinx ISE
THEORY: The Excess-3 binary code is an example of a self-complementary BCD code. A selfcomplementary binary code is a code which is always complimented in itself.
The process of converting BCD to Excess-3 is quite simple from other conversions. The Excess3 code can be calculated by adding 3, i.e., 0011 to each four-digit BCD code. Below is the truth table for the conversion of BCD to Excess-3 code. In the below table, the variables A, B, C, and D represent the bits of the binary numbers.

VHDL Code:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity BCDtoExcess3 is
port(
        din : in STD_LOGIC_VECTOR(3 downto 0);
dout : out STD_LOGIC_VECTOR(3 downto 0)
        );
end BCDtoExcess3;

architecture Behavioral of BCDtoExcess3 is

begin with din select      dout
<= "0011" when "0000",
"0100" when "0001",
            "0101" when "0010",
            "0110" when "0011",
"0111" when "0100",
            "1000" when "0101",
            "1001" when "0110",
            "1010" when "0111",
            "1011" when "1000",
            "1100" when "1001",
            "ZZZZ" when others;

end Behavioral;
```

Output Waveform:



RESULT: Design and Simulation of BCD to Excess-3 code converter using VHDL program on Xilinx ISE software has been done and the waveform were plotted successfully.

EXPERIMENT NO-13

OBJECTIVE: Design and Simulation of 3 to 8 decoder using VHDL program module

SOFTWARE REQUIRED: Xilinx ISE

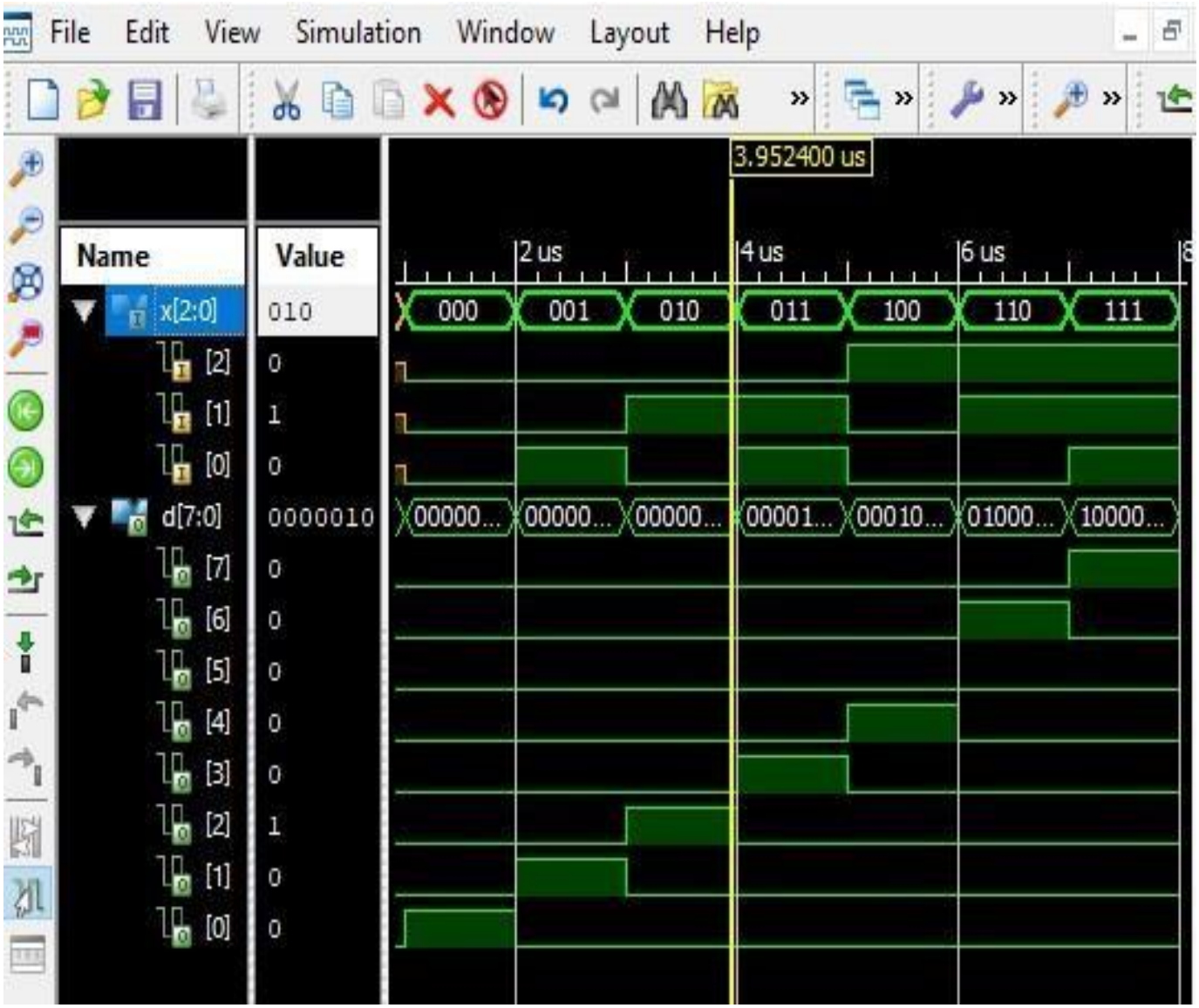
THEORY: The conversion of binary to decimal can be done using a device namely a decoder. Decoder is a combinational circuit that has 'n' input lines and maximum of 2^n output lines. One of these outputs will be active High based on the combination of inputs present, when the decoder is enabled. That means decoder detects a particular code

Inputs			Outputs							
X	Y	Z	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0	0	0	**1**	0	0	0	0	0	0	0
0	0	1	0	**1**	0	0	0	0	0	0
0	1	0	0	0	**1**	0	0	0	0	0
0	1	1	0	0	0	**1**	0	0	0	0
1	0	0	0	0	0	0	**1**	0	0	0
1	0	1	0	0	0	0	0	**1**	0	0
1	1	0	0	0	0	0	0	0	**1**	0
1	1	1	0	0	0	0	0	0	0	**1**

VHDL Code:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity Decoder is
Port ( x : in STD_LOGIC_VECTOR (2 downto 0);
D : out STD_LOGIC_VECTOR (7 downto 0)); end
Decoder;

architecture Behavioral of Decoder is begin
with x select
D<="00000001" when "000",
"00000010" when "001",
"00000100" when "010",
"00001000" when "011",
"00010000" when "100",
"00100000" when "101",
"01000000" when "110",
"10000000" when "111",
"00000000" when others;

end Behavioral;
```

Output Waveform:



RESULT: Design and Simulation of 3:8 decoder using VHDL program on Xilinx ISE software has been done and the waveform were plotted successfully.

EXPERIMENT NO-14

OBJECTIVE: Design and Simulation of JK Flip-flop using VHDL program module

SOFTWARE REQUIRED: Xilinx ISE

THEORY: A JK flip-flop is a sequential bi-state single-bit memory device named after its inventor by Jack Kil**.** In general, it has one clock input pin (CLK), two data input pins (J and K), and two output pins (Q and $\overline{Q}$) as shown in Figure 1. The JK Flip-Flop is a type of flipflop that can be set, reset, and toggled.

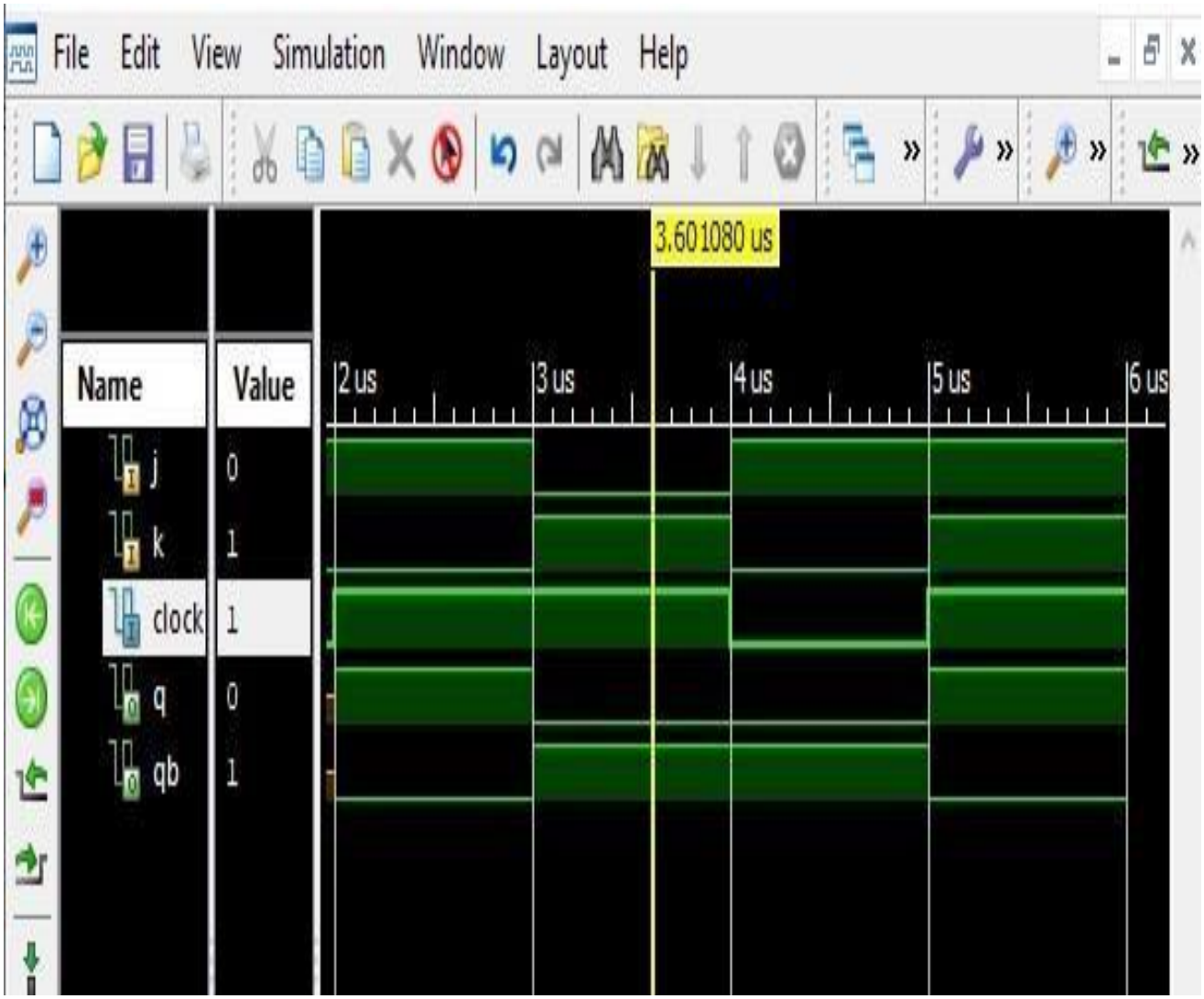
Truth Table of JK Flip-Flop:

CLK	J	K	Q_{n+1}	State
1	0	0	Q_n	NO CHANGE
1	0	1	0	RESET
1	1	0	1	SET
1	1	1	$\overline{Q}_n$	TOGGLES

VHDL Code:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity JKFlipFlop is PORT(
J,K,CLOCK: in std_logic; Q, QB:
out std_logic);
end JKFlipFlop;

architecture Behavioral of JKFlipFlop is
begin
PROCESS(CLOCK)
variable TMP: std_logic; begin
if(CLOCK='1' and CLOCK'EVENT) then
if(J='0' and K='0')then
TMP:=TMP;
elsif(J='1' and K='1')then TMP:=
not TMP;
elsif(J='0' and K='1')then
TMP:='0';
else
TMP:='1'; end
if; end
if;
Q<=TMP;  QB
<=not TMP;
end PROCESS;

end Behavioral;
```

Output Waveform:



RESULT: Design and Simulation of JK flip flop using VHDL program on Xilinx ISE software has been done and the waveform were plotted successfully.

EXPERIMENT NO-15

OBJECTIVE: Design and Simulation of CMOS Inverter using verilog Module

SOFTWARE REQUIRED: Xilinx ISE

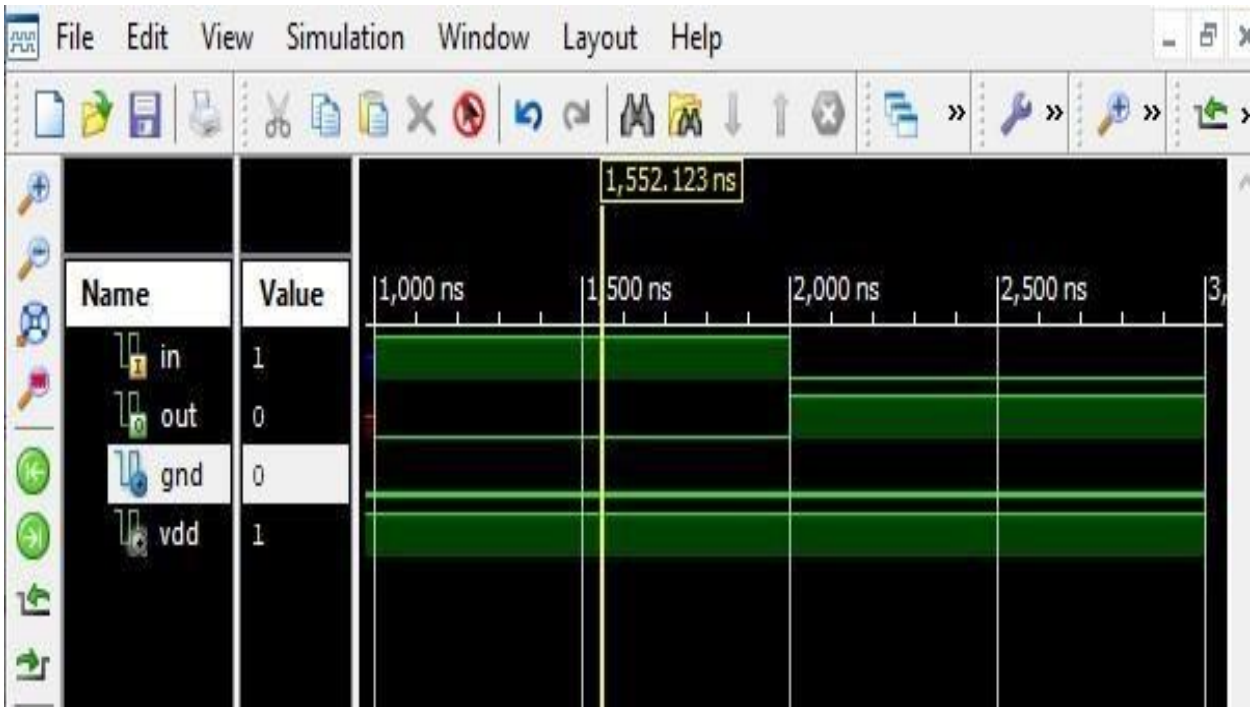
THEORY: The term CMOS stands for complementary metal oxide semiconductor. The basic structure of a Complementary Metal oxide semiconductor inverter consists of an n-MOS transistor and p-MOS transistor as a load and the gates of the two transistors are shorted at the input and the drains of the two transistors are also shorted where the output is obtained.

Working operation of CMOS inverter: When the low input voltage is given to the CMOS inverter, then the PMOS transistor is switched ON whereas the NMOS transistor will switch OFF and produce high logic output voltage. Similarly, when the high input voltage is given to the CMOS inverter then, the PMOS transistor is switched OFF whereas the NMOS transistor will be switched ON and produce low logic output voltage.

Verilog Code:

```
module CMOS(input wire in, output wire out);
supply0 gnd; //Define ground line
   supply1 vdd; //Define supply line

   pmos (out, vdd, in); //Two transistor inverter
nmos (out, gnd, in); //  endmodule
```

Output Waveform:



RESULT: Design and Simulation of CMOS inverter using Verilog module on Xilinx ISE software has been done and the waveform were plotted successfully.